Université de Rennes

USTH

Lab - Practice

Advanced computer architectures

Bachelor ICT – USTH
2022-2023

Daniel.Chillet@irisa.fr
Daniel.Chillet@univ-rennes1.fr

informatiques mathématiques

UMR IRISA

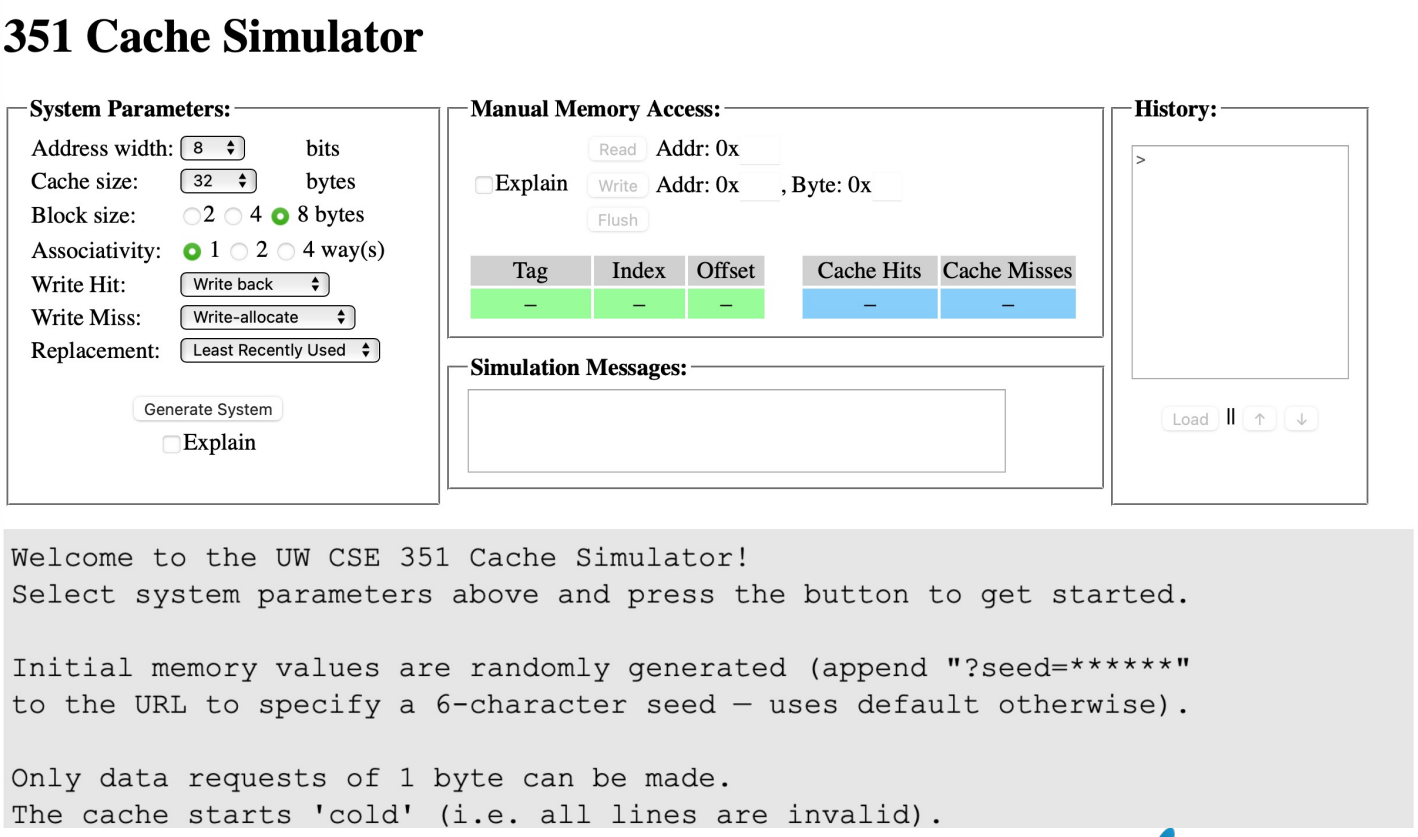
UMR IRISA

Lab Introduction

- Objectives
  - Use several cache simulators to understand how cache memories work
    - Low level simulator: 351 Cache simulator
    - Medium level simulator: Dinero IV cache simulator
    - High level simulation: C codes

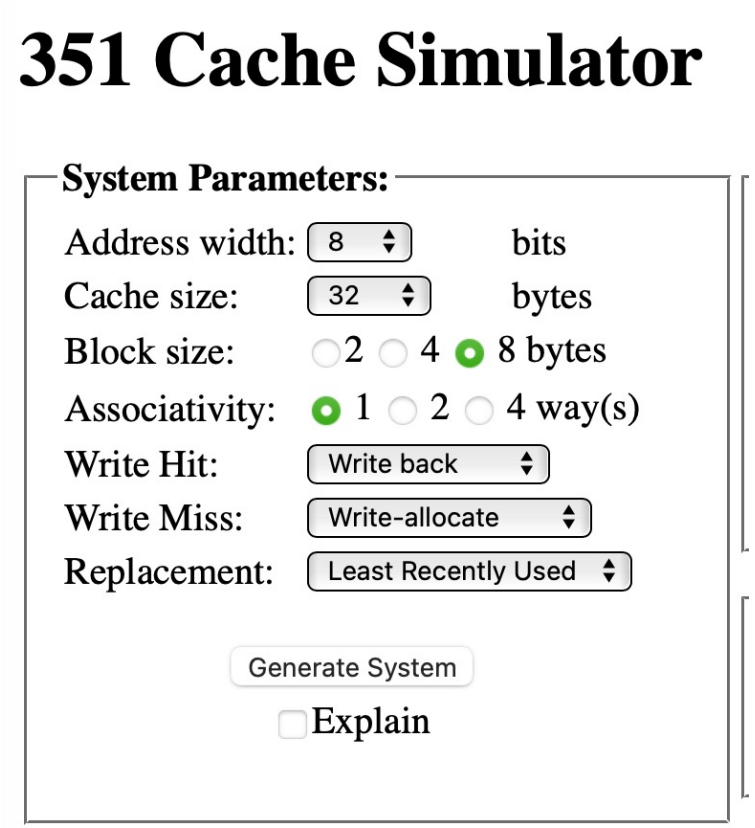
Low level simulator

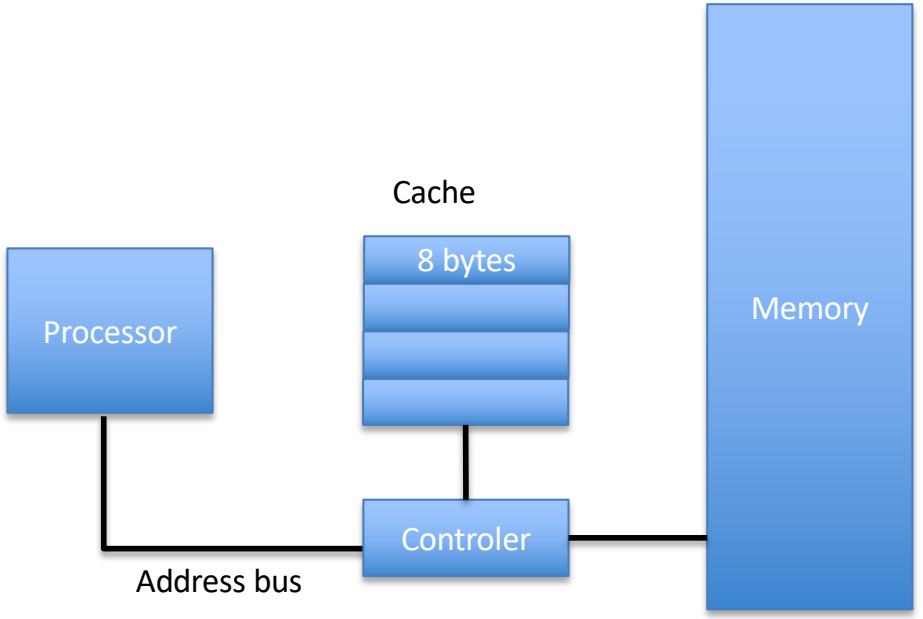
- Connect on the following web page
  - https://courses.cs.washington.edu/courses/cse351/cachesim/



Low level simulator

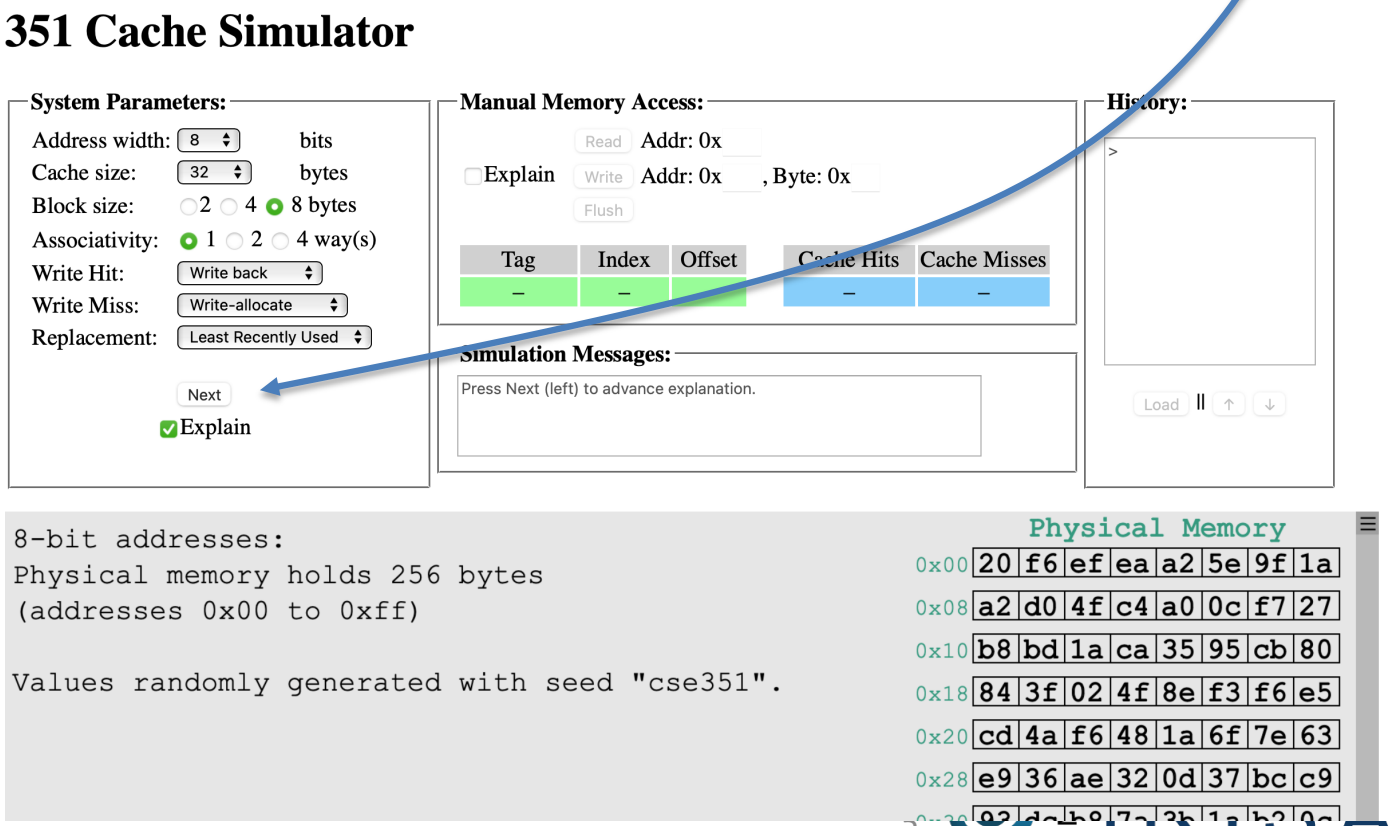
- Connect on the following web page
  - https://courses.cs.washington.edu/courses/cse351/cachesim/





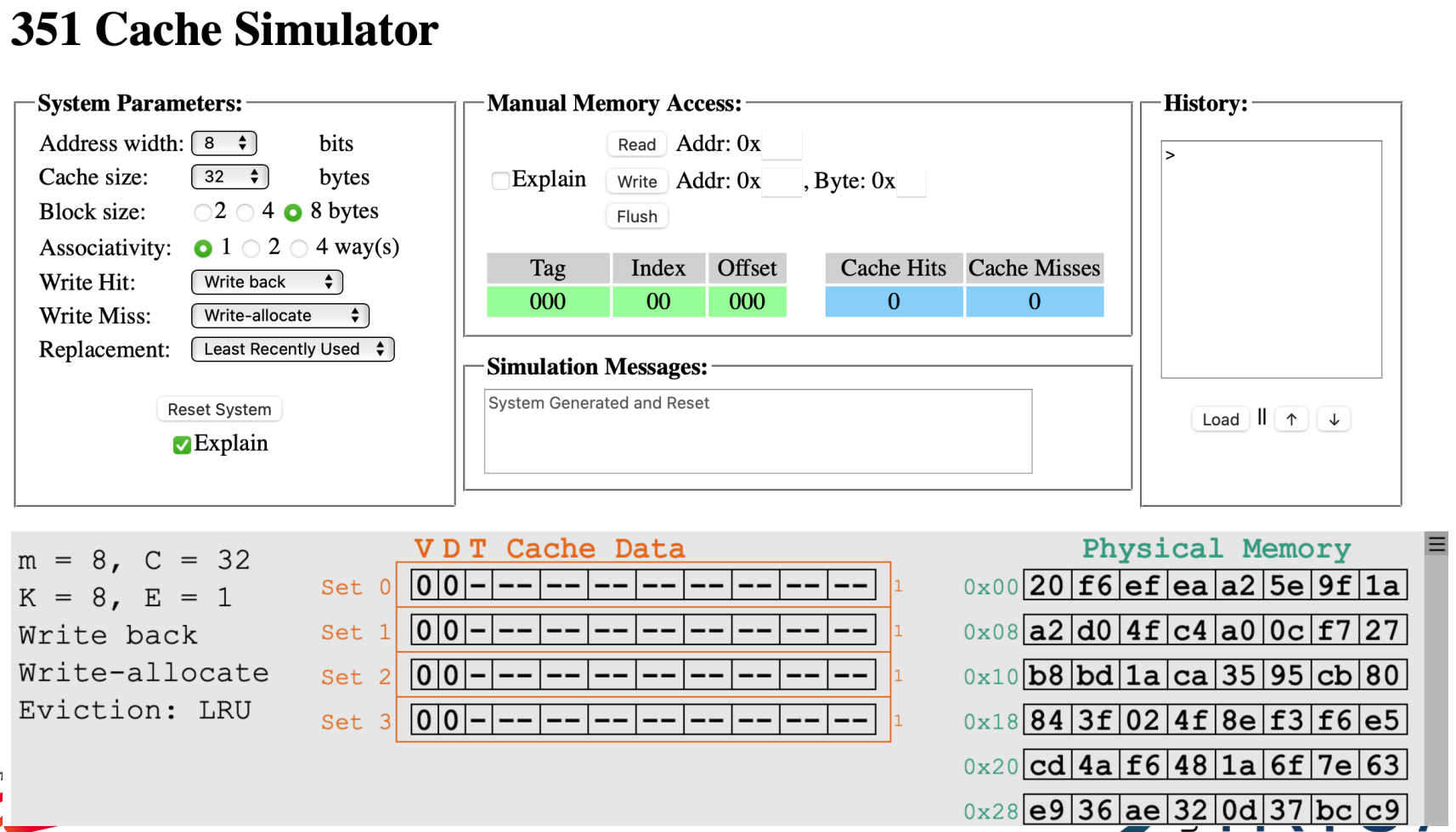
Low level simulator

- Click on « Explain button »
- Then click on button « Generate System » / « Next »
- Observe what is happenning on the simulator (step by step)



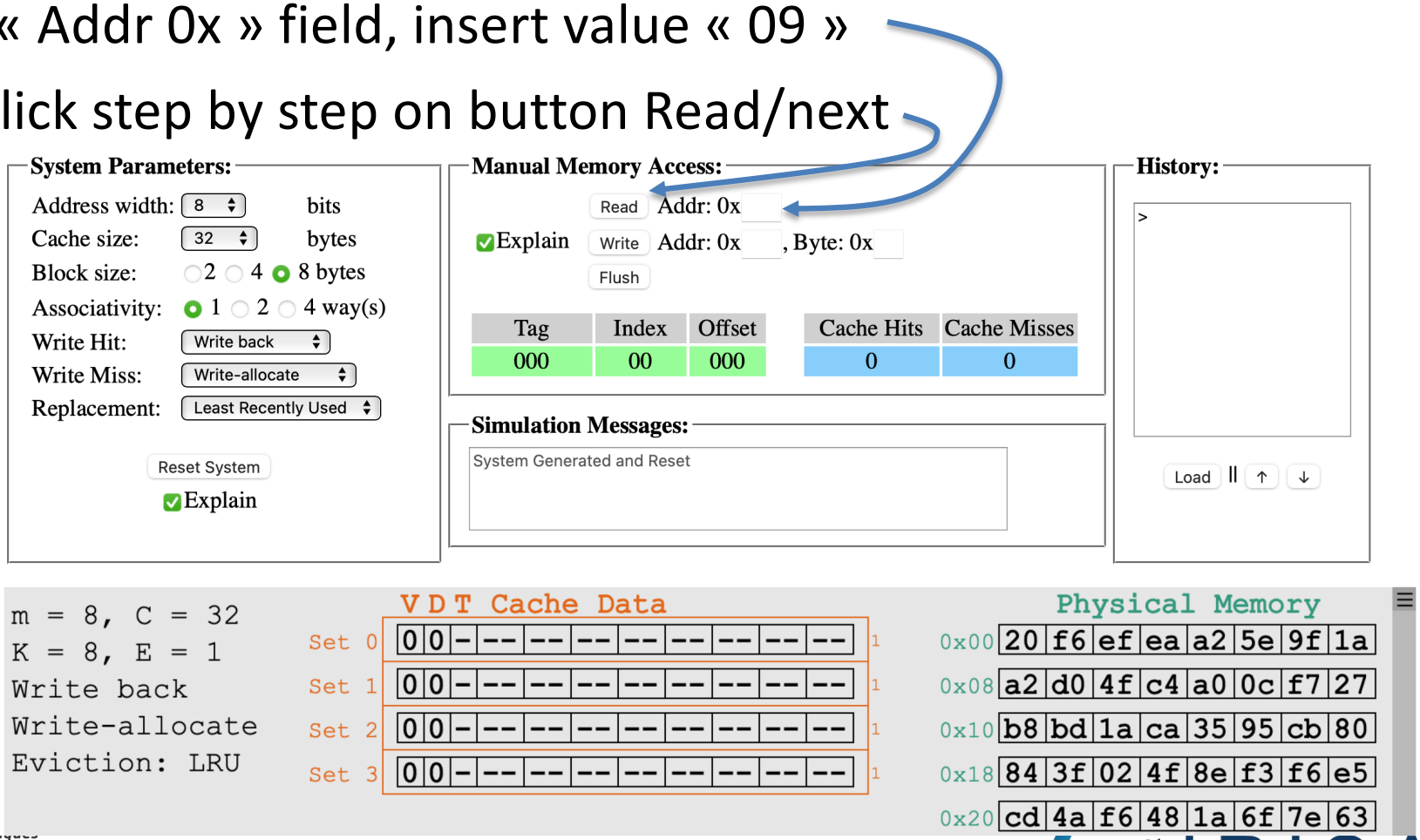
Low level simulator

- You are supposed to obtain this



Low level simulator

- Validate the button « Explain »
- In the « Addr 0x » field, insert value « 09 »
- Then click step by step on button Read/next



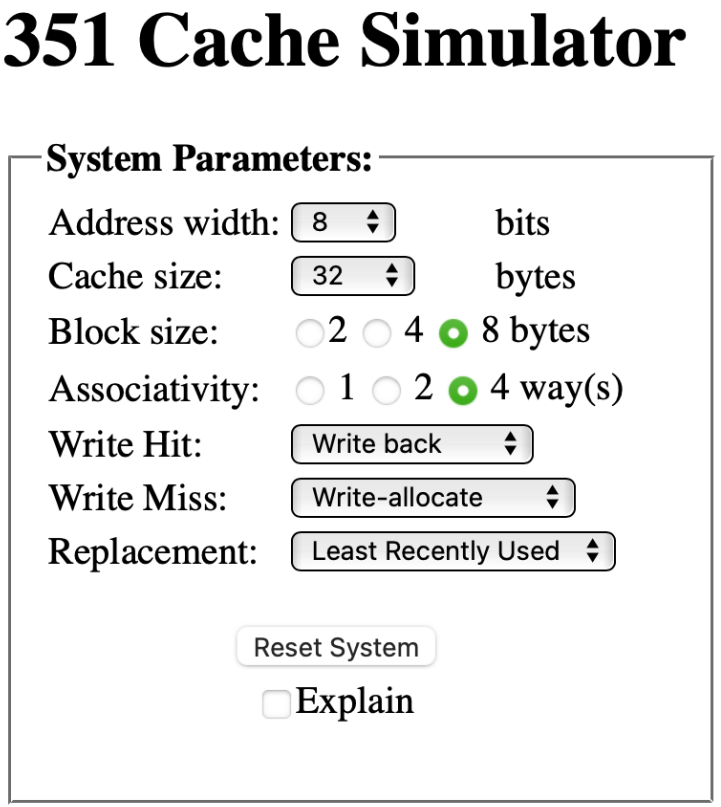
Low level simulator

- After executing step by step the read to address 0x09, do the following simulations
  - Execute a Read memory request to address 0x13
  - Execute a Read memory request to address 0x21
  - Execute a Read memory request to address 0x2a
  - Execute a Read memory request to address 0x15
  - Execute a Write memory request to address 0x11
  - Execute a Read memory request to address 0x33
  - Execute a Read Memory request to address 0x11

  - For each request execution, analyse the execution (step by step)
    - How many cache hits, cache misses ?
    - Analyse where the blocks are loaded in the cache
    - Analyse the write policy
    - Etc …

Low level simulator

- Modification of cache configuration
  - Change cache size: 32 bytes
  - Change Associativity: 4 ways
  - Analyse the cache structure
  - Then, analyse what is happenning if you apply the same list of memory requests
    - Execute a Read memory request to address 0x13
    - Execute a Read memory request to address 0x21
    - Execute a Read memory request to address 0x2a
    - Execute a Read memory request to address 0x15
    - Execute a Write memory request to address 0x11
    - Execute a Read memory request to address 0x33
    - Execute a Read Memory request to address 0x11
  - What is the performance of this cache configuration compare to the first one ?
    - How many cache hits, cache misses ?
    - Analyse where the blocks are loaded in the cache
    - Analyse the write policy
    - Etc …



Low level simulator

- Modification of cache configuration
  - Change cache size: 32 bytes
  - Change Associativity: 2 ways
  - Analyse the cache structure
  - Then, analyse what is happenning if you apply the same list of memory requests
    - Execute a Read memory request to address 0x13
    - Execute a Read memory request to address 0x21
    - Execute a Read memory request to address 0x2a
    - Execute a Read memory request to address 0x15
    - Execute a Write memory request to address 0x11
    - Execute a Read memory request to address 0x33
    - Execute a Read Memory request to address 0x11
  - What is the performance of this cache configuration compare to the first one ?
    - How many cache hits, cache misses ?
    - Analyse where the blocks are loaded in the cache
    - Analyse the write policy
    - Etc …