

# Practice + project

Advanced computer architectures

Bachelor ICT – USTH  
2022-2023

[Daniel.Chillet@irisa.fr](mailto:Daniel.Chillet@irisa.fr)

Daniel.Chillet@univ-rennes1.fr

# First simulation

- Cache memory organisation
  - Connect on
    - <https://cairn.enssat.fr/enseignements/Archi/SimuleCache/>
  - You are supposed to obtain this window

Configuration of the cache simulator

Clic on the blue lines to open the configuration zones

General configuration

Simulate

Show the access trace : ☐ Oui ; ☒ Non

Configuration of the number of levels of caches

Cache level 1 unified : ☒ Yes ; ☐ No  
Cache level 2 unified : ☒ yes ; ☐ No  
Cache level 3 unified : ☒ Yes ; ☐ No

Main Memory size :   
Main memory time access :  ns  
Memory access trace :  aucun fichier sélectionné

Level 1 Cache Configuration

Level 2 Cache Configuration

Level 3 Cache Configuration

Simulate

# First simulation

- Define the following configuration

- Show access trace: yes
- Nb Levels: 1
- Level L1: Unified cache
- Memory: 1kmots
- Access time: 100ns
- For Data cache
- Cache size: 128
- Block size : 16 mots/bytes
- Access time: 10ns
- Associativity : Complete
- Write policy : LRU
- Allocation policy : write allocate
- For Instruction cache
- No configuration, because no instruction cache

Configuration of the cache simulator

Clic on the blue lines to open the configuration zones

General configuration

Simulate

Show the access trace : ☒ Oui ; ☐ Non

Configuration of the number of levels of caches : 1

Cache level 1 unified : ☒ Yes ; ☐ No  
 Cache level 2 unified : ☒ yes ; ☐ No  
 Cache level 3 unified : ☒ Yes ; ☐ No

Main Memory size : 1 kmots  
 Main memory time access : 100 ns  
 Memory access trace : Choisir le fichier aucun fichier sélectionné

Level 1 Cache Configuration

Data cache or unified cache :

Cache size : 128 mots  
 Block size : 16 mots  
 Cache access time : 10 ns  
 Associativity : ☐ Direct associativity ; ☒ Completely associative ; ☐ n Ways associative nb ways  
 Replacement policy : ☐ FIFO ; ☒ LRU ; ☐ Random  
 Write policy : ☒ Write back ; ☐ Write through  
 Allocation policy for write : ☒ Write allocate ; ☐ Write no allocate

Instruction cache :

Cache size : mots  
 Block size : mots  
 Cache access time : ns  
 Associativity : ☐ Direct associativity ; ☐ Completely associative ; ☐ n Ways associative nb ways  
 Replacement policy : ☒ FIFO ; ☐ LRU ; ☐ Random

Level 2 Cache Configuration

Daniel Chillet

Level 3 Cache Configuration

Simulate

# First simulation

- Cache memory organisation
  - Memory access trace
    - MemoryTraceExample.mem
  - Click on « Validate »
  - Analyse the results
  - Conclusions

Configuration of the cache simulator

Clic on the blue lines to open the configuration zones

General configuration

Simulate

Show the access trace : ☒ Oui ; ☐ Non

Configuration of the number of levels of caches

Cache level 1 unified : ☒ Yes ; ☐ No  
Cache level 2 unified : ☒ yes ; ☐ No  
Cache level 3 unified : ☒ Yes ; ☐ No

Main Memory size :  kmots  
Main memory time access :  ns  
Memory access trace :  aucun fichier sélectionné

Level 1 Cache Configuration

Data cache or unified cache :  
Cache size :  mots  
Block size :  mots  
Cache access time :  ns  
Associativity : ☐ Direct associativity ; ☒ Completely associative ; ☐ n Ways associative  nb ways  
Replacement policy : ☐ FIFO ; ☒ LRU ; ☐ Random  
Write policy : ☒ Write back ; ☐ Write through  
Allocation policy for write : ☒ Write allocate ; ☐ Write no allocate

Instruction cache :  
Cache size :  mots  
Block size :  mots  
Cache access time :  ns  
Associativity : ☒ Direct associativity ; ☐ Completely associative ; ☐ n Ways associative  nb ways  
Replacement policy : ☒ FIFO ; ☐ LRU ; ☐ Random

Level 2 Cache Configuration

Level 3 Cache Configuration

Simulate

# Second simulation

- Cache memory organisation
  - Use ProdMat.s to extract memory access trace
    - Extract only data accesses
    - Use SJimVEM to execute the code, and to extract memory access trace
- Then, you can use the cache simulator
  - <https://cairn.enssat.fr/enseignements/Archi/SimuleCache/>



# Second simulation

- Cache memory organisation
  - Simulate cache memory with the following parameters
    - One level of cache
    - Unified cache (for L1)
    - L1 cache
      - Cache size 128 words (mots)
      - Cache blocks size 4 words
      - Replacement policy : LRU
      - Associativity : Direct
      - Allocation policy : write allocate
      - Cache access time = 10 ns
      - Memory Access time = 100 ns
  - What is the number of defaults ? Miss ?
  - What is the number of hits ?
  - What is the miss time ? Hit time ?
  - What is the total time of memory access ?
    - For total nb of misses + total nb of hits

# Third simulation

- Cache memory organisation
  - Change the block size to 8 words
    - What are the modifications ?
      - nb of misses/hits → Given by simulator
      - Time of miss, time of hit ? → To compute
  - Change the block size to 16 words
    - What are the modifications ?
      - nb of misses/hits → Given by simulator
      - Time of miss, time of hit ? → To compute

# Fourth simulation

- Cache memory organisation
  - Change the associativity, Complete associativity
  - And redo the previous simulations
    - What are the modifications ?
      - nb of misses/hits  Given by simulator
      - Time of miss, time of hit ?  To compute



ProdMat.s

