Université de Rennes

USTH

Practice + project

Advanced computer architectures

Bachelor ICT – USTH
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Inria informatiques mathématiques

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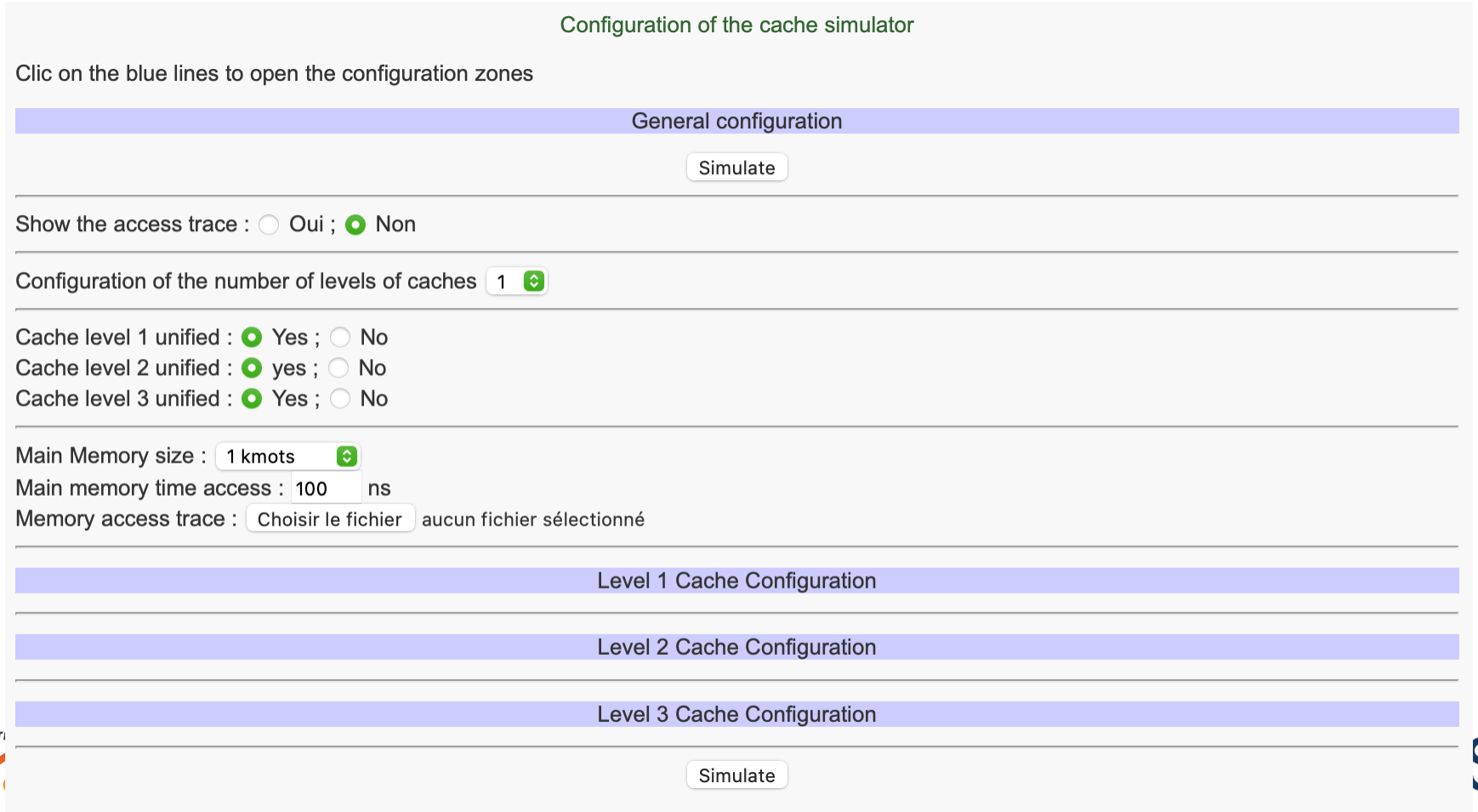
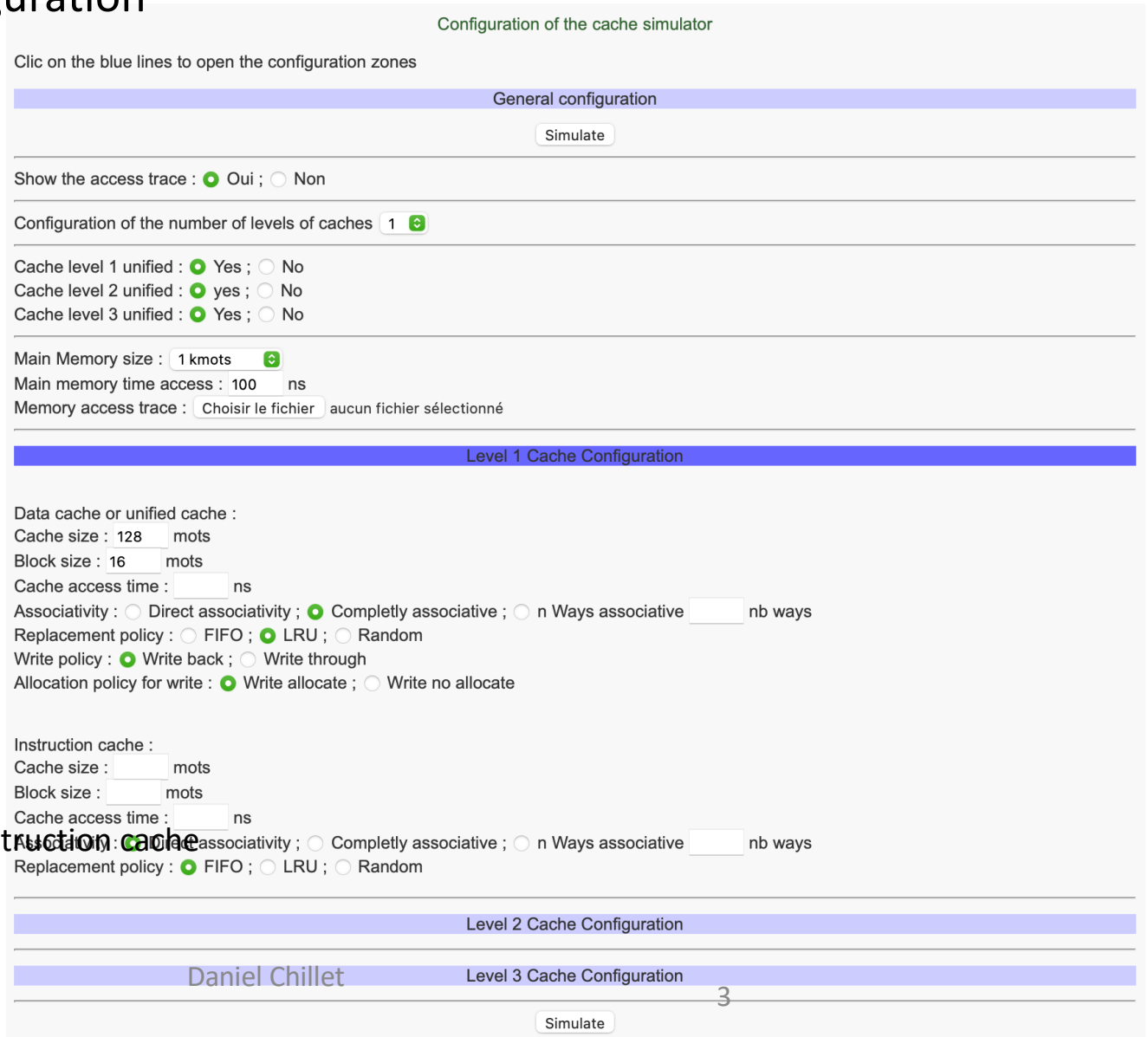
First simulation

- Cache memory organisation
  - Connect on
    - https://cairn.enssat.fr/enseignements/Archi/SimuleCache/
  - You are supposed to obtain this window



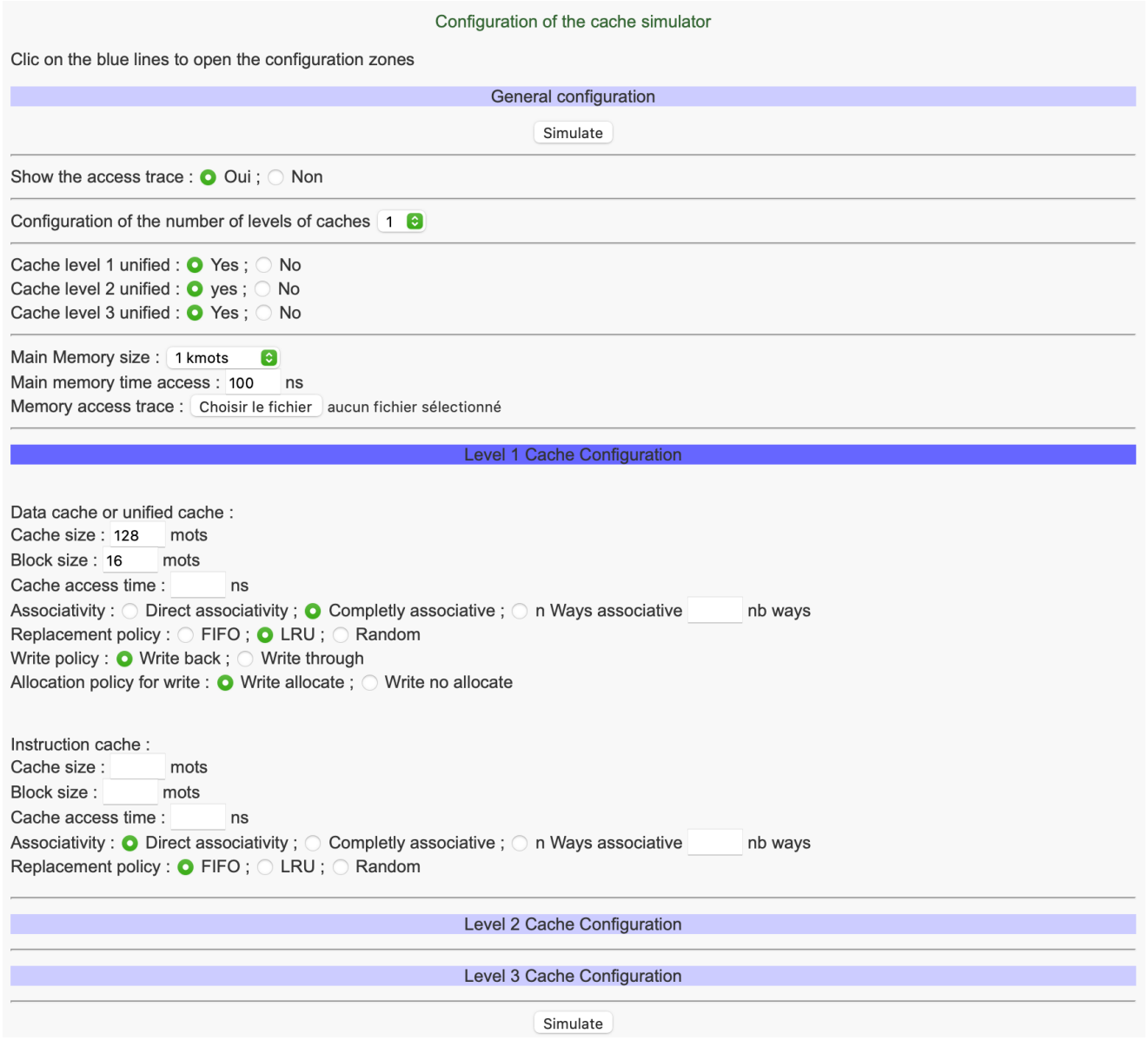
First simulation

- Define the following configuration
  - Show access trace: yes
  - Nb Levels: 1
  - Level L1: Unified cache
  - Memory: 1kmots
  - Access time: 100ns
  - For Data cache
  - Cache size: 128
  - Block size : 16 mots/bytes
  - Access time: 10ns
  - Associativity : Complete
  - Write policy : LRU
  - Allocation policy : write allocate
  - For Instruction cache
  - No configuration, because no instruction cache



First simulation

- Cache memory organisation
  - Memory access trace
    - MemoryTraceExample.mem
  - Click on « Validate »
  - Analyse the results
  - Conclusions



Second simulation

- Cache memory organisation
  - Use ProdMat.s to extract memory access trace
    - Extract only data accesses
    - Use SJimVEM to execute the code, and to extract memory access trace

- Then, you can use the cache simulator
  - https://cairn.enssat.fr/enseignements/Archi/SimuleCache/

Second simulation

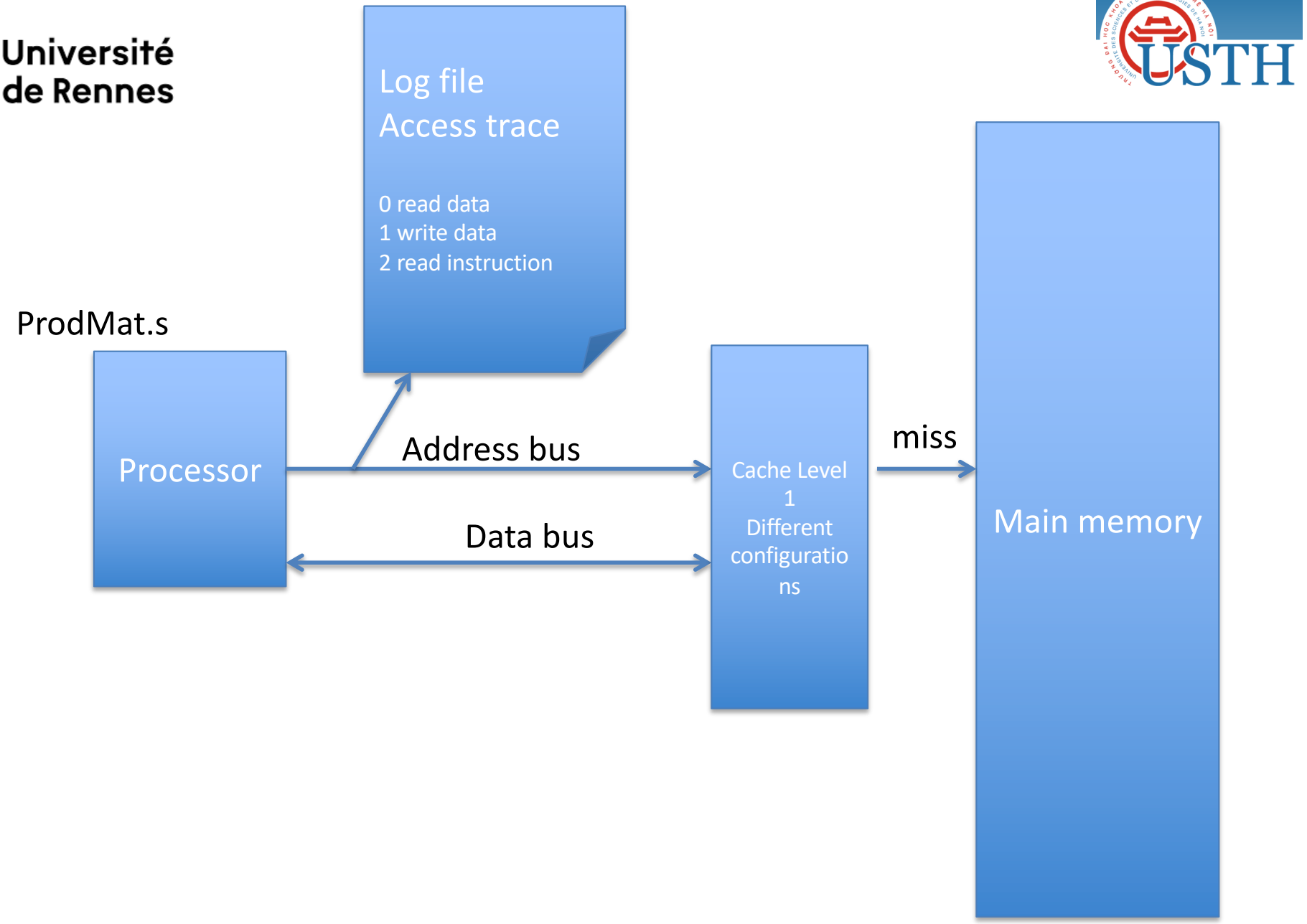
- Cache memory organisation
  - Simulate cache memory with the following parameters
    - One level of cache
    - Unified cache (for L1)
    - L1 cache
      - Cache size 128 words (mots)
      - Cache blocks size 4 words
      - Replacement policy : LRU
      - Associativity : Direct
      - Allocation policy : write allocate
      - Cache access time = 10 ns
      - Memory Access time = 100 ns
  - What is the number of defaults ? Miss ?
  - What is the number of hits ?
  - What is the miss time ? Hit time ?
  - What is the total time of memory access ?
    - For total nb of misses + total nb of hits

Third simulation

- Cache memory organisation
  - Change the block size to 8 words
    - What are the modifications ?
      - nb of misses/hits → Given by simulator
      - Time of miss, time of hit ? → To compute
  - Change the block size to 16 words
    - What are the modifications ?
      - nb of misses/hits → Given by simulator
      - Time of miss, time of hit ? → To compute

Fourth simulation

- Cache memory organisation
  - Change the associativity, Complete associativity
  - And redo the previous simulations
    - What are the modifications ?
      - nb of misses/hits → Given by simulator
      - Time of miss, time of hit ? → To compute


Log file
Access trace
0 read data
1 write data
2 read instruction
ProdMat.s
Processor
Address bus
Data bus
Cache Level 1
Different configuratio ns
miss
Main memory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