

Lab - Practice

Advanced computer architectures

Bachelor ICT – USTH
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Daniel.Chillet@irisa.fr

Daniel.Chillet@univ-rennes1.fr

Lab Introduction

- Objectives
 - Use several cache simulators to understand how cache memories work
 - Low level simulator: 351 Cache simulator
 - Medium level simulator: Dinero IV cache simulator
 - High level simulation: C codes

Low level simulator

- Connect on the following web page
 - <https://courses.cs.washington.edu/courses/cse351/cachesim/>

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☒ 1 ☐ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☐ Explain

Manual Memory Access:

Addr: 0x

☐ Explain Addr: 0x , Byte: 0x

Tag	Index	Offset	Cache Hits	Cache Misses
–	–	–	–	–

Simulation Messages:

History:

Welcome to the UW CSE 351 Cache Simulator!

Select system parameters above and press the button to get started.

Initial memory values are randomly generated (append "?seed=*****" to the URL to specify a 6-character seed – uses default otherwise).

Only data requests of 1 byte can be made.

The cache starts 'cold' (i.e. all lines are invalid).

Low level simulator

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 - <https://courses.cs.washington.edu/courses/cse351/cachesim/>

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

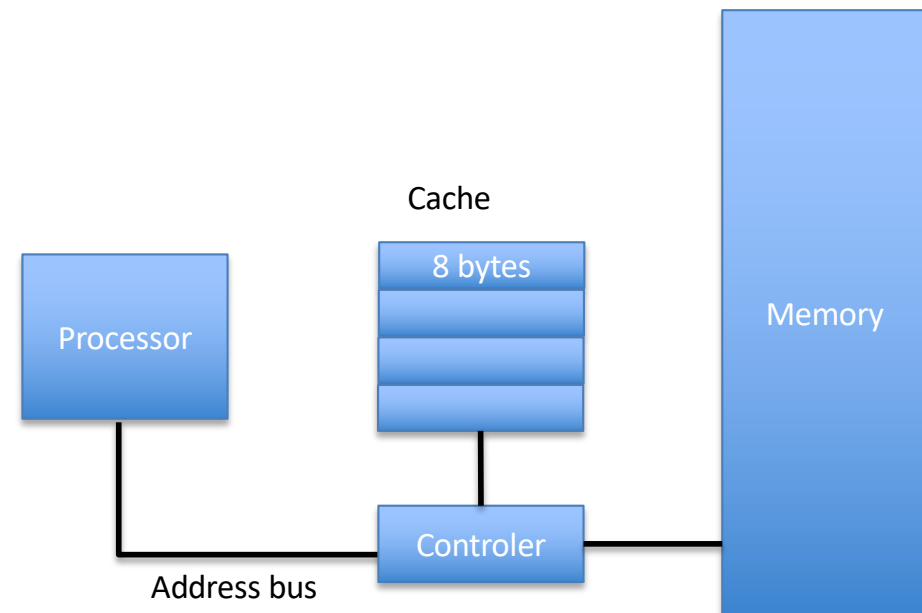
Associativity: ☒ 1 ☐ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☐ Explain



Low level simulator

- Click on « Explain button »
- Then click on button « Generate System » / « Next »
- Observe what is happening on the simulator (step by step)

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☒ 1 ☐ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

Manual Memory Access:

Addr: 0x

Addr: 0x, Byte: 0x

Tag	Index	Offset	Cache Hits	Cache Misses
-	-	-	-	-

History:

Simulation Messages:

Press Next (left) to advance explanation.

8-bit addresses:

Physical memory holds 256 bytes
(addresses 0x00 to 0xff)

Values randomly generated with seed "cse351".

Physical Memory

0x00	20	f6	ef	ea	a2	5e	9f	1a
0x08	a2	d0	4f	c4	a0	0c	f7	27
0x10	b8	bd	1a	ca	35	95	cb	80
0x18	84	3f	02	4f	8e	f3	f6	e5
0x20	cd	4a	f6	48	1a	6f	7e	63
0x28	e9	36	ae	32	0d	37	bc	c9

Low level simulator

- You are supposed to obtain this

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☒ 1 ☐ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☒ Explain

Manual Memory Access:

Addr: 0x

☐ Explain Addr: 0x , Byte: 0x

Tag	Index	Offset	Cache Hits	Cache Misses
000	00	000	0	0

Simulation Messages:

System Generated and Reset

History:

m = 8, C = 32

K = 8, E = 1

Write back

Write-allocate

Eviction: LRU

V D T Cache Data	
Set 0	0 0 - - - - - - - - - - 1
Set 1	0 0 - - - - - - - - - - 1
Set 2	0 0 - - - - - - - - - - 1
Set 3	0 0 - - - - - - - - - - 1

Physical Memory	
0x00	20 f6 ef ea a2 5e 9f 1a
0x08	a2 d0 4f c4 a0 0c f7 27
0x10	b8 bd 1a ca 35 95 cb 80
0x18	84 3f 02 4f 8e f3 f6 e5
0x20	cd 4a f6 48 1a 6f 7e 63
0x28	e9 36 ae 32 0d 37 bc c9

Low level simulator

- Validate the button « Explain »
- In the « Addr 0x » field, insert value « 09 »
- Then click step by step on button Read/next

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☒ 1 ☐ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☒ Explain

Manual Memory Access:

Addr: 0x

☒ Explain Addr: 0x , Byte: 0x

Tag	Index	Offset	Cache Hits	Cache Misses
000	00	000	0	0

Simulation Messages:

System Generated and Reset

History:

>

m = 8, C = 32

K = 8, E = 1

Write back

Write-allocate

Eviction: LRU

V D T Cache Data

Set	0	1	2	3
00	--	--	--	--
00	--	--	--	--
00	--	--	--	--
00	--	--	--	--

Physical Memory

0x00	20	f6	ef	ea	a2	5e	9f	1a
0x08	a2	d0	4f	c4	a0	0c	f7	27
0x10	b8	bd	1a	ca	35	95	cb	80
0x18	84	3f	02	4f	8e	f3	f6	e5
0x20	cd	4a	f6	48	1a	6f	7e	63

Low level simulator

- After executing step by step the read to address 0x09, do the following simulations
 - Execute a Read memory request to address 0x13
 - Execute a Read memory request to address 0x21
 - Execute a Read memory request to address 0x2a
 - Execute a Read memory request to address 0x15
 - Execute a Write memory request to address 0x11
 - Execute a Read memory request to address 0x33
 - Execute a Read Memory request to address 0x11
- For each request execution, analyse the execution (step by step)
 - How many cache hits, cache misses ?
 - Analyse where the blocks are loaded in the cache
 - Analyse the write policy
 - Etc ...

Low level simulator

- Modification of cache configuration
 - Change cache size: 32 bytes
 - Change Associativity: 4 ways
 - Analyse the cache structure
 - Then, analyse what is happening if you apply the same list of memory requests
 - Execute a Read memory request to address 0x13
 - Execute a Read memory request to address 0x21
 - Execute a Read memory request to address 0x2a
 - Execute a Read memory request to address 0x15
 - Execute a Write memory request to address 0x11
 - Execute a Read memory request to address 0x33
 - Execute a Read Memory request to address 0x11
 - What is the performance of this cache configuration compare to the first one ?
 - How many cache hits, cache misses ?
 - Analyse where the blocks are loaded in the cache
 - Analyse the write policy
 - Etc ...

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☐ 1 ☐ 2 ☒ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☐ Explain

Low level simulator

- Modification of cache configuration
 - Change cache size: 32 bytes
 - Change Associativity: 2 ways
 - Analyse the cache structure
 - Then, analyse what is happening if you apply the same list of memory requests
 - Execute a Read memory request to address 0x13
 - Execute a Read memory request to address 0x21
 - Execute a Read memory request to address 0x2a
 - Execute a Read memory request to address 0x15
 - Execute a Write memory request to address 0x11
 - Execute a Read memory request to address 0x33
 - Execute a Read Memory request to address 0x11
 - What is the performance of this cache configuration compare to the first one ?
 - How many cache hits, cache misses ?
 - Analyse where the blocks are loaded in the cache
 - Analyse the write policy
 - Etc ...

351 Cache Simulator

System Parameters:

Address width: bits

Cache size: bytes

Block size: ☐ 2 ☐ 4 ☒ 8 bytes

Associativity: ☐ 1 ☒ 2 ☐ 4 way(s)

Write Hit:

Write Miss:

Replacement:

☐ Explain