LABFAT

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Course:Digital Logic Design

Course Code: ECE2003

Slot: L5+L6+L23+L24

Q)Write a Verilog code for a Mealy FSM having a single input line ‘x’ and a single output-line ’z’. An output of 1 is to be produced coincident with the pattern 0111and an output of ‘0’ is to be produced for all the other sequences. Simulate with a test bench.

Solution:

Verilog Code:

```
module MealyFSM(
  output reg y,
  input x_in,clock,reset
);
reg [2:0] state,next_state;
parameter S0=3'b000,S1=3'b001,S2=3'b010,S3=3'b011,S4=3'b100,S5=3'b101;

always @ (posedge clock,negedge reset)
if(reset==0) state<=S0;
else state<=next_state;
always @ (state,x_in)
case(state)
S0:if (~x_in) next_state=S1;else next_state=S0;
S1:if (x_in) next_state=S2;else next_state=S3;
S2:if (~x_in) next_state=S1;else next_state=S5;
S3:if (x_in) next_state=S2;else next_state=S4;
S4:if (x_in) next_state=S1;else next_state=S4;
S5:if (x_in) next_state=S0;else next_state=S1;
endcase
always @ (state,x_in)
case(state)
S0,S1,S2,S3:y=0;
S4: y=x_in;
```

```
S5: y=~x_in;
endcase
endmodule
```

Testbench Code:

```
`timescale 1s/100ms
`include "MealyFSM.v"

module MealyFSM_TB();
wire y;
reg t_x_in,t_clock,t_reset;
MealyFSM M0(y,t_x_in,t_clock,t_reset);
initial #190 $finish;
initial
begin
    $dumpfile("Mealy.vcd");
    $dumpvars(0,MealyFSM_TB);
    t_clock=0;
    forever #5 t_clock = ~t_clock;
end
initial fork
    t_x_in=0;
    t_reset=0;
#20 t_reset=1;
#30 t_x_in=0;
#40 t_x_in=1;
#50 t_x_in=1;
#60 t_x_in=0;
#70 t_x_in=0;
#80 t_x_in=0;
#90 t_x_in=1;
#100 t_x_in=1;
#110 t_x_in=0;
#120 t_x_in=0;
#130 t_x_in=0;
#140 t_x_in=1;
#150 t_x_in=1;
#160 t_x_in=0;
#170 t_x_in=0;
```

```
#180 t_x_in=0;
#190 t_x_in=1;
join
endmodule
```

Graph: