Experience of Using OpenROAD-flow-scripts on a ibex Design

***Abstract*— In this paper, we present our experience using OpenROAD-flow-scripts on a ibex design. OpenROAD is an open-source electronic design automation tool flow that can provide an end-to-end design implementation solution for the digital integrated circuit industry. The OpenROAD Flow Project aims for automated-in-the-loop digital circuit design with 24-hour turnaround time.**

Keywords—OpenROAD-flow-scripts, RTL-to-GDSII flow, open-source tools, automated design, no-human-in-the-loop

I. INTRODUCTION

OpenROAD-flow-scripts(ORFS) is a powerful toolset that is an automated flow from RTL-GDSII. The tool enables full RTL-GDSII flow using open-source tools. The flow will execute without human intervention. In this paper, we describe our experience of using ORFS on asap7 ibex design project aims to develop an open-source 24-hour no-human-in-the-loop RTL-GDSII flow.

IV.MODIFICATION DONE

In the asap7 ibex design we can changed following to achieve a design with good results and TNS/WNS to zero.

1. Update config.mk

```
export CTS_BUF_CELL = BUFx8_ASAP7_75t_R
```

2. Update constraint.sdc

```
set clk_io_pct 0.15
```

3. After running floorplan stage updated .sdc file with following set_false_path for the end-points which are TIE_LOW*, asynchronous clock path etc.,

```
set_false_path -to [get_ports {alert_major_o}]
set_false_path -to [get_ports {alert_minor_o}]
set_false_path -to [get_ports {instr_addr_o[0]}]
set_false_path -to [get_ports {instr_addr_o[1]}]
set_false_path -to [get_ports {data_addr_o[0]}]
set_false_path -to [get_ports {data_addr_o[1]}]

set_false_path -to [get_ports {rst_ni}]
set_false_path -from [get_pins _36182_/CLK]
set_false_path -from [get_pins _36313_/CLK]
```

```
. TIELOx1_ASAP7_75t_R _36327_ (
   .L(_18389_)
 );
 BUFx2_ASAP7_75t_R _36328_ (
   .A(_18389_),
   .Y(alert_major_o)
 );
 BUFx2_ASAP7_75t_R _36329_ (
   .A(_18389_),
   .Y(alert_minor_o)
 );
 BUFx2_ASAP7_75t_R _36330_ (
   .A(_18389_),
   .Y(data_addr_o[0])
 );
 BUFx2_ASAP7_75t_R _36331_ (
   .A(_18389_),
   .Y(data_addr_o[1])
 );
BUFx2_ASAP7_75t_R _36362_ (
   .A(_18389_),
   .Y(instr_addr_o[0])
 );
 BUFx2_ASAP7_75t_R _36363_ (
   .A(_18389_),
   .Y(instr_addr_o[1])
```

With Default configuration:

```
finish report_tns
--------------------------------
tns -296.50

================================
finish report_wns
--------------------------------
wns -92.38

================================
finish report_worst_slack
--------------------------------
worst slack -92.38

--------------------------------
```

After Updating IO_PCT/.sdc:

```
============================================================
finish report_tns
------------------------------------------------------------
tns 0.00

============================================================
finish report_wns
------------------------------------------------------------
wns 0.00

============================================================
finish report_worst_slack
------------------------------------------------------------
worst slack 135.65

------------------------------------------------------------
```

Detailed explanation available in following github repo: https://github.com/naveen17440/asap7_contest

VI. CONCLUSION

In conclusion, the log file captures all the timing reports with min/max/un-constrained paths. With default constraint setup, flow generates with all timing paths. The ports that are connected with TIELO* and asynchronous paths that are shown unconstrained are showing in all path group and some paths are violating. Actually those paths are not to consider for timing report, i.e., considered as false path.

So I request OpenROAD team can filter those TIELO*/async group path into false path, makes OpenSTA timing logs looks clean and improves timing report analysis easy for beginners and those coming from HW/SW background.

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