

# Experience of Using OpenROAD Flow Scripts on a ibex Design

**Abstract**— In this paper, we present our experience using OpenROAD Flow Scripts on a ibex design. OpenROAD is an open-source electronic design automation tool flow that can provides an end-to-end design implementation solution for the digital integrated circuit industry. The OpenROAD Flow Project aims for automated-in-the-loop digital circuit design with 24-hour turnaround time.

**Keywords**—OpenROAD Flow Scripts, RTL-to-GDSII flow, open-source tools, automated design, no-human-in-the-loop

## I. INTRODUCTION

OpenROAD Flow Scripts(ORFS) is a powerful toolset that is an automated flow from RTL-GDSII flow. The tool enables full RTL-GDSII flow using open-source tools. The open-source tool will execute the flow from RTL-GDS flow without human intervention. In this paper, we describe our experience of using ORFS on asap7 ibex design project aims to develop an open-source 24-hour no-human-in-the-loop RTL-to-GDSII flow.

## IV. MODIFICATION DONE

In the asap7 ibex design we can change the cells list and increase the buffer size at cts stage and change the metal layers at routing stage. We are able to achieve a design with good results.

```
set_false_path -to [get_ports {alert_major_o}]
set_false_path -to [get_ports {alert_minor_o}]
set_false_path -to [get_ports {instr_addr_o[0]}]
set_false_path -to [get_ports {instr_addr_o[1]}]
set_false_path -to [get_ports {data_addr_o[0]}]
set_false_path -to [get_ports {data_addr_o[1]}]
```

```
set_false_path -to [get_ports {rst_ni}]
set_false_path -from [get_pins _36182_/CLK]
set_false_path -from [get_pins _36313_/CLK]
```

```
.TIELOx1_ASAP7_75t_R_36327_ (
.L(_18389_)
);
BUFx2_ASAP7_75t_R_36328_ (
.A(_18389_),
.Y(alert_major_o)
);
BUFx2_ASAP7_75t_R_36329_ (
.A(_18389_),
.Y(alert_minor_o)
);
BUFx2_ASAP7_75t_R_36330_ (
.A(_18389_),
.Y(data_addr_o[0])
);
BUFx2_ASAP7_75t_R_36331_ (
.A(_18389_),
.Y(data_addr_o[1])
);
BUFx2_ASAP7_75t_R_36362_ (
.A(_18389_),
.Y(instr_addr_o[0])
);
BUFx2_ASAP7_75t_R_36363_ (
.A(_18389_),
.Y(instr_addr_o[1])
);
```

**Before:**

```
finish report_tns
-----
tns -296.50

=====
finish report_wns
-----
wns -92.38

=====
finish report_worst_slack
-----
worst slack -92.38
-----
```

```
finish report_power
-----
Group          Internal  Switching  Leakage    Total
                Power    Power      Power      Power (Watts)
-----
Sequential      2.31e-03  9.78e-04  2.39e-07  3.29e-03  11.6%
Combinational    1.07e-02  1.45e-02  1.99e-06  2.52e-02  88.4%
Macro           0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.0%
Pad             0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.0%
-----
Total           1.30e-02  1.55e-02  2.23e-06  2.85e-02  100.0%
                45.5%    54.5%    0.0%

=====
finish report_design_area
-----
Design area 2490 u^2 45% utilization.

[INFO GUI-0075] Warning: Ignoring XDG_SESSION_TYPE=wayland on Gnome. Use QT_QPA_PLATFORM=wayland to run on Wayland anyway.
Elapsed time: 1:28.02[h:]min:sec. CPU time: user 81.83 sys 0.59 (93%). Peak memory: 712100KB.
-
```

After:

```
=====
finish report_tns
-----
tns -2.86

=====
finish report_wns
-----
wns -2.86

=====
finish report_worst_slack
-----
worst slack -2.86
```

```
=====
finish report_power
-----
Group          Internal  Switching  Leakage    Total
                Power    Power      Power      Power (Watts)
-----
Sequential      2.32e-03  9.74e-04  2.39e-07  3.29e-03  11.5%
Combinational    1.09e-02  1.45e-02  2.02e-06  2.54e-02  88.5%
Macro           0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.0%
Pad             0.00e+00  0.00e+00  0.00e+00  0.00e+00  0.0%
-----
Total           1.32e-02  1.55e-02  2.26e-06  2.87e-02  100.0%
                46.1%    53.9%    0.0%

=====
finish report_design_area
-----
Design area 2501 u^2 45% utilization.

[INFO GUI-0075] Warning: Ignoring XDG_SESSION_TYPE=wayland on Gnome. Use QT_QPA_PLATFORM=wayland to run on Wayland anyway.
Elapsed time: 1:37.54[h:]min:sec. CPU time: user 79.41 sys 0.64 (82%). Peak memory: 712340KB.
-
```

VI. CONCLUSION

In conclusion, the log file captures all the timing reports. The ports are connected with TIELO and asynchronous paths that are shown unconstrained and that are set to be false paths and now they are not present in the timing report. We can not worry much about it but it is confusing for the beginners to constrain or make it a false path.

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