Conversion Config_register_set verilog code to VHDL

entity: entity means it is actually specifications of the systems external interface(or) module or Outer structure of module

architecture: architecture means specifications internal implementation of a entity or module

process: Basic unit of execution in VHDL

All operations that are performed in the vhdl simulation are broken int small small programs or into multiple programs

Generic: pass information to an entity

A generic is a vhdl term for a parameter that passes information to an entity then that vhdl term or parameter we called it as generic

```
library IEEE;

use IEEE.STD_LOGIC_116.4_all; // this are packages for in built functions

entity config_register_set is

generic (reg_width: integer := 8;

num_regs: integer := 4);

port(clk : in std_logic;

rst_n: in std_logic;

wr_data: in std_logic_vector(reg_width-1 downto 0);

wr_addr: in std_logic _vector (1 downto 0);

wr_enable: in std_logic;

rd_data: in std_logic_vector (reg_width-1 down_to 0));

end config_register_set;

////internal register array

/////in vhdl we can't directly declare a reg variable so we declare it as type then assign to it wire (signal)

type reg_array_type ;

signal reg_array:= (0 to num_regs-1) of std_logic_vector(reg_width-1 downt 0);

process(clk,rst_n)

begin
```

```
if rst_n='0' then
for i in 0 to num_regs-1 loop
reg_array(i)<='0';
end loop;
else if rising_edge(clk)
then
reg_array(wr_addr)<=wr_data;
end if;
end if;
endprocess;
rd_data<=reg_array(wr_addr);
end behavioral;
```