

1.DIGITAL CONCEPTS

1.Any number with an exponent of zero is equal to:

- a) Zero
- b) One
- c) That number
- d) Ten

Answer: option B

Explanation:-

As per maths rules..."any thing to the power zero is always one". $A^0=1$.

2.In the decimal numbering system, what is the MSB?

- a) The middle digit of a stream of numbers
- b) The digit to the right of the decimal point
- c) The last digit on the right
- d) The digit with the most weight

Answer: option D

Explanation:-

MSB is nothing but most significant bit

Ex:11000.

'1' is the MSB.

'0' is the LSB.

3.Which of the following statements does not describe an advantage of digital technology?

- a) The values may vary over a continuous range.
- b) The circuits are less affected by noise.
- c) The operation can be programmed.
- d) Information storage is easy.

Answer: option A

Explanation:-

Digital values are discrete in nature.

4.The generic array logic (GAL) device is _____

- a) One-time programmable
- b) Reprogrammable
- c) A CMOS device
- d) Reprogrammable and a CMOS device

Answer: option B

Explanation:-

The generic array logic (also known as GAL) device was an innovation of the PAL (programmable array logic) and was invented by lattice semiconductor. The GAL was an improvement on the PAL because one device was able to take the place of many PAL devices or could even have functionality not covered by the original range. Its primary benefit, however, was that it was erasable and re-programmable making prototyping and design changes easier for engineers.

5. The range of voltages between $V_{l(max)}$ and $V_{h(min)}$ are _____.

- a) Unknown
- b) Unnecessary
- c) Unacceptable
- d) Between 2 v and 5 v

Answer: option C

Explanation:-

Digital devices works on 0 and 1 only. i.e For 0, the voltage range is $V_{l(min)}$ - $V_{l(max)}$ and for 1, its $V_{h(min)}-V_{h(max)}$. So, the gap between $V_{l(max)}$ and $V_{h(min)}$ means nothing to a digital system because its neither 0 nor 1. Its just a transition state. That's why, this region is unacceptable for digital devices. this question is from digital point of view, not from analog.

6. What is a digital-to-analog converter?

- a) It takes the digital information from an audio cd and converts it to a usable form.
- b) It allows the use of cheaper analog techniques, which are always simpler.
- c) It stores digital data on a hard drive.
- d) It converts direct current to alternating current.

Answer: option A

Explanation:-

There are two basic type of converters, digital-to-analog (DAC's) and analog-to-digital (ADC's). Their purpose is fairly straightforward. In the case of DAC's, they output an analog voltage that is a proportion of a reference voltage, the proportion based on the digital word applied. In the case of the ADC, a digital representation of the analog voltage that is applied to the ADC's input is outputed, the representation proportional to a reference voltage.

7. What are the symbols used to represent digits in the binary number system?

- a) 0,1

- b) 0,1,2
- c) 0 through 8
- d) 1,2

Answer: option A

Explanation:-

Digital use only 0 & 1.

0=logic 0=low.

1=logic 1=high.

8.A full subtracter circuit requires _____.

- a) Two inputs and two outputs
- b) Two inputs and three outputs
- c) Three inputs and one output
- d) Three inputs and two outputs

Answer: option D

Explanation:-

$D_n = a_n \oplus b_n \oplus c_{n-1}$

$c_n = a' n b_n + a' n c_{n-1} + b n c_{n-1}$

it is a representation of full subtractor, which need 3-inputs and 2-outputs.

9.The output of an AND Gate is low _____.

- a) All the time
- b) When any input is low
- c) When any input is high
- d) When all inputs are high

Answer: option B

Explanation:-

AND Gate truth table

a b f

0 0 0

0 1 0

1 0 0

1 1 1

10.Give the decimal value of binary 10010.

- a) 6_{10}
- b) 9_{10}
- c) 18_{10}
- d) 20_{10}

Answer: option C

Explanation:-

10010
| | | | | _____ $0 \times 2^0 = 0$
| | | | | _____ $1 \times 2^1 = 2$
| | | | | _____ $0 \times 2^2 = 0$
| | | | | _____ $0 \times 2^3 = 0$
| | | | | _____ $1 \times 2^4 = 16$

--

18

Or

Binary code decimal mean convert in to binary to decimal

16 8 4 2 1

(1 0 0 1 0)

now see $16 \times 1 + 2 \times 1$

$16+2 = 18$

ans 18

11. Parallel format means that:

- a) Each digital signal has its own conductor.
- b) Several digital signals are sent on each conductor.
- c) Both binary and hexadecimal can be used.
- d) No clock is needed.

Answer: option A

Explanation:-

Data transmission can be done by two ways:

1) serial - here the data bits/bytes are queued up so that all the data can be transferred over a single data line. All the data can be sent, but transmission takes more time.

2) parallel - here number of lines are given depending on number of data bits.e.g. For hexadecimal numbers 0-f(0000-1111), four parallel transmission lines may be used. More number of data lines are needed, but data is sent almost simultaneously & speedily.

the above is a single wire through which bits can be transmitted serially i.e., one bit at a time.

-----0000
-----1101
-----1010
-----0001

the above are four parallel lines through which hexadecimal number can be transmitted simultaneously. It saves time.

12.A decoder converts _____.

- a) Noncoded information into coded form
- b) Coded information into noncoded form
- c) Highs to lows
- d) Lows to highs

Answer: option B

Explanation:-

Decoder is used to convert the coded form like binary, BCD etc into un-coded form. It has n i/p s and 2^n o/p's.

13.A DAC changes _____.

- a) An analog signal into digital data
- b) Digital data into an analog signal
- c) Digital data into an amplified signal
- d) None of the above

Answer: option B

Explanation:-

Digital means 0's and 1's (i.e) data. D/a means that data converts into analog (i.e) signal form like sin, cosine etc.

14.The output of a NOT Gate is high when _____.

- a) The input is low
- b) The input is high
- c) The input changes from low to high
- d) Voltage is removed from the gate

Answer: option A

Explanation:-

NOT Gate acts as an inverter. The output is complemented form of input.hence when input goes low the output becomes high

Input(0) = output (1)

input(1) = output (0)

15.The output of an OR Gate is low when _____.

- a) All inputs are low
- b) Any input is low
- c) Any input is high
- d) All inputs are high

Answer: option A

Explanation:-

OR truth table

i/p1 i/p2 o/p

0	0	0
0	1	1
1	0	1
1	1	1

all i/p are low at first case and o/p is also low

As we know the OR Gate is the addition and it gives high output only when any one of the inputs is high.

$$A \ b \ y=a+b$$

0 0 0 low

0 1 1 high

1 0 1 high

1 1 1 high

16.Which of the following is not an analog device?

- a) Thermocouple
- b) Current flow in a circuit
- c) Light switch
- d) Audio microphone

Answer: option C

Explanation:-

Options a, c & d denote devices showing different outputs over different inputs. The output here is analogous to the input. Hence, these are analog devices. However, for a light switch, if it is off, the output is 0(light off) for any voltage extremes. Similarly, if it is on, output is 1(light on). As output fluctuates between 0 & 1, switch is a digital device here.

17.A demultiplexer has _____.

- a) One data input and a number of selection inputs, and they have several outputs
- b) One input and one output
- c) Several inputs and several outputs
- d) Several inputs and one output

Answer: option A

Explanation:-

Demultiplexer refers to demux means one to many and multiplexer refers to many to one.

It frequently use in digital signal processing, if there is requirement of one signal to many user can easily send by using Demultiplexer.

18.A flip-flop has _____.

- a) One stable state

- b) No stable states**
- c) Two stable states**
- d) None of the above**

Answer: option C

Explanation:-

Actually flip flop used as primary memory(0 or 1) devices in digital circuits so it has two states 0 or 1 that's why known as two stable states.

Note:-

- The flip flops and latches are data storage elements. Flip flop is having only 2 stable states and flip flop is called as multivibrators or trigger circuits. If you consider monostable it is having only one stable state and 1 quasi stable state. If you consider bistable it is having 2 stable states so we called flip flop as bistable multivibrator.
- Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information.
The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted.
In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal.
This enables signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

19.Digital signals transmitted on a single conductor (and a ground) must be transmitted in:

- a) Slow speed.**
- b) Parallel.**
- c) Analog.**
- d) Serial.**

Answer: option D

Explanation:-

To transfer signals in parallel each signal should have one conductor. To transfer all the signals using one conductor they should be transmitted in series.

20.In a certain digital waveform, the period is four times the pulse width. The duty cycle is _____.

- a) 0%**

- b) 25%
- c) 50%
- d) 100%

Answer: option B

Explanation:-

Duty cycle= (on time) / (on time+off time).
i.e. , pulse width= on time+off time.
So D. C = $1/4 * 100$.
=25%.

21.In positive logic, _____.

- a) A high = 1, a low = 0
- b) A low = 1, a high = 0
- c) Only highs are present
- d) Only lows are present

Answer: option A

Explanation:-:

Note:-

Actually the voltage levels are represented in low and high. Here we are having 2 logics one is positive logic and another is negative logic. If the signal is activating the circuit it is represented as logic '1' and if the signal disable the circuit then it is represented as logic '0'.

Negative logic is the inverse operation of positive logic.

Example:

if we take two voltages 0 and -5, for logic 1 has 0 volts and logic 0 has -5 volts.

If two volts are 5v and 10v then in positive logic 5v for logic 0 and 10v for logic 1.

For positive logic, "1" level value > "0" level value and,
for negative logic, "1" level value < "0" level value.

22.Convert the fractional binary number 0000.1010 to decimal.

- a) 0.625
- b) 0.50
- c) 0.55
- d) 0.10

Answer: option A

Explanation:-:

Binary-decimal is::

$$\dots + 2^{\text{power}2} + 2^{\text{power}1} + 2^{\text{power}0} \rightarrow \text{before point value } 2^{\text{power}-1} + 2^{\text{power}-2} + 2^{\text{power}-3} \dots \rightarrow \text{after point value so-} > > (1 * 2^{\text{power}-1}) + (0 * 2^{\text{power}-2}) + (1 * 2^{\text{power}-3}) + (0 * 2^{\text{power}-4}) \\ = 1/2 + 0 + 1/8 + 0 \\ = 625 \\ \text{there for= .625}$$

23. Digital representations of numerical values of quantities may best be described as having characteristics:

- a) That are difficult to interpret because they are continuously changing.
- b) That vary constantly over a continuous range of values.
- c) That vary in constant and direct proportion to the values they represent.
- d) That vary in discrete steps in proportion to the values they represent.

Answer: option D

Explanation:-

Let's see the binary equivalents of numbers 0-9: a)0000 b)0001 c)0010 d)0011 e)0100 f)0101 g)0110 h)0111 i)1000 j)1001. As seen here, every number with 0 in units place is followed by a number with 1. Also, if a 1 is followed by a series of 1's, next number will be bigger by one bit, with leftmost bit being 1 & rest being 0. Hence, digital representation follows a definite pattern for positive integers. For fractions, the units place digit maybe replaced by the bit to farthest right & similar pattern maybe observed. Regarding negative numbers, sign bits are set & 1's complement method is used to denote the number.

24. A common instrument used in troubleshooting a digital circuit is a(n) _____.

- a) Logic probe
- b) Oscilloscope
- c) Pulser
- d) All of the above

Answer: option D

Explanation:-

Note:-

- **Troubleshooting:-** Troubleshooting means checking each & every component & path in a circuit to see whether it is working correctly. If

a circuit doesn't work correctly, troubleshooting helps to find the fault so that it can be rectified.

- **Probe**:-Probe is used to check connectivity in input and output. In oscilloscope we check waveforms of circuit.
- **Pulser**:-Pulser is a device which generates digital waveforms. So by checking for certain input what is output we can troubleshoot easily

25.The parallel transmission of digital data:

- a) Is much slower than the serial transmission of data
- b) Requires only one signal line between sender and receiver.
- c) Requires as many signal lines between sender and receiver as there are data bits.
- d) Is less expensive than the serial method of data transmission

Answer: option C

Explanation:-

Parallel transmission of digital data means hole digital input transfers at a time. The number of input lines required is same as the number of data lines.

The transmission is in between so many lines and in parallel communication also having different types half duplex,full duplex like that we have.

- Half duplex means communication is two way, but they do not occur simultaneously,
- full duplex both transmission and reception takes place simultaneously.
-

26.Convert the fractional decimal number 6.75 to binary.

- a) 0111.1100
- b) 0110.1010
- c) 0110.1100
- d) 0110.0110

Answer: option C

Explanation:-

0110.1100

left side of the point $0110 = 0 + 1 \cdot 2^1 + 1 \cdot 2^2 + 0 = 4 + 2 = 6$.

Right side of the point $1100 = 1 \cdot 2^{-1} + 1 \cdot 2^{-2} = 1/2 + 1/4 = 0.5 + 0.25 = 0.75$.
 $6 + 0.75 = 6.75$.

27.What is one relative disadvantage of serial transfer?

- a) It requires too many conductors.
- b) Its interconnect system is complex.
- c) It is slow.
- d) It can only be used over very short distances.

Answer: option C

Explanation:-

If we consider serial transfer the operation will be slow. Let us consider the example as binary adder. The output of first adder will gives the input of next adder as the process is continuing like that the more amount of time will be taken. That wise only the serial transfer operation is slow. This can be used only for short distance because at long distance transmission the distortion is occur which stops it signal and used a parallel transfer operation which bounds the signal in a particular way.

28.Which format requires fewer conductors?

- a) Parallel
- b) Serial
- c) Both are the same
- d) Cannot tell

Answer: option B

Explanation:-

In serial circuit it uses only one connector to send data from transmitter to receiver and it can travel data to longer distance and cheaper in cost

29.A pulse has a period of 15 ms. Its frequency is _____.

- a) 6.66 hz
- b) 66.66 hz
- c) 666.66 hz
- d) 15 hz

Answer: option B

Explanation:-

Frequency = $1/t$ hz,

now given: $t = 15\text{ms} = 15 \times 10^{-3}$ seconds.

Frequency = $1 / (15 \times 10^{-3}) = 0.06667 \times 10^3 = 66.67\text{hz}$.

30.Give the decimal value of binary 10000110.

- a) 134_{10}
- b) 144_{10}
- c) 110_{10}
- d) 126_{10}

Answer: option A

Explanation:-

1 0 0 0 0 1 1 0

$1 \times 2^7 + 0 \times 2^6 + 0 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$.
 $2^7 + 2^2 + 2^1$.
128+4+2 = (134)₁₀ decimal.

31. The rise time is the time it takes a pulse to go from _____.

- a) The base line to the maximum high voltage
- b) 10% of the pulse amplitude to the maximum high voltage
- c) The base line to 90% of the pulse amplitude
- d) 10% of the pulse amplitude to 90% of the pulse amplitude

Answer: option D

Explanation:-

In electronics, when describing a voltage or current step function, rise time refers to the time required for a signal to change from a specified low value to a specified high value. Typically, in analog electronics, these values are 10% and 90% of the step height: in control theory applications, according to Levine (1996, p. 158), rise time is defined as "the time required for the response to rise from x% to y% of its final value", with 0%-100% rise time common for under damped second order systems, 5%-95% for critically damped and 10%-90% for over damped. The output signal of a system is characterized also by fall time: both parameters depend on rise and fall times of input signal and on the characteristics of the system.

32. What is an analog-to-digital converter?

- a) It makes digital signals.
- b) It takes analog signals and puts them in digital format.
- c) It allows the use of digital signals in everyday life.
- d) It stores information on a cd.

Answer: option B

Explanation:-

ADC converter-i/p will be analog signal and the o/p will be in digital signal

33. A multiplexer has _____.

- a) One input and several outputs
- b) One input and one output
- c) Several inputs and several outputs
- d) Several inputs and one output

Answer: option D

Explanation:-

Multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. Let us consider example 4:1 mux, it is having 4 inputs and 2 selection lines and 1 output.

34.What is the decimal value of 2^3 ?

- a) 2
- b) 6
- c) 4
- d) 8

Answer: option D

Explanation:-

$$2^3 = 2*2*2=8$$

35.An encoder converts _____.

- a) Noncoded information into coded form
- b) Coded information into noncoded form
- c) Highs to lows
- d) Lows to highs

Answer: option A

Explanation:-

Encoder by the name implies one secret code is added to a signal and gives as a output.

36.What kind of logic device or circuit is used to store information?

- a) Counter
- b) Register
- c) Inverter
- d) Buffer

Answer: option B

Explanation:-

Register is made of flip-flop units which are capable of storing one bit of data at a time. Hence, register can be considered as storage device.

Buffer can be used to delay data propagation in order to synchronize various data handling components.

Counters, are used to generate(multiply or divide) clock frequencies
inverters are simply NOT Gates.

- Simply we can say that buffer is to hold the data (i.e it doesn't store the data) but register made of flip flop can store data. We can say the content present in buffer is not stored and so it will get automatically deleted because it makes delay in the propagation of data which seems to be saved, but it is not actually stored in buffer.
- Both the register and buffer are memory devices but register is located in CPU holds small amount of data where as buffer is an area of ram designed to store data in advance.

37.PICC packages have leads on _____.

- a) One side
- b) Two side
- c) Three side
- d) Four side

Answer: option D

Explanation:-

PICC: plastic leaded chip carrier. Normally a four-sided quad package in which an IC is installed with j-type leads extending out from the sides of the package then down and rolled under the body of the device.

Plcc -> computer-information technology :

plastic leaded chip carrier (pentium socket on mother board) information technology-it-electronics :plastic leadless chip carrier.In plcc connections are made on all four edges of a square package; the internal cavity for mounting the integrated circuit is large, compared to the package overall size.

38.What is the typical invalid voltage for a binary signal?

- a) 0.7–2.8 volts
- b) 0.8–3 volts
- c) 0.8–2 volts
- d) 0.7–2.5 volts

Answer: option C

Explanation:-

On other hand, every logic family has a specified minimum voltage specification. That determines the range for said family.

In digital circuit there are almost three families CMOS, TTL, ECL and the region occurs between low to high is invalid region.

In TTL low voltage is 0 to 0.8v for logic 0 and high voltage is 2 to vcc for logic 1. So there is a transition region between .8v to 2v. Hence it is invalid region.

Examples of binary logic levels:

technology | L Voltage | H Voltage | notes.

CMOS | 0 v to vdd/2 | vdd/2 to vdd | vdd = supply voltage.

TTL | 0 v to 0.8 v | 2 v to vcc | vcc is 4.75 v to 5.25 v.

Ecl | -1.175 v to vee | 0.75 v to 0 v | vee is about -5.2 v. Vcc=ground.

It is usual to allow some tolerance in the voltage levels used; for example, 0 to 2 volts might represent logic 0, and 3 to 5 volts logic 1. A voltage of 2 to 3 volts would be invalid, and occur only in a fault condition or during a logic level transition.

39.Convert the fractional binary number 0001.0010 to decimal.

- a) 1.40

- b) 1.125
- c) 1.20
- d) 1.80

Answer: option B

Explanation:-

$$\begin{aligned} &= 1*2^0.0*(2^{-1})+0*(2^{-2})+1*(2^{-3})+0*(2^{-4}). \\ &= 1.1/8. \\ &= 1.125. \end{aligned}$$

40. How many binary bits are necessary to represent 748 different numbers?

- a) 9
- b) 7
- c) 10
- d) 8

Answer: option C

Explanation:-

$$\begin{aligned} 748/2 &= \text{div}-374 \text{ rem}=0 \\ 374/2 &= \text{div}-187 \text{ rem}=0 \\ 187/2 &= \text{div}-93 \text{ rem}=1 \\ 93/2 &= \text{div}-46 \text{ rem}=1 \\ 46/2 &= \text{div}-23 \text{ rem}=0 \\ 23/2 &= \text{div}-11 \text{ rem}=1 \\ 11/2 &= \text{div}-5 \text{ rem}=1 \\ 5/2 &= \text{div}-2 \text{ rem}=1 \\ 2/2 &= \text{div}-1 \text{ rem}=0 \\ 1/2 &= \text{div}=0 \text{ rem}=1 \\ \text{hence } (748) &= 1011101100 \end{aligned}$$

so 10 digits are required to represent 748.

41. periodic digital waveform has a pulse width (t_w) of 6 ms and a period (t) of 18 ms. The duty cycle is _____.

- a) 3.3%
- b) 33.3%
- c) 6%
- d) 18%

Answer: option B

Explanation:-

$D = t_{on}/\text{total time period}$

$t_{on} = 6\text{ms}$

$\text{total time period} = 18\text{ms}$

so in percentage 33.33%

$$D = t/p * 100 \%$$

Where D is the duty cycle, t is the time the signal is active, and p is the total period of the signal.

$$D = 6\text{ms}/18\text{ms} * 100 \quad \{\text{where milli} = 10^{-3}\}$$

42. Any number with an exponent of one is equal to:

- a) Zero.
- b) One
- c) Two
- d) That number

Answer: option D

Explanation:-

Anything¹=anything

43. Serial format means digital signals are:

- a) Sent over many conductors simultaneously.
- b) Sent over one conductor sequentially.
- c) Sent in groups of eight signals.
- d) Sent in binary coded decimal.

Answer: option B

Explanation:-

In serial format data are sent in single line.

44. What is the decimal value of 2^{-1} ?

- a) 0.5
- b) 0.25
- c) 0.05
- d) 0.1

Answer: option A

Explanation:-

$$2^{-1} = 1/2 = 0.5$$

45. Which format can send several bits of information faster?

- a) Parallel
- b) Serial
- c) Both are the same
- d) Cannot tell

Answer: option A

Explanation:-

data transmission lines are more so data can be transferred fastly compared to serial communication. Parallel data transfer has problem of induction at high frequency, cause of that there is a possibility that at higher frequency the data can be flip. So for high speed serial data transfer is preferred. Example USB, PCI express.

46. The frequency of a pulse train is 2 khz. The pulse period is _____.

- a) 5 ms
- b) 50 ms
- c) 500 μ s
- d) 2 μ s

Answer: option C

Explanation:-

$$T=1/f$$
$$\text{so } t=1/2 \times 10^3$$
$$\text{then } t=10^{-3}/2$$
$$=10^{-3} \times 0.5$$
$$=500 \times 10^{-6}$$
$$=500\text{us}$$

47. What has happened to the advances in digital technologies over the past three decades?

- a) Slowed down considerably
- b) Continued to increase, but at a decreasing rate
- c) Made excellent progress
- d) Nothing short of phenomenal

Answer: option D

Explanation:-

Phenomenal means extraordinary and outstanding. Since the last three decades have marked a phenomenal phase in the development of digital technologies hence option d.

48. A type of digital circuit technology that uses bipolar junction transistors is _____.

- a) TTL
- b) CMOS
- c) LSI
- d) NMOS

Answer: option A

Explanation:-

Note:-

- TTL - transistor - transistor logic.
 - LSI - large scale integration circuits.
 - CMOS - complementary metal oxide semiconductor.
 - NMOS - n - type metal oxide semiconductor.
-
- Transistor-transistor logic (TTL) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called transistor-transistor logic because both the logic gating function (e.g. , and) and the amplifying function are performed by transistors (contrast with rtl and dtl).
 - TTL is notable for being a widespread integrated circuit (ic) family used in many applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics.
 - TTL uses bipolar junction transistor. CMOS uses mosfet.
 - Lsi means large scale integration words related to ic chip design.

49.How many unique symbols are used in the decimal number system?

- a) One
- b) Nine
- c) Ten
- d) Unlimited

Answer: option C

Explanation:-

Symbols 0,1,2,3,4,5,6,7,8,9.. Totally ten

50.A classification of IC's with complexities of 12 to 100 equivalent gates on a chip is known as _____.

- a) SSI
- b) MSI
- c) LSI
- d) VLSI

Answer: option B

Explanation:-

SSI: small scale integration = up to 10 gates.

MSI: medium scale integration = up to 1000 gates.

LSI: large scale integration = up to 10000 gates.

VLSI: very large scale integration = over 10000 gates.

SOC: million gate, software & hardware.

51.Which of the following is a semiconductor memory?

RAM
MAR
CD-ROM
CD

Answer: option A

Explanation:-

semiconductor memory is an electronic data storage device, often used as computer memory.

Computer memory types

Volatile:

- dram (e.g., ddr sdram)
- sram: in development t-ram
- z-ram
- ttram
- historical delay line memory:
- selectron tube
- williams tube

Non-Volatile:

- rom prom
- eprom
- eeprom

Flash memory:

- early stage feram
- mram
- pram

Development cbram:

- sonos
- rram
- racetrack memory
- nram
- millipede

Historical drum memory:

- magnetic core memory
- plated wire memory
- bubble memory
- twistor memory

52.The holes through a pc board are _____.

- a) Smaller with SMT than with through-hole mounting
- b) Larger with SMT than with through-hole mounting
- c) The same size as with through-hole mounting
- d) Usually unnecessary

Answer: option C

Explanation:-

In SMT, the components are lead-less and are directly mounted to the board surface. In through hole the components have lead wires that are taken to the wiring boards via holes.

SMT helps significantly in solving the space problems that were commonly noticed with the through hole mounting.

53.A classification of IC's with complexities of 100 to 10,000 equivalent gates per chip is known as _____.

- a) SSI
- b) MSI
- c) LSI
- d) VLSI

Answer: option C

Explanation:-:

SSI: small scale integration = up to 10 gates.

MSI: medium scale integration = up to 1000 gates.

LSI: large scale integration = up to 10000 gates.

VLSI: very large scale integration = over 10000 gates.

TRUE/FALSE

1.The voltage levels used to represent binary values (0 and 1) in a digital system are nearly equal in value.

A)True

B)False

Answer: option B

Explanation:-

In digital systems the logic 1 represents the high value of a signal which is greater than +5 volts and the logic 0 represents the low value which is nearly equal to +0.8 volts or less than it. So both the logics have different values with a very big difference.

2.In a serial data system, the data is transmitted along a group of conductors simultaneously.

A)True

B)False

Answer: option B

Explanation:-

In serial communication only single conductor use to transmit a digital digit or analog voltage level, digit& voltage level transmit serially.

Ex- digit are 101101 first transmit 1 then 0 from right and so on.

If want to transmit parallel no of digit equal to no of conductor.

3.Temperature variation is normally an analog quantity.

A)True

B)False

Answer: option A

4.Transistor-transistor logic (TTL) uses the bipolar transistor as its main circuit element.

A)True

B)False

Answer: option A

5.A Digital quantity has a discrete set of values.

A)True

B)False

Answer: option A

Explanation:-

Analog signal is a continuous, digital signal is a discreet.

6.SMT stands for small-to-medium technology.

A)True

B)False

Answer: option B

Explanation:-

SMT stands for surface mount technology. It is the specific way for mounting the components on pcb (printed circuit board)

7.X-Ray, MRI, and ULTRASOUND systems in hospitals are examples of analog systems.

A)True

B)False

Answer: option A

Explanation:-

In X-Ray, MRI, and ULTRASOUND systems has the wave form which is in the analog form. So that's why the above examples are of analog system.

8.Greater accuracy and precision are possible with digital techniques.

- A)True
B)False**

Answer: option A

9.With an OR Gate, the output is high only when both inputs are high.

- A)True
B)False**

Answer: option B

Explanation:-

- OR Gate will give high output when one of the two inputs is high. It will give low output when both inputs are low.
- The output is high only when both inputs are high in case of AND Gate.

10.The time interval on the leading edge of a pulse between 10% and 90% of the amplitude is the rise time.

- A)True
B)False**

Answer: option A

11.Telcommunications systems do not use digital techniques.

- A)True
B)False**

Answer: option B

Explanation:-

If communication is within the small area then we can use any wired transmission media but if it is far away (like satellite communication) then we have to use digital technique to transfer 0 & 1.

12.The real world is mainly analog.

- A)True
B)False**

Answer: option A

Explanation:-

Digital form is converted from the analog. So that the real world is analog.

13. Binary means having two states or values.

- A) True
- B) False

Answer: option A

14. Four bits equal one byte.

- A) True
- B) False

Answer: option B

Explanation:-

8 bits=1 byte and 4 bits=1 nibble

15. An inverter performs a not operation.

- A) True
- B) False

Answer: option A

16. In a positive logic system, the logic low could be between 0 v and 0.8 v.

- A) True
- B) False

Answer: option A

Explanation:-

In a positive logic system, the logic low is between 0 v and 0.8 v.

The logic high is between 2.5 v to V_{CC} .

17. In a binary system there are only two symbols.

- A) True
- B) False

Answer: option A

Explanation:-

A is the right answer because in a binary system only 0 and 1 are allowed.

18. Using digital techniques of information storage is easy.

- A) True
- B) False

Answer: option A

Explanation:-

Because of using 0's & 1's, one can store the information easily.

19. One advantage of analog circuits over digital circuits is that it's easier to store data.

A) True

B) False

Answer: option B

Explanation:-

Very difficult to store in analog systems due to physical conditions it would be changed.

20. Digital circuits cannot perform logic comparisons since the circuit can have only one of two values at any instant.

A) True

B) False

Answer: option B

21. A digital circuit will not obey a set of logic rules.

A) True

B) False

Answer: option B

22. Circuits that exhibit the property of memory normally revert to their original state when the input is removed.

A) True

B) False

Answer: option B

Explanation:-

Generally digital ckt's have property of data storage (memory). & once data is stored it does not vanish or removed upto the system is running. The input does not affect the stored data.

23. A logic analyzer is used to display a timing diagram.

A) True

B) False

Answer: option A

Explanation:-

A logic analyzer is an electronic instrument which displays signals in a digital circuit. A logic analyzer may convert the captured data into timing diagrams.

24. Parallel transmission is faster than serial.

A)True

B)False

Answer: option A

25.A microcomputer is the smallest type of computer.

A)True

B)False

Answer: option A

26.A device to convert a binary number to a 7-segment display format is a decoder.

A)True

B)False

Answer: option A

Explanation:-

Decoder is a logic circuit which is used to change a BCD number into an equivalent decimal number.

27.The two binary digits are 1 and 2.

A)True

B)False

Answer: option B

Explanation:-

The two binary digits are 0 and 1.

28.It is possible to have an overlap between high and low levels in digital logic.

A)True

B)False

Answer: option B

Explanation:-

High level=+5v

Low level= 0 to 0.8v

hence there is no chance for overlap between high and low levels

29.A microcomputer is not a general-purpose computer.

A)True

B)False

Answer: option B

30.An invalid digital signal is used as a zero.

A)True

B)False

Answer: option B

Explanation:-

An invalid digital signal can be represented by high impedance state.

31.Memory devices store binary data.

A)True

B)False

Answer: option A

32.A graph of phase vs. Time is a timing diagram.

A)True

B)False

Answer: option B

Explanation:-

A graph between frequency(f) and time(t) is called as timing diagram.

A graph between amplitude and time is called timing diagram

33.In a negative logic system, a high is represented by 0.

A)True

B)False

Answer: option A

Explanation:-

- Positive logic: if high voltage level is represented by 1 & low voltage level is represented by 0, then the logic system is said to be based on positive logic.
- Negative logic: if high voltage is represented by 0 & low voltage level is represented by 1, then the logic system is said to be based on negative logic.

34.The LSB is always to the right of the MSB.

A)True

B)False

Answer: option A

Explanation:-

1 0 0 0 0

MSB LSB

the LSB is always to the right of the MSB.

LSB means least significant bit and MSB means most significant bit.

35. With an AND Gate, if one input is high, the output reflects the other input.

- A) True**
- B) False**

Answer: option A

Explanation:-

Because with An AND Gate the output is high only when both the inputs are high.

36. An ADC is an analog-to-digital converter.

- A) True**
- B) False**

Answer: option A

37. The arithmetic/logic unit will send the results of its decisions to memory.

- A) True**
- B) False**

Answer: option B

Explanation:-

Alu will send the results to accumulator.

38. Digital systems require that voltage levels change between high and low.

- A) True**
- B) False**

Answer: option A

39. The cpu (central processing unit) is composed of memory and outputs.

- A) True**
- B) False**

Answer: option B

Explanation:-

Cpu consist of alu and registers.

40. PALs are relatively simple integrated circuit devices.

- A) True**
- B) False**

Answer: option A

Explanation:-

PAL is programmable array logic. It is programmable logic device (pld) consists of fixed or and programmable and plane. These are simple IC's compared to PLA.

FILLING THE BLANKS

1.Digital systems have _____.

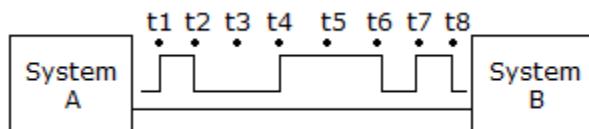
- a) One state
- b) Two state
- c) Three state
- d) Four state

Answer: option B

Explanation:-

Two binary states like 0's and 1's.

2.The systems shown in the given figure transfer data _____.



- a) Serially
- b) Sequentially
- c) In parallel
- d) Both serially and sequentially

Answer: option D

Explanation:-

Serial means if we want to add some data then add at any place, means order is random, but sequential is just like serial but order of data is fixed, not random.

3.Digital systems are called _____.

- a) Binary systems
- b) Logic systems
- c) Numbering systems
- d) ADC systems

Answer: option B

Explanation:-

we use logic for every moment of 0 and 1...for that digital electronics called as logic systems..

4.1/4 as a binary number would be _____.

- a) 0.01
- b) 0.11
- c) 0.10
- d) 0.00

Answer: option A

Explanation:-

It's execute we have to convert 1/4 to in fractions = 0.25.

-> first we have to multiple 0.25 with 2, while converting into binary.

$$0.25 \times 2 = 0.5 \rightarrow 0.$$

$$0.5 \times 2 = 1.0 \rightarrow 1.$$

We have to write up to down,

answer : 0.01.

5.The invalid range for an input to TTL logic is from _____.

- a) 0 to 0.8 v
- b) 1.2 to 1.6 v
- c) 0.8 to 2.0 v
- d) 2.0 to 5.0 v

Answer: option C

Explanation:-

Acceptable- valid range for an input to TTL logic is from 0 to 0.8 and 2.0 to 2 to 5 volts.

6.In a typical digital system, logic 0 is 0v–0.8v, and logic 1 is

- _____.
- a) 2–5v
 - b) 2.5–5v
 - c) 3.0–5.5v
 - d) 3.5–5.5v

Answer: option A

Explanation:-

Actually digital circuits are made by transistors so in order to conduct transistor 0.7v is must(for si) after that transistor conducts and there is output(high).

0 to 0.8 = low.

0.9 to 5 = high.

**7.Once a signal is digitized, the information it contains does not
_____ as it is processed.**

- a) Complain

- b) Stiffen
- c) Compress
- d) Deteriorate

Answer: option D

Explanation:-

Deteriorate means weak or go down.

8.The rise-time of a pulse is normally measured between the _____.

- a) 0 and 100% level
- b) 10% and 90% level
- c) 30% and 70% level
- d) 50% level on the leading edge to the 50% level on the trailing edge

Answer: option B

9.A logic circuit that can store one bit of information is a _____.

- a) Flip-flop
- b) Counter
- c) Gate
- d) Code converter

Answer: option A

Explanation:-

Flip-flops are logical circuits to store one bit information.

This will design by using NOR and NAND Gates.

10.The horizontal axis of an oscilloscope is normally calibrated in units of _____

- a) Voltage
- b) Current
- c) Time
- d) Frequency

Answer: option C

Explanation:-

In oscilloscope always the x axis is shown a time and y axis is shown voltage of other measurement.

11.The combination of waveforms consisting of the given figures 1 and 2 is generally referred to as _____.

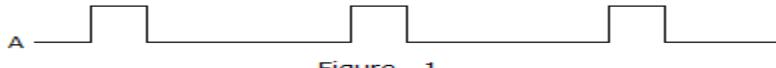


Figure - 1



Figure - 2

- a) Simultaneous waveforms
- b) A timing diagram
- c) Two-phase waveforms
- d) Pulse waveforms

Answer: option B

Explanation:-

Here, the waveform is given with the clock i. E, the response w. Are. T clock period. So, it is timing diagram.

12. The digit that changes most often when counting is called the _____.

- a) LSB
- b) LL BEAN
- c) LED
- d) LCD

Answer: option A

Explanation:-

13. Since unit place is changes ten times change than tens places.

Example: 2 digit binary counting,

00
01
10
11

LSB changes most often.

13. Memory devices that use electronic latching circuits are called _____.

- a) Ram
- b) flip-flop
- c) Magnetic tape
- d) Dram

Answer: option B

14. A set of instructions for a computer is called a(n) _____.

- a) Instruction manual
- b) Logic unit

- c) Program
- d) Diagram

Answer: option C

15.A microprocessor that performs only specific, dedicated tasks is also called a _____

- a) Microcontroller
- b) Calculator
- c) Laptop microcomputer
- d) Workstation processor

Answer: option A

16.The decimal system is composed of _____ symbols.

- a) 2
- b) 8
- c) 10
- d) 16

Answer: option C

Explanation:-

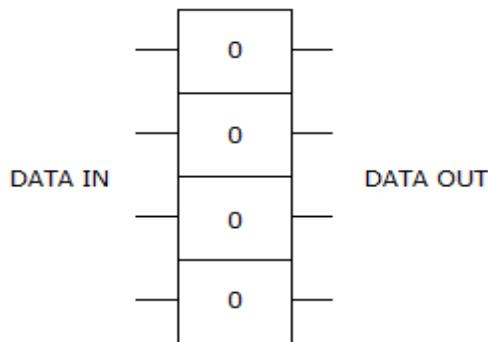
The 10 symbols are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

17.The manner in which a digital circuit responds to an input is the circuit's _____.

- a) Logic
- b) Wiring
- c) Inputs
- d) Outputs

Answer: option A

18.The given figure is most likely a _____.



- a) Register
- b) Decoder
- c) Counter

d) Multiplexer

Answer: option A

Explanation:-

Register is use to store the data bits.

decoder is use to convert a code into a decoded form. Mainly example 2-4 decoder 3-8 decoder. Mean 2 input 4 output (2^2 n 2^3).

Counter is a sequential circuit example which count the data bits.

Multiplexer is a device which allow transfer of data bits from different source on a single channel. So for multiple input there is single output.

19.A(n) _____ is not a functional unit of a computer.

- a) Input unit
- b) Memory unit
- c) Modem
- d) Control unit

Answer: option C

20.The duty cycle of a square wave is _____.

- a) 10%
- b) 25%
- c) 50%
- d) 100%

Answer: option C

Explanation:-

$$\text{Duty cycle} = (1/2)*100.$$

$$= 0.50*100.$$

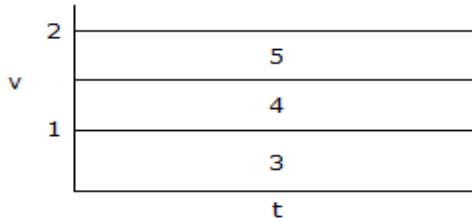
$$= 50\%.$$

21.If a high logic level is assigned a binary zero (0), and a low level is assigned a binary one (1), the logic is called _____

- a) Negative logic
- b) Positive logic
- c) Invalid logic
- d) Assertion-level logic

Answer: option A

22.The quantity represented by #1 in the given figure is _____.



- a) $V_h(\max)$
- b) $V_l(\min)$
- c) $V_h(\min)$
- d) $V_l(\max)$

Answer: option D

Explanation:-

$$V_h(\max) = 5.0 \text{ volts.}$$

$$V_h(\min) = 2.0 \text{ volts.}$$

$$V_l(\max) = 0.8 \text{ volts.}$$

$$V_l(\min) = 0.0 \text{ volts.}$$

23.A binary number can be converted to be viewed on a 7-segment display by a(n) _____.

- a) Decoder
- b) Encoder
- c) Multiplexer
- d) Magnitude comparator

Answer: option A

Explanation:-

Ic 7447 (decoder ic) can be used for converting data from BCD to seven segment display.

24.The cpu contains all the circuitry for _____.

- a) Storing data
- b) Keeping track of time
- c) Fetching and interpreting instructions
- d) Internet operations

Answer: option C

25.Demultiplexing is a logic function that _____.

- a) Determines which of several inputs is the greatest
- b) Switches logic from one input to any of several output lines
- c) Switches logic from several inputs onto one output line
- d) Converts a code from one form to another

Answer: option B

26.In _____ the quantities are not represented by continuously variable indicators.

- a) Analog representation
- b) Digital representation
- c) Signal representation
- d) Computer representation

Answer: option B

Explanation:-

Digital has only two digits whereas analog has wide no.of values.

27.A continually variable, proportional indicator is a(n) _____ representation.

- a) Decimal
- b) Digital
- c) Unconstitutional
- d) Analog

Answer: option D

Explanation:-

Obviously the continuation means its a analog one.

28.The control and arithmetic/logic units are often considered as one unit called the _____.

- a) Central processing unit
- b) Inputs and outputs
- c) Microcomputer
- d) Arithmetic/logic unit

Answer: option A

29.A microcontroller would not be used in a(n) _____.

- a) Vcr
- b) Automobile ignition system
- c) Antilock brakes
- d) Grandfather clock

Answer: option D

30._____ is the highest-value seven-bit binary number

- a) 128
- b) 127
- c) 126
- d) 125

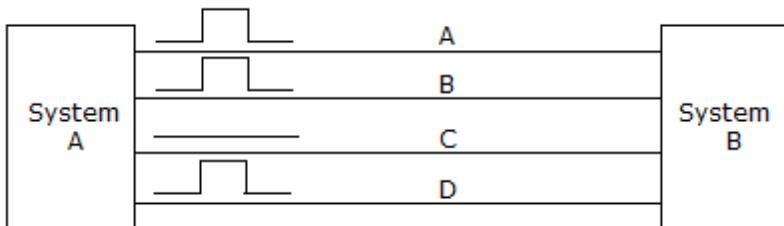
Answer: option B

Explanation:-

Any n digit number using base b can have b^n possible values (b to the power of n). Since 0 is a possible value, the largest value possible is $(b^n) - 1$.

Plugging in your values... $2^7 - 1 = 128 - 1 = 127$.

31.The systems shown in the given figure communicate using _____.



- a) Parallel data
- b) Serial data
- c) Serial-parallel data
- d) Both parallel and serial data

Answer: option A

Explanation:-

Because data parallel in, then data parallel out.

32.The set of instructions for a computer is called a(n) _____.

- a) Program
- b) Input
- c) Output
- d) Control unit

Answer: option A

33.The controls on an oscilloscope that will help obtain a stable display are in the _____.

- a) Vertical section
- b) Horizontal section
- c) Trigger section
- d) Display section

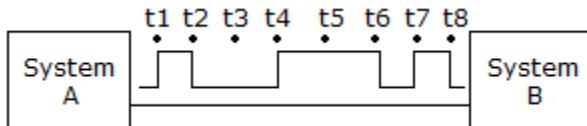
Answer: option C

Explanation:-

Trigger section controls the start event of the sweep (ie. Horizontal time base). So this trigger (eg:edge trigger can happen) will happen for each time intervals in most of the oscillators automatically. This will eliminate distortion of signal and a stable display can be achieved.

But one more option is there external trigger which we used in our electronics lab. We will connect external probe to one input of the oscilloscope and we can trigger the input till the display is stable.

34. The value of the data shown in the given figure is _____.



- a) Between 0 and 1
- b) 1011001
- c) 5
- d) 1001101

Answer: option B

Explanation:-

Here in the above transmission first we send MSB and then the sequence till LSB. As we know that the data should be always represented in the form "MSB _____ LSB" so we need to consider the sequence in the reverse order to get the correct sent sequence.

35. To determine which of two binary numbers is larger, you could use a(n) _____.

- a) Register
- b) Adder
- c) Encoder
- d) Magnitude comparator

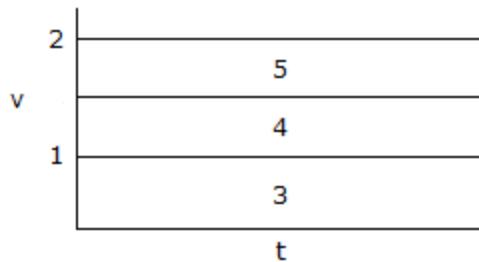
Answer: option D

36. In _____ transmission, a single conductor is used.

- a) Digital
- b) Automatic
- c) Serial
- d) Binary

Answer: option C

37. In a negative logic system, the area represented by #3 in the given figure would be the _____ level.



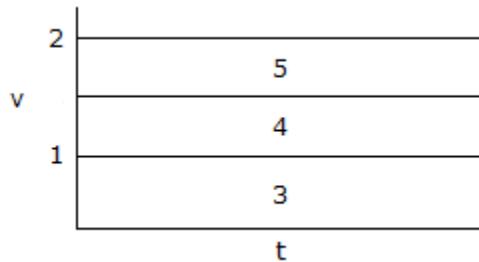
- a) High
- b) Low
- c) Off
- d) Uncertain

Answer: option A

Explanation:-

At the above the value of 1 voltage, there is value of 3. So high. Since 1=high.

38.The area represented by #4 in the given figure is the _____ level.



- a) High
- b) Low
- c) Off
- d) Unacceptable

Answer: option D

39.Other _____ are often used to interpret or represent binary quantities for the convenience of the people who work with and use these digital systems.

- a) Analog systems
- b) Digital systems
- c) Number systems
- d) Binary systems

Answer: option C

40.In a positive logic system, the high level is usually represented by _____.

- a) 0v
- b) +1 v
- c) +5 v
- d) +9 v

Answer: option C

Explanation:-

In terms of voltage it high is +5v and 0 is low.

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2. NUMBER SYSTEMS AND CODES

1. Convert hexadecimal value 16 to decimal.

- a) 22_{10}
- b) 16_{10}
- c) 10_{10}
- d) 20_{10}

Answer: option A

Explanation:-

$$=16^1 * 1 + 16^0 * 6$$

$$=16+6$$

$$=22$$

the answer is 22(a).

2. Convert the following decimal number to 8-bit binary 187

- a) 10111011_2
- b) 11011101_2
- c) 10111101_2
- d) 10111100_2

Answer: option A

Explanation:-

$$\begin{array}{r} 2 | 187 | 1 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 93 | 1 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 46 | 0 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 23 | 1 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 11 | 1 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 5 | 1 \\ \hline \end{array}$$

--

$$\begin{array}{r} 2 | 2 | 0 \\ \hline \end{array}$$

--

$$\begin{array}{r} | 1 | 1 \\ \hline \end{array}$$

answer = 10111011 .

3. Convert binary 11111110010 to hexadecimal.

- a) EE₁₆\
- b) FF₁₆
- c) 2FE₁₆
- d) FD₁₆

Answer: option B

Explanation:-

11111110010

a=10, b=11, c=12, d=13, e=14, f=15

select 4-4 pair group

1111 1111 0010

15 15 2

F F 2

ans:(b).(ff2)16.

4. Convert the following binary number to decimal 01011₂

- a) 11
- b) 35
- c) 15
- d) 10

Answer: option A

Explanation:-

$$010111 = (1*2^0) = (1*1) = 1.$$

$$1 = (1*2^1) = (1*2) = 2.$$

$$0 = (0*2^2) = (0*4) = 0.$$

$$1 = (1*2^3) = (1*8) = 8.$$

$$0 = (0*2^4) = (0*16) = 0.$$

$$01011 = 1+2+0+8+0 = 11.$$

5. Convert the binary number 1001.0010₂ to decimal.

- a) 90.125
- b) 9.125
- c) 125
- d) 12.5

Answer: option B

Explanation:-

1001=9 after point

$$.0010=0*2^0+0*2^1+1*2^3+0*2^4=.125$$

6. Decode the following ASCII message.

**10100111010100101010110001001011001
01000001001000100000110100101000100**

- a) Studyhard
- b) Study hard
- c) Stydyhard
- d) Study hard

Answer: option B

Explanation:-

Correct Explanation:- available here:

step 1: divide the code into 7-bits each

(1010011) (1010100) (1010101) (1000100) (1011001)
(0100000) (1001000) (1000001) (1010010) (1000100)

step 2: convert binary data to decimal individually

step 3: (83) (84) (85) (68) (89) (32) (72) (65) (82) (68)

step 4: substitute characters of ASCII values

example:-

65-a

66-b

67-c

....

....

90-z

32-blank, etc.

I.e code converted into text as study hard

note:- if given data is not consisting 7 multiples of bits then append 0's to MSB i.e left hand side of data.

Also you should remember that characters case i.e upper or lower.

ASCII value for

a = 65, b = 66,

A = 98, b = 99,

7.The voltages in digital electronics are continuously variable.

- a) True
- b) False

Answer: option B

Explanation:-

Change in voltages in digital electronics is not continuous but instantaneous.

8.One hex digit is sometimes referred to as a(n):

- a) Byte
- b) Nibble
- c) Grouping

d) Instruction

Answer: option B

Explanation:-

Binary number system has 2 characters.

Decimal number system has 9 characters.

Octal number system has 8 characters.

Hexa decimal number system has 16 characters.

Bit = 0 or 1;

nibble = 0000 to 1111 ; (any 4 bits btw these).

Byte = 0000 0000 to 1111 1111 (any 8 bit btw those limits).

Similarly, word = any 16 bit.

So the maximum value of hexadecimal number system is f.

And the equivalent value of f in binary is 1111.

Which is the maximum value for a nibble. And so a hex can be referred as a nibble.

9.Which of the following is the most widely used alphanumeric code for computer input and output?

- a) GRAY
- b) ASCII
- c) PARITY
- d) EBCDIC

Answer: option B

Explanation:-

Several coding techniques have been invented that represent alphanumeric information as a series of 1's and 0's.

- ASCII and EBCDIC codes are the two most widely used alphanumeric codes. The ASCII code is very popular code used in all personal computers and workstations whereas the EBCDIC code is mainly alphanumeric code, the unicode, has evolved to overcome the limitation of limited character encoding as in case of ASCII and EBCDIC code.
- The american standard-code for information interchange (ASCII) pronounced "as-kee" is a 7-bit code based on the ordering of the english alphabets.

It is a seven-bit code, it can almost represent 128 characters. These include 95 printable characters including 26 upper-case letters (a to z), 26 lowercase letters (a to z), 10 numerals (0 to 9) and 33 special characters such as mathematical symbols, space character etc.

10.If a typical pc uses a 20-bit address code, how much memory can the cpu address?

- a) 20 MB
- b) 10 MB
- c) 1 MB
- d) 580 MB

Answer: option C

Explanation:-

The answer is very simple. We know 1024 bytes is 1 kb and 2^{10} is 1024, hence $2^{10} * 2^{10} = 2^{20}$, that is $1024 * 1024$, 1kb*1024 is equal to 1 mb.

10. Convert 59.72_{10} to BCD.

- a) 111011
- b) 01011001.01110010
- c) 1110.11
- d) 0101100101110010

Answer: option B

Explanation:-

In BCD no. System all single digit is represent by 4 bit like

5=0101

9=1001

after decimal point same procedure,

7=0111

2=0010

11. Convert $8b3f_{16}$ to binary.

- a) 35647
- b) 011010
- c) 101100111100011
- d) 1000101100111111

Answer: option D

Explanation:-

8 b 3 f

(1000) (1011) (0011) (1111)

12. Which is typically the longest: bit, byte, nibble, word?

- a) Bit
- b) Byte
- c) Nibble
- d) Word

Answer: option D

Explanation:-

1. Bit a single binary digit, that can have either value 0 or 1.
2. Byte 8 bits.
3. Nybble(nibble often nybble or even nyble) 4 bits.
4. Word 32 bits.
5. Half word 16 bits.
6. Double word 64 bits.

13. Assign the proper odd parity bit to the code 111001.

- a) 1111011
- b) 1111001
- c) 0111111
- d) 0011111

Answer: option B

Explanation:-

I believe it is not MSB we add parity.

First you need to know what is sent first: LSB or MSB. Second, you append the odd parity bit at the end of the transmission such that the total number of 1s is odd. So, if you want to send the ASCII 'b' (0x42 -> 1000010) using a communication system that sends LSB first (most common), you would send 0xc2 (11000010), so you would see on the wire 0,1,0,0,0,0,1,1. If you're using a communication system that sends MSB first, the same 'b' would be sent as 0x85. In that case, you would see on the wire 1,0,0,0,0,1,0,1. I hope this helps!

A parity bit, or check bit, is a bit added to the end of a string of binary code that indicates whether the number of bits in the string with the value one is even or odd. Parity bits are used as the simplest form of error detecting code.

14. Convert decimal 64 to binary.

- a) 01010010
- b) 01000000
- c) 00110110
- d) 01001000

Answer: option B

Explanation:-

$$64/2=32-0$$

$$32/2=16-0$$

$$16/2=8-0$$

$$8/2=4-0$$

$$4/2=2-0$$

$$2/2=1-0$$

$$\text{ans}=01000000$$

15. Convert hexadecimal value c1 to binary.

- a) 11000001
- b) 1000111
- c) 111000100
- d) 111000001

Answer: option A

Explanation:-

Hexadecimal has 4-bit i.e nibble hence

c value is 1100

1 value is 0001

so answer is 11000001. Option a.

16. Convert the following octal number to decimal. 17₈

- a) 51
- b) 82
- c) 57
- d) 15

Answer: option D

Explanation:-

$$17 = 7*8^0 + 1*8^1$$

$$7*1+1*8 = 7+8$$

$$= 15$$

17. Convert the following binary number to octal. 010111100₂

- a) 172₈
- b) 872₈
- c) 174₈
- d) 274₈

Answer: option D

Explanation:-

In binary to octal conversion first group the three bits from right to left in any conversion we group the bits from right to left. Here simply 274 is get the answer.

18. How many binary digits are required to count to 100₁₀?

- a) 7
- b) 2
- c) 3
- d) 100

Answer: option A

Explanation:-

8 4 2 1 numbering system can applied upto max. 15. I.e. 4 binary input.

16 8 4 2 1 numbering system can applied upto max. 31. I.e. 5 binary input.

32 16 8 4 2 1 numbering system can applied upto max. 63. I. E. 6 binary input.

64 32 16 8 4 2 1 numbering system can applied upto max. 127. I. E. 7 binary input.

Here 100 number is given and it is covered by 7 binary digit as input. Hence answer is a.

19.The BCD number for decimal 347 is _____.

- a) 1100 1011 1000
- b) 0011 0100 0111
- c) 0011 0100 0001
- d) 1100 1011 0110

Answer: option B

Explanation:-

3 in binary form 0011.

4 in binary form 0100.

7 in binary form 0111.

So BCD num of 347 is,
0011 0100 0111.

20.The binary number for octal 45₈ is _____.

- a) 100010
- b) 100101
- c) 110101
- d) 100100

Answer: option B

Explanation:-

First convert it into decimal & then to binary.

In decimal: $4 \times 8 + 5 = 37$.

In binary: 100101.

21.The sum of 11101 + 10111 equals _____.

- a) 110011
- b) 100001
- c) 110100
- d) 100100

Answer: option C

Explanation:-

$$\begin{array}{r}
 11101 \\
 10111 + \\
 \hline
 110100
 \end{array}$$

Convert 11101 to decimal form = 29.
 Convert 10111 to decimal form = 23.
 Do sum of decimal numbers 29+23 = 52.
 Convert 59 to binary no = 110100.

21. Convert the following binary number to decimal 10011010_2

- a) 154
- b) 155
- c) 153
- d) 157

Answer: option A

Explanation:-

$$\begin{aligned}
 &0*2^0+1*2^1+0*2^2+1*2^3+1*2^4+0*2^5+0*2^6+1*2^7 \\
 &=0+2+0+8+16+0+0+127 \\
 &=153
 \end{aligned}$$

22. The best way to think is the unity bit is 0, so it cannot be an odd number. Every number except 154 is odd. So correct answer is 154. The decimal number 188 is equal to the binary number _____.

- a) 10111100
- b) 0111000
- c) 11000011
- d) 1111000

Answer: option A

Explanation:-

$$\begin{aligned}
 188/2 &= 94 \text{ remainder } 0. \\
 94/2 &= 47 \text{ remainder } 0. \\
 47/2 &= 23 \text{ remainder } 1. \\
 23/2 &= 11 \text{ remainder } 1. \\
 11/2 &= 5 \text{ remainder } 1. \\
 5/2 &= 2 \text{ remainder } 1. \\
 2/2 &= 1 \text{ remainder } 0. \\
 1.
 \end{aligned}$$

Then answer is 10111100.

23. Convert the following binary number to octal. 001101011_2

- a) 153_8

- b) 351_8
- c) 253_8
- d) 352_8

Answer: option A

Explanation:-

$$001 = 1 * 2^0 + 0 * 2^1 + 1 * 2^2 = 1 + 0 + 0 = 1.$$

$$101 = 1 * 2^0 + 0 * 2^1 + 1 * 2^2 = 1 + 0 + 4 = 5.$$

$$011 = 1 * 2^0 + 1 * 2^1 + 1 * 2^2 = 1 + 2 + 0 = 3 (\text{since } 2^0 = 1).$$

24. How many bits are in an ASCII character?

- a) 16
- b) 8
- c) 7
- d) 4

Answer: option C

Explanation:-

> basically ASCII system consist 7bits to represent the any num/character.

> if parity bit is added then it has 8bits but basically it is 7bit alphanumeric code.

24. A binary number's value changes most drastically when the _____ is changed.

- a) MSB
- b) Frequency
- c) LSB
- d) Duty cycle

Answer: option A

Explanation:-

A parity bit, or check bit, is a bit added to the end of a string of binary code that indicates whether the number of bits in the string with the value one is even or odd. Parity bits are used as the simplest form of error detecting code.

Neither in LSB or MSB.

25. Convert decimal 213 to binary.

- a) 11001101
- b) 11010101
- c) 01111001
- d) 11100011

Answer: option B

26.The decimal number for octal 74_8 is _____.

- a) 74
- b) 60
- c) 22
- d) 62

Answer: option B

Explanation:-

$$7*8^1 + 4*8^0 = 60$$

27.The sum of the two BCD numbers, $0011 + 0011$, is _____.

- a) 0110
- b) 0111
- c) 0011
- d) 1100

Answer: option A

Explanation:-

$$\begin{array}{r} 0011 \\ 0011 + \\ \hline \end{array}$$

--

$$\begin{array}{r} 0110 \\ \hline \end{array}$$

--

note:
1+1=0,
1+0=1
0+0=0

28.Convert binary 01001110 to decimal.

- a) 4E
- b) 78
- c) 76
- d) 116

Answer: option B

Explanation:-

$$1 \times 2^1 + 1 \times 2^2 + 1 \times 2^3 + 1 \times 2^6 = 78$$

29.Which is not a word size?

- a) 64
- b) 28
- c) 16
- d) 8

Answer: option B

Explanation:-

4 bits is nibble
8 bits is byte
16 bits is word
32 bits is double word
and this word bits also depends upon machine
1 word=32 bits
double word=64 bits
half word=16 bits

30.The octal numbering system:

- a) Simplifies tasks
- b) Groups binary numbers in groups of 4
- c) Saves time
- d) Simplifies tasks and saves time

Answer: option D

31.The binary number 1110 is equal to the decimal number

-
- a) 3
 - b) 1
 - c) 7
 - d) 14

Answer: option D

Explanation:-

$$\begin{aligned} &= 0*2^0+1*2^1+1*2^2+1*2^3. \\ &= 2+4+8 = 14. \end{aligned}$$

32.Convert the following octal number to binary.76₈

- a) 110111₂
- b) 111110₂
- c) 111100₂
- d) 100111₂

Answer: option B

Explanation:-

There are two ways:

i. We can convert the given number into decimal then to binary:

$$(7*8^1) + (6*8^0) = (56 + 6) = 62(\text{which is in decimal}).$$

$$2|62$$

$$2|31 - 0$$

$$2|15 - 1$$

2|7 - 1
2|3 - 1
2|1 - 1
2|0 - 1

answer is ==> 111110.

Ii. Directly convert to binary by following method which is very simple:

7:- for 7->111 and for 6->110.

By combining: 76 = 111110.

33. Convert 1100101000110101_2 to hexadecimal.

- a) 121035
- b) CA35
- c) 53AC1
- d) 530121

Answer: option B

Explanation:-

Grouping in four numbers.

1100 1010 0011 0101.

C A 3 5.

34. Convert the following decimal number to octal. 281

- a) 134_8
- b) 431_8
- c) 331_8
- d) 133_8

Answer: option B

Explanation:-

$281/8=35, 1$

$35/8=4, 3$

4

35. When using even parity, where is the parity bit placed?

- a) Before the MSB
- b) After the LSB
- c) In the parity word
- d) After the odd parity bit

Answer: option A

Explanation:-

Usually parity occupies the 9th bit position.

Hence it should be placed before MSB.

36Convert the following octal number to decimal. 35_8

- a) 71
- b) 17
- c) 92
- d) 29

Answer: option D

Explanation:-

$$3*8^0+5*8^1 = 24+5 = 29.$$

37.Convert binary 11001111 to hexadecimal.

- a) $8f_{16}$
- b) Ce_{16}
- c) Df_{16}
- d) Cf_{16}

Answer: option D

Explanation:-

$$(1100\ 1111)_2 = (12\ 15)$$

$(CF)_{16}$

38.Convert 1731_8 to decimal.

- a) 216.4
- b) 985
- c) 3d9
- d) 1123

Explanation:-

$$1*(8^3)+7*(8^2)+3*(8^1)+1*(8^0)$$

$$=512+448+24+1$$

$$=985$$

39.An analog signal has a range from 0 v to 5 v. What is the total number of analog possibilities within this range?

- a) 5
- b) 50
- c) 250
- d) Infinite

Answer: option D

Explanation:-

Analog signal has an infinite number of possibilities within 0v to 5v because in analog domain we have every point like 0.1, 0.01, 0.001... For every point, there will be some value.

Digital system process time varying signals that can take only two of the digital values of voltages.

40. Hexadecimal letters a through f are used for decimal equivalent values from:

- a) 1 through 6
- b) 9 through 14
- c) 10 through 15
- d) 11 through 17

Answer: option C

41. Convert the following decimal number to 8-bit binary. 35

- a) 00010010₂
- b) 00010011₂
- c) 00100011₂
- d) 00100010₂

Answer: option C

42. Convert the following hexadecimal number to binary. c9₁₆

- a) 10111001₂
- b) 10111011₂
- c) 10011100₂
- d) 11001001₂

Answer: option D

Explanation:-

C-> 1101.

9-> 1001.

So the obtained solution is 11011001.

43. Convert the following decimal number to hexadecimal. 125

- a) 7d₁₆
- b) D7₁₆
- c) 7c₁₆
- d) C7₁₆

Answer: option A

Explanation:-

First we convert to binary (divide by 2)

125 /2

62.5/2 1

31 /2 0

15.1/2 1

7.5 /2 1

3.5 /2 1

1.5 /2 1

0.5 /2 1

-> (1111101) binary

now we convert to hexadecimal by taking 4 digit from right to left.

The last numbers in the left is (3) digit but we add (0) at the end to be in 4 digit .

0111 1101

(7 d) -> hexadecimal

44.A decimal 11 in BCD is _____.

- a) 00001011
- b) 00001100
- c) 00010001
- d) 00010010

Answer: option C

Explanation:-

In BCD we use a combination of 4 bits. For conversion we separate each decimal digits for example if decimal number 11 convert into BCD we must separate 1 and 1 and convert it in to 4 bits

8 4 2 1 8 4 2 1

0 0 0 1 0 0 0 1

46.What is the resultant binary of the decimal problem 49 + 01 = ?

- a) 01010101
- b) 00110101
- c) 00110010
- d) 00110001

Answer: option C

Explanation:-

First we have to convert 49 into binary. I.e

49/2 = 24 1

24/2 = 12 0

12/2 = 6 0

6/2 = 3 0

3/2 = 1 1

now binary form of 49 = 110001.

Add 01 = + 01

answer = 110010.

47.The difference of 111 – 001 equals _____.

- a) 100
- b) 111

- c) 001
- d) 110

Answer: option D

Explanation:-

Step 1 : find the compliment of the smallest number<here 001>

=>110.

Step 2 : add the result with the first number

111+

110

 *1 101 ///*1 = carry.

Step 3 : add the carry with the previous result

ie; 101+

1

110.

48.Convert the binary number 1100 to gray code.

- a) 0011
- b) 1010
- c) 1100
- d) 1001

Answer: option B

Explanation:-

Let b₀ b₁ b₂ b₃ = 1 1 0 0

g₀ = b₀ = 1

g₁ = b₀ xor b₁ = 0

g₂ = b₁ xor b₂ = 1

g₃ = b₂ xor b₃ = 0

therefore g₀ g₁ g₂ g₃ = 1 0 1 0

hence 1010.

Gray code is one bit change code which is used in certain circuits to reduce the switching of circuit.

E.g. After 0001 there will come 0011 and not 0010 because there is one bit switching (3rd bit) from 0001 to 0011.

49.The binary number 11101011000111010 can be written in hexadecimal as _____.

- a) DD63A₁₆
- b) 1D63A₁₆
- c) 1D33A₁₆
- d) 1D631₁₆

Answer: option B

Explanation:-

split the given number into 4 digits.

I.e; 0001 1101 0110 0011 1010 which is equal to 1d63a respectively in hexadecimal form.

50.Which of the following is an invalid BCD code?

- a) 0011
- b) 1101
- c) 0101
- d) 1001

Answer: option B

Explanation:-

In BCD code, each decimal is represented in its binary value. For eg., BCD code for 8 is 1000. Similarly, BCD for 79 is 01111001. In this question, for the single digit decimal number, the code is from 0000-1001 (0-9). If the number is 2 digits, the answer will be of 8 bits.BCD code has 6 un-used states that are 10 to 15.

The number when converted to binary is greater than 9.

51.What decimal number does 2^5 represent?

- a) 10
- b) 31
- c) 25
- d) 32

Answer: option D

52.Convert the gray code 1011 to binary.

- a) 1011
- b) 1010
- c) 0100
- d) 1101

Answer: option D

Explanation:-

Let g₀ g₁ g₂ g₃ = 1 0 1 1

b₀ = g₀ = 1

b₁ = g₁ xor b₀ = 1

$b_2 = g_2 \text{ xor } b_1 = 0$
 $b_3 = g_3 \text{ xor } b_2 = 1$
therefore $b_0 \ b_1 \ b_2 \ b_3 = 1 \ 1 \ 0 \ 1$
hence 1101.

53. Determine the decimal equivalent of the signed binary number 11110100 in 1's complement.

- a) 116
- b) -12
- c) 11
- d) 128

Answer: option C

Explanation:-

In BCD MSB is 1 -> negative.

In case MSB is 0 -> positive.

The 1's complement of 11110100 is 00001011 which is equal to decimal 11 so answer is (c).

54. What is the difference between binary coding and binary-coded decimal?

- a) BCD is pure binary.
- b) Binary coding has a decimal format.
- c) BCD has no decimal format.
- d) Binary coding is pure binary.

Answer: option D

Explanation:-

In binary coding we represents decimal no. In 16 8 4 2 1 format
eg. Binary coding of 17 is 10001.

Whereas in BCD we represent each digit of decimal no. In binary form
eg. BCD of 17 is 00010111.

55. Convert the following decimal number to BCD. 127

- a) 011100100001
- b) 1110100001
- c) 001010111
- d) 000100100111

Answer: option D

56. Digital electronics is based on the _____ numbering system.

- a) Decimal
- b) Octal
- c) Binary

d) Hexadecimal

Answer: option C

57. An informational signal that makes use of binary digits is considered to be:

- a) Solid state**
- b) Digital**
- c) Analog**
- d) Non-oscillating**

Answer: option B

58. The 1's complement of 10011101 is _____.

- a) 01100010**
- b) 10011110**
- c) 01100001**
- d) 01100011**

Answer: option A

Explanation:-

When code is ex. 1100 then,

1- is convert into - 0.

0- is convert into - 1.

Then answer is 0011.

59. The binary number 101110101111010 can be written in octal as _____.

- a) 51562₈**
- b) 56577₈**
- c) 65627₈**
- d) 56572₈**

Answer: option D

60. Convert 457₁₀ to hexadecimal

- a) 711**
- b) 2c7**
- c) 811**
- d) 1c9**

Answer: option D

61. Convert 457 in to binary. Then convert the binary number in to hexadecimal.

62. Convert the decimal number 151.75 to binary.

- a) 10000111.11**

- b) 11010011.01
- c) 00111100.00
- d) 10010111.11

Answer: option D

Explanation:-

Remainder

$$151/2=75 \text{ } 1$$

$$75/2=37 \text{ } 1$$

$$37/2=18 \text{ } 1$$

$$18/2=9 \text{ } 0$$

$$9/2=4 \text{ } 1$$

$$4/2=2 \text{ } 0$$

$$2/2=1 \text{ } 0$$

$$1/2=0 \text{ } 1$$

from backward(10010111)

for fractional part .75

value before decimal point

$$2*.75=1.50 \text{ } 1$$

$$2*.50=1.00 \text{ } 1$$

downward(.11)

so by merging, the answer is 10010111.11(d)

63. Convert the following octal number to binary. 104₈

- a) 001000100₂
- b) 100000001₂
- c) 0010100₂
- d) 1000001₂

Answer: option A

64. $3 \times 10^1 + 7 \times 10^0$ is equal to _____.

- a) 3.7
- b) 37
- c) 10
- d) 370

Answer: option B

Explanation:-

$$= (3 \times 10) + (7 \times 1).$$

$$= 30 + 7 = 37.$$

65. 3428 is the decimal value for which of the following binary-coded decimal (BCD) groupings?

- a) 11010001001000

- b) 11010000101000
- c) 011010010000010
- d) 110100001101010

Answer: option B

Explanation:-

To make the group of 4 digits from l.s.b to m.s.b. And you will get the answer!

66.The binary-coded decimal (BCD) system can be used to represent each of the 10 decimal digits as a(n):

- a) 4-bit binary code
- b) 8-bit binary code
- c) 16-bit binary code
- d) ASCII

Answer: option A

67.The decimal number 18 is equal to the binary number _____.

- a) 11110
- b) 10001
- c) 10010
- d) 1111000

Answer: option C

68.The 2's complement of 11100111 is _____.

- a) 11100110
- b) 00011001
- c) 00011000
- d) 00011010

Answer: option B

Explanation:-

First take 1's of 11100111=00011000 (just change the value of 1 as 0 & 0 as 1).

Then we have to find the 2's of 00011000 by adding 1.
00011000 + 1 = 00011001. So answer is b.

69.Convert the following decimal number to BCD.469

- a) 100101101000
- b) 010001101001
- c) 100001101001
- d) 100101100100

Answer: option B

70. Express the decimal number -37 as an 8-bit number in sign-magnitude.

- a) 10100101
- b) 00100101
- c) 11011000
- d) 11010001

Answer: option A

Explanation:-

The binary conversion of $37 = 101101$

Now to make 8 bit no we add 00 at left but as here 37 is negative so very first(MSB) we add 1

so it becomes 10100101 that's a.

Step 1: convert 37 to binary ($37 = 100101$)

step 2: add 00 ate the left of MSB as 00100101

step 3: take 1's complement as 11011010

step 4: take 2's complement (by adding 1 to 1's complement of the no.) As
 11011010

+ 1

11011011

so the final answer for -37 is 11011011

and its not there is ant of the options.

Or

Decimal number $37 = 00100101$ in 8 bit binary form
and sign representation depends on MSB bit,

if MSB = 1 then no is negative

if MSB = 0 then no is positive

so; to represent -37 placed 1 to MSB bit

therefore;

decimal number $-37 = 10100101$ in 8 bit binary form

71. Convert the following BCD number to decimal. 010101101001_{BCD}

- a) 539
- b) 2551
- c) 569
- d) 1552

Answer: option C

Explanation:-

divide the given code of four bits each and write decimal equivalent of divided code.

$0101 \mid 0110 \mid 1001$.

5 3 9.

72.The binary number 11001110 is equal to the decimal number _____.

- a) 12
- b) 206
- c) 127
- d) 66

Answer: option B

73.The binary number for f3a₁₆ is _____.

- a) 111100111010
- b) 111100111110
- c) 000000111010
- d) 000011000100

Answer: option A

74.Convert the following BCD number to decimal.100000000011_{BCD}

- a) 8003
- b) 803
- c) 1003
- d) 103

Answer: option B

Explanation:-

1000 = 8.
0000 = 0.
0011 = 3.
10000000011 = 803.

75.Convert the following hexadecimal number to binary.

14b₁₆

- a) 101101000001₂
- b) 000101001011₂
- c) 000101001101₂
- d) 110101000001₂

Answer: option B

Explanation:-

Hexadecimal 16=2⁴
=>4 represents 4bits
hence
1-0001
4-0100
b-1011

76.What is the result when a decimal 5238 is converted to base 16?

- a) 327.375
- b) 12.166
- c) 1388
- d) 1476

Answer: option D

Explanation:-

5238 lcm with 2 by converting into binary and then convert binary to hex.

77.The octal number for binary 1101110101110110 is _____.

- a) 654521₈
- b) 556551₈
- c) 156656₈
- d) 156566₈

Answer: option D

78.Convert the following hexadecimal number to decimal.1cf₁₆

- a) 463
- b) 4033
- c) 479
- d) 4049

Answer: option A

Explanation:-

Here 1cf.

(12) (15)....(a = 10, b = 11, c = 12.....so on).

$$= 1 \ 12 \ 15.$$

$$= 16^2 \ 16^1 \ 16^0.$$

$$= 1*256 + 16*12 + 15.$$

$$= 256 + 192 + 15 = 463$$

79.Convert the binary number 1011010 to hexadecimal.

- a) 5B
- b) 5F
- c) 5A
- d) 5C

Answer: option C

80.Convert the following decimal number to hexadecimal.74

- a) A4₁₆
- b) B4₁₆
- c) 4A₁₆
- d) 4B₁₆

Answer: option C

81. Convert hexadecimal c0b to binary.

- a) 110000001011
- b) 110000001001
- c) 110000001100
- d) 110100001011

Answer: option A

82. Convert binary 1001 to hexadecimal.

- a) 9_{16}
- b) 11_{16}
- c) 101_{16}
- d) 10_{16}

Answer: option A

83. Convert 731_{16} to decimal.

- a) 216.4
- b) 985
- c) 3d9
- d) 1841

Answer: option D

Explanation:-

$$7*16^2 + 3*16^1 + 1*16^0 = 1841.$$

84. What is the decimal value of the hexadecimal number 777?

- a) 191
- b) 1911
- c) 19
- d) 19111

Answer: option B

Explanation:-

$$7*16^2 + 7*16^1 + 7*16^0$$

$$1792 + 112 + 7 = 1911$$

85. Convert 11001001_2 (binary) to decimal.

- a) 201
- b) 2001
- c) 20
- d) 210

Answer: option A

86.Convert the following decimal number to octal.39

- a) 63_8
- b) 36_8
- c) 47_8
- d) 74_8

Answer: option C

87.The american standard code for information interchange (ASCII) uses how many individual pulses for any given character?

- a) 1
- b) 2
- c) 7
- d) 8

Answer: option C

88.Convert the following hexadecimal number to decimal.b5₁₆

- a) 212
- b) 197
- c) 165
- d) 181

Answer: option D

Explanation:-

First step, b5=115.

$$16^0 \cdot 5 + 16^1 \cdot 11 = 5 + 176 = 181.$$

89.The BCD number for decimal 16 is _____.

- a) 00010110
- b) 00010000
- c) 00010010
- d) 11100000

Answer: option A

90.Alphanumeric codes should include as a minimum:

- a) The capacity to represent the alphabet upper- and lowercase characters and the decimal numbers in a straight binary format.
- b) The capacity to code all possible decimal numbers in a direct octal representation of BCD codes.
- c) The alphabet upper- and lowercase letters, the decimal digits, the seven punctuation marks, and other characters or symbols
- d) The ability to represent decimal numbers greater than 128^{10} in a straight binary format.

Answer: option C

91. Convert 527_{16} to binary.

- a) 343
- b) 001101000111
- c) 010100100111
- d) 011100100101

Answer: option C

92. Convert 527_8 to binary.

- a) 011100111
- b) 101010111
- c) 343
- d) 111010101

Answer: option B

93. The base of the hexadecimal system is:

- a) Eight
- b) Sixteen
- c) Ten
- d) Two

Answer: option B

94. Assign the proper even parity bit to the code 1100001.

- a) 11100001
- b) 1100001
- c) 01100001
- d) 01110101

Answer: option A

95. Even parity should be assigned at MSB. Select one of the following statements that best describes the parity method of error detection.

- a) Parity checking is best suited for detecting single-bit errors in transmitted codes.
- b) Parity checking is not suitable for detecting single-bit errors in transmitted codes.
- c) Parity checking is capable of detecting and correcting errors in transmitted codes.
- d) Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.

Answer: option A

96. Which of the following is the primary advantage of using the BCD code instead of straight binary coding?

- a) Fewer bits are required to represent a decimal number with the BCD code.**
- b) The relative ease of converting to and from decimal. BCD codes are easily converted to hexadecimal codes.**
- c) BCD codes are easily converted to straight binary codes.**

Answer: option B

97. How many BCD code bits and how many straight binary bits would be required to represent the decimal number 643?

- a) 12 BCD, 12 binary**
- b) 12 BCD, 10 binary**
- c) 12 BCD, 9 binary**
- d) 16 BCD, 9 binary**

Answer: option B

Explanation:-

Value of 6 in BCD is 0110.

Value of 4 in BCD is 0100.

Value of 3 in BCD is 0011.

So 643 requires 011001000011 a total of 12 BCD code bits.

Now for decimal to binary conversion.

2| 643
2| 321-1.
2| 160-1.
2| 80-0.
2| 40-0.
2| 20-0.
2| 10-0.
2| 5--0.
2| 2--1.
2| 1--0.

So counting from down to up 1010000011 total 10 straight binary bits are required.

98. When using the repeated division by 2 method of converting from decimal to binary, one must write the first remainder as the:

- a) MSB**
- b) MSB, provided the following sequence of remainders are written in descending order until the final remainder is achieved.**
- c) LSB**
- d) LSB, provided the final remainder is used to replace the original LSB, which is then moved to the MSB position**

Answer: option A

Explanation:-

Is zero which is the LSB.

TRUE/FALSE

1.In ASCII code, the hexadecimal sequence 53 54 55 44 45 4E 54 decodes to student.

- A)True
B)False**

Answer: option A

2.A decimal number is converted to BCD by replacing each decimal digit with the appropriate 3-bit binary code.

- A)True
B)False**

Answer: option B

3.A decimal fraction can be converted to binary by using the repeated division-by-2 method.

- A)True
B)False**

Answer: option B

4. $15_{10} = 1111_2 = f_{16} = 00010101$ BCD

- A)True
B)False**

Answer: option A

5.Hex is often used in digital applications as a shorthand way to represent strings of bits.

- A)True
B)False**
Answer: option A

6.The binary number system is fundamental to all digital computers.

- A)True
B)False**
Answer: option A

7.Repeated division-by-10 is used to convert decimal numbers to binary numbers.

- A)True
B)False**

Answer: option B

8.The largest single BCD digit has a binary value of 15.

- A)True
- B)False

Answer: option B

Explanation:-

The largest single BCD digit is 9.

9.A byte has 8 bits.

- A)True
- B)False

Answer: option A

Explanation:-

4 bit - 1 nibble.

8 bit - 1 byte.

10.A binary number can be converted to a decimal number by summing the decimal values of the weights of all the 1s in the binary number.

- A)True
- B)False

Answer: option A

11.Binary-coded-decimal numbers use only binary numbers between 0000 and 1001.

- A)True
- B)False

Answer: option A

12.A good example of the use of a digital representation of an analog quantity is the audio recording of music.

- A)True
- B)False

Answer: option B

13.Each position in a decimal multidigit number will have a weighting factor based on a power of only 10.

- A)True
- B)False

Answer: option A

14.The BCD equivalent of 73 is 01001001.

- A)True
- B)False

Answer: option B

15.Digital systems operate only on discrete digits that represent numbers, letters, or symbols.

- A)True
- B)False

Answer: option A

16.The octal number system consists of eight digits, 0 through 7.

- A)True
- B)False

Answer: option A

17.The gray code has a base of eight.

- A)True
- B)False

Answer: option B

Explanation:-

Octal has only base of 8 not gray code.

18.The hexadecimal equivalent of a decimal number would produce a larger number than the original decimal number.

- A)True
- B)False

Answer: option B

19.ASCII stands for american standard code for information interchange.

- A)True
- B)False

Answer: option A

20.When converting from decimal to binary by the repeated division-by-two method, the initial remainder becomes the MSB

- A)True
- B)False

Answer: option B

21. $3C1D_{16} = 11110000011101_2$

- A)True
- B)False

Answer: option A

22.Zeros may be added to the left of the MSB to produce even groups of 4 bits when converting from binary to hexadecimal.

A)True

B)False

Answer: option A

Explanation:-

Let the number 1111011 now convert it into hexadecimal. Starting from right to left take 4 bit of binary number like (1011).

It is equal to 11 in decimal now take remaining 3 digits (111) but we have 3 binary bit now add zero to the left to MSB (0111). So its complete 4 digits now convert it into decimal which is 3.

23.Digital electronics must use a numbering system that has more than ten digits.

A)True

B)False

Answer: option B

24.A debugging utility is used to take the "bugs" out of a program.

A)True

B)False

Answer: option A

25.The primary advantage of the hexadecimal numbering system is the ease in conversion between the binary and hexadecimal systems.

A)True

B)False

Answer: option B

26.In odd parity, 100011010 would pass the parity check.

A)True

B)False

Answer: option B

27.The primary advantage of the hexadecimal number system is the ease with which conversion can be made between binary and hexadecimal numbers.

A)True

B)False

Answer: option A

28.A binary code decimal representation of a binary number will always have more bits than the binary number.

- A)True
- B)False

Answer: option A

Explanation:-

In binary it is 1100. In binary code decimal it is 0001 0010 more bits. Its true.

29.The decimal number system consists of the digits 0–10.

- A)True
- B)False

Answer: option B

Explanation:-

0-10 is it representing two digits i.e. 0 & 1 or it is representing from 0, 1, 2,...., 10.

$30.12_{10} = 1101_2 = C_{16} = 00010010$ BCD

- A)True
- B)False

Answer: option B

Explanation:-

The binary representation of 12 is 1100 but in the question it given as 1101 so it is false.

31.Hexadecimal is used to encode BCD numbers.

- A)True
- B)False

Answer: option B

32.A method of converting decimal to binary is by successive division.

- A)True
- B)False

Answer: option A

33.Digital circuitry is the foundation of digital computers and many automated control systems.

- A)True
- B)False

Answer: option A

34.A parity bit is used to detect an error in data transmission caused by noise.

- A)True**
- B)False**

Answer: option A

35.Most computers store binary data in groups of 32 bits called dwords.

- A)True**
- B)False**

Answer: option B

36.The word size is defined as the number of bits in the binary word that a digital system operates on.

- A)True**
- B)False**

Answer: option A

37.The hexadecimal number system consists of 16 digits, 0–15.

- A)True**
- B)False**

Answer: option B

38.The 1's complement of a binary number is derived by changing 0s to 1s and 1s to 0s.

- A)True**
- B)False**

Answer: option A

39.A binary number with four digits has a maximum value of 15.

- A)True**
- B)False**

Answer: option A

40.The 2's complement of a binary number is derived by adding 1 to the 1's complement.

- A)True**
- B)False**

Answer: option A

41.A positive binary number is represented by a 1 sign bit.

- A)True**
- B)False**

Answer: option B

42.The ASCII code is a special code that represents all alphanumeric data.

A)True

B)False

Answer: option A

43.Many digital electronic systems work in hexadecimal instead of binary.

A)True

B)False

Answer: option B

44.In even parity, the sum of the individual bits in the code group must be even.

A)True

B)False

Answer: option B

45.Adding an odd-parity bit to ASCII hex code 2b results in 10101011.

A)True

B)False

Answer: option A

46.Octal-to-binary conversion is accomplished by simply replacing each octal digit with its 4-bit binary equivalent.

A)True

B)False

Answer: option B

47.The hexadecimal numbering system uses base 15.

A)True

B)False

Answer: option B

48.Manufacturers of computers utilize 3-bit codes to indicate operations or instructions.

A)True

B)False

Answer: option B

49.A computer will use ASCII code to store information internally.

A)True

B)False

Answer: option B

Explanation:-

ASCII values not to be used for storage it used to identify the values for each and every element.

FILL IN THE BLANKS

1.A complete alphanumeric code would include 26 lowercase letters, 26 uppercase letters, 10 numeric digits, 7 punctuation marks, and anywhere from _____ to _____ other characters.

- a) 5,10
- b) 10,15
- c) 10,20
- d) 20, 40

Answer: option D

2.Hex 4b5258 is _____ in ASCII code.

- a) Fgm
- b) Klm
- c) Krx
- d) Jqw

Answer: option C

3.Most computers store data in strings of _____ bits called a _____.

- a) 8, word
- b) 8, byte
- c) 16, word
- d) 16, byte

Answer: option B

4.The _____ code represents alphanumeric characters as seven-bit binary numbers.

- a) ASCII
- b) Octal
- c) Alphanumeric
- d) Boy scout

Answer: option A

5.Hexadecimal 16 is _____ in decimal

- a) 32_{10}

- b) 22_{10}
- c) 25_{10}
- d) 27_{10}

Answer: option B

6. Hexadecimal f2 is _____ in binary.

- a) 11100011
- b) 10100001
- c) 11110010
- d) 11111100

Answer: option C

7. The _____ number system has a base of sixteen.

- a) Johnson
- b) Hexadecimal
- c) Binary
- d) Octal

Answer: option B

8. Binary 001011101111110 is _____ in hexadecimal.

- a) $77F2_{16}$
- b) $4EEE_{16}$
- c) $2F7e_{16}$
- d) $2F77_{16}$

Answer: option C

9. The decimal equivalent of the BCD number 1010 is _____.

- a) 8
- b) 10
- c) 12
- d) Invalid

Answer: option D

Explanation:-

The correct answer is option b i.e. 10. By doing lcm we can get the answer.

10. The BCD of decimal numbers is given as:

0 - 0000.

1 - 0001.

2 - 0010.

3 - 0011.

4 - 0100.

5 - 0101.

6 - 0110.

7 - 0111.

8 - 1000.

9 - 1001.

10 - 1010.

The BCD has only maximum of 9 in 4 digits not 10. It is only 1001.

10. The largest unsigned decimal number that can be represented in binary using six bits is _____.

- a) 63
- b) 64
- c) 127
- d) 128

Answer: option A

Explanation:-

$$2^6 - 1 = 63$$

11. The two digits in the binary number system are ___ and ___.

- a) 1, 2
- b) H,I
- c) T,f
- d) 0,1

Answer: option D

12. Decimal 37 is _____ in binary with an even parity bit.

- a) 00100101
- b) 10100101
- c) 11000100
- d) 01001011

Answer: option B

13. The decimal fraction $1/4$ can be written in binary as_____.

- a) 0.010
- b) 0.100
- c) 0.110
- d) 0.011

Answer: option A

14. Decimal 474 is _____ in BCD.

- a) 0100 0111 0100
- b) 0100 1011 0101
- c) 0100 1001 0011
- d) 0110 1011 1001

Answer: option A

15.An unweighted code in which only one bit changes from one code number to the next is _____.

- a) BCD
- b) EXCESS-3
- c) GRAY
- d) ASCII

Answer: option C

16.Binary 10111111 is _____ in hexadecimal.

- a) BF₁₆
- b) FB₁₆
- c) 277₁₆
- d) 10111111

Answer: option A

Explanation:-

1 to 9 are used same binary but 9 to 15 take a b c d e f for number.

1010 = a.

1011 = b.

1100 = c.

1101 = d.

1110 = e.

1111 = f.

Hence,

b = 1011.

F = 1111.

17.Hexadecimal 44 is _____ in binary.

- a) 01000100
- b) 10011010
- c) 01011000
- d) 10001100

Answer: option A

18.Resistors—usually 300 Ω apiece—inserted between a decoder and a 7-segment display are _____.

- a) Pull-up resistors to keep logic high when the input is open
- b) Sense resistors to enable a test of logic levels
- c) Current limiting resistors for the 7-segment display
- d) Surge resistors to prevent damage from power-line variations

Answer: option C

19.Adding a zero to the leftmost bit of an ASCII code is called

_____.

- a) Extra-zero
- b) Zero-padding

Answer: option B

20. The largest BCD number that can be represented with four binary bits is _____.

- a) 9
- b) 10
- c) 15
- d) 16

Answer: option A

21. Binary-coded-decimal 0111 1001 0011 is _____ in binary.

- a) 011110010011
- b) 010110101111
- c) 001100110011
- d) 001100011001

Answer: option D

22. Decimal 12 is _____ in hexadecimal.

- a) 12_{16}
- b) C_{16}
- c) $A2_{16}$
- d) A_{16}

Answer: option B

23. Hexadecimal AA is _____ in decimal.

- a) 165_{10}
- b) 170_{10}
- c) 186_{10}
- d) 176_{10}

Answer: option B

24. Decimal 42 is equivalent to binary _____.

- a) 01000010
- b) 52
- c) 2a
- d) 101010

Answer: option D

25. The decimal number -128 is represented in the signed 2's complement system as _____.

- a) 1111 1110
- b) 0111 1111

- c) 1000 0000
- d) 1111 1111

Answer: option C

Explanation:-

Question is decimal number of 128 in 2's complement.

(e.x) 2|128

2|64-0

2|32-0

2|16-0

2|8-0

2|4-0

2|2-0

2|1-0

binary value is : 1000 0000

1's complement : 0111 1111

2's complement : 1000 0000

26. Odd-parity $9E_{16}$ is _____ decimal.

- a) 30
- b) 158
- c) 78
- d) Nothing. Parity does not check.

Answer: option A

Explanation:-

What does odd parity mean?

In asynchronous communication systems, odd parity refers to parity checking modes, where each set of transmitted bits has an odd number of bits. If the total number of ones in the data plus the parity bit is an odd number of ones, it is called odd parity. If the data already has an odd number of ones, the value of the added parity bit is 0, otherwise it is 1.
 $9E = 1001\ 1110$.

MSB 1 odd parity bit, 0011110 is data.

So 11110 -> 30(decimal).

27. Hexadecimal 12 is _____ in binary.

- a) 00010111
- b) 00010100
- c) 00010010
- d) 00100001

Answer: option C

28.Overflow can occur if two signed numbers are added and _____.

- a) They have opposite signs
- b) They have the same sign
- c) Both of the above
- d) None of the above

Answer: option B

29.A typical CD-ROM can store _____ of digital data.

- a) 90 minutes
- b) Analog portions
- c) 650 megabytes
- d) Octal bytes

Answer: option C

30.The MSB of 11001 is _____.

- a) 1
- b) 1100
- c) C
- d) 19_{16}

Answer: option A

31._____ symbols are needed to represent all digits in hexadecimal.

- a) Six
- b) Ten
- c) Tweleve
- d) Sixteen

Answer: option D

32.In the decimal number 481, the powers-of-10 weight of the digit 4 is _____.

- a) 400
- b) 10^2
- c) 10^4
- d) 100

Answer: option B

33.Decimal 2875 is _____ bytes in binary.

- a) 2
- b) 3
- c) 4
- d) 5

Answer: option A

34.Even-parity 01101000 binary is _____ in hexadecimal.

- a) C8₁₆
- b) 68₁₆
- c) D0₁₆
- d) Nothing. Parity does not check.

Answer: option D

35.The column weight of the "1" in the hexadecimal number 1AB is _____.

- a) 64
- b) 256
- c) 512
- d) 1024

Answer: option B

$$1ab = 0001\ 1010\ 1011.$$

$$256 = 1.$$

$$128 = 1.$$

$$64 = 0.$$

$$32 = 1.$$

$$16 = 0.$$

$$8 = 1.$$

$$4 = 0.$$

$$2 = 1.$$

$$1 = 1.$$

36.In binary, the decimal number 93 converts to _____ digits.

- a) Seven
- b) Eight
- c) 11
- d) Five

Answer: option A

Explanation:-

93 is 1011101 in binary. So count the number of zero and one.

37.The 2's complement of the binary number 1000 is _____.

- a) 111
- b) 0110
- c) 1110
- d) 1000

Answer: option D

38.Hexadecimal 44 is _____ in decimal.

- a) 68_{10}
- b) 74_{10}
- c) 77_{10}
- d) 98_{10}

Answer: option A

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3.LOGIC GATES

1.The output of an AND Gate with three inputs, a, b, and c, is high when _____.

- a) A = 1, b = 1, c = 0
- b) A = 0, b = 0, c = 0
- c) A = 1, b = 1, c = 1
- d) A = 1, b = 0, c = 1

Answer: option C

Explanation:-

A b o/p

0 0 0

0 1 0

1 0 0

1 1 1

for AND Gate o/p is high, when all inputs are high.

2.If a 3-input NOR Gate has eight input possibilities, how many of those possibilities will result in a high output?

- a) 1
- b) 2
- c) 7
- d) 8

Answer: option A

Explanation:-

Truth table of nor

Actually the truth table for NOR Gate is given by

a b y

0 0 1

0 1 0

1 0 0

1 1 0

And similarly truth table for 3input NOR Gate s

a b c y

0 0 0 1

0 0 1 0

0 1 0 0

0 1 1 0

1 0 0 0

1 0 1 0
1 1 0 0
1 1 1 0

so, only one output is high.hence option a is the correct option to be elected which was given in the choices

3.If a signal passing through a gate is inhibited by sending a low into one of the inputs, and the output is high, the gate is a(n):

- a) AND
- b) NAND
- c) NOR
- d) OR

Answer: option B

Explanation:-

NAND Gate

4.A device used to display one or more digital signals so that they can be compared to expected timing diagrams for the signals is a:

- a) Dmm
- b) Spectrum analyzer
- c) Logic analyzer
- d) Frequency counter

Answer: option C

Explanation:-

- **Logic Analyser**:-A logic analyzer is an electronic instrument which displays signals in a digital circuit. A logic analyzer may convert the captured data into timing diagrams, protocol decodes, state machine traces, assembly language, or correlate assembly with source-level software.
- **DMM**:-DMM is a multimeter or a multimeter, also known as a vomm (volt-ohm meter), is an electronic measuring instrument that combines several measurement functions in one unit. A typical multimeter would include basic features such as the ability to measure voltage, current, and resistance. Multimeters may use analog or digital circuits-analog multimeters (amm) and digital multimeters (often abbreviated dmm or dvom.).

Spectrum Analyser:-Spectrum analyser:a spectrum analyzer measures the magnitude of an input signal versus frequency within the full frequency range of the instrument. The primary use is to measure the power of the spectrum of known and unknown signals.

Frequency Counter:-A frequency counter is an electronic instrument, or component of one, that is used for measuring frequency. Frequency counters usually measure the number of oscillations or pulses per second in a repetitive electronic signal. Such an instrument is sometimes referred to as a cymometer.

5. When used with an ic, what does the term "quad" indicate?

- a) 2 circuits
- b) 4 circuits
- c) 6 circuits
- d) 8 circuits

Answer: option B

Explanation:-

In terms of ic, 2 indicates "dual" & 4 indicates "quad".

6. The output of an OR Gate with three inputs, a, b, and c, is low when _____.

- a) A = 0, b = 0, c = 0
- b) A = 0, b = 0, c = 1
- c) A = 0, b = 1, c = 1
- d) All the above

Answer: option A

Explanation:-

Bcoz OR Gate performs addition between two variables.

If we want low output, then all variables values should be low, if any one of the value becomes high, then the output of OR Gate will be high.

A b c output($a+b+c$) truth table.

0 0 0 0

0 0 1 1

0 1 0 1

0 1 1 1

1 0 0 1

1 0 1 1

1 1 0 1

1 1 1 1

7. Which of the following logical operations is represented by the + sign in boolean algebra?

- a) Inversion
- b) And

- c) Or
- d) Complementation

Answer: option C

Explanation:-

- OR Gate performs addition.
- AND Gate performs multiplication.
- NOT Gate performs inversion.

8. Output will be a low for any case when one or more inputs are zero for a(n):

- a) OR GATE
- b) NOT GATE
- c) AND GATE
- d) NOR GATE

Answer: option C

Explanation:-

AND Gate operation is multiplication so any one of the input '0' the total o/p also '0'.

Ex:

a	b	c	y
0	1	1	0
1	1	0	0
1	0	1	0
1	0	1	0

9. How many pins does the 4049 ic have?

- a) 14
- b) 16
- c) 18
- d) 20

Answer: option B

Explanation:-

Inverter: 1 input 1 output

hex inverter: 6 input 6 output

that constitutes 12 pins

2 not connected

2 vcc and gnd

thus, total = $12+2+2=16$

10.Which of the following choices meets the minimum requirement needed to create specialized waveforms that are used in digital control and sequencing circuits?

- a) Basic gates, a clock oscillator, and a repetitive waveform generator
- b) Basic gates, a clock oscillator, and a johnson shift counter
- c) Basic gates, a clock oscillator, and a demorgan pulse generator
- d) Basic gates, a clock oscillator, a repetitive waveform generator, and a johnson shift counter

Answer: option A

Explanation:-

Specialized waveform are additional feature added in function generators there maximum output frequency will often be much less than the typical sine and square wave frequencies available from the generator.

Function generator contains a electronic oscillator which generates repetitive waveform.

11.TTL operates from a _____.

- a) 9-volt supply
- b) 3-volt supply
- c) 12-volt supply
- d) 5-volt supply

Answer: option D

Explanation:-

Logic families are two types:

1.bipolar logic families

a.saturated

b.non-saturated

2.unipolar logic families

a.PMOS

b.NMOS

c.CMOS

Transistor transistor logic, level 2.5 to 5v.

Transistor-transistor logic (TTL) is a class of digital circuits built from bipolar junction transistors (BJT) and resistors. It is called transistor-transistor logic because both the logic gating function (e.g., and) and the amplifying function are performed by transistors (contrast with rtl and dtl).

CMOS is a technology used for constructing ic's, microprocessor micro-controllers, image sensor, highly integrated trans-receiver, image sensors

and other digital logic circuits. CMOS devices are generally high noise immunity and low static power dissipation.

12.The output of a nOR Gate is high if _____.

- a) All inputs are high
- b) Any input is high
- c) Any input is low
- d) All inputs are low

Answer: option D

Explanation:-

13.The switching speed of CMOS is now _____.

- a) Competitive with TTL
- b) Three times that of TTL
- c) Slower than TTL
- d) Twice that of TTL

Answer: option A

Explanation:-

Msi and ssi implemented with TTL ,lsi and vlsi are implemented with CMOS because they require less area on chip and consumes less power.

CMOS has lower power consumption and switching speed(propagation delay)than TTL and CMOS is most certainly used in ic's and processors. So to use lsi scale and low delay CMOS is dominant.

14.The format used to present the logic output for the various combinations of logic inputs to a gate is called a(n):

- a) Boolean constant
- b) Boolean variable
- c) Truth table
- d) Input logic function

Answer: option C

Explanation:-

Truth table is used to represent the inputs and output of corresponding logic functions to understand the function clearly.

15.The power dissipation, p_d , of a logic gate is the product of the _____.

- a) Dc supply voltage and the peak current
- b) Dc supply voltage and the average supply current
- c) Ac supply voltage and the peak current
- d) Ac supply voltage and the average supply current

Answer: option B

Explanation:-

Each gate is connected to a power supply vcc (vdd in the case of CMOS). Draws a certain amount of current during its operation. Since each gate can be in a high state, transition or low state, there are three distinguish currents drawn from power supply.

ICCH : current drawn during high state.

ICCT: current drawn during high to low, low to high transition.

ICCL : current drawn during low state.

For TTL, icct the transition current is negligible, in comparison to icch and iccl. If we assume that icch and iccl are equal then,

$$\text{average power dissipation} = \text{vcc} * (\text{icch} + \text{iccl})/2$$

for CMOS, icch and iccl current is negligible, in comparison to icct. So the average power dissipation is calculated as below.

$$\text{Average power dissipation} = \text{vcc} * \text{icct}.$$

So for TTL like logic family, power dissipation does not depend on frequency of operation, and for CMOS the power dissipation depends on the operation frequency.

Other this, power dissipation can be classified into static power dissipation and dynamic power dissipation.

- Ps (static power dissipation) : power consumed when the output or input are not changing or rather when clock is turned off. Normally static power dissipation is caused by leakage current. (as we reduce the transistor size, i.e. Below 90nm, leakage current could be as high as 40% of total power dissipation).
- Pd (dynamic power dissipation) : power consumed during output and input transitions, so we can say pd is actual power i.e. Power consumed by transistors + leakage current.

Thus total power dissipation is

$$\text{total power dissipation} = \text{static power dissipation} + \text{dynamic power dissipation.}$$

16.A logic probe is again applied to the pins of a 7421 ic with the following results. Is there a problem with the circuit and if so, what is the problem?

pin	indicator	pin	indicator
1	ON	14	ON
2	PULSING	13	ON
3	DIM	12	ON
4	ON	11	DIM
5	ON	10	OFF
6	PULSING	9	PULSING
7	OFF	8	OFF

- a) Pin 6 should be on.
- b) Pin 8 should be on.
- c) Pin 6 should be pulsating.
- d) No problem

Answer: option D

Explanation:-

Ic 7421 is 4 input single output dual AND Gate ic.

Pin no 1, 2, 4 & 5 are inputs to the first AND Gate. Output is pin no: 6.

So first AND Gate output is pulsing because(logic 1 and pulsing and logic 1 and logic 1).

Pin no 14 is power supply to the ic, pin no 13, 12, 10 & 9 are inputs to the second AND Gate. Output is pin no: 8.

So second AND Gate output is off or logic 0 because(logic 1 and logic 1 and logic 0 and pulsing).

So overall there is "no problem" in the circuit or ic.

17.If a 3-input AND Gate has eight input possibilities, how many of those possibilities will result in a high output?

- a) 1
- b) 2
- c) 7
- d) 8

Answer: option A

Explanation:-

For 3-input AND Gate: the output $y = a * b * c$

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0

1 1 0 0

1 1 1 1 <== on this case only the output will be high.
Therefore, the answer is 1 possibility.

18.A CMOS ic operating from a 3-volt supply will consume _____.

- a) Less power than a TTL ic
- b) More power than a TTL ic
- c) The same power as a TTL ic
- d) No power at all

Answer: option A

Explanation:-

CMOS is the advanced version of TTL. So it consumes less power than TTL.

19.What are the pin numbers of the outputs of the gates in a 7432 ic?

- a) 3, 6, 10, and 13
- b) 1, 4, 10, and 13
- c) 3, 6, 8, and 11
- d) 1, 4, 8, and 11

Answer: option C

Explanation:-

7432 is a 14 pin ic is An OR Gate.

Pin description

- 1 a input gate 1
- 2 b input gate 1
- 3 y output gate 1
- 4 a input gate 2
- 5 b input gate 2
- 6 y output gate 2
- 7 ground
- 8 y output gate 3
- 9 a input gate 3
- 10 b input gate 3
- 11 y output gate 4
- 12 a input gate 4
- 13 b input gate 4
- 14 positive supply

so 3, 6, 8, 11 are output pins for OR Gate.

20.What does the small bubble on the output of the nAND Gate logic symbol mean?

- a) Open collector output

- b) Tristate**
- c) The output is inverted.**
- d) None of the above**

Answer: option C

Explanation:-

Already NAND Gate is the inversion of AND Gate and the small bubble on the output indicates the NOT Gate operation and thus the output is the inverted form.

21.The output of a NOT Gate is high when _____.

- a) The input is low**
- b) The input is high**
- c) Power is applied to the gate's ic**
- d) Power is removed from the gate's ic**

Answer: option A

Explanation:-

If input is zero (low) then output will be 1 (high). Because NOT Gate performs invert operation.

22.If the input to a NOT Gate is a and the output is x, then _____.

- a) $X = a$**
- b) $X = \bar{A}$**
- c) $X = 0$**
- d) None of the above**

Answer: option B

Explanation:-

Because it is the inversion of the input

23.A logic probe is used to test the pins of a 7411 ic with the following results. Is there a problem with the chip and if so, what is the problem?

pin	indicator	pin	indicator
1	ON	14	ON
2	PULSING	13	ON
3	PULSING	12	PULSING
4	ON	11	ON
5	ON	10	OFF
6	OFF	9	ON
7	OFF	8	OFF

- a) Pin 6 should be on.
- b) Pin 6 should be pulsing.
- c) Pin 8 should be on.
- d) No problem

Answer: option B

Explanation:-

Because, pulsing means it will be 0 or 1. It is a 3i/p AND Gate; and here 6 is the o/p of the i/p=3,4,5; here 4i/p=1; 5i/p=1 and only 3 is pulsing; so the ans will be 0 or 1;
so ans is also pulsing.

24. How many inputs of a four-input AND Gate must be high in order for the output of the logic gate to go high?

- a) Any one of the inputs
- b) Any two of the inputs
- c) Any three of the inputs
- d) All four inputs

Answer: option D

Explanation:-

If any of the input is low then output goes low so it is necessary that all input (four input) must be high.

25. If the output of a three-input AND Gate must be a logic low, what must the condition of the inputs be?

- a) All inputs must be low.
- b) All inputs must be high
- c) At least one input must be low.
- d) At least one input must be high.

Answer: option C

Explanation:-

Inputs = a, b, c. And output = y. So resultant will be $y = abc$.

Truth table of AND Gate:

a	b	c	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

26. Logically, the output of a nOR Gate would have the same boolean expression as a(n):

- a) NAND Gate immediately followed by an inverter
- b) OR Gate immediately followed by an inverter
- c) AND Gate immediately followed by an inverter
- d) NOR Gate immediately followed by an inverter

Answer: option B

27. A logic probe is placed on the output of a gate and the display indicator is dim. A pulser is used on each of the input terminals, but the output indication does not change. What is wrong?

- a) The dim indication on the logic probe indicates that the supply voltage is probably low.
- b) The output of the gate appears to be open.
- c) The dim indication is the result of a bad ground connection on the logic probe.
- d) The gate is a tristate device.

Answer: option B

Explanation:-

When output does not appear, at that time only one problem occurred like not proper connection between output & probe.

28. What is the boolean expression for a three-input AND Gate?

- a) $X = a + b + c$
- b) $X = a \cdot b \cdot c$
- c) $A - b - c$
- d) $A \$ b \$ c$

Answer: option B

Explanation:-

Because and means multiplication so the answer is b.

29.Which of the following gates has the exact inverse output of the OR Gate for all possible input combinations?

- a) NOR
- b) NOT
- c) NAND
- d) AND

Answer: option A

Explanation:-

Nor is the complement of or. So every input is opposite

30.What is the difference between a 7400 and a 7411 ic?

- a) 7400 has two four-input nAND Gates; 7411 has three three-input AND Gates
- b) 7400 has four two-input nAND Gates; 7411 has three three-input AND Gates
- c) 7400 has two four-input AND Gates; 7411 has three three-input nAND Gates
- d) 7400 has four two-input AND Gates; 7411 has three three-input nAND Gates

Answer: option B

Explanation:-

7400 - quad 2 input NAND Gate.

7411 - triple input AND Gate.

31.Write the boolean expression for an inverter logic gate with input c and output y.

- a) $Y=c$
- b) $Y = \bar{c}$

Answer: option B

32.The output of an exclusive-OR Gate is high if _____.

- a) All inputs are low
- b) All inputs are high
- c) The inputs are unequal
- d) None of the above

Answer: option C

Explanation:-

In fact, output of exclusive-OR Gate is high if the no.of 1's is odd.

33.A clock signal with a period of 1 μ s is applied to the input of an enable gate. The output must contain six pulses. How long must the enable pulse be active?

- a) Enable must be active for 0 μ s
- b) Enable must be active for 3 μ s
- c) Enable must be active for 6 μ s
- d) Enable must be active for 12 μ s

Answer: option C

Explanation:-

1 pulse doesn't mean a positive half part.

It means a complete period of pulse. So if output needs 6 pulses the enable need to be active for 6 times i.e $6 \times 1\mu\text{s}$.

34.The and function can be used to _____ and the or function can be used to _____

- a) Enable, disable
- b) Disable, enable
- c) Enable or disable
- d) Detect, invert

Answer: option C

Explanation:-

Or AND Gates can be used as switch operation.

Perhaps invert operation is not possible using or AND Gates.

35.One advantage TTL has over CMOS is that TTL is _____.

- a) Less expensive
- b) Not sensitive to electrostatic discharge
- c) Faster
- d) More widely available

Answer: option B

Explanation:-

In TTL the conduction is only due to charge carriers (i.e. , holes and electrons) but not with electrostatic field elements like fet.

36.A 2-input nOR Gate is equivalent to a _____.

- a) Negative-OR Gate
- b) Negative-AND Gate
- c) Negative-nAND Gate
- d) None of the above

Answer: option B

Explanation:-

AND ==negative==> NOR
OR ==negative==> NAND
NAND ==negative==> OR
NOR ==negative==> AND

37.If a 3-input OR Gate has eight input possibilities, how many of those possibilities will result in a high output?

- a) 1
- b) 2
- c) 7
- d) 8

Answer: option C

Explanation:-

In OR Gate if any input is one the output will be one and truth table has given below for 3 inputs

000-0->except this input all are having output high(i.e 1).

001-1.
010-1.
011-1.
100-1.
101-1.
110-1.
111-1.

So, total -7 output high.

38.Fan-out is specified in terms of _____.

- a) Voltage
- b) Current
- c) Wattage
- d) Unit loads

Answer: option D

Explanation:-

The maximum fan-out of an output measures its load-driving capability: it is the greatest number of inputs of gates of the same type to which the output can be safely connected.

39.How many input combinations would a truth table have for a six-input AND Gate?

- a) 32
- b) 48
- c) 64

d) 128

Answer: option C

Explanation:-

The truth table formula is 2^n .

N= number of variable.

For example : 6 input variable.

$$2^6=64.$$

40.What is the circuit number of the ic that contains four two-input AND Gates in standard TTL?

- a) 7402
- b) 7404
- c) 7408
- d) 7432

Answer: option C

Explanation:-

7400 - nand,

7402 - nor,

7404 - not,

7408 - and,

7432 - or,

7486 - xor.

41.The terms "low speed" and "high speed," applied to logic circuits, refer to the _____.

- a) Rise time
- b) Fall time
- c) Propagation delay time

Answer: option C

Explanation:-

I think speed of the component is depends only on clock speed but here it is not asking about the component speed here they are asking why we are applying low speed and fast speed.

42.The nor logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

- a) Or
- b) and
- c) Nand
- d) None of the above

Answer: option A

Explanation:-

Yes option a is correct. Because in or operation input is 00,01,10,11,then o/p will be 0,1,1,1and after inverting o/p will be 1,0,0,0 which as same as NOR Gate

43.The logic expression for a nOR Gate is _____.

- a) $X = \bar{A} + B$
- b) $X = A + \bar{B}$
- c) $X = A + B$
- d) $X = \overline{A + B}$

Answer: option D

Explanation:-

And = $a * b$, nand = $\neg(a * b)$.

Or = $a + b$, nor: $\neg(a + b)$.

Not = $\neg a$.

44.With regard to an AND Gate, which statement is true?

- a) An AND Gate has two inputs and one output.
- b) An AND Gate has two or more inputs and two outputs.if one input to a 2-input AND Gate is high, the output reflects the other input.
- c) A 2-input AND Gate has eight input possibilities.

Answer: option C

Explanation:-

This problem can be consider like as it is AND Gate for this we require 2 input. We also know if both the inputs are high the result will be 1 or high. So if one input of 2-input AND Gate is high, the output depends upon other input.

45.The term "hex inverter" refers to:

- a) An inverter that has six inputs
- b) Six inverters in a single package
- c) A six-input symbolic logic device
- d) An inverter that has a history of failure

Answer: option B

Explanation:-

The hex inverter is an integrated circuit that contains six (hexa-) inverters. For example, the 7404 TTL chip which has 14 pins and the 4049 CMOS chip which has 16 pins, 2 of which are used for power/referencing, and 12 of

which are used by the inputs and outputs of the six inverters (the 4049 has 2 pins with no connection).

46.How many inputs are on the logic gates of a 74hc21 ic?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option D

Explanation:-

The right answer is d because 74hc21 is dual 4-input AND Gate TTL ic.

47.The basic logic gate whose output is the complement of the input is the:

- a) OR Gate
- b) AND Gate
- c) Inverter
- d) Comparator

Answer: option C

48.When reading a boolean expression, what does the word "not" indicate?

- a) The same as
- b) Inversion
- c) High
- d) Low

Answer: option B

49.The output of an exclusive-nOR Gate is high if _____.

- a) The inputs are equal
- b) One input is high, and the other input is low
- c) The inputs are unequal
- d) None of the above

Answer: option A

Explanation:-

In OR Gate:

a	b	y
0	0	0
0	1	1
1	0	1
1	1	1

EX-OR Gate:

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

EX-NOR Gate:

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

50. How many AND Gates are found in a 7411 ic?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option C

Explanation:-

Note:-

7411ic contains 14 pins. Out of which 1 is +vcc and 1 is gnd .now left 12 pins. One AND Gate requires 3 pins (2 for i/p and 1 for o/p).so there should be 4 AND Gates. 2 on one side and 2 on other side.

54ls11/dm54ls11/dm74ls11 / 74hc11 / 74hct11 / dm74ls11 : triple 3-input

AND Gates

7411 general description

this device contains three independent gates each of which performs the logic and function.

7411 absolute maximum ratings:

- * supply voltage: 7v
- * input voltage: 7v
- * operating free air temperature range : 0 c to +70 c
- * storage temperature range: -65 c to +150 c

triple input...one output. So 3 AND Gates.

51.Which of the following equations would accurately describe a four-input OR Gate when a = 1, b = 1, c = 0, and d = 0?

- a) $1 + 1 + 0 + 0 = 01$
- b) $1 + 1 + 0 + 0 = 1$
- c) $1 + 1 + 0 + 0 = 0$
- d) $1 + 1 + 0 + 0 = 00$

Answer: option B

Explanation:-

We can use + because or use + symbol.

$1+1=1$, $1+0=1$, $1+0=1$.

So answer is 1.

52.What is the name of a digital circuit that produces several repetitive digital waveforms?

- a) An inverter
- b) An OR Gate
- c) A johnson shift counter
- d) An AND Gate

Answer: option C

Explanation:-

There are two types of shift counters.

- 1) straight shift counter (only able to move 1 bit, i.e. There can be only one "1" in all the bits).
- 2) johnson counter (able to circulate a particular pattern irrespective of number of "1"s).

53.The basic types of programmable arrays are made up of

- a) AND Gates
- b) OR Gates
- c) Nand and nOR Gates
- d) AND Gates and OR Gates

Answer: option D

Explanation:-

A programmable logic array (pla) is a kind of programmable logic device used to implement combinational logic circuits. The pla has a set of programmable AND Gate planes, which link to a set of programmable OR Gate planes, which can then be conditionally complemented to produce an output.

54.The logic gate that will have high or "1" at its output when any one (or more) of its inputs is high is a(n):

- a) OR Gate
- b) AND Gate
- c) NOR Gate
- d) Not operation

Answer: option A

55.CMOS ic packages are available in _____.

- a) Dip configuration
- b) Soic configuration
- c) Dip and soic configurations
- d) Neither dip nor soic configurations

Answer: option C

Explanation:-

Small outline integrated circuit (soic).

Dual inline package (dip).

56.Which of the following is not a basic boolean operation?

- a) OR
- b) NOT
- c) AND
- d) NOR

Answer: option D

57.Which of the following gates is described by the expression

$$X = \overline{ABCD} ?$$

- a) OR
- b) AND
- c) NOR
- d) NAND

Answer: option D

Explanation:-

When we have taken four input nAND Gate it will give compliment of aBCD.

58.What is the boolean expression for a four-input OR Gate?

- a) $Y = a + b + c + d$
- b) $Y = a \square b \square c \square d$
- c) $Y = a - b - c - d$
- d) $Y = a \$ b \$ c \$ d$

Answer: option A

59.How many truth table entries are necessary for a four-input circuit?

- a) 4
- b) 8
- c) 12
- d) 16

Answer: option D

Explanation:-

$$2^4=16$$

60.How many entries would a truth table for a four-input nAND Gate have?

- a) 2
- b) 8
- c) 16
- d) 32

Answer: option C

Explanation:-

0 0 0 1

1 0 0 1

1 0 1 1

1 1 1 0

total = 16 nos.

No of combinations = $2^4 = 16$.

61.The boolean expression for a 3-input OR Gate is _____.

- a) $X = a + b$
- b) $X = a + b+c$
- c) $X = abc$
- d) $X = a + bc$

Answer: option B

62.From the truth table for a three-input nOR Gate, what is the only condition of inputs a, b, and c that will make the output x high?

- a) A = 1, b = 1, c = 1
- b) A = 1, b = 0, c = 0
- c) A = 0, b = 0, c = 1
- d) A = 0, b = 0, c = 0

Answer: option D

63.The logic gate that will have a low output when any one of its inputs is high is the:

- a) NAND Gate
- b) AND Gate
- c) NOR Gate
- d) OR Gate

Answer: option C

64. The output of a nAND Gate is low if _____.

- a) All inputs are low
- b) All inputs are high
- c) Any input is low
- d) Any input is high

Answer: option B

Explanation:-

When all inputs are low then output of AND Gate is low, nAND Gate is quietly opposite to the AND Gate because of ans is b.

TRUE/FALSE

1. A truth table illustrates how the input level of a gate responds to all the possible output level combinations.

- A)True
- B)False

Answer: option B

Explanation:-

A truth table illustrates how the input level of a gate responds to all the possible input (not output) level combinations.

2. A nOR Gate output is low if any of its inputs is low.

- A)True
- B)False

Answer: option B

Explanation:-

NOR Gate is opposite to OR Gate.

NOR Gate produce 1 if both inputs are 0.

3. As a rule, CMOS has the lowest power consumption of all ic families.

- A)True
- B)False

Answer: option A

4.A popular waveform generator is the johnson shift counter.

- A)True
- B)False

Answer: option A

5.Good troubleshooting is done by looking at the input signal and how it interacts with the circuits.

- A)True
- B)False

Answer: option B

Explanation:-

The process of solving a problem or determining a problem to an issue. Troubleshooting often involves the process of elimination, where a technician will follow a set of steps in order to determine the problem or resolve the problem

6.A nOR Gate and an OR Gate operate in exactly the same way.

- A)True
- B)False

Answer: option B

Explanation:-

NOR->NOT+OR

7.An or array is programmed by blowing fuses to eliminate selected variables from the output functions.

- A)True
- B)False

Answer: option A

8.A nAND Gate output is low only if all the inputs are high.

- A)True
- B)False

Answer: option A

9.An AND Gate output is low if all the inputs are high.

- A)True
- B)False

Answer: option B

10.Power is connected to pins 7 and 14 of a 7408 quad two-input AND Gate ic to allow voltage for all four AND Gates on the ic.

- A)True

B)False

Answer: option B

Explanation:-

Pin 7 is ground.

11.An exclusive-nOR Gate output is high when the inputs are unequal.

A)True

B)False

Answer: option B

12.An OR Gate output is high only if all the inputs are high.

A)True

B)False

Answer: option B

Explanation:-

For OR Gate truth table is:

0 0 0

0 1 1

1 0 1

1 1 1

13.A waveform can be enabled or disabled by both and and OR Gates.

A)True

B)False

Answer: option A

14.An exclusive-OR Gate output is high when the inputs are unequal.

A)True

B)False

Answer: option A

15.In a boolean equation the use of the + symbol represents the or function.

A)True

B)False

Answer: option A

16.A logic gate has one or more output terminals and one input terminal.

A)True

B)False

Answer: option B

17.A logic pulser is used to determine the level of floating in a circuit.

A)True

B)False

Answer: option B

Explanation:-

Logic pulser is used to generate digital waveforms.

18.An inverter output is the complement of its input.

A)True

B)False

Answer: option A

Explanation:-

Basically inverter o/p is complement of i/p.

19.It is important to memorize logic symbols, boolean equations, and truth tables for logic gates.

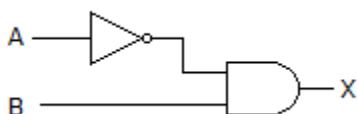
A)True

B)False

Answer: option A

FILL IN THE BLANKS

1.The gates in this figure are implemented using TTL logic. If the input of the inverter is open, and you apply logic pulses to point b, the output of the AND Gate will be _____.



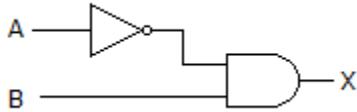
- a) A steady low**
- b) A steady high**
- c) An undefined level**
- d) Pulses**

Answer: option A

Explanation:-

If a is open it mean input to the inverter is 0 so the o/p will be 1. Which is applied to the AND Gate input. So the o/p will be the pulses applied on b.

2.The gates in this figure are implemented using TTL logic. If the output of the inverter is open, and you apply logic pulses to point b, the output of the AND Gate will be _____.



- a) A steady low
- b) A steady high
- c) An undefined level
- d) Pulses

Answer: option D

Explanation:-

If the o/p of inverter is open that means 0 and for b i/p is pulse means 1 so the o/p become 0.

3.If a is low or b is low or both are low, then x is low. If a is high and b is high, then x is high. These rules specify the operation of a(n)

-
- a) AND Gate
 - b) OR Gate
 - c) NAND Gate
 - d) XOR Gate

Answer: option A

Explanation:-

As we know for AND Gate

if both the inputs are low then output is low.

If both are high then output is high.

So it is AND Gate.

Or

Or is also the right answer because.

If both the inputs are low then output is low.

If both the inputs are high then output is high.

4.A major advantage of ecl logic over TTL and CMOS is _____.

- a) Low power dissipation
- b) High speed
- c) Both low power dissipation and high speed
- d) Neither low power dissipation nor high speed

Answer: option B

Explanation:-

Because in ECL, transistor sits upon output transistor so charging and discharging time is less than other gate.

5. The output of an xOR Gate is high only when _____.

- a) Both inputs = 0
- b) Both inputs = 1
- c) The two inputs are unequal
- d) Both inputs are undefined

Answer: option C

6. A 2-input gate that can be used to pass a digital waveform unchanged at certain times and inverted at other times is a(n)

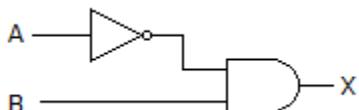
- a) AND Gate
- b) OR Gate
- c) NAND Gate
- d) XOR Gate

Answer: option D

Explanation:-

XOR Gate: suppose for 2 input x-or if one input is fixed to 0 then output would be second input, while if one input is fixed to 1 then output would be inverted form of second input (due to un-equality detection property).

7. The gates in this figure are implemented using TTL logic. If the output of the inverter has an internal open circuit, what voltage would you expect to measure at the inverter's output?



- a) Less than 0.4 v
- b) 1.6 v
- c) Greater than 2.4 v
- d) All of the above

Answer: option B

8. When does the output of a nAND Gate = 1?

- a) Whenever a 0 is present at an input
- b) Only when all inputs = 0
- c) Whenever a 1 is present at an input
- d) Only when all inputs = 1

Answer: option A

9.The number of input combinations for a 4-input gate is _____.

- a) 9
- b) 8
- c) 15
- d) 16

Answer: option D

10.When does the output of a nOR Gate = 0?

- a) Whenever a 0 is present at an input
- b) Only when all inputs = 0
- c) Whenever a 1 is present at an input
- d) Only when all inputs = 1

Answer: option C

11.If r is any register, then $r \text{ xor } r$ is _____.

4.EX-OR AND EX-NOR GATES

1.Select the statement that best describes the parity method of error detection:

- a) Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.**
- b) Parity checking is not suitable for detecting single-bit errors in transmitted codes.**
- c) Parity checking is best suited for detecting single-bit errors in transmitted codes.**
- d) Parity checking is capable of detecting and correcting errors in transmitted codes.**

Answer: option C

Explanation:-

Parity checking is done for single bit correction only.

A parity bit is a bit that is added to ensure that the number of bits with the value one in a set of bits is even or odd. Parity bits are used as the simplest form of error detecting code.

2.A logic circuit that provides a high output for both inputs high or both inputs low is a(n):

- a) Ex-nOR Gate**
- b) OR Gate**
- c) Ex-OR Gate**
- d) NAND Gate**

Answer: option A

Explanation:-

Ex-OR Gate gives 1 if both the inputs are different means 0 or 1. And gives 0 if both are same.

And ex-nor is opposite of ex-OR Gate, so it provides a high output for both inputs high or both inputs low is

truth table for exOR Gate:

in1 in2 out

0	0	0
0	1	1
1	0	1
1	1	0

truth table for OR Gate:

in1 in2 out
0 0 0
0 1 1
1 0 1
1 1 1 (condition violated-out is 1 when both inputs are 1)

truth table for nAND Gate:

in1 in2 out
0 0 1 (condition violated-out is 1 when both inputs are 0)
0 1 1
1 0 1
1 1 0

3. Identify the type of gate below from the equation $X = A \oplus B = \bar{A}B + A\bar{B}$

- a) Ex-nOR Gate
- b) OR Gate
- c) Ex-OR Gate
- d) NAND Gate

Answer: option C

Explanation:-

Ex-or gives 1 on either 10 or 01 and gives 0 if both the inputs are same 11 or 00.

4. How is odd parity generated differently from even parity?

- a) The first output is inverted.
- b) The last output is inverted.

Answer: option B

Explanation:-

Parity bit is added before MSB. So that means we want to convert even parity to odd parity then we will have to invert the MSB bit.

MSB bit always occurs as last output because the output starts coming from LSB side.

5. Parity systems are defined as either _____ or _____ and will add an extra _____ to the digital information being transmitted.

- a) Positive, negative, byte
- b) Odd, even, bit
- c) Upper, lower, digit
- d) On, off, decimal

Answer: option B

6.Which type of gate can be used to add two bits?

- a) Ex-or
- b) Ex-nor
- c) Ex-nand
- d) Nor

Answer: option A

Explanation:-

Yes. XOR Gates are used to implement binary addition in computers.

A b (a xor b)

0 0 0

0 1 1

1 0 1

1 1 0

7.Why is an exclusive-nOR Gate also called an equality gate?

- a) The output is false if the inputs are equal.
- b) The output is true if the inputs are opposite.
- c) The output is true if the inputs are equal.

Answer: option C

Explanation:-

Truth table for ex-nOR Gate is,

i/p o/p

0 0 1

0 1 0

1 0 0

1 1 1

8.Show from the truth table how an exclusive-OR Gate can be used to invert the data on one input if the other input is a special control function.

- a) Using a as the control, when a = 0, x is the same as b. When a = 1, x is the same as b.
- b) Using a as the control, when a = 0, x is the same as b. When a = 1, x is the inverse of b.
- c) Using a as the control, when a = 0, x is the inverse of b. When a = 1, x is the same as b.
- d) Using a as the control, when a = 0, x is the inverse of b. When a = 1, x is the inverse of b.

Answer: option B

Explanation:-

Truth table of ex-OR Gate is.

0 0 0.

0 1 1.

1 0 1.

1 1 0.

Considering 2nd, 4th case answer is b

9.Determine odd parity for each of the following data words:

1011101 11110111 10011101

- a) P = 1, p = 1, p = 0
- b) P = 0, p = 0, p = 0
- c) P = 1, p = 1, p = 1
- d) P = 1, p = 1, p = 1

Answer: option D

Explanation:-

Parity is nothing checking no.of 1's and in the given question it is given to follow odd parity i.e. No.of 1's in given byte should be odd and if it is not odd we need to add 1 in order to make it odd parity.

10.The ex-nor is sometimes called the _____.

- a) Parity gate
- b) Equality gate
- c) Inverted or
- d) Parity gate or the equality gate

Answer: option B

Explanation:-

Because when both the inputs equal output is equal to one.

TRUE/FALSE

1.The odd/even parity system would require a sixth bit to be added to a 4-bit system.

- A)True
- B)False

Answer: option B

2.Electrical noise does not affect the transmission of binary information.

- A)True
- B)False

Answer: option B

3.In an exclusive-or, both inputs cannot be high to provide a high output.

- A)True**
- B)False**

Answer: option A

4.Using the cpld design environment, we can simulate any combinations of inputs and observe the resulting output to check for proper circuit operation.

- A)True**
- B)False**

Answer: option A

5.The exclusive-or provides a low input if one input or the other input is high.

- A)True**
- B)False**

Answer: option B

6.The exclusive-or is written in a boolean equation as a plus sign with a circle around it.

- A)True**
- B)False**

Answer: option A

7.Parity generator and checker circuits are available in single ic packages.

- A)True**
- B)False**

Answer: option A

8.The ex-nor is sometimes called the equality gate.

- A)True**
- B)False**

Answer: option A

9.A parity checker is constructed in the same way as a parity generator, except that in a 4-bit system there must be five inputs, and the output is used as the error indicator.

- A)True**
- B)False**

Answer: option A

10.In a parity generator circuit, an error is signaled on an error indicator.

- A)True**
- B)False**

Answer: option B

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5. BOOLEAN ALGEBRA AND LOGIC SIMPLIFICATION

1. Convert the following sop expression to an equivalent pos expression. $A B C + A \bar{B} \bar{C} + A \bar{B} C + A B \bar{C} + \bar{A} \bar{B} C$

- a) $(\bar{A} + \bar{B} + \bar{C})(A + B + \bar{C})(\bar{A} + B + C)$
- b) $(A + B + C)(A + \bar{B} + C)(A + \bar{B} + \bar{C})$
- c) $(\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + C)(A + \bar{B} + C)$
- d) $(A + B + C)(\bar{A} + B + \bar{C})(A + \bar{B} + C)$

Answer: option B

Explanation:-

Short cut : no. of combination possible with 3 variable is (01234567)

min terms of the abv eq is: 7,4,5,6,1

in pos is taking max terms : remaining numbers is = 0,2,3

min term is : 1 if u get 0 is compliment using method is : sop

max term is : 0 if u get 1 is complement using method is : pos

$$\begin{aligned}F(a,b,c) &= m7+m4+m5+m6+m1 \\&= a'b'c' + ab'c' + ab'c + abc' + a'b'c \\f'(a,b,c) &= m0 + m2 + m3\end{aligned}$$

if we complement f' , we get f ;

$$f = (m0 + m2 + m3)'$$

by demorgan's theorem;

$$\begin{aligned}f &= (a'b'c')'(a'bc')'(a'bc) \\&= (a''+b''+c'')(a''+b'+c'')(a''+b'+c') \\&= (a+b+c)(a+b'+c)(a+b'+c') \\&\text{so answer is letter b.}\end{aligned}$$

2. Determine the values of a, b, c, and d that make the sum term

$\bar{A} + B + \bar{C} + D$ **equal to zero.**

- a) A = 1, b = 0, c = 0, d = 0
- b) A = 1, b = 0, c = 1, d = 0
- c) A = 0, b = 1, c = 0, d = 0
- d) A = 1, b = 0, c = 1, d = 1

Answer: option B

Explanation:-

A is negotiate the value must be 1 so that a value will be zero same like c is negotiate the value must be 1 so that c value will be zero if all the values are zero then if we add those values we will get zero.

3.Which of the following expressions is in the sum-of-products (sop) form?

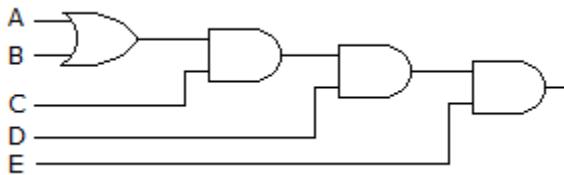
- a) $(a + b)(c + d)$
- b) $(a)b(cd)$
- c) $Ab(cd)$
- d) $Ab + cd$

Answer: option D

Explanation:-

Sop is sum of minterms.here no of variable=4(a,b,c,d)
so $ab+cd$ is not a sop form.for example $aBCD+aBCD'$ is a sop form.which can be written as sum(14,15).because $14=1110$; and $15=1111$ in binary which makes the corresponding minterm logic high.

4.Derive the boolean expression for the logic circuit shown below:



- a) $C(A + B)DE$
- b) $[C(A + B)D + \bar{E}]$
- c) $[(C(A + B)D]\bar{E}]$
- d) $ABCDE$

Answer: option A

Explanation:-

OR Gate op= $(a+b)$
1st and op= $(a+b)c$
2nd and op= $[(a+b)c]d$
3rd and op= $[(a+b)c]d)e$
ans: $[(a+b)c]d)e$ {after simplification}

5.From the truth table below, determine the standard sop expression.

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- a) $X = \bar{A}\bar{B}\bar{C} + A\bar{B}C + A\bar{B}C$
- b) $X = A\bar{B}C + A\bar{B}C + A\bar{B}C$
- c) $X = A\bar{B}C + \bar{A}\bar{B}C + A\bar{B}\bar{C}$
- d) $X = \bar{A}\bar{B}C + \bar{A}\bar{B}C + A\bar{B}\bar{C}$

Answer: option D

Explanation:-

consider output if you get less no of 1's take: sop (sum of product)
 consider output if you get less no of 0's take: pos (product of sum)

6. One of de morgan's theorems states that $\overline{X+Y} = \overline{X} \cdot \overline{Y}$. Simply stated, this means that logically there is no difference between:

- a) A nor and an AND Gate with inverted inputs
- b) A nand and an OR Gate with inverted inputs
- c) A and and an nOR Gate with inverted inputs
- d) A nor and an nAND Gate with inverted inputs

Answer: option A

Explanation:-

Since the LHS of the expression is the logical expression of two inputs nOR Gate and the RHS of the expression consists of two inverted inputs of a and b, that is two inverted input are and to get the rhs of the expression and since according to demorgan laws, the complement of the sum of two or more variables are equivalent to the product of the complement of the individual variables, we can say that a nOR Gate is equivalent to An AND Gate with inverted inputs.

7. The commutative law of boolean addition states that $a + b = a \times b$.

- A) True
- B) False

Answer: option B

8. Applying demorgan's theorem to the expression \overline{ABC} , we get

- a) $\overline{\overline{A} + \overline{B} + \overline{C}}$
b) $\overline{A + B + C}$
c) $A + \overline{B} + C\overline{C}$
d) $A(B + C)$

Answer: option A

Explanation:-

De morgan's theorem states that.

$$(ab)' = a'b'.$$

And

$$(a+b)' = a'b'.$$

So by referring the above,

$$(abc)' = a'b'c' \text{ and } (a+b+c)' = a'b'c' \dots$$

9. The systematic reduction of logic circuits is accomplished by:

- a) Using boolean algebra
b) Symbolic reduction
c) TTL logic
d) Using a truth table

Answer: option A

Explanation:-

The systematic reduction of logic circuit is accomplished by two ways,

1. Boolean algebra method
2. Karnaugh map(k-map) method.

10. Which output expression might indicate a product-of-sums circuit construction?

- a) $X = \overline{CH}(D + E + F)$
b) $X = CG(DE)$
c) $X = \overline{AC + BD + EF}$
d) $X = (C + D)(E + G)$

Answer: option D

Explanation:-

Well, c and d all make sense. In c the whole expression is complimented, if you simplify it, Because in this type 1st we take sum and after this we do product.

11. An AND Gate with schematic "bubbles" on its inputs performs the same function as a(n) _____ gate.

- a) NOT

- b) OR
- c) NOR
- d) NAND

Answer: option C

Explanation:-

And inverted nor.
Or inverted nand.
Nand inverted or.
Nor inverted and.

12. For the sop expression $A\bar{B}C + \bar{A}BC + AB\bar{C}$, how many 1s are in the truth table's output column?

- a) 1
- b) 2
- c) 3
- d) 5

Answer: option C

Explanation:-

Step 1:
consider product inputs: a b c are 1 and a- b- c- as 0.

Step 2:
resulting sop (sum of product) will look like.
 $101+011+110 = x$.
 $5+3+6 = 14$ i.e 1110.

Step 3:
so we have 3 1's in answer.

Answer: 3.

Or

Bar take as 0.

So $a\bar{b}\bar{c} = 1\ 0\ 1 = 5$.

:

:

:

$$5 + 3 + 6 = 14 = 1110 = 1 + 1 + 1 + 0 = 3.$$

13. A truth table for the sop expression $A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$ has how many input combinations?

- a) 1
- b) 2
- c) 4

d) 8

Answer: option D

Explanation:-

Number of input variables used is 3(a, b, c). So, number of input combinations are 8(0 to 7).

14. How many gates would be required to implement the following boolean expression before simplification? $Xy + x(x + z) + y(x + z)$

- a) 1
- b) 2
- c) 4
- d) 5

Answer: option D

Explanation:-

AND Gate (1st) = xy .

OR Gate (1st) = $x+z$.

AND Gate (2nd) = $x(x+z)$.

AND Gate (3rd) = $y(x+z)$.

OR Gate (2nd) = final expression.

So, no. Of total gates = 5.

16. Determine the values of a, b, c, and d that make the product term $\bar{A}B\bar{C}D$ equal to 1.

- a) A = 0, b = 1, c = 0, d = 1
- b) A = 0, b = 0, c = 0, d = 1
- c) A = 1, b = 1, c = 1, d = 1
- d) A = 0, b = 0, c = 1, d = 0

Answer: option A

Explanation:-

Take a and apply values in given term.

$1*1*1*1$ (b=1,bbar=0).so a is correct.

17. What is the primary motivation for using boolean algebra to simplify logic expressions?

- a) It may make it easier to understand the overall function of the circuit.
- b) It may reduce the number of gates.
- c) It may reduce the number of inputs required.
- d) All of the above

Answer: option D

18. How many gates would be required to implement the following boolean expression after simplification? $Xy + x(x + z) + y(x + z)$

- a) 1
- b) 2
- c) 4
- d) 5

Answer: option B

Explanation:-

$$\begin{aligned} & Xy + x(x+z) + y(x+z) \\ & = xy + xx + xz + yx + yz \\ & = xy + x + xz + yx + yz \\ & = x + xz + yx + yz \\ & = x + yx + yz \\ & = x + yz \end{aligned}$$

One AND Gate for yz and one OR Gate for $x+yz$.

Total 2 gates required.

19. $AC + ABC = AC$

- A) True
- B) False

Answer: option A

Explanation:-

Given expression is $ac+abc=ac$

L.H.S

by associative law $ac(1+b)$

and we know that $1+a=1$

.

. . $AC(1)$

and we also know that $a.1=a$

.

. . L.H.S= ac

thus L.H.S. = R.H.S.

20. When \bar{A}, \bar{B} are the inputs to a nAND Gate, according to de morgan's theorem, the output expression could be:

- a) $X = a + b$
- b) $X = \overline{AB}$
- c) $X = (a)(b)$
- d) $X = \overline{AB}$

Answer: option A

Explanation:-

For AND Gate a and $b = a.b$.

For nAND Gate a nand $b = \text{bar}(ab)$.

Inputs are $\text{bar}(a)$ nand $\text{bar}(b) = \text{bar}(\text{bar}(a)+\text{bar}(b)) = a+b$.

21. Which boolean algebra property allows us to group operands in an expression in any order without affecting the results of the operation [for example, $a + b = b + a$]?

- a) Associative
- b) Commutative
- c) Boolean
- d) Distributive

Answer: option B

22. Applying demorgan's theorem to the expression $\overline{(X + Y)} + \overline{Z}$, we get

- a) $(X + Y)Z$
- b) $(\bar{X} + \bar{Y})Z$
- c) $(X + Y)\bar{Z}$
- d) $(\bar{X} + \bar{Y})\bar{Z}$

Answer: option A

Explanation:-

$[(x+y)' + z']'$

$(x+y)''.(z)''$

therefore we get

$(x+y).z$

23. When grouping cells within a k-map, the cells must be combined in groups of _____.

- a) 2s
- b) 1, 2, 4, 8, etc.
- c) 4s
- d) 3s

Answer: option B

Explanation:-

The relationship between no. Of cells(m) and no. Of input variables(n)is given as $m=2^n$

hence when $n=0$ $m=1$

$n=1$ $m=2$

$n=2$ $m=4$

$n=3$ $m=8$ etc.....

24. Use boolean algebra to find the most simplified sop expression for $f = abd + cd + acd + abc + aBCD$.

- a) $F = abd + abc + cd$
- b) $F = cd + ad$
- c) $F = bc + ab$
- d) $F = ac + ad$

Answer: option A

Explanation:-

$$\begin{aligned} & abd+cd+acd+abc+abcd \\ & =abd+cd(1+a)+abc(1+d) \\ & =abd+cd(1)+abc(1).. \text{as}(1+a=1 \& 1+d=1) \\ & =abd+cd+abc \\ & =abd+abc+cd \end{aligned}$$

25. Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as a BCD-to-decimal converter. These result in _____ terms in the k-map and can be treated as either _____ or _____, in order to _____ the resulting term.

- a) Don't care, 1s, 0s, simplify
- b) Spurious, ands, ors, eliminate
- c) Duplicate, 1s, 0s, verify
- d) Spurious, 1s, 0s, simplify

Answer: option A

26. The nand or nOR Gates are referred to as "universal" gates because either:

- a) Can be found in almost all digital circuits
- b) Can be used to build all the other types of gates
- c) Are used in all countries of the world
- d) Were the first gates to be integrated

Answer: option B

Explanation:-

Nand and nOR Gates can be used in place of all basic gates that and ,or & not. They can be used to implement any circuity. We can use only one type of universal gate to implement any circuit.

27. The truth table for the sop expression $AB + \bar{B}C$ has how many input combinations?

- a) 1
- b) 2
- c) 4

d) 8

Answer: option D

Explanation:-

Its has 3 inputs a, b, c so no. Of input combinations is 2^n here $n=3$ so $2^3=8$ hence 8 input combinations.

Or

2 to the power of 3 = 8.

28. Converting the boolean expression $Im + m(no + pq)$ to sop form, we get _____.

- a) $Im + mnopq$
- b) $I + mno + mpq$
- c) $Im + m + no + mpq$
- d) $Im + mno + mpq$

Answer: option D

Explanation:-

$$Im + m(no + pq) = Im + mno + mpq.$$

29. A karnaugh map is a systematic way of reducing which type of expression?

- a) Product-of-sums
- b) Exclusive nor
- c) Sum-of-products
- d) Those with overbars

Answer: option C

30. The boolean expression $X = \bar{A} + \bar{B} + \bar{C}$ is logically equivalent to what single gate?

- a) Nand
- b) Nor
- c) And
- d) Or

Answer: option A

Explanation:-

According to de-morgan's law, $a' + b' = (a \cdot B)'$.

So, applying this to the question,

$$a' + b' + c' = (a \cdot B)' + c'.$$

$$(a \cdot B)' + c' = (a \cdot B \cdot C)'$$
 [applying demorgans theorem again!].

Now, $(a \cdot B \cdot C)' = \text{nAND Gate}$. So in short, bubbled OR Gate= nAND Gate and bubbled AND Gate=nOR Gate.

31. Applying the distributive law to the expression $A(B + \bar{C} + D)$, we get _____.

- a) $AB + AC + AD$
- b) $ABCD$
- c) $A + B + C + D$
- d) $AB + A\bar{C} + AD$

Answer: option D

Explanation:-

$$A(b+c+d) = (a.b)+(ac)+(ad)$$
$$ab+ac+ad$$

32. Mapping the sop expression $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C}$, we get _____.

		C	0	1
		AB	00	
		00		
		01	1	1
		11		1
		10	1	

(A)

		C	0	1
		AB	00	
		00	1	
		01	1	1
		11	1	
		10		

(B)

		C	0	1
		AB	00	
		00		1
		01		
		11	1	1
		10	1	1

(C)

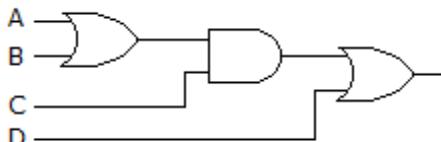
		C	0	1
		AB	00	
		00	1	1
		01		
		11		1
		10	1	

(D)

- a) (A)
- b) (B)
- c) (C)
- d) (D)

Answer: option B

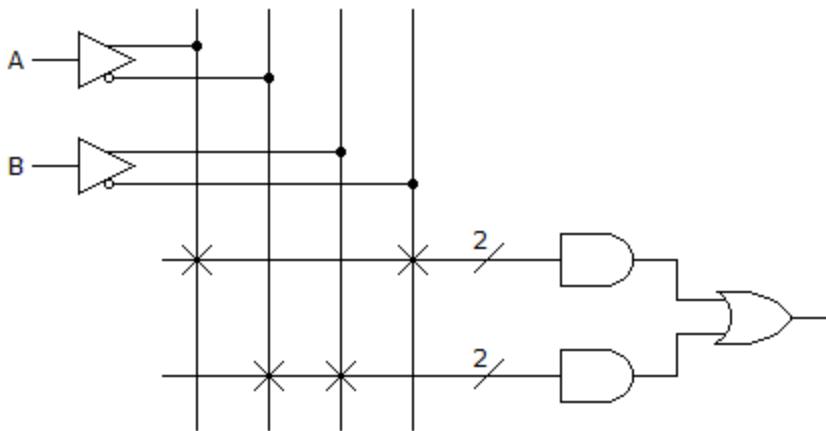
33. Derive the boolean expression for the logic circuit shown below:



- a) $CA + CB + CD$
- b) $C(A + B)\bar{D}$
- c) $C(A + B) + D$
- d) $CA + CB + D$

Answer: option C

34. Which is the correct logic function for this PAL diagram?



- a) $X = \bar{A}\bar{B} + \bar{B}\bar{A}$
- b) $X = A\bar{B} + \bar{B}A$
- c) $X = A\bar{B} + B\bar{A}$
- d) $X = AB + BA$

Answer: option C

Explanation:-

As PAL has programmable and followed by fixed OR Gates. The first AND Gate has inputs as inverted b and uncomplemented a. Also the second AND Gate has similarly inverted a and uncomplemented b as their inputs. Finally the outputs of AND Gates will be OR together leads to the output of x-OR Gate. (option c).

35. For the sop expression $AB + \bar{B}C$, how many 0s are in the truth table's output column?

- a) 0
- b) 1
- c) 4
- d) 5

Answer: option C

Explanation:-

Because we can write it like $(ab(c+c\bar{)}) + b\bar{c}(a+a\bar{})$.

In expanded form it will be $(abc + abc\bar{c}) + (a\bar{b}c + a\bar{b}c\bar{c})$.

So we need 4 one's to represent it & 4 zero's to represent rest.

Or

A b c ab b' b'c ab+b'c

0 0 0 0 1 0 0

0 0 1 0 1 1 1

0 1 0 0 0 0 0

0 1 1 0 0 0 0

1 0 0 0 1 0 0

1 0 1 0 1 1 1
 1 1 0 1 0 0 1
 1 1 1 1 0 0 1

answer contain 4 zeros.

36.Mapping the standard sop expression $A B C \bar{D} + \bar{A} \bar{B} C D + A \bar{B} \bar{C} D + \bar{A} \bar{B} \bar{C} \bar{D}$, we get

		CD	00	01	10	11
AB	CD	00	1			
		01				1
AB	CD	10		1		
		11			1	

(A)

		CD	00	01	10	11
AB	CD	00	1			
		01				1
AB	CD	10		1		
		11			1	

(B)

		CD	00	01	10	11
AB	CD	00		1		
		01				
AB	CD	10				
		11	1			

(C)

		CD	00	01	10	11
AB	CD	00		1	1	
		01				
AB	CD	10				1
		11	1			

(D)

- a) A
- b) B
- c) C
- d) D

Answer: option B

37.Applying demorgan's theorem to the expression $\overline{(W + X + Y)Z}$, we get _____.

- a) $\overline{W \bar{X} \bar{Y} Z}$
- b) $\overline{WXY Z}$
- c) $WXY \bar{Z}$
- d) $\overline{W \bar{X} \bar{Y}} + \bar{Z}$

Answer: option D

38.Which of the examples below expresses the distributive law of boolean algebra?

- a) $(a + b) + c = a + (b + c)$
- b) $a(b + c) = ab + ac$
- c) $a + (b + c) = ab + ac$
- d) $a(bc) = (ab) + c$

Answer: option B

39.Applying demorgan's theorem to the expression $\overline{A + B + C + D}$, we get _____.

- a) $\overline{A} \bar{B} \bar{C} \bar{D}$
- b) $\overline{A} + \bar{B} + \bar{C} + \bar{D}$
- c) $A + \bar{B} + \bar{C} + D$
- d) $\overline{A} + B + C + \bar{D}$

Answer: option A

Explanation:-

According to demorgan's law $(a+b)\bar{=} = a(\bar{ }) + b(\bar{ })$.

40.Which of the following is an important feature of the sum-of-products (sop) form of expression?

- a) All logic circuits are reduced to nothing more than simple and and OR Gates.
- b) The delay times are greatly reduced over other forms.
- c) No signal must pass through more than two gates, not including inverters.
- d) The maximum number of gates that any signal must pass through is reduced by a factor of two.

Answer: option C

41.An OR Gate with schematic "bubbles" on its inputs performs the same functions as a(n)_____ gate.

- a) NOR
- b) OR
- c) NOT
- d) NAND

Answer: option D

Explanation:-

AND ==negative==> NOR

OR ==negative==> NAND

NAND ==negative==> OR

NOR ==negative==> AND

42.Which of the examples below expresses the commutative law of multiplication?

- a) $a + b = b + a$
- b) $ab = b + a$
- c) $ab = ba$
- d) $ab = a \times b$

Answer: option C

Explanation:-

They asked about multiplication. So c is correct.

43.Determine the binary values of the variables for which the following standard pos expression is equal to 0. $(A + \bar{B} + C)(\bar{A} + B + \bar{C})$

- a) $(0 + 1 + 0)(1 + 0 + 1)$
- b) $(1 + 1 + 1)(0 + 0 + 0)$
- c) $(0 + 0 + 0)(1 + 0 + 1)$
- d) $(1 + 1 + 0)(1 + 0 + 0)$

Answer: option A

44.The expression $w(x + yz)$ can be converted to sop form by applying which law?

- a) Associative law
- b) Commutative law
- c) Distributive law
- d) None of the above

Answer: option C

Explanation:-

$W(x+yz)$ applying the distributive law,
 $wx+wyz$, which is in sum of products(sop) form.

45.The commutative law of addition and multiplication indicates that:

- a) We can group variables in an and or in an or any way we want
- b) An expression can be expanded by multiplying term by term just the same as in ordinary algebra
- c) The way we or and two variables is unimportant because the result is the same
- d) The factoring of boolean expressions requires the multiplication of product terms that contain like variables

Answer: option C

46.Which of the following combinations cannot be combined into k-map groups?

- a) Corners in the same row
- b) Corners in the same column
- c) Diagonal
- d) Overlapping combinations

Answer: option C

TRUE/FALSE

1.A variable is a symbol used to represent a logical quantity that can have a value of 1 or 0.

- A)True
- B)False

Answer: option A

2.The or function is boolean multiplication and the and function is boolean addition.

- A)True
- B)False

Answer: option B

Explanation:-

Or is for addition & and is for multiplication.

3.In boolean algebra, $a + 1 = 1$.

- A)True
- B)False

Answer: option A

4.The product-of-sums (pos) is basically the oring of anded terms.

- A)True
- B)False

Answer: option B

5.In boolean algebra, $\bar{a} \cdot a = 0$.

- A)True
- B)False

Answer: option A

6.Sop stands for sum-of-powers.

- A)True
- B)False

Answer: option B

Explanation:-

Sop sum of product

7.The VHDL editor provided with a schematic editor development system will produce a file with the extension .vhd, which can be used by the simulator to test the output of the logic design.

- A)True
- B)False

Answer: option A

8.In the commutative law, in oring and anding of two variables, the order in which the variables are ored or anded makes no difference.

- A)True
- B)False

Answer: option A

9.The binary value of 1010 is converted to the product term $\bar{A}\bar{B}CD$.

- A)True
- B)False

Answer: option B

10. Most boolean reductions result in an equation in only one form.

- A)True
- B)False

Answer: option B

Explanation:-

It may sop or pos form.

11. The symbol shown below is for a 2-input nAND Gate



- A)True
- B)False

Answer: option B

12. A karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

- A)True
- B)False

Answer: option A

13. The process of reduction or simplification of combinational logic circuits increases the cost of the circuit.

- A)True
- B)False

Answer: option B

14. By applying de morgan's theorem to a nOR Gate, two identical truth tables can be produced.

- A)True
- B)False

Answer: option A

15. Five-variable karnaugh maps are impossible.

- A)True
- B)False

Answer: option B

16. If you need a nand, an and, and an inverter you would purchase a 7400 ic.

- A)True

B)False

Answer: option A

17.The systematic reduction of logic circuits is performed using boolean algebra.

A)True

B)False

Answer: option A

18.Cpld software can be used to design original circuits that prove the boolean rules and laws.

A)True

B)False

Answer: option A

Explanation:-

A complex programmable logic device (cpld) is a programmable logic device with complexity between that of PALs and fpgas, and architectural features of both.

19.A karnaugh map is similar to a truth table.

A)True

B)False

Answer: option A

20.Boolean algebra simplifies logic circuits.

A)True

B)False

Answer: option A

Fill in the blanks

1.The boolean expression $c + cd$ is equal to _____.

- a) C
- b) d
- c) $c+d$
- d) 1

Answer: option A

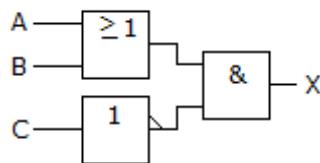
Explanation:-

Because its not distributive law i.e. $C(c+d)$.

Its $c+cd = c(1+d)$.

$=> c*1, c*d = cd$.

2.The boolean expression for the logic circuit shown is _____.



- a) $(A + B)C$
- b) $AB + C$
- c) $(A + B)\bar{C}$
- d) $AB + \bar{C}$

Answer: option C

Explanation:-

1 = NOT Gate.

>1 = OR Gate .

& = AND Gate.

Above notation is as per ieee.

3.Applying demorgan's theorem and boolean algebra to the expression $(\bar{A}\bar{B}) + (\bar{A}\bar{C})$ results in _____.

- a) $A + \bar{C}$
- b) $AB + \bar{AC}$
- c) $\bar{AB}(\bar{A} + C)$
- d) $(\bar{A} + B)(A + \bar{C})$

Answer: option D

Explanation:-

$$((ab') + (a'c))' = (ab')'(a'c)' = (a'+b'')(a''+c') = (a'+b)(a+c').$$

4.The standard sop form of the expression $\bar{A}\bar{B} + \bar{A}\bar{C}$ is _____.

- a) $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$
- b) $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}B C$
- c) $\bar{A}\bar{B}C + \bar{A}B C + A\bar{B}\bar{C}$
- d) $\bar{A}\bar{B}C + A\bar{B}C + A B\bar{C}$

Answer: option B

Explanation:-

$$A'b + a'c$$

$$= a'b(c+c') + a'c(b+b')$$

$$= a'bc + a'bc' + a'cb + a'cb'$$

$$= a'bc + a'bc' + a'bc + a'b'c \text{ (after aligned in abc sequence)}$$

$$= (a'bc) + a'bc' + (a'bc) + a'b'c$$

$$= a'bc + a'bc' + a'b'c$$

$= a'b'c + a'bc' + a'bc$ [rewritten as per option b]
therefore, the correct answer is $\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}B C$.

5. Identify the boolean expression that is in standard pos form.

- a) $(A + \bar{B})(\bar{A} + B + \bar{C})$
- b) $\bar{A}\bar{B}C + A\bar{B}C$
- c) $(A + \bar{B} + \bar{C})(A + B + C)$
- d) $(a + b)(c + d)$

Answer: option C

6. The boolean expression $C + \bar{C}D$ is equal to _____.

- a) C
- b) D
- c) C+D
- d) 1

Answer: option C

Explanation:-

You can solve by using the distributive law

i.e. $A+b'c=(a+b')(a+c)$

here- $c+c'd$

$$\begin{aligned}&= (c+c')(c+d) \\&= 1.(c+d) \\&= c+d\end{aligned}$$

7. The boolean expression $\bar{A}\bar{B}(A + \bar{B})$ can be reduced to _____.

- a) $\bar{A}\bar{B} + A\bar{B}$
- b) $\bar{A}B$
- c) $A\bar{B} + \bar{A}B$
- d) $A\bar{B}$

Answer: option D

8. Which of the following is true for a 5-variable karnaugh map?

- a) There is no such thing.
- b) It can be used only with the aid of a computer.
- c) It is made up of two 4-variable karnaugh maps.
- d) It is made up of a 2-variable and a 3-variable karnaugh map.

Answer: option C

Explanation:-

Answer is c as it is obtained by 2 two variable karnaugh maps one for 5th variable and another for negated 5th variable.

9. When four 1s are taken as a group on a karnaugh map, the number of variables eliminated from the output expression is _____.

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option B

10. In boolean algebra, the word "literal" means _____.

- a) A product term
- b) All the variables in a boolean expression
- c) The inverse function
- d) A variable or its complement

Answer: option D

6. DESCRIBING LOGIC-CIRCUITS

1. The format used to present the logic output for the various combinations of logic inputs to a gate is called a(n):

- a) Truth table.
- b) Input logic function.
- c) Boolean constant.
- d) Boolean variable.

Answer: option A

2. What is the basic difference between AHDL and VHDL?

- a) Ahdl is used in all pld's.
- b) Vhdl is used in all pld's.
- c) Ahdl is proprietary.
- d) Vhdl is proprietary.

Answer: option C

Explanation:-

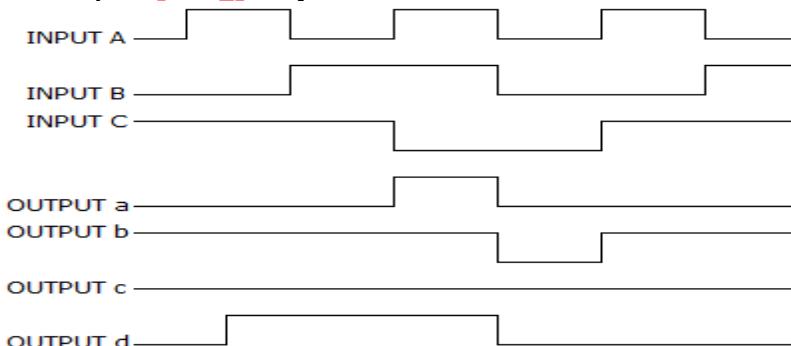
AHDL means analog hardware description languages.

3. A small circle on the output of a logic gate is used to represent the:

- a) Comparator operation.
- b) Or operation.
- c) Not operation.
- d) And operation.

Answer: option C

4. For a three-input OR Gate, with the input waveforms as shown below, which output waveform is correct?

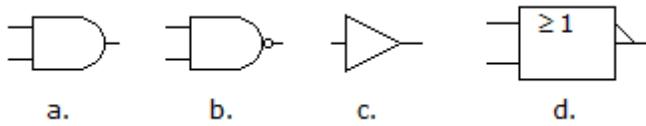


- a) A

- b) B
- c) C
- d) D

Answer: option B

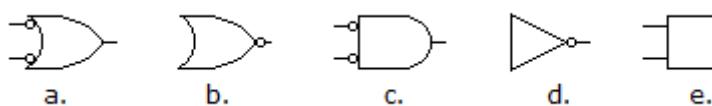
5.Which of the figures given below represents a nOR Gate?



- a) A
- b) B
- c) C
- d) D

Answer: option D

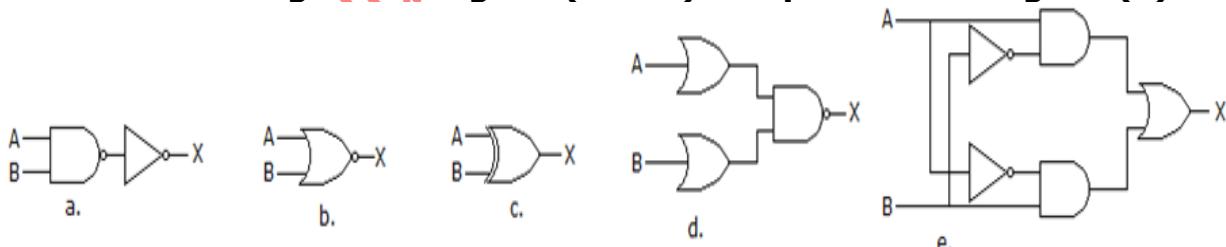
6.Which of the figures (a to d) is the demorgan equivalent of figure (e)?



- a) A
- b) B
- c) C
- d) D

Answer: option A

7.Which of the figures in figure (a to d) is equivalent to figure (e)?



- a) A
- b) B
- c) C
- d) D

Answer: option C

8.In VHDL, the mode of a port does not define:

- a) An input.

- b) An output.
- c) Both an input and an output.
- d) The type of the bit.

Answer: option D

Explanation:-

In VHDL, the port mode gives the direction of the signal and also specifies the direction of signal transfer. There are 4 modes :-

- 1) in
- 2) out
- 3) inout
- 4) buffer

it is defined by :-

port(a,b,cin: in bit; sum: out bit; cout: out bit);
but for defining type of bit (i.e. 1 or 0) we use :-
type bit is ('0','1')

9.Which of the following equations would accurately describe a 4-input OR Gate when a = 1, b = 1, c = 0, and d = 0?

- a) $1 + 1 + 0 + 0 = 1$
- b) $1 + 1 + 0 + 0 = 01$
- c) $1 + 1 + 0 + 0 = 0$
- d) $1 + 1 + 0 + 0 = 00$

Answer: option A

10.Which of the examples below expresses the distributive law?

- a) $(a + b) + c = a + (b + c)$
- b) $A(b + c) = ab + ac$
- c) $A + (b + c) = ab + ac$
- d) $A(bc) = (ab) + c$

Answer: option B

11.Which of the examples below expresses the associative law of addition:

- a) $A + (b + c) = (a + b) + c$
- b) $A + (b + c) = a + (bc)$
- c) $A(bc) = (ab) + c$
- d) $Abc = a + b + c$

Answer: option A

12.How are the statements between begin and end not evaluated in VHDL?

- a) Constantly
- b) Simultaneously

- c) Concurrently
- d) Sequentially

Answer: option D

Explanation:-

In VHDL statements appear outside process will be executed concurrently. But inside process sequential execution. In question no process statement is given between begin and end so it is not evaluated sequentially.

13.Which logic gate does this truth table describe?

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

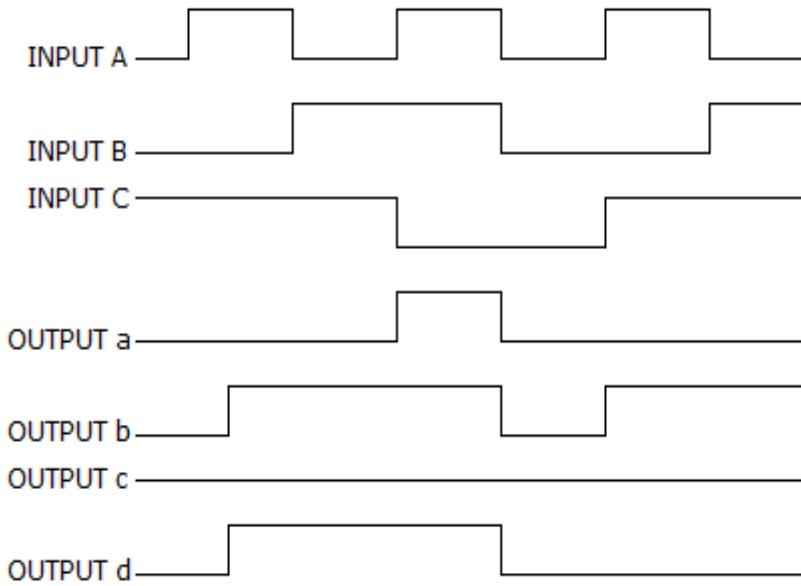
- a) And
- b) Or
- c) Nand
- d) Nor

Answer: option D

Explanation:-

A nOR Gate is simply an inverted OR Gate. Output is high when neither input a nor input b is high.

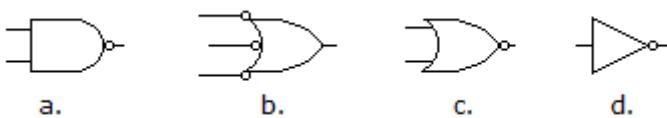
14.For a 3-input nAND Gate, with the input waveforms as shown below, which output waveform is correct?



- a) A
- b) B
- c) C
- d) D

Answer: option C

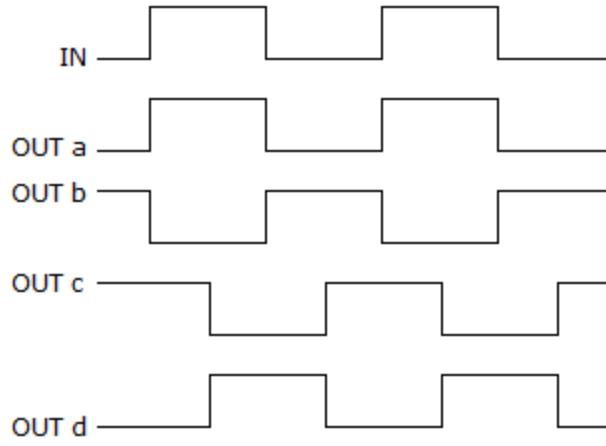
15. Which of the figures given below represents a nAND Gate?



- a) A
- b) B
- c) C
- d) D

Answer: option A

16. Which timing diagram shown below is correct for an inverter?



- a) A
- b) B
- c) C
- d) D

Answer: option B

17. A nOR Gate with one high input and one low input:

- a) Will output a high
- b) Functions as an and
- c) Will not function
- d) Will output a low

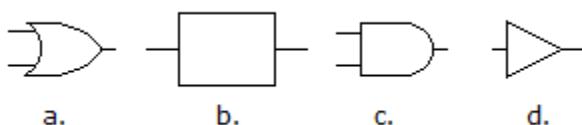
Answer: option D

18. A nAND Gate has:

- a) Active-low inputs and an active-high output.
- b) Active-low inputs and an active-low output.
- c) Active-high inputs and an active-high output.
- d) Active-high inputs and an active-low output.

Answer: option D

19. Which of the figures given below represents an OR Gate?



- a) A
- b) B
- c) C
- d) D

Answer: option A

20. Which of the following is a form of demorgan's theorem?

- a) $\overline{X+Y} = \bar{X} + \bar{Y}$
- b) $X(1) = X$
- c) $\overline{XY} = \bar{X} + \bar{Y}$
- d) $X + 0 = X$

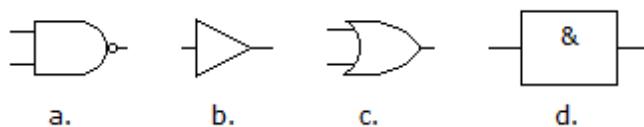
Answer: option C

21. The logic gate that will have high or "1" at its output when any one of its inputs is high is a(n):

- a) NOR Gate
- b) OR Gate
- c) AND Gate
- d) Not operation

Answer: option B

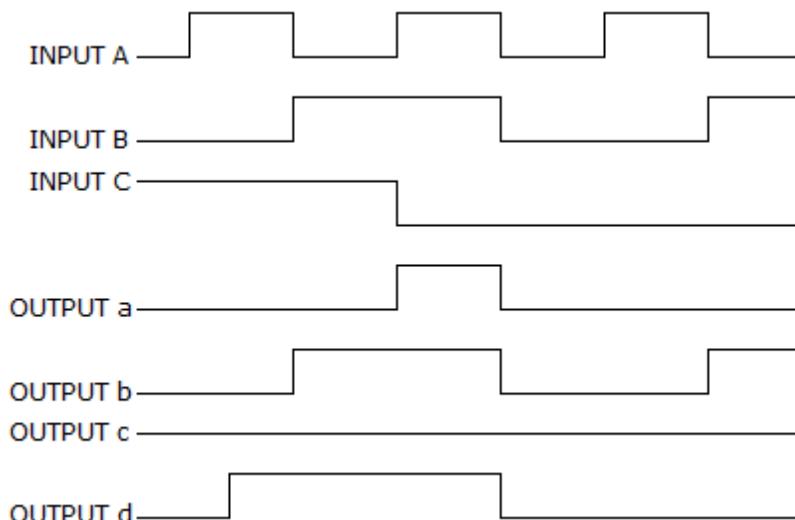
22. Which of the symbols shown below represents an AND Gate?



- a) A
- b) B
- c) C
- d) D

Answer: option D

23. For a three-input AND Gate, with the input waveforms as shown below, which output waveform is correct?



- a) A
- b) B
- c) C
- d) D

Answer: option C

24.An OR Gate with inverted inputs functions as:

- a) An AND Gate.
- b) A nAND Gate.
- c) A nOR Gate.
- d) An inverter.

Answer: option B

Explanation:-

For example

$$a=1, a'=0$$

$$b=1, b'=0$$

or

$$a'+b'=0$$

nand

$$\{ab\}'=a'+b'$$

25.An OR Gate with inverted inputs functions as:

- 1. An AND Gate.
- 2. A NAND Gate.
- 3. A NOR Gate.
- 4. An Inverter.

Answer: option B

Explanation:-

For example

$$a=1, a'=0$$

$$b=1, b'=0$$

or

$$a'+b'=0$$

nand

$$\{ab\}'=a'+b'$$

26.The special software application that translates from HDL into a grid of 1's and 0's, which can be loaded into a pld, is called a:

- a) Formatter.
- b) Compiler.
- c) Programmable wiring.
- d) Cpu.

Answer: option B

27.The boolean equation for a nor function is:

- a) $X = A + \bar{B}$

b) $X = \overline{A + B}$

c) $X = \overline{A} + B$

d) $X = A + B$

Answer: option B

28. Which step in this reduction process is using demorgan's theorem?

$$X = \overline{A * B} (\overline{B} + C)$$

STEP 1 $X = (\overline{A} + \overline{B})(\overline{B} \overline{C})$

STEP 2 $X = \overline{A} \overline{B} \overline{C} + \overline{B} \overline{B} \overline{C}$

STEP 3 $X = \overline{B} \overline{C}(\overline{A} + 1)$

STEP 4 $X = \overline{B} \overline{C}$

a) Step 1

b) Step 2

c) Step 3

d) Step 4

Answer: option A

29. Simplify the expression $\overline{(AB) + C}$ using demorgan's theorems.

a) $\overline{\overline{AB}} + C$

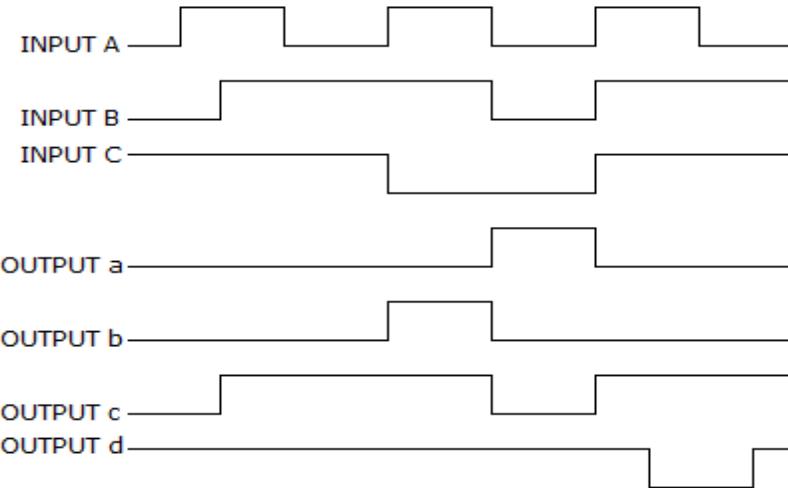
b) \overline{ABC}

c) $\overline{AB} + \overline{C}$

d) $(A + B)C$

Answer: option B

30. For a three-input nOR Gate, with the input waveforms as shown below, which output waveform is correct?



- a) A
- b) B
- c) C
- d) D

Answer: option A

True/false

1.A low placed on the input of an inverter will produce a high output.

- A)True
- B)False

Answer: option A

2.The subdesign section defines the input and output of the logic circuit block.

- A)True
- B)False

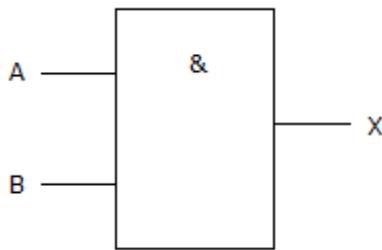
Answer: option A

3.The nAND Gate is an example of combinational logic.

- A)True
- B)False

Answer: option A

4.The symbol shown below is an AND Gate.



- A)True
B)False**

Answer: option A

5.The complement of 1 is 0.

- A)True
B)False**

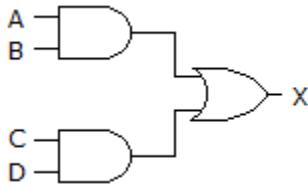
Answer: option A

6.In VHDL, local signals are declared in the variable section, which is placed between the subdesign section and the logic section.

- A)True
B)False**

Answer: option B

7.The given figure shows the correct logic implementation of the distributive law.



- A)True
B)False**

Answer: option A

8.Boolean algebra was first applied to the analysis of digital circuits by claude shannon at stanford university.

- A)True
B)False**

Answer: option B

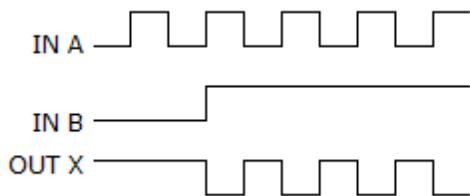
9.The application of demorgan's theorems to a boolean expression with double and single inversions produces a resultant expression that contains only single inverter signs over single variables.

- A)True**

B)False

Answer: option A

**10.The timing diagram for a two-input nAND Gate is shown below.
The gate is working correctly.**



A)True

B)False

Answer: option A

11.The truth table shown below describes the operation of a nOR Gate.

INPUTS		OUTPUT
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

A)True

B)False

Answer: option B

12.A two-input nAND Gate has inputs of 1 and 0; the output is 0.

A)True

B)False

Answer: option B

13.A nAND Gate consists of an AND Gate and an OR Gate connected in series with each other.

A)True

B)False

Answer: option B

14.A nAND Gate consists of AND Gate with an NOT Gate in series..

In an expression containing both and and or operations, the and operations are performed first (unless parentheses indicate otherwise).

- A)True
- B)False

Answer: option A

15.In a text-based language, the circuit being described must be given a name.

- A)True
- B)False

Answer: option A

16.The effect of an inverted output being connected to the inverting input of another gate is to effectively eliminate one of the inversions, resulting in a single inversion.

- A)True
- B)False

Answer: option B

17.A minimum of three universal nOR Gates would be required to perform the logical operation of a 2-input AND Gate.

- A)True
- B)False

Answer: option A

18.The boolean expression for a three-input AND Gate is $x = abc$.

- A)True
- B)False

Answer: option A

19.Output logic levels for certain input conditions of a logic circuit may often be determined without using the boolean expression.

- A)True
- B)False

Answer: option A

20.The comments in adhl are enclosed between # characters.

- A)True
- B)False

Answer: option B

21.The expressions, \overline{AB} and $\overline{A} + \overline{B}$, are equivalent.

- A)True

B)False

Answer: option A

22.The output of a nAND Gate is the inverse of the output for an AND Gate for all possible input combinations.

A)True

B)False

Answer: option A

23.NOR Gates can be used to construct AND Gates.

A)True

B)False

Answer: option A

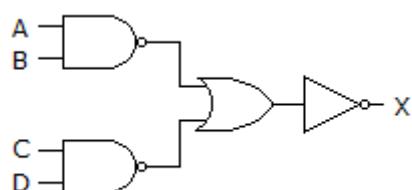
24.The commutative law of boolean addition states that $a + b = a \cdot b$.

A)True

B)False

Answer: option B

25.The figure given below is an example of the implementation of and-or-invert logic.



A)True

B)False

Answer: option B

26.The OR Gate performs like two switches wired in a series.

A)True

B)False

Answer: option B

27.The inputs to an AND Gate are: a = 1, b = 0, c = 1. The output will be low.

A)True

B)False

Answer: option A

28.In boolean algebra, $1 \cdot 0 = 0$.

A)True

B)False

Answer: option A

30.Boolean multiplication is symbolized by a + b.

A)True

B)False

Answer: option B

31.VHDL is not a new language.

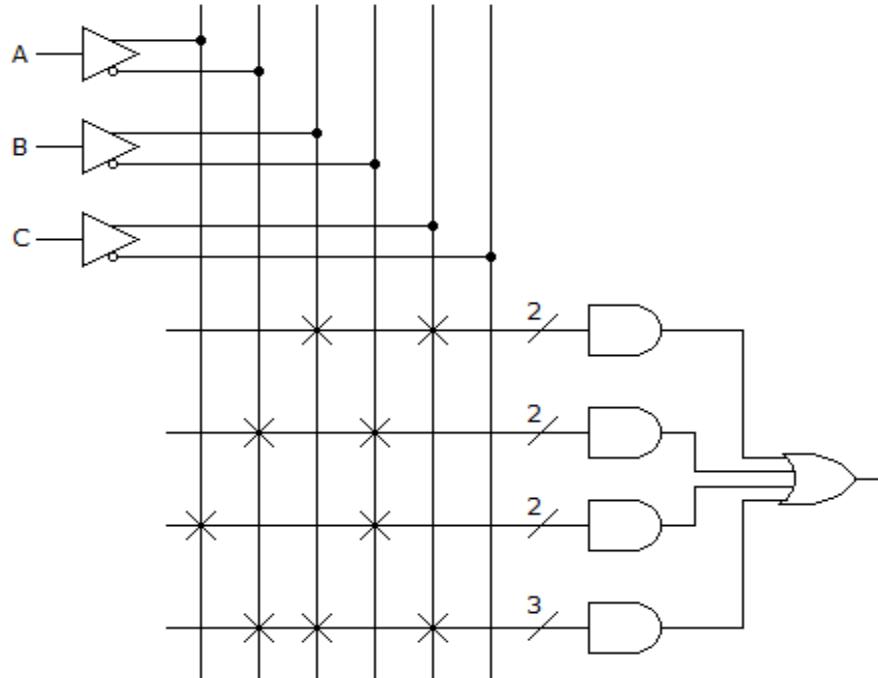
A)True

B)False

Answer: option A

7. COMBINATIONAL LOGIC ANALYSIS

1. Referring to the GAL diagram, which is the correct logic function?



- a) $X = BC + \bar{A}\bar{B} + A\bar{B} + \bar{A}BC$
b) $X = B\bar{C} + \bar{A}\bar{B} + A\bar{B} + ABC$
c) $X = BC + \bar{A}\bar{B} + \bar{A}B + \bar{A}BC$
d) $X = BC + \bar{A}\bar{B} + A\bar{B} + \bar{A}\bar{B}C$

Answer: option A

Explanation:-

Here the 'x' mark represents that the corresponding input is connected to the corresponding AND Gate... Here, the numbers(2/3) before the AND Gates denotes the number of inputs to the AND Gate.

Note:-

The GAL is a re-programmable logic device unlike PAL. GAL uses EECMOS technology instead of BJT. GAL also has programmable output configurations.

2. The output of an exclusive-nOR Gate is 1. Which input combination is correct?

- a) $A = 1, b = 0$
b) $A = 0, b = 1$
c) $A = 0, b = 0$

d) None of the above

Answer: option C

3. The boolean sop expression obtained from the truth table below is

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

- a) $A B C + A B C$
- b) $A \bar{B} C + A B \bar{C}$
- c) $\bar{A} \bar{B} C + A B \bar{C}$
- d) None of these

Answer: option C

Explanation:-

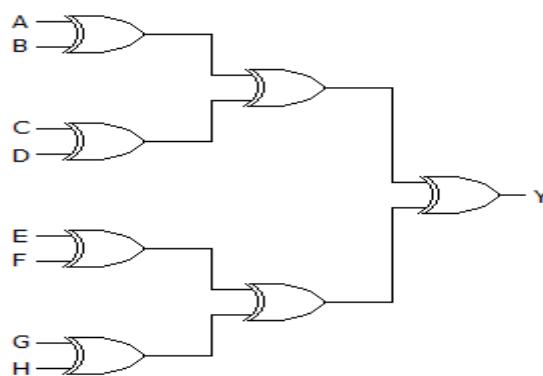
See the output = 1.

0 0 1 = 1 : a b c.

1 1 0 = 1 : a b c.

Answer: c.

4. The 8-input xor circuit shown has an output of $y = 1$. Which input combination below (ordered a - h) is correct?



- a) 10111100
- b) 10111000
- c) 11100111

d) 00011101

Answer: option A

Explanation:-

Option a = 10 11 11 00

a xor b = 1 xor 0 => 1

c xor d = 1 xor 1 => 0

e xor f = 1 xor 1 => 0

g xor h = 0 xor 0 => 0

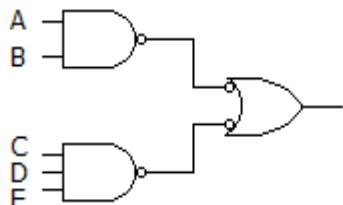
(a xor b) xor (c xor d) = 1 xor 0 => 1(1)

(e xor f) xor (g xor h) = 0 xor 0 => 0(2)

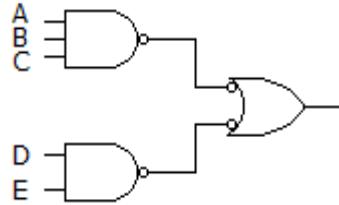
(1) xor (2) = 1 xor 0 => 1.

Hence the option a is correct.

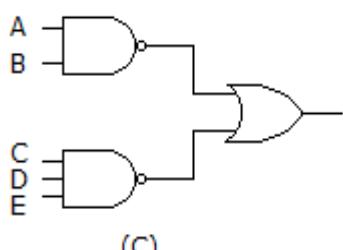
5.Implementing the expression ab + cde using nand logic, we get:



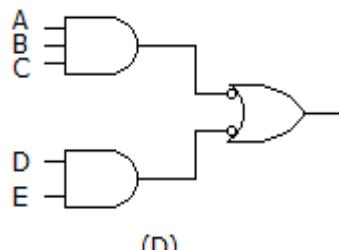
(A)



(B)



(C)



(D)

- a) A
- b) B
- c) C
- d) D

Answer: option A

Explanation:-

Bubble at the end of AND Gate and bubble at the starting of OR Gate will cancel each other so a is correct answer. Because 1st AND Gate will give ab and 2nd AND Gate will give cde and OR Gate taking input 1st input=ab, 2nd input=cde will give the result ab+cde

6. Before an sop implementation, the expression $X = AB(\bar{C}D + EF)$ would require a total of how many gates?

- a) 1
- b) 2
- c) 4
- d) 5

Answer: option D

Explanation:-

$Ab = 1.$

$C' = 1.$

$C'd = 1.$

$Ef = 1.$

$C'd + ef = 1.$

$Ab(c'd+ef) = 5.$

Totally 5 gates are used.

Or

Ab - AND Gate.

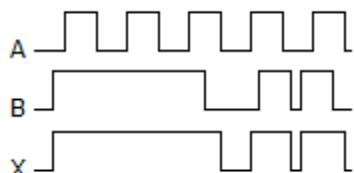
$C'd$ - nAND Gate.

Ef - AND Gate.

$C'd+ef$ - OR Gate.

$Ab(c'd+ef)$ - AND Gate.

7. The following waveform pattern is for a(n) _____.



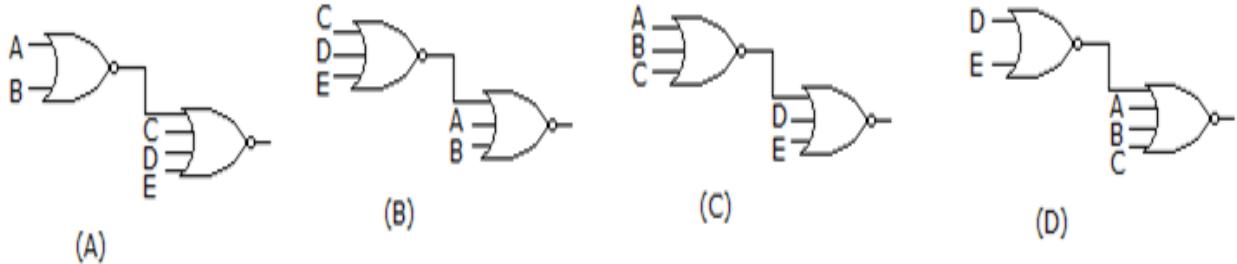
- a) 2-input AND Gate
- b) 2-input OR Gate
- c) Exclusive-OR Gate
- d) None of the above

Answer: option B

Explanation:-

Because in the timing diagram, whenever $a=0$ & $b=0$ then only $x=0$ else output is 1. Thus it follows the truth table of OR Gate.

8. Implementing the expression $X = \overline{\overline{A}\overline{B}} + (\overline{C} + \overline{D} + \overline{E})$ with nor logic, we get:



- a) A
- b) B
- c) C
- d) D

Answer: option A

Explanation:-

$A \text{ nor } b = a'b'$.

$A'b' \text{ nor } c \text{ nor } d \text{ nor } e = (a'b' + (c+d+e))'$.

So answer is a.

9.A 4-variable and-or-invert circuit produces a 0 at its y output.

Which combination of inputs is correct?

- a) $\bar{A}B + \bar{C}D$
- b) $\bar{A}\bar{B} + \bar{C}\bar{D}$
- c) $\bar{A}\bar{B} + CD$
- d) **None of the above**

Answer: option C

Explanation:-

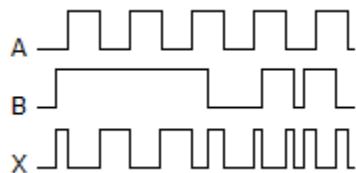
Answer c is correct. Because,

$a'b' + cd = y' = y$.

Take $a=1, b=1, c=1$ and $d=1$.

$A'=0, b'=0$ is connected to AND Gate-1, $c=1, d=1$ is connected to AND Gate-2. I.e $a'b'=0, cd=1$. Outputs of AND Gate are given to OR Gate. I.e $0+1=1$. Output is connected to inverter. Hence the output $y=0$.

10.The following waveform pattern is for a(n) _____.



- a) 2-input AND Gate
- b) 2-input OR Gate
- c) Exclusive-OR Gate

d) None of the above

Answer: option C

Explanation:-

Truth table

x	y	z
0	0	0
0	1	1
1	0	1
1	1	0

11. To implement the expression $\bar{A}\bar{B}CD + A\bar{B}\bar{C}D + AB\bar{C}\bar{D}$, it takes one OR Gate and _____.

- a) Three AND Gates and three inverters**
- b) Three AND Gates and four inverters**
- c) Three AND Gates**
- d) One AND Gate**

Answer: option A

Explanation:-

The expression is $ab'cd + abc'd + abcd'$.

AND Gate-i is for the expression $ab'cd$; inverter-1 is connected to i/p b.

AND Gate-ii is for the expression $abc'd$; inverter-2 is connected to i/p c.

AND Gate-iii is for the expression $abcd'$; inverter-3 is connected to i/p d.

For adding all these 3 expressions ,v need one OR Gate.

So totally the expression needs 3 AND Gate, 3 inverters, 1 OR Gate.

12. One positive pulse with $t_w = 75 \mu s$ is applied to one of the inputs of an exclusive-or circuit. A second positive pulse with $t_w = 15 \mu s$ is applied to the other input beginning 20 μs after the leading edge of the first pulse. Which statement describes the output in relation to the inputs?

- a) The exclusive-or output is a 20 μs pulse followed by a 40 μs pulse, with a separation of 15 μs between the pulses.**
- b) The exclusive-or output is a 20 μs pulse followed by a 15 μs pulse, with a separation of 40 μs between the pulses.**
- c) The exclusive-or output is a 15 μs pulse followed by a 40 μs pulse.**
- d) The exclusive-or output is a 20 μs pulse followed by a 15 μs pulse, followed by a 40 μs pulse.**

Answer: option D

Explanation:-

When both the input pulses are high or low x-or output is low.but when one of the input is high and another is low or vice-verse output is high. In this problem for the first 20us one input is high and another is low, so obviously output is a high. For next 15us both the input is high so output is low and for remaining 40us(75-20-15) first input is still high and second one is low so output is high.

13.How many AND Gates are required to implement the boolean expression, $X = AB\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option C

14.How many NOT Gates are required to implement the boolean expression, $X = A\bar{B}C + \bar{A}BC$?

- a) 1
- b) 2
- c) 4
- d) 5

Answer: option B

15.The inverter can be produced with how many nAND Gates?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option A

Explanation:-

The inverter can be produced with single (1) nAND Gate, because we can tie (combine) both the inputs of the nAND Gate together and make it single. It works as a inverter.

16.A 4-variable and-or circuit produces a 0 at its y output. Which combination of inputs is correct?

- a) A = 0, b = 0, c = 1, d = 1
- b) A = 1, b = 1, c = 0, d = 0
- c) A = 1, b = 1, c = 1, d = 1
- d) A = 1, b = 0, c = 1, d = 0

Answer: option D

Explanation:-

A and with b.

C and with d.

Output of first AND Gate ab is or with output of second AND Gate is cd.

So, output of OR Gate is,

$$y = ab + cd$$

So, a=1, b=0, c=1, d=0.

$$ab = 0, cd = 0$$

So output y=0.

Option d is the write answer.

17. A 4-variable and-or circuit produces a 1 at its y output. Which combination of inputs is correct?

- a) A = 0, b = 0, c = 0, d = 0
- b) A = 0, b = 1, c = 1, d = 0
- c) A = 1, b = 1, c = 0, d = 0
- d) A = 1, b = 0, c = 0, d = 0

Answer: option C

Explanation:-

Option c is right answer.

Same as q 16 only the difference is output is high.

A and with b & c and with d.

First AND Gate output is ab & second AND Gate output is cd.

Ab or with cd so,

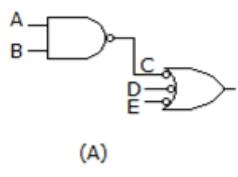
$$y = ab + cd$$

A=1, b=1, c=0, d=0,
output will be high only.

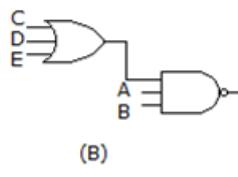
Or

Use two and for 4 inputs, and then simply use OR Gate. Answer will be 1
(a=1, b=1, c=0, & d=0) one AND Gate will send 1 and the other will send 0.
ThAn OR Gate will operate.

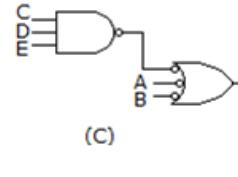
18. Implementing the expression $\overline{(\bar{A} + \bar{B})CDE}$ using nand logic, we get:



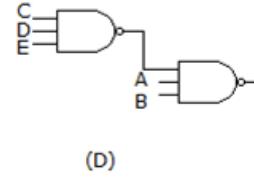
(A)



(B)



(C)



(D)

- a) A
- b) B
- c) C
- d) D

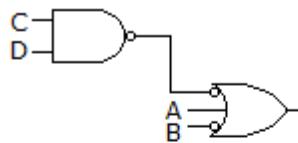
Answer: option D

Explanation:-

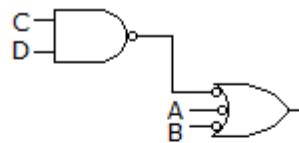
swer is a.

$$((ab)')' + c' + d' + e' = ((ab)'cde)' = ((a' + b')cde)'$$

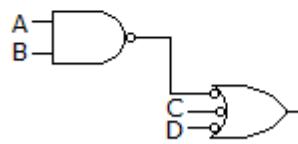
19. Implementing the expression $\bar{A} + \bar{B} + CD$ using nand logic, we get:



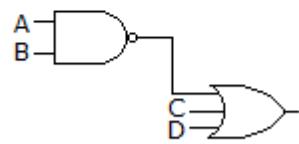
(A)



(B)



(C)



(D)

- a) A
- b) B
- c) C
- d) D

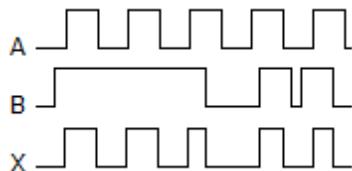
Answer: option B

Explanation:-

In option b c nand d = cd'.

Before or it is inverted so input to OR Gate is cd and a' and b'. So that's why o/p= $(a' + b' + cd)$.

20. The following waveform pattern is for a(n) _____.



- a) 2-input AND Gate
- b) 2-input OR Gate
- c) Exclusive-OR Gate
- d) None of the above

Answer: option A

Explanation:-

B waveform is one on(1).

A waveform is three on(3).

$3 \times 1 = 3$ using AND Gate.

The output waveform x is a multiplication of a and b.

21. Implementation of the boolean expression $X = ABC + AB + A\bar{C}$ results in _____.

- a) Three AND Gates, one OR Gate
- b) Three AND Gates, one NOT Gate, one OR Gate
- c) Three AND Gates, one NOT Gate, three OR Gates
- d) Three AND Gates, three OR Gates

Answer: option B

Explanation:-

One AND Gate for ab, one AND Gate to combine ab & c, one NOT Gate for c' , then one AND Gate for ac' , and then OR Gate for abc & ab , another OR Gate to combine ac' . So there is need of 2 OR Gate.

22. One possible output expression for an and-or-invert circuit having one AND Gate with inputs a, b, and c and one AND Gate with inputs d and e is _____

- a) $ABC + DE$
- b) $\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E}$
- c) $(\bar{A} + \bar{B} + \bar{C})(\bar{D} + \bar{E})$
- d) $(A + B + C)(D + E)$

Answer: option C

Explanation:-

According to de morgan's theorem states that: $(ab)' = a' + b'$ and $(a+b)' = a'b'$.

So therefore $(abc)' = a' + b' + c'$ and $(de)' = d' + e'$. So option c is correct.

23. How many 2-input nOR Gates does it take to produce a 2-input nAND Gate?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option D

Explanation:-

Because, let a is given to first nOR Gate then output is $a\bar{b}$.

Same as for b, the output is $b\bar{a}$.

When both output is apply on another nor-gate the output is.

Bar of (a-bar + b-bar) is equals to a.b by de-morgan's law.

24.A logic circuit with an output $X = \bar{A}\bar{B}C + \bar{A}B\bar{C}$ consists of _____.

- a) Two AND Gates, two OR Gates, two inverters
- b) Three AND Gates, two OR Gates, one inverter
- c) Two AND Gates, one OR Gate, two inverters
- d) Two AND Gates, one OR Gate

Answer: option C

Explanation:-

For a bar one inverter with b and c to give one AND Gate and for b bar one inverter with a to give ab bar for second AND Gate together to add one OR Gate. So option c is correct.

TRUE/FALSE

1.The output of a nAND Gate is low when all inputs are high at the same time.

- A)True
- B)False

Answer: option A

2.When the output of an and-or circuit is complemented, it results in an

- A)True
- B)False

Answer: option A

Explanation:-

And-or-invert circuit.

3.If one input to a 2-input AND Gate is high, the output reflects the other input.

- A)True
- B)False

Answer: option A

4.A nAND Gate can function as a negative-OR Gate.

- A)True
- B)False

Answer: option A

Explanation:-

NAND Gate can function as a negative-AND Gate.

5.An AND Gate is a universal gate.

- A)True
- B)False

Answer: option B

Explanation:-

And, or, not are basic gates.
Nand &nor are universal gate.

6.A nOR Gate is a universal gate.

- A)True
- B)False

Answer: option A

Explanation:-

Nand and nor are the universal gates

7.An exclusive-OR Gate's output is high when its inputs are equal.

- A)True
- B)False

Answer: option B

Explanation:-

If both the inputs are high the output is low, if both the inputs are low the output is high.

8.A VHDL component is a predefined logic function.

- A)True
- B)False

Answer: option B

9.The output of an AND Gate is high when any input is high.

- A)True
- B)False

Answer: option B

10.A nOR Gate's truth table is the opposite of that of an OR Gate.

- A)True
- B)False

Answer: option A

FILL UP THE BLANKS

1. Assume you have a, b, c, and d available but not their complements. The minimum number of 2-input nAND Gates required to implement the equation $X = \bar{A}\bar{B} + \bar{B}\bar{C}$ is _____.

- a) 3
- b) 4
- c) 5
- d) 6

Answer: option C

2. The symbol shown represents a(n) _____.



- a) AND Gate
- b) OR Gate
- c) NAND Gate
- d) NOR Gate

Answer: option D

3. A gate can drive a number of load gate inputs up to its specified _____.

- a) Supply voltage
- b) Noise margin
- c) Fan-in
- d) Fan-out

Answer: option D

4. The expression $\overline{AB} + \overline{CD}$ can be directly implemented using only _____.

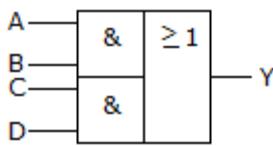
- a) An XOR Gate
- b) An XNOR Gate
- c) An AOI circuit
- d) Three 2-input nAND Gates

Answer: option C

Explanation:-

AOI means and-or-invert circuit. this circuit is implemented in the CMOS logic family. AOI perform one or more and operation followed by an or operation and inversion.

5. The symbol shown represents _____.



- a) And-or logic
- b) AOI logic
- c) XOR Gate
- d) XnOR Gate

Answer: option A

Explanation:-

$$Y = a \& b + c \& d$$

1st half block \rightarrow and logic.

2nd half block \rightarrow summation of ab and cd will be "1" when either both are "1" or anyone of ab or cd is "1"

$\rightarrow >=1$ represent or logic.

6.If both inputs of a 2-input nOR Gate are connected, the gate will function as an _____.

- a) OR Gate
- b) AND Gate
- c) Inverter
- d) Any of the above

Answer: option C

7.Assume that you have a 3-input nAND Gate but need only a 2-input gate. The unused input should be _____.

- a) Connected to ground
- b) Left open
- c) Connected to a high
- d) Any of the above

Answer: option C

8.A node is defined as _____.

- a) A common point in a circuit
- b) A circuit implemented as a sum-of-products
- c) The output signals from a circuit
- d) A shorted input

Answer: option A

9.Using the universal property of a nAND Gate, one or more nAND Gates can be used to replace an _____.

- a) OR Gate

- b) AND Gate**
- c) Inverter**
- d) Any of the above**

Answer: option D

10. The expression $\bar{A}\bar{B} + \bar{A}B$ can be directly implemented using only _____.

- a) An xOR Gate**
- b) An xnOR Gate**
- c) An AOI logic**
- d) Three 2-input nAND Gates**

Answer: option A

8. COMBINATIONAL LOGIC CIRCUITS

1. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

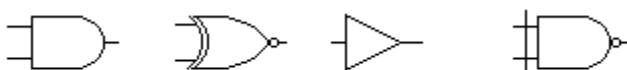
- a) 1
- b) 2
- c) 4
- d) 8

Answer: option C

Explanation:-

Required outputs/given outputs == $(32/8) = 4$.

2. Which of the figures shown below represents the exclusive-nOR Gate?



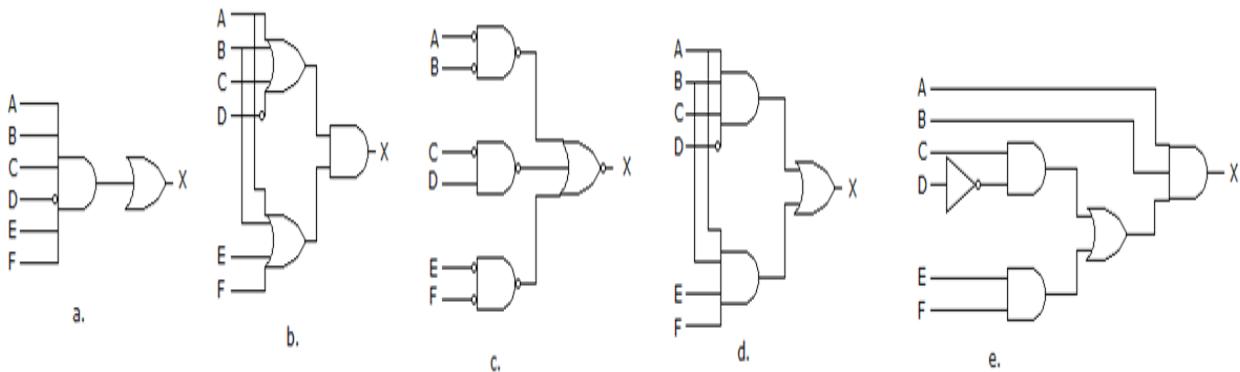
- a) A
- b) B
- c) C
- d) D

Answer: option B

Explanation:-

Ex-nOR Gate means negation of ex-OR Gate. Means bubble to the ex-OR Gate.

3. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



- a) A
- b) B
- c) C
- d) D

Answer: option D

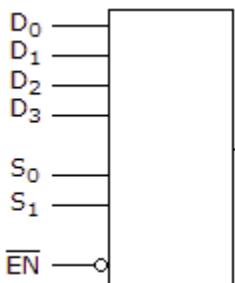
Explanation:-

a.b.c. \wedge d + a.b.e.f is the sum of product

Or

Since we get output of e ckt as $(c^*\wedge d + e^*f)*a.b$ multiply we get $abc^*d + abef$ which sum of product form.

4. For the device shown here, let all d inputs be low, both s inputs be high, and the \overline{EN} input be low. What is the status of the y output?



- a) Low
- b) High
- c) Don't care
- d) Cannot be determined

Answer: option A

Explanation:-

$d_0 = d_1 = d_2 = d_3 = 0$;

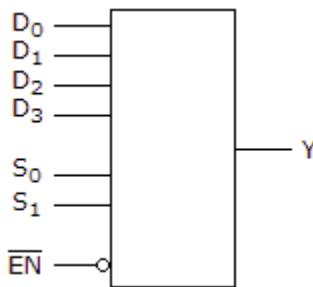
$s_0 = s_1 = 1$.

For producing output $en = 0$;

when $s_1 = s_2 = 1$.

Then d₃ is selected.
Hence, $y = d_3s_1s_2 = 0$;

5. For the device shown here, let all d inputs be low, both s inputs be high, and the \overline{EN} input be high. What is the status of the y output?



- a) Low
- b) high
- c) Don't care
- d) Cannot be determined

Answer: option A

Explanation:-

Enable input is used only for on the device. The o/p is depends on en and also data lines. When en is high the o/p depends upon data lines where as en low o/p is depends on en input, whatever it may be data lines low or high.

Or

The device is "not enable". Not enable = 0, 0=low. The answer is low.

Or

An enable input makes the multiplexer operate. When en = 0, the output is 0. When en = 1, the multiplexer performs its operation depending on the selection line. In this case it is en not.

6. Convert BCD 0001 0010 0110 to binary.

- a) 1111110
- b) 1111101
- c) 1111000
- d) 1111111

Answer: option A

Explanation:-

0001 = 1

0010 = 2

0110 = 6

then 0001 0010 0110 = 126

126 / 2 = 63 ...0

$63 / 2 = 31 \dots 1$
 $31 / 2 = 15 \dots 1$
 $15 / 2 = 7 \dots 1$
 $7 / 2 = 3 \dots 1$
 $3 / 2 = 1 \dots 1$
 $1 / 2 = 0 \dots 1$
126 = 1111110

7.A 74hc147 priority encoder has ten active-low inputs and four active-low outputs. What would be the state of the four outputs if inputs 4 and 5 are low and all other inputs are high?

- a) $\overline{A_0} = 0, \overline{A_1} = 1, \overline{A_2} = 0, \overline{A_3} = 1$
- b) $\overline{A_0} = 1, \overline{A_1} = 1, \overline{A_2} = 0, \overline{A_3} = 1$
- c) $\overline{A_0} = 1, \overline{A_1} = 0, \overline{A_2} = 1, \overline{A_3} = 0$
- d) $\overline{A_0} = 0, \overline{A_1} = 0, \overline{A_2} = 1, \overline{A_3} = 1$

Answer: option A

Explanation:-

As two inputs are low, i4 is given priority(5th i/p), so respective o/p 0101 represents 5. So, it is the correct answer.

8.Convert BCD 0001 0111 to binary.

- a) 10101
- b) 10010
- c) 10001
- d) 11000

Answer: option C

Explanation:-

0001 - 1.
0010 - 2.
0011 - 3.
0100 - 4.
0101 - 5.
0110 - 6.
0111 - 7.
0001 0111 = (17)₁₀.

2|17

-

2| 8 - 1

-

2| 4 - 0

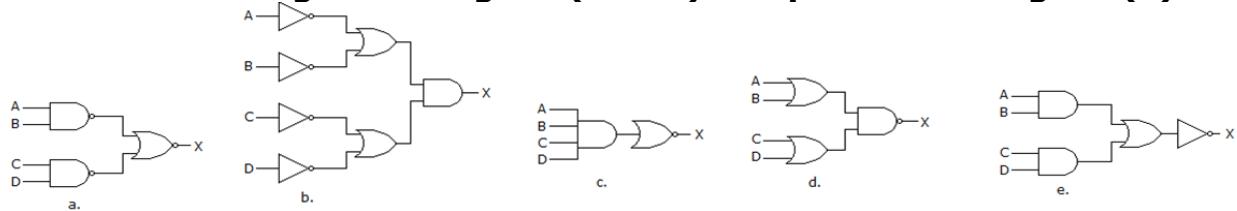
-

2| 2 - 0

-
10.

So we count start from below 10001(answer).

9.Which of the figures in figure (a to d) is equivalent to figure (e)?



- a) A
- b) B
- c) C
- d) D

Answer: option B

Explanation:-

By calculating option e output is bar of $(ab+cd)$ or $(\bar{a}\bar{b} \cdot \bar{c}\bar{d})$, which equivalent is option b o/p.

Or

Can solve using de morgan's theorem which is,
nor = inverter followed by an and.

10.How many data select lines are required for selecting eight inputs?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option C

Explanation:-

Because input combinations are 8 which is corresponding to 3 variables.hence 3 select lines are required

11.The simplest equation which implements the k-map shown below is:

	\bar{C}	C
$\bar{A} \bar{B}$	0	0
$\bar{A} B$	1	1
A \bar{B}	1	1
A B	0	1

- a) $X = AC + B$
- b) $X = A\bar{B}$
- c) $ABC + A\bar{B}C + A\bar{B}C$
- d) $AB + A\bar{B}$

Answer: option A

Explanation:-

By K-MAP:-Using k map the upper four 1's make a quad which gives expression b and the remaining 1 make doublet with its upper 1 which gives expression ac. We are solving this kmap by assuming sop form. So output will be sum of both expression i.e. B+ac.

By Boolean Algebra:-

$$(\bar{a} \bar{b} \bar{c}) + (\bar{a} \bar{b} c) + (a \bar{b} \bar{c}) + (a \bar{b} c) + (a b \bar{c}).$$

$$(\bar{a} \bar{b} b(c + c\bar{b})) + a \bar{b} (c\bar{b} + c) + (a b \bar{c}).$$

$$(\bar{a} \bar{b} b) + (a \bar{b}) + (a b \bar{c}).$$

$$B(\bar{a} \bar{b} + a) + (a b \bar{c}).$$

$$B + (a b \bar{c}).$$

$$Ac(b + b\bar{b}).$$

$$\text{Ans} = ac.$$

12. How many 1-of-16 decoders are required for decoding a 7-bit binary number?

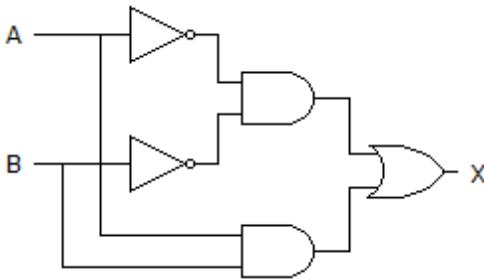
- a) 5
- b) 6
- c) 7
- d) 8

Answer: option D

Explanation:-

7 bit means 2^7 combinations i.e 128. So to decode 128 combinations we require $128/16=8$ 1 of 16 decoders.

13. Which of the following logic expressions represents the logic diagram shown?



- a) $X = A \bar{B} + \bar{A} B$
- b) $X = \bar{A} \bar{B} + A B$
- c) $X = \bar{A} \bar{B} + \bar{A} \bar{B}$
- d) $X = \bar{A} \bar{B} + A B$

Answer: option D

Explanation:-

1st AND Gate o/p is - $a' \cdot b'$

2nd AND Gate o/p is - $a \cdot b$

OR Gate o/p is - $(a' \cdot b') + (ab) = ab + a' \cdot b'$

14. The implementation of simplified sum-of-products expressions may be easily implemented into actual logic circuits using all universal _____ gates with little or no increase in circuit complexity. (select the response for the blank space that will best make the statement true.)

- a) AND/OR
- b) NAND
- c) NOR
- d) OR/AND

Answer: option B

Explanation:-

Sop is better to design with nand, for pos we use nor Gate.

Both nand and nor are universal, nand for sop requires less circuitry as compare to nor with sop. Similarly pos with nor require less circuitry.

15. Which of the following statements accurately represents the two best methods of logic circuit simplification?

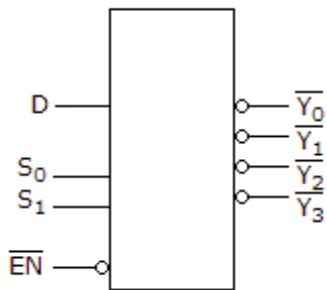
- a) Boolean algebra and karnaugh mapping
- b) Karnaugh mapping and circuit waveform analysis
- c) Actual circuit trial and error evaluation and waveform analysis
- d) Boolean algebra and actual circuit trial and error evaluation

Answer: option A

Explanation:-

Logic circuit can be simplified by only boolean algebra up to 3 variable and by karnaugh map up to 5 variables.

16. For the device shown here, assume the d input is low, both s inputs are high, and the \overline{EN} input is high. What is the status of the \overline{Y} outputs?



- a) All are high.
- b) All are low.
- c) All but $\overline{Y_0}$ are low.
- d) All but $\overline{Y_0}$ are high.

Answer: option A

Explanation:-

For a given mux, en i/p is active low i.e, mux is active if and only if en=0, but they given en=1, so mux is in disable condition.

The resultant o/p is all zeros. But o/p is inverted, so o/p is all ones.

17. Which of the following combinations cannot be combined into k-map groups?

- a) Corners in the same row
- b) Corners in the same column
- c) Diagonal corners
- d) Overlapping combinations

Answer: option C

18. As a technician you are confronted with a TTL circuit board containing dozens of ic chips. You have taken several readings at numerous ic chips, but the readings are inconclusive because of their erratic nature. Of the possible faults listed, select the one that most probably is causing the problem.

- a) A defective ic chip that is drawing excessive current from the power supply
- b) A solar bridge between the inputs on the first ic chip on the board
- c) An open input on the first ic chip on the board

d) A defective output ic chip that has an internal open to V_{CC}

Answer: option C

Explanation:-

Because all are giving strange readings, the error is in 1st chip.

19.Which gate is best used as a basic comparator?

- a) NOR
- b) OR
- c) EXOR
- d) AND

Answer: option C

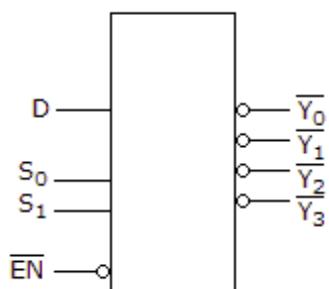
Explanation:-

Truth table

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

when both the input are same then the output is low & when the two inputs are differ then the output is high that mens the ex-OR Gate compair both the inputs & then gives the output.

20.The device shown here is most likely a _____.



- a) Comparator
- b) Multiplexer
- c) Demultiplexer
- d) Parity generator

Answer: option C

Explanation:-

The given dig. Is shown demultiplexer bcoz it takes single input & gives many outputs. This is a 1:4 demux.. With two select lines..

21.In VHDL, macrofunctions is/are:

- a) Digital circuits.
- b) Analog circuits.
- c) A set of bit vectors.
- d) Preprogrammed TTL devices.

Answer: option D

22.Which of the following expressions is in the product-of-sums form?

- a) $(a + b)(c + d)$
- b) $(ab)(cd)$
- c) $Ab(cd)$
- d) $Ab + cd$

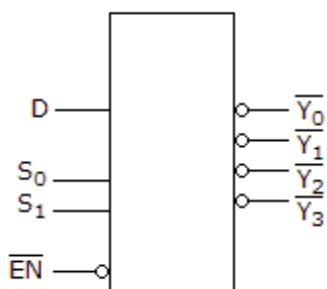
Answer: option A

23.Which of the following is an important feature of the sum-of-products form of expressions?

- a) All logic circuits are reduced to nothing more than simple and and or operations.
- b) The delay times are greatly reduced over other forms.
- c) No signal must pass through more than two gates, not including inverters.
- d) The maximum number of gates that any signal must pass through is reduced by a factor of two.

Answer: option A

24.For the device shown here, assume the D input is low, both S inputs are low, and the \overline{EN} input is low. What is the status of the \overline{Y} outputs?



- a) All are high.
- b) All are low.
- c) All but $\overline{Y_0}$ are low.
- d) All but $\overline{Y_0}$ are high.

Answer: option D

Explanation:-

We know s0 and s1 are selection bits;

s0 & s1 both are low so o/p y0 is activate. But i/p d is low.

So o/p y0 is low but y0 is inverted so y0 is high and other o/p is low.

25.An output gate is connected to four input gates; the circuit does not function. Preliminary tests with the dmm indicate that the power is applied; scope tests show that the primary input gate has a pulsing signal, while the interconnecting node has no signal. The four load gates are all on different ics. Which instrument will best help isolate the problem?

- a) Current tracer
- b) Logic probe
- c) Oscilloscope
- d) Logic analyzer

Answer: option A

26.The binary numbers a = 1100 and b = 1001 are applied to the inputs of a comparator. What are the output levels?

- a) A > b = 1, a < b = 0, a = b = 1
- b) A > b = 0, a < b = 1, a = b = 0
- c) A > b = 1, a < b = 0, a = b = 0
- d) A > b = 0, a < b = 1, a = b = 1

Answer: option C

Explanation:-

A = 1100,(12).

B = 1001,(9).

1 is represent true.

0 is represent false.

So,

a>b=1, a<b=0, a=b=0;

true, false, false.

27.A logic probe is placed on the output of a gate and the display indicator is dim. A pulser is used on each of the input terminals, but the output indication does not change. What is wrong?

- a) The output of the gate appears to be open.
- b) The dim indication on the logic probe indicates that the supply voltage is probably low.
- c) The dim indication is a result of a bad ground connection on the logic probe.
- d) The gate may be a tristate device.

Answer: option A

28.Two 4-bit binary numbers (1011 and 1111) are applied to a 4-bit parallel adder. The carry input is 1. What are the values for the sum and carry output?

- a) $\Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 0111$, $C_{out} = 0$
- b) $\Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 1111$, $C_{out} = 1$
- c) $\Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 1011$, $C_{out} = 1$
- d) $\Sigma_4 \Sigma_3 \Sigma_2 \Sigma_1 = 1100$, $C_{out} = 1$

Answer: option C

Explanation:-

-1 <- previous carry

1011

1111

--

1 1011 <- cout is 1 and result is 1011

--

29.Each "1" entry in a k-map square represents:

- a) A high for each input truth table condition that produces a high output.
- b) A high output on the truth table for all low input combinations.
- c) A low output for all possible high input conditions.
- d) A don't care condition for all possible input truth table combinations.

Answer: option A

30.Looping on a k-map always results in the elimination of:

- a) Variables within the loop that appear only in their complemented form.
- b) Variables that remain unchanged within the loop.
- c) Variables within the loop that appear in both complemented and uncomplemented form.
- d) Variables within the loop that appear only in their uncomplemented form.

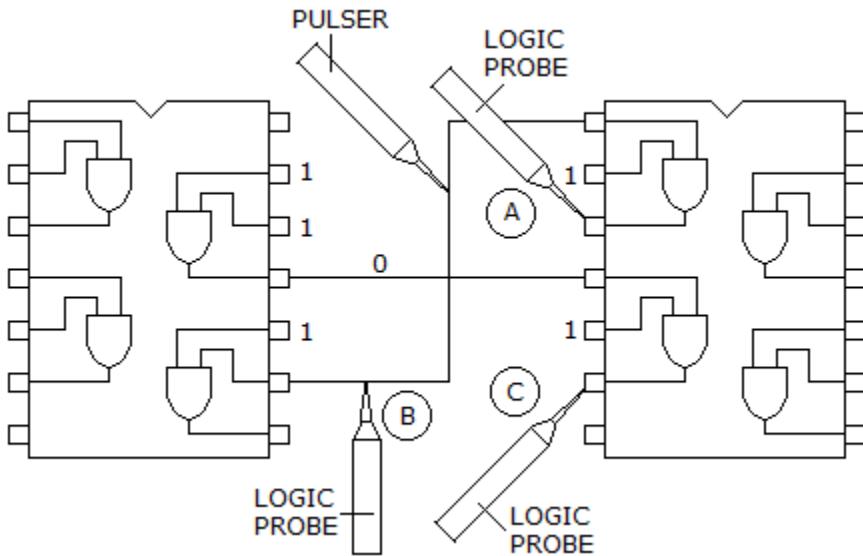
Answer: option C

31.What will a design engineer do after he/she is satisfied that the design will work?

- a) Put it in a flow chart
- b) Program a chip and test it
- c) Give the design to a technician to verify the design
- d) Perform a vector test

Answer: option B

32.Based on the indications of probe a in the figure given below, what is wrong, if anything, with the circuit?



- a) The logic probe is unable to determine the state of the circuit at that point and is blinking to alert the technician to the problem.
- b) The output appears to be shorted to v_{cc} , but is being pulsed by the pulser.
- c) The output appears to be low, but is being pulsed by the pulser.
- d) Nothing appears to be wrong at that point.

Answer: option D

33.What is the indication of a short on the input of a load gate?

- a) Only the output of the defective gate is affected.
- b) There is a signal loss to all gates on the node.
- c) The affected node will be stuck in the low state.
- d) There is a signal loss to all gates on the node, and the affected node will be stuck in the low state.

Answer: option D

35.In HDL, literals is/are:

- a) Digital systems.
- b) Scalars.
- c) Binary coded decimals.
- d) A numbering system.

Answer: option B

36.Which of the following expressions is in the sum-of-products form?

- a) $(a + b)(c + d)$

- b) $(ab)(cd)$
- c) $Ab(cd)$
- d) $Ab + cd$

Answer: option D

37.The carry propagation can be expressed as _____.

- a) $C_p = ab$
- b) $C_p = a+b$
- c) $C_p = A \oplus B$
- d) $C_p = A + \bar{B}$

Answer: option B

Explanation:-

Carry propagate is $cp = a \oplus b$.

The number of gate levels for the carry propagation can be found from the circuit of full adder.

For reference see m. Morris mano digital design page no. 159 (v th edition).

38.Which of the k-maps given below represents the expression $x = ac + bc + b$?

	\bar{C}	C
$\bar{A} \bar{B}$	1	1
$\bar{A} B$	1	1
$A \bar{B}$	0	0
$A B$	0	0

a.

	\bar{C}	C
$\bar{A} \bar{B}$	0	1
$\bar{A} B$	0	0
$A \bar{B}$	1	1
$A B$	1	1

b.

	\bar{C}	C
$\bar{A} \bar{B}$	0	0
$\bar{A} B$	1	1
$A \bar{B}$	1	1
$A B$	0	1

c.

	\bar{C}	C
$\bar{A} \bar{B}$	1	1
$\bar{A} B$	0	1
$A \bar{B}$	0	1
$A B$	1	1

d.

- a) A
- b) B
- c) C
- d) D

Answer: option C

39.A decoder can be used as a demultiplexer by _____.

- a) Tying all enable pins low
- b) Tying all data-select lines low
- c) Tying all data-select lines high
- d) Using the input lines for data selection and an enable line for data input

Answer: option D

40.How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 300_{10} ?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option C

Explanation:-

$300 = 100101100$ (binary).

Total number of digits == 9.

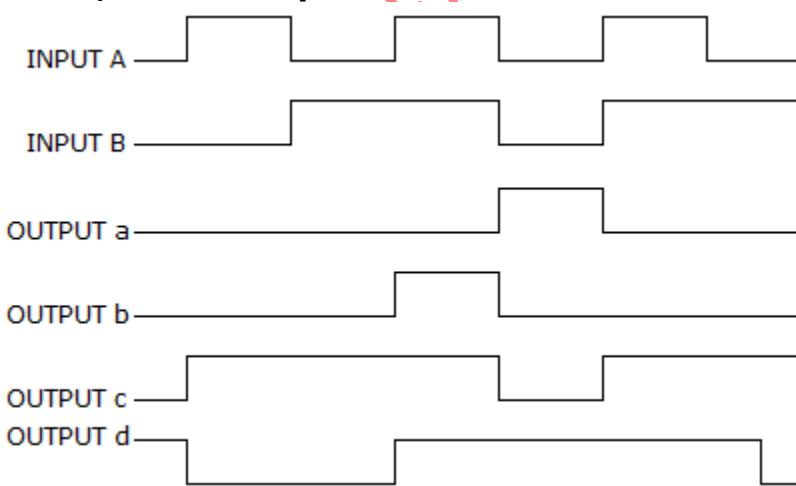
$9/4$ is greater than 2 and less than 4, so obviously 3.

41.Which statement below best describes a karnaugh map?

- a) A karnaugh map can be used to replace boolean rules.
- b) The karnaugh map eliminates the need for using nand and nOR Gates.
- c) Variable complements can be eliminated by using karnaugh maps.
- d) Karnaugh maps provide a visual approach to simplifying boolean expressions.

Answer: option D

42.For a two-input xnOR Gate, with the input waveforms as shown below, which output waveform is correct?



- a) A
- b) B
- c) C
- d) D

Answer: option D

Explanation:-

When both inputs are same then the o/p is high for a xnOR Gate.

I.e.,

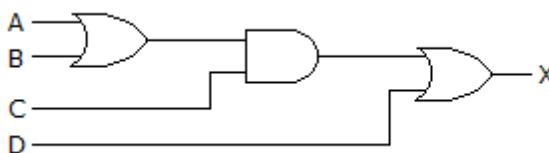
a b o/p
0 0 1
0 1 0
1 0 0
1 1 1

43.A certain BCD-to-decimal decoder has active-high inputs and active-low outputs. Which output goes low when the inputs are 1001?

- a) 0
- b) 3
- c) 9
- d) **None. All outputs are high.**

Answer: option C

44.Solve the network in the figure given below for x.



- a) $A + bc + d$
- b) $((a + b)c) + d$
- c) $D(a + b + c)$
- d) $(ac + bc)d$

Answer: option B

Explanation:-

$A \& B$ are the inputs of OR Gate ,output is $a+b$.

$(a+b) \& C$ are inputs of AND Gate, output is $(a+b)c$.

$(a+b)c \& D$ are the inputs of OR Gate, output is $(a+b)c+d$.

Ans: $(a+b)c+d$.

45.A full-adder has a $c_{in} = 0$. What are the sum (Σ) and the carry (c_{out}) when $a = 1$ and $b = 1$?

- a) $\Sigma = 0, c_{out} = 0$
- b) $\Sigma = 0, c_{out} = 1$
- c) $\Sigma = 1, c_{out} = 0$
- d) $\Sigma = 1, c_{out} = 1$

Answer: option B

Explanation:-

Here a is 1.

And b is 1.

And cin is 0.

For full adder circuit first we have to add a to b.

Then add the result to cin so the result is 0 because,

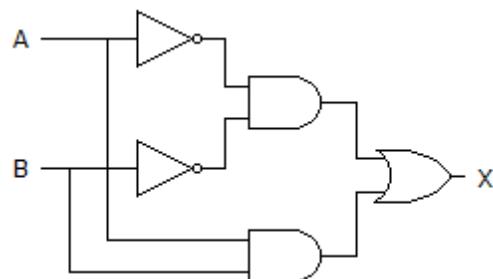
$a+b$ i.e. $1+1=0$.

And $0+cin$ i.e. $0+0=0$.

Here when we are adding a and b, carry is produced.

So cout is 1.

46.What type of logic circuit is represented by the figure shown below?



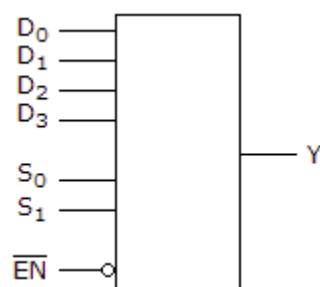
- a) XOR
- b) XNOR
- c) XAND
- d) XNAND

Answer: option B

Explanation:-

Solve the circuit. You get $(ab)' + ab$ which is xnor operation.

47.The device shown here is most likely a _____.



- a) Comparator
- b) Multiplexer
- c) Demultiplexer

d) Parity generator

Answer: option B

48.The design concept of using building blocks of circuits in a pld program is called a(n):

- a) Hierarchical design.**
- b) Architectural design.**
- c) Digital design.**
- d) Verilog.**

Answer: option A

49.When adding an even parity bit to the code 110010, the result is

- _____.
- a) 1110010**
 - b) 1111001**
 - c) 110010**
 - d) 001101**

Answer: option A

Explanation:-

Basically, all the number of ones including the parity bit should be an even number. Before adding the parity bit we had 3 ones to make that even, i.e. Four ones, we need to put 1 in the parity bit place. In even parity the code must contain even number of 1's vice versa.

50.Which of the following combinations of logic gates can decode binary 1101?

- a) One 4-input AND Gate**
- b) One 4-input AND Gate, one OR Gate**
- c) One 4-input nAND Gate, one inverter**
- d) One 4-input AND Gate, one inverter**

Answer: option D

Explanation:-

For decoding any number output must be high for that code and this is possible in d option only.

51.What is the indication of a short to ground in the output of a driving gate?

- a) Only the output of the defective gate is affected.**
- b) There is a signal loss to all load gates.**
- c) The node may be stuck in either the high or the low state.**
- d) The affected node will be stuck in the high state.**

Answer: option B

52.How many outputs would two 8-line-to-3-line encoders, expanded to a 16-line-to-4-line encoder, have?

- a) 3
- b) 4
- c) 5
- d) 6

Answer: option B

TRUE/FALSE

1.An encoder in which the highest and lowest value input digits are encoded simultaneously is known as a priority encoder.

- A)True
- B)False

Answer: option B

2.Three select lines are required to address four data input lines.

- A)True
- B)False

Answer: option B

3.Single looping in groups of three is a common k-map simplification technique.

- A)True
- B)False

Answer: option B

4.In true sum-of-products expressions, the inversion signs cannot cover more than single variables in a term.

- A)True
- B)False

Answer: option A

5.A combinatorial logic circuit has memory characteristics that "remember" the inputs after they have been removed.

- A)True
- B)False

Answer: option B

6.A data selector is also called a demultiplexer.

- A)True
- B)False

Answer: option B

7.A digital circuit that converts coded information into a familiar or non-coded form is known as an encoder.

- A)True
- B)False

Answer: option B

Explanation:-

It's called as a decoder not an encoder.

Because it decodes the information to pc language i.e. Bit 0 or 1.

8.An exclusive-OR Gate will invert a signal on one input if the other is always high.

- A)True
- B)False

Answer: option A

9.The following combination is correct for an even parity data transmission system: data = 100111100 and parity = 0

- A)True
- B)False

Answer: option B

10.The case control structure is used when an expression has a list of possible values.

- A)True
- B)False

Answer: option A

11.Even parity is the condition of having an even number of 1s in every group of bits.

- A)True
- B)False

Answer: option A

12.The look-ahead carry method suffers from propagation delays.

- A)True
- B)False

Answer: option B

13.The boolean equation $(A \bar{B} \bar{C} \bar{D}) + (\bar{A} B \bar{C}) + (\bar{A} D) + (B D)$ results from this karnaugh map.

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$		1	1	
$\bar{A}B$	1	1	1	
$A\bar{B}$		1	1	
AB	1			

A)True

B)False

Answer: option A

14.A pull-up resistor is a resistor used to keep a given point in a circuit high when in the active state.

A)True

B)False

Answer: option A

15.The simplified form of $X = AB + ABC + A(\bar{B} + \bar{C})$ is $X = A$.

A)True

B)False

Answer: option A

16.In an even-parity system, the following data will produce a parity bit = 1.

Data = 1010011

A)True

B)False

Answer: option B

17.The following combination is correct for an odd parity data transmission system: data = 011011100 and parity = 0

A)True

B)False

Answer: option A

18.The xOR Gate will produce a high output if only one but not both of the inputs is high.

A)True

B)False

Answer: option A

19.When decisions demand one of many possible actions, the elseif control structure is used.

A)True

B)False

Answer: option A

20.The k-map provides a "graphical" approach to simplifying sum-of-products expressions.

A)True

B)False

Answer: option A

21.The 54 prefix on ics indicates a broader operating temperature range, generally intended for military use.

A)True

B)False

Answer: option A

22.This is an example of a pos expression: $X = (A + B)(C + D)$

A)True

B)False

Answer: option A

24.The boolean equation $(\bar{A} \bar{B}) + (\bar{A} C) + (B C)$ results from this karnaugh map.

\bar{C}	C
$\bar{A} \bar{B}$	1
$\bar{A} B$	1
$A \bar{B}$	1
$A B$	1

A)True

B)False

Answer: option B

25.The abbreviation for an exclusive-OR Gate is xor.

A)True

B)False

Answer: option A

26.In an even-parity system, the parity bit is adjusted to make an even number of one bits.

A)True

B)False

Answer: option A

27.The boolean equation of the exclusive-nor function is $x = AB + \bar{A}\bar{B}$.

- A)True
- B)False

Answer: option A

Explanation:-

Answer is $x=ab+(\sim a)(\sim b)$

28.To implement the full-adder sum functions, two exclusive-OR Gates can be used.

- A)True
- B)False

Answer: option A

29.The input at the 1, 2, 4, 8 inputs to a 4-line to 16-line decoder with active-low outputs is 1110. As a result, output line 7 is driven low.

- A)True
- B)False

Answer: option B

Explanation:-

The answer should be "true".

Reason:

the decimal equivalent of given input is 7, so in the decoder 7th line should be active. Since the decoder has active low output, it means the output will be low(0) at the line which has to be active.

Now 7th line has to be active according to given condition.so it should be low. Hence answer is "true".

30.When decisions demand two possible actions, the if/then/else control structure is used.

- A)True
- B)False

Answer: option A

31.TTL stands for transistor-technology-logic.

- A)True
- B)False

Answer: option B

Explanation:-

TTL is transistor transistor logic.

32. Truth tables are great for listing all possible combinations of independent variables.

A) True

B) False

Answer: option A

33. The k-map in the figure below shows the correct implementation of the expression $x = acd + ab(cd + bc)$.

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}B$	0	0	0	0
$\bar{A}B$	0	0	1	1
$A\bar{B}$	0	0	0	1
$A\bar{B}$	0	0	0	1

A) True

B) False

Answer: option B

34. A square in the top row of a k-map is considered to be adjacent to its corresponding square in the bottom row.

A) True

B) False

Answer: option A

35. $X = ABC\bar{C} + BCD\bar{D}$ is in the form of a sum-of-products expression.

A) True

B) False

Answer: option A

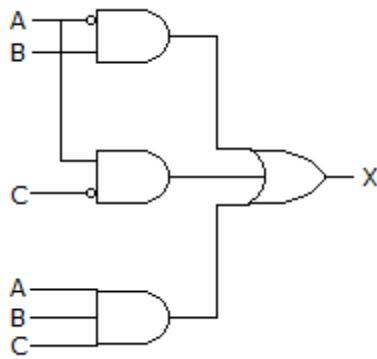
Explanation:-

In a sop all the variables must be present in the expression(either in true or complement form).

So the answer will be false. Here in the 1st term d is missing so multiply it with $d+d'$ and similarly in the 2nd term multiply with $a+a'$.

The sop will be $abc'd + abc'd' + aBCD' + a'BCD$ '

36. The circuit given below implements the equation, $X = \bar{A}B + A\bar{C} + ABC$.



- A)True
B)False**

Answer: option A

37.The simplified form of $X = \bar{A} + A\bar{C}$ is $X = A\bar{C}$.

- A)True
B)False**

Answer: option B

38.The carry output of each adder in a ripple adder provides an additional sum output bit.

- A)True
B)False**

Answer: option A

39.A good rule of thumb for determining the pin numbers of dual-in-line package ic chips would be to place the notch to your right and pin #1 will always be in the lower right corner.

- A)True
B)False**

Answer: option B

Explanation:-

Notch is placed to left and pin 1 is in lower left.

FILL UP THE BLANKS

1.For the xnOR Gate truth table shown below, the values for w, x, y, and z are _____, _____, _____, and _____, respectively.

INPUTS	OUTPUT
0 0	w
0 1	x
1 0	y
1 1	z

- a) 1, 0, 0, 1
- b) 0, 1, 0, 1
- c) 1, 1, 1, 0
- d) 1, 0, 0, 0

Answer: option A

Explanation:-

If both bits are equal then o/p is 1.

2.A half-adder does not have _____.

- a) Carry in
- b) Carry out
- c) Two inputs
- d) All of the above

Answer: option A

3.The equation _____ cannot be further simplified.

- a) $\bar{A}B + A\bar{C} + \bar{B}C = X$
- b) $\bar{A}B(\bar{A}C + C) = X$
- c) $\bar{A}B + AB + \bar{A}C = X$
- d) $\bar{A}B(B + C) = X$

Answer: option A

4._____ is a correct combination for an odd-parity data transmission system.

- a) Data = 1101 1011;parity = 1
- b) Data = 1101 0010;parity = 0
- c) Data = 0001 0101;parity = 1
- d) Data = 1010 1111;parity = 0

Answer: option A

5.A circuit that can convert one of ten numerical keys pressed on a keyboard to BCD is a _____.

- a) Priority encoder
- b) Decoder
- c) Multiplexer
- d) Demultiplexer

Answer: option A

6.The _____ prefix on ic's indicates a broader operating temperature range, and the devices are generally used by the military.

- a) 54
- b) 2n
- c) 74
- d) TTL

Answer: option A

7.When an open occurs on the input of a TTL device, the output will _____.

- a) Go low, because there is no current in an open circuit
- b) React as if the open input were a high
- c) Go high, since full voltage appears across an open
- d) Still be good, if only the good inputs are used

Answer: option B

8.The boolean equation for the exclusive-or function is _____.

- a) $X = \overline{A}B + A\overline{B}$
- b) $X = \overline{A}B + \overline{A}\overline{B}$
- c) $X = \overline{A}\overline{B} + A\overline{B}$
- d) $X = \overline{A}B + A\overline{B}$

Answer: option D

9.The largest truth table that can be implemented directly with an 8-line-to-1-line mux has _____.

- a) 3 rows
- b) 4 rows
- c) 8 rows
- d) 16 rows

Answer: option C

10.Parity generation and checking is used to detect _____.

- a) Which of two numbers is greater
- b) Errors in binary data transmission
- c) Errors in arithmetic in computers
- d) When a binary counter counts incorrectly

Answer: option B

11.Except for _____, std_logic may have the following values.

- a) 'Z'
- b) 'U'

- c) '?'
- d) 'L'

Answer: option C

12.A gate that could be used to compare two logic levels and provide a high output if they are equal is a(n) _____.

- a) XOR Gate
- b) XnOR Gate
- c) NAND Gate
- d) NOR Gate

Answer: option B

13.VHDL is very strict in the way it allows us to assign and compare _____ such as signals, variables, constants, and literals.

- a) Objects
- b) Logic_vectors
- c) Designs
- d) Arrays

Answer: option A

14.The and-or-invert gates are designed to simplify implementation of _____.

- a) Pos logic
- b) Demorgan's theorem
- c) Nand logic
- d) Sop logic

Answer: option B

15.The output of a gate has an internal short; a current tracer will _____.

- a) Identify the defective gate
- b) Show whether the gate is shorted to v_{cc} or ground
- c) Probably not be able to locate the problem
- d) Be able to identify the defective load node

Answer: option A

16.Parity generators and checkers use _____ gates.

- a) Exclusive-and
- b) Exclusive-or/nor
- c) Exclusive-or
- d) Exclusive-nand

Answer: option B

17.The 7447a is a BCD-to-7-segment decoder with ripple blanking input and output functions. The purpose of these lines is to _____.

- a) Turn off the display for any non significant digit
- b) Turn off the display for any zero
- c) Turn off the display for leading or trailing zeros
- d) Test the display to assure all segments are operational

Answer: option A

18.One reason for using the sum-of-products form is that it can be implemented using all _____ gates without much difficulty.

- a) NOR
- b) NAND
- c) AND
- d) OR

Answer: option B

19.When an open occurs on the input of a CMOS gate, the output will _____.

- a) Go low, because there is no current in an open circuit
- b) React as if the open input were a high
- c) Go high, since full voltage appears across an open
- d) Be unpredictable; it may go high or low

Answer: option D

20.To subtract a signed number (the subtrahend) from another signed number (the minuend) in the 2's complement system, the minuend is _____.

- a) Complemented only if it is positive
- b) Complemented only if it is negative
- c) Always complemented
- d) Never complemented

Answer: option D

21.The correct output for this xor truth table is _____.

A	B	X
0	0	?
0	1	?
1	0	?
1	1	?

$X = 0$

0

1

a) $\begin{array}{r} 1 \\ X = 0 \end{array}$

0

0

b) $\begin{array}{r} 1 \\ X = 0 \end{array}$

1

1

c) $\begin{array}{r} 1 \\ X = 0 \end{array}$

1

1

d) $\begin{array}{r} 0 \\ X = 0 \end{array}$

Answer: option D

22.In an odd-parity system, the data that will produce a parity bit = 1 is _____.

- a) Data = 1010011
- b) Data = 1111000
- c) Data = 1100000
- d) All of the above

Answer: option D

23.The addition of two signed numbers in the 2's complement system can cause overflow. For overflow to occur both numbers must _____.

- a) Be positive
- b) Be negative
- c) Have the same sign
- d) Have opposite signs

Answer: option C

24.The boolean equation _____ results from this karnaugh map.

	\bar{C}	C
$\bar{A} \bar{B}$	1	1
$\bar{A} B$		1
A \bar{B}	1	
A B	1	

$$(\bar{A} \bar{B}) + (\bar{A} C) + (A \bar{C})$$

$$(\bar{A} \bar{B}) + (A \bar{B}) + (B \bar{C})$$

$$(A \bar{B}) + (\bar{A} B) + (\bar{B} \bar{C})$$

$$(A B) + (\bar{B} \bar{C}) + (\bar{B} C)$$

Answer: option A

25. A karnaugh map will _____.

- a) Eliminate the need for tedious boolean simplifications
- b) Allow any circuit to be implemented with just AND and OR Gates
- c) Produce the simplest sum-of-products expression
- d) Give an overall picture of how the signals flow through the logic circuit

Answer: option A

26. An 8-bit binary number is input to an odd parity generator. The parity bit will equal 1 only if _____.

- a) The number is odd
- b) The number of 1s in the number is odd
- c) The number is even
- d) The number of 1s in the number is even

Answer: option D

27. Two 4-bit comparators are cascaded to form an 8-bit comparator. The cascading inputs of the most significant 4 bits should be connected _____.

- a) To the outputs from the least significant 4-bit comparator
- b) To the cascading inputs of the least significant 4-bit comparator
- c) A = b to a logic high, a < b and a > b to a logic low
- d) Ground

Answer: option A

28. When karnaugh mapping, we must be sure to use the _____ number of loops.

- a) Maximum
- b) Minimum

- c) Median
- d) Karnaugh

Answer: option B

29. The final output of a pos circuit is generated by _____.

- a) An and
- b) An or
- c) An nor
- d) An nand

Answer: option A

30. After each circuit in a subsection of a VHDL program has been _____, they can be combined and the subsection can be tested.

- a) Designed
- b) Tested
- c) Engineered
- d) Produced

Answer: option B

31. The _____ series of ic's are pin, function, and voltage-level compatible with the 74 series ic's.

- a) Als
- b) CMOS
- c) hct
- d) 2n

Answer: option C

31. The simplified form of $X = AC + \bar{C}(A + B)$ is _____.

- a) $X = \bar{C} + AC$
- b) $X = AC + B$
- c) $X = AC + BC$
- d) $X = A + BC$

Answer: option D

32. The _____ circuit produces a high output whenever the two inputs are equal.

- a) Exclusive-and
- b) Exclusive-nand
- c) Exclusive-nor
- d) Exclusive-or

Answer: option C

33. A 4-bit adder has the following inputs: $c_0 = 0$, $a_1 = 0$, $a_2 = 1$, $a_3 = 0$, $a_4 = 1$, $b_1 = 0$, $b_2 = 1$, $b_3 = 1$, $b_4 = 1$. The output will be _____.

- a) 01100
- b) 10101
- c) 11000
- d) 00011

Answer: option C

34. The _____ statement evaluates the variable status.

- a) If/then
- b) If/then/else
- c) Case
- d) Elseif

Answer: option A

35. In VHDL, data can be each of the following types except _____.

- a) Bit
- b) Bit_vector
- c) Std_logic
- d) Std_vector

Answer: option D

36. When grouping cells within a k-map, the cells must be combined in groups of _____.

- a) 2's
- b) 1, 2, 4, 8, etc.
- c) 4's
- d) 3's

Answer: option B

37. The _____ circuit produces a high output whenever the two inputs are unequal.

- a) Exclusive-and
- b) Exclusive-nor
- c) Exclusive-or
- d) Inexclusive-or

Answer: option C

38. The boolean equation _____ results from this karnaugh map.

	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
$\bar{A}\bar{B}$		1		1
$\bar{A}B$		1		
$A\bar{B}$		1		1
AB		1		1

- a) $(A C \bar{D}) + (\bar{B} C \bar{D}) + (\bar{C} D)$
- b) $(A B \bar{D}) + (\bar{B} \bar{C} D) + (\bar{C} D)$
- c) $(\bar{A} C \bar{D}) + (B \bar{C} \bar{D}) + (\bar{B} \bar{C})$
- d) $(\bar{A} B \bar{D}) + (A \bar{C} D) + (C D)$

Answer: option A

39. Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as in a BCD-to-decimal converter. These result in _____ terms in the k-map and can be treated as either _____ or _____, in order to _____ the resulting term.

- a) Don't care, 1's, 0's, simplify
- b) Spurious, and's, or's, eliminate
- c) Duplicate, 1's, 0's, verify
- d) Spurious, 1's, 0's, simplify

Answer: option A

9.SIGNALS AND SWITCHES

1.Why does the TTL family use a totem-pole circuit on the output?

- a) It provides active pull-up.
- b) It provides active pull-down.
- c) It provides active pull-up and active pull-down.

Answer: option C

Explanation:-

Totem-pole means push pull output.

2.What is the frequency of a clock waveform if the period of that waveform is 1.25 μ s?

- a) 8 khz
- b) .8 khz
- c) .8 mhz
- d) 8 mhz

Answer: option C

Explanation:-

By the formula of frequency we can find the frequency of clock waveform.

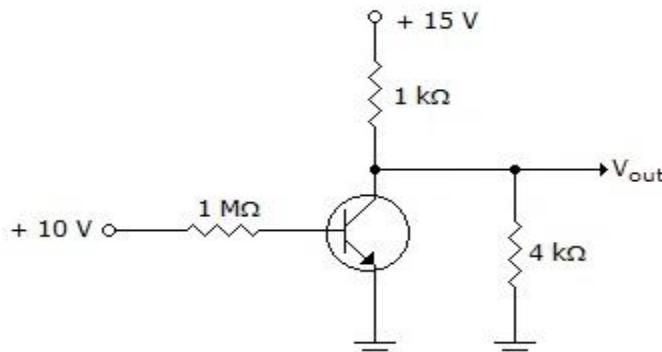
Time period(t)is given of that waveform is=1.25microseconds
 $f=1/t$

where t is the time taken by the clock waveform.

$$F=(1/1.25)$$

and $f=0.8\text{mhz}$

3.Why is the given circuit called an inverter?



- a) The output is the opposite (inverse) of the input.
- b) The output is in phase with the input.
- c) The output is the same as the input.
- d) There is no output.

Answer: option A

Explanation:-

If the input signal is high there will flow current through 1 megohm and the transistor's base-emitter junction (base, NOT Gate). This current will be amplified, and the collector current through 1 kohm will cause a voltage drop so that the output will be low. Input high, output low.

If the input signal is low there won't be any base current, and no collector current. No current through r1 means no voltage drop, so that the output will be at +v. Input low, output high.

From figure, when base current is maximum in the positive direction, collector emmiter voltage become max'm in the negative direction and vise-versa. Thus, input and output voltages are in phase opposition ie.the transister has produced a phase reversal of output voltage w.r.t. The input signal voltage.

4.The hexadecimal number $4b_{16}$ is transmitted as an 8-bit word in parallel. What is the time required for this transmission if the clock frequency is 2.25 mhz?

- a) 444 ns
- b) 444 μ s
- c) 3.55 μ s
- d) 3.55 ms

Answer: option A

Explanation:-

Thats because data is being transmitted in a parallel manner, so it would take only one clock pulse to transmit whole data.

Or

Because the clock pulse of 4-bit transmit the data of 8-bit word in parallel mode.

And this transmission done at 2.25mhz frequency.

We know that;

$$f=1/t$$

and we can find the time required for this transmission by the clock pulse

5.Internally, a computer's binary data are almost always transmitted on parallel channels, commonly referred to as the:

- a) Parallel bus
- b) Serial bus
- c) Data bus
- d) Memory bus

Answer: option C

Explanation:-

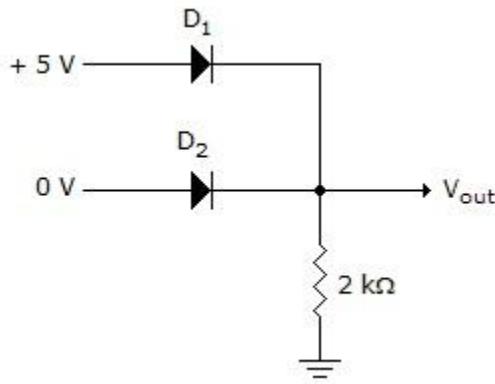
Because computer's data always in the binary form which is stored in the bus that transmit the data on any channels it doesn't matter that it's in parallel or serial.

6.Why is parallel data transmission preferred over serial data transmission for most applications?

- a) It is much slower.
- b) It is cheaper.
- c) More people use it.
- d) It is much faster.

Answer: option D

7.Determine if diodes d_1 and d_2 in the given figure are forward or reverse biased.



- a) D_1 forward and d_2 reverse
- b) D_2 forward and d_1 reverse
- c) D_1 and d_2 reverse
- d) D_1 and d_2 forward

Answer: option A

Explanation:-

consider at time t0: voltage v_{out} is undefined. If we assume that voltage to be less than the anode v_g of the diode d_1 then and then only it is said to forward biased. Same thing to the diode d_2 and hence anode voltage at d_2 is 0v and hence which is less than the previous assumption the it is reverse biased. (if you assume in opposite way then both of the diodes are reverse biased).

7.With surface-mount technology (smt), the devices should:

- a) Utilize transistor outline connections
- b) Mount directly
- c) Have parallel connecting pins
- d) Require holes and pads

Answer: option B

Explanation:-

Surface-mount technology (smt) is a method for producing electronic circuits in which the components are mounted or placed directly onto the surface of printed circuit boards (pcbs). An electronic device so made is called a surface-mount device (smd). In the industry it has largely replaced the through-hole technology construction method of fitting components with wire leads into holes in the circuit board. Both technologies can be used on the same board for components not suited to surface mounting such as large transformers and heat-sunked power semiconductors.

8.To forward bias a diode, a _____ potential is needed on the _____ and a _____ is needed on the _____.

- a) Negative, cathode, positive, anode
- b) Negative, anode, positive, cathode

Answer: option A

9.Why, in most applications, are transistor switches used in place of relays?

- a) They consume less power.
- b) They are faster.
- c) They are quieter and smaller.
- d) All of the above

Answer: option D

10.How long will it take to serially transmit the hexadecimal number $c3_{16}$ if the clock frequency is 1.5 mhz?

- 1. 4.69 ms
- 2. 4.69 μ s
- 3. 5.33 ms
- 4. 5.33 μ s

Answer: option D

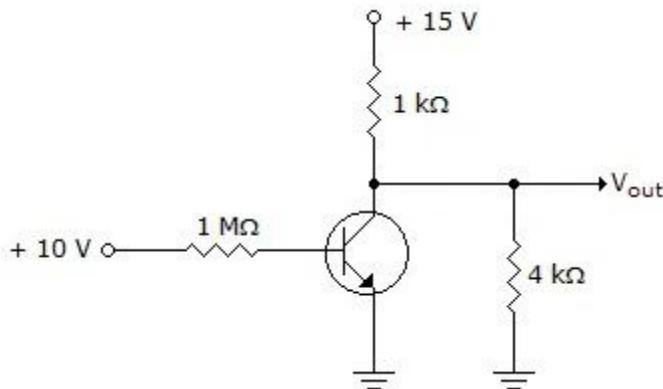
Explanation:-

Here in this question the data are serially transmit right so we will consider the bits.

Now, (c3) hexa decimal means (1100 0011) right that means no of bits is 8 and the value is c3.

So, time = (no of bits/frequency) = $8 / (1.5 * 10^6)$ = 5.33 micro seconds.

11.What is the output voltage from the circuit in the given figure?



- a) +15 v
- b) +12 v
- c) +3 v
- d) 0 v

Answer: option D

Explanation:-

$$V_{ce} = V_{cc} - I_c \cdot R_C$$

When the tr. Conduct(due to positive i/p or base-emitter voltage here ce config.) the collector current increases and voltage drop across R_C increases which in turns decreases V_{ce} bcz V_{cc} is fixed. That's why when input voltage is high then output voltage V_{ce} is 0 i.e 0v.

12.The family of logic that is composed of bipolar junction transistors is ____.

- a) TTL
- b) CMOS
- c) DIP
- d) BJT

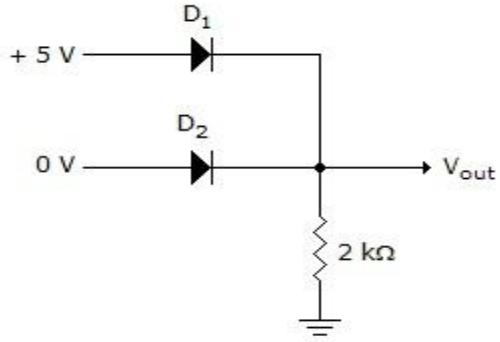
Answer: option A

13.What can a relay provide between the triggering source and the output that semiconductor switching devices cannot?

- a) Total isolation
- b) Faster
- c) Higher current rating
- d) Total isolation and higher current rating

Answer: option D

14.Determine the output voltage V_{out} for the circuit in the given figure.



- a) -0.5 v
- b) 0 v
- c) +5 v
- d) +4.3 v

Answer: option D

Explanation:-

Voltage drop by the diode is .7v .

So the output will be

$$5v-.7v=4.3v$$

(d) is correct answer.

15. The serial format for transmitting binary information uses:

- a) A single conductor
- b) Multiple conductors
- c) Infrared technology
- d) Fiber-optic

Answer: option A

16. Which device(s) have almost ideal on and off resistances?

- a) Electromechanical relays
- b) Manual switches
- c) Semiconductor devices (diodes and transistors)
- d) Electromechanical relays and manual switches

Answer: option D

17. A diode placed in parallel across a relay coil serves what function?

- a) To regulate input voltage
- b) To protect the coil from arcing
- c) To ensure most of the current passes through the coil
- d) To reduce arcing across the relay contacts

Answer: option B

Explanation:-

During opening of current carrying contacts in a circuit breaker the medium in between opening contacts become highly ionized through which the interrupting current gets low resistive path and continues to flow through this path even the contacts are physically separated. During the flowing of current from one contact to another the path becomes so heated that it glows. This is called arc.

18. Serial communication can be speed up by:

- a) Using silver or gold conductors instead of copper
- b) Using high-speed clock signals
- c) Adjusting the duty cycle of the binary information
- d) Using silver or gold conductors instead of copper and high-speed clock signals

Answer: option B

19. What is the period of a clock waveform that has a frequency of 15.4 khz?

- a) 649 μ s
- b) 6.49 μ s
- c) 64.9 μ s
- d) .649 μ s

Answer: option C

Explanation:-

Use formulae:

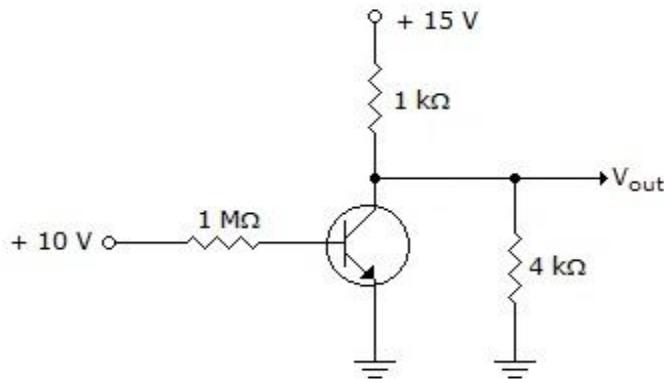
$$f=1/t$$

20. TTL logic chips must have connections to v_{cc} and ground, even if all inputs and outputs are properly used and tied to valid signals.

- A) True
- B) False

Answer: option A

21. What is the output voltage v_{out} for the given circuit if the input voltage changes to 0 v?



- a) +12 v
- b) +15 v
- c) +3 v
- d) 0 v

Answer: option A

Explanation:-

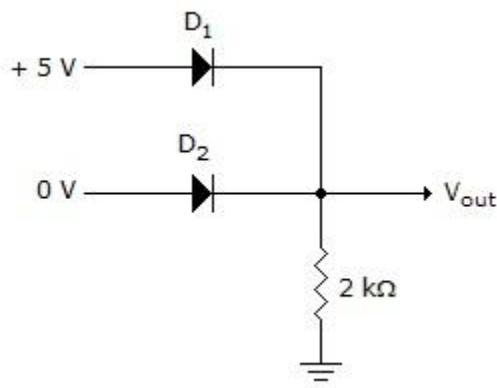
It is similar to voltage divider.

$$V_{out} = \{[r_2/(r_1+r_2)] * v_{in}\}.$$

$$= (4/5)*15.$$

$$= 12v.$$

22. If the input voltage on D_1 in the given figure is changed to 0 v, what is the output voltage V_{out} ?



- a) -5 v
- b) 0 v
- c) + 5 v
- d) +4.3 v

Answer: option B

Explanation:-

Because when we will apply 0v to the input of d1 then both the diodes will be reversed biased and thus they will be open circited and thus output will be 0 volt.

23.An indication of cutoff in an npn bipolar transistor is that the:

- a) Collector current is maximum
- b) Collector-to-emitter voltage equals zero
- c) Base-to-emitter voltage equals 0.7 v
- d) Collector to emitter appears to be open

Answer: option D

24.When an ic has two rows of parallel connecting pins, the device is referred to as a:

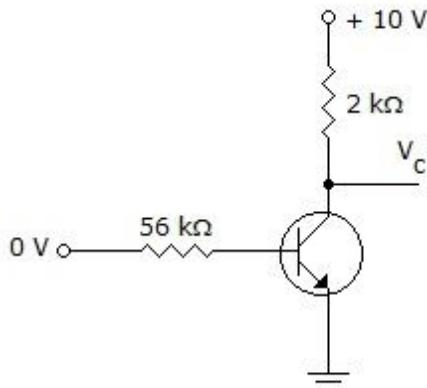
- a) Qfp
- b) Dip
- c) Tssop
- d) CMOS

Answer: option B

Explanation:-

Dual in-line package (dip).

25.If the input voltage on the base of the transistor in the given figure is changed to +10 v, what is the new voltage at the collector V_c ?



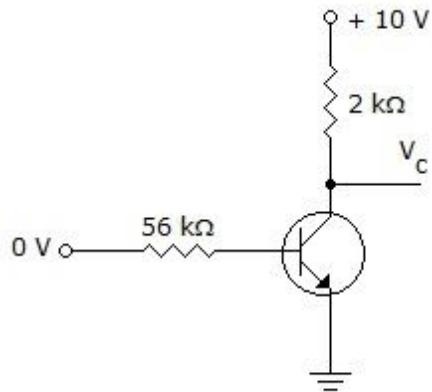
- a) Not enough information is provided.
- b) $V_c = 10 \text{ v}$
- c) $V_c = 0 \text{ v}$
- d) $V_c = 5 \text{ v}$

Answer: option C

Explanation:-

To turn on npn bipolar transistor requires the base to be negative with respect to collector.

26. Is the transistor in the given figure considered on or off?



- a) Off
- b) On
- c) Not enough information is provided.

Answer: option A

Explanation:-

To turn the npn transistor on, the base should be negative with respect to the collector.

27. Normal operation of an npn bipolar transistor requires the base to be _____ with respect to the emitter, and _____ with respect to the collector.

- a) Positive, negative
- b) Positive, positive
- c) Negative, positive
- d) Negative, negative

Answer: option A

28. The abbreviation NO, when used with respect to electromechanical relays, stands for not operational.

- A) True
- B) False

Answer: option B

Explanation:-

No means "normally open"

29.In a graphical representation of voltage versus time, _____ is displayed on the _____ axis and _____ is displayed on the _____ axis.

- a) Time, y, voltage, x
- b) Voltage, y, time, x

Answer: option B

Explanation:-

Constant will be always on y axis and varying quantity will be always on x axis.

30.What is the minimum voltage required before a diode will allow current to flow between the cathode and the anode?

- a) 0.7 v
- b) 0.07 v
- c) 4.3 v
- d) 0.2 v

Answer: option A

Explanation:-

This is called as break down voltage of the diode. It is the voltage after which diode starts conducting.

31.What is the advantage of using serial data transmission over parallel data transmission?

- a) It is slower.
- b) Only one pair of wires is required.
- c) More people use it.
- d) It is faster.

Answer: option B

32.A TTL totem-pole circuit is designed so that the output transistors:

- a) Are always on together
- b) Provide phase splitting
- c) Provide voltage regulation
- d) Are never on together

Answer: option D

33.What is the advantage of using CMOS logic over TTL?

- a) It switches faster.
- b) It uses less power.
- c) It is larger.
- d) Cost

Answer: option B

Explanation:-

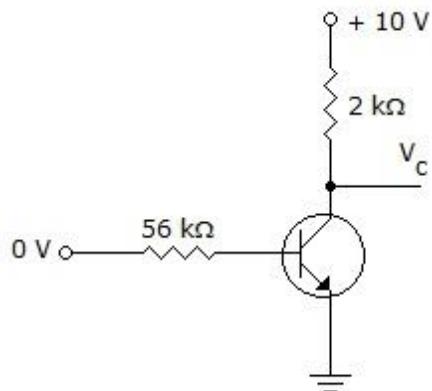
Option a is also right because CMOS switching speed is faster than TTL.

34.What is used to graphically show the time relationship between two or more digital waveforms?

- a) Reference diagram
- b) Timing diagram
- c) Voltage curve
- d) Load line

Answer: option B

35.Determine the voltage on the collector v_c of the given transistor circuit.



- a) 0 v
- b) +10 v
- c) +4.7 v
- d) +0.5 v

Answer: option B

Explanation:-

Simply here emitter current(i_e) is zero.so $i_e = i_c$ (collector current)due to small value of beta. $I_e = i_c = 0$ so $v_c = 10v$

36.The period of a waveform is the percentage of time the signal is high.

- A)True
- B)False

Answer: option B

37.What is a disadvantage of CMOS in place of TTL?

- a) It switches slower.

- b) It uses less power.
- c) It is smaller.
- d) Cost

Answer: option A

38.The units for the high time for a periodic wave are _____.

- a) Seconds
- b) Hertz
- c) Cycles
- d) %

Answer: option A

Explanation:-

I think answer is d, i.e, duty cycle = $t_{on}/t_{in} \%$.

TRUE/FALSE

1.Precise timing is not important in digital signals.

- A)True
- B)False

Answer: option B

2.A plot of voltage versus time is called a timing diagram.

- A)True
- B)False

Answer: option A

3.The CMOS uses bipolar transistors instead of mosfet.

- A)True
- B)False

Answer: option B

4.Most modern digital systems are based on semiconductor technology.

- A)True
- B)False

Answer: option A

5.The so package is available for the most popular TTL and CMOS digital logic and analog ic devices.

- A)True
- B)False

Answer: option A

6.The ability to manufacture smaller, more dense components has been fulfilled by smd.

- A)True**
- B)False**

Answer: option A

7.An electromechanical relay is operated manually.

- A)True**
- B)False**

Answer: option A

8.Serial communications cannot be speed up.

- A)True**
- B)False**

Answer: option B

9.Manual switches and relays have identical on and off resistances.

- A)True**
- B)False**

Answer: option B

10.The frequency of the clock waveform is defined as the reciprocal of the clock period.

- A)True**
- B)False**

Answer: option A

10.FLIP-FLOPS

1.Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 mhz.

- a) 10.24 khz
- b) 5 khz
- c) 30.24 khz
- d) 15 khz

Answer: option B

Explanation:-

We know that a single flip flop contains 2 states. For 1 ff frequency is $1/2$, for 2 ff frequency is $1/4$.

I.e. $1/2^n$, where n is the no. Of ff.

So for 12 ff, frequency is $1/2^{12} = 1/4096$.

So, o/p frequency = (i/p frequency)*(1/4096)...

We also called it as a divider ckt.

2.Which statement best describes the operation of a negative-edge-triggered d flip-flop?

- a) The logic level at the d input is transferred to q on ngt of clk.
- b) The q output is always identical to the clk input if the d input is high.
- c) The q output is always identical to the d input when clk = pgt.
- d) The q output is always identical to the d input.

Answer: option A

Explanation:-

Point1:

ff is -ve edge triggered means the o/p will follow i/p only on transition of clock from 1 to 0.

It means that the o/p $d = q_n = q_{n-1}$ when clock changes from 1 to 0.

3.Propagation delay time, t_{plh} , is measured from the _____.

- a) Triggering edge of the clock pulse to the low-to-high transition of the output
- b) Triggering edge of the clock pulse to the high-to-low transition of the output
- c) Preset input to the low-to-high transition of the output
- d) Clear input to the high-to-low transition of the output

Answer: option A

Explanation:-

Propagation delay is the time taken to change the state after applying the clock pulse.

T_{plh} means : propagation delay time for low to high transition of output.

Therefore,

answer (a) is correct one.

Propagation delay time, t_{plh} is the time between (the instant at which clock pulse is applied) and (the instant at which the low to high transition of the output takes place).

T_{plh} is the time it takes for the input to the output from low to high.

The thing to note here is that, the "change" in the output of the flip flop is not governed by the input at the din port but the edge of the clock. So no matter when the input at din arrived, it'll not affect the output unless a positive edge of the clock is encountered. This is the reason why t_{plh} (or hl) is measured with respect to clock.

4.How is a j-k flip-flop made to toggle?

- a) J = 0, k = 0
- b) J = 1, k = 0
- c) J = 0, k = 1
- d) J = 1, k = 1

Answer: option D

Explanation:-

J-k ff will toggle means it has to behave like a t-ff.

So if we design a t-ff from a j-k ff simply make j=k connection.

Now this ff will behave like t-ff.

When t=1(indirectly j=k=1) in t-ff, it toggles its input.

When j=k=1 then the race condition is occurs that means both output wants to become high. Hence there is toggle condition is occurs.

When j=1 and k=1, with each passing clock pulse the output q changes from 0 to 1 and 1 to 0. That's why its called a toggle state.

5.How many flip-flops are in the 7475 ic?

- a) 1
- b) 2
- c) 4
- d) 8

Answer: option C

Explanation:-

Ic-7475 it is the code (or number) to find out the j-k flip-flop, while ic-7474 is d-ff. And some other ff's have their own codes to find or recognize.

Rs flip-flop

jk flip-flop
d flip-flop
t flip-flop

6.How many flip-flops are required to produce a divide-by-128 device?

- a) 1
- b) 4
- c) 6
- d) 7

Answer: option D

Explanation:-

Even if there is 127 it is less than 128(2^7) and more than 64 (2^6). So the number of flip flop requires will be the same 7.

Or

$2^{(n-1)} < n < 2^n$. [here $n=128$].

Since given that it's a divide by 128 device. $2^n > 127$ {because the flip flops could count from 0 to given no-1 i.e, 0 to $128-1=127$ }..

Therefore. =7.. Where n is the no of flip flops necessary.

7.Which is not an altera primitive port identifier?

- a) Clk
- b) Ena
- c) Clr
- d) Prn

Answer: option C

Explanation:-

Clk - clock

ena - enable (level triggered)

prn - preset (asynchronous)

j,k,d,s,r-input

q - q output

these are the only altera primitive port identifiers.

Clr is not there.

Basically when we are writing program in VHDL we use some standard libraries. Over there, there are some instances already provided for use. It is one of those instances. We use them by "-.q" where - can be name of flipflop we have given.

8.The timing network that sets the output frequency of a 555 astable circuit contains _____.

- a) Three external resistors are used

- b) Two external resistors and an external capacitor are used**
- c) An external resistor and two external capacitors are used**
- d) No external resistor or capacitor is required**

Answer: option B

Explanation:-

The above referenced astable circuit is multivibrator. The astable multivibrator generates a square wave, the period.

Of which is determined by the circuit external to ic 555. The astable multivibrator does not require any external trigger to change the state of the output. Hence it is also known as free running oscillator. The time during which the output is either high or low is determined by the two resistors and a capacitor which are externally connected to the 555 timer.

9.What is the difference between the enable input of the 7475 and the clock input of the 7474?

- a) The 7475 is edge-triggered.**
- b) The 7474 is edge-triggered.**

Answer: option B

Explanation:-

Flipflops are all edge sensitive, where latches are level sensitive. Flipflops can be made by connecting latches with additional gates connected to it.

10.The phenomenon of interpreting unwanted signals on j and k while c_p (clock pulse) is high is called _____.

- a) Parity error checking**
- b) Ones catching**
- c) Digital discrimination**
- d) Digital filtering**

Answer: option B

Explanation:-

The "catching" issue has to do with short-term glitches, not with the well-known indeterminate states of sr or jk flip-flops. Even a master-slave jk flip-flop, under the right conditions, will set or clear if an input is glitched. Ones-catching means that the input transitioned to a 1 and back very briefly (unintentionally due to a glitch), but the flip-flop responded and latched it in anyway, i.e., it caught the 1. Similarly for 0's catching.

The interior of the jk flip flop still has asynchronous bi-stables made from either nands or nors. The nand will catch ones, the nor will catch zeroes.

10.What is another name for a one-shot?

- a) Monostable**

- b) Multivibrator**
- c) Bistable**
- d) Astable**

Answer: option A

Explanation:-

Since after triggering one monostable multivibrator attains stability.

11.On a master-slave flip-flop, when is the master enabled?

- a) When the gate is low**
- b) When the gate is high**
- c) Both of the above**
- d) Neither of the above**

Answer: option B

Explanation:-

Option b is correct since, basically master slave ff is used to solve the problem of "race around condition. This ff consists of two circuits namely master and slave, and for master we will give clock directly (i.e high) and for slave we will give invert of clock (i.e low), and the output state will change only when the state of the slave changes (i.e the output state of the master -slave ff depend's only on the state of the slave) so that the option b is absolutely correct.

12.One example of the use of an s-r flip-flop is as a(n):

- a) Racer**
- b) Astable oscillator**
- c) Binary storage register**
- d) Transition pulse generator**

Answer: option C

Explanation:-

Yes i agree flip flop is a memory element that's why example of s-r flip flop is binary storage register.

Or

S-r refers to set-reset. So it is used to store two values 0 and 1. Hence it is referred as binary storage element.

13.What is the difference between the 7476 and the 74ls76?

- a) The 7476 is master-slave, the 74ls76 is master-slave**
- b) The 7476 is edge-triggered, the 74ls76 is edge-triggered**
- c) The 7476 is edge-triggered, the 74ls76 is master-slave**
- d) The 7476 is master-slave, the 74ls76 is edge-triggered**

Answer: option D

Explanation:-

7476 and 74ls76 both are master slave because here "ls" indicates low power schottky.

14.Which of the following is correct for a gated d flip-flop?

- a) The output toggles if one of the inputs is held high.**
- b) Only one of the inputs can be high at a time.**
- c) The output complement follows the input when enabled.**
- d) Q output follows the input d when the enable is high.**

Answer: option D

Explanation:-

If clock is high then the d flip flop operate and we know that input is equals to output in case d flip flop. As in this d-flip flop the output will be same as of input, it is the condition of this flip flop.

15.With regard to a d latch, _____.

- a) The q output follows the d input when en is low**
- b) The q output is opposite the d input when en is low**
- c) The q output follows the d input when en is high**
- d) The q output is high regardless of en's input state**

Answer: option C

16.How can the cross-coupled nand flip-flop be made to have active-high s-r inputs?

- a) It can't be done.**
- b) Invert the q outputs.**
- c) Invert the s-r inputs.**

Answer: option C

Explanation:-

When we use nand cross coupling in sr flip flop , the whole outputs are inverted . Therefore , s=1, r=1 gives q=0 , q'=0 . And hence high inputs are accepted .

17.When is a flip-flop said to be transparent?

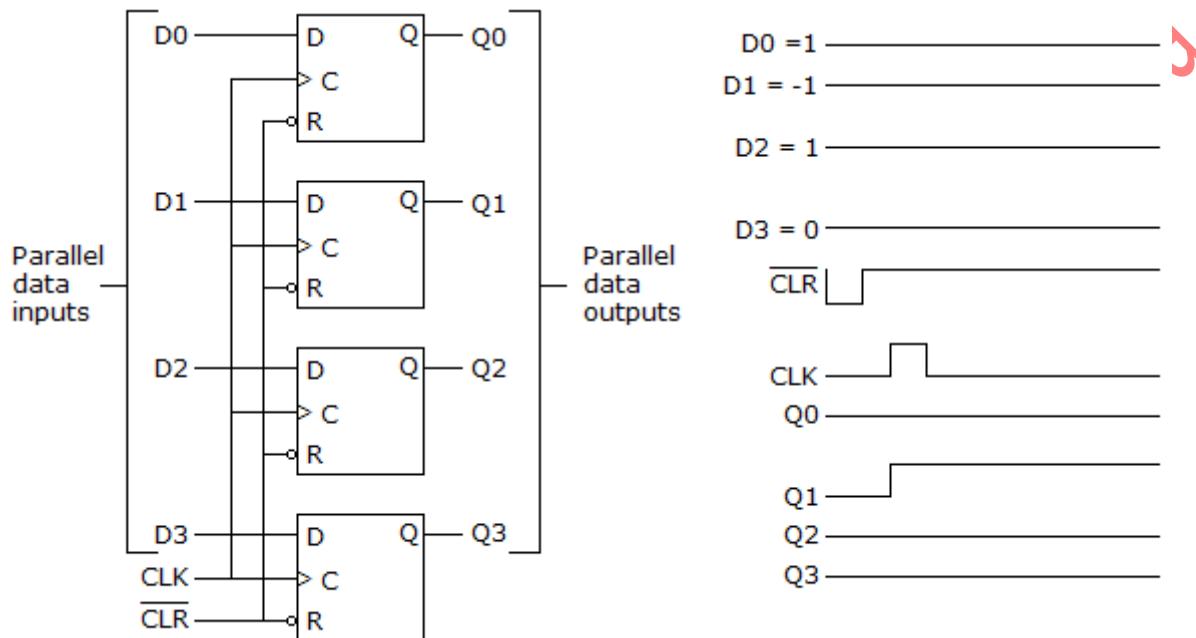
- a) When the q output is opposite the input**
- b) When the q output follows the input**
- c) When you can see through the ic packaging**

Answer: option B

Explanation:-

Responding to the input immediately is called transparency which has made flip-flops unique.

18. Four positive edge-triggered D flip-flops are used to store a 4-bit binary number as shown below. Determine if the circuit is functioning properly, and if not, what might be wrong.



- a) The circuit is functioning properly.
- b) Q2 is incorrect; the flip-flop is probably bad.
- c) The input to flip-flop 3 (d2) is probably wrong; check the source of d2.
- d) A bad connection probably exists between ff-3 and ff-4, causing ff-3 not to reset.

Answer: option B

Explanation:-

Option b is correct since, the output of the D ff follows the input i.e for $\text{clk}=1$ i/p $D=0$ o/p $Q=0$,
i/p $D=1$ o/p $Q=1$.

If you see the options, option b is incorrect because it's not following the i/p properly.

19. A 555 operating as a monostable multivibrator has an R_1 of $1 \text{ m}\Omega$. Determine C_1 for a pulse width of 2 s.

- a) $1.8 \mu\text{f}$
- b) 18 f
- c) 18 pf

d) 18 nf

Answer: option A

Explanation:-

From formula, $w = 1.1rc$.

Here $w = 2s$ $r = 1m$ ohms.

$$2 = 1.1 * 1 * 10^6 * c$$

$$c = 2 / (1.1 * 1 * 10^6) = 1.818 * 10^{-6}$$

$$= 1.8 \text{ micro farad}$$

20.Master-slave j-k flip-flops are called pulse-triggered or level-triggered devices because input data is read during the entire time the clock pulse is at a low level.

A)True

B)False

Answer: option B

Explanation:-

Master slave j-k f/f behave like negative edge triggered f/f because it's timing diagram same as that of m-s level triggered f/f.

Master slave is basically level triggered but their behavior resembles edge triggered. Hence called edge triggered flip flops.

21.Which of the following is correct for a d latch?

- a) The output toggles if one of the inputs is held high.**
- b) Q output follows the input d when the enable is high.**
- c) Only one of the inputs can be high at a time.**
- d) The output complement follows the input when enabled.**

Answer: option B

Explanation:-

If clock is high then the d flip flop operate and we know that input is equals to output in case d flip flop.

22.A j-k flip-flop is in a "no change" condition when _____.

- a) J = 1, k = 1**
- b) J = 1, k = 0**
- c) J = 0, k = 1**
- d) J = 0, k = 0**

Answer: option D

Explanation:-

In truth table $j=0, k=0$ mean no change.

23.A correct output is achieved from a master-slave j-k flip-flop only if its inputs are stable while the:

- a) Clock is low
- b) Slave is transferring
- c) Flip-flop is reset
- d) Clock is high

Answer: option D

Explanation:-

The clock is high only the flip flops are in stable when the inputs are stable.

24.Which of the following describes the operation of a positive edge-triggered d flip-flop?

- a) If both inputs are high, the output will toggle.
- b) The output will follow the input on the leading edge of the clock.
- c) When both inputs are low, an invalid state exists.
- d) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.

Answer: option B

Explanation:-

This condition is just 4 confusing us...the main phenomenon of d flip flop is the o/p will follow d i/p whn enable pin is high.

25.What does the triangle on the clock input of a j-k flip-flop mean?

- a) Level enabled
- b) Edge-triggered

Answer: option B

Explanation:-

Triangle on the clock input = edge triggered.

Direct line clock input = level triggered.

Circle on the line and circle before triangle shows the negative level and negative edge triggered.

26.A j-k flip-flop with j = 1 and k = 1 has a 20 khz clock input. The q output is _____.

- a) Constantly low
- b) Constantly high
- c) A 20 khz square wave
- d) A 10 khz square wave

Answer: option D

Explanation:-

- J=0 , k=0---> no change state.
- J=1 , k=0---> set condition means output = 1.
- J=0 , k=1---> reset condition means output = 0.
- J=1 , k=1 ---> toggle.

Or

O/p frequency = i/p freq / 2^n ; where n is the number of f/fs used.

Jk flip-flop has 2 flipflop s master and slave so according to that,
op freq = $20 / 2^1 ; 2^{(n-1)} < n > 2^n$.
= 10 hz.

27.The toggle condition in a master-slave j-k flip-flop means that q and \bar{Q} will switch to their _____ state(s) at the _____.

- a) Opposite, active clock edge
- b) Inverted, positive clock edge
- c) Quiescent, negative clock edge
- d) Reset, synchronous clock edge

Answer: option A

Explanation:-

Master slave j-k flip flop may be positive or negative edge triggered so active clock edge is suitable option.q and q bar will switch to their opposite state(inverted)so option a is correct

28.An rc circuit used in a nonretriggerable 74121 one-shot has an r_{ext} of 49 k Ω and a c_{ext} of 0.2 μF . The pulse width (t_w) is approximately _____.

- a) 6.9 μs
- b) 6.9 ms
- c) 69 ms
- d) 690 ms

Answer: option B

Explanation:-

Pulse width= $0.69rc$

substituting values of r&c in the above eqn we'll get 6.9 ms.

29.On a positive edge-triggered s-r flip-flop, the outputs reflect the input condition when _____.

- a) The clock pulse is low
- b) The clock pulse is high
- c) The clock pulse transitions from low to high
- d) The clock pulse transitions from high to low

Answer: option C

Explanation:-

Edge triggered device will follow when there is transition. And positive edge triggered when transition from low to high.

30.What is the hold condition of a flip-flop?

- a) Both s and r inputs activated
- b) No active s or r input
- c) Only s is active
- d) Only r is active

Answer: option B

Explanation:-

This one for active high, but for active low different inverse the answer above.

31.If an active-high s-r latch has a 0 on the s input and a 1 on the r input and then the r input goes to 0, the latch will be _____.

- a) Set
- b) Reset
- c) Clear
- d) Invalid

Answer: option B

Explanation:-

First at $s=0, r=1$ so flip flop is at reset condition.

Then at $s=0, r=0$ flip flop no change.

So it remains in reset.

32.In VHDL, how many inputs will a primitive jk flip-flop have?

- a) 2
- b) 3
- c) 4
- d) 5

Answer: option D

Explanation:-

VHDL is the hardware description language used in electronic design automation to describe digital and mixed-signal systems.

33.A 555 operating as a monostable multivibrator has a $C_1 = 0.01 \mu F$. Determine R_1 for a pulse width of 2 ms.

- a) $200 k\Omega$

- b) $182 \text{ k}\Omega$
- c) $91 \text{ k}\Omega$
- d) 182Ω

Answer: option B

Explanation:-

$$W=2\text{ms} \quad c=.01\text{uf}$$

$$\text{nw } w=1.1 \text{ rc}$$

$$\text{evaluating we get } r=181.8 \text{ kohm}$$

Note:-

Pulse width for astable multivibrator is $0.69rc$. For mono-stable it is $1.1rc$. Just see the circuit of both, it'll be clear that why there is change in formula.

34. A d flip-flop utilizing a pgt clock is in the clear state. Which of the following input actions will cause it to change states?

- a) Clk = ngt, d = 0
- b) Clk = pgt, d = 1
- c) Clock ngt, d = 1
- d) Clock pgt, d = 1
- e) Clk = ngt, d = 0, clock ngt, d = 1

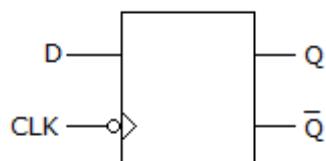
Answer: option D

Explanation:-

Pgt is positive going transition
and ngt is negative going transition.

Earlier dff is in clear state (output is 0)
so if d = 1 then in next stage output will be 1
and hence the stage will be changed.

35. The symbols on this flip-flop device indicate _____.



- a) Triggering takes place on the negative-going edge of the clk pulse
- b) Triggering takes place on the positive-going edge of the clk pulse
- c) Triggering can take place anytime during the high level of the clk waveform
- d) Triggering can take place anytime during the low level of the clk waveform

Answer: option A

Explanation:-

Triangle with bobble indicates negative triggering and if only triangle symbol present then it is positive triggering.

36.In a 555 timer, three 5 k Ω resistors provide a trigger level of _____.

- a) $1/4 V_{CC}$ and a threshold level $1/2 V_{CC}$
- b) $1/3 V_{CC}$ and a threshold level $3/4 V_{CC}$
- c) $1/3 V_{CC}$ and a threshold level $2/3 V_{CC}$
- d) $1/4 V_{CC}$ and a threshold level $2/3 V_{CC}$

Answer: option C

Explanation:-

The 555 timer ic is an amazingly simple yet versatile device. The ic is quiescent so long as the trigger input (pin 2) remains at +vcc.

The three resistors in the voltage divider all have the same value (5k in the bipolar).

This doesn't give us absolute values for "e" or "e," but it does give us the ratio $e/e = 2/3$. The 555 timer ic is an amazingly simple yet versatile device.

The ic is quiescent so long as the trigger input (pin 2) remains at +vcc.

The three resistors in the voltage divider all have the same value (5k in the bipolar).

This doesn't give us absolute values for "e" or "e," but it does give us the ratio $e/e = 2/3$.

37.Does the cross-coupled nor flip-flop have active-high or active-low set and reset inputs?

- a) Active-high
- b) Active-low

Answer: option A

Explanation:-

Cross-coupled nOR Gates means output of one nOR Gate is given as one of the input of the 2nd nOR Gate and vice versa.

Means here sr flip flop. They have active high set-reset.

The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the:

- Edge-detection circuit.
- Nor latch.
- Nand latch.
- Pulse-steering circuit.

8. With four j-k flip-flops wired as an asynchronous counter, the first output change of divider #4 indicates a count of how many input clock pulses?

- a) 16
- b) 8
- c) 4
- d) 2

Answer: option B

Explanation:-

So when 4th f/f has o/p 1 then count is 1000 and it counted 8 clock pulses.

39. What is the significance of the j and k terminals on the j-k flip-flop?

- a) There is no known significance in their designations.
- b) The j represents "jump," which is how the q output reacts whenever the clock goes high and the j input is also high.
- c) The letters were chosen in honor of jack kilby, the inventor of the integrated circuit.
- d) All of the other letters of the alphabet are already in use.

Answer: option C

40. Why are the s and r inputs of a gated flip-flop said to be synchronous?

- a) They must occur with the gate.
- b) They occur independent of the gate.

Answer: option A

41. Gated s-r flip-flops are called asynchronous because the output responds immediately to input changes.

- A) True
- B) False

Answer: option B

Explanation:-

Asynchronous means o/p depends on i/p.

Synchronous means o/p depends on clock pulse.

Sr ff are depends on clock pulse. So sr ff is synchronous.

42. Which of the following is not generally associated with flip-flops?

- a) Hold time
- b) Propagation delay time
- c) Interval time
- d) Set up time

Answer: option C

43.An rc circuit used in a 74122 retriggerable one-shot has an r_{ext} of 100 k Ω and a c_{ext} of 0.005 μF . The pulse width is _____.

- a) 70 μs
- b) 16 μs
- c) 160 μs
- d) 32 μs

Answer: option C

Explanation:-

As per data sheet of 74122, if $c_{ext} > 1000 \mu F$,
then, width of the pulse, $tw = k * c_{ext} * r_{ext} (1 + 0.7/r_{ext})$ $k = 0.32$.
Here $c_{ext} = 0.005 \mu F > 1000 \mu F$.
 $= 0.32 * 0.005 \mu F * 100 k (1 + 0.7/100 k) = 160 \mu s$.

44.A 555 operating as a monostable multivibrator has an r_1 of 220 k Ω . Determine c_1 for a pulse width of 4 ms.

- a) 0.017 μF
- b) 17 μF
- c) 170 μF
- d) 1,700 μF

Answer: option A

Explanation:-

Pulse width = $1.1rc$.
 $C = 4m/1.1 * 220k$.
0.017 micro.

45.What is one disadvantage of an s-r flip-flop?

- a) It has no enable input.
- b) It has an invalid state.
- c) It has no clock input.
- d) It has only a single output.

Answer: option B

Explanation:-

When both inputs of sr flip flops are high i.e. S = 1 and r = 1, the state in which ff goes is called as an invalid state.

46.To completely load and then unload an 8-bit register requires how many clock pulses?

- a) 2
- b) 4

- c) 8
- d) 16

Answer: option D

Explanation:-

It is clearly mentioned in the question that it is a 8 bit register. There is only one register which is of 8 bits. (it is not 8 registers of one bit each). So we need 8 clock signals to load it and 8 clock signals to unload it.

47.What is one disadvantage of an s-r flip-flop?

- a) It has no enable input.
- b) It has an invalid state.
- c) It has no clock input.
- d) It has only a single output.

Answer: option B

Explanation:-

When both $s=1$ and $r=1$ the occurrence of a clock pulse causes both outputs to go to 0 (zero) and when the pulse is removed the state of the flip-flop is indeterminate or invalid as shown in answer b.

48.Which of the following best describes the action of pulse-triggered ff's?

- a) The clock and the s-r inputs must be pulse shaped.
- b) The data is entered on the leading edge of the clock, and transferred out on the trailing edge of the clock
- c) A pulse on the clock transfers data from input to output.
- d) The synchronous inputs must be pulsed.

Answer: option B

49.An invalid condition in the operation of an active-high input s-r latch occurs when _____.

- a) Highs are applied simultaneously to both inputs s and r
- b) Lows are applied simultaneously to both inputs s and r
- c) A low is applied to the s input while a high is applied to the r input
- d) A high is applied to the s input while a low is applied to the r input

Answer: option A

50.On a j-k flip-flop, when is the flip-flop in a hold condition?

- a) $J = 0, k = 0$
- b) $J = 1, k = 0$
- c) $J = 0, k = 1$

d) $J = 1, k = 1$

Answer: option A

Explanation:-

$J=0$ $k=0$ output continues to be in same state.

51. The output pulse width for a 555 monostable circuit with $r_1 = 3.3$ k Ω and $C_1 = 0.02 \mu F$ is _____.

- a) 7.3 μs
- b) 73 μs
- c) 7.3 ms
- d) 73 ms

Answer: option B

Explanation:-

As it is mono-stable so use the formula: pulse width = $1.1 * r * C$.

52. Edge-triggered flip-flops must have:

- a) Very fast response times.
- b) At least two inputs to handle rising and falling edges.
- c) A pulse transition detector.
- d) Active-low inputs and complemented outputs.

Answer: option C

53. As a general rule for stable flip-flop triggering, the clock pulse rise and fall times must be:

- a) Very long.
- b) Very short.
- c) At a maximum value to enable the input control signals to stabilize. of no consequence as long as the levels are within the determinate range of value.

Answer: option B

Explanation:-

As there is a term of "propagation delay" related to flip flop which affects on the output of flip-flop, and if this rising and falling time is less. There is some possibilities of decreasing the propagation delay. That's why i think short time must be the correct answer.

54. A positive edge-triggered D flip-flop will store a 1 when

- a) The D input is high and the clock transitions from high to low
- b) The D input is high and the clock transitions from low to high

- c) The d input is high and the clock is low
- d) The d input is high and the clock is high

Answer: option B

55. If an input is activated by a signal transition, it is _____.

- a) Edge-triggered
- b) Toggle triggered
- c) Clock triggered
- d) Noise triggered

Answer: option A

56. A positive edge-triggered j-k flip-flop is used to produce a two-phase clock. However, when the circuit is operated it produces erratic results. Close examination with a scope reveals the presence of glitches. What causes the glitches, and how might the problem be corrected?

- a) The preset and clear terminals may have been left floating; they should be properly terminated if not being used.
- b) The problem is caused by a race condition between the j and k inputs; an inverter should be inserted in one of the terminals to correct the problem.
- c) A race condition exists between the q and q outputs to the AND Gate; the AND Gate should be replaced with a nAND Gate.
- d) A race condition exists between the clock and the outputs of the flip-flop feeding the AND Gate; replace the flip-flop with a negative edge-triggered j-k flip-flop.

Answer: option D

Explanation:-

Answer should be a according to me because preset and clear terminals are the reason of synchronization and hence they produces glitches if they are not being used then they must be terminated.

57. A 555 operating as a monostable multivibrator has a $C_1 = 100 \text{ pF}$. Determine r_1 for a pulse width of 500 ms.

- a) 45Ω
- b) 45Ω
- c) 455Ω
- d) $4.5 \text{ k}\Omega$
- e) $455 \text{ k}\Omega$

Answer: option C

Explanation:-

Explanation:-

Pulse width(w) = $1.1 \cdot r \cdot C$
given that $w = 500 \cdot 10^{-3}$
 $C = 100 \cdot 10^{-3}$
from formula $r = 4.5k$

58. Asynchronous inputs will cause the flip-flop to respond immediately with regard to the clock input.

- A) True
- B) False

Answer: option B

Explanation:-

The question is when the input is asynchronous that is when the input is taken from previous flip-flop output it will respond immediately with regard to the clock input. The answer is false because. Clk pulse will be needed when synchronous operation is needed.

59. Which is not a real advantage of HDL?

- a) Using higher levels of abstraction
- b) Tailoring components to exactly fit the needs of the project
- c) The use of graphical tools
- d) Using higher levels of abstraction and tailoring components to exactly fit the needs of the project

Answer: option C

60. Two j-k flip-flops with their j-k inputs tied high are cascaded to be used as counters. After four input clock pulses, the binary count is _____.

- a) 00
- b) 11
- c) 01
- d) 10

Answer: option A

Explanation:-

- a) Every o/p repeats after its mod here mod is 4 so after 4 clk pulses the o/p repeats i.e. 00.

61. Latches constructed with nor and nAND Gates tend to remain in the latched condition due to which configuration feature?

- a) Cross coupling
- b) Gate impedance
- c) Low input voltages
- d) Asynchronous operation

Answer: option A

62.In VHDL, how is each instance of a component addressed?

- a) A name followed by a colon and the name of the library primitive
- b) A name followed by a semicolon and the component type
- c) A name followed by the library being used
- d) A name followed by the component library number

Answer: option A

63.The output of a gated s-r flip-flop changes only if the:

- a) Flip-flop is set
- b) Control input data has changed
- c) Flip-flop is reset
- d) Input data has no change

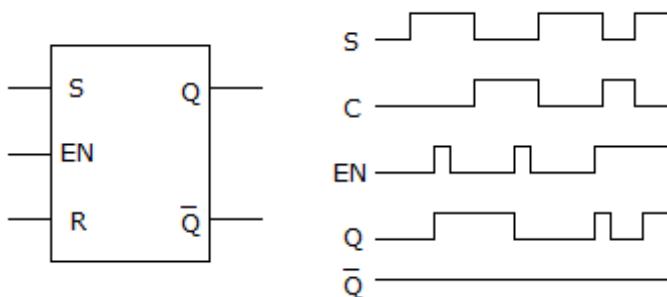
Answer: option B

64.In VHDL, in which declaration section is a component declared?

- a) Architecture
- b) Library
- c) Entity
- d) Port map

Answer: option A

65.A gated s-r latch and its associated waveforms are shown below. What, if anything, is wrong and what could be causing the problem?



- a) The \bar{Q} output is always low; the circuit is defective.
- b) The q output should be the complement of the \bar{Q} output; the s and r terminals are reversed.
- c) The q should be following the r input; the r input is defective.
- d) There is nothing wrong with the circuit.

Answer: option A

66.The output pulse width of a 555 monostable circuit with $r_1 = 4.7 \text{ k}\Omega$ and $c_1 = 47 \text{ }\mu\text{f}$ is _____.

- a) 24 s
- b) 24 ms
- c) 243 ms
- d) 243 μ s

Answer: option C

Explanation:-

$$T = 1.1rc = 242.99\text{ms}$$

67. If both inputs of an s-r flip-flop are low, what will happen when the clock goes high?

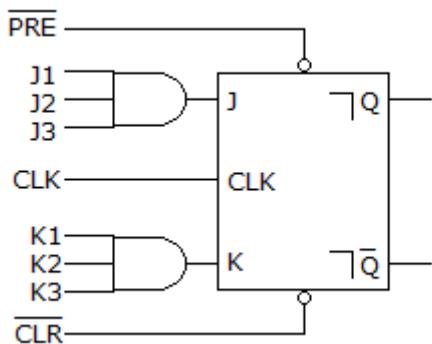
- a) An invalid state will exist.
- b) No change will occur in the output.
- c) The output will toggle.
- d) The output will reset.

Answer: option B

Explanation:-

Because $s=0$ $r=0$ is a memory state.

68. The circuit given below fails to function; the inputs are checked with a logic probe and the following indications are obtained: clk, j1, j2, j3, k1, k2, and k3 are pulsing. Q and \overline{Q} are high. \overline{Q} and pre are low. What could be causing the problem?



- a) There is no problem.
- b) The clock should be held high.
- c) The pre is stuck low.
- d) The clr is stuck high.

Answer: option C

Explanation:-

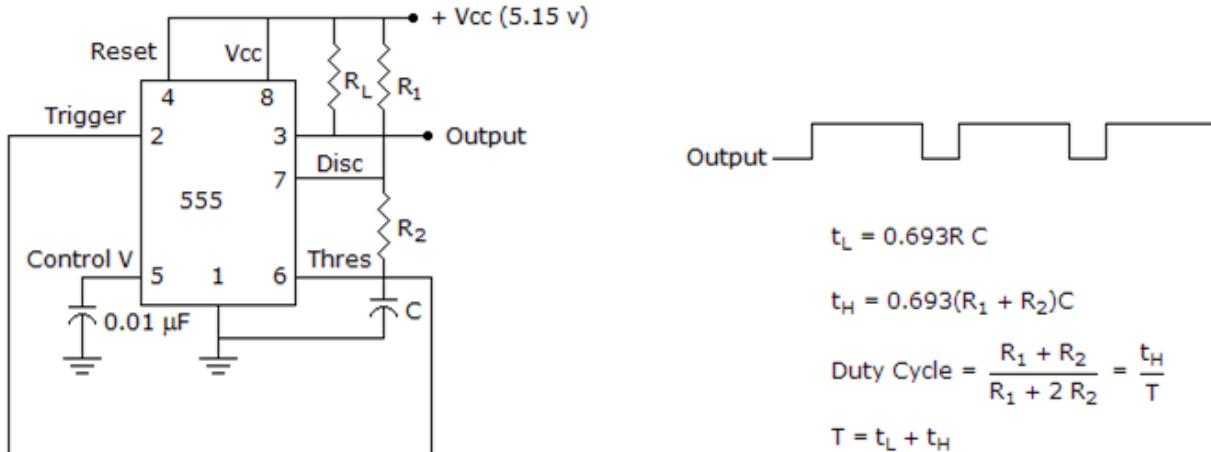
If preset pin pin is low or high according to the logic used (here it is negative logic so low) then it sets the output (i.e. Q=1) in advance whether the clock is applied or not.

69.A push-button switch is used to input data to a register. The output of the register is erratic. What could be causing the problem?

- a) The power supply is probably noisy.
- b) The switch contacts are bouncing.
- c) The socket contacts on the register ic are corroded.
- d) The register ic is intermittent and failure is imminent.

Answer: option B

70.A 555 timer is connected for astable operation as shown below along with the output waveform. It is determined that the duty cycle should be 0.5. What steps need to be taken to correct the duty cycle, while maintaining the same output frequency?



- a) Increase the value of C.
- b) Increase V_{cc} and decrease R_1 .
- c) Decrease R_1 and R_2 .
- d) Decrease R_1 and increase R_2 .

Answer: option D

Explanation:-

Correct me if i'm wrong, but i think decreasing r_1 and increasing r_2 will change the output frequency.

71.The pulse width of a one-shot circuit is determined by _____.

- a) A resistor and capacitor
- b) Two resistors
- c) Two capacitors
- d) None of the above

Answer: option A

Explanation:-

$W=1.1rc$ so one cap and one resistor

72. For an s-r flip-flop to be set or reset, the respective input must be:

- a) Installed with steering diodes
- b) In parallel with a limiting resistor
- c) Low
- d) high

Answer: option D

73. An active-high input s-r latch has a 1 on the s input and a 0 on the r input. What state is the latch in?

- a) $Q = 1, \bar{Q} = 0$
- b) $Q = 1, \bar{Q} = 1$
- c) $Q = ?, \bar{Q} = 1$
- d) $Q = ?, \bar{Q} = 0$

Answer: option A

74. If both inputs of an s-r flip-flop are low, what will happen when the clock goes high?

- a) No change will occur in the output.
- b) An invalid state will exist.
- c) The output will toggle.
- d) The output will reset.

Answer: option A

75. Four j-k flip-flops are cascaded with their j-k inputs tied high. If the input frequency (f_{in}) to the first flip-flop is 32 khz, the output frequency (f_{out}) is _____.

- a) 1 khz
- b) 2 khz
- c) 4 khz
- d) 16 khz

Answer: option B

Explanation:-

$32/2=16$:-first flip-flop

$16/2=8$:- second flip-flop

$8/2=4$:- third flip-flop

$4/2=2$:- fourth flip-flop

O.p. Frequency = i.p. frequency / (2^n) where n is number of flipflops

TRUE/FALSE

1.A gated s-r flip-flop goes into the set condition when s is high, r is low, and en is high.

A)True

B)False

Answer: option A

2.VHDL does require a special designation for an output with a feedback.

A)True

B)False

Answer: option A

3.A negative edge-triggered flip-flop will accept inputs only when the clock is low.

A)True

B)False

Answer: option B

4.The term clear always means that $Q = 0, \bar{Q} = 1$.

A)True

B)False

Answer: option A

5.Preset and clear inputs are normally synchronous.

A)True

B)False

Answer: option B

6.VHDL was created as a very flexible language and it allows us to define the operation of clocked devices in the code without relying on logic primitives.

A)True

B)False

Answer: option A

7.The q output of a flip-flop is normally high when the device is in the "clear" or "reset" state.

A)True

B)False

Answer: option B

8.An astable multivibrator is sometimes referred to as a clock.

A)True

B)False

Answer: option A

9.The 7476 and 74ls76 are both dual flip-flops.

A)True

B)False

Answer: option A

10.The 7475 is an example of an ic d latch (also called a bistable latch) that contains four transparent d latches.

A)True

B)False

Answer: option A

11In VHDL, each instance of a component is given a name followed by a semicolon and the name of the library primitive.

A)True

B)False

Answer: option B

12.The 555 timer can be used in either the astable or monostable modes.

A)True

B)False

Answer: option A

13.Ics can perform sequential operations, including counting and data shifting.

A)True

B)False

Answer: option A

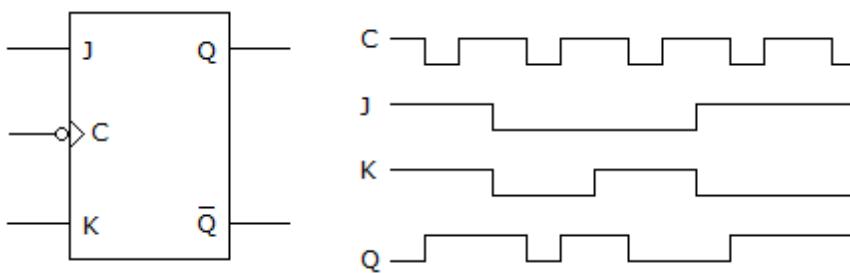
14.An input which can only be accepted when an enable or trigger is present is called asynchronous.

A)True

B)False

Answer: option B

15.A j-k flip-flop and associated waveforms are shown below. The circuit is operating properly.



A)True

B)False

Answer: option B

16.All multivibrators require feedback.

A)True

B)False

Answer: option A

17.The propagation delay time t_{ph} is measured from the triggering edge of the clock pulse to the low-to-high transition of the output.

A)True

B)False

Answer: option A

18.The j-k flip-flop is a standard building block of clocked (sequential) logic circuits known as logic standard primitives.

A)True

B)False

Answer: option B

19.A latch can act as a contact-bounce eliminator.

A)True

B)False

Answer: option A

20.Connecting components together using HDL is not difficult.

A)True

B)False

Answer: option A

21.A flip-flop's normal starting state when power is first applied to a circuit is always the set state.

A)True

B)False

Answer: option B

22.Latches are tristate devices whose state normally depends on asynchronous inputs.

- A)True
- B)False

Answer: option B

23.Using knowledge from previous chapters, an s-r flip-flop circuit is easy to design.

- A)True
- B)False

Answer: option A

24.Inputs that cause the output of a flip-flop to change instantaneously are asynchronous.

- A)True
- B)False

Answer: option A

25.A one-shot is a special type of multivibrator that must be triggered to produce each output pulse.

- A)True
- B)False

Answer: option A

26.Generally, a flip-flop's hold time is short enough so that its output will go to a state determined by the logic levels present at its synchronous control inputs just prior to the active clock transition.

- A)True
- B)False

Answer: option A

27.The j-k flip-flop eliminates the invalid state by toggling when both inputs are high and the clock transitions.

- A)True
- B)False

Answer: option A

28.A d-type latch is able to change states and "follow" the d input regardless of the level of the enable input.

- A)True
- B)False

Answer: option B

29.A positive edge-triggered flip-flop changes states with a high-to-low transition on the clock input.

- A)True**
B)False

Answer: option B

30. When using edge-triggered flip-flops, the data is entered into the flip-flop on the leading edge of the clock, but the output does not change until the trailing edge of the clock.

- A)True**
B)False

Answer: option B

31. A d latch has one data-input line.

- A)True**
B)False

Answer: option A

32. The 7474 has two distinct types of inputs: synchronous and asynchronous.

- A)True**
B)False

Answer: option A

33. Most basic latches and flip-flops are available in ic packages of eight latches or flip-flops with a common clock.

- A)True**
B)False

Answer: option A

34. Edge-triggered flip-flops can be identified by the triangle on the clock input.

- A)True**
B)False

Answer: option A

35. Parallel data transfers between two different sets of registers require more than one shift pulse.

- A)True**
B)False

Answer: option B

36. A toggle input to a j-k flip-flop causes the q and \bar{Q} outputs to switch to their opposite state.

- A)True**
B)False

Answer: option A

37. When the output of the nOR Gate s-r flip-flop is $Q = 1$ and $\bar{Q} = 0$, the inputs are $S = 1, R = 1$.

- A)True
- B)False

Answer: option B

38. Edge-triggered j-k flip-flops make it hard for design engineers to know when to accept input data.

- A)True
- B)False

Answer: option B

39. A one-shot circuit is also known as a timer.

- A)True
- B)False

Answer: option B

Explanation:-

555 timer or mono stable multi vibrator or 1-shot they are all same.
So a 1-shot circuit is also a timer.

40. The s-r flip-flop has no invalid or unused state.

- A)True
- B)False

Answer: option B

41. Pulse-triggered flip-flops are identified by a bubble on the q output terminal.

- A)True
- B)False

Answer: option B

42. Some flip-flops have invalid states.

- A)True
- B)False

Answer: option A

43. Multivibrators must be level-triggered.

- A)True
- B)False

Answer: option B

44. Simple gate circuits, combinational logic, and transparent s-r flip-flops are synchronous.

- A) True
- B) False

Answer: option B

45. A flip-flop is in the clear condition when $Q = 1, \bar{Q} = 1$

- A) True
- B) False

Answer: option B

46. Pulse-triggered or level-triggered devices are the same.

- A) True
- B) False

Answer: option A

47. A d flip-flop is constructed by connecting an inverter between the set and clock terminals.

- A) True
- B) False

Answer: option B

48. It takes four flip-flops to act as a divide-by-4 frequency divider.

- A) True
- B) False

Answer: option B

49. The gated s-r flip-flop is asynchronous.

- A) True
- B) False

Answer: option B

FILL UP THE BLANKS

1. The asynchronous inputs are normally labeled _____ and _____, and are normally active-_____ inputs.

- a) Pre, clr, low
- b) On, off, high
- c) Start, stop, low
- d) Set, reset, high

Answer: option A

2. Assume a j-k flip-flop has 1s on the j and k inputs. The next clock pulse will cause the output to _____.

- a) Set
- b) Reset
- c) Latch
- d) Toggle

Answer: option D

3. In synchronous systems, the exact times at which any output can change state are determined by a signal commonly called the _____.

- a) Traffic
- b) D
- c) Flip-flop
- d) Clock

Answer: option D

4. The key to edge-triggered sequential circuits in VHDL is the _____.

- a) Architecture
- b) Process
- c) Function
- d) Variable

Answer: option B

5. Assume an \bar{S} - \bar{R} latch, made from cross-coupled nAND Gates, has a 0 on both inputs. The outputs will be _____.

- a) $Q = 0, \bar{Q} = 0$
- b) $Q = 0, \bar{Q} = 1$
- c) $Q = 1, \bar{Q} = 0$
- d) $Q = 1, \bar{Q} = 1$

Answer: option D

Explanation:-

S(bar) r(bar) q q(bar)
0 0 1* 1*
0 1 0 1
1 0 1 0
1 1 q ~q

6. The j-k flip-flop is a standard building block of clocked (sequential) logic circuits known as a _____.

- a) Function
- b) Logic primitive
- c) Variable
- d) Process

Answer: option B

7.A gated d latch does not have _____.

- a) A clock input
- b) An enable input
- c) A Output
- d) Steering gates

Answer: option A

8.Setup time specifies _____.

- a) The minimum time for the control levels to be maintained on the inputs prior to the triggering edge of the clock in order for data to be reliably clocked into the ff
- b) The maximum time interval required for the control levels to remain on the inputs before the triggering edge of the clock in order for the data to be reliably clocked out of the ff
- c) How long the operator has in order to get the flip-flop running before the maximum power level is exceeded
- d) How long it takes the output to change states after the clock has transitioned

Answer: option A

9.When the output of the nOR Gate s-r flip-flop is $q = 0$ and $\bar{Q} = 1$, the inputs are:

- a) S = 1, r = 1
- b) S = 1, r = 0
- c) S = 0, r = 1
- d) S = 0, r = 0

Answer: option C

10.A retriggerable one-shot has a pulse width of 10 ms; 3 ms after being triggered, another trigger pulse is applied. The resulting output pulse will be _____ ms.

- a) 3
- b) 7
- c) 10
- d) 13

Answer: option D

11.Most people would prefer to use _____ over HDL.

- a) Graphic descriptions
- b) Functions
- c) VHDL
- d) AHDL

Answer: option A

12.A major drawback to an \bar{S} - \bar{R} latch is its _____.

- a) Complexity
- b) Slow speed
- c) Invalid condition
- d) Latch mode

Answer: option C

13.In VHDL, each instance of a component is given a name followed by a _____ and the name of the library primitive.

- a) Function
- b) Signal
- c) Semicolon
- d) Colon

Answer: option D

Explanation:-

Discussion on VHDL codes and primitives will be great. Thanks

14.The duty cycle of a 555 timer configured as a basic astable multivibrator is controlled by _____.

- a) One register
- b) Two register
- c) One capacitor
- d) A resistor and a capacitor

Answer: option D

Explanation:-

Doubt as the formula for the duty cycle is $r1/(r1+r2)*100$.

15.The major advantage of a schmitt trigger input is that it _____.

- a) Avoids erratic triggering
- b) Has more triggering methods
- c) Has a wider range of outputs
- d) Can be retriggered

Answer: option A

16.When the output of the nOR Gate s-r flip-flop is in the hold state (no change), the inputs are _____.

- a) S = 1, r = 1
- b) S = 1, r = 0
- c) S = 0, r = 1

d) $S = 0, r = 0$

Answer: option D

Explanation:-

For a sr flip-flop truth table.

S r output

0 0 q

0 1 0

1 0 1

1 1 q'

17. Regardless of whether you develop a description in aHDL or VHDL, the circuit's proper operation can be verified using a _____.

- a) Process**
- b) Computer**
- c) Simulator**
- d) Primitive library**

Answer: option C

18. The 74121 nonretriggerable multivibrator can have the output pulse set by a single external component. This component is a(n) _____.

- a) Capacitor**
- b) Inductor**
- c) Resistor**
- d) Led**

Answer: option A

19. The signal used to identify edge-triggered flip-flops is _____.

- a) A bubble on the clock input**
- b) An inverted "I" on the output**
- c) The letter "e" on the enable input**
- d) A triangle on the clock input**

Answer: option D

20. An edge-triggered flip-flop can change states only when _____.

- a) The trigger is high**
- b) The d input is high**
- c) The trigger is low**
- d) The trigger input changes levels**

Answer: option D

21. When both inputs of a j-k pulse-triggered ff are high and the clock cycles, the output will _____.

- a) Be invalid
- b) Not change
- c) Remain unchanged
- d) Toggle

Answer: option D

22. The term hold always means _____.

- a) $Q = 0, \bar{Q} = 1$
- b) $Q = 1, \bar{Q} = 0$
- c) $Q = 0, \bar{Q} = 0$
- d) No change

Answer: option D

23. A gated s-r flip-flop goes into the clear condition when _____.

- a) S is high; r is low; en is high
- b) S is low; r is high; en is high
- c) S is low; r is high; en is low
- d) S is high; r is low; en is low

Answer: option B

24. What type of multivibrator is a latch?

- a) Astable
- b) Monostable
- c) Bistable
- d) It depends on the type of latch.

Answer: option C

25. If an input is activated by a signal transition, it is _____.

- a) Hair-triggered
- b) Line-triggered
- c) Pulse-triggered
- d) Edge-triggered

Answer: option D

26. An astable multivibrator is a circuit that _____.

- a) Has two stable states
- b) Is free-running
- c) Produces a continuous output signal
- d) Is free-running and produces a continuous output signal

Answer: option C

27.The inputs on a 7474 d flip-flop are s, r, d, and clk _____ is/are synchronous.

- a) Only s
- b) S and r
- c) Only d
- d) All the above

Answer: option D

28.A flip-flop operation is described as a toggle when the result after a clock is _____.

- a) $Q = 1, \bar{Q} = 1$
- b) $Q = 1$
- c) $Q = 0, \bar{Q} = 1$
- d) Q and \bar{Q} change to opposite states

Answer: option D

29.The asynchronous inputs on a j-k flip-flop _____.

- a) Are normally not at the active level at the same time
- b) Take precedence over the j and k inputs
- c) Do not require a clock pulse to affect the output
- d) All of the above

Answer: option D

30.A positive edge-triggered flip-flop will accept inputs only when the clock _____.

- a) Is low
- b) Changes from high to low
- c) Is high
- d) Changes from low to high

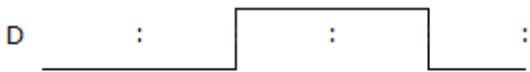
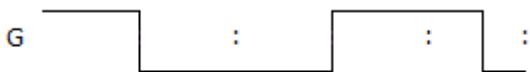
Answer: option D

31.If data is brought into the j terminal and its complement to the k terminal, a j-k flip-flop operates as a(n) _____.

- a) S-r flip-flop
- b) D flip-flop
- c) Gated s-c flip-flop
- d) Toggle flip-flop

Answer: option B

32.The point(s) on this timing diagram where the q output of a d latch will be high is/are _____.



Q 1 : 2 : 3 : 4 : 5 :

- a) Point 4
- b) Points 3 and 4
- c) Points 1 and 2
- d) Points 4 and 5

Answer: option A

Explanation:-

D is edge triggered. So only at the positive edge of the clock o/p changes.

33. The action of _____ a ff or latch is also called resetting.

- a) Breaking
- b) Clearing
- c) Freeing
- d) Changing

Answer: option B

34. The postponed symbol (\neg) on the output of a flip-flop identifies it as being _____.

- a) A d flip-flop
- b) A j-k flip-flop
- c) Pulse triggered
- d) Trailing edge-triggered

Answer: option C

35. The advantage of a j-k flip-flop over an s-r ff is that _____.

- a) It has fewer gates
- b) It has only one output
- c) It has no invalid states
- d) It does not require a clock input

Answer: option C

36. The _____ is the time interval immediately following the active transition of the clock signal.

- a) Hold time
- b) Setup time

- c) Over-time
- d) Hang-time

Answer: option A

37.A gated s-r flip-flop is in the hold condition whenever _____.

- a) The gate enable is high
- b) The gate enable is low
- c) The s and r inputs are both low
- d) The gate enable is high and the s and r inputs are both low

Answer: option D

38.The toggle mode is the mode in which a(n) _____ changes states for each clock pulse.

- a) Logic level
- b) Flip-flop
- c) Edge-detector circuit
- d) Toggle detector

Answer: option B

11.DIGITAL ARITHMETIC OPERATIONS AND CIRCUITS

1. For a 4-bit parallel adder, if the carry-in is connected to a logical high, the result is:

- a) The same as if the carry-in is tied low since the least significant carry-in is ignored.
- b) That carry-out will always be high.
- c) A one will be added to the final result.
- d) The carry-out is ignored.

Answer: option C

2. What is the first thing you will need if you are going to use a macrofunction?

- a) A complicated design project
- b) An experienced design engineer
- c) Good documentation
- d) Experience in HDL

Answer: option C

3. Perform subtraction on each of the following binary numbers by taking the two's-complement of the number being subtracted and then adding it to the first number. 01001 01100

00011 00111

- a) 01100 10011
- b) 00110 00101
- c) 10110 10101
- d) 00111 00100

Answer: option B

Explanation:-

Given:

1) 011001.00011->2's complement =11101. Add with 011001 we will get 00110.

2) 01100.

00111->2's complement =11001. Add with 01100 we will get 00101.
So answer is b 00110 00101.

Or

When we are subtracting any binary no using 2's compliment attention on it.
Take binary no, which we want to subtract.

Ex. A-b = (110011)-(011011).

Take $b = 011011$.

Find out 2's compliment of b .

First find 1's compliment as convert it as '1' becomes 0 and '0' becomes 1.

1's compliment is $b = 100100$.

Add 1 on LSB with 1's compliment.

2's compliment is $b' = 100100 + 1$.

$B' = 100101$.

Then $a+b' = 110011 + 100101$.

= 011000 this is our answer.

4. Solving $-11 + (-2)$ will yield which two's-complement answer?

- a) 1110 1101
- b) 1111 1001
- c) 1111 0011
- d) 1110 1001

Answer: option C

Explanation:-

-11 written in 2's complement

-11=0101 2's complement

& similar value of -2=1110 2's complement

then $-11 + (-2)$

$0101 + 1110 = 1\ 0011$

msd 1 represent negative sign

5. Multiply the following binary numbers.

- | | | |
|----------------------------------|-------|-------|
| 1010 | 1011 | 1001 |
| X0011 | x0111 | x1010 |
| a) 0001 1110 0100 1101 0101 1011 | | |
| b) 0001 1110 0100 1100 0101 1010 | | |
| c) 0001 1110 0100 1101 0101 1010 | | |
| d) 0001 1101 0100 1101 0101 1010 | | |

Answer: option C

Explanation:-

$1010 * 00011 = 10 * 3 = 30 = 0001\ 1110$

$1011 * 0111 = 11 * 7 = 77 = 0100\ 1101$

$1001 * 1010 = 9 * 10 = 90 = 0101\ 1010$

so ans is c

= 0001 1110 0100 1101 0101 1010

6. Add the following BCD numbers.

- | | | |
|------|------|------|
| 0110 | 0111 | 1001 |
| 0101 | 1000 | 1000 |

- a) 0000 1011 0000 1111 0001 0001
- b) 0001 0001 0001 0101 0001 0001
- c) 0000 1011 0000 1111 0001 0111
- d) 0001 0001 0001 0101 0001 0111

Answer: option D

7. Add the following hexadecimal numbers.

$$\begin{array}{r}
 3c & 14 & 3b \\
 +25 & +18 & +dc \\
 \hline
 \end{array}$$

- a) 60 3c 116
- b) 62 3c 118
- c) 61 3c 117
- d) 61 3d 117

Answer: option C

Explanation:-

Value of c=1100, d=1101, b=1011

in binary addition

$$\begin{array}{r}
 0011\ 1100 & 0001\ 0101 & 0011\ 1011 \\
 0010\ 0101 & 0010\ 1000 & 1101\ 1100 \\
 =0110\ 0001 & =0011\ 1101 & =0001\ 0001\ 0111 \\
 61 & 3c & 117
 \end{array}$$

8. Solve this BCD problem: 0100 + 0110 =

- a) 00010000_{BCD}
- b) 00010111_{BCD}
- c) 00001011_{BCD}
- d) 00010011_{BCD}

Answer: option A

Explanation:-

0100+0110=1010 in BCD addition (greater than 9 add 0110)

1010+0110=0001 0000

9. What are constants in VHDL code?

- a) Fixed numbers represented by a name
- b) Fixed variables used in functions
- c) Fixed number types
- d) Constants do not exist in VHDL code.

Answer: option A

10. The 2's-complement system is to be used to add the signed binary numbers 11110010 and 11110011. Determine, in decimal, the sign and value of each number and their sum.

- a) -113 and -114, -227**
- b) -14 and -13, -27**
- c) -11 and -16, -27**
- d) -27 and -13, -40**

Answer: option B

Explanation:-

When we complement 11110010 for 1's complement, we get 00001101.

Then add 1 in 1's complement to get 2's complement.

$$00001101 + 1 = 00001110.$$

The decimal of 00001110 is 14. And the sign of the number is "-" because in 11110010, the starting number is "1". So, the number is -14.

Similarly the 2's complement of 2nd number is 00001101, and we get 13 as decimal value. The sign of the number is again negative as we can see "1" as MSB, so the number in decimal is -13.

When we add the 2's complement of both numbers, we get 27 as total decimal value and the sign is negative, because both the numbers were negative.

11. The most commonly used system for representing signed binary numbers is the:

- a) 2's-complement system.**
- b) 1's-complement system.**
- c) 10's-complement system.**
- d) Sign-magnitude system.**

Answer: option A

12. What is the major difference between half-adders and full-adders?

- a) Nothing basically; full-adders are made up of two half-adders.**
- b) Full adders can handle double-digit numbers.**
- c) Full adders have a carry input capability.**
- d) Half adders can handle only single-digit numbers.**

Answer: option C

Explanation:-

half adders have only two inputs a and b. When we add two 4 bit binary number like 0001 and 0011, then half adder can not be used because if the first bit of both the numbers is 1, then the sum would be 0 and carry would be 1. But this carry can not be added with the second bits addition of the number. So, half adders are useless. But in full adders, one more carry input is present, so that, if carry of one stage is present, it can be added with the next stage as it is done in normal addition. So, therefore, full adders have a carry input capability.

13.The decimal value for e_{16} is:

- a) 12_{10}
- b) 13_{10}
- c) 14_{10}
- d) 15_{10}

Answer: option C

Explanation:-

Decimal value for a = 10.

B = 11.

C = 12.

D = 13.

E = 14.

So option c is correct.

14.Fast-look-ahead carry circuits found in most 4-bit full-adder circuits:

- a) Determine sign and magnitude
- b) Reduce propagation delay
- c) Add a 1 to complemented inputs
- d) Increase ripple delay

Answer: option B

15.Add the following hex numbers: $0110_{16} + 10010_{16}$

- a) 10120_{16}
- b) 10020_{16}
- c) 11120_{16}
- d) 00120_{16}

Answer: option A

Explanation:-

As it is hex addition the addition value will range from 0-9 and a-f.

16.The binary subtraction $0 - 0 =$

- a) Difference = 0;borrow = 0
- b) Difference = 1;borrow = 0
- c) Difference = 1;borrow = 1
- d) Difference = 0;borrow = 1

Answer: option A

17.Convert each of the decimal numbers to 8-bit two's-complement form and then perform subtraction by taking the two's-complement and adding.

18

- 4

- a) 0001 0011
- b) 0000 1110
- c) 0010 1110
- d) 1110 0000

Answer: option B

Explanation:-

The given answer is right because convert 18 and 4 in 8 bit that means 18 = 0001 0010.

4 = 0000 0100.

Now convert 4 into 2's complement i.e 1111 1011.

+ 1.

1111 1100.

Now add this by 18.

0001 0010.

+1111 1100.

1 0000 1110.

Neglect carry hence we got the answer.

18-4 = 14 and its (1110) decimal is 14.

15. Adding in binary, a decimal 26 + 27 will produce a sum of:

- a) 111010
- b) 110110
- c) 110101
- d) 101011

Answer: option C

Explanation:-

(26)+(27)=53 this value is in decimal.

Convert them in binary:

53/2=26 1

26/2=13 0

13/2=6 1

6/2=3 0

3/2=1 1

1,

move from down to up,

we get, 110101.

11010 26's binary conversion.

+11011 27's binary conversion.

(110101) = 53 so the addition is 53. Answer is c.

26+27 = 53.

Binary conversion of 53 is 110101.

Answer is c.

16. Convert each of the following signed binary numbers (two's-complement) to a signed decimal number.

00000101 11111100 11111000

- a) -5 +4 +8
- b) +5 -4 -8
- c) -5 +252 +248
- d) +5 -252 -248

Answer: option B

Explanation:-

00000101 positive MSB (0) so +5.

Rest two binary numbers are negative because MSB is high. So take 2's complement and convert in decimal with negative sign.

17. How many basic binary subtraction operations are possible?

- a) 4
- b) 3
- c) 2
- d) 1

Answer: option A

Explanation:-

0-0=0.

0-1=1 borrow=1.

1-0=1.

1-1=0.

18. If [a] = 1011 1010, [b] = 0011 0110, and [c] = [a] • [b], what is [c 4..2] in decimal?

- a) 1
- b) 2
- c) 3
- d) 4

Answer: option D

Explanation:-

$[c]=[a].[b]=00110010$ (bit by bit multiplication-zeroth bit with zeroth bit,first bit with first bit and so on)
values at bit positions 4,3,2 are 1,0,0 respectively.
 $100=4$ in decimal

19.Using 4-bit adders to create a 1sec section 6-bit adder:

- a) Requires 16 adders.
- b) Requires 4 adders.
- c) Requires the carry-out of the less significant adder to be connected to the carry-in of the next significant adder.
- d) Requires 4 adders and the connection of the carry out of the less significant adder to the carry-in of the next significant adder.

Answer: option D

20.When performing subtraction by addition in the 2's-complement system:

- a) The minuend and the subtrahend are both changed to the 2's-complement.
- b) The minuend is changed to 2's-complement and the subtrahend is left in its original form.
- c) The minuend is left in its original form and the subtrahend is changed to its 2's-complement.
- d) The minuend and subtrahend are both left in their original form.

Answer: option C

21.The two's-complement system is to be used to add the signed numbers 11110010 and 11110011. Determine, in decimal, the sign and value of each number and their sum.

- a) -14 and -13, -27
- b) -113 and -114, 227
- c) -27 and -13, 40
- d) -11 and -16, -27

Answer: option A

22.When 1100010 is divided by 0101, what is the decimal remainder?

- a) 2
- b) 3
- c) 4
- d) 6

Answer: option B

Explanation:-

1100010 is =98 in decimal.

0101 is =5 in decimal.

Now performing 98/5, remainder will be 3.

Answer is b.

23. One way to make a four-bit adder perform subtraction is by:

- a) Inverting the output.
- b) Inverting the carry-in.
- c) Inverting the b inputs.
- d) Grounding the b inputs.

Answer: option C

26. What is the most important operation in binary-coded decimal (BCD) arithmetic?

- a) Addition
- b) Subtraction
- c) Multiplication
- d) Division

Answer: option A

24. The range of positive numbers when using an eight-bit two's-complement system is:

- a) 0 to 64
- b) 0 to 100
- c) 0 to 127
- d) 0 to 256

Answer: option C

25. What are the two types of basic adder circuits?

- a) Sum and carry
- b) Half-adder and full-adder
- c) Asynchronous and synchronous
- d) One- and two's-complement

Answer: option B

26. The truth table for a full adder is shown below. What are the values of x, y, and z?

P	Q	C1	CO	Σ
0	0	0	0	0
0	0	1	0	X
0	1	0	0	1
0	1	1	Y	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	Z	

- a) X = 0, y = 1, z = 1
- b) X = 1, y = 1, z = 1
- c) X = 1, y = 0, z = 1
- d) X = 0, y = 0, z = 1

Answer: option B

27. A half-adder circuit would normally be used each time a carry input is required in an added circuit.

- A) True
- B) False

Answer: option B

28. If b[7..0] = 10100101, what is the value of b[6..2]?

- a) 10100
- b) 01001
- c) 10010
- d) 00101

Answer: option B

Explanation:-

B[7..0] = 10100101.

B[6..2] = ?

Start from most significant bit.

B[7]=1.

B[6]=0.

B[5]=1.

B[4]=0.

B[3]=0.

B[2]=1.

B[1]=0.

B[0]=1, we take bit from 6 to 2 indexing so answer would be 01001.

29.How many inputs must a full-adder have?

- a) 4
- b) 2
- c) 5
- d) 3

Answer: option D

$$\begin{array}{r} 01101000_{BCD} \\ + 00110110_{BCD} \\ \hline \end{array}$$

30. = ______{BCD}

- a) 10011110
- b) 01211110
- c) 000100000100
- d) 001000001000

Answer: option C

Explanation:-

After addition we have to add 0110 (6) to both the term i.e. After addition we get 1001 1110 and now we add 0110 to 1001 and also 0110 to 1110. I.e 0110 0110 will be added to 1001 1110 because no term would be greater than or equal to 9.

After addition final result will be 100000100. For making it a three 4 bit number we add extra 3 zero.

31.Determine the two's-complement of each binary

number. 00110 00011 11101

- a) 11001 11100 00010
- b) 00111 00010 00010
- c) 00110 00011 11101
- d) 11010 11101 00011

Answer: option D

32.Solve this binary problem: 01110010 – 01001000 =

00011010

00101010

01110010

00111100

Answer: option B

33.What distinguishes the look-ahead-carry adder?

- a) It is slower than the ripple-carry adder.
- b) It is easier to implement logically than a full adder.

- c) It is faster than a ripple-carry adder.
- d) It requires advance knowledge of the final answer.

Answer: option C

34. Solve this binary problem:

1000

- 0001

- a) 1001
- b) 0110
- c) 0111
- d) 0101

Answer: option C

35. Half-adders can be combined to form a full-adder with no additional gates.

- A) True
- B) False

Answer: option B

36. Perform the following hex subtraction: ace₁₆ - 999₁₆ =

- a) 235₁₆
- b) 135₁₆
- c) 035₁₆
- d) 335₁₆

Answer: option B

37. Which of the following is correct for full adders?

- a) Full adders have the capability of directly adding decimal numbers.
- b) Full adders are used to make half adders.
- c) Full adders are limited to two inputs since there are only two binary digits.
- d) In a parallel full adder, the first stage may be a half adder.

Answer: option D

38. Convert each of the signed decimal numbers to an 8-bit signed binary number (two's-complement). +7 -3 -12

- a) 0000 0111 1111 1101 1111 0100
- b) 1000 0111 0111 1101 0111 0100
- c) 0000 0111 0000 0011 0000 1100
- d) 0000 0111 1000 0011 1000 1100

Answer: option A

Explanation:-

+7 => 00000111.

-3=>for -ve sign the 1st four digit should be 1111 and the 3 becomes 0011 in binary. Take 2's complement of 3. We will get 1101.

I.e 3=>0011.

1's complement => 1100.

2's complement => 1101.

39.What is one disadvantage of the ripple-carry adder?

- a) The interconnections are more complex.
- b) More stages are required to a full adder.
- c) It is slow due to propagation time.
- d) All of the above.

Answer: option C

40.Solve this binary problem: $01000110 \div 00001010 =$

- a) 0111
- b) 100011
- c) 1001
- d) 0011

Answer: option A

Explanation:-

First convert given binary numbers into decimal numbers. Then divide two decimal numbers gives one decimal number. They given binary numbers as input so output must in binary. So again convert decimal number to binary.

$$01000110 = 0 + 64 + 0 + 0 + 0 + 4 + 2 + 0 = 70$$

$$00001010 = 0 + 0 + 0 + 0 + 8 + 0 + 2 + 0 = 10$$

$$70/10 = 7$$

$$7 = (0111) \text{in hexa}$$

41.Divide the following binary numbers.

$$\begin{array}{r} 0110 \end{array} \overline{)001100} \quad \begin{array}{r} 0011 \end{array} \overline{)000110} \quad \begin{array}{r} 0010 \end{array} \overline{)001000}$$

- a) 0000 0010 0000 0010 1000 1111
- b) 0000 0010 0001 0010 0000 0100
- c) 0000 0011 0000 0010 0000 0100
- d) 0000 0010 0000 0010 0000 0100

Answer: option D

42.Convert the decimal numbers 275 and 965 to binary-coded decimal (BCD) and add. Select the BCD code groups that reflect the final answer.

- a) 1101 1110 1010

- b) 1110 0010 1110
- c) 0001 0010 0100 0000
- d) 0010 0011 0100 0000

Answer: option C

Explanation:-

$275 + 965 = 1240$. Convert it into BCD then we get 0001 0010 0100 0000.

43. When multiplying 13×11 in binary, what is the third partial product?

- a) 1011
- b) 00000000
- c) 100000
- d) 100001

Answer: option B

Explanation:-

1101

1011

--

so third is zero.

So $0*1=0, 0*0=0, 0*1=0, 0*1=0$ so ans is b: (0000 0000)

44. How many BCD adders would be required to add the numbers $973_{10} + 39_{10}$?

- a) 3
- b) 4
- c) 5
- d) 6

Answer: option A

Explanation:-

Firstly write BCD code for 973 i.e 1001 0111 0011

BCD code for 39 i.e 0011 1001

add both binary no's. I.e 1001 1010 1100

> than 9. So add 6 BCD code

now result 1010 0001 0010

again > 9. Add 6

00001 0000 0001 0010 is finally our result,

thus 3 times BCD adder used.

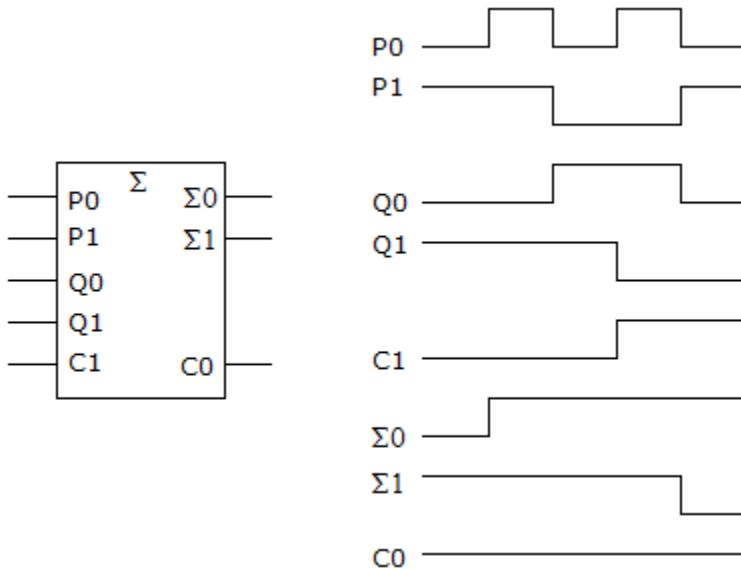
45. The selector inputs to an arithmetic/logic unit (alu) determine the:

- a) Selection of the ic

- b) Arithmetic or logic function
- c) Data word selection
- d) Clock frequency to be used

Answer: option B

46.What is wrong, if anything, with the circuit in the given figure based on the logic analyzer display accompanying the circuit?



- a) The co terminal is shorted to ground.
- b) The s1 output is shorted to V_{cc} .
- c) The p1 input is not being added into the total.
- d) Nothing is wrong; the circuit is functioning correctly.

Answer: option C

TRUE/FALSE

1.An alu is a multipurpose device capable of providing several different logic operations.

- A)True
- B)False

Answer: option A

2.BCD arithmetic is performed using base 10 numbers.

- A)True
- B)False

Answer: option B

3.A full adder has a carry-in.

- A)True
- B)False

Answer: option A

4. Hexadecimal is a base 4 numbering system.

- A) True
- B) False

Answer: option B

5. The solution to the binary problem $00110110 - 00011111$ is 00011000 .

- A) True
- B) False

Answer: option B

6. A binary sum is made up of only 1s and 0s.

- A) True
- B) False

Answer: option A

7. Overflow indicators in alu circuits indicate when add or subtract operations produce results that are too large to fit into four bits.

- A) True
- B) False

Answer: option A

8. The inputs of a full adder are labeled a_1 , b_1 , and c_{in} .

- A) True
- B) False

Answer: option A

9. Larger number capacities may be obtained from 2-bit adders by paralleling them.

- A) True
- B) False

Answer: option A

10. If $[a] = 10$ and $[b] = 01$, then $[a] + [b] = []$.

- A) True
- B) False

Answer: option B

11. 111101000_2 is the 2's-complement representation of -24 .

- A) True
- B) False

Answer: option B

12.The look-ahead-carry adder is slower than the ripple-carry adder because it requires additional logic circuits.

- A)True
- B)False

Answer: option B

13.The solution to the binary problem 1011×0110 is 01100110 .

- A)True
- B)False

Answer: option B

14.The solution to the BCD problem $0101 + 0100$ is 00001001_{BCD} .

- A)True
- B)False

Answer: option A

15.A macrofunction is a self-contained description of a logic circuit with all of its inputs, outputs, and operational characteristics defined.

- A)True
- B)False

Answer: option A

16.A half-adder circuit would normally be used each time a carry input is required in an adder circuit.

- A)True
- B)False

Answer: option B

17.The binary subtraction $0 - 1 =$ is difference = 1;borrow = 0

- A)True
- B)False

Answer: option B

18.A sign bit of "1" in the difference of a 2's-complement subtraction problem indicates the magnitude is negative and in true binary form.

- A)True
- B)False

Answer: option B

Explanation:-

The "1" that comes in the result after one's complement show that the result is -ve. In 2's complement, the 1 is already wrapped and added to the LSB of the result after 1's complement.

19.Constants must be included in a package.

- A)True
- B)False

Answer: option A

20.10011100 in two's-complement notation has a decimal value of – 100.

- A)True
- B)False

Answer: option B

21.There are four possible combinations for subtracting two binary numbers.

- A)True
- B)False

Answer: option A

22.It is not necessary to have the same number of bits when adding or subtracting signed binary numbers in the 2's-complement system.

- A)True
- B)False

Answer: option B

23.Full adder results are typically stored in registers.

- A)True
- B)False

Answer: option A

24.The representation of -1_{10} in eight-bit two's-complement notation is 11110111.

- A)True
- B)False

Answer: option B

25.Binary division and decimal division use the same procedure.

- A)True
- B)False

Answer: option A

26.When the 2's-complement system is used, the number to be subtracted is changed to its 2's complement and then added to the minuend.

- A)True

B)False

Answer: option A

27.Full adders can add two numbers and need not have a carry input or a carry output.

A)True

B)False

Answer: option A

28.The VHDL compiler requires libraries to be specified at the beginning of the code if components from those libraries are being used.

A)True

B)False

Answer: option A

29.The carry-out of a binary adder is identified using the summation symbol, sigma.

A)True

B)False

Answer: option B

30.The 74ls382 alu is a 24-pin arithmetic/logic unit.

A)True

B)False

Answer: option B

31.The two's-complement method is used in computer systems that perform arithmetic.

A)True

B)False

Answer: option A

32.Digital computers use an easier method to subtract binary numbers, called one's complement.

A)True

B)False

Answer: option B

Explanation:-

Digital computers use an easier method to subtract binary numbers, called two's complement.

33. Binary multiplication is like decimal multiplication except you deal only with 1s and 0s.

- A) True
- B) False

Answer: option A

34. The solution to the binary problem $1011 - 0111$ is 1000.

- A) True
- B) False

Answer: option B

35. A 74hc283 can be used to implement a 4-bit full adder.

- A) True
- B) False

Answer: option A

36. The range of negative numbers when using an eight-bit two's-complement system is -1 to -128.

- A) True
- B) False

Answer: option A

37. If no bits are designated inside square braces, [], it means the variable is the null set.

- A) True
- B) False

Answer: option B

38. This logic gate is used to produce an arithmetic sum xor.

- A) True
- B) False

Answer: option A

39. The solution to the binary problem $0101 + 1111$ is 10100.

- A) True
- B) False

Answer: option A

40. Alu circuits cannot be cascaded to perform functions on more than four bits.

- A) True
- B) False

Answer: option B

FILL UP THE BLANKS

1.In VHDL, the architecture declaration always begins with the _____ of variable signals or components that will be used in the concurrent description between begin and end.

- a) Type
- b) Vectors
- c) Functions
- d) Declarations

Answer: option D

2.When decimal numbers with several digits are to be added together using BCD adders _____.

- a) A separated BCD adder is required for each digit position
- b) The BCD adders must have the carry-outs grounded
- c) The BCD's must be grouped in twos
- d) Full adders are also used

Answer: option A

3.The binary adder circuit is designed to add _____ binary number(s) at a time.

- a) 1
- b) 3
- c) 2
- d) 5

Answer: option C

4.The 74hc382 alu can perform _____ operations.

- a) 2
- b) 4
- c) 8
- d) 16

Answer: option C

5.Subtraction of the 2's-complement system actually involves the operation of _____.

- a) Multiplication
- b) Subtraction
- c) Addition
- d) Division

Answer: option C

6.The carry-out of a full adder is _____.

- a) $\bar{A}B + A\bar{B}$
- b) $\bar{A}BC_{IN} + A\bar{B}C_{IN}$

- c) $\bar{A}BC_{IN} + A\bar{B}C_{IN} + ABC\bar{C}_{IN}$
d) $\bar{A}BC_{IN} + A\bar{B}C_{IN} + AB\bar{C}_{IN} + ABC_{IN}$

Answer: option D

7. $Fc48 - ab91 = \underline{\hspace{2cm}}$.

- a) 5B77
b) 5267
c) 50B7
d) 5077

Answer: option C

Explanation:-

$$\begin{array}{r} 1111 \ 1100 \ 0100 \ 1000 \\ - \\ 1010 \ 1011 \ 1001 \ 0001 \\ \hline 0101 \ 0000 \ 1011 \ 0111 \\ 5 \ 0 \ b \ 7 \end{array}$$

8. In BCD addition, the value _____ is added to any invalid code group.

- a) 010101
b) 0U812
c) 100110
d) 0110

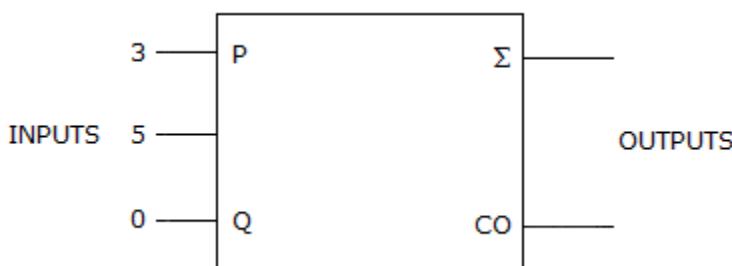
Answer: option D

9. In aHDL macrofunctions, the first thing that should go into any source file is _____ your code.

- a) A field of comments that documents
b) A library of
c) A function name of
d) The universal global definition of

Answer: option A

10. The circuit shown is a(n) _____.



- a) Multiplexer
- b) Adder
- c) Comparator
- d) Converter

Answer: option B

11. The binary addition of $1 + 1 = \underline{\hspace{2cm}}$.

- a) Sum = 1; carry = 1
- b) Sum = 0; carry = 0
- c) Sum = 1; carry = 0
- d) Sum = 0; carry = 1

Answer: option D

12. A 74hc283 can be used to implement a(n) _____ adder.

- a) 4-bit BCD
- b) 8-bit BCD
- c) 4-bit full
- d) 8-bit full

Answer: option C

13. The two's complement of 00001111 is _____.

- a) 11111111
- b) 11110000
- c) 11110001
- d) 11110111

Answer: option C

14. Inside a computer all arithmetic operations take place in the _____.

- a) Accumulator register
- b) Alu
- c) Cpu
- d) B register

Answer: option B

15. -9_{10} represented in eight-bit two's-complement notation is _____.

- a) 11110111
- b) 11111001
- c) 11110110
- d) 01111101

Answer: option A

16. Solve this binary problem: $01011000 \div 00001011 = \underline{\hspace{2cm}}$.

- a) 1010
- b) 0110
- c) 1000
- d) 1110

Answer: option C

17. If $[a] = 10$ and $[b] = 01$, then $[a] \otimes [b] = \text{_____}$.

- a) [00]
- b) 00
- c) 11
- d) [11]

Answer: option C

18. Binary numbers can be added together in a basic parallel-adder circuit when _____.

- a) Negative numbers are in 2's-complement form
- b) Negative numbers are in 1's-complement form
- c) All carry pins are grounded
- d) All negative numbers are noted

Answer: option A

19. To make an eight-bit adder from two four-bit adders you must connect _____.

- a) The high-order carry-in to ground
- b) The low-order carry-out to the high-order carry-in
- c) The high-order carry-out to ground
- d) The low-order sum to the high-order data input

Answer: option B

20. Packages are used to contain _____ and other information that must be available to all entities in the design file.

- a) Types
- b) Vectors
- c) Components
- d) Variables

Answer: option C

21. $34FC + AD31 = \text{_____}$.

- a) E22D
- b) E31D
- c) E21D
- d) E42D

Answer: option A

22. Solve this binary problem: $1001 \times 1100 = \underline{\hspace{2cm}}$.

- a) 01110001
- b) 01111000
- c) 01101100
- d) 01101110

Answer: option C

23. A four-bit adder can perform $\underline{\hspace{2cm}}$.

- a) Addition
- b) Subtraction
- c) Logical and
- d) All of the above

Answer: option A

24. The concurrent section of the hardware description is where the $\underline{\hspace{2cm}}$ are interconnected.

- a) Function
- b) Components
- c) Circuits
- d) Macro functions

Answer: option B

25. The contents of the a register after $[A] = 0001\ 1001 \rightarrow [B]$ S \rightarrow $\underline{\hspace{2cm}}$ is

- a) 0000
- b) 0001
- c) 1001
- d) 1010

Answer: option D

26. The binary subtraction $1 - 1 = \underline{\hspace{2cm}}$.

- a) Difference = 0; borrow = 0
- b) Difference = 1; borrow = 0
- c) Difference = 1; borrow = 1
- d) Difference = 0; borrow = 1

Answer: option A

27. When subtracting 6 from 9 using 2's-complement methods, the $\underline{\hspace{2cm}}$ is 2's complemented before the addition.

- a) Six
- b) Multiplier
- c) Nine
- d) Two

Answer: option A

28. When performing binary addition using the 2's-complement method, an _____ can occur if _____ are of the same _____; the error is indicated by a(n) _____.

- a) Error, both numbers, magnitude, negative sign
- b) Overflow, both numbers, sign, incorrect sign bit
- c) Overflow, signs, magnitude, incorrect sum
- d) Error, the signs, polarity, incorrect polarity

Answer: option B

29. Negation is performed by simply performing the _____ operation.

- a) 1's-complement
- b) Sign
- c) Surrogate
- d) 2's-complement

Answer: option D

30. Solve this BCD problem: $0101 + 0110 = \underline{\hspace{2cm}}$.

- a) 00010111_{BCD}
- b) 00001001_{BCD}
- c) 00010001_{BCD}
- d) 00010011_{BCD}

Answer: option C

Explanation:-

$0101 = 5$.

$0110 = 6$.

$5+6 = 11$.

Here, final answer is 11. So we can split 11 as 1 and 1.

The equivalent value of 1 = 0001 (1st split up).

The equivalent value of 1 = 0001 (2nd split up).

$11 = 00010001$ is the answer.

12.COUNTERS

1.How many flip-flops are required to make a mod-32 binary counter?

- a) 3
- b) 45
- c) 3
- d) 6

Answer: option C

Explanation:-

$$N=32$$

$$\Rightarrow 2^{n-1} \leq n \leq 2^n$$

if $n=5$it satisfy the condition.

$$\Rightarrow 2^4 \leq n \leq 2^5$$

so..... $n=5$ i.e. 5 flip flops.

2.Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?

- a) 50,000
- b) 65,536
- c) 25,536
- d) 15,536

Answer: option D

Explanation:-

$$2^4=16 \text{ ffs.}$$

For 4 bit counter 4 ffs used.

For 4 cascaded 4 bit counter $4*4=16$ ffs used.

$$2^{16}=65536.$$

But we have 50000.

$$\text{So, } 65536 - 50000 = 15536.$$

3.A mod-16 ripple counter is holding the count 1001_2 . What will the count be after 31 clock pulses?

- a) 1000_2
- b) 1010_2
- c) 1011_2
- d) 1101_2

Answer: option A

Explanation:-

Current state of flip-flop is 9(1001), means total 9 pulses are completed and we require after 31 pulses, so total clock pulses are 40.

Mod-16 ripple counter count 16 states and it will repeat again. So for 2nd round 32 clock pulses are completed.

Therefore $40-32 = 8$.

4. The terminal count of a modulus-11 binary counter is _____.

- a) 1010
- b) 1000
- c) 1001
- d) 1100

Answer: option A

Explanation:-

Terminal count means the final count modulus-11 binary counter requires 4 ffs. It can have 11 different states. Hence the terminal count is 1010.

5. List which pins need to be connected together on a 7493 to make a mod-12 counter.

- a) 12 to 1, 11 to 3, 9 to 2
- b) 12 to 1, 11 to 3, 12 to 2
- c) 12 to 1, 11 to 3, 8 to 2
- d) 12 to 1, 11 to 3, 1 to 2

Answer: option C

Explanation:-

12 & 1 are clear pins, 11&3 are clk pins, 8&2 are input for 7493 ff.

6. How can a digital one-shot be implemented using HDL?

- a) By using a resistor and a capacitor
- b) By applying the concept of a counter
- c) By using a library function
- d) By applying a level trigger

Answer: option B

7. Integrated-circuit counter chips are used in numerous applications including:

- a) Timing operations, counting operations, sequencing, and frequency multiplication
- b) Timing operations, counting operations, sequencing, and frequency division
- c) Timing operations, decoding operations, sequencing, and frequency multiplication

- d) Data generation, counting operations, sequencing, and frequency multiplication**

Answer: option B

8.Synchronous construction reduces the delay time of a counter to the delay of:

- a) All flip-flops AND Gates**
- b) All flip-flops AND Gates after a 3 count**
- c) A single gate**
- d) A single flip-flop and a gate**

Answer: option D

Explanation:-

Synchronous:-In synchronous construction, clock is applied simultaneously to flip flop & gate.

Asynchronous:-If output of one flipflop is connected to the input of next and soon like that then in that case the delay will be equal to sum of delays of all flip flops.

9.Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:

- a) Input clock pulses are applied only to the first and last stages**
- b) Input clock pulses are applied only to the last stage**
- c) Input clock pulses are not used to activate any of the counter stages**
- d) Input clock pulses are applied simultaneously to each stage**

Answer: option D

Explanation:-

In synchronous counters, clock is applied simultaneously to all the stages therefore delay time is reduced.

In asynchronous counter, clock is applied to only first stage & next stage depends on the response of the previous stage that causes delay.

Or

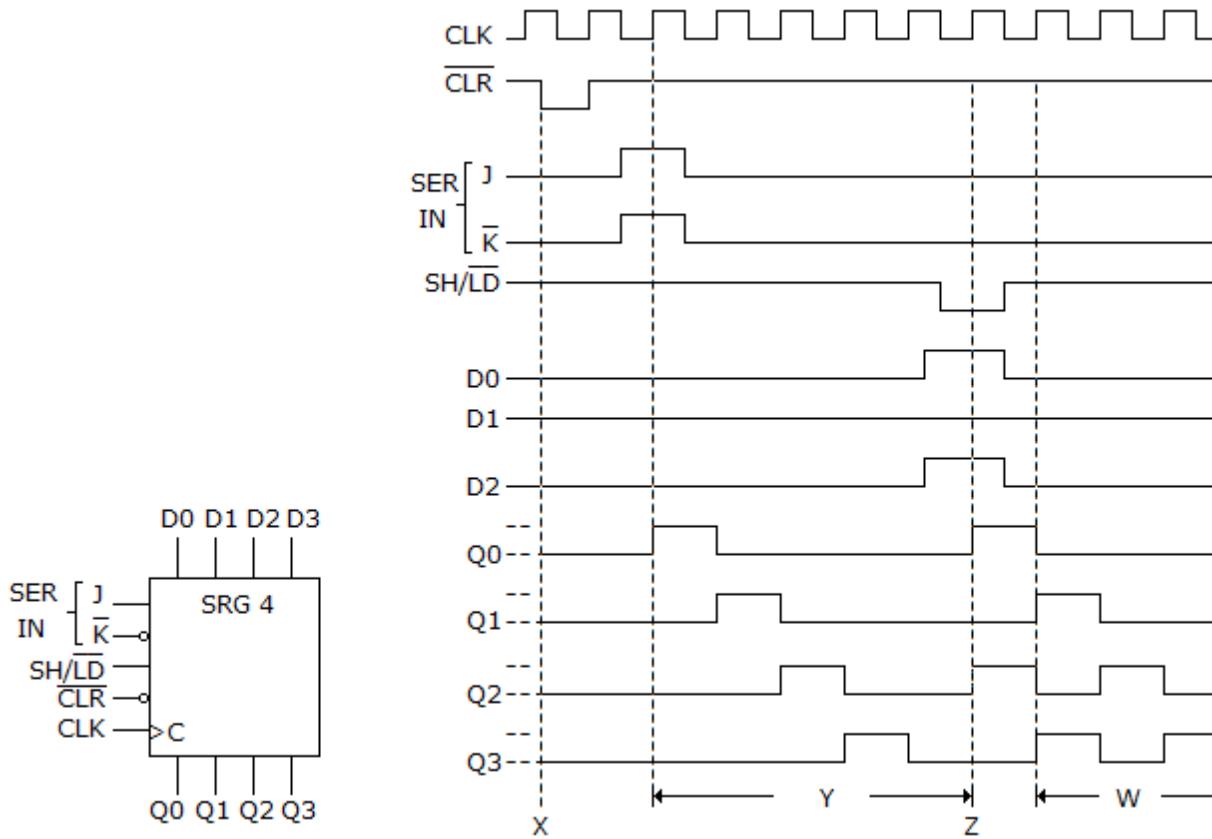
In synchronous counters clock is applied at each bit. So we can reduce delay.

10.What is the difference between a 7490 and a 7492?

- a) 7490 is a mod-12, 7492 is a mod-10**
- b) 7490 is a mod-12, 7492 is a mod-16**
- c) 7490 is a mod-16, 7492 is a mod-10**
- d) 7490 is a mod-10, 7492 is a mod-12**

Answer: option D

11.What type of register is shown below?



- a) Parallel in/parallel out register
- b) Serial in/parallel out register
- c) Serial/parallel-in parallel-out register
- d) Parallel-access shift register

Answer: option D

Explanation:-

Because the o/p is in the form of jonson counter.Parallel access shift register means it is parallel in serial out register.

12.When two counters are cascaded, the overall mod number is equal to the _____ of their individual mod numbers.

- a) Product
- b) Sum
- c) Log
- d) Reciprocal

Answer: option A

Explanation:-

Because output frequency is fin/modulus, modulus = no.of state in first counter*no.of state in second counter.

13.A mod-12 and a mod-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 mhz.

- a) 500 khz
- b) 1,500 khz
- c) 6 mhz
- d) 5 mhz

Answer: option A

Explanation:-

Total mod=12 x 10 =120

so output frequency = 60 mhz /120 =500k

14.Which segments of a seven-segment display would be required to be active to display the decimal digit 2?

- a) A, b, d, e, and g
- b) A, b, c, d, and g
- c) A, c, d, f, and g
- d) A, b, c, d, e, and f

Answer: option A

Explanation:-

In the 8 segment display naming starts from clockwise direction ie, a, b, ..., f and finally g in the middle therefore to have 2 displayed on the screen we will need a, b, d, e, g.

16.How many AND Gates would be required to completely decode all the states of a mod-64 counter, and how many inputs must each AND Gate have?

- a) 128 gates, 6 inputs to each gate
- b) 64 gates, 5 inputs to each gate
- c) 64 gates, 6 inputs to each gate
- d) 128 gates,5 inputs to each gate

Answer: option C

Explanation:-

Total 64 states ie input combination so 64 gates.

For 64 input combinations need 6 variables so 6 input for each gates.

Or

Mod = 64;

mod = 2^6 ;

because,

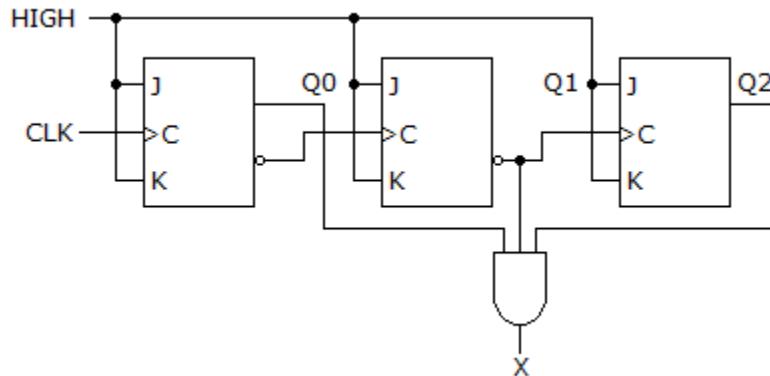
starting mod = 000000.

Ending mod = 111111 for understanding(32 16 8 4 2 1).

Total state = 64(0 to 63).

For every state need of 6 input gate then,
total no.of AND Gate = 64;(every 6 input AND Gate).

17.What decimal value is required to produce an output at "x"?



- a) 1
- b) 1 or 4
- c) 2
- d) 5

Answer: option D

Explanation:-

J=k=high,so output is toggle.toggle means complement of previous output.
Suppose previous output zero ,the output of q2=1,q1=0&q=1. The output of x=5.

Otherwise=>010=>2

Or

For AND Gate if all input is high '1' then o/p is high.

Otherwise low '0';

for o/p '1' means(here x o/p).

All i/p must be '1';

also in this ckt mention that.

Here,

for q0 = 1.

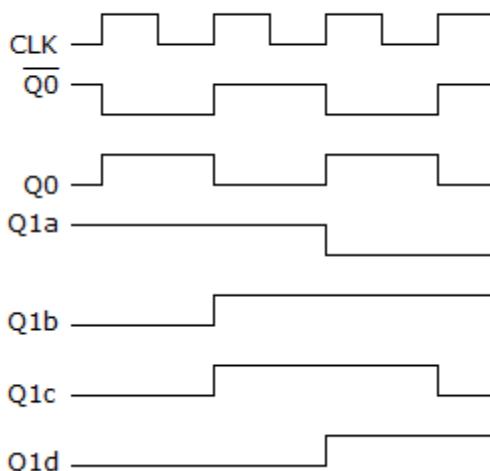
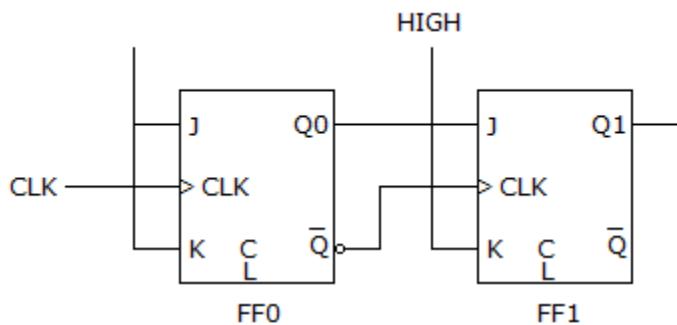
Q1 = 0(bcg ~q=1).

Q2 = 1 then.

O/p is 'high' or 'x'.

18.The circuit given below has no output on q₁ when examined with an oscilloscope. All j-k inputs are high, the clk signal is present, and

the q_0 is toggling. The c input of ff_1 is a constant low. What could be causing the problem?



- a) The q_0 output should be connected to the j input of ff_1 .
b) The output of ff_0 may be shorted to ground.
c) The input of ff_1 may be shorted to ground.
d) Either the output of ff_0 or the input of ff_1 may be shorted to ground.**

Answer: option D

Explanation:-

Here, the output of ff_0 and input of ff_1 becomes low. So became ground. (may be)

19. How many flip-flops are required to construct a decade counter?

- a) 10
b) 8
c) 5
d) 4**

Answer: option D

Explanation:-

$2^4=16$ and $2^3=8$..there for 4 flip flops needed

20.The terminal count of a typical modulus-10 binary counter is

- 0000
1010
1001
1111

Modulus 10 means count from 0 to 9 so terminal count is 9 (1001).

21.A seven-segment, common-anode led display is designed for:

- a) All cathodes to be wired together
- b) One common led
- c) A high to turn off each segment
- d) Disorientation of segment modules

Answer: option C

Explanation:-

Common anode. So to turn on should give grn. So to off high.

22.To operate correctly, starting a ring counter requires:

- a) Clearing one flip-flop and presetting all the others.
- b) Clearing all the flip-flops.
- c) Presetting one flip-flop and clearing all the others.
- d) Presetting all the flip-flops.

Answer: option C

23.The process of designing a synchronous counter that will count in a non binary manner is primarily based on:

- a) External logic circuits that decode the various states of the counter to apply the correct logic levels to the j-k inputs
- b) Modifying BCD counters to change states on every second input clock pulse
- c) Modifying asynchronous counters to change states on every second input clock pulse
- d) Elimination of the counter stages and the addition of combinational logic circuits to produce the desired counts

Answer: option A

24.Select the response that best describes the use of the master reset on typical 4-bit binary counters.

- a) When mr_1 and mr_2 are both high, all qs will be reset to zero.
- b) When mr_1 and mr_2 are both high, all qs will be reset to one.
- c) Mr_1 and mr_2 are provided to synchronously reset all four flip-flops.

d) To enable the count mode, mr_1 and mr_2 must be held low.

Answer: option A

25. For a multistage counter to be truly synchronous, the _____ of each stage must be connected to _____.

- a) C_p , the same clock input line**
- b) Ce , the same clock input line**
- c) \overline{PL} , the terminal count output**
- d) \overline{RC} , both clock input lines**

Answer: option A

Explanation:-

Because BCD counter can count only upto 9 (1001).

26. Which of the following is an invalid output state for an 8421 BCD counter?

- a) 1110**
- b) 0000**
- c) 0010**
- d) 0001**

Answer: option A

Explanation:-

Because BCD counter can count only upto 9 (1001).

26. How many different states does a 3-bit asynchronous counter have?

- a) 2**
- b) 4**
- c) 8**
- d) 16**

Answer: option C

Explanation:-

$2^3 = 8$ so 8 states

27. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay ($t_{p(tot)}$) is _____.

- a) 12 ms**
- b) 24 ms**
- c) 48 ms**
- d) 60 ms**

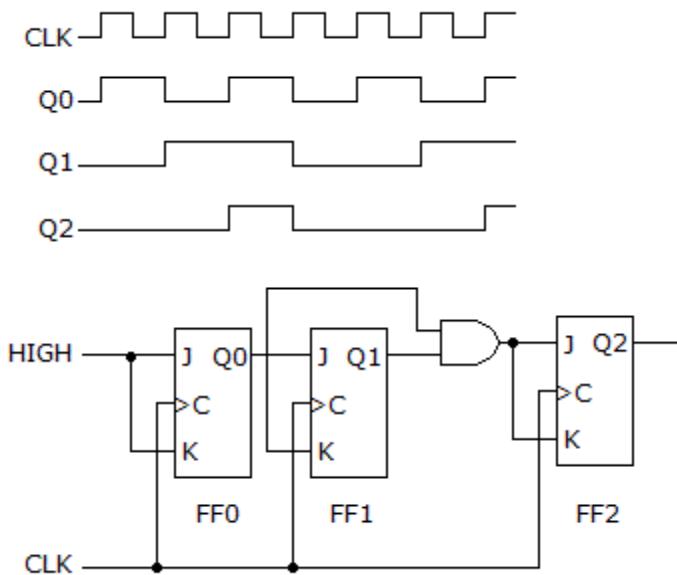
Answer: option D

Explanation:-

Each bit=12ns

5bits= $12\text{ns} \times 5 = 60\text{ns}$.

28.A four-channel scope is used to check the counter in the figure given below. Are the displayed waveforms correct?



- a) Yes
- b) No

Answer: option B

Explanation:-

Case(1):

q2 will go high at falling edges of q0 & q1.

Assume clock skew=0 for simplicity of analysis & take "clock to data delay" under consideration. So we have to consider inputs to "2 right side ff's" will be previous value.

Case(2):

if "clock to data delay" is considered to be 0,then q1 & q2 both wave forms are wrong here.

Please correct if anybody found i am wrong.

29.Which of the following procedures could be used to check the parallel loading feature of a counter?

- a) Preset the load inputs, set the clr to its active level, and check to see that the q outputs match the values preset into the load inputs.
- b) Apply lows to the parallel data inputs, pulse the clk input, and check for lows on all the q outputs.

- c) Apply highs to all the data inputs, pulse the clk and clr inputs, and check to be sure that the q outputs are all low.
- d) Apply highs to all the q terminals, pulse the clk, and check to see if the data terminals now match the q outputs.

Answer: option B

30. One of the major drawbacks to the use of asynchronous counters is:

- a) Low-frequency applications are limited because of internal propagation delays
- b) High-frequency applications are limited because of internal propagation delays
- c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
- d) Asynchronous counters do not have propagation delays and this limits their use in high-frequency applications

Answer: option B

31. Once an up-/down-counter begins its count sequence, it cannot be reversed.

- a) True
- b) False

Answer: option B

Explanation:-

If it is up/down ripple counter, then it is possible. We can simply change the pulse m (mode control) m = 0 or 1 respectively for up counter or down counter .So, the answer is false.

32. Three cascaded modulus-5 counters have an overall modulus of _____.

- a) 5
- b) 25
- c) 125
- d) 500

Answer: option C

Explanation:-

Cube of 5 = 125.

33. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?

- a) None

- b) One
- c) Two
- d) Fifteen

Answer: option D

Explanation:-

Carefully read the question again.it's down counter so to transit from 2 to 3 it has to cover all counts once.
So fifteen is the right answer.

34.The final output of a modulus-8 counter occurs one time for every _____.

- a) 8 clock pulses
- b) 16 clock pulses
- c) 24 clock pulses
- d) 32 clock pulses

Answer: option A

Explanation:-

Since for every mod -n counter there will be n state and each clock pulse is stand for one of its state. So in case of mod-8 counter final state i.e. State 111 will arrive at 8th clock pulse.

35.A 4-bit up/down binary counter is in the down mode and in the 1100 state. To what state does the counter go on the next clock pulse?

- a) 1101
- b) 1011
- c) 1111
- d) 0000

Answer: option B

Explanation:-

It states down count here so 1100 is equal to 12.
So down count is 11 ie 1011.

36.A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____.

- a) 15 ns
- b) 30 ns
- c) 45 ns
- d) 60 ns

Answer: option D

Explanation:-

One bit change is 15ns ... In the qust 1111 to 0000 ie 4 bit change so
 $4 \times 15 = 60\text{ns}.....$

37.The terminal count of a 3-bit binary counter in the down mode is _____.

- a) 000
- b) 111
- c) 101
- d) 010

Answer: option A

Explanation:-

Because it is a down counter. So, counting sequence is 7, 6, 5, ... 0.

38.The hexadecimal equivalent of 15,536 is _____.

- a) 3CB0
- b) 3C66
- c) 63C0
- d) 6300

Answer: option A

Explanation:-

Divide by 16 and get the remainder as the LSB of the hexadecimal, repeat the process till the complete of all division.

- 1) $15536/16 = \text{rem}(0) \& \text{quo}(971)$. The LSB of hexadecimal is 0.
- 2) $971/16 = \text{rem}(11) \& \text{quo}(60)$. The next to LSB is 11, i.e., b.
- 3) $60/16 = \text{rem}(12) \& \text{quo}(3)$. The second next to LSB is 12, i.e., c.
- 4) $3/16 = \text{rem}(3) \& \text{quo}(0)$. The last one is 3.

So the final answer be (3cb0).

39.In an HDL ring counter, many invalid states are included in the programming by:

- a) Using a case statement.
- b) Using an elsif statement.
- c) Including them under others.
- d) The ser_in line.

Answer: option C

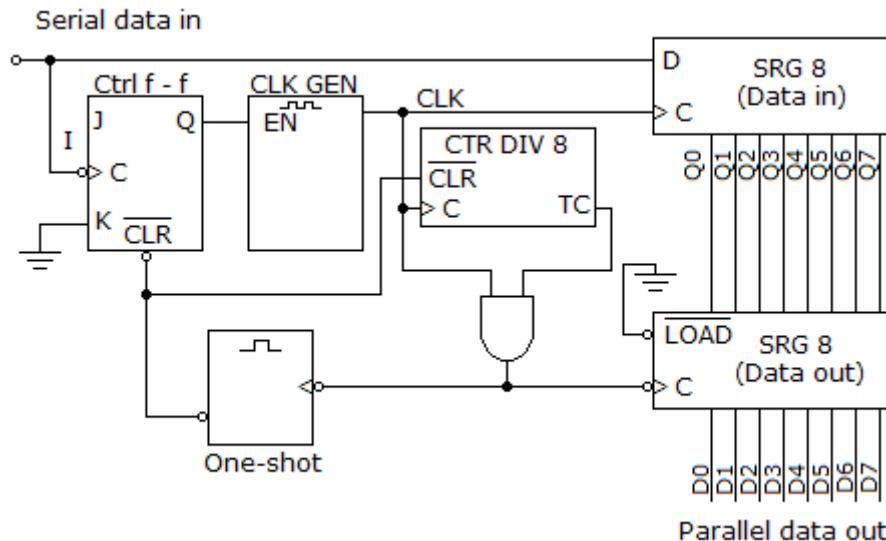
40.In a VHDL retriggerable edge-triggered one-shot, which condition will not exist when a clock edge occurs?

- a) A trigger edge has occurred and we must load the counter.
- b) The counter is zero and we need to keep it at zero.
- c) The shift register is reset.

d) The counter is not zero and we need to count down by one.

Answer: option C

41.What function does the ctr div 8 circuit given below perform?



- a) It divides the clock frequency down to match the frequency of the serial data in.
- b) The divide-by-8 counter is triggered by the control flip-flop and clock, which then allows the data output register to begin storing the input data. Once all eight data bits are stored in the data output register, the data output register and the divide-by-8 counter trigger the one-shot. The one-shot then begins the process all over again.
- c) The divide-by-8 counter is used to verify that the parity bit is attached to the input data string.
- d) It keeps track of the eight data bits, triggering the transfer of the data through the output register and the one-shot, which then resets the control flip-flop and divide-by-8 counter.

42.Synchronous (parallel) counters eliminate the delay problems encountered with asynchronous (ripple) counters because the:

- a) Input clock pulses are applied only to the first and last stages.
- b) Input clock pulses are applied only to the last stage.
- c) Input clock pulses are applied simultaneously to each stage.
- d) Input clock pulses are not used to activate any of the counter stages.

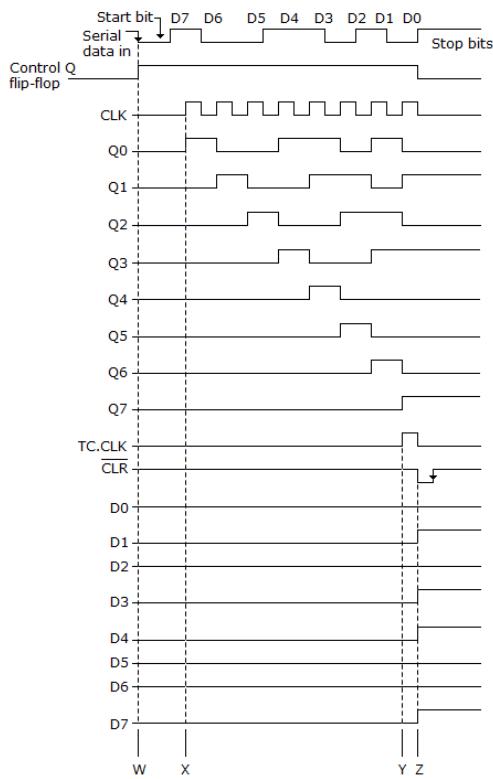
Answer: option C

43.List the state of each output pin of a 7447 if rbi = 0, It = 1, a₀ = 1, a₁ = 0, a₂ = 0, and a₃ = 1.

- a) Rbo = 0, a = 0, b = 0, c = 0, d = 1, e = 1, f = 0, g = 0
- b) Rbo = 1, a = 0, b = 0, c = 0, d = 1, e = 1, f = 0, g = 0
- c) Rbo = 0, a = 0, b = 0, c = 0, d = 0, e = 1, f = 0, g = 0
- d) Rbo = 1, a = 0, b = 0, c = 0, d = 0, e = 1, f = 0, g = 0

Answer: option A

44. Referring to the given figure, what causes the control ff to reset after d7?



Answer: option C

Explanation:-

Once the data cycle is initiated by the start bit, the one-shot produces an output pulse equal to the duration of the eight data bits. Once the eight data bits have been transferred to the data input register, the falling edge of the one-shot pulse resets the control ff to start the sequence all over again.

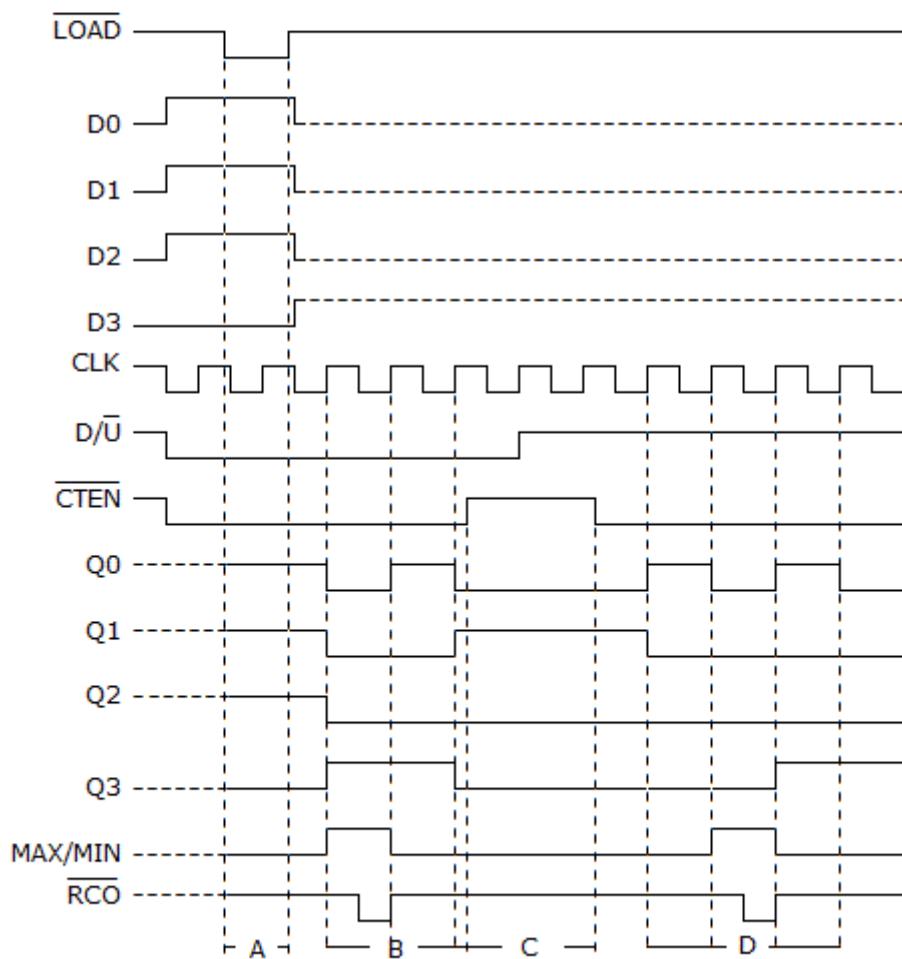
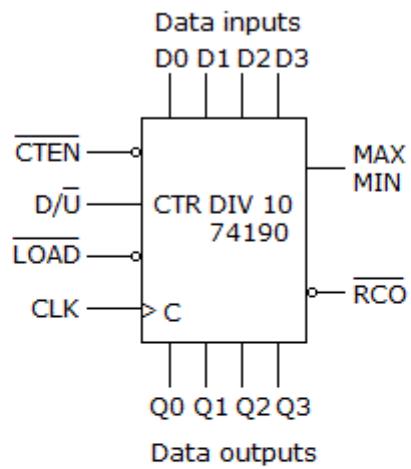
After counting the eight data bits, the divide-by-8 counter produces an output on its active-low clr line to reset the control ff.

After counting eight clock pulses equivalent to eight data periods, the terminal count of the divide-by-8 counter and the clock trigger the one-shot, which in turn resets the control ff and divide-by-8 circuits to begin the sequence all over again. Simultaneously the data is transferred through the output register.

When the data output register is full, it produces an output on its c terminal that triggers the one-shot, which in turn resets the control ff.

44.What function will the counter shown below be performing during period "b" on the timing diagram?

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- a) Counting up**
- b) Counting down**
- c) Inhibited**

d) Loading

Answer: option A

Explanation:-

See the waveform of q0 - q3 its

1000

1001

so its count up.

If d/u is 0 up, else down

(in a: its loading inputs).

45.Three cascaded decade counters will divide the input frequency by _____.

- a) 10
- b) 20
- c) 100
- d) 1000

Answer: option D

Explanation:-

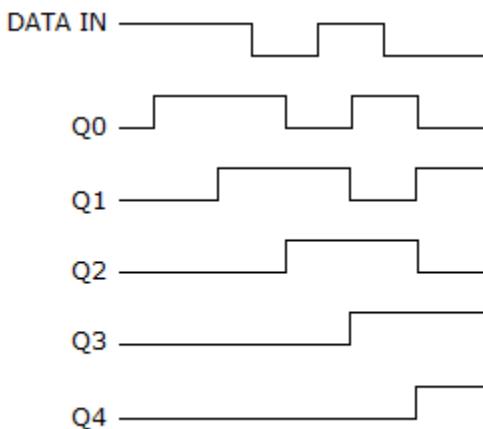
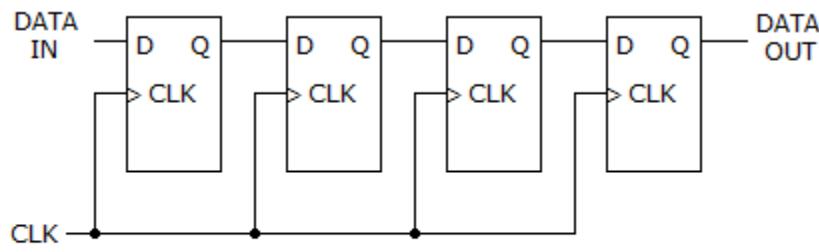
Decade counter has 10 states. So three decade counters are cascaded ie. ,
 $10 \times 10 \times 10 = 1000$.

46.A counter with a modulus of 16 acts as a _____.

- a) Divide-by-8 counter
- b) Divide-by-16 counter
- c) Divide-by-32 counter
- d) Divide-by-64 counter

Answer: option B

47.How many data bits can be stored in the register shown below?



with chandra

- a) 5
- b) 32
- c) 31
- d) 4

Answer: option A

48.What is the difference between a 7490 and a 7493?

- a) 7490 is a mod-10, 7493 is a mod-16
- b) 7490 is a mod-16, 7493 is a mod-10
- c) 7490 is a mod-12, 7493 is a mod-16
- d) 7490 is a mod-10, 7493 is a mod-12

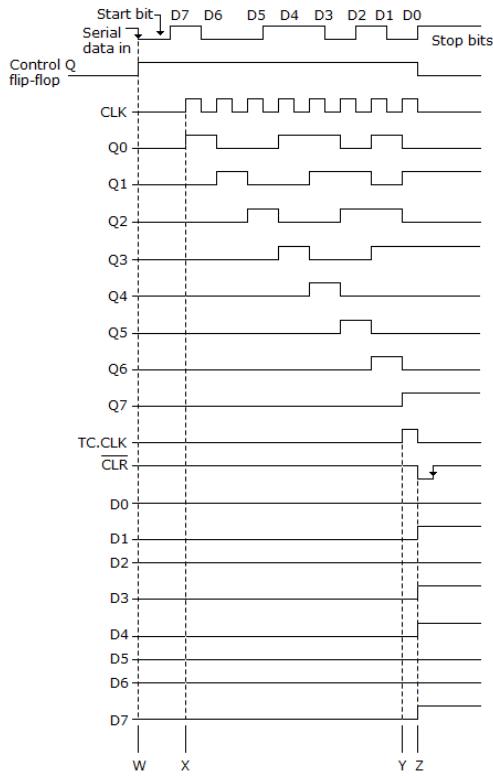
Answer: option A

49.A ripple counter's speed is limited by the propagation delay of:

- a) Each flip-flop
- b) All flip-flops AND Gates
- c) The flip-flops only with gates
- d) Only circuit gates

Answer: option A

50.Referring to the given figure, at which point is the serial data transferred to the parallel output?



- a) W
- b) X
- c) Y
- d) Z

Answer: option D

50.A 4-bit counter has a maximum modulus of _____.

- a) 3
- b) 6
- c) 8
- d) 16

Answer: option D

Explanation:-

$$2^4 = 16.$$

51.Which of the following statements best describes the operation of a synchronous up-/down-counter?

- a) The counter can count in either direction, but must continue in that direction once started.
- b) The counter can be reversed, but must be reset before counting in the other direction.

- c) In general, the counter can be reversed at any point in its counting sequence.
- d) The count sequence cannot be reversed, once it has begun, without first resetting the counter to zero.

Answer: option C

Explanation:-

As this counter has upcount and down count signals separately thus at any time we can provide high at desire one .

52.The parallel outputs of a counter circuit represent the:

- a) Parallel data word
- b) Clock frequency
- c) Counter modulus
- d) Clock count

Answer: option D

53.Any divide-by-n counter can be formed by using external gating to _____ at a predetermined number.

- a) High
- b) Reset
- c) Low
- d) Preset

Answer: option B

54.A mod-16 synchronous counter has inputs labeled

\bar{R}_o , \bar{C}_{PO} , 2^0 , 2^1 , 2^2 and 2^3 . These inputs would most probably be used to:

- a) Reset the counter to 0000 at the end of each count cycle
- b) Preset the counter to a value determined by the $\bar{C}_{PO} - 2^3$ inputs any time the \bar{R}_o is active-high
- c) Preset the counter to a value determined by the $\bar{C}_{PO} - 2^3$ inputs any time the \bar{R}_o is active-low
- d) Reset the counter to 0000 any time $\bar{C}_{PO} - 2^3$ is active-high and \bar{R}_o is active-low

Answer: option D

55.How many natural states will there be in a 4-bit ripple counter?

- a) 4
- b) 8
- c) 16
- d) 32

Answer: option C

Explanation:-

$$2^4 = 16.$$

56. List which pins need to be connected together on a 7492 to make a mod-12 counter.

- a) 1 to 12, 11 to 6, 9 to 7
- b) 1 to 12, 12 to 6, 11 to 7
- c) 1 to 12, 9 to 6, 8 to 7
- d) 1 to 12

Answer: option D

57. A principle regarding most display decoders is that when the correct input is present, the related output will switch:

- a) High
- b) To high impedance
- c) To an open
- d) Low

Answer: option D

58. A modulus-10 counter must have _____.

- a) 10 flip-flops
- b) Flip-flops
- c) 2 flip-flops
- d) Synchronous clocking

Answer: option B

Explanation:-

For any number of modulus we need only 1 flip flop. Because it takes 1 bit but works as a many modulus.

59. For a one-shot application, how can HDL code be used to make a circuit respond once to each positive transition on its trigger input?

- a) By using a counter
- b) By using an active clock
- c) By using an immediate reload
- d) By using edge trapping

Answer: option D

60. Which is not an example of a truncated modulus?

- a) 8
- b) 9
- c) 11
- d) 15

Answer: option A

Explanation:-

Truncated modulus means modulus is not in the power of 2. So in this case, 9, 11 and a5 are not power of 2. So they are truncated. And 8 is 2^3 . So it is not truncated.

61. Four cascaded modulus-10 counters have an overall modulus of _____.

- a) 10
- b) 100
- c) 1000
- d) 10000

Answer: option D

Explanation:-

$$10 * 10 * 10 * 10 = 10000.$$

62. What is the maximum delay that can occur if four flip-flops are connected as a ripple counter and each flip-flop has propagation delays of $t_{phl} = 22 \text{ ns}$ and $t_{plh} = 15 \text{ ns}$?

- a) 15 ns
- b) 22 ns
- c) 60 ns
- d) 88 ns

Answer: option D

Explanation:-

Maximum propagation delay is the longest delay between an input changing value and the output changing value hence $22 * 4 = 88$

We have to consider worst case transition that is "1111" to "0000" here, as t_{phl} is greater. So $22 * 4 = 88$ ns

Please clarify that whether the ripple counter is synchronous or asynchronous.

Because when it is asynchronous then the total delay is $4 * (t_{plh} + t_{phl}) / 2$ else it would be only $(t_{plh} + t_{phl}) / 2$;

63. Which of the following statements are true?

- a) Asynchronous events do not occur at the same time.
- b) Asynchronous events are controlled by a clock.
- c) Synchronous events do not need a clock to control them.
- d) Only asynchronous events need a control clock.

Answer: option A

64.Which segments (by letter) of a seven-segment display need to be active in order to display a digit 6?

- a) B, c, d, e, f, and g
- b) A, c, d, e, f, and g
- c) A, b, c, d, and f
- d) B, c, d, e, and f

Answer: option B

Explanation:-

In seven segment display we see that the numbers from 0 to 9. The letters are arranged in clocked wise from top to bottom in clockwise direction.

65.Which of the following groups of logic devices would be the minimum required for a mod-64 synchronous counter?

- a) Five flip-flops, three AND Gates
- b) Seven flip-flops, five AND Gates
- c) Four flip-flops, ten AND Gates
- d) Six flip-flops, four AND Gates

Answer: option D

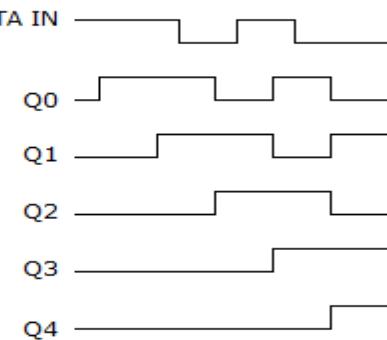
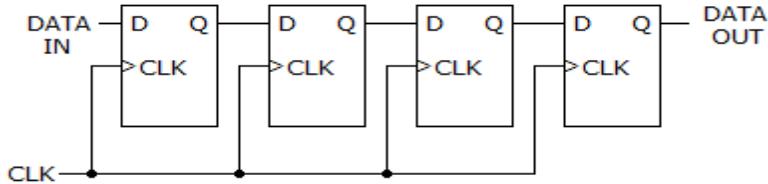
Explanation:-

With n flipflop maximum states possible in counter is 2^n states no of states is called modulus count = 2^6 so 6ffs.

Now remove the line according to the problem we get 6.

With n flipflop maximum states possible in counter is 2^n states no of states is called modulus count = 2^6 so 6ffs.

66.The circuit given below fails to produce data output. The individual flip-flops are checked with a logic probe and pulser, and each checks ok. What could be causing the problem?



- a) The data output line may be grounded.
- b) One of the clock input lines may be open.
- c) One of the interconnect lines between two stages may have a solder bridge to ground.
- d) One of the flip-flops may have a solder bridge between its input and V_{cc} .

Answer: option B

67. A 22-mhz clock signal is put into a mod-16 counter. What is the frequency of the q output of each stage of the counter?

- a) $Q_1 = 22 \text{ mhz}, q_2 = 11 \text{ mhz}, q_3 = 5.5 \text{ mhz}, q_4 = 2.75 \text{ mhz}$
- b) $Q_1 = 11 \text{ mhz}, q_2 = 5.5 \text{ mhz}, q_3 = 2.75 \text{ mhz}, q_4 = 1.375 \text{ mhz}$
- c) $Q_1 = 11 \text{ mhz}, q_2 = 11 \text{ mhz}, q_3 = 11 \text{ mhz}, q_4 = 11 \text{ mhz}$
- d) $Q_1 = 22 \text{ mhz}, q_2 = 22 \text{ mhz}, q_3 = 22 \text{ mhz}, q_4 = 22 \text{ mhz}$

Answer: option B

Explanation:-

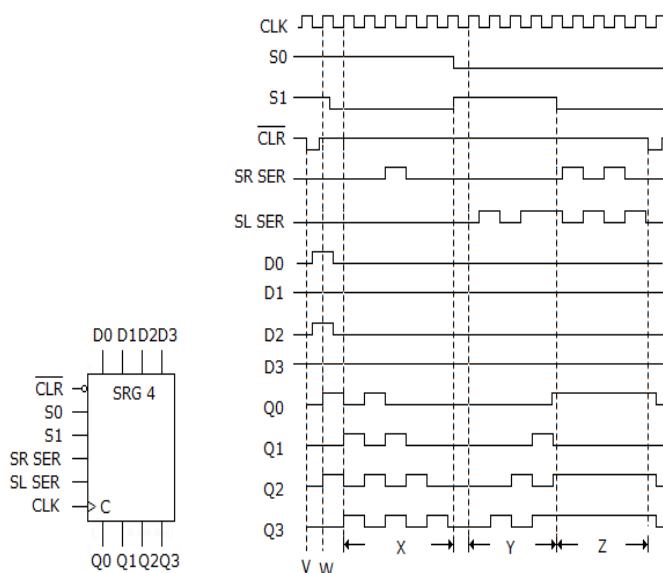
4ff are used $2^4 = 16$ {output of each ff is equal to $f/2, f/4, f/8, f/16$ } so $f=22\text{mhz}$. $[11, 5.5, 2.75, 1.375]$.

68. The designation UP/DOWN means that the _____.

- a) Up count is active-high, the down count is active-low
- b) Up count is active-low, the down count is active-high
- c) Up and down counts are both active-low
- d) Up and down counts are both active-high

Answer: option A

69. What type of device is shown below?



CLEAR	MODE S1 S2	CLK	INPUTS		OUTPUTS			
			SERIAL LEFT RIGHT	PARALLEL D0 D1 D2 D3	QA	QB	QC	QD
L	X X	X	X X	a a X X	L	L	L	L
H	X X	L	X X	X X X X	QA0	QBO	QCO	QD0
H	H H	↑	X X	a b c d	a	b	c	d
H	L H	↑	X H	X X X X	H	QAn	QBn	QCn
H	L H	↑	X L	X X X X	L	QAn	QBn	QCn
H	H L	↑	H X	X X X X	QBn	QCn	QDn	H
H	H L	↑	L X	X X X X	QBn	QCn	QDn	L
H	L L	X	X X	X X X X	QA0	QBO	QCO	QD0

- a) 4-bit bidirectional universal shift register
- b) Parallel in/parallel out shift register with bidirectional data flow
- c) 2-way parallel in/serial out bidirectional register
- d) 2-bit serial in/4-bit parallel out bidirectional shift register

Answer: option A

70.A multiplexed display being driven by a logic circuit:

- a) Accepts data inputs from one line and passes this data to multiple output lines
- b) Accepts data inputs from several lines and allows one of them at a time to pass to the output
- c) Accepts data inputs from multiple lines and passes this data to multiple output lines
- d) Accepts data inputs from several lines and multiplexes this input data to four BCD lines

Answer: option B

71.What is meant by parallel load of a counter?

- a) Each ff is loaded with data on a separate clock.
- b) The counter is cleared.
- c) All ffs are preset with data.

Answer: option C

72.Which of the following is an example of a counter with a truncated modulus?

- a) 8
- b) 13
- c) 16

d) 32

Answer: option B

73. Which of the following is a type of shift register counter?

- a) DECADE**
- b) BINARY**
- c) RING**
- d) BCD**

Answer: option C

Explanation:-

Ring counter is nothing but siso shift register.

74. Mod-6 and mod-12 counters and multiples are most commonly used as:

- a) Frequency counters**
- b) Multiplexed displays**
- c) Digital clocks**
- d) Power consumption meters**

Answer: option C

75. Which of the following is an invalid state in an 8421 BCD counter?

- a) 0011**
- b) 1001**
- c) 1000**
- d) 1100**

Answer: option D

Explanation:-

BCD counter means only we get the value till 9.

76. After 10 clock cycles, and assuming that the data input had returned to 0 following the storage sequence, what values would be stored in q₄, q₃, q₂, q₁, q₀ of the register in figure 7-5?

- a) 0,1,0,1,1**
- b) 1,1,0,1,0**
- c) 1,0,1,0,1**
- d) 0,0,0,0,0**

Answer: option D

77. How many different states does a 2-bit asynchronous counter have?

- a) 1**
- b) 2**

- c) 4
- d) 8

Answer: option C

78.A 12 mhz clock frequency is applied to a cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is _____.

- a) 10 khz
- b) 20 khz
- c) 30 khz
- d) 60 khz

Answer: option C

Explanation:-

Cascaded counter containing a modulus-5 counter, a modulus-8 counter, and a modulus-10 counter.

So $5*8*10=400$.

Mod(400)

12 mhz clock frequency

the lowest output frequency possible is

$12\text{mhz}/400=30\text{ khz}$

TRUE/FALSE

1.Bidirectional shift registers can shift data either right or left.

- A)True
- B)False

Answer: option A

2.In many cases, counters must be strobed in order to eliminate glitches.

- A)True
- B)False

Answer: option A

3.A state diagram is a table of states.

- A)True
- B)False

Answer: option B

4.A ripple counter is an asynchronous counter.

- A)True
- B)False

Answer: option A

5.The mod number of a johnson counter will always be equal to one-half the number of flip-flops in the counter.

- A)True
- B)False

Answer: option B

Explanation:-

Rather it will be double the number of flip flops in the counter.

6.To cascade is to connect in parallel.

- A)True
- B)False

Answer: option B

7.Cascade means to connect the q output of one flip-flop to the clock input of the next.

- A)True
- B)False

Answer: option A

8.In a synchronous counter, each state is clocked by the same pulse.

- A)True
- B)False

Answer: option A

9.Basic counters can be cascaded in parallel to increase the number of data bits that the counter can handle.

- A)True
- B)False

Answer: option B

10.In a 74192 BCD decade up-/down-counter, the terminal count up and the terminal count down are active-low.

- A)True
- B)False

Answer: option A

11.Dependency notation is no longer used.

- A)True
- B)False

Answer: option B

12.A parallel in/serial out shift register enters all data bits simultaneously and transfers them out one bit at a time.

- A)True
- B)False

Answer: option A

13.Generally speaking, the synchronous counter requires more circuitry than an asynchronous counter.

- A)True
- B)False

Answer: option A

14.Another term used to describe up/down counters is bidirectional.

- A)True
- B)False

Answer: option A

15.When implementing a complete system application using ic counter chips, output devices such as led indicators must be configured to operate from the counter outputs.

- A)True
- B)False

Answer: option B

16.One characteristic of a ring counter is that the modulus is equal to the number of flip-flops in the register and, consequently, there are never any unused or invalid states.

- A)True
- B)False

Answer: option B

17.In a full-featured counter in HDL, the concept of rolling over simply means the count sequence has reached its limit and must start over at the beginning of the sequence.

- A)True
- B)False

Answer: option A

18.The 7447 has a 4-bit BCD input, seven individual active-low outputs, and a ripple blanking input and output.

- A)True
- B)False

Answer: option A

19.All decade counters are BCD counters.

- A)True
- B)False

Answer: option B

20.Shift register counters use logic functions to reset the registers when the desired count is reached.

- A)True
- B)False

Answer: option B

21.Three cascaded modulus-10 counters have an overall modulus of 1000.

- A)True
- B)False

Answer: option A

22.A reliable method for eliminating decoder spikes is to use strobing.

- A)True
- B)False

Answer: option A

23.An asynchronous counter differs from a synchronous counter in the method of clocking.

- A)True
- B)False

Answer: option A

24.The terminal count of a typical modulus-10 binary counter is 1010.

- A)True
- B)False

Answer: option B

25.A j-k flip-flop excitation table lists the present state, the next state, and the j and k levels required to produce each transition.

- A)True
- B)False

Answer: option A

26.The concept of a counter to implement a digital one-shot using HDL is not used.

- A)True

B)False

Answer: option B

27.The modulus of a counter is the actual number of states in its sequence.

A)True

B)False

Answer: option A

28.All flip-flops in an asynchronous counter change states at the same time.

A)True

B)False

Answer: option B

29.A glitch is a short pulse resulting in an undesired result in a digital circuit.

A)True

B)False

Answer: option A

30.Aynchronous counters are known as modulus counters.

A)True

B)False

Answer: option B

31.In VHDL, when we want to remember a value it must be stored in a variable.

A)True

B)False

Answer: option A

32.In a seven-segment led display, the BCD must be decoded into a format that can be used to drive the decimal numeric display.

A)True

B)False

Answer: option A

33.Parallel in/parallel out registers have parallel input and output busses.

A)True

B)False

Answer: option A

34. Once an up/down counter begins its count sequence, it cannot be reversed.

- A) True
- B) False

Answer: option B

35. Shift registers are used to store and transfer data.

- A) True
- B) False

Answer: option A

36. An effective time delay device can be constructed by using the propagation delay characteristic of parallel shift registers.

- A) True
- B) False

Answer: option B

37. The term synchronous refers to events that do not occur at the same time.

- A) True
- B) False

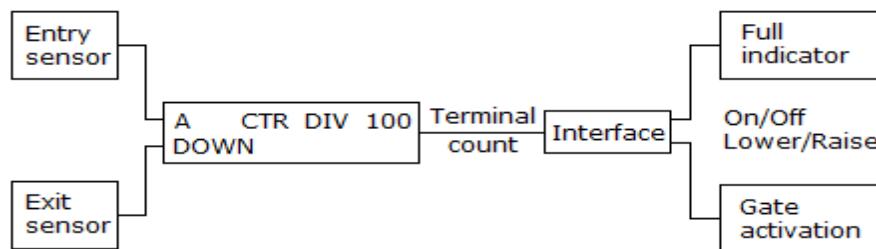
Answer: option B

38. Synchronous binary counters can only be used for the application of timing of digital systems.

- A) True
- B) False

Answer: option B

39. The terminal marked A on the ctr block in the given figure is the set terminal.



- A) True
- B) False

Answer: option B

40.The term synchronous, as applied to counter operations, means that the counter is clocked such that each flip-flop in the counter is triggered at the same time.

- A)True**
- B)False**

Answer: option A

41.Counters are generally decoded in order to determine their count state.

- A)True**
- B)False**

Answer: option A

42.Phototransistors have varying resistance from collector to emitter, depending on how much light strikes them.

- A)True**
- B)False**

Answer: option A

43.Most sequential circuits contain a combinational logic section and a memory section.

- A)True**
- B)False**

Answer: option A

44.A serial in/serial out shift register transfers data from one line of a parallel bus to another line one bit at a time.

- A)True**
- B)False**

Answer: option B

45.The serial in/parallel out shift register transfers data from one parallel data bus to another parallel data bus one bit at a time across a single line.

- A)True**
- B)False**

Answer: option B

46.To design a divide-by-200 counter using synchronous counters, two 4-bit counters could be cascaded together to form an 8-bit counter.

- A)True**
- B)False**

Answer: option A

Explanation:-

If cascading here means to put in, all the outputs of the first counter into an AND Gate which ensures that it gives one when all the outputs are one, and give this as the first input of the second counter.

Also the counters must be edge triggered so that the first input of the second counter does not turn 1 while the first counter has all ones.

Is 'cascading' the right word here then?

47. When a j-k flip-flop is used in a circuit, we only have to consider the level at j and k at the active clock edge to know the states of the outputs.

- A) True
- B) False

Answer: option B

Filling the blanks

1. A reliable method for eliminating decoder spikes is the technique called _____.

- a) Strobing
- b) Feeding
- c) Wagging
- d) Waving

Answer: option A

2. A decade counter will count through decimal _____.

- a) 10
- b) 9
- c) 15
- d) 0

Answer: option B

3. One method of troubleshooting involves _____ the circuit under test with a _____ or _____ and then observing the output to check for proper bit patterns.

- a) Checking, voltmeter, ohmmeter
- b) Exercising, stimulus, test pattern
- c) Testing, scope, logic analyzer
- d) Smashing, hammer, axe

Answer: option B

4. In VHDL, if we need to remember a value it must be stored in a _____.

- a) Funcion

- b) Type declaration
- c) Variable
- d) Process

Answer: option A

5.A glitch that appears on the decoded output of a ripple counter is often difficult to see on an oscilloscope because _____.

- a) It is a random event
- b) It occurs less frequently than the normal decoded output
- c) It is very fast
- d) All of the above

Answer: option D

6.It is a characteristic of ring counters that the _____ equal to the number of flip-flops in the register.

- a) Number of invalid states is
- b) Number of case statements is
- c) Modulus is
- d) Other states are

Answer: option C

7.Many parallel counters use _____ presetting whereby the counter is preset on the active transition of the same clock signal that is used for counting.

- a) Feedback
- b) Synchronous
- c) Ripple
- d) Asynchronous

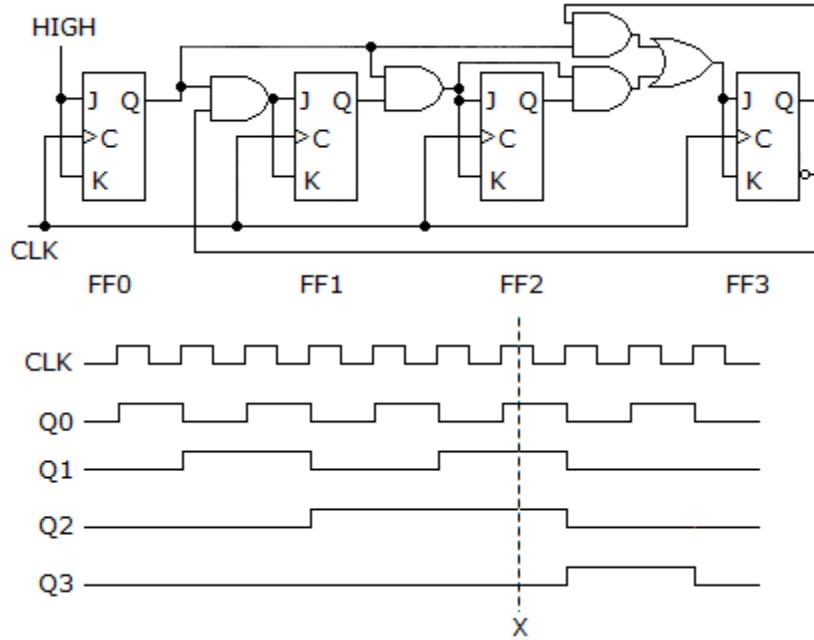
Answer: option B

8.A d flip-flop can be made to toggle by _____.

- a) Connecting to to d
- b) Connecting to q to d
- c) Connecting d low
- d) Connecting d high

Answer: option A

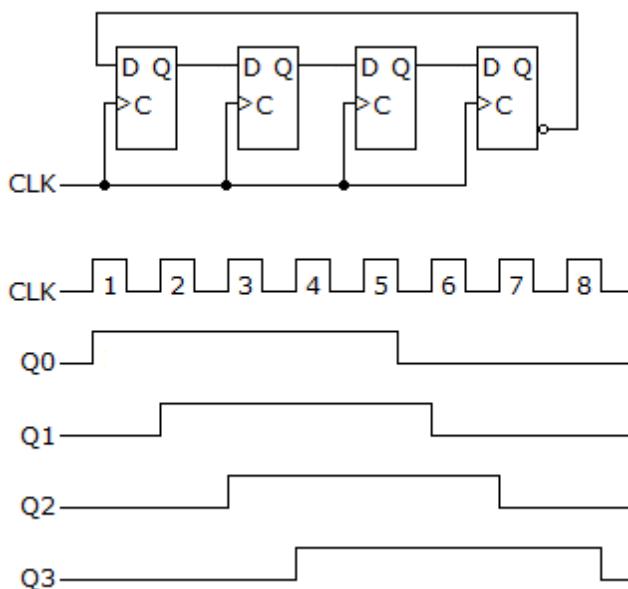
9.The given circuit represents a(n) _____.



- a) Four-bit binary counter
- b) Asynchronous BCD decade counter
- c) Synchronous BCD decade counter
- d) BCD-to-decimal decoder

Answer: option C

10. The circuit shown below is a _____.



- a) Johnson counter
- b) Ring counter
- c) Decade counter
- d) BCD counter

Answer: option A

11.A(n) _____ one-shot starts a pulse in response to a trigger and will restart the internal pulse timer every time a subsequent trigger edge occurs before the pulse is complete.

- a) Non-retriggerable
- b) Retriggerable
- c) High-level triggered
- d) Edge-triggered

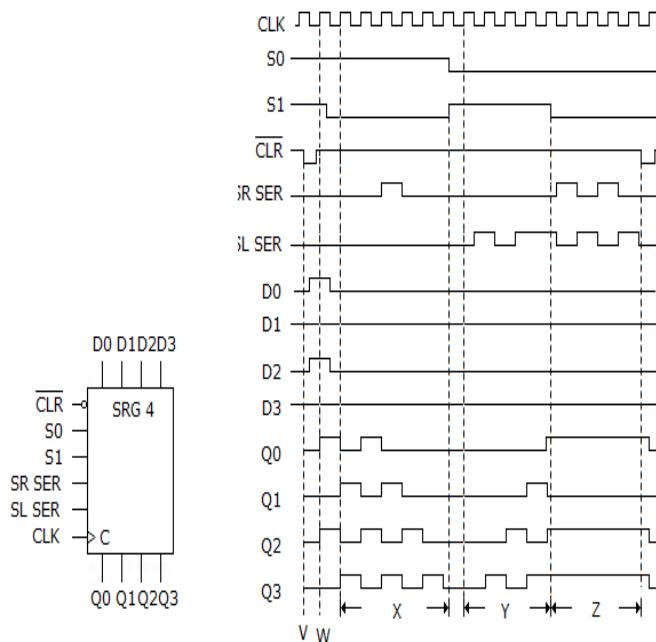
Answer: option B

12.Assume you want to determine the timing diagram for a 4-bit counter using an oscilloscope. The best choice for an oscilloscope trigger signal is _____.

- a) The most significant bit (MSB)
- b) The least significant bit (LSB)
- c) The clock signal
- d) From a composite of the MSB and LSB

Answer: option C

13.Referring to the function table given below, taking the clear, s1, and s0 inputs all high _____.



CLEAR	MODE S1 S2	INPUTS				OUTPUTS					
		CLK		SERIAL		PARALLEL		QA	QB	QC	QD
		LEFT	RIGHT	D0	D1	D2	D3	L	L	L	L
L	X X	X	X X	X X	X X	X X	X X	L	L	L	L
H	X X	L	X X	X X	X X	X X	X X	QA0	QB0	QC0	QD0
H	H H	↑	X X	a b c d	a b c d	a b c d	a b c d				
H	L H	↑	X H	X X X X	X X X X	X X X X	X X X X	H	QAn	QBn	QCn
H	L H	↑	X L	X X X X	X X X X	X X X X	X X X X	L	QAn	QBn	QCn
H	H L	↑	H X	X X X X	X X X X	X X X X	X X X X	QBn	QCn	QDn	H
H	H L	↑	L X	X X X X	X X X X	X X X X	X X X X	QBn	QCn	QDn	L
H	L L	X	X X	X X X X	X X X X	X X X X	X X X X	QA0	QB0	QC0	QD0

- a) Will inhibit the operation of the register
- b) Will reset the parallel registers and inhibit the serial data inputs

- c) Will cause the parallel data inputs to be loaded and passed to the parallel data outputs
- d) Will depend on what values are loaded into the parallel data inputs

Answer: option C

14. Assume a 4-bit ripple counter has a failure in the second flip-flop such that it "locks up." the third and fourth stages will _____.

- a) Continue to count with correct outputs
- b) Continue to count but have incorrect outputs
- c) Stop counting
- d) Turn into molten silicon

Answer: option C

15. In order to use a shift register as a counter, _____.

- a) The register's serial input is the counter input and the serial output is the counter output
- b) The parallel inputs provide the input signal and the output signal is taken from the serial data output
- c) Serial in/serial out register must be used
- d) The serial output of the register is connected back to the serial input of the register

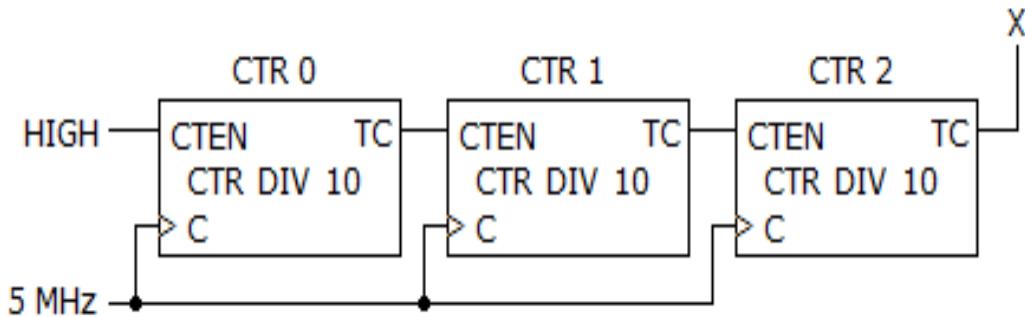
Answer: option D

16. In order to check the clr function of a counter, _____.

- a) Apply the active level to the clr input and check all of the q outputs to see if they are all in their reset state
- b) Ground the clr input and check to be sure that all of the q outputs are low
- c) Connect the clr input to v_{cc} and check to see if all of the q outputs are high
- d) Connect the clr to its correct active level while clocking the counter; check to make sure that all of the q outputs are toggling

Answer: option A

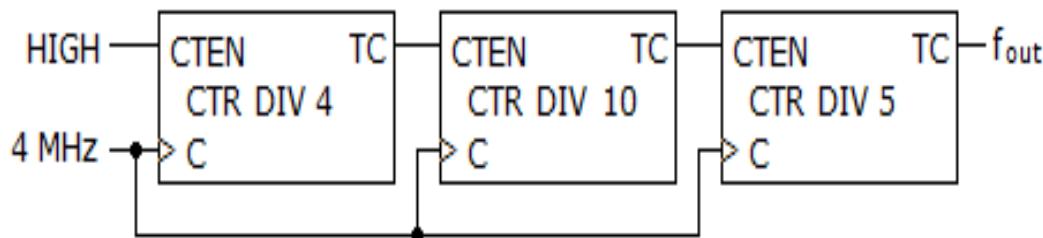
17. The circuit shown below is used for _____, and for the inputs shown, the data output will be _____.



- a) Multiplexing, 1
- b) Parallel-to-serial conversion, 0
- c) Demultiplexing, 0
- d) Parallel-to-serial conversion, high

Answer: option B

18. _____ is the output frequency of the counter shown below.



- a) 4 mhz
- b) 20 khz
- c) 210.5 khz
- d) 800 hz

Answer: option B

19. An asynchronous binary up counter, made from a series of leading edge-triggered flip-flops, can be changed to a down counter by _____.

- a) Taking the output on the other side of the flip-flops (instead of q)
- b) Clocking of each succeeding flip-flop from the other side (instead of q)
- c) Changing the flip-flops to trailing edge triggering
- d) All of the above

Answer: option D

20. A 4-bit binary up counter has an input clock frequency of 20 khz. The frequency of the most significant bit is _____.

- a) 1.25 khz
- b) 2.50 khz
- c) 160 khz
- d) 320 khz

Answer: option A

Explanation:-

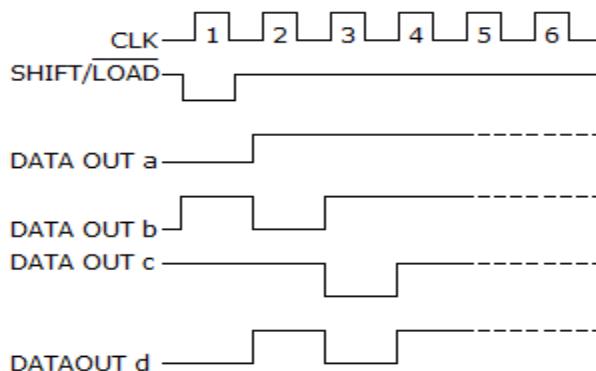
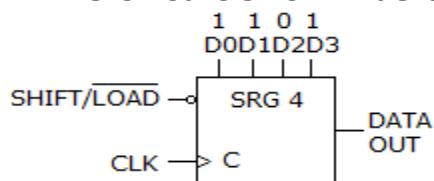
If i am not wrong,
we need to take input clock is = $20k/2$.
So count on basis of 10k clock.
And MSB changes on 8th stage so = $10k/8 = 1.25k$ answer.

21. Modulus refers to _____.

- a) A method used to fabricate decade counter units
- b) The modulus of elasticity, or the ability of a circuit to be stretched from one mode to another
- c) An input on a counter that is used to set the counter state, such as up/down
- d) The maximum number of states in a counter sequence

Answer: option D

22. The circuit shown below is a _____.



- a) Parallel in/serial out register
- b) Serial in/parallel load register
- c) Multiplexer
- d) Demultiplexer

Answer: option A

23.A sequential circuit design is used to _____.

- a) Count up
- b) Count down
- c) Decode an end count
- d) Count in a random order

Answer: option D

24.The mod-10 counter is also referred to as a _____ counter.

- a) Decade
- b) Strobbing
- c) BCD
- d) Circuit

Answer: option A

25.In general, when using a scope to troubleshoot digital systems the instrument should be triggered by _____.

- a) The a channel or channel 1
- b) The vertical input mode, when using more than one channel
- c) The system clock
- d) Line sync, in order to observe troublesome power line glitches

Answer: option C

26._____ counters are often used whenever pulses are to be counted and the results displayed in decimal.

- a) Synchronous
- b) Bean
- c) Decade
- d) BCD

Answer: option D

27.The technique used by one-shots to respond to an edge rather than a level is called _____.

- a) Level management
- b) Edge triggering
- c) Trigger input
- d) Edge trapping

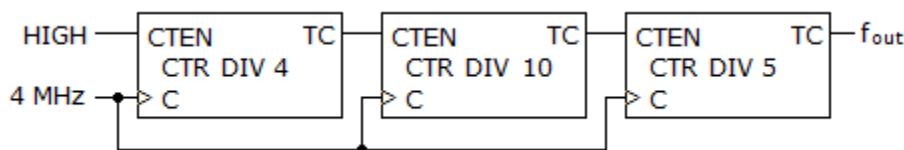
Answer: option A

28.A j-k flip-flop is reset and must stay reset after the clock pulse. This transition requires that _____.

- a) J and k inputs must both = 0
- b) J must be 0, k doesn't matter
- c) J doesn't matter, k must = 0
- d) J must be 0 and k must be 1

Answer: option B

29. _____ is the modulus of the counter shown below.



- a) 200
- b) 19
- c) 0.005
- d) 5000

Answer: option A

Explanation:-

The flip flops are cascading so the mod of the counter is nothing but product of the states i.e. $4 \times 10 \times 5 = 200$.

30. The _____ counter in the altera library has controls that allow it to count up or down, and perform synchronous parallel load and asynchronous cascading.

- a) 74134
- b) Lpm
- c) Synchronous
- d) AHDL

Answer: option B

31. A BCD counter has _____ states.

- a) 8
- b) 9
- c) 10
- d) 11

Answer: option C

32. The decimal equivalent of the largest number that can be stored in a 4-bit binary counter is _____.

- a) 8
- b) 15
- c) 16
- d) 32

Answer: option B

33. The minimum number of flip-flops that can be used to construct a modulus-5 counter is _____.

- a) 3
- b) 5
- c) 8
- d) 10

Answer: option A

34. The duty cycle of the most significant bit from a 4-bit (0-9) BCD counter is _____.

- a) 10%
- b) 20%
- c) 50%
- d) 80%

Answer: option B

Explanation:-

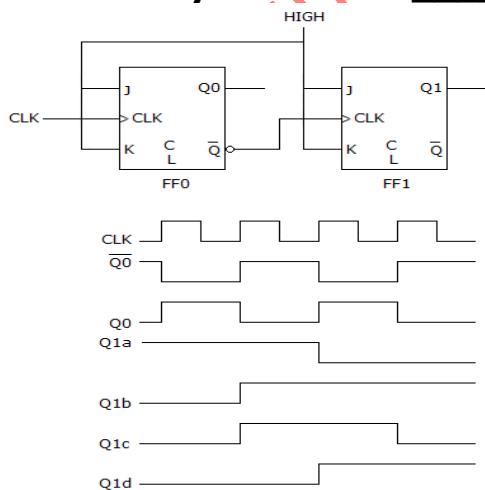
There are 10 states out of which MSB is high only for (1000, 1001) 2 times. Hence duty cycle is $2/10 \times 100 = 20\%$.

35. Shift-register counters use _____, which means that the output of the last ff in the register is connected back to the first ff in some way.

- a) Mod
- b) Feedback
- c) Strobing
- d) Switchbacks

Answer: option B

36. The counter circuit and associated waveforms shown below are for a(n) _____ counter, and the correct output waveform for q_b is shown by waveform _____.



- a) Synchronous, a

- b) Asynchronous, b
- c) Synchronous, c
- d) Asynchronous, d

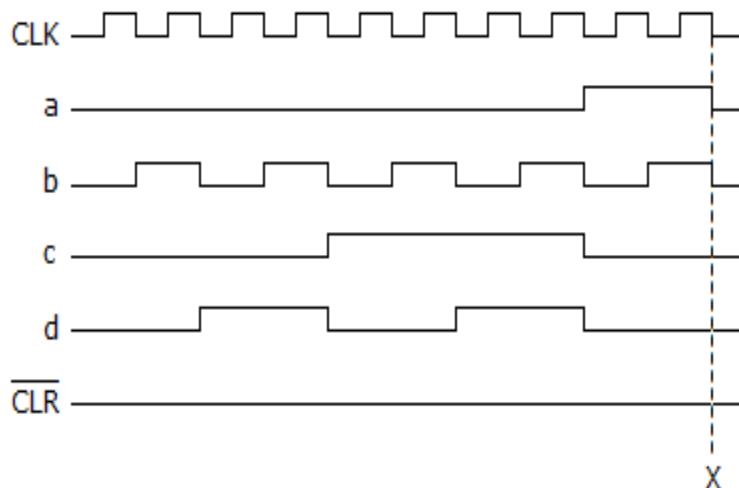
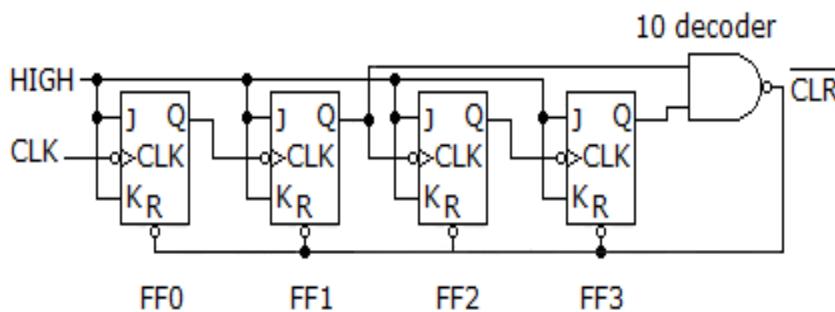
Answer: option C

37.Asynchronous counters are often called _____ counters.

- a) Toggle
- b) Ripple
- c) Binary
- d) Flip-flop

Answer: option B

38.The given circuit is a(n) _____.



- a) Three-bit synchronous binary counter
- b) Eight-bit asynchronous binary flip-flop
- c) Two-bit asynchronous binary counter
- d) Four-bit asynchronous binary counter

Answer: option D

13.SHIFT REGISTERS

1. On the fifth clock pulse, a 4-bit johnson sequence is $q_0 = 0$, $q_1 = 1$, $q_2 = 1$, and $q_3 = 1$. On the sixth clock pulse, the sequence is _____.

- a) $Q_0 = 1, q_1 = 0, q_2 = 0, q_3 = 0$
- b) $Q_0 = 1, q_1 = 1, q_2 = 1, q_3 = 0$
- c) $Q_0 = 0, q_1 = 0, q_2 = 1, q_3 = 1$
- d) $Q_0 = 0, q_1 = 0, q_2 = 0, q_3 = 1$

Answer: option C

Explanation:-

In case of Johnson counter ,the complement o/p of last ff will connect to input of fast ff.if the value is 0111,then it will produce 0011.(comp of 1 is 0 and that value will reflect at first)
so 0111-0011

2. The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the q outputs after two clock pulses?

- a) 0000
- b) 0010
- c) 1000
- d) 1111

Answer: option C

Explanation:-

1st time all the ff clear i.e) 0 states and then we give the i/p 0010.
As 1st clk the o/p is 0000 and then the 2nd clk the o/p is 1000.
3rd clk the o/p is 0100...4th clk the o/p is 0010.

3. What is a shift register that will accept a parallel input, OR a bidirectional serial load and internal shift features, called?

- a) Tri-State
- b) End around
- c) Universal
- d) Conversion

Answer: option C

Explanation:-

The register capable of shifting in one direction is unidirectional shift register. The register capable of shifting in both left and right mode then it is

bidirectional shift register. The universal register that is capable of left & right shift and parallel load capabilities.

4. On the third clock pulse, a 4-bit Johnson sequence is $q_0 = 1$, $q_1 = 1$, $q_2 = 1$, and $q_3 = 0$. On the fourth clock pulse, the sequence is _____.

- a) $Q_0 = 1, q_1 = 1, q_2 = 1, q_3 = 1$
- b) $Q_0 = 1, q_1 = 1, q_2 = 0, q_3 = 0$
- c) $Q_0 = 1, q_1 = 0, q_2 = 0, q_3 = 0$
- d) $Q_0 = 0, q_1 = 0, q_2 = 0, q_3 = 0$

Answer: option A

Explanation:-

In Johnson counter, complement o/p of last f/f is connected to i/p of 1st f/f as q_3 is 0 its complement 1 is applied as i/p to the 1st f/f. So o/p is 1111.

5. A bidirectional 4-bit shift register is storing the nibble 1101. Its RIGHT/LEFT input is high. The nibble 1011 is waiting to be entered on the serial data-input line. After three clock pulses, the shift register is storing _____.

- a) 1101
- b) 0111
- c) 0001
- d) 1110

Answer: option B

Explanation:-

Signal line high means shift right
shift | waiting nibble | stored nibble

-----|-----|-----

initially | 1011: | 1101
right shift (1) | 101 | 1:110
right shift (2) | 10 | 11:11
right shift (3) | 1 | 011:1

rule : when a stored nibble bit is shifted out, a waiting nibble bit is shifted in
hence after the 3rd shift, the stored nibble is 0111

6. How can parallel data be taken out of a shift register simultaneously?

- a) Use the q output of the first ff.
- b) Use the q output of the last ff.
- c) Tie all of the q outputs together.
- d) Use the q output of each ff.

Answer: option D

Explanation:-

The pipo shift register is the simplest of the four configurations as it has only three connections, the parallel input (pi) which determines what enters the Flip-Flop, the parallel output (po) and the sequencing clock signal (clk).

7. What is meant by parallel load of a shift register?

- a. All ffs are preset with data.
- b. Each ff is loaded with data, one at a time.

Answer: option A

Explanation:-

The name itself suggests that data is parallelly loaded which means that if one of the ff of a n- bit register with parallelly load is loaded with a bit then simultaneously all the off as will be loaded with the same value at that particular clock pulse. At preset condition, o/p's of flip-flops will be 1.

Preset = 1 means q = 1..thus i/p is definitely 1.

When clr = 1 then qbar = 1.

8. What does the output enable do on the 74395a chip?

- a) It determines when data can be loaded.
- b) It forces all outputs to go high.
- c) It forces all outputs to go low.
- d) It activates the three-state buffer.

Answer: option D

9. To operate correctly, starting a ring shift counter requires:

- a) Clearing all the flip-flops
- b) Presetting one Flip-Flop and clearing all others
- c) Clearing one Flip-Flop and presetting all others
- d) Presetting all the flip-flops

Answer: option B

10. In a 6-bit johnson counter sequence there are a total of how many states, OR bit patterns?

- a) 2
- b) 6
- c) 12
- d) 24

Answer: option C

Explanation:-

For a Johnson counter with n number of flip-flops we have 2^n output values OR 2^n states will be there at output.

11. A modulus-12 ring counter requires a minimum of _____.

- a) 10 flip-flops
- b) 12 flip-flops
- c) 6 flip-flops
- d) 2 flip-flops

Answer: option B

Explanation:-

For mod-12 counter only 4 ff.

For mod- ring counter 12 ff.

12. Stepper motors have become popular in digital automation systems because _____.

- a) Of their low cost
- b) They are driven by sequential digital signals
- c) They can be used to provide repetitive mechanical movement
- d) They are driven by sequential digital signals and can be used to provide repetitive mechanical movement

Answer: option D

13. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110.

After three clock pulses, the register contains _____.

- a) 01110
- b) 00001
- c) 00101
- d) 00110

Answer: option C

Explanation:-

LSB bit is inverted and feed back to MSB.

01110->initial.

10111->first clk pulse.

01011->second.

00101->third.

14. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (right-most bit first.)

- a) 1100
- b) 0011
- c) 0000

d) 1111

Answer: option C

Explanation:-

Wait | store.

1100 | 0000.

110 | 0000 1st clk.

11 | 0000 2nd clk.

Answer: 0000.

15. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____.

- a) 0000**
- b) 1111**
- c) 0111**
- d) 1000**

Answer: option C

Explanation:-

Wait | store.

0 1 1 1 | 0 0 0 0.

0 1 1 | 1 0 0 0 1st clk.

0 1 | 1 1 0 0 2nd clk.

0 | 1 1 1 0 3rd clk.

| 0 1 1 1 4th clk.

Answer 0111.

16. With a 200 KHz clock frequency, eight bits can be serially entered into a shift register in _____.

- a) 4 μ s**
- b) 40 μ s**
- c) 400 μ s**
- d) 40 ms**

Answer: option B

Explanation:-

F = 200 khz;

t = (1/200) m sec;

t = (1/0.2) micro-sec;

t = 5 micro-sec;

after 8 clock cycles only 8 bit will be loaded=8*5=40 micro-sec;.

17. An 8-bit serial in/serial out shift register is used with a clock frequency of 2 MHz to achieve a time delay (t_d) of _____.

- a) 16 μ s
- b) 8 μ s
- c) 4 μ s
- d) 2 μ s

Answer: option C

Explanation:-

$$T = (n/f).$$

$$T = (8/200 \text{ mhz}).$$

$$T = 4 \text{ micro-sec.}$$

18. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?

- a) Ring shift
- b) Clock
- c) Johnson
- d) Binary

Answer: option A

Explanation:-

Ring shift can be represented data carry by one ff & delete by others.

19. The bit sequence 10011100 is serially entered (right-most bit first) into an 8-bit parallel out shift register that is initially clear. What are the q outputs after four clock pulses?

- a) 10011100
- b) 11000000
- c) 00001100
- d) 11110000

Answer: option B

Explanation:-

10011100/00000000

1001110/00000000 -> 1st clk

100111/00000000 --> 2nd clk

100111/10000000 --> 3rd clk

100111/11000000 --> 4th clk

so ans is 11000000.

20. If an 8-bit ring counter has an initial state 10111110, what is the state after the fourth clock pulse?

- a) 11101011

- b) 00010111
- c) 11110000
- d) 00000000

Answer: option A

Explanation:-

1. For the 1st clk pulse, it would be, 01011111
 2. For the 2nd clk pulse, it would be, 10101111
 3. For the 3rd clk pulse, it would be, 11010111
 4. For the 4th clk pulse, it would be, 11101011
- so answer is 11101011.

21. How would a latch circuit be used in a microprocessor system?

- a) As transportation for intel employees
- b) For a group of data that is the same
- c) As a set of common connections for transfer of data

Answer: option C

22. A 4-bit shift register that receives 4 bits of parallel data will shift to the _____ by _____ position(s) for each clock pulse.

- a) Right, one
- b) Right, two
- c) Left, one
- d) Left, three

Answer: option A

Explanation:-

Two type of register are available. Left and right shift register. If register left shift it shift bit to left or right shift register it shift to right. It is needed to mention it is right or left shift register.

23. How many clock pulses will be required to completely load serially a 5-bit shift register?

- a) 2
- b) 3
- c) 4
- d) 5

Answer: option D

Explanation:-

For submit a each bit, we required 1 clock pulse for 1 shift register. So, for 5-bit shift register we require 5 clock pulses.

24. How is a strobe signal used when serially loading a shift register?

- a) To turn the register on and off
- b) To control the number of clocks
- c) To determine which output q_s are used
- d) To determine the ffs that will be used

Answer: option B

25. An 8-bit serial in/serial out shift register is used with a clock frequency of 150 khz. What is the time delay between the serial input and the q_3 output?

- a) 1.67 μ s
- b) 26.67 μ s
- c) 26.7 ms
- d) 267 ms

Answer: option B

Explanation:-

Q0 to q3 4shifts therefore $4/150\text{khz}=26.67$ microseconds

26. What are the three output conditions of a three-state buffer?

- a) High, low, float
- b) 1, 0, float
- c) Both of the above
- d) Neither of the above

Answer: option C

27. The primary purpose of a three-state buffer is usually:

- a) To provide isolation between the input device and the data bus
- b) To provide the sink OR source current required by any device connected to its output without loading down the output device
- c) Temporary data storage
- d) To control data flow

Answer: option A

28. What is the difference between a ring shift counter and a johnson shift counter?

- a) There is no difference.
- b) A ring is faster
- c) The feedback is reversed.
- d) The johnson is faster.

Answer: option C

Explanation:-

Ring Counter:-A ring counter is a shift register (a cascade connection of flip-flops) with the output of the last one connected to the input of the first, that is, in a ring. Typically a pattern consisting of a single 1 bit is circulated, so the state repeats every n clock cycles if n flip-flops are used. It can be used as a cycle counter of n states.

Johnson Counter:-a johnson counter (or switchtail ring counter, twisted-ring counter, walking-ring counter, or moebius counter) is a modified ring counter, where the output from the last stage is inverted and fed back as input to the first stage. A pattern of bits equal in length to twice the length of the shift register thus circulates indefinitely.

29. What is a recirculating register?

- a) Serial out connected to serial in
- b) All q outputs connected together
- c) A register that can be used over again

Answer: option A

30. When is it important to use a three-state buffer?

- a) When two or more outputs are connected to the same input
- b) When all outputs are normally high
- c) When all outputs are normally low
- d) When two or more outputs are connected to two OR more inputs

Answer: option A

31. A bidirectional 4-bit shift register is storing the nibble 1110. Its RIGHT/LEFT input is low. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____

- a) 1110
- b) 0111
- c) 1000
- d) 1001

Answer: option D

Explanation:-

Stored nibble : waitin nibble.

Initially 1110 : 0111.

1st pulse 1100 : 111.

2nd pulse 1001 : 11.

The final answer after 2nd clk pulse is 1001.

32. In a parallel in/parallel out shift register, $d_0 = 1$, $d_1 = 1$, $d_2 = 1$, and $d_3 = 0$. After three clock pulses, the data outputs are _____.

- a) 1110
- b) 0001
- c) 1100
- d) 1000

Answer: option B

Explanation:-

Yes because as far as i know parallel in parallel out gives the same output as input.

33. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains _____.

- a) 10111000
- b) 10110111
- c) 11110000
- d) 11111100

Answer: option D

Explanation:-

10110111/11110000 -> initial.

10110111/11111000 -> after 1st clk pulse.

10110111/11111100 -> after 2nd clk pulse.

Finally the sol is 11111100.

34. By adding recirculating lines to a 4-bit parallel-in, serial-out shift register, it becomes a _____, _____, and _____-out register.

- a) Parallel-in, serial, parallel
- b) Serial-in, parallel, serial
- c) Series-parallel-in, series, parallel
- d) Bidirectional in, parallel, series

Answer: option A

35. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?

- a) Parallel-in, parallel-out
- b) Parallel-in, serial-out
- c) Serial-in, parallel-out
- d) Serial-in, serial-out

Answer: option C

Explanation:-

I think it should be serial-in, serial-out.

36. When an 8-bit serial in/serial out shift register is used for a $20\ \mu s$ time delay, the clock frequency is _____.

- a) 40 khz
- b) 50 khz
- c) 400 khz
- d) 500 khz

Answer: option C

Explanation:-

Because overall time delay is 20 micro secs.

For each bit $20/8 = 2.5$ micro secs
in frequency it will be 400 khz ($1/2.5$ micro secs).

OR

$$\begin{aligned}F &= (n/t). \\F &= (8/20 \text{ micro-sec}). \\F &= 400 \text{ khz.}\end{aligned}$$

37. Ring shift and johnson counters are:

- a) Synchronous counters
- b) Asynchronous counters
- c) True binary counters
- d) Synchronous and true binary counters

Answer: option A

38. What is the difference between a shift-right register and a shift-left register?

- a) There is no difference.
- b) The direction of the shift

Answer: option B

39. What is a transceiver circuit?

- a) A buffer that transfers data from input to output
- b) A buffer that transfers data from output to input
- c) A buffer that can operate in both directions

Answer: option C

40. A 74hc195 4-bit parallel access shift register can be used for

-
- a) Serial in/serial out operation
 - b) Serial in/parallel out operation

- c) Parallel in/serial out operation
- d) All of the above

Answer: option D

41. Which type of device may be used to interface a parallel data format with external equipment's serial format?

- a) Key matrix
- b) Uart
- c) Memory chip
- d) Series in, parallel out

Answer: option B

42. What is the function of a buffer circuit?

- a) To provide an output that is inverted from that on the input
- b) To provide an output that is equal to its input
- c) To clean up the input
- d) To clean up the output

Answer: option B

43. What is the preset condition for a ring shift counter?

- a) All ffs set to 1
- b) All ffs cleared to 0
- c) A single 0, the rest 1
- d) A single 1, the rest 0

Answer: option D

44. Which is not characteristic of a shift register?

- a) Serial in/parallel in
- b) Serial in/parallel out
- c) Parallel in/serial out
- d) Parallel in/parallel out

Answer: option A

Explanation:-

At a time both serial in **or** parallel are not possible. One should be as input other should be as output.

45. To keep output data accurate, 4-bit series-in, parallel-out shift registers employ a _____.

- a) Divide-by-4 clock pulse
- b) Sequence generator
- c) Strobe line
- d) Multiplexer

Answer: option C

46. With a 50 khz clock frequency, six bits can be serially entered into a shift register in _____.

- a) 12 μ s
- b) 120 μ s
- c) 12 ms
- d) 120 ms

Answer: option B

47. Another way to connect devices to a shared data bus is to use a _____.

- a) Circulating gate
- b) Transceiver
- c) Bidirectional encoder
- d) Strobed latch

Answer: option B

48. To serially shift a nibble (four bits) of data into a shift register, there must be _____.

- a) One clock pulse
- b) Four clock pulses
- c) Eight clock pulses
- d) One clock pulse for each 1 in the data

Answer: option B

Explanation:-

FF's are arranged to form shift registers. FF has only one bit storage.
So 4 clock pulses are needed.

49. Computers operate on data internally in a _____ format.

- a) Tri-State
- b) Universal
- c) Parallel
- d) Serial

Answer: option C

50. In a 4-bit johnson counter sequence there are a total of how many states, OR bit patterns?

- a. 1
- b. 2
- c. 4
- d. 8

Answer: option D

Explanation:-

In johnson no.of states are determined by 2^n so $2^4 = 8$.

51. If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?

- a) 1101000000
- b) 0011010000
- c) 1100000000
- d) 0000000000

Answer: option B

52. How much storage capacity does each stage in a shift register represent?

- a) One bit
- b) Two bits
- c) Four bits (one nibble)
- d) Eight bits (one byte)

Answer: option A

53. When the output of a Tri-State shift register is disabled, the output level is placed in a:

- a) Float state
- b) Low state
- c) High-impedance state
- d) Float or high-impedance state

Answer: option D

TRUE/FALSE

1. One of the stages in a register consists of a latch.

- a) True
- b) False

Answer: option A

2. There are several ways to construct a stepper motor to achieve digitally controlled stepping action. One possibility is to construct four stator coils set up as four pole pairs, each 45° apart and using three ferromagnetic pairs spaced 60° apart.

- a. True
- b. False

Answer: option A

3. A parallel load operation is asynchronous, so it is not dependent on the clock.

- a) True
- b) False

Answer: option A

4. A counter has a specified sequence of states, but a shift register does not.

- a) True
- b) False

Answer: option A

5. In a 74164 8-bit shift register, in order for the parallel data output to be synchronously loaded on the negative clock edge, the parallel enable input is low.

- a) True
- b) False

Answer: option B

7. Practically every possible load, shift, and conversion operation is available in a shift register IC.

- a) True
- b) False

Answer: option A

8. Using separate serial inputs for shifting left or shifting right is a major difference between the 74194 and other shift registers.

- a) True
- b) False

Answer: option A

9. Parallel load means to load all flip-flops at the same time.

- a) True
- b) False

Answer: option A

10. The ring and johnson shift counters are uncommon circuits that are similar to synchronous counters.

- a) True
- b) False

Answer: option B

11. A stepper motor makes its rotation in smooth continuous motion.

- a) True
- b) False

Answer: option B

12. A universal shift register has both serial and parallel input and output capacity.

- a) True
- b) False

Answer: option A

13. The storage capacity of a register makes it an important type of memory.

- a) True
- b) False

Answer: option A

14. The 74194 4-bit bidirectional universal shift register has a wide range of applications.

- a) True
- b) False

Answer: option A

3. A ferromagnetic material is one that forms a resistance to magnetic fields.

- a) True
- b) False

Answer: option B

15. To transmit parallel data over a serial cable, the data must first go through data conversion to the serial format.

- a) True
- b) False

Answer: option A

16. A ring counter is a register in which a certain pattern of 1s and 0s is continuously outputted in parallel.

- a) True
- b) False

Answer: option A

17. Bidirectional means having two states.

- a) True
- b) False

Answer: option B

18. Eight states are in an 8-bit johnson counter sequence.

- a) True

b) False

Answer: option B

19. A stage is two storage elements in a register.

a) True

b) False

Answer: option B

20. When SHIFT/LOAD is low, the data are shifted one bit per clock pulse.

a) True

b) False

Answer: option B

FILL UP THE BLANKS

1. Assume a low logic level is placed on the shift/load input of a 74195 shift register. The output will change _____.

- a. Immediately**
- b. If the clock is also low**
- c. On the next clock leading edge**
- d. Depending on the j and k inputs**

Answer: option C

2. A type of shift register in which the q OR \bar{q} output of one stage is not connected to the input of the next stage is _____.

- a. Parallel in/serial out**
- b. Serial in/parallel out**
- c. Serial in/serial out**
- d. Parallel in/parallel out**

Answer: option D

3. A johnson counter, constructed with n flip-flops, has how many unique states?

- a. N**
- b. $2n$**
- c. 2^n**
- d. N^2**

Answer: option B

4. A type of shift register that requires access to the q outputs of all stages is _____.

- a. Parallel in/serial out**
- b. Serial in/parallel out**

- c. Serial in/serial out
- d. A bidirectional shift register

Answer: option B

5. An 8-bit serial in/parallel out shift register is clocked at 4 MHz and is used to delay a serial digital signal by 1.25 μ s. The output that has the proper delay is _____.

- a. Qe
- b. Qf
- c. Qg
- d. Qh

Answer: option A

6. A 4-bit ring counter is loaded with a single 1. The frequency of any given output is _____.

- a. The same as the clock
- b. Twice the clock frequency
- c. One-half the clock frequency
- d. One-fourth the clock frequency

Answer: option D

7. Shifting a binary number to the left by one position is equivalent to _____.

- a. Multiplying by two
- b. Multiplying by four
- c. Dividing by two
- d. Dividing by four

Answer: option A

Explanation:-

Shifting a binary number by one bit is equivalent to multiplying (when shifting to the left) or dividing (when shifting to the right) the number by 2. Here answer is a ... 32 16 8 4 2 1(from right to left value is multiplied by 2)

8. Assume a 4-bit johnson counter is initially cleared. After the first clock pulse the output is 0001. After the next clock pulse the output will be _____.

- a. 0011
- b. 0010
- c. 1000
- d. 0110

Answer: option A

9. Assume a 4-bit parallel in/serial out shift register is loaded with a binary number. How many clock pulses are required after the parallel load has occurred before the first bit in the sequence appears on the serial output line?

- a. 0
- b. 1
- c. 2
- d. 3

Answer: option B

10. Assume an 8-bit serial in/parallel out shift register needs to be cleared but has no clear input. How many clock cycles are required before a zero applied to the input appears on the q_h output?

- a. 1
- b. 7
- c. 8
- d. 9

Answer: option C

14.CODE CONVERTERS AND MULTIPLEXERS

1. How many outputs are on a BCD decoder?

- a. 4
- b. 16
- c. 8
- d. 10

Answer: option D

Explanation:-

A BCD to decimal decoder has 10 number of outputs because the decimal digits range is from 0 to 9. Normally a BCD decoder has 4 input and 10 outputs.

2. In a gray code, each number is 3 greater than the binary representation of that number.

- a. True
- b. False

Answer: option B

Explanation:-

In gray code any two successive numbers will be differed by only one bit position. But it is not true that the gray code number is 3 greater than binary equality of that number.

For example the gray code of a binary number 1000 is 1100 (difference is 4) similarly for 1111 is 1000 (difference is 7).

3. Use the weighting factors to convert the following BCD numbers to binary.

0101 0011	0010 0110 1000
a. 01010011	001001101000
b. 11010100	100001100000
c. 110101	100001100
d. 101011	001100001

Answer: option C

Explanation:-

BCD we consider 4 bits are taken as one digit because BCD range is 0 to 9 nothing but 4 bits so we consider like that

4. Which digital system translates coded characters into a more useful form?

- a. Encoder
- b. Display
- c. Counter
- d. Decoder

Answer: option D

Explanation:-

Encoder is used to convert non coding to coding.

Decoder is used to convert coding to non coding.

5. From the following list of input conditions, determine the state of the five output leads on a 74148 octal-to-binary encoder.

$I_0=1 I_3=1 I_6=1$

$I_1=1 I_4=0 I_7=1$

$I_2=1 I_5=1 Ei=0$

- a. $G_s = l, a_0 = l, a_1 = l, a_2 = h, e_o = h$
- b. $G_s = l, a_0 = h, a_1 = l, a_2 = l, e_o = h$
- c. $G_s = l, a_0 = l, a_1 = h, a_2 = l, e_o = h$
- d. $G_s = l, a_0 = h, a_1 = h, a_2 = l, e_o = h$

Answer: option D

Explanation:-

I guess the answer should be a) as if $i_4=0$ then output in binary is 100, note- inputs of 74148 are low active hence giving a zero to i_4 gives binary equivalent of 4 i.e 100, $a_2=1, a_1=0, a_0=0$.

6. What is the function of an enable input on a multiplexer chip?

- a. To apply V_{cc}
- b. To connect ground
- c. To active the entire chip
- d. To active one half of the chip

Answer: option C

7. The expansion inputs to a comparator are used for expansion to a(n):

- a. 4-bit system
- b. 8-bit system
- c. BCD system
- d. Counter system

Answer: option B

8. What do the mathematical symbols $a < b$ and $a > b$ mean?

- a. $A < b$ means a is greater than b . $A > b$ means a is less than b .
- b. $A > b$ means a is less than b . $A < b$ means a is greater than b .
- c. $A < b$ means a is less than b . $A > b$ means a is greater than b .

Answer: option C

Explanation:-

This is very simple if we have liTTLe knowledge about algebra.

9. A basic multiplexer principle can be demonstrated through the use of a:

- a. Single-pole relay
- b. Dpdt switch
- c. Rotary switch
- d. Linear stepper

Answer: option C

10. How many inputs will a decimal-to-BCD encoder have?

- a. 4
- b. 8
- c. 10
- d. 16

Answer: option C

Explanation:-

Dec-BCD converter decimal values are ips ranges from 0-9 total 10 ips & BCD values represent by 4-bits so 4 o/p's.

11. A principle regarding most ic decoders is that when the correct input is present, the related output will switch:

- a. Active-high
- b. To a high impedance
- c. To an open
- d. Active-low

Answer: option D

12. What control signals may be necessary to operate a 1-line-to-16 line decoder?

- a. Flasher circuit control signal
- b. A low on all gate enable inputs
- c. Input from a hexadecimal counter
- d. A high on all gate enable circuits

Answer: option B

13. One multiplexer can take the place of:

- a. Several ssi logic gates
- b. Combinational logic circuits
- c. Several ex-nOR Gates
- d. Several ssi logic gates OR combinational logic circuits

Answer: option D

14. How many exclusive-nOR Gates would be required for an 8-bit comparator circuit?

- a. 4
- b. 6
- c. 8
- d. 10

Answer: option C

15. How many inputs are required for a 1-of-10 BCD decoder?

- a. 4
- b. 8
- c. 10
- d. 1

Answer: option A

Explanation:-

We can make 1 of 10 decoder with 4 inputs because the inputs are b1, b2, b3, b4 and outputs extends to d0 to d9.

OR

A is correct because 1-of-10 stands for BCD to decimal decoder.

OR

1 select line,

3 inputs- 000-11, 12, 13-0 to 9.

16. A BCD decoder will have how many rows in its truth table?

- a. 10
- b. 9
- c. 8
- d. 3

Answer: option A

17. How many possible outputs would a decoder have with a 6-bit binary input?

- a. 16
- b. 32
- c. 64
- d. 128

Answer: option C

Explanation:-

$$2^6=64$$

18. Most demultiplexers facilitate which type of conversion?

- a. Decimal-to-hexadecimal
- b. Single input, multiple outputs
- c. Ac to dc
- d. Odd parity to even parity

Answer: option B

19. The inputs/outputs of an analog multiplexer/Demultiplexer are:

- a. Bidirectional
- b. Unidirectional
- c. Even parity
- d. Binary-coded decimal

Answer: option A

20. Why can a CMOS ic be used as both a multiplexer and a Demultiplexer?

- a. It cannot be used as both.
- b. CMOS uses bidirectional switches.

Answer: option B

21. One application of a digital multiplexer is to facilitate:

- a. Data generation
- b. Serial-to-parallel conversion
- c. Parity checking
- d. Data selector

Answer: option D

22. The primary use for gray code is:

- a. Coded representation of a shaft's mechanical position
- b. Turning on/off software switches
- c. To represent the correct ASCII code to indicate the angular position of a shaft on rotating machinery
- d. To convert the angular position of a shaft on rotating machinery into hexadecimal code

Answer: option A

23. Why is a Demultiplexer called a data distributor?

- a. The input will be distributed to one of the outputs.
- b. One of the inputs will be selected for the output.

- c. The output will be distributed to one of the inputs.

Answer: option A

24. What is the status of the inputs s_0 , s_1 , and s_2 of the 74151 eight-line multiplexer in order for the output y to be a copy of input i_5 ?

- a. $S_0 = 0, S_1 = 1, S_2 = 0$
- b. $S_0 = 0, S_1 = 0, S_2 = 1$
- c. $S_0 = 1, S_1 = 1, S_2 = 0$
- d. $S_0 = 1, S_1 = 0, S_2 = 1$

Answer: option D

25. One way to convert BCD to binary using the hardware approach is:

- a. With msi ic circuits
- b. With a keyboard encoder
- c. With an alu
- d. Uart

Answer: option A

26. A microcontroller differs from a microprocessor in that it has several _____ ports and _____ built into its architecture, making it better suited for _____ applications.

Communication, proms, control

- a. Parallel, logic gates, processing
- b. Input/output, memory, control
- c. Data, memory, decoding

Answer: option C

27. How is an encoder different from a decoder?

- a. The output of an encoder is a binary code for 1-of- n input.
- b. The output of a decoder is a binary code for 1-of- n input.

Answer: option A

28. Why is the gray code more practical to use when coding the position of a rotating shaft?

- a. All digits change between counts.
- b. Two digits change between counts.
- c. Only one digit changes between counts.

Answer: option C

29. For the following conditions on a 7485 magnitude comparator, what will be the state of each of the three outputs?

$$A_0 = 0 \quad B_0 = 1 \quad I_a < b = 0$$

$A_1 = 1 \ B_1 = 0 \ I_a=b=1$

$A_2 = 1 \ B_2 = 0 \ I_a>b=0$

$A_3 = 0 \ B_3 = 0$

- a. **$A = b = 0, a < b = 0, a > b = 1$**
- b. **$A = b = 0, a < b = 1, a > b = 0$**
- c. **$A = b = 1, a < b = 0, a > b = 0$**
- d. **$A = b = 0, a < b = 0, a > b = 0$**

Answer: option A

Explanation:-

A -> 0110 = 6.

B -> 0001 = 1.

A>b.

30. When two or more inputs are active simultaneously, the process is called:

- a. First-in, first-out processing
- b. Priority encoding
- c. Ripple blanking
- d. First-in, first-out processing OR priority encoding

Answer: option B

31. A binary code that progresses such that only one bit changes between two successive codes is:

- a. Nine's-complement code
- b. 8421 code
- c. Excess-3 code
- d. Gray code

Answer: option D

32. Which of the following is not a weighted value positional numbering system:

- a. Hexadecimal
- b. Binary-coded decimal
- c. Binary
- d. Octal

Answer: option B

33. How many inputs are required for a 1-of-16 decoder?

- a. 2
- b. 4
- c. 8
- d. 16

Answer: option B

34. A truth table with output columns numbered 0–15 may be for which type of decoder ic?

- a. Hexadecimal 1-of-16
- b. Dual octal outputs
- c. Binary-to-hexadecimal
- d. Hexadecimal-to-binary

Answer: option A

35. In a BCD-to-seven-segment converter, why must a code converter be utilized?

- a. To convert the 4-bit BCD into 7-bit code
- b. To convert the 4-bit BCD into 10-bit code
- c. To convert the 4-bit BCD into gray code
- d. No conversion is necessary.

Answer: option A

36. How can the active condition (high or low) or the decoder output be determined from the logic symbol?

- a. A bubble indicates active-high.
- b. A bubble indicates active-low.
- c. A square indicates active-high.
- d. A square indicates active-low.

Answer: option B

37. If two inputs are active on a priority encoder, which will be coded on the output?

- a. The higher value
- b. The lower value
- c. Neither of the inputs
- d. Both of the inputs

Answer: option A

38. A circuit that responds to a specific set of signals to produce a related digital signal output is called a(n):

- a. BCD matrix
- b. Display driver
- c. Encoder
- d. Decoder

Answer: option C

39. How many 74184 BCD-to-binary converters would be required to convert two complete BCD digits to a binary number?

- a. 8
- b. 4
- c. 2
- d. 1

Answer: option C

40. How many select lines would be required for an 8-line-to-1-line multiplexer?

- a. 2
- b. 3
- c. 4
- d. 8

Answer: option B

Explanation:-

2^n input lines, n control lines and 1 output line available for mux.

Here 8 input line means 2^3 inputs. So 3 control lines possible.

TRUE/FALSE

1. In a multiplexer, the data select control inputs are responsible for determining which data input is selected to be transmitted to the data output line

- a. True
- b. False

Answer: option A

2. Before you can make a design you must decide if you want an active-high output.

- a. True
- b. False

Answer: option A

3. The microcontroller needs to use only three input lines to monitor eight separate points.

- a. True
- b. False

Answer: option A

4. A BCD is used for communication between a computer and a human being because it is too easy to deal with arithmetically.

- a. True
- b. False

Answer: option B

5. A Demultiplexer takes a dual input data value and routes it to one of several outputs.

- a. True
- b. False

Answer: option B

6. The digit bus and display bus are each just a common set of conductors shared by the digit storage registers and display segments.

- a. True
- b. False

Answer: option A

7. The basic comparator evaluates two binary strings bit by bit and always outputs a 1.

- a. True
- b. False

Answer: option B

8. In a priority encoder, the input with the highest priority is represented on the output.

- a. True
- b. False

Answer: option A

9. Exclusive-AND Gates are needed for conversions between gray code and binary code.

- a. True
- b. False

Answer: option B

10. The 74154 is a 1-of-16 decoder. It accepts a 4-bit binary input.

- a. True
- b. False

Answer: option A

15. MEMORY AND STORAGE

1. How many address bits are needed to select all memory locations in the 2118 16k × 1 ram?

- a. 8
- b. 10
- c. 14
- d. 16

Answer: option C

Explanation:-

$$16k = 16 \times 1024 = 2^4 \times 2^{10} = 2^{14}$$

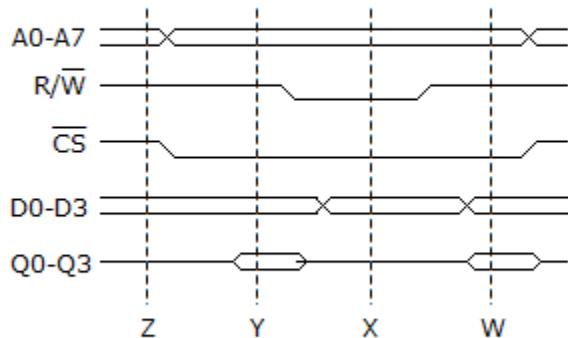
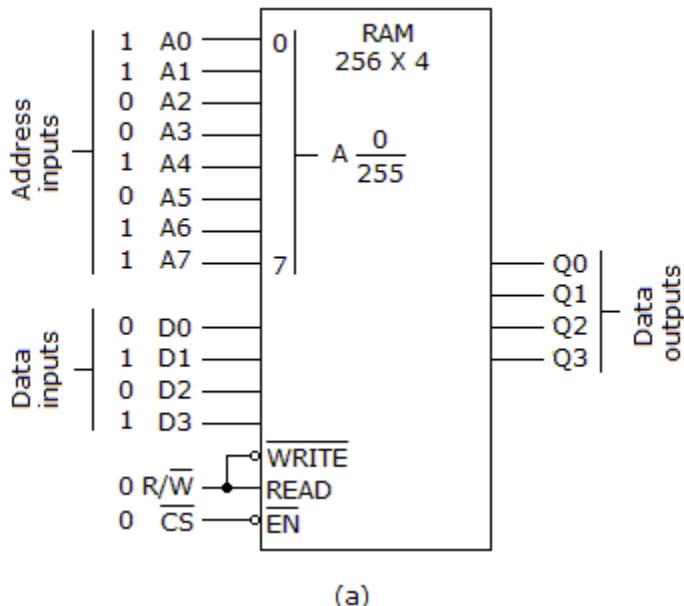
So total 14 address lines require.

2. The check sum method of testing a rom:

- a. Indicates if the data in more than one memory location is incorrect.
- b. Provides a means for locating and correcting data errors in specific memory locations.
- c. Allows data errors to be pinpointed to a specific memory location.
- d. Simply indicates that the contents of the rom are incorrect.

Answer: option D

3. Refer to the given figures (a) and (b). A logic analyzer is used to check the circuit in figure (a) and displays the waveforms shown in figure (b). The actual analyzer display shows all four data outputs, q_0-q_3 . The analyzer's cursor is placed at position x and all four of the data output lines show a low level output. What is wrong, if anything, with the circuit?



(b)

- a. Nothing is wrong, according to the display. The outputs are in the open state and should show zero output voltage.
- b. The circuit is in the read mode and the outputs, q_0-q_3 , should reflect the contents of the memory at that address. The chip is defective; replace the chip.
- c. The circuit is in the WRITE mode and should be writing the contents of the selected address to q_0-q_3 .
- d. The q_0-q_3 lines can be either low OR high, since the chip is in the Tri-State mode in which case their level is unpredictable.

Answer: option A

4. What is the meaning of ram, and what is its primary role?

- a. Readily available memory; it is the first level of memory used by the computer in all of its operations.

cd with chandra

- b. Random access memory; it is memory that can be reached by any sub- system within a computer, and at any time.**
- c. Random access memory; it is the memory used for short-term temporary data storage within the computer.**
- d. Resettable automatic memory; it is memory that can be used and then automatically reset, OR cleared, after being read from OR written to.**

Answer: option C

5. The storage element for a static ram is the _____.

- a. Diode**
- b. Resistor**
- c. Capacitor**
- d. Flip-Flop**

Answer: option D

Explanation:-

- 1.Static ram or SRAM stores data in flip-flops which retains data as long as SRAM is powered up.
- 2.Dynamic ram or dram stores in cells that depends on capacitors.

6. In a dram, what is the state of r/w during a read operation?

- a. Low**
- b. High**
- c. Hi-z**
- d. None of the above**

Answer: option B

Explanation:-

Read is high(1).

Write is low(0).

7. The condition occurring when two OR more devices try to write data to a bus simultaneously is called _____.

- a. Address decoding**
- b. Bus contention**
- c. Bus collisions**
- d. Address multiplexing**

Answer: option B

Explanation:-

Bus contention is an undesirable state of the bus of a computer, in which more than one memory mapped device **OR** the cpu is attempting to place output values onto the bus at once. Normally, integrated circuits that

connect to the bus are designed so that the likelihood of bus contention is nil provided that the chips are operated within their rated set-up times and so forth. However, if the bus is deliberately driven too fast, these setup times may be violated - leading to contention. Contention may also arise on a system whose memory mapping is programmable, and illegal values are written to the registers controlling the mapping.

8. Which is/are the basic refresh mode(s) for dynamic ram?

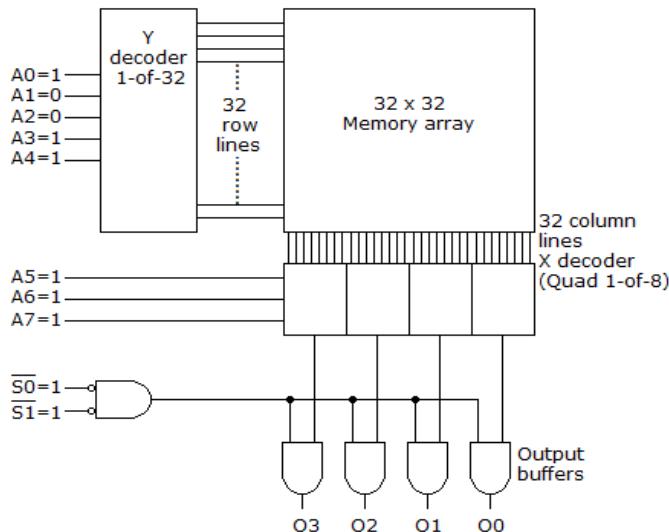
- a. Burst refresh
- b. Distributed refresh
- c. Open refresh
- d. Burst refresh and distributed refresh

Answer: option D

Explanation:-

- 1) Burst refresh - a series of refresh cycles are performed one after another until all the rows have been refreshed, after which normal memory accesses occur until the next refresh is required.
- 2) Distributed refresh - refresh cycles are performed at regular intervals, interspersed with memory accesses.

9. For the given circuit, what memory location is being addressed?



- a. 10111
- b. 249
- c. 5
- d. 157

Answer: option B

Explanation:-

$$(11111001)_b = (249)d$$

10. One of the most important specifications on magnetic media is the _____.

- a. Rotation speed
- b. Tracks per inch
- c. Data transfer rate
- d. Polarity reversal rate

Answer: option C

11 a 64-bit word consists of _____.

- a. 4 bytes
- b. 8 bytes
- c. 10 bytes
- d. 12 bytes

Answer: option B

Explanation:-

4 bits = 1 nibble

1 byte = 8 bits

4 bytes = 32 bits

64 bits = 8 bytes

12. Which of the following ram timing parameters determine its operating speed?

- a. T_{acc}
- b. T_{aa} and T_{acs}
- c. T_{co} and T_{od}
- d. T_{rc} and T_{wc}

Answer: option D

Explanation:-

Time required for read cycle and time required for write cycle.

13. The reason the data outputs of most rom ics are Tri-State outputs is to:

- a. Allow for three separate data input lines.
- b. Allow the bidirectional flow of data between the bus lines and the rom registers.
- c. Permit the connection of many rom chips to a common data bus.
- d. Isolate the registers from the data bus during read operations.

Answer: option C

14. Select the statement that best describes read-only memory (rom).

- a. Nonvolatile, used to store information that changes during system operation
- b. Nonvolatile, used to store information that does not change during system operation
- c. Volatile, used to store information that changes during system operation
- d. Volatile, used to store information that does not change during system operation

Answer: option B

Explanation:-

Rom is a permanent memory storage i.e, non volatile memory where as ram is volatile memory i.e, temporary storage.

15. How many $2k \times 8$ rom chips would be required to build a $16k \times 8$ memory system?

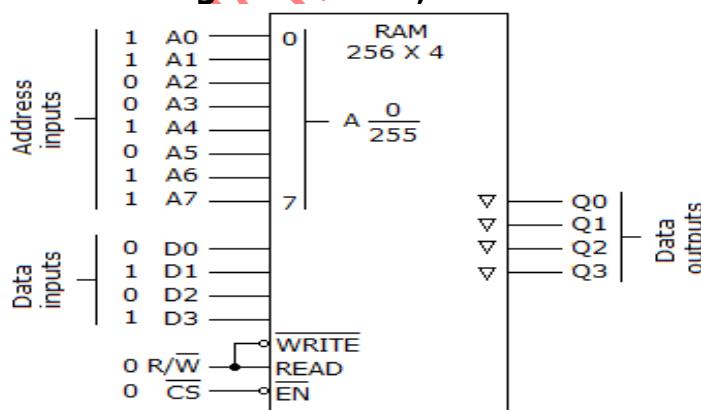
- a. 2
- b. 4
- c. 8
- d. 16

Answer: option C

Explanation:-

Since the required data bits are same so, we need only 8, $2k \times 8$ rom chips. These chips will be connected in parallel and only one chip will be active at a time through address lines (14 lines). Extra three lines will be used to active one chip among 8 chips.

16. For the given circuit, which of the following is correct?



- a. The number 5 is being written to the memory at address location 203.

- b. The chip has not been enabled, since the en terminal is 0; therefore, nothing will be written to the chip and the output is tri-stated.
- c. Decimal 10 is being written into memory location 211.
- d. The read/write line is low; therefore, decimal 5 is being stored at memory location 211.

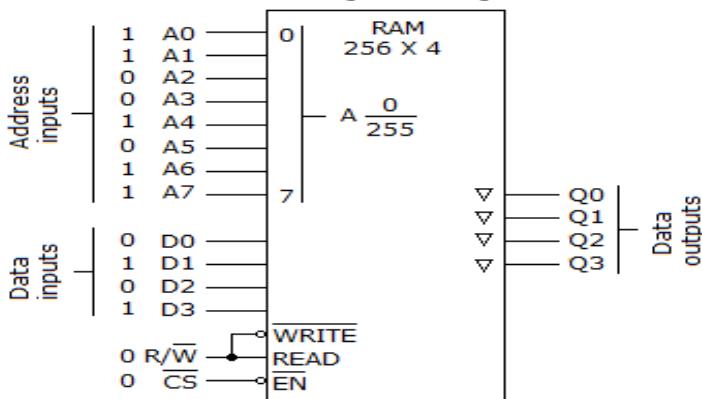
Answer: option C

Explanation:-

As the cs is active low when 0 is given as input it is activated, for read and write the input is 0.

So as write is active low it is activated and the data given is 1010(b) = 10(d) and is written onto memory as 1101001(b) = 211(d).

17. What is the significance of the inverted triangles on the outputs of the device in the given figure?



- a. They represent inverters and mean that the outputs are active-low.
- b. They represent buffers and mean that the outputs can drive 40 TTL loads, instead of the normal 10.
- c. It means that the outputs will be active only if a change has occurred at that memory location since the last read/write cycle.
- d. The outputs are tristated.

Answer: option D

18. What is the maximum time required before a dynamic ram must be refreshed?

- a. 2 ms
- b. 4 ms
- c. 8 ms
- d. 10 ms

Answer: option A

19. Which of the following best describes random-access memory (RAM)?

- a. A type of memory in which access time depends on memory location
- b. A type of memory that can be written to only once but can be read from an infinite number of times
- c. A type of memory in which access time is the same for each memory location
- d. Mass memory

Answer: option C

20. Why are roms called nonvolatile memory?

- a. They lose memory when power is removed.
- b. They do not lose memory when power is removed.

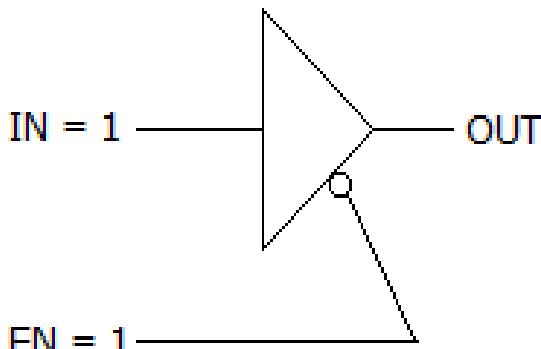
Answer: option B

21. A CD-Rom disk is created by applying heat to special chemicals on the disk and these chemicals reflect less light than the areas that are not burned, thus creating the same effect as a pit does on a regular cd.

- a. True
- b. False

Answer: option A

22. The device shown in the given figure is checked with a logic probe and the output is high.



- a. The device is working properly.
- b. For the input conditions shown the output should be low; the input is shorted to ground.
- c. For the input conditions shown the output should be neither high nor low; the device is shorted to V_{∞} .
- d. The device is probably alright; the problem is most likely caused by the stage connected to the output of the device.

Answer: option C

23. Which of the following best describes static memory devices?

- a. Memory devices that are magnetic in nature and do not require constant refreshing
- b. Memory devices that are magnetic in nature and require constant refreshing
- c. Semiconductor memory devices in which stored data will not be retained with the power applied unless constantly refreshed
- d. Semiconductor memory devices in which stored data is retained as long as power is applied

Answer: option D

24. Which is not a removable drive?

- a. Zip
- b. Jaz
- c. Hard
- d. Superdisk

Answer: option C

25. Which of the following best describes eproms?

- a. Eproms can be programmed only once.
- b. Eproms can be erased by uv.
- c. Eproms can be erased by shorting all inputs to the ground.
- d. All of the above.

Answer: option B

26. How many storage locations are available when a memory device has 12 address lines?

- a. 144
- b. 512
- c. 2048
- d. 4096

Answer: option D

Explanation:-

If a memory device has 'n' address lines, then it can access 2^n locations in memory.

Ie, $2^{12}=4096$

27. Fifo is formed by an arrangement of _____.

- a. Diodes
- b. Transistors
- c. Mos cells

d. Shift registers

Answer: option D

28. Why do most dynamic rams use a multiplexed address bus?

- a. It is the only way to do it.**
- b. To make it faster**
- c. To keep the number of pins on the chip to a minimum**

Answer: option C

29. Ccd stands for _____.

- a. Capacitor charging device**
- b. Capacitor-capacitor drain**
- c. Charged-capacitor device**
- d. Charge-coupled device**

Answer: option D

30. What is the major difference between SRAM and dram?

- a. Drams must be periodically refreshed.**
- b. Srams can hold data via a static charge, even with power off.**
- c. The only difference is the terminal from which the data is removed—from the fet drain OR source.**
- d. Dynamic rams are always active; static rams must reset between data read/write cycles.**

Answer: option A

31. Which of the following best describes volatile memory?

- a. Memory that retains stored information when electrical power is removed**
- b. Memory that loses stored information when electrical power is removed**
- c. Magnetic memory**
- d. Nonmagnetic**

Answer: option B

32. What is a major disadvantage of ram?

- a. Its access speed is too slow.**
- b. Its matrix size is too big.**
- c. It is volatile.**
- d. High power consumption**

Answer: option C

Explanation:-

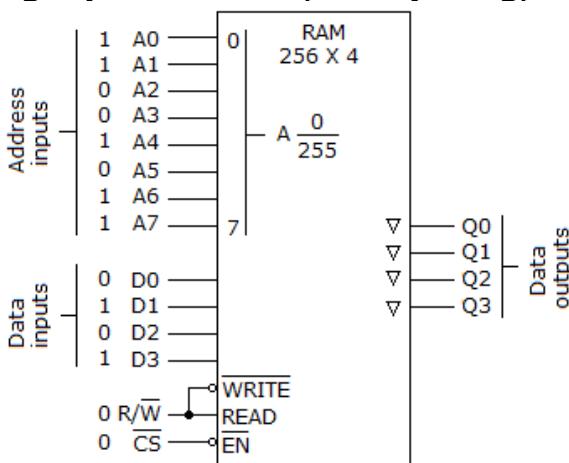
Ram is non volatile memory.

33. What two functions does a dram controller perform?

- a. Address multiplexing and data selection
- b. Address multiplexing and the refresh operation
- c. Data selection and the refresh operation
- d. Data selection and cpu accessing

Answer: option B

34. The ram circuit given below is suspected of being bad. A check with a logic probe shows pulse activity on all of the address lines and data inputs. The / line and inputs are forced high and the data output lines are checked with the logic probe. Q0, q2, and q3 show a dim indication on the logic probe; q1 indicates a high level on the logic probe. What, if anything, is wrong with the circuit?



- a. The q0, q2, and q3 output lines are open; the chip is defective.
- b. The q1 line appears to be shorted to V_{cc} ; replace the chip.
- c. The outputs should be active only when the / line is held low, so the circuit is behaving normally considering the fact that the line is high.
- d. The en input should be forced high and the outputs rechecked; if they are still giving the same indications as before, then the three outputs are definitely open and the ic will have to be replaced.

Answer: option B

35. Dynamic memory cells store a data bit in a _____.

- a. Diode
- b. Resistor
- c. Capacitor
- d. Flip-Flop

Answer: option C

37. Which is not part of a hard disk drive?

- a. Spindle
- b. Platter
- c. Read/write head
- d. Valve

Answer: option D

37. Roms retain data when the _____.

- a. Power is off
- b. Power is on
- c. System is down
- d. All of the above

Answer: option D

38. Typically, how often is dram refreshed?

- a. 2 to 8 ms
- b. 4 to 16 ms
- c. 8 to 16 μ s
- d. 1 to 2 μ s

Answer: option B

39. Which type of rom can be erased by an electrical signal?

- a. Rom
- b. Mask rom
- c. EEPROM
- d. EEPROM

Answer: option D

40. Suppose that a certain semiconductor memory chip has a capacity of $8k \times 8$. How many bytes could be stored in this device?

- a. 8,000
- b. 64,000
- c. 65,536
- d. 8,192

Answer: option D

Explanation:-

$$8k = 8 * 1024 = 8192$$

41. Data is written to and read from the disk via a magnetic _____ head mechanism in the floppy drive.

- a. Cylinder
- b. Read/write
- c. Recordable

d. Cluster

Answer: option B

42. What does the term "random access" mean in terms of memory?

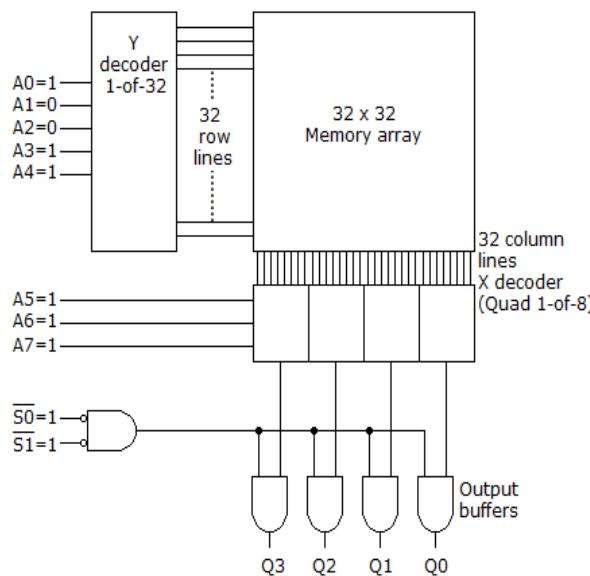
- a. Addresses must be accessed in a specific order.
- b. Any address can be accessed in any order.

Answer: option B

43. A 64-mbyte simm is installed into a system, but when a memory test is executed, the simm is detected as a 32-mbyte device. What is a possible cause?

- a. The memory module was not installed properly.
- b. The voltage on the memory module is incorrect.
- c. The most significant address line is stuck high OR low.
- d. The address decoder on the simm is faulty.

44. Refer the given figure. The outputs (q_0-q_3) of the memory are always low. The address lines (a_0-a_7) are checked with a logic probe and all are indicating pulse activity, except for a_3 , which shows a constant high, and a_7 , which shows a constant low; the select lines, $\overline{S_0}$ and $\overline{S_1}$ are checked and $\overline{S_0}$ shows pulse activity, while $\overline{S_1}$ indicates a constant high. What is wrong, and how can the memory be tested to determine whether it is defective OR if the external circuitry is defective?



- a. One of the inputs to the active-low select AND Gate may be stuck high for some reason; take both select lines low and check for pulse activity on the outputs, q_0-q_3 . If the outputs now respond, the problem is most likely in the program OR circuitry driving the select lines.

- b. The problem appears to be in the two address lines that never change levels; the problem is probably in the program driving the memory address bus.
- c. The output buffers are probably defective since they are all tied together; the common input line is most likely stuck low. Change the output buffer ic.
- d. Since no data appears to be getting through to the output buffers, the problem may be in the x decoder; change the x decoder ic.

Answer: option A

45. How many address lines would be required for a 2k x 4 memory chip?

- a. 8
- b. 10
- c. 11
- d. 12

Answer: option C

Explanation:-

$$2k = 2 * 1k = 2^1 * 2^{10} = 2^{11}$$

11 address lines are needed

46. When a ram module passes the checkerboard test it is:

- a. Able to read and write only 1s.
- b. Faulty
- c. Probably good.
- d. Able to read and write only 0s.

Answer: option C

47. Which type of rom has to be custom built by the factory?

- a. Rom
- b. Mask rom
- c. EEPROM
- d. EEPROM

Answer: option B

Explanation:-

Other all types of rom are programmable and can be programmed as per requirement but the mask rom is always programmed for specific application and it can't be reprogrammed.

48. What is the computer main memory?

- a. Hard drive and ram

- b. CD-ROM and hard drive
- c. Ram and rom
- d. CMOS and hard drive

Answer: option C

- 49. A major disadvantage of the mask rom is that it:**
- a. Is time consuming to change the stored data when system requirements change
 - b. Is very expensive to change the stored data when system requirements change
 - c. Cannot be reprogrammed if stored data needs to be changed
 - d. Has an extremely short life expectancy and requires frequent replacement

Answer: option C

- 50. The periodic recharging of dram memory cells is called _____.**

- a. Multiplexing
- b. Bootstrapping
- c. Refreshing
- d. Flashing

Answer: option C

- 51. Which of the following is normally used to initialize a computer system's hardware?**

- a. Bootstrap memory
- b. Volatile memory
- c. External mass memory
- d. Static memory

Answer: option A

- 52. What is the difference between static ram and dynamic ram?**

- a. Static ram must be refreshed, dynamic ram does not.
- b. There is no difference.
- c. Dynamic ram must be refreshed, static ram does not.

Answer: option C

Explanation:-

Dynamic ram must be refreshed because it made up of capacitor, and capacitor required refresh. Static ram made up of flip flop and flip flop donot required refresh.

53. Microprocessors and memory ics are generally designed to drive only a single TTL load. Therefore, if several inputs are being driven from the same bus, any memory ic must be _____.

- a. Buffered
- b. Decoded
- c. Addressed
- d. Stored

Answer: option A

54. What are the typical values of t_{oe} ?

- a. 10 to 20 ns for bipolar
- b. 25 to 100 ns for NMOS
- c. 12 to 50 ns for CMOS
- d. All of the above

Answer: option D

55. Which type of rom can be erased by uv light?

- a. Rom
- b. Mask rom
- c. EEPROM
- d. EEPROM

Answer: option C

56. Which of the following is not a type of memory?

- a. Ram
- b. Rom
- c. Feprom
- d. EEPROM

Answer: option C

57. How many address bits are required for a 4096-bit memory organized as a 512×8 memory?

- a. 2
- b. 4
- c. 8
- d. 9

Answer: option D

Explanation:-

$2^{\text{address line}} * \text{data line} = \text{memory location.}$

$$2^9 * 8 = 512 * 8.$$

Answer is 9.

58. In general, the _____ have the smallest bit size and the _____ have the largest.

- a. Eeproms, flash
- b. SRAM, mask rom
- c. Mask rom, SRAM
- d. Dram, PROM

Answer: option A

59. Advantage(s) of an EEPROM over an EEPROM is/are:

- a. The EEPROM can be erased with ultraviolet light in much less time than an EEPROM
- b. The EEPROM can be erased and reprogrammed without removal from the circuit
- c. The EEPROM has the ability to erase and reprogram individual words
- d. The EEPROM can be erased and reprogrammed without removal from the circuit, and can erase and reprogram individual words

Answer: option D

60. The mask rom is _____.

- a. Permanently programmed during the manufacturing process
- b. Volatile
- c. Easy to reprogram
- d. Extremely expensive

Answer: option A

61. How many $1k \times 4$ ram chips would be required to build a $1k \times 8$ memory system?

- a. 2
- b. 4
- c. 8
- d. 16

Answer: option A

62. Which of the following memories uses a mos capacitor as its memory cell?

- a. SRAM
- b. Dram
- c. Rom
- d. Fifo

Answer: option B

63. Which of the following faults will the checkerboard pattern test for in ram?

- a. Short between adjacent cells**
- b. Ability to store both 0s and 1s**
- c. Dynamically introduced errors between cells**
- d. All of the above**

Answer: option D

64. On a CD-ROM, _____ are raised areas representing a 1.

- a. Mounds**
- b. Lands**
- c. Holes**
- d. Pits**

Answer: option B

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16.PROGRAMMABLE LOGIC DEVICE

1.The difference between a PLA and a PAL is:

- a. The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.
- b. The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane.
- c. The PAL has more possible product terms than the PLA.
- d. PALs and PLAs are the same thing.

Answer: option A

Explanation:-

In PLA the OR plane as well as the AND plane is varied according to the input and output while in PAL the OR plane is fixed and the AND plane is programmable.

2.ALM is the acronym for _____.

- a. Array logic matrix
- b. Arithmetic logic module
- c. Asynchronous local modulator
- d. Adaptive logic module

Answer: option D

3.The GAL16V8 has:

- a. 16 dedicated inputs.
- b. 8 special function pins.
- c. 8 pins that are used as inputs OR outputs.
- d. All of the above

Answer: option C

4.PALs tend to execute _____ logic.

- a. Sap
- b. SOP
- c. PLA
- d. spd

Answer: option B

SOP means sum-of-products.

4.How many pins are in an edf10k70 package?

- a. 70

- b. 140
- c. 240
- d. 532

Answer: option C

5.A GAL is essentially a _____.

- a. Non-reprogrammable PAL
- b. PAL that is programmed only by the manufacturer
- c. Very large PAL
- d. Reprogrammable PAL

Answer: option D

Explanation:-

GAL = generic array logic.

6.What is an otp device?

- a. Optical transporting port
- b. Octal transmitting pixel
- c. Operational topical portable
- d. One-time programmable

Answer: option D

7.How many product terms can a max+plus ii compiler borrow from adjacent macrocells in the same lab?

- a. 0
- b. 5
- c. 10
- d. 20

Answer: option B

8.Each programmable array logic (PAL) gate product is applied to an OR Gate and, if combinational logic is desired, the product is ored and then:

- a. The polarity fuse is restored
- b. Sent to an inverter for output
- c. Sent immediately to an output pin
- d. Passed to the and function for output

Answer: option B

9._____ are used at the inputs of PAL/GAL devices in order to prevent input loading from a large number of AND Gates.

- a. Simplified AND Gates
- b. Fuses
- c. Buffers

d. Latches

Answer: option C

10.A(n) _____ consists of a programmable array of AND Gates that connects to a fixed array of OR Gates and is usually otp.

- a. GAL
- b. CPLD
- c. PAL
- d. SPLD

Answer: option C

Explanation:-

PAL is a fixed device, whereas PLA is variable device.x

11.What is another name for digital circuitry called sequential logic?

- a. Logic macro-cell
- b. Logic array
- c. Flip-Flop memory circuitry
- d. Inverter

Answer: option C

12.When did the first PLD appear?

- a. More than 10 years ago
- b. More than 20 years ago
- c. More than 30 years ago
- d. More than 40 years ago

Answer: option C

13.Splds, cplds, and FPGA'S are all which type of device?

- a. PAL
- b. PLD
- c. EEPROM
- d. SRAM

Answer: option B

14.Cascade chains are closely associated with _____.

- a. Clbs
- b. SOP function
- c. Logic expansion
- d. All of the above

Answer: option D

15.FPLA is:

- a. A non memory programmable device.

- b. A programmable AND array.
- c. A programmable OR array
- d. All of the above

Answer: option D

16.A(n) _____ is a section of embedded logic that is commonly found in FPGA'S.

- a. LUT
- b. core
- c. DSP
- d. pi

Answer: option B

17.In a flex10k, what two outputs will the LE produce?

- a. The lab and the fast track
- b. On and off
- c. Hi-z and on
- d. Hi-z and off

Answer: option A

18.What is the major downfall of microprocessor/DSP systems?

- a. Speed—they are too fast
- b. Speed—they are too slow
- c. Too much flexibility
- d. Not enough flexibility

19.ASIC stands for:

- a. Advanced speed integrated circuit.
- b. Advanced standard integrated circuit.
- c. Advanced specific integrated circuit.
- d. Advanced speedy integrated circuit.

Answer: option C

20.A look-up table is simply a truth table with all the possible output connections listed with their desired input response.

A)True

B)False

Answer: option B

21.The final step in the device programming sequence is _____.

- a. Compiling
- b. Downloading
- c. Simulation
- d. Synthesis

Answer: option B

22. Most look-up tables in field-programmable gate arrays (fgpas) use _____ inputs, resulting in _____ possible outputs.

- a. 4,16
- b. 8,16
- c. 4,12
- d. 6,12

Answer: option A

23. What is the defining difference between microprocessor/DSP systems and other digital systems?

- a. The digital system follows a programmed sequence of instructions that the designer specified.
- b. The microprocessor follows a programmed sequence of instructions that the designer specified.
- c. The digital system is faster.
- d. The microprocessor/DSP is faster.

Answer: option A

24. What is the defining difference between microprocessor/DSP systems and other digital systems?

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- b. The microprocessor follows a programmed sequence of instructions that the designer specified.
- c. The digital system is faster.
- d. The microprocessor/DSP is faster.

Answer: option A

25. Why have pld's taken over so much of the market?

- a. One PLD does the work of many ICs.
- b. The pld's are cheaper.
- c. Less power is required.
- d. All of the above

Answer: option D

26. CLB is the acronym for _____.

- a. Configurable logic block
- b. Configurable logic buffer
- c. Critical logic buffer
- d. Constant logic buffer

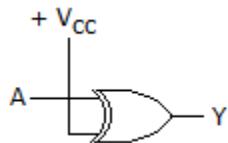
Answer: option A

27.What can the GAL22v10 do that the GAL16v8 cannot?

- a. It has an extra-large array.
- b. It is in-system programmable.
- c. It has twice the special function pins.
- d. All of the above

Answer: option B

28.The output of this circuit is always _____.



- a. 1
- b. 0
- c. A bar
- d. A

Answer: option C

29.A circuit that implements a combinational logic function by storing a list of output values that correspond to all possible input combinations is a(n) _____.

- a. Output logic macro-cell
- b. Look-up table
- c. Parallel logic expander
- d. Logic element

Answer: option B

30.By adding an OR Gate to a simple programmable logic device (SPLD) the foundation for a(n) _____ is made possible.

- a. PAL
- b. PLA
- c. CPLD
- d. EEPROM

Answer: option A

Explanation:-

But PAL has only programmable and plane.

31.What does the Altera flex10k PLD use in place of AND & OR arrays?

- a. Nothing, it uses and and OR arrays.
- b. Look-up tables
- c. SRAM-based memory
- d. HPLD architecture

Answer: option B

32.Pia is an acronym for _____.

- a. Programmable interface array
- b. Post integrated array
- c. Programmable input array
- d. Programmable interconnect array

Answer: option D

33.Which one of the following is an embedded function of the stratix ii FPGA?

- a. And-OR logic
- b. Programmable SOP
- c. Digital signal processing
- d. None of the above

Answer: option C

34.In an olmc, where does the fmux signal go?

- a. Omux
- b. D Flip-Flop
- c. Matrix
- d. PAL

Answer: option C

35.Which of the following testing procedures has one OR more external moving parts?

- a. Bed-of-nails
- b. Flying probe
- c. Extest
- d. Boundary scan

Answer: option B

36.Field-programmable gate arrays (fgpas) use _____ memory technology, which is _____.

- a. Dram, nonvolatile
- b. SRAM, nonvolatile
- c. SRAM, volatile
- d. Ram, volatile

Answer: option C

37.A PAL16I8 has:

- a. 10 inputs and 8 outputs.
- b. 8 inputs and 8 outputs.
- c. 16 inputs and 16 outputs.

d. 16 inputs and 8 outputs.

Answer: option A

38.How many times can a GAL be erased and reprogrammed?

- a. 0**
- b. At least 100**
- c. At least 1000**
- d. Over 10,000**

Answer: option B

39.Mpga stands for:

- a. Mass produced gated array.**
- b. Morgan-phillips gated array.**
- c. Memory programmed rom.**
- d. Mask programmed rom.**

Answer: option D

40.Which of the following increases the number of product terms by borrowing unused product from other macrocells?

- a. Shared expander**
- b. Parallel expander**
- c. Series expander**
- d. Slice expander**

Answer: option B

41.Which is a mode of operation of the GAL16v8?

- a. Simple mode**
- b. Complex mode**
- c. Registered mode**

Answer: option D

42.Which of the following testing procedures uses the jtag ieee standard?

- a. Bed-of-nails**
- b. Flying probe**
- c. Extest**
- d. boundary scan**

Answer: option D

43.The macro cells in a PAL/GAL are located _____.

- a. After the programmable and arrays**
- b. Ahead of the programmable and arrays**
- c. At the input terminals**
- d. At the output terminals**

Answer: option A

44.The content of a simple programmable logic device (PLD) consists of:

- a. Fuse-link arrays
- b. Thousands of basic logic gates
- c. Advanced sequential logic functions
- d. Thousands of basic logic gates and advanced sequential logic functions

Answer: option D

45.Which is a major digital system category?

- a. Standard logic devices
- b. Asics
- c. Microprocessor/DSP devices
- d. All of the above

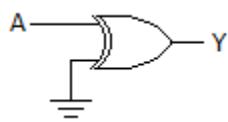
Answer: option D

46.What is the input/output pin configuration of the GAL22v10?

- a. 10 output pins and 12 input pins\
- b. 2 special-purpose pins
- c. 8 pins that are either inputs OR outputs
- d. All of the above

Answer: option A

47.The output of this circuit is always _____.



- a. 1
- b. 0
- c. A bar
- d. A

Answer: option C

Explanation:-

$$\begin{aligned} A \text{XOR} .0 &= a. \\ A \text{XOR} .1 &= a'. \end{aligned}$$

48.What does a dot mean when placed on a PLD circuit diagram?

- a. A point that is programmable
- b. A point that cannot change
- c. An intersection of logic blocks

d. An input OR output point

Answer: option B

49.FPGA is the acronym for _____.

- a. Flexible programming [of] generic assemblies**
- b. Field programmable generic array**
- c. Field programmable gate array**
- d. Field programmable generic assembly**

Answer: option C

50.How many combinations are handled in an LUT?

- a. 4**
- b. 8**
- c. 16**
- d. 32**

Answer: option C

51.Which of the following is true?

- a. Altera uses PAL architecture and xilinx uses PLA architecture.**
- b. Altera uses PAL architecture and xilinx uses PAL architecture.**
- c. Altera and xilinx uses both PAL architecture.**
- d. Altera and xilinx uses both PLA architecture.**

Answer: option A

52.What is the status of a Tri-State output buffer on a max7000s family device?

- a. It is permanently enabled OR disabled.**
- b. It is controlled by one of the two global output enable pins.**
- c. It is controlled by other inputs OR functions generated by other macrocells.**
- d. All of the above**

Answer: option D

53.GAL is an acronym for _____.

- a. Generic array logic**
- b. General array logic**
- c. Giant array logic**
- d. Generic analysis logic**

Answer: option A

54.What gives a GAL its flexibility?

- a. Its speed**
- b. Its reprogrammableEEPROM**
- c. Its large logic arrays**

d. Its programmable olmcs

Answer: option D

55.What programmable technology is used in FPGA devices?

- a. SRAM**
- b. flash**
- c. antifuse**
- d. All of the above**

Answer: option D

56.What is an epm7128s?

- a. An Altera max7000s CPLD**
- b. An Altera up2**
- c. A devry esoc**
- d. A bsr pl dt-2**

Answer: option A

57.An SPLD listed as 22v10 has _____.

- a. 10 inputs, 10 outputs, and requires a 22 v power source**
- b. 11 inputs, 11 outputs, and requires a 10 v power source**
- c. 22 inputs, 10 outputs**
- d. 10 inputs, 22 outputs**

Answer: option C

58.The Altera max 7000 series _____.

- a. Uses an e²prom process technology**
- b. Can have between 2 and 16 labs and i/o control blocks**
- c. Is available with dc supply voltages between 2.5 v and 5 v**
- d. All of the above**

Answer: option D

59.A macro-cell basically contains _____.

- a. A programmable and-OR Gate array and some input buffers**
- b. An OR-gate array and some output logic**
- c. An and-OR Gate array and some output logic**
- d. Licensed programming**

Answer: option B

**60.The complex programmable logic device (CPLD) features a(n)
_____ type of memory.**

- a. Volatile**
- b. Nonvolatile**
- c. EEPROM**
- d. VolatileEEPROM**

Answer: option B

61.How many macrocells are in a max700s lab?

- a. 8
- b. 16
- c. 32
- d. 64

Answer: option B

62.Which is not a type of PLD?

- a. SPLD
- b. HPLD
- c. CPLD
- d. FPGA

Answer: option B

63.An SPLD listed as 16h8 would have _____.

- a. Active-high outputs
- b. Active-low outputs
- c. Variable-level outputs
- d. Latches at the outputs

Answer: option A

64.Which type of PLD could be used to program basic logic functions?

- a. PLA
- b. PAL
- c. CPLD
- d. All of the above

Answer: option D

65.The complex programmable logic device (CPLD) contains several PAL-type simple programmable logic devices (splds) called:

- a. Macro cells
- b. Microcells
- c. And/OR arrays
- d. Fuse-link arrays

Answer: option A

66.Which is not a part of a GAL16v8's olmc?

- a. Tsmux
- b. Omux
- c. Fmux
- d. Psmux

Answer: option D

67.What is PROM?

- a. SPLD
- b. QPLD
- c. HPLD
- d. PLD

Answer: option D

68.A slice consists of _____.

- a. Only two logic cells
- b. Between 2 and 8 logic cells
- c. Up to 16 logic cells
- d. A single CLB

Answer: option A

69.Product terms are the outputs of which type of gate within a PLD array?

- a. OR
- b. XOR
- c. AND
- d. Flip-Flop

Answer: option C

Fill in tthe blanks

1.The jtag signals are named tdi, tdo, tms, and tck.

A)True

B)False

Answer: option A

2.The programming technologies that are used in CPLD devices are all nonvolatile.

A)True

B)False

Answer: option A

3.Generally, plds can be described as being one of four different types.

A)True

B)False

Answer: option B

4.The programming technologies that are used in FPGA devices include SRAM, flash, and antifuse, with flash being most common.

- A)True
- B)False

Answer: option B

5.The Altera upix educational development board contains an ep10k60 device in a 280-pin package.

- A)True
- B)False

Answer: option B

6.SPLD is a program language used by PLD software.

- A)True
- B)False

Answer: option B

7.The Boolean sum of the four product terms is called the sum-of-products.

- A)True
- B)False

Answer: option A

8.CPLDS and FPGA'S are often referred to as high-capacity programmable logic devices (HCPLDS).

- A)True
- B)False

Answer: option A

9.In a PLD, a blown fuse at an OR Gate is a low and a blown fuse at an AND Gate is a high.

- A)True
- B)False

Answer: option A

10.The hard core portions of FPGA'S are reprogrammable in the field.

- A)True
- B)False

Answer: option A

11.The PLA has a programmable and array and a programmable OR array.

- A)True

B)False

Answer: option A

12.The PAL structure is able to perform any sum-of-products (SOP) operation.

A)True

B)False

Answer: option A

13.Using a hardware solution for your digital system design is always faster than a software solution.

A)True

B)False

Answer: option A

14.A GAL is a programmable/reprogrammable PAL.

A)True

B)False

Answer: option A

15.Alterra corporation and xilinx corporation are the two leading PLD manufacturers.

A)True

B)False

Answer: option A

16.The PAL has an AND and OR structure similar to a PROM, but in the PAL the inputs to the AND Gates are programmable, whereas the inputs to the OR Gate are hard-wired.

A)True

B)False

Answer: option A

17.Gate arrays are ULSI circuits that offer hundreds of thousands of gates.

A)True

B)False

Answer: option A

18.Schematic capture is a process performed by PLD software.

A)True

B)False

Answer: option A

19.An expensive form of programmable logic is SPLD.

- A)True
- B)False

Answer: option B

20.Most PAL devices have a Tri-State buffer driving the input pins.

- A)True
- B)False

Answer: option B

21.The schematic editor allows you to connect with predefined logic symbols.

- A)True
- B)False

Answer: option A

22.VHDL code is divided into three sections: library declaration, entity declaration, and architecture body.

- A)True
- B)False

Answer: option A

23.All inputs to the max7000s device and all macro-cell outputs feed the pia.

- A)True
- B)False

Answer: option A

24.Sum-of-products is two OR more product terms that are nanded together.

- A)True
- B)False

Answer: option B

25.Most complex digital designs include a mix of different hardware categories.

- A)True
- B)False

Answer: option A

26.The Altera flex10k family uses a look-up table (LUT) architecture.

- A)True
- B)False

Answer: option A

27.PIDs cannot meet all the possible requirements of complex digital circuitry.

- A)True
- B)False

Answer: option B

28.The four input-only pins found on devices in the max7000s family can be configured as specific high-speed control signals OR as general user inputs.

- A)True
- B)False

Answer: option A

29.In the olmc of a GAL16v8, the fmux selects the signal that is fed into the input matrix.

- A)True
- B)False

Answer: option A

30.A PAL consists of an array of fixed AND Gates that are connected to a programmable array of OR Gates.

- A)True
- B)False

Answer: option B

31.The max+plus ii compiler will automatically program a macro-cell to borrow up to six product terms from each of three adjacent macrocells in the same lab.

- A)True
- B)False

Answer: option B

32.Antifuse devices are volatile.

- A)True
- B)False

Answer: option B

33.The major digital system categories include Boolean logic, asics, and microprocessor/DSP devices.

- A)True
- B)False

Answer: option B

34.The GAL chip uses an EEPROM array that is erasable and reprogrammable at least 1000 times.

- A)True
- B)False

Answer: option B

35.PLds did not gain widespread acceptance with digital until the mid-1980s, when a device called a PAL was introduced.

- A)True
- B)False

Answer: option B

36.Expanders make it possible to increase the number of terms in a programmable SOP operation.

- A)True
- B)False

Answer: option A

37.The GAL16v8 has eight dedicated input pins.

- A)True
- B)False

Answer: option A

38.In the flex10k device, the Ie can produce two outputs to drive local (lab) and global (fast track) interconnects on the chip.

- A)True
- B)False

Answer: option A

39.The architecture of a PAL differs slightly from that of a PROM.

- A)True
- B)False

Answer: option A

40.LUT is an acronym for look-up table.

- A)True
- B)False

Answer: option A

41.A PAL uses a programmable OR array followed by a fixed AND array.

- A)True
- B)False

Answer: option B

42.The SRAM technology is volatile.

- A)True
- B)False

Answer: option A

43.The major structures of the max7000s are the logic array block (lab) and the programmable intermediate array (pia).

- A)True
- B)False

Answer: option B

44.All i/o pins in the max7000s family have a Tri-State buffer.

- A)True
- B)False

Answer: option A

45.Based on the high-density architecture of logic cells, flex10k devices are generally classified as hcplds.

- A)True
- B)False

Answer: option B

46.A CPLD is basically a simplified PLD.

- A)True
- B)False

Answer: option B

47.The GAL22v10 has 12 outputs pins and 10 input pins.

- A)True
- B)False

Answer: option B

Explanation:-

It has 12 input pins & 10 output pins.

48.The GAL16v8 has 32 input variables.

- A)True
- B)False

Answer: option B

49.Xilinx software uses triangular symbols called buffers to define pins as input OR output.

- A)True

B)False

Answer: option B

FILL UP THE BLANKS

1.A unit of logic in an FPGA that is made up of multiple smaller logic modules and a local programmer interconnect that is used to connect internal logic modules is called a _____.

- a) Bed-of-nails
- b) Boundary scan
- c) CLB
- d) CPLD

Answer: option C

2.In a flex10k device, the carry chain provides a fast carry forward function between _____.

- a) Luts
- b) Eabs
- c) Les
- d) Labs

Answer: option C

3.The Boolean expression $(a + b)(c + d)$ is an example of _____.

- a) Lab
- b) LUT
- c) SOP
- d) POS

Answer: option D

4.An Altera flex10k device uses a(n) _____ architecture.

- a) OR array
- b) And array
- c) OR and and array
- d) Look-up table

Answer: option D

5.The _____ is the most popular standard logic device family today.

- a) TTL
- b) CMOS
- c) ECL
- d) None of the above

Answer: option B

6.A GAL22v10 _____.

- a) Has up to 32 inputs and 10 outputs
- b) Is a type of SPLD
- c) Has 10 inputs and 22 outputs
- d) Is downloadable from the manufacturer's web site

Answer: option B

7. Most FPGA logic modules utilize a(n) _____ approach to create the desired logic functions.

- a) And array
- b) Look up table
- c) OR array
- d) And and OR array

Answer: option B

8. An epm 7128s in a _____ pqfp package has 12 i/o per lab plus 4 additional input-only pins for a total of 100 pins.

- a) 100-pin
- b) 120-pin
- c) 140-pin
- d) 160-pin

Answer: option D

9. A macro-cell is _____.

- a) Part of a PAL OR GAL
- b) A type of one-time programmable SPLD
- c) An example of intellectual property
- d) A logic array block

Answer: option A

10. The final step in a design flow in which the logic design is implemented in the target device is called _____.

- a) Design entry
- b) Simulation
- c) Downloading
- d) Compiling

Answer: option C

11. In the GAL16v8, the _____ controls the Tri-State buffer's enable input.

- a) Fmux
- b) omux
- c) ptmux
- d) tmux

Answer: option D

12.All inputs to the max7000s device and all macro-cell outputs feed the _____.

- a) LUT
- b) Pia
- c) Lab
- d) Pia and lab

Answer: option B

13.In the GAL16v8, the _____ selects the signal that is fed back into the input matrix.

- a) Fmux
- b) omux
- c) ptmux
- d) tmux

Answer: option A

14.An application program in the development software package that controls the operation of the software is called a _____.

- a) Compiler
- b) Bed-of-nails
- c) Boundary scan
- d) Primitive

Answer: option A

15.Most complex digital designs include _____.

- a) Standard logic devices
- b) ASIC devices
- c) Microprocessor/DSP devices
- d) A mix of different hardware categories

Answer: option D

16.Using a hardware solution for a digital system is always _____ than a software solution.

- a) Slower
- b) Harder
- c) Easier
- d) Faster

Answer: option D

17.The programming technologies that are used in FPGA devices include SRAM, flash, and antifuse, with _____ being the most common.

- a) SRAM

- b) flash
- c) Antifuse
- d) SRAM and flash

Answer: option A

18.A method for the automated testing of printed circuit boards is called a(n) _____.

- a) Bed-of-nails
- b) LUT
- c) CLB
- d) CPLD

Answer: option A

19.In a max7000s device, when an i/o pin is configured as an input, the associated macro-cell can be used for _____.

- a) Buried logic
- b) Another output
- c) Extra speed
- d) In-system testing

Answer: option A

20.The process OR sequence of all operations carried out to ultimately program a target device is called the _____.

- a) Graphic entry
- b) Lab
- c) Downloading
- d) Design flow

Answer: option D

21.Full custom ics can operate at _____ and require the _____.

- a) Lowest speed, largest die area
- b) Lowest speed, smallest die area
- c) Highest speed, largest die area
- d) Highest speed, smallest die area

Answer: option D

22.Gated arrays are _____ circuits that offer hundreds of thousands of gates.

- a) VLSI
- b) Full custom
- c) LSI
- d) ULSI

Answer: option D

23.The max+plus ii compiler will automatically program a macro-cell to borrow up to _____ product terms from each of the 3 adjacent macrocells in the same lab.

- a) 4
- b) 5
- c) 6
- d) 7

Answer: option B

24.A complex programmable logic device that consists of multiple SPLD arrays with programmable interconnections is called a _____.

- a) Bed-of-nails
- b) Boundary scan
- c) CLB
- d) CPLD

Answer: option D

25.Design costs for standard cell asics are _____ those for mpgas.

- a) Lower than
- b) About the same as
- c) Higher than
- d) None of the above

Answer: option C

26.The _____ can generate any possible logic function of the input variables because it generates every possible product term.

- a) GAL
- b) SOP
- c) PROM
- d) lab

Answer: option C

27.The epm 7128s is a(n) _____ device.

- a) PLD
- b) jtag
- c) EEPROM
- d) isp

Answer: option D

28.The distinction between cplds and FPGA'S is _____.

- a) Well known

- b) Very small
- c) Often fuzzy
- d) Very large

Answer: option C

Explanation:-

Complex programmable logic device.

Field programmable gate array.

29. _____ is a mature technology consisting of numerous subfamilies that have been developed over many years of use.

- a) TTL
- b) CMOS
- c) ECL
- d) None of the above

Answer: option A

30. The flexibility of the GAL16v8 is in its _____.

- a) And/OR array
- b) D flip-flops
- c) Programmable output logic macro cells
- d) EEPROM

Answer: option C

31. The field programmable logic array was the first _____ programmable logic device.

- a) Understandable
- b) Logic array
- c) Multifunction
- d) Nonmemory

Answer: option D

32. The GAL16v8 has architecture that is very similar to the _____ device.

- a) PAL
- b) PROM
- c) PLD
- d) SPLD

Answer: option A

33. In a GAL16v8, the d flip-flops contained in the olmcs have _____ and _____.

- a) Asynchronous reset, synchronous preset
- b) Asynchronous preset, synchronous reset

- c) Asynchronous clear, synchronous set
- d) Asynchronous set, synchronous clear

Answer: option A

34.In a programmable logic device circuit diagram, the inputs to each of the OR Gates are designated by _____.

- a) A dot
- b) A bus
- c) A single line
- d) 4 inputs

Answer: option C

35.The SPLD classification includes the _____ PLD devices.

- a) Earliest
- b) Smallest
- c) Largest
- d) Newest

Answer: option A

36.In the max7000s device up to _____ signals can feed each lab from the pia.

- a) 0
- b) 18
- c) 36
- d) 72

Answer: option C

37.Flex10k devices are generally classified as _____.

- a) Plds
- b) FPGA'S
- c) Hcplds
- d) Cplds

Answer: option B

38.The major structures in the max7000s are the _____ and _____.

- a) LUT, pia
- b) Fmux, lab
- c) Lab, pia
- d) LUT, fmux

Answer: option C

39.Four subcategories of ASIC devices are available to create digital systems. These are plds, gate arrays, standard cells, and _____.

- a) Hcplds**
- b) Full custom**
- c) GAL**
- d) Fplds**

Answer: option B

40. The Boolean expression $ab + cd$ is an example of _____.

- a) PAL**
- b) GAL**
- c) SOP**
- d) POS**

Answer: option C

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17. INTERFACING TO THE ANALOG WORLD

1.If an analog signal is to be converted to an 8-bit resolution, how many comparators are used in a parallel-encoded ADC?

- a) 127
- b) 128
- c) 255
- d) 256

Answer: option D

Explanation:-

Answer is 255. In parallel type means flash type **ADC** we need $(2^n) - 1$ comparators.

2.A transducer is a device that:

- a) Converts a physical variable to an electrical variable
- b) Converts analog data to meaningful data
- c) Controls a physical variable
- d) Stores digital data and then processes that data according to a set of specified instructions

Answer: option A

3.How many different voltages can be output from a DAC with a 6-bit resolution?

- a) 6
- b) 16
- c) 32
- d) 64

Answer: option D

Explanation:-

2^n

where n=no of bits

Equal to number of comparator.

4.A 4-bit r/2r d/a converter has a reference of 5 v. What is the analog output for the input code 0101?

- a) 3.125 v
- b) .3125 v
- c) .78125 v

d) -3.125 v

Answer: option D

Explanation:-

For 4 bit **DAC** $v_{out} = -(5*0/16 + 5*1/8 + 5*0/4 5*1/2)$.

$V_{out} = -(5/8 + 5/2)$.

$V_{out} = -(25/8)$.

$V_{out} = -3.125$.

5.Which of the following describes the basic operation of a single-slope a/d converter.

- a) The input voltage is used to set the frequency of a voltage-controlled oscillator (vco). The vco quits changing frequency when the input voltage stabilizes. The frequency of the vco, which is proportional to the analog input voltage, is measured and is displayed on the digital display as a voltage reading.**
- b) A ramp generator is used to enable a counter through a comparator. When the ramp voltage equals the input voltage the counter is latched and then reset. The counter reading is proportional to the input voltage since the ramp is changing at a constant v/second rate.**
- c) A ramp voltage and analog input voltage are applied to a comparator. As the input voltage causes the integrating capacitor to charge, it will at some point equal the ramp voltage. The ramp voltage is measured and displayed on the digital panel meter.**
- d) Any of the above could be correct, depending on the specific type of a/d converter involved.**

Answer: option B

6.The main advantage of the successive-approximation a/d converter over the counter-ramp a/d converter is its:

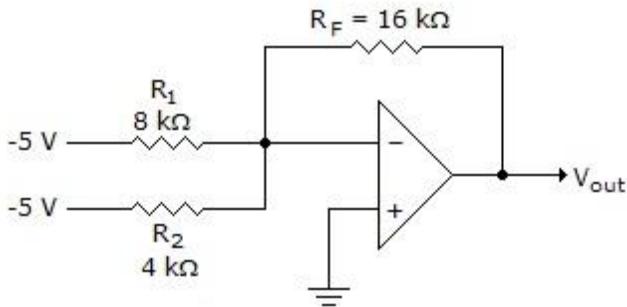
- a) More complex circuitry**
- b) Less complex circuitry**
- c) Longer conversion time**
- d) Shorter conversion time**

Answer: option D

Explanation:-

Because it has only n clks. So it is shorter conversion time.

7.What is the current in the feedback resistor for the circuit given below?



- a) 0.625 ma
- b) 1.25 ma
- c) 1.875 ma
- d) 1.625 ma

Answer: option C

Explanation:-

Its simply a opamp adder

here we can use equation of this circuit to calculate vout as

$$v_{out} = -[r_f/r_1(v_1) + r_f/r_2(v_2)]$$

$$= -[16/8(-5) + 16/4(-5)]$$

$$= -[-10 - 20] = 30 \text{ v.}$$

Hence we can calculate feedback current if,

$$I_f = v_{out}/r_f$$

$$= (30/16 \text{ kohm}) \text{ ampere}$$

$$= 1.875 \text{ ma.}$$

OR

From kcl, the current in the feedback resistor is equal to the sum of the currents flowing through the two input branches [since, the inverting terminal is at a virtual ground].

So, current through feedback resistor = $5/8 + 5/4 = 1.875 \text{ ma.}$

8.The quantization error in an analog-to-digital converter can be reduced by:

- a) Increasing the number of bits in the counter and DAC.
- b) Decreasing the number of bits in the counter and increasing the number of bits in the DAC.
- c) Increasing the number of bits in the counter and decreasing the number of bits in the DAC.
- d) Decreasing the number of bits in the counter and DAC.

Answer: option A

9.One disadvantage of the tracking a/d converter is:

- a) That it requires two counters—one for up and one for down.

- b) That the binary output will oscillate between two binary states when the analog input is constant.
- c) The need for an accurate clock reference for the counter.
- d) The need for a latch and its associated control circuit.

Answer: option B

Explanation:-

It always track the analog voltage OR amplitude w.r.t to reference voltage while receiving of the analog s/g and the process to the circuit. So it is time taking process.

10.If the range of output voltage of a 6-bit DAC is 0 to 15 volts, what is the step voltage of the output?

- a) 0.117 volt/step
- b) 0.234 volt/step
- c) 2.13 volt/step
- d) 4.26 volt/step

Answer: option B

Explanation:-

We know full scale voltage=no of step*step size

$$\text{no.of steps} = 2^6 = 64$$

i.e. Step size=full scale voltage/no of steps

$$= 15/64$$

$$=.234 \text{volts}$$

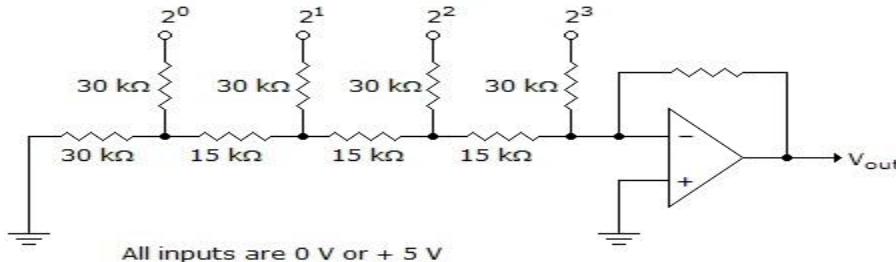
11.The process by which a computer acquires digitized analog data is referred to as _____.

- a) Data acquisition
- b) Monotonicity
- c) Analog resolution
- d) Systematic digital conversation

Answer: option A

12.What is the output voltage of the given circuit if the inputs are as follows:

$$20 = 1, 21 = 1, 22 = 0, 23 = 0?$$



All inputs are 0 V or + 5 V

- a) -3.115 volts
- b) -2.8025 volts
- c) -1.875 volts
- d) -1.24 volts

Answer: option C

Explanation:-

Here $r_f = 30k$, $r = 15k$.

$$V_{out} = -(r_f/r) \cdot v_{in}$$

$$v_{in} = (v/8) + (v/16)$$

$$= 5/8 + 5/16$$

$$= 0.9375 \text{ volt.}$$

$$V_{out} = -(30/15) \cdot 0.9375$$

$$= -1.875 \text{ volt.}$$

If this is the right solution for this but I consider the the binary zeros on the above figure as active so it will be:

$$-(5(1/2^2 + 1/2^3)) = -1.875.$$

13. Describe offset error for a DAC.

- a. Missing codes
- b. Error in the slope of the output staircase waveform
- c. More OR less input voltage is required for the first step than what is specified
- d. what is specified

Answer: option C

14. Two principal advantages of the dual-slope ADC are its:

- a. High speed and low cost.
- b. High sensitivity to noise and low cost.
- c. Low sensitivity to noise and high speed.
- d. Low sensitivity to noise and low cost.

Answer: option D

15. _____ are the most linear of all the temperature transducers.

- a. Thermistors
- b. Thermocouples
- c. I_c temperature sensors
- d. Resistance temperature detectors

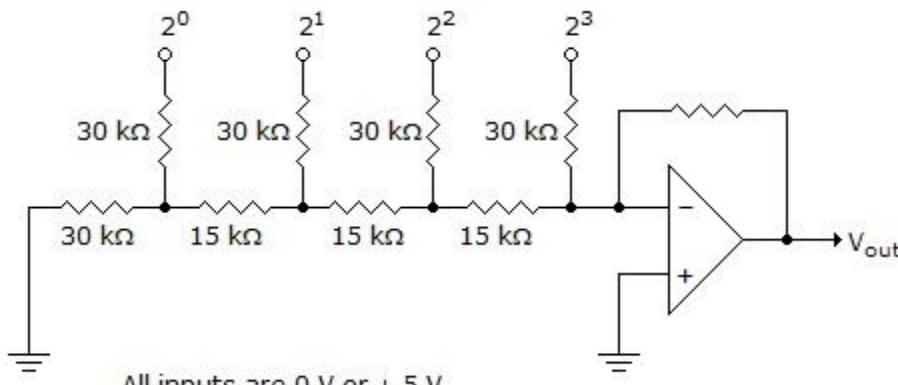
Answer: option C

16. The basic approach to testing d/a converters is to:

- Apply a sequence of binary codes covering the full range of input values to the circuit input while observing the output on an oscilloscope. The output should consist of a linear stairstep ramp.**
- Single-step the device through its full input range while checking the output with a dmm.**
- Check the output with zero input and then full input. The output of the converter should extend from zero to its maximum value. If so, then everything in between can be assumed to be operating properly.**
- Apply the correct input to the analog terminal and then check to see if the proper binary code exists on the digital inputs.**

Answer: option A

17. What is the maximum output voltage for the circuit shown below?



- 20 volts
- 5 volts
- 9.375 volts
- 2.1775 volts

Answer: option C

18. One major difference between a counter-ramp a/d converter and a successive-approximation converter is:

- The counter-ramp a/d converter is much faster than the successive-approximation converter**
- With the successive-approximation converter the final binary result is always slightly less than the equivalent analog input, whereas with the counter-ramp a/d converter it is slightly more**

- c. With the successive-approximation converter the final binary result is always slightly more than the equivalent analog input, whereas with the counter-ramp a/d converter it is slightly less
- d. None of the above

Answer: option B

19. One major difference between a counter-ramp a/d converter and a successive-approximation converter is:

- a. The counter-ramp a/d converter is much faster than the successive-approximation converter
- b. With the successive-approximation converter the final binary result is always slightly less than the equivalent analog input, whereas with the counter-ramp a/d converter it is slightly more
- c. With the successive-approximation converter the final binary result is always slightly more than the equivalent analog input, whereas with the counter-ramp a/d converter it is slightly less
- d. None of the above

Answer: option B

20. Which of the following characterizes an analog quantity?

- a. Discrete levels represent changes in a quantity.
- b. Its values follow a logarithmic response curve.
- c. It can be described with a finite number of steps.
- d. It has a continuous set of values over a given range.

Answer: option D

21. What is the resolution of a d/a converter?

- a. The comparison between the actual output of the converter and its expected output
- b. The reciprocal of the number of discrete steps in the d/a output
- c. The deviation between the ideal straight-line output and the actual output of the converter
- d. The ability to resolve between forward and reverse steps when sequenced over its entire range

Answer: option B

Explanation:-

The resolution of the converter indicates the number of discrete values.

22. What is the conversion time of a flash converter?

- a. 20 μ s
- b. 10 μ s
- c. 1 μ s

d. The conversion takes place continuously.

Answer: option D

23.What is the speed of the up/down digital-ramp ADC (tracking ADC)?

- a. 20 μ s**
- b. 10 μ s**
- c. 1 μ s**
- d. Relatively slow**

Answer: option D

24.The practical use of binary-weighted digital-to-analog converters is limited to:

- a. R/2r ladder d/a converters**
- b. 4-bit d/a converters**
- c. 8-bit d/a converters**
- d. Op-amp comparators**

Answer: option B

25.What is the major advantage of the r/2r ladder DAC as compared to a binary-weighted-input DAC?

- a. It has fewer parts for the same number of inputs.**
- b. It is much easier to analyze its operation.**
- c. It uses only two different resistor values.**
- d. The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.**

Answer: option C

26.An analog-to-digital converter has a four-bit output. How many analog values can it represent?

- a. 4**
- b. 1/4**
- c. 16**
- d. 0.0625**

Answer: option C

27.When comparing the conversions from digital-to-analog and analog-to-digital, the a/d conversion is generally:

- a. Less complicated but more time consuming than the d/a conversion.**
- b. More complicated and more time consuming than the d/a conversion.**
- c. Less complicated but less time consuming than the d/a conversion.**

- d. More complicated and less time consuming than the d/a conversion.**

Answer: option B

28.Which of the statements below best describes the basic operation of a dual-slope a/d converter?

- a. The input voltage is used to set the frequency of a voltage-controlled oscillator (vco). The vco quits changing frequency when the input voltage stabilizes. The frequency of the vco, which is proportional to the analog input voltage, is measured and is displayed on the digital display as a voltage reading.**
- b. A ramp generator is used to enable a counter through a comparator. When the ramp voltage equals the input voltage, the counter is latched and then reset. The counter reading is proportional to the input voltage since the ramp is changing at a constant v/second rate.**
- c. A ramp voltage and analog input voltage are applied to a comparator. As the input voltage causes the integrating capacitor to charge, it will at some point equal the ramp voltage. The ramp voltage is measured and displayed on the digital panel meter.**
- d. Two ramps are generated: one by the input voltage and the other by a reference voltage. The input voltage ramp charges the integrating capacitor, while the reference voltage discharges the capacitor and enables the counter until the capacitor is discharged, at which time the counter value is loaded into the output latches.**

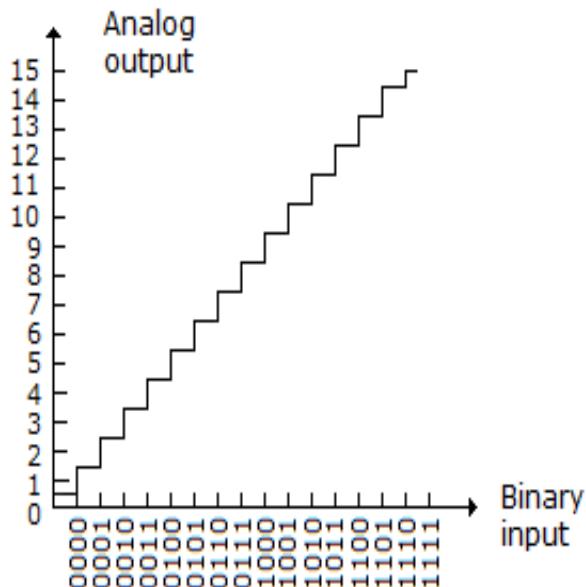
Answer: option D

29.The output of a basic 4-bit input digital-to-analog converter would be capable of outputting:

- a. 16 different values of voltage OR current that are not proportional to the input binary number**
- b. 16 different values of voltage OR current that are proportional to the input binary number**
- c. 32 different values of voltage OR current that are not proportional to the input binary number**
- d. 32 different values of voltage OR current that are proportional to the input binary number**

Answer: option B

30. Referring to the given figure, what appears to be wrong, if anything, with the d/a converter and what should be done to correct the problem?



- a. There is nothing wrong with the converter.
- b. There is an offset error; if no provision is made for adjusting the offset, the op-amp may need to be changed.
- c. There is a nonlinearity error; the op-amp must be changed.
- d. The power supply voltage appears to be too high; adjust the power supply to the correct value.

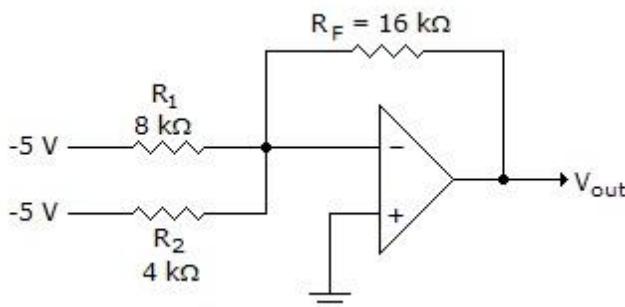
Answer: option B

31. Which of the following characterizes an analog quantity?

- a. Discrete levels represent changes in a quantity.
- b. Its values follow a logarithmic curve.
- c. It can be described with a finite number of steps.
- d. It has a continuous set of values over a given range.

Answer: option D

32. What is the current in r_1 and the current in r_2 for the circuit shown below?



- a. $I_1 = 0.416$ ma, $i_2 = 0.416$ ma
- b. $I_1 = 0.357$ ma, $i_2 = 0.357$ ma
- c. $I_1 = 1.25$ ma, $i_2 = 0.625$ ma
- d. $I_1 = 0.625$ ma, $i_2 = 1.25$ ma

Answer: option D

Explanation:-

$$I_1 = (v_1 - v_a)/r_1; i_2 = (v_2 - v_b)/r_2;$$
$$v_1 = -5, v_2 = -5, v_a = v_b = 0, r_1 = 8k, r_2 = 4k.$$

33. A 4-bit stairstep-ramp a/d converter has a clock frequency of 100 khz and maximum input voltage of 10 v.

- a. The maximum number of samples per second will be 6250.
- b. The maximum sample rate will be 100,000 samples/second.
- c. The minimum sample rate will be 6250 samples/second.
- d. The minimum sample rate will be 100,000 samples/second.

Answer: option C

34. What is the accuracy of a d/a converter?

- a. It is the reciprocal of the number of discrete steps in the d/a output.
- b. It is the comparison between the actual output of the converter and its expected output.
- c. It is the converter's ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.
- d. It is the deviation between the ideal straight-line output and the actual output of the converter.

Answer: option B

35. Which of the equations below expresses the voltage gain relationship for an operational amplifier?

- a. $V_{out} = v_{in}/av$
- b. $V_{out}/v_{in} = r_{out}/r_{in}$
- c. $V_{in}/v_{out} = r_{out}/r_{in}$
- d. $V_{out}/v_{in} = -rf/rin$

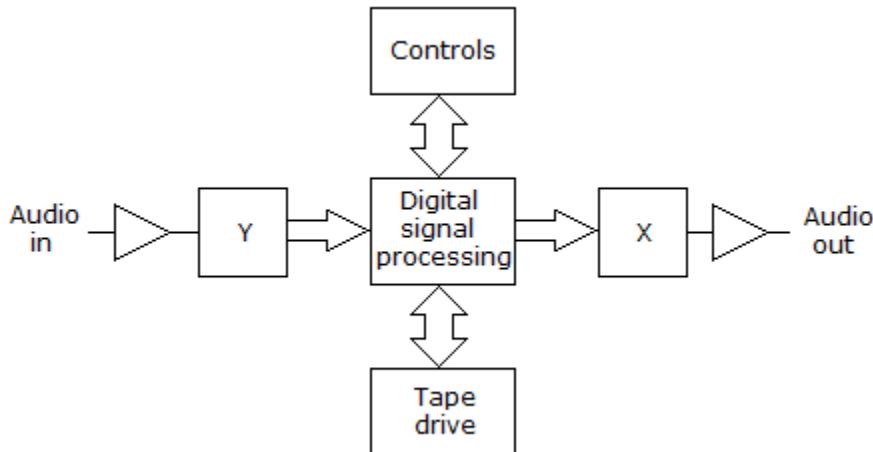
Answer: option D

36. An analog quantity varies from 0–7 v and is input to a 6-bit a/d converter. What analog value is represented by each step on the digital output?

- a. 0.111v
- b. 1.17 v
- c. 0.109 v
- d. 0.857 v

Answer: option A

37.What function is performed by the block labeled x in the given figure?



- a. Analog-to-digital conversion
- b. Digital-to-analog conversion
- c. Audio on/off control
- d. Power supply for the audio amplifier

Answer: option B

38.Inaccurate a/d conversion may be due to:

- a. Constant analog input voltage
- b. Linear ramp usage
- c. Intermittent counter inputs
- d. Faulty sample-and-hold circuitry

Answer: option D

39.What is the resolution, in percent, of a 12-bit DAC?

- a. 8.33
- b. 0.049
- c. 0.000488
- d. 0.083

Answer: option B

Explanation:-

$R = (100/2048)$ which comes by the given formula below:

$$r = (1/2^{n-1}) * 100$$

$$\Rightarrow 100/2^{11}$$

OR

Actually, there should be 11-bit **DAC** instead of 12-bit in the question.

$$So, r = (1/2^{11} - 1) * 100 = 0.049.$$

40.What circuitry is on an ADC0808 ic?

- a. A multiplexer
- b. An ADC
- c. A 3-bit select input code
- d. All of the above

Answer: option D

41.What is the maximum conversion time for an 8-bit successive-approximation ADC with a clock frequency of 20 khz?

- a. 12.8 ms
- b. 6.4 ms
- c. 0.05 ms
- d. 0.4 ms

Answer: option D

Explanation:-

Conversion time for successive-approximation **ADC** is $n \cdot t_p$.
I.e $8 \cdot (1/20\text{khz}) = 0.4 \text{ ms}$.

42.What is one advantage to using a parallel-encoded (flash) ADC?

- a. Less expensive
- b. Very fast conversion
- c. Less complicated circuit

Answer: option B

43.If the same analog signal is to be converted to an 8-bit resolution using a counter-ramp ADC, how many comparator circuits would be used?

- a. 1
- b. 8
- c. 127
- d. 255

Answer: option A

44.What is the major advantage of the $r/2r$ ladder d/a converter as compared to a binary-weighted d/a converter?

- a. It has fewer parts for the same number of inputs.
- b. It is much easier to analyze its operation.
- c. It uses only two different resistor values.
- d. The virtual ground is eliminated and the circuit is therefore easier to understand and troubleshoot.

Answer: option C

45.What is the main disadvantage of the stairstep-ramp a/d converter?

- a. The counter must count up from zero at the beginning of each conversion sequence, and the conversion time will vary depending on the input voltage.
- b. It requires a counter.
- c. It requires a precision clock in order for the conversion to be reliable.
- d. All of the above

Answer: option A

46.What is the purpose of a sample-and-hold circuit?

- a. To keep temporary memory
- b. To hold a voltage constant so an ADC has time to produce an output
- c. To hold a voltage constant so a DAC has time to produce an output
- d. To hold data after a multiplexer has selected an output

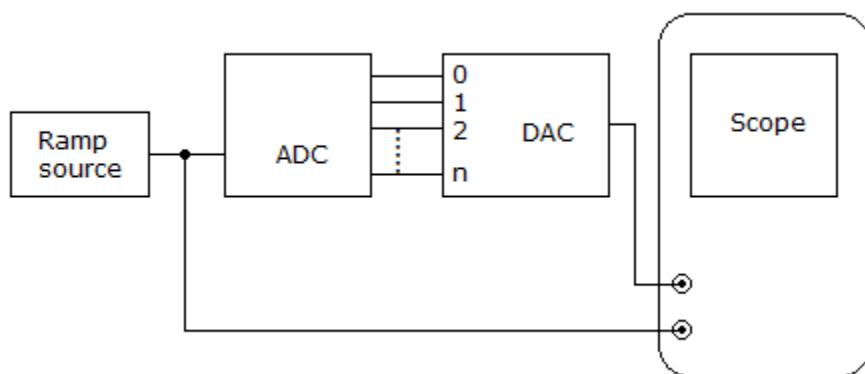
Answer: option B

47.What is the linearity of a d/a converter?

- a. It is the reciprocal of the number of discrete steps in the d/a output.
- b. It is the comparison between the actual output of the converter and its expected output.
- c. It is the converter's ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.
- d. It is the deviation between the ideal straight-line output and the actual output of the converter.

Answer: option D

48.Referring to the given figure, what should the display on the scope look like if the a/d converter is working properly?



- a. It should be a circular lissajous pattern resulting from the simultaneous application of ramps to the vertical and horizontal inputs of the oscilloscope.
- b. The pattern should be a straight line across the screen due to the equal but opposite voltages being applied to the scope inputs.
- c. A uniform staircase pattern should be displayed.
- d. The scope should display a sequential binary count with the LSB on the left and the MSB on the right side of the display.

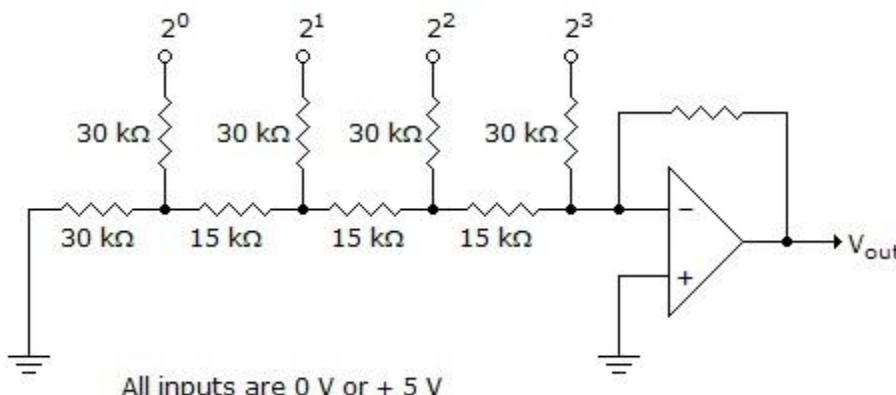
Answer: option C

49.What is the acquisition time of the ad1154 sample-and-hold ic?

- a. 1.5 μ s
- b. 2.5 μ s
- c. 3.5 μ s
- d. 4.5 μ s

Answer: option C

50.What type of DAC is shown below?



All inputs are 0 V or + 5 V

- a. Binary-weighted
- b. R- $2r$ ladder

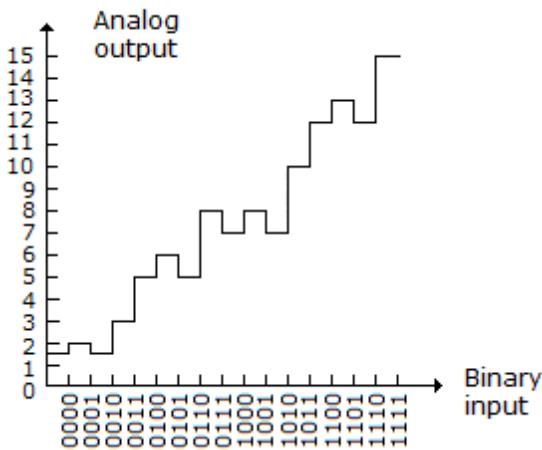
Answer: option B

51.What is the disadvantage to using a counter-ramp type ADC?

- a. Complex circuit
- b. High cost
- c. Very slow

Answer: option C

52.Referring to the given figure, what appears to be wrong, if anything, with the output of the d/a converter?



- a. The input signal is probably noisy.
- b. There appears to be some nonlinearity in the scope display.
- c. The converter has a nonmonotonic output error.
- d. It appears that certain input codes are incorrect; double-check the input coding.

Answer: option C

53What is the maximum conversion time for a counter-ramp ADC with 8-bit resolution and a clock frequency of 20 khz?

- a. 12.8 ms
- b. 6.4 ms
- c. 0.05 ms
- d. 0.4 ms

Answer: option A

Explanation

Conversion time 2^{n-1} .

Here conversion time is 255.

Max conversion time = $(255(1/f)) = 12.8 \text{ ms.}$

54.A test system using the gpib is being used to monitor a potentially dangerous crash test from a distance of 200 feet. The engineer decides to have you fabricate a special cable, rather than order one, since all the materials are on hand and the tests are already behind schedule. When the tests are run, the test system is erratic and the data is almost useless. What has gone wrong?

- a. The engineer is probably not using the correct data format for the specific instruments being used to collect the data.
- b. The gpib cable is too long; a bus extender should be used.
- c. The cable should be shielded and properly grounded.

- d. The tests themselves probably produced extraneous signals that confused the instruments, resulting in unusable data.**

Answer: option B

55.A certain digital-to-analog converter has a step size of 0.25 v and a full-scale output of 7.75 v. Determine the percent of resolution and the number of input binary bits.

- a. 31%, 4 bits
- b. 3.23%, 4 bits
- c. 31%, 5 bits
- d. 3.23%, 5 bits

Answer: option D

56.A simultaneous a/d converter is also known as a(n) _____ a/d converter.

- a. Flash
- b. Synchronous
- c. Comparator
- d. Asynchronous

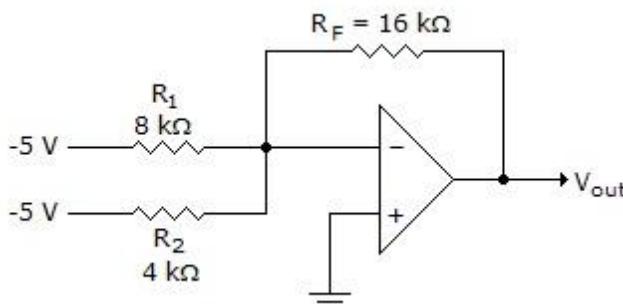
Answer: option A

57.The primary disadvantage of the simultaneous a/d converter is:

- a. That it requires the input voltage to be applied to the inputs simultaneously
- b. The long conversion time required
- c. The large number of output lines required to simultaneously decode the input voltage
- d. The large number of comparators required to represent a reasonable sized binary number

Answer: option D

58.What is the output voltage for the circuit shown below?



- a. 10 v
- b. 20 v
- c. 30 v

d. 40 v

Answer: option C

59.Three characteristics of op amps make them almost ideal amplifiers: very high input impedance, very low impedance, and

- a. Very high voltage gain**
- b. Unlimited bandwidth**
- c. A low slew rate**
- d. Very high current gain**

Answer: option A

Explanation

An ideal op-amp should have the following properties:

infinite open-loop gain $g = v_{out}/v_{in}$.

Infinite input impedance r_{in} ,

zero input current.

Zero input offset voltage.

Infinite voltage range available at the output.

Infinite bandwidth.

Infinite slew rate.

Zero output impedance r_{out} .

Zero noise.

Infinite common-mode rejection ratio (cmrr).

Infinite power supply rejection ratio.

60.Sample-and-hold circuits in a/d converters are designed to:

- a. Sample and hold the output of the binary counter during the conversion process**
- b. Stabilize the comparator's threshold voltage during the conversion process**
- c. Stabilize the input analog signal during the conversion process**
- d. Sample and hold the d/a converter staircase waveform during the conversion process**

Answer: option C

61.What is the main disadvantage of the counter-ramp a/d converter?

- a. It requires a counter.**
- b. The counter must count up from zero at the beginning of each conversion sequence, and the conversion time will vary depending on the input voltage.**
- c. It requires a precision clock in order for the conversion to be reliable.**

- d. The counter must count up from zero at the beginning of each conversion sequence, and the conversion time will vary depending on the input voltage. It requires a precision clock in order for the conversion to be reliable.

Answer: option B

62.Why is a binary-weighted DAC usually limited to 4-bit binary conversion?

- a. Too many pins on the ic
- b. Too many op amps needed
- c. Too many different values of capacitors
- d. Too many different values of resistors

Answer: option D

63.What is the resolution of a d/a converter?

- a. It is the reciprocal of the number of discrete steps in the d/a output.
- b. It is the comparison between the actual output of the converter and its expected output.
- c. It is the deviation between the ideal straight-line output and the actual output of the converter.
- d. It is the converter's ability to resolve between forward and reverse steps when sequenced over its entire range of inputs.

Answer: option A

64.What is gain error in a DAC?

- a. Missing codes
- b. Error in the slope of the output staircase waveform
- c. More OR less input voltage is required for the first step than what is specified

Answer: option B

65.An actuator is usually a device that:

- a. Converts analog data to meaningful digital data.
- b. Controls a physical variable.
- c. Stores digital data and then processes that data according to a set of specified instructions.
- d. Converts a physical variable to an electrical variable.

Answer: option B

True/false

- 1.The DAC0808 and the mc1408 are very popular and inexpensive 8-bit d/a converters.

A)True

B)False

Answer: option A

2.The delay between a change on the digital input of a DAC and the appearance of the change on the output is called settling time.

A)True

B)False

Answer: option A

3.The main advantage of the sar ADC method is its high speed.

A)True

B)False

Answer: option A

4.One way to determine the resolution of a DAC is to calculate the ratio of one step voltage to the maximum output voltage.

A)True

B)False

Answer: option A

5.The output voltage OR current of a digital-to-analog converter is truly an analog signal.

A)True

B)False

Answer: option B

6.The amount of deviation of the measured step size from the ideal step size is a measure of linearity.

A)True

B)False

Answer: option A

7.When analog inputs from several sources are to be converted, a multiplexing technique can be used so that one ADC may be time-shared.

A)True

B)False

Answer: option A

8.An ad7524 is an eight-bit d/a converter that uses an r/2r ladder network.

A)True

B)False

Answer: option A

9.Voltage-to-frequency ADC is more complicated than other ADCs.

A)True

B)False

Answer: option B

10.Two characteristics of ideal operational amplifiers are very high input impedance and very high voltage gain.

A)True

B)False

Answer: option A

11.Electrical quantities can be interpreted without conditioning by a digital computer.

A)True

B)False

Answer: option B

12.It is possible to develop more than 16 different analog levels using 4-bit resolution.

A)True

B)False

Answer: option B

13.A simultaneous, multiple comparator, OR flash converter uses parallel encoding.

A)True

B)False

Answer: option A

14.A DAC is monotonic if its output increases as its binary input is incremented from one value to the next.

A)True

B)False

Answer: option A

15.An operational amplifier is used as a comparator.

A)True

B)False

Answer: option A

16.Resolution in the analog output of a DAC is primarily dependent on the number of input binary bits.

A)True

B)False

Answer: option A

17.The primary disadvantage of the flash a/d converter is the large number of comparators required.

A)True

B)False

Answer: option A

18.A summing op-amp can be used for DAC.

A)True

B)False

Answer: option A

19.A data acquisition system may communicate via two common buses: the data bus and the control bus.

A)True

B)False

Answer: option A

20.The time required to complete a conversion cycle is called conversion time.

A)True

B)False

Answer: option A

21.Generally speaking, DACs with a current output will have a shorter settling time than those with voltage outputs.

A)True

B)False

Answer: option A

22.A d/a converter changes things such as temperature variations into digital quantities.

A)True

B)False

Answer: option B

23.If the least significant bit (LSB) of a four-bit binary-weighted resistor d/a converter connects to a 200Ω resistor, then the resistor needed for the next bit is 100Ω .

A)True

B)False

Answer: option A

24.Flash a/d converters depend on an input clock pulse to perform each conversion.

A)True

B)False

Answer: option B

25.Linearity error is the maximum deviation in step size from the ideal step size.

A)True

B)False

Answer: option A

26.One form of a sigma/delta modulator circuit is designed to convert a continuous analog signal into a modulated bit stream (a/d).

A)True

B)False

Answer: option A

27.In a binary-weighted d/a converter the sum of all the currents from the binary weighted resistors flows through the operational amplifier.

A)True

B)False

Answer: option B

28.An eight-bit d/a converter has a resolution of 0.125.

A)True

B)False

Answer: option B

29.In a counter-ramp a/d converter, the end-of-conversion line must be tied back to the clear input of the counter to change the circuit to perform continuous conversions.

A)True

B)False

Answer: option A

30.D/a conversion is the process of taking a voltage OR current and converting it to a digital code.

A)True

B)False

Answer: option B

31.A sample-and-hold circuit is used in d/a conversion.

- A)True
- B)False

Answer: option B

32.The output of an analog-to-digital converter is a voltage level.

- A)True
- B)False

Answer: option B

33.A cd player probably uses a sigma/delta d/a converter.

- A)True
- B)False

Answer: option A

34.When the inputs of a four-bit d/a converter are connected to a binary up-counter, the output looks like an upward sloping line.

- A)True
- B)False

Answer: option B

35.The current across the MSB "rung" of a 4-bit $r/2r$ ladder DAC if the reference voltage is 5 v and r is 8 Ω is 625 μ a.

- A)True
- B)False

Answer: option B

36.When the analog input to a tracking a/d converter is at a constant level, the digital output will oscillate.

- A)True
- B)False

Answer: option A

37.To be useful, a/d OR d/a converters must have meaningful representation of the analog quantity and a digital representation and the digital quantity as an analog representation.

- A)True
- B)False

Answer: option A

38.A light bulb and a switch are examples of an analog circuit.

- A)True
- B)False

Answer: option B

39. When a DAC output shows a deviation of the measured step size from the ideal step size, this error is called nonlinearity.

A) True

B) False

Answer: option A

40. In a digital storage scope, when memory is full, the next data point is lost.

A) True

B) False

Answer: option B

FILL IN THE BLANKS

1. There are many applications in which analog data must be digitized and transferred into a computer's memory. The process by which the computer acquires these digitized analog data is referred to as _____.

- a) Sampling**
- b) Multiplexing**
- c) Data acquisition**
- d) Pre scaling**

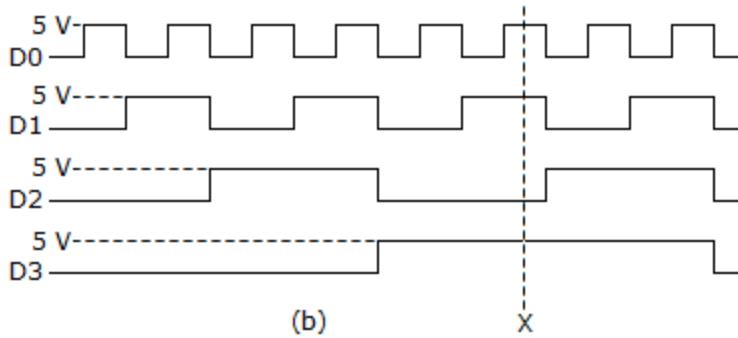
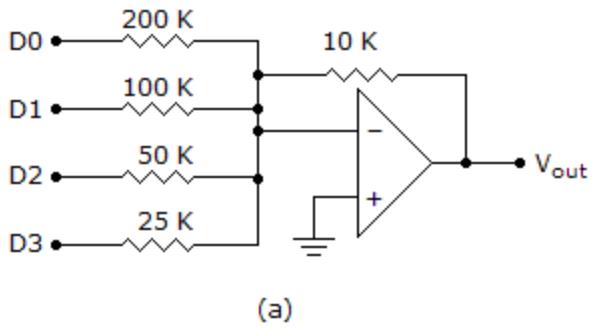
Answer: option C

2. When analog inputs from several sources are to be converted, a(n) _____ technique can be used.

- a) Demultiplexing**
- b) Multiplexing**
- c) R/2r**
- d) Comparator**

Answer: option B

3. The output of the circuit in the given figure (a) at point x on figure (b) will be _____.



- a) 1.011 v
- b) 2.75 v
- c) -1.011 v
- d) -2.75 v

Answer: option D

4. The stability of the ADC process can be improved by using a(n) _____ to hold the analog voltage constant while the a/d conversion is taking place.

- a) Sample-and-hold circuit
- b) Op-amp comparator
- c) Npn amp
- d) Current loop

Answer: option A

5. The characteristic that a change of one binary step on the input of a DAC should cause exactly one step change on the output is called _____.

- a) Resolution
- b) Linearity
- c) Monotonicity
- d) Accuracy

Answer: option C

6.On a binary-weighted d/a converter the least significant binary input _____.

- a) Connects to the smallest resistor
- b) Supplies the least voltage
- c) Connects to a $1\text{ k}\Omega$ resistor
- d) Connects to the largest resistor

Answer: option D

7._____ ADCs use no clock signal, because there is no timing OR sequencing required.

- a) Actuator
- b) Dual
- c) Flash
- d) Bipolar

Answer: option C

8.The input of an analog-to-digital converter is _____.

- a) A voltage level
- b) A clock pulse
- c) A binary number
- d) Any of the above

Answer: option A

9.A(n) _____ converts an analog input to a digital output.

- a) ADC
- b) DAC
- c) Flash converter
- d) Bipolar converter

Answer: option A

10.The ad7524, a CMOS ic available from several ic manufacturers, is an eight-bit d/a converter that uses a(n) _____.

- a) Sample-and-hold circuit
- b) $R/2^r$ ladder network
- c) Multiplexer
- d) 10^{-12} s clock

Answer: option B

11.A counter-ramp ADC uses a comparator to compare the input voltage with _____.

- a) A binary number
- b) The output of a counter
- c) The output of a DAC
- d) A voltage divider network

Answer: option C

12.A binary-weighter resistor DAC is practical only up to a resolution of _____.

- a) 10 bits
- b) 2 bits
- c) 8 bits
- d) 4 bits

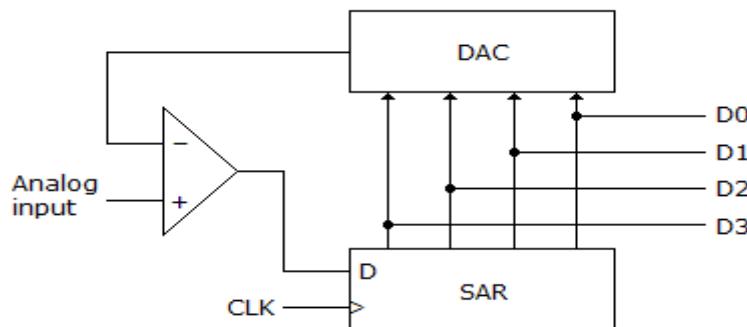
Answer: option D

13.A simultaneous a/d converter is also known as a(n) _____ a/d converter.

- a) Flash
- b) Synchronous
- c) Comparator
- d) Asynchronous

Answer: option A

14.The figure given below represents a _____.



- a) Successive-approximation a/d converter
- b) Dual-slope a/d converter
- c) Tracking a/d converter
- d) Dual-approximation d/a comparator

Answer: option A

15.The primary disadvantage of the simultaneous a/d converter is _____.

- a) That it requires the input voltage to be applied to the inputs simultaneously
- b) The long conversion time required
- c) The large number of output lines required to simultaneously decode the input voltage
- d) The large number of comparators required to represent a reasonable-sized binary number

Answer: option D

16. The dso _____, _____, and _____ analog waveforms.

- a) Filters, conditions, sends
- b) Levels, stores, weighs
- c) Sends, receives, translates
- d) Digitizes, stores, displays

Answer: option C

17. A signal _____ is produced by sampling the signal at a rate less than the minimum rate identified by nyquist.

- a) Nyquist
- b) Sampling frequency
- c) Basis
- d) Alias

Answer: option D

18. For each bit that is added to a digital ramp ADC, the conversion time _____.

- a) Doubles
- b) Triples
- c) Decrease by one-third
- d) Decrease by one-half

Answer: option A

19. _____ DACs produce both positive and negative output values.

- a) Tristates
- b) Double
- c) Bipolar
- d) Unilateral

Answer: option C

20. A DAC is _____ if its output increases as the binary input increments from one value to the next.

- a) Monotonic
- b) Self adjusting
- c) Accurate
- d) Broken

Answer: option A

21. A 4-bit stairstep-ramp a/d converter has a clock frequency of 100 khz and a maximum input of 10 v, and has 6 v applied to the input.

The conversion time will be _____.

- a) 10 microseconds

- b) 160 microseconds
- c) 90 microseconds
- d) 6250 microseconds

Answer: option C

22.A major application for DSP is in _____ and _____ of analog signals.

- a) Sending, receiving
- b) Digitizing, weighting
- c) Filtering, conditioning
- d) Leveling, translating

Answer: option C

23.The fastest analog-to-digital converter is the _____.

- a) Counter ADC
- b) Successive-approximation ADC
- c) Dual slope ADC
- d) Parallel ADC

Answer: option D

24.The main advantage of the tracking a/d converter over the stairstep-ramp a/d converter is that _____.

- a) It does not require a counter
- b) It uses an up/down counter to indicate the polarity of the input voltage
- c) It uses an up/down counter to measure both positive and negative voltages
- d) It is faster

Answer: option D

25.A counter-ramp ADC stops counting when _____.

- a) The input voltage equals the DAC staircase voltage
- b) The counter reaches a maximum count
- c) The input voltage equals 5 volts
- d) The DAC staircase voltage equals 5 volts

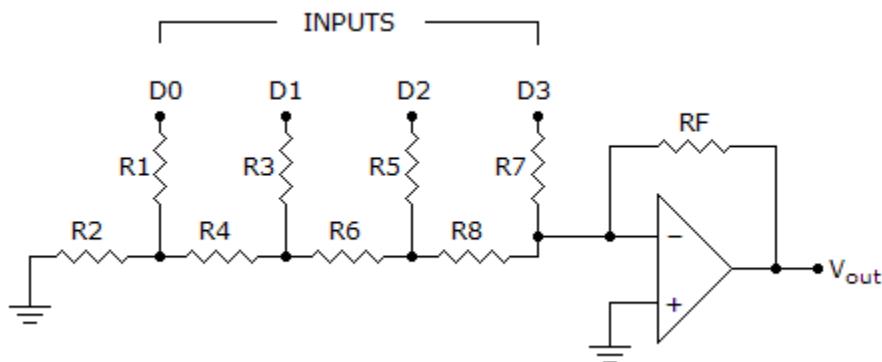
Answer: option A

26._____ ADCs have a fixed value of conversion time that is not dependent on the value of the analog input.

- a) Substandard
- b) Dual
- c) Recessive-approximation
- d) Successive-approximation

Answer: option D

27.The circuit shown below is a(n) _____.



- a) $R/2r$ ladder d/a converter
- b) Four-bit decoder
- c) Binary-weighted-input DAC
- d) Four-bit a/d converter

Answer: option A

28.A digital voltmeter converts an analog voltage to its _____ representation.

- a) BCD-code
- b) Decimal
- c) Digital
- d) Alias

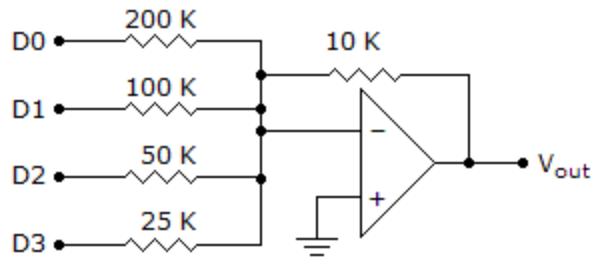
Answer: option A

29.The number of binary bits at the input of a DAC OR the output of an ADC is known as _____.

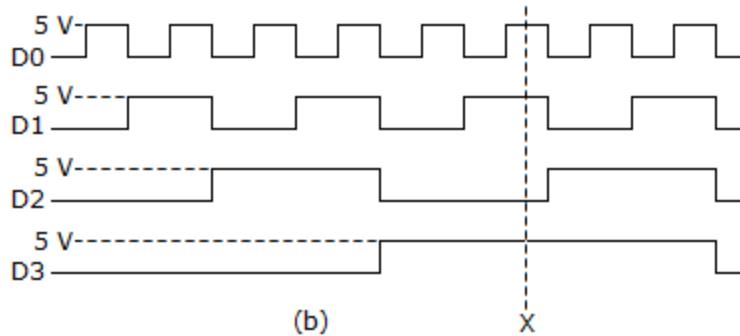
- a) Accuracy
- b) Linearity
- c) Resolution
- d) Monotonic

Answer: option C

30.The circuit shown below is a(n) _____.



(a)



(b)

- a) $R/2r$ ladder d/a converter
- b) Four-bit decoder
- c) Binary-weighted-input DAC
- d) Four-bit a/d converter

Answer: option C

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18.LOGIC FAMILIES AND THEIR CHARACTERISTICS

1.What is unique about TTL devices such as the 74sxx?

- a) These devices use schottky transistors and diodes to prevent them from going into saturation; this results in faster turn-on and turn-off times, which translates into higher frequency operation.
- b) The gate transistors are silicon (s), and the gates therefore have lower values of leakage current.
- c) The s denotes the fact that a single gate is present in the ic rather than the usual package of 2–6 gates.
- d) The s denotes a slow version of the device, which is a consequence of its higher power rating.

Answer: option A

Explanation:-

S represents schottky

74 prefix represents TTL logic family

Schottky diode is made up of metal and semiconductor junction, hence it will have low forward knee voltage compared to pn junction diode.

It has less rc constant because of size, and it has larger current density carrying capacity hence it is faster device and hence mainly used in rf applications.

2.Which of the following logic families has the shortest propagation delay?

- a) CMOS
- b) BICMOS
- c) ECL
- d) 74sxx

Answer: option C

Explanation:-

ECL is the unsaturated logic family and fastest of all the logic families.

OR

ECL has shortest propagation delay because it is the fastest logic as compared to all others.

OR

Because ECL does not enter into saturation. It always operates in linear region. Hence it takes less time to do transition from one state to another state. (ie. , from high to low OR viceversa).

OR

ECL, mostly transistors operated in saturation mode, due to this transition delay from one logic state to another is easy (i.e high to low OR low to high).

OR

ECL doesn't go to saturation. So, it has the shortest delay.

3.Why must CMOS devices be handled with care?

- a) So they don't get dirty**
- b) Because they break easily**
- c) Because they can be damaged by static electricity discharge**

Answer: option C

4.Special handling precautions should be taken when working with mos devices. Which of the following statements is not one of these precautions?

- a) All test equipment should be grounded.**
- b) Mos devices should have their leads shorted together for shipment and storage.**
- c) Never remove OR insert mos devices with the power on.**
- d) Workers handling mos devices should not have grounding straps attached to their wrists.**

Answer: option D

Explanation:-

All CMOS devices should be placed on a ground bench surface and operators should ground themselves prior to handling devices since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended.

5.What should be done to unused inputs on TTL gates?

- a) They should be left disconnected so as not to produce a load on any of the other circuits and to minimize power loading on the voltage source.**
- b) All unused gates should be connected together and tied to v_{cc} through a $1\ k\ \Omega$ resistor.**
- c) All unused inputs should be connected to an unused output; this will ensure compatible loading on both the unused inputs and unused outputs.**
- d) Unused and and nand inputs should be tied to v_{cc} through a $1\ k\ \Omega$ resistor; unused OR and nor inputs should be grounded.**

Answer: option D

Explanation:-

Assume that a particular ic has a supply voltage (V_{cc}) equal to +5 v and $i_{cch} = 10$ ma and $i_{cl} = 23$ ma. What is the power dissipation for the chip?

50 mw

82.5mw

115 mw

165 mw

Answer: option B

$$I_{cc} = (10+23)/2 = 16.5 \text{ ma}$$

power = voltage * current

$$= V_{cc} * I_{cc}$$

$$= 16.5 * 5$$

$$= 82.5 \text{ mw}$$

6. Can a 74hCMOS logic gate directly connect to a 74alsTTL gate?

- a) Yes
- b) No

Answer: option A

Explanation:-

Because CMOS is always compatible with TTL logic family.

7. What is the major advantage of ECL logic?

- a) Very high speed
- b) Wide range of operating voltage
- c) Very low cost
- d) Very high power

Answer: option A

Explanation:-

Due to low propagation delay, the speed is high.

8. As a general rule, the lower the value of the speed-power product, the better the device because of its:

- a) Long propagation delay and high power consumption
- b) Long propagation delay and low power consumption

Answer: option B

9. What is the range of invalid TTL output voltage?

- a) 0.0–0.4 v
- b) 0.4–2.4 v
- c) 2.4–5.0 v
- d) 0.0–5.0 v

Answer: option B

10.What is the difference between the 54xx and 74xx series of TTL logic gates?

- a) 54xx is faster.
- b) 54xx is slower.
- c) 54xx has a wider power supply and expanded temperature range.
- d) 54xx has a narrower power supply and expanded temperature range.

Answer: option C

Explanation:-

54xx series is for military application and hence have wider supply and operating temperature range.

11.An open collector output can _____ current, but it cannot _____.

- a) Sink, source current
- b) Source, sink current
- c) Sink, source voltage
- d) Source, sink voltage

Answer: option A

12.Why is a decoupling capacitor needed for TTL ics and where should it be connected?

- a) To block dc, connect to input pins
- b) To reduce noise, connect to input pins
- c) To reduce the effects of noise, connect between power supply and ground

Answer: option C

13.Using the schematic diagram of a TTL nAND Gate, determine the state of each transistor (on OR off) when all inputs are high.

- a) Q₁-on, q₂-off, q₃-on, q₄-off
- b) Q₁-on, q₂-on, q₃-off, q₄-off
- c) Q₁-off, q₂-off, q₃-on, q₄-on
- d) Q₁-off, q₂-on, q₃-off, q₄-on

Answer: option D

14.If all inputs to a TTL nAND Gate are low, what is the on, off condition of each transistor in the circuit?

- a) Q_1 -on, q_2 -off, q_3 -on, q_4 -off
- b) Q_1 -on, q_2 -on, q_3 -off, q_4 -off
- c) Q_1 -off, q_2 -off, q_3 -on, q_4 -on
- d) Q_1 -off, q_2 -on, q_3 -off, q_4 -on

Answer: option A

15.Which of the following summarizes the important features of emitter-coupled logic (ECL)?

- a) Low noise margin, low output voltage swing, negative voltage operation, fast, and high power consumption
- b) Good noise immunity, negative logic, high-frequency capability, low power dissipation, and short propagation time
- c) Low propagation time, high-frequency response, low power consumption, and high output voltage swings
- d) Poor noise immunity, positive supply voltage operation, good low-frequency operation, and low power

Answer: option A

16.Why is a pull-up resistor needed for an open collectOR Gate?

- a) To provide v_{cc} for the ic
- b) To provide ground for the ic
- c) To provide high voltage
- d) To provide low voltage

Answer: option C

17.Why is a pull-up resistor needed when connecting TTL logic to CMOS logic?

- a) To increase the output low voltage
- b) To decrease the output low voltage
- c) To increase the output high voltage
- d) To decrease the output high voltage

Answer: option C

18.The word "interfacing" as applied to digital electronics usually means:

- a) A conditioning circuit connected between a standard TTL nAND Gate and a standard TTL OR Gate
- b) A circuit connected between the driver and load to condition a signal so that it is compatible with the load
- c) Any gate that is a TTL operational amplifier designed to condition signals between NMOS transistors
- d) Any TTL circuit that is an input buffer stage

Answer: option B

19. The rise time (t_r) is the time it takes for a pulse to rise from its _____ point up to its _____ point. The fall time (t_f) is the length of time it takes to fall from the _____ to the _____ point.

- a) 10%, 90%, 90%, 10%
- b) 90%, 10%, 10%, 90%
- c) 20%, 80%, 80%, 10%
- d) 10%, 70.7%, 70.70%, 10%

Answer: option A

20. The term buffer/driver signifies the ability to provide low output currents to drive light loads.

A) True

B) False

Answer: option B

Explanation:-

Buffer is used to isolate the input to output.

21. PMOS and NMOS _____.

- a) Represent MOSFET devices utilizing either p-channel OR n-channel devices exclusively within a given gate
- b) Are enhancement-type CMOS devices used to produce a series of high-speed logic known as 74hc
- c) Represent positive and negative mos-type devices, which can be operated from differential power supplies and are compatible with operational amplifiers
- d) None of the above

Answer: option A

22. Why is the operating frequency for CMOS devices critical for determining power dissipation?

- a) At low frequencies, power dissipation increases.
- b) At high frequencies, the gate will only be able to deliver 70.7 % of rated power.
- c) At high frequencies, charging and discharging the gate capacitance will draw a heavy current from the power supply and thus increase power dissipation.
- d) At high frequencies, the gate will only be able to deliver 70.7 % of rated power and charging and discharging the gate capacitance will draw a heavy current from the power supply and thus increase power dissipation.

Answer: option C

23.Ten TTL loads per TTL driver is known as:

- a) Noise immunity
- b) Fan-out
- c) Power dissipation
- d) Propagation delay

Answer: option B

Explanation:-

Fan out : max no of loads driven by driver.

24.The problem of different current requirements when CMOS logic circuits are driving TTL logic circuits can usually be overcome by the addition of:

- a) A CMOS inverting bilateral switch between the stages
- b) A TTL Tri-State inverting buffer between the stages
- c) A CMOS noninverting bilateral switch between the stages
- d) A CMOS buffer OR inverting buffer

Answer: option D

25.Totem-pole outputs _____ be connected _____ because _____.

- a) Can, in parallel, sometimes higher current is required
- b) Cannot, together, if the outputs are in opposite states excessively high currents can damage one OR both devices
- c) Should, in series, certain applications may require higher output voltage
- d) Can, together, together they can handle larger load currents and higher output voltages

Answer: option B

26.The high input impedance of mosfets:

- a) Allows faster switching
- b) Reduces input current and power dissipation
- c) Prevents dense packing
- d) Creates low-noise reactions

Answer: option B

27.The output current capability of a single 7400 nAND Gate when high is called _____.

- a) Source current
- b) Sink current
- c) I_{oh}

d) Source current of i_{oh}

Answer: option A

28.The time needed for an output to change from the result of an input change is known as:

- a) Noise immunity**
- b) Fan-out**
- c) Propagation delay**
- d) Rise time**

Answer: option C

29.The problem of interfacing ic logic families that have different supply voltages (V_{cc} 's) can be solved by using a:

- a) Level-shifter**
- b) Tri-State shifter**
- c) Decoupling capacitor**
- d) Pull-down resistor**

Answer: option A

Explanation:-

Like max232 by texas instruments. From CMOS to TTL logic conversion especially using serial communication interfacing via rs232 standards.

30.What is the advantage of using low-power schottky (ls) over standard TTL logic?

- a) More power dissipation**
- b) Cost power dissipation**
- c) Cost is less**
- d) Cost is more**

Answer: option B

31.When is a level-shifter circuit needed in interfacing logic?

- a) A level shifter is always needed.**
- b) A level shifter is never needed.**
- c) When the supply voltages are the same**
- d) When the supply voltages are different**

Answer: option D

32.A TTL totem-pole circuit is designed so that the output transistors:

- a) Are always on together**
- b) Provide linear phase splitting**
- c) Provide voltage regulation**
- d) Are never on together**

Answer: option D

33.The most common TTL series ics are:

- a) E-MOSFET
- b) 7400
- c) Quad
- d) Ac00

Answer: option B

34.Fan-out is determined by taking the _____ result(s) of _____.

- a) Smaller, $\frac{I_{OL}}{I_{IL}}$ or $I_{oh} = \frac{V_{OH}}{R_{OH}}$
- b) Larger, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$
- c) Smaller, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$
- d) Average, $\frac{I_{OL}}{I_{IL}}$ or $\frac{I_{OH}}{I_{IH}}$

Answer: option C

35.Which family of devices has the characteristic of preventing saturation during operation?

- a) TTL
- b) MOS
- c) ECL
- d) IIL

Answer: option C

36.How many 74lsTTL logic gates can be driven from a 74TTL gate?

- a) 10
- b) 20
- c) 200
- d) 400

Answer: option B

37.What is the difference between the 74hc00 series and the 74hct00 series of CMOS logic?

- a) The hct series is faster.
- b) The hct series is slower.
- c) The hct series is input and output voltage compatible with TTL.
- d) The hct series is not input and output voltage compatible with TTL.

Answer: option C

38.From the following specifications determine the fan-out for the logic family.

$$I_{OH} = 20 \mu A \quad I_{IH} = 2.5 \mu A$$

$$I_{OL} = 32 mA \quad I_{IL} = 2 mA$$

- a) High state is 16, low state is 8
- b) High state is 8, low state is 16
- c) High state is 4, low state is 8
- d) High state is 8, low state is 4

Answer: option B

39.Why are the maximum value of v_{ol} and the minimum value of v_{oh} used to determine the noise margin rather than the typical values for these parameters?

- a) These are worst-case conditions.
- b) These are normal conditions.
- c) These are best-case conditions.
- d) It doesn't matter what values are used.

Answer: option A

40.What is the standard TTL noise margin?

- a) 5.0 V
- b) 0.0 V
- c) 0.8 V
- d) 0.4 V

Answer: option D

41.How can ECL have both a nor and an OR output?

- a) ECL does not have this feature.
- b) They are simply the inverse of each other.

Answer: option B

42.Which logic family is characterized by a multiemitter transistor on the input?

- a) ECL
- b) CMOS
- c) TTL
- d) None of the above

Answer: option C

43.How is the speed–power product of a logic family determined?

- a) The propagation delay in μ s is multiplied by the power dissipation in mw.
- b) The propagation delay in ms is multiplied by the power dissipation in μ w.
- c) The propagation delay in ns is multiplied by the power dissipation in mw.
- d) The propagation delay in ns is multiplied by the power dissipation in μ w.

Answer: option C

44. The problem of the $v_{oh(min)}$ of a TTL ic being too low to drive a CMOS circuit and meet the CMOS requirement of $v_{ih(min)}$ is usually easily overcome by:

- a) Adding a fixed voltage-divider bias resistive network at the output of the TTL device
- b) Avoiding this condition and only using TTL to drive TTL
- c) Adding an external pull-down resistor to ground
- d) Adding an external pull-up resistor to vcc

Answer: option D

45. How does the 4000 series of CMOS logic compare in terms of speed and power dissipation to the standard family of TTL logic?

- a) More power dissipation and slower speed
- b) More power dissipation and faster speed
- c) Less power dissipation and faster speed
- d) Less power dissipation and slower speed

Answer: option D

46. What should be done with unused inputs to a TTL nAND Gate?

- a) Let them float
- b) Tie them low
- c) Tie them high

Answer: option C

Explanation:-

Since floating TTL is susceptible to picking up noise signals, it is recommended to tie them high.

47. The TTL high level source current is higher than the low level sinking current.

- a) True
- b) False

Answer: option B

Explanation:-

The resistor whose electrical resistance value can be adjusted as per requirement by adjustable component attached to it is called variable resistor.

This is the reason for b.

True/false

1.In ECL, the high and low levels are determined by which transistor in a differential amplifier is conducting more.

- A)True**
- B)False**

Answer: option A

2.Propagation delay in TTL is due to slow switching speeds.

- A)True**
- B)False**

Answer: option B

3.In TTL the noise margin is between 0.8 v and 0.4 v.

- A)True**
- B)False**

Answer: option A

4.The and is the simplest of the gates, requiring the least amount of circuitry to implement in TTL.

- A)True**
- B)False**

Answer: option B

5.A typical fan-out for most TTL is 9.

- A)True**
- B)False**

Answer: option B

6.The basic part numbers of ics are the same regardless of the manufacturer because digital logic ics have been standardized.

- A)True**
- B)False**

Answer: option A

7.Schottky logic overcomes the saturation and stored charge problem by placing a schottky diode across the base-to-collector junction.

- A)True**

B)False

Answer: option A

8.Interfacing (74hCMOS to 74alsTTL OR 74TTL to 74lsTTL) can be done with no danger.

A)True

B)False

Answer: option B

9.A pulse is not perfectly square; it takes time for the digital level to rise from 0 up to 1 and to fall from 1 down to 0.

A)True

B)False

Answer: option A

10.PMOS and NMOS are commonly used for small memories and microprocessors.

A)True

B)False

Answer: option B

Explanation:-

We use combination of PMOS & NMOS in the design of small memories, then the answer may be true.

19.INTEGRATED CIRCUIT TECHNOLOGIES

1.Which is not a MOSFET terminal?

- a) Gate
- b) Drain
- c) Source
- d) Base

Answer: option D

2.For a CMOS gate, which is the best speed-power product?

- a) 1.4 pj
- b) 1.6 pj
- c) 2.4 pj
- d) 3.3 pj

Answer: option A

3.Which transistor element is used in CMOS logic?

- a) FET
- b) MOSFET
- c) Bipolar
- d) Unijunction

Answer: option B

Explanation:-

MOSFET : metal oxide semiconductor field effect transistor. As in fabrication process of CMOS semiconductors are used hence MOSFET is used.

OR

Basically, CMOS technology is a combination of PMOS and NMOS devices.
PMOS is a -ve logic and NMOS is +ve logic device.

OR

MOSFET is very important device used in large no.of electrical circuit OR replacing fet.

4.In a TTL circuit, if an excessive number of load gate inputs are connected, _____.

- a) Voh(min) drops below voh
- b) Voh drops below voh(min)
- c) Voh exceeds voh(min)
- d) Voh and voh(min) are unaffected

Answer: option B

5.The greater the propagation delay, the _____.

- a) Lower the maximum frequency
- b) Higher the maximum frequency
- c) Maximum frequency is unaffected
- d) Minimum frequency is unaffected

Answer: option A

Explanation:-

Frequency = 1/time.

If time delay is more frequency will be less.

6.An open-drain gate is the CMOS counterpart of _____.

- a) An open-collector TTL gate
- b) A Tri-State TTL gate
- c) A bipolar junction transistor
- d) An emitter-coupled logic gate

Answer: option A

7.A TTL nAND Gate with $i_{il(max)}$ of -1.6 mA per input drives eight TTL inputs. How much current does the drive output sink?

- a) -12.8 mA
- b) -8 mA
- c) -1.6 mA
- d) -25.6 mA

Answer: option A

Explanation:-

Just multiply $-1.6 \times 8 = -12.8 \text{ mA}$.

8.The nominal value of the dc supply voltage for TTL and CMOS is _____.

- a) $+3 \text{ V}$
- b) $+5 \text{ V}$
- c) $+9 \text{ V}$
- d) $+12 \text{ V}$

Answer: option B

9.Which logic family combines the advantages of CMOS and TTL?

- a) BICMOS
- b) TTL/CMOS
- c) ECL
- d) TTLMOS

Answer: option A

10.Which equation is correct?

- a) $V_{nl} = v_{il(max)} + v_{ol(max)}$
- b) $V_{nh} = v_{oh(min)} + v_{ih(min)}$
- c) $V_{nl} = v_{oh(min)} - v_{ih(min)}$
- d) $V_{nh} = v_{oh(min)} - v_{ih(min)}$

Answer: option D

11.The active switching element used in all TTL circuits is the _____.

- a) Bipolar junction transistor (bjt)
- b) Field-effect transistor (fet)
- c) Metal-oxide semiconductor field-effect transistor (MOSFET)
- d) Unijunction transistor (uj)

Answer: option A

12.An open-collector output requires _____.

- a) A pull-down resistor
- b) A pull-up resistor
- c) No output resistor
- d) An output resistor

Answer: option B

13.Most TTL logic used today is some form of _____.

- a) Schottky TTL
- b) Tri-State TTL
- c) Low-power TTL
- d) Open-collector TTL

Answer: option A

Explanation:-

Because the schottky diode has switching speed thrice to a normal TTL and a schottky diode connect with a transistor improve the speed so it is used.

13.A standard TTL circuit with a totem-pole output can sink, in the low state ($i_{ol(max)}$), _____.

- a) 16 ma
- b) 20 ma
- c) 16 μ a
- d) 20 μ a

Answer: option A

14.One output structure of a TTL gate is often referred to as a _____.

- a) Totem-pole arrangement
- b) Diode arrangement
- c) Jbt arrangement
- d) Base, emitter, collector arrangement

Answer: option A

15. It is best not to leave unused TTL inputs unconnected (open) because of TTL's _____.

- a) Noise sensitivity
- b) Low-current requirement
- c) Open-collector outputs
- d) Tri-State construction

Answer: option A

16. Which is not an output state for Tri-State logic?

- a) High
- b) low
- c) high-z
- d) Low-z

Answer: option D

17. TTL is alive and well, particularly in _____.

- a) Industrial applications
- b) Educational applications
- c) Military applications
- d) Commercial applications

Answer: option B

18. A TTL nAND Gate with $i_{ih(max)}$ of 40 μA per input drives ten TTL inputs. How much current does the drive output source?

- a) 40 μA
- b) 200 μA
- c) 400 μA
- d) 800 μA

Answer: option C

Explanation:-

Just multiply 40 and 10.

19. A certain gate draws 1.8 μA when its output is high and 3.3 μA when its output is low. V_{cc} is 5 v and the gate is operated on a 50% duty cycle. What is the average power dissipation (P_d)?

- a) 2.55 μW
- b) 1.27 μW

c) **12.75 μ w**

d) **5 μ w**

Answer: option C

Explanation:-

$$P_d = V_{cc} \cdot I_{cc(\text{avg})}$$

$$I_{cc(\text{avg})} = I_{cch} + I_{cl}/2$$

$$P_d = 5 * (1.8 + 3.3)/2 = 12.75$$

20. PMOS and NMOS circuits are used largely in _____.

a) **Msi functions**

b) **LSI functions**

c) **Diode functions**

d) **TTL functions**

Answer: option B

21. If I_{cch} is specified as 1.1 ma when V_{cc} is 5 v and if the gate is in a static (noncharging) high output state, the power dissipation (P_d) of the gate is _____.

a) **5.5 mw**

b) **5.5 w**

c) **5 mw**

d) **1.1 mw**

Answer: option A

Explanation:-

Power = voltage * current is basic formula.

22. Which is not a precaution for handling CMOS?

a) **Devices should be placed with pins down on a grounded surface, such as a metal plate.**

b) **All tools, test equipment, and metal workbenches should be earth grounded.**

c) **CMOS devices should not be inserted into sockets OR pc boards with the power on.**

d) **Wear wool clothes at all times.**

Answer: option D

Explanation:-

Because CMOS is made with the metal oxide so definitely we should use clothing like wool cotton.

23. Which factor does not affect CMOS loading?

- a) Charging time associated with the output resistance of the driving gate**
- b) Discharging time associated with the output resistance of the driving gate**
- c) Output capacitance of the load gates**
- d) Input capacitance of the load gates**

Answer: option C

24.Which is not part of emitter-coupled logic (ECL)?

- a) Differential amplifier**
- b) Bias circuit**
- c) Emitter-follower circuit**
- d) Totem-pole circuit**

Answer: option D

True/false

1.The speed-power product provides a basis for the comparison of logic circuits when power dissipation and propagation delay are important considerations in the selection of the type of logic to be used.

A)True

B)False

Answer: option A

2.ECL ic technology is faster than TTL technology.

A)True

B)False

Answer: option A

3.CMOS is a more dominant ic technology than TTL.

A)True

B)False

Answer: option A

4.Unused TTL inputs should be tied low.

A)True

B)False

Answer: option B

5.The greater the propagation delay, the higher the maximum frequency.

A)True

B)False

Answer: option B

Explanation:-

False!. As the propagation delay increases, the frequency decreases.

6.A pull-down resistor must be used with open-collector TTL circuits.

- A)True
- B)False

Answer: option B

7.Metal-oxide semiconductor field-effect transistors (mosfets) are the active switching elements in CMOS circuits.

- A)True
- B)False

Answer: option A

8.There are four different logic level ranges for TTL and CMOS: v_{il} , v_{ih} , v_{ol} , and v_{oh} .

- A)True
- B)False

Answer: option A

9.Power dissipation is a measure of a circuit's noise immunity.

- A)True
- B)False

Answer: option B

10.The total sink current decreases with an increase in each load gate input.

- A)True
- B)False

Answer: option B

20. INTEGRATED-CIRCUIT LOGIC FAMILIES

1. Which of the following logic families has the highest maximum clock frequency?

- a) S-TTL
- b) As-TTL
- c) Hs-TTL
- d) HCMOS

Answer: option B

Explanation:-

As-TTL (advanced schottky) has max that is 105mhz.

S-TTL (schottky high speed TTL) has 100mhz.

Found nothing as hs-TTL. There is h and s separate TTL.

HCMOS has 50mhz.

2. Why is the fan-out of CMOS gates frequency dependent?

- a) Each CMOS input gate has a specific propagation time and this limits the number of different gates that can be connected to the output of a CMOS gate.
- b) When the frequency reaches the critical value, the gate will only be capable of delivering 70% of the normal output voltage and consequently the output power will be one-half of normal; this defines the upper operating frequency.
- c) The higher the number of gates attached to the output, the more frequently they will have to be serviced, thus reducing the frequency at which each will be serviced with an input signal.
- d) The input gates of the fets are predominantly capacitive, and as the signal frequency increases the capacitive loading also increases, thereby limiting the number of loads that may be attached to the output of the driving gate.

Answer: option D

3. Logic circuits that are designated as buffers, drivers, OR buffer/drivers are designed to have:

- a) A greater current/voltage capability than an ordinary logic circuit.
- b) Greater input current/voltage capability than an ordinary logic circuit.

- c) A smaller output current/voltage capability than an ordinary logic.
- d) Greater input and output current/voltage capability than an ordinary
- e) Logic circuit.

Answer: option A

4.Which of the following will not normally be found on a data sheet?

- a) Minimum high level output voltage
- b) Maximum low level output voltage
- c) Minimum low level output voltage
- d) Maximum high level output voltage

Answer: option C

5.Which of the following logic families has the shortest propagation delay?

- a) S-TTL
- b) As-TTL
- c) Hs-TTL
- d) HCMOS

Answer: option B

Explanation:-

As-TTL has maximum allow clock frequency. So, it has shorest propagation delay.

6.Which of the following summarizes the important features of ECL?

- a) Low noise margin, low output voltage swing, negative voltage operation, fast, and high power consumption
- b) Good noise immunity, negative logic, high frequency capability, low power dissipation, and short propagation time
- c) Slow propagation time, high frequency response, low power consumption, and high output voltage swings
- d) Poor noise immunity, positive supply voltage operation, good low frequency operation, and low power

Answer: option A

7.What must be done to interface TTL to CMOS?

- a) A dropping resistor must be used on the CMOS 12 v supply to reduce it to 5 v for the TTL.
- b) As long as the CMOS supply voltage is 5 v, they can be interfaced; however, the fan-out of the TTL is limited to five CMOS gates.

- c) A 5 v zener diode must be placed across the inputs of the TTL gates in order to protect them from the higher output voltages of the CMOS gates.
- d) A pull-up resistor must be used between the TTL output-CMOS input node and v_{cc} ; the value of r_p will depend on the number of CMOS gates connected to the node.

Answer: option D

8.What causes low-power schottky TTL to use less power than the 74xx series TTL?

- a) The schottky-clamped transistor
- b) Nothing. The 74xx series uses less power.
- c) A larger value resistor
- d) Using nAND Gates

Answer: option C

9.What are the major differences between the 5400 and 7400 series of ic's?

- a) The 5400 series are military grade and require tighter supply voltages and temperatures.
- b) The 5400 series are military grade and allow for a wider range of supply voltages and temperatures.
- c) The 7400 series are an improvement over the original 5400s.
- d) The 7400 series was originally developed by texas instruments.
The 5400 series was brought out by national semiconductors after ti's patents expired, as a second supply source.

Answer: option B

10.Which of the following statements apply to CMOS devices?

- a) The devices should not be inserted into circuits with the power on.
- b) All tools, test equipment, and metal workbenches should be tied to earth ground.
- c) The devices should be stored and shipped in antistatic tubes OR conductive foam.
- d) All of the above.

Answer: option D

Explanation:-

Both 5400 and 7400 ic's were developed by texas instruments only. The difference between the 5400 and the 7400 series is that the 5400 series devices operate over the military temperature range of -55°C to 125°C, and the less expensive 7400 series devices need only operate over the

commercial temperature range of 0°C to 70°C. In short, 5400 ics are of military grade and 7400 ics are of commercial grade.

11.What must be done to interface CMOS to TTL?

- a) A dropping resistor must be used on the CMOS 12 v supply to reduce it to 5 v for the TTL.
- b) As long as the CMOS supply voltage is 5 v, they can be interfaced; however, the fan-out of the CMOS is limited to two TTL gates.
- c) A 5 v zener diode must be placed across the inputs of the TTL gates in order to protect them from the higher output voltages of the CMOS gates.
- d) The two series cannot be interfaced without the use of special interface buffers designed for that purpose, such as the open-collector buffers.

Answer: option B

12.What is the static charge that can be stored by your body as you walk across a carpet?

- a) 300 volts
- b) 3,000 volts
- c) 30,000 volts
- d) Over 30,000 volts

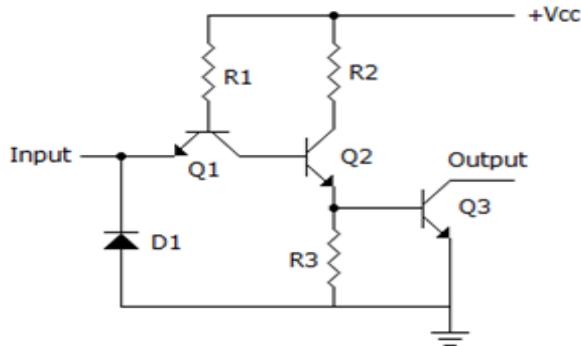
Answer: option D

Explanation:-

When a person walks across a carpeted OR tile floor, electric charge builds up in the body due to the friction between the shoes and floor material. The more you generate this friction static the greater the voltage potential develops in the body.

You start acting as a capacitor. This is called electrostatic discharge. And if one feels OR sees the static shock, it is a minimum of 3000 volts. The potential static charge that can develop from walking on tile floors is greater than 15,000 volts, while carpeted floors can generate in excess of 30,000 volts.

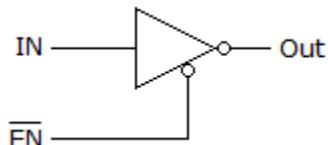
13.What type of circuit is shown below, and how is the output ordinarily connected?



- a) It is an open-collector OR Gate and is used to drive loads that cannot be connected directly to V_{cc} due to high noise levels.
- b) It represents an active-low inverter and is used in negative logic systems.
- c) It is an open-collector OR Gate. An external load must be connected between the output terminal and an appropriate supply voltage.
- d) Any of the above could be correct, depending on the specific application involved.

Answer: option C

14. What type of circuit is represented in the given figure, and which statement best describes its operation?



- a) It is a Tri-State inverter. When the enable input is high, the output is effectively an open circuit—it is neither low nor high.
- b) It is a programmable inverter. It can be programmed to function as either an active low OR an active high inverter.
- c) It is an active low buffer, which can be turned on and off by the enable input.
- d) None of the above.

Answer: option A

Explanation:-

The output mainly depends on the enable pin but from this figure we can't say anything because inverter also can be of this type.

15. Which of the following logic families has the highest noise margin?

- a) TTL
- b) LS TTL
- c) CMOS

d) hCMOS

Answer: option D

16.A "floating" TTL input may be defined as:

- a) Unused input that is tied to v_{cc} through a $1\text{ k}\Omega$ resistor.
- b) Unused input that is tied to used inputs.
- c) Unused input that is tied to the ground.
- d) Unused input that is not connected.

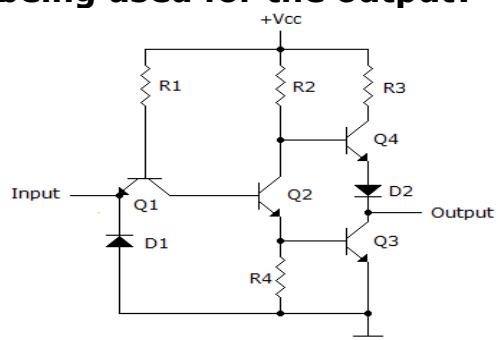
Answer: option D

17.Which of the logic families listed below allows the highest operating frequency?

- a) 74as
- b) ECL
- c) HCMOS
- d) S4s

Answer: option B

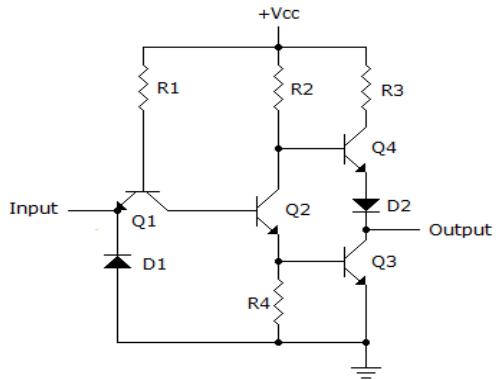
18.Refer to the given figure. What type of output arrangement is being used for the output?



- a) Complementary-symmetry
- b) Push-pull
- c) Quasi push-pull
- d) Totem-pole

Answer: option D

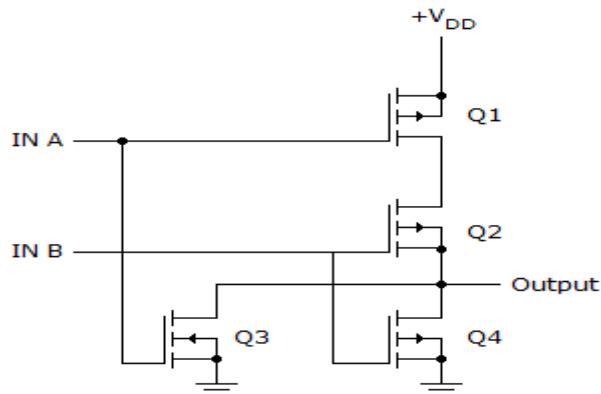
19.Refer the given figure. Which of the following describes the operation of the circuit?



- a) A low input turns q_1 and q_3 on; q_2 and q_4 are off.
- b) A low input turns q_1 and q_4 off; q_2 and q_3 are on.
- c) A high input turns q_1 , q_2 , and q_3 off, and q_4 is on.
- d) A high input turns q_1 , q_2 , and q_4 on; q_3 is off.

Answer: option C

20. What type of logic circuit is shown below and what logic function is being performed?



- a) It is an NMOS AND Gate.
- b) It is an CMOS AND Gate.
- c) It is an CMOS nOR Gate.
- d) It is an PMOS nAND Gate.

Answer: option C

Explanation:-

Here the PMOS is connected in series manner and also placed in pull up network so this CMOS circuit acts as nOR Gate so answer is c.

21. Whenever a totem-pole TTL output goes from low to high, a high-amplitude current spike is drawn from the V_{CC} supply. How is this effect corrected to a digital circuit?

- a) By connecting a radio-frequency capacitor from V_{CC} to ground.
- b) By using a switching power supply
- c) By connecting a capacitor from V_{OUT} to ground

d) By connecting a large resistor from vcc to vout

Answer: option A

22.What is the increase in switching speed between 74ls series TTL and 74hc/hct (high-speed CMOS)?

- a) 5
- b) 10
- c) 50
- d) 100

Answer: option B

23.A logic signal experiences a delay in going through a circuit. The two propagation delay times are defined as:

- a) T_{phl} and t_{phl} .
- b) T_{dih} and t_{dhl} .
- c) T_{hpl} and t_{iph} .
- d) T_{ldh} and t_{HDL} .

Answer: option A

24.What does ECL stand for?

- a) It stands for electron-coupled logic; all of the devices used within the gates are n-type transistors.
- b) It stands for emitter-coupled logic; all of the inputs are coupled into the device through the emitters of the input transistors.
- c) It stands for emitter-coupled logic; all of the emitters of the input transistors are connected together and each transistor functions as an emitter follower.
- d) It stands for energy-coupled logic; the input energy is amplified by the input transistors and allows the device to deliver higher output currents.

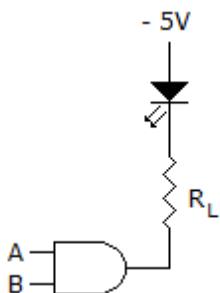
Answer: option C

25.What is unique about TTL devices such as the 74s00?

- a) The gate transistors are silicon (s), and the gates therefore have lower values of leakage current.
- b) The s denotes the fact that a single gate is present in the ic rather than the usual package of 2–6 gates.
- c) The s denotes a slow version of the device, which is a consequence of its higher power rating.
- d) The devices use schottky transistors and diodes to prevent them from going into saturation; this results in faster turn on and turn off times, which translates into higher frequency operation.

Answer: option D

26. Refer to the figure given below. What type of device is shown and what input levels are required to turn the led off?



- a) The device is an open-collector AND Gate and requires both inputs to be high in order to turn the led off.
- b) The device is a schottky AND Gate and requires only one low input to turn the led off.
- c) The device is an open-collector AND Gate and requires only one low input to turn the led off.
- d) The device is a schottky open-collector AND Gate and requires a low on both inputs to turn the led off.

Answer: option A

Explanation:-

Does that say -5v at the top? If so, it probably doesn't matter what the input states are. The led will never light.

27. Generally, the voltage measured at an unused TTL input would typically be measured between:

- a) 1.4 to 1.8 v.
- b) 0 to 5 v.
- c) 0 to 1.8 v.
- d) 0.8 to 5 v.

Answer: option A

28. The ieee/ansi notation of an internal underlined diamond denotes:

- a) Totem-pole outputs.
- b) Open-collector outputs.
- c) Quadrature amplifiers.
- d) Tri-State buffers.

Answer: option B

29. The bipolar TTL logic family that was developed to increase switching speed by preventing transistor saturation is:

- a) Emitter-coupled logic (ECL).

- b) Current-mode logic (cml).
- c) Transistor-transistor logic (TTL).
- d) Emitter-coupled logic (ECL) and transistor-transistor logic (TTL).

Answer: option D

True/false

1.The major advantage of TTL logic circuits over CMOS is lower propagation delay.

- A)True
- B)False

Answer: option A

2.The data sheet for the 74 series of TTL ics shows that v_{cc} has a range of 4.5 v to 5.5 v.

- A)True
- B)False

Answer: option B

3.The major advantage of CMOS logic circuits over TTL is very low power consumption.

- A)True
- B)False

Answer: option A

4.The dc noise margins calculated using the proper values from a standard TTL data sheet are the worst-case margins. The typical dc noise margins are usually somewhat higher.

- A)True
- B)False

Answer: option A

5.The noise margin for TTL is 0.8 v.

- A)True
- B)False

Answer: option B

Explanation:-

Noise margin for TTL is 0.4 v

6.The principal advantage of mos ics over TTL ics is their fast operating speed.

- A)True
- B)False

Answer: option B

7.The CMOS series that is pin-compatible with the TTL family is the 4000 series.

- A)True
- B)False

Answer: option B

8.The TTL high level source current is higher than the low level sinking current.

- A)True
- B)False

Answer: option B

9.The maximum output voltage recognized as a low by a TTL gate is 2.0 v.

- A)True
- B)False

Answer: option B

10.Usually p-mos and n-mos circuits are identical with the exception of the voltage polarities.

- A)True
- B)False

Answer: option A

11.An unused input of a nAND Gate can be left unconnected, pulled high by a pull-up resistor and tied together with another input and not change the logic output.

- A)True
- B)False

Answer: option A

12.ECL gates are noted for their high frequency capability and small output voltage swing.

- A)True
- B)False

Answer: option A

13.The logic family with the highest maximum clock frequency is hs-TTL.

- A)True
- B)False

Answer: option B

14.The output current capability for a high output condition is called a source current.

- A)True
- B)False

Answer: option A

15.The 74xx series TTL operates using saturated switching in which many of the transistors, when conducting, will be in the saturated condition.

- A)True
- B)False

Answer: option A

16.The abbreviated designator for a high input voltage is V_{ih} .

- A)True
- B)False

Answer: option A

17.A current-sourcing transistor may also be referred to as a pull-down transistor.

- A)True
- B)False

Answer: option B

18.Most TTL gates use the totem-pole output arrangement.

- A)True
- B)False

Answer: option A

19.The fan-out of CMOS gates is frequency dependent.

- A)True
- B)False

Answer: option A

20.The upper transistor of a totem-pole output is off when the gate output is low.

- A)True
- B)False

Answer: option A

21.The noise immunity of a logic circuit refers to the circuit's ability to tolerate noise by causing spurious charges in the output voltage.

- A)True
- B)False

Answer: option B

22.CMOS stands for "complementary metal-oxide semiconductors" and the fets are normally enhancement mode devices.

A)True

B)False

Answer: option A

23.A common means for measuring and comparing the overall performance of an ic family is the speed-power product.

A)True

B)False

Answer: option A

24.The time it takes for a square wave to go from 10% to 90% of its voltage level is called propagation delay.

A)True

B)False

Answer: option B

25.When the outputs of several standard TTL gates are connected together, the gate outputs produce more fan-out.

A)True

B)False

Answer: option B

26.A major drawback in using ECL logic circuits in conjunction with TTL and mos circuits is its negative supply voltages and logic levels.

A)True

B)False

Answer: option A

27.Due to the extremely low power requirements of CMOS logic circuits, any number of CMOS and TTL gates can be interconnected.

A)True

B)False

Answer: option B

28.The maximum current for a low output on a standard TTL gate is 100 μ a.

A)True

B)False

Answer: option B

29.Power-supply decoupling uses a radio-frequency capacitor to short out high frequency spikes.

A)True

B)False

Answer: option A

30.Integrated injection logic offers high component density and is easier to fabricate than TTL.

A)True

B)False

Answer: option A

FILL IN THE BLANKS

1.When the outputs of several open-collector TTL gates are connected together, the gate outputs _____.

- a) Usually burn out**
- b) Produce more voltage**
- c) Are anded together**
- d) Produce more fan-out**

Answer: option C

2.Propagation delay is important because _____.

- a) The logic gates must be given a short break during each clock cycle OR else they will overheat**
- b) It limits the maximum operating frequency of a gate**
- c) It is a measure of how long the clock must be applied to the gate before it will make the required decision**
- d) All the gates in a system must have the same propagation times in order to be compatible**

Answer: option A

3._____ output levels would *not* be a valid low for a TTL gate.

- a) 0.2 v**
- b) 0.3 v**
- c) 0.5 v**
- d) All of the above**

Answer: option D

4.The minimum input voltage recognized as high by a TTL gate is _____.

- a) 2.0 v**
- b) 2.4 v**
- c) 0.8 v**

d) 5.0 v

Answer: option A

5.The propagation delay of standard TTL gates is approximately _____.

- a) 2 μ s
- b) 1 μ s
- c) 4 μ s
- d) 10 μ s

Answer: option D

6.Several manufacturers have developed logic that combines the best features of TTL and CMOS. This is called _____.

- a) I²L
- b) BICOMOS
- c) 74ACT
- d) 74HCT

Answer: option B

7.Totem-pole outputs _____ be connected _____ because _____.

- a) Can, in parallel, sometimes higher output current is required
- b) Cannot, together, if the outputs are in opposite states excessively high currents can damage one OR both of the devices
- c) Should, in series, certain applications may require higher output voltage
- d) Can, together, together they can handle larger load currents and higher output voltages

Answer: option B

8.The power dissipation of a CMOS ic will _____.

- a) Decrease with frequency
- b) Increase with gate size
- c) Decrease with gate size
- d) Increase with frequency

Answer: option D

9.When $v_{gs} = 0$ on an n-channel MOSFET switch, there is no _____ between the source and the drain.

- a) Voltage drop
- b) Conductive channel
- c) Capacitance
- d) Inductance

Answer: option B

10.The number of gates that can be connected to a single output without exceeding the current ratings of the gate is called _____.

- a) Fan-out
- b) Propagation
- c) Dissipation
- d) Ssi

Answer: option A

11.The output current for a low output is called a(n) _____.

- a) Sink current
- b) Ground current
- c) Exit current
- d) Fan-out

Answer: option A

12._____ TTL allows three possible output states.

- a) Triswitch
- b) Triinput
- c) Tri-State
- d) Trident

Answer: option C

13.The proliferation of small handheld consumer equipment such as digital video cameras, cellular phones, handheld computers (_____), portable audio systems, and other devices has created a need for logic circuits in very small packages.

- a) HDLs
- b) Gdas
- c) Pdas
- d) TTLs

Answer: option C

14.The lower transistor of a totem-pole output is saturated when the gate output is _____.

- a) Overdriven
- b) High
- c) Low
- d) Malfunctioning

Answer: option C

15.When the output of a standard TTL gate is high, it can _____.

- a) Sink 16 mA of current from the attached input gates
- b) Source 400 μ A of current to no more than 10 attached gates
- c) Source 16 mA of current to no more than 10 attached gates
- d) Sink a maximum of 400 μ A from no more than 10 load gates

Answer: option B

16. A _____ is a testing and troubleshooting tool that generates a short-duration pulse when manually activated, usually by depressing a push button.

- a) CaTTL prod
- b) Jimmy rod
- c) Logic pulser
- d) Bilateral switch

Answer: option C

17. Fan-out for a typical TTL gate is _____.

- a) 100
- b) 54
- c) 10
- d) 4

Answer: option C

18. An open-collector TTL gate _____.

- a) Can source current but cannot sink current
- b) Can sink current but cannot source current
- c) Cannot source OR sink current
- d) Can sink more current than a standard TTL gate

Answer: option B

19. One advantage that MOSFET transistors have over bipolar transistors is _____.

- a) High input impedance
- b) Higher switching speed
- c) Low input impedance
- d) Reduced propagation delay

Answer: option A

20. The time it takes for an input signal to pass through internal circuitry and generate the appropriate output effect is known as _____.

- a) Fan-out
- b) Propagation delay
- c) Rise time
- d) Fall time

Answer: option B

21. The 74f-fast TTL integrated-circuit fabrication technique uses reduced interdevice _____ to achieve reduced propagation delays.

- a) Noise
- b) Resistance
- c) Capacitance
- d) Inductance

Answer: option C

22. In a dip the spacing between pins is typically _____.

- a) 5 mils
- b) 10 mils
- c) 50 mils
- d) 100 mils

Answer: option D

23. _____ is about twice as fast as p-mos.

- a) CMOS
- b) dmos
- c) mod
- d) n-mos

Answer: option D

24. P-mos and n-mos _____.

- a) Represent MOSFET devices utilizing either p-channel OR n-channel devices exclusively within a given gate
- b) Are enhancement-type CMOS devices used to produce a series of high-speed logic known as 74hc
- c) Represent positive and negative mos-type devices that can be operated from differential power supplies and are compatible with operational amplifiers
- d) None of the above are.

Answer: option A

25. The output stage of a TTL gate is a special design called _____.

- a) Multimeter
- b) Totem-pole
- c) Msi
- d) Dip

Answer: option B

26.The _____ is defined as the maximum number of standard logic inputs that an output can drive reliably.

- a) Fan-drive
- b) Fan-out
- c) Fan-in
- d) Open-collector

Answer: option B

27._____ is ideally suited for applications using battery power OR battery backup power.

- a) Mos
- b) P-mos
- c) N-mos
- d) CMOS

Answer: option D

28.A logic probe is placed on the output of a digital circuit and the probe lamp is dimly lit. This display indicates _____.

- a) That an open OR bad logic level exists
- b) A high level output
- c) A high-frequency pulse train
- d) That the supply voltage is low

Answer: option A

29.A logic probe is placed on the input of a digital circuit and the probe lamp blinks slowly, indicating _____.

- a) That an open OR bad logic level exists
- b) A high level output
- c) A high-frequency pulse train
- d) That the supply voltage is low

Answer: option C

30.The high logic level for a standard TTL output must be at least _____.

- a) 2.4 v
- b) 2.0 v
- c) 0.8 v
- d) 5 v

Answer: option A

65. The location of a unit of data in a memory array is called its _____.

- a. Storage
- b. Ram
- c. Address
- d. Data

Answer: option C

66. On a CD-ROM, _____ are recessed areas representing a 0.

- a. Mounds
- b. Lands
- c. Holes
- d. Pits

Answer: option D

67. Why is a refresh cycle necessary for a dynamic ram?

- a. To clear the flip-flops
- b. To set the flip-flops
- c. The refresh cycle discharges the capacitor cells.
- d. The refresh cycle keeps the charge on the capacitor cells

Answer: option D

68. Which is not a magnetic storage device?

- a. Magnetic disk
- b. Magnetic tape
- c. Magneto-optical disk
- d. Optical disk

Answer: option D

69. The time from the beginning of a read cycle to the end of t_{acs} OR t_{aa} is referred to as:

- a. Access time
- b. Data hold
- c. Read cycle time
- d. Write enable time

Answer: option A

70. Which of the following memories is volatile?

- a. Rom
- b. Erom
- c. Ram
- d. Flash

Answer: option C

71. The refresh period for capacitors used in drams is _____.

- a. 2 ms
- b. 2 μ s
- c. 64 ms
- d. 64 μ s

Answer: option A

72. What is the principal advantage of using address multiplexing with dram memory?

- a. Reduced memory access time
- b. Reduced requirement for constant refreshing of the memory contents
- c. Reduced pin count and decrease in package size
- d. It eliminates the requirement for a chip-select input line, thereby reducing the pin count.

Answer: option C

73. What is a multitap digital delay line?

- a. A series of inverter gates with rc circuits between each one
- b. A series of inverter gates with rl circuits between each one
- c. A series of nAND Gates with rc circuits between each one
- d. A series of nAND Gates with rl circuits between each one

Answer: option A

74. The bit capacity of a memory that has 2048 addresses and can store 8 bits at each address is _____.

- a. 4096
- b. 8129
- c. 16358
- d. 32768

Answer: option C

Explanation:-

It is supposed to be 2048×8but i think the option is wrong...it is actually supposed to be 16384

75. How many 8 k \times 1 rams are required to achieve a memory with a word capacity of 8 k and a word length of eight bits?

- a. Eight
- b. Four
- c. Two
- d. One

Answer: option A

76. The mask rom is _____.

- a. Mos technology
- b. Diode technology
- c. Resistor-diode technology
- d. Drom technology

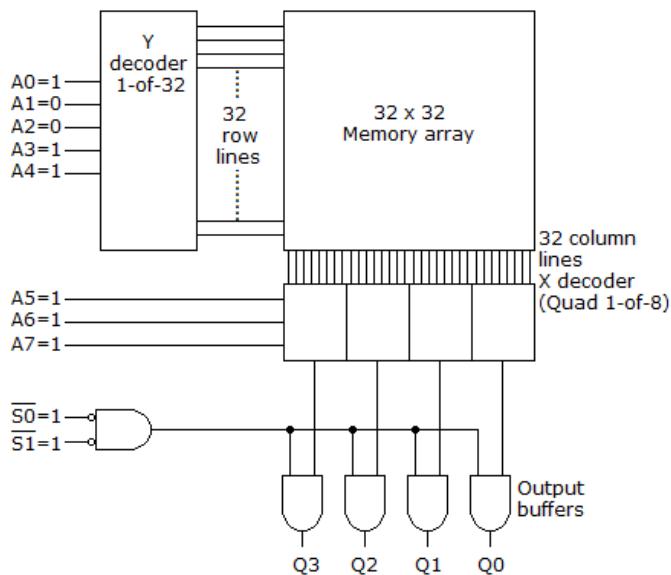
Answer: option A

77. Which of the following is not a flash memory mode OR operation?

- a. Burst
- b. Read
- c. Erase
- d. Programming

Answer: option A

78. For the given circuit, what is the bit length of the output data word?



- a. 3
- b. 4
- c. 8
- d. 32

Answer: option B

Explanation:-

Q0, q1, q2, q3 -> outputs.

of outputs = bit length of the output.

Therefore it is 4.

79. The smallest unit of binary data is the _____.

- a. Bit
- b. Nibble
- c. Byte
- d. Word

Answer: option A

Explanation:-

1 byte = 8 bits. 1 nibble = 4 bits.

1 word can be any bytes depends on architecture.

80. Select the statement that best describes the fusible-link PROM.

- a. User-programmable, one-time programmable
- b. Manufacturer-programmable, one-time programmable
- c. User-programmable, reprogrammable
- d. Manufacturer-programmable, reprogrammable

Answer: option A

81. How can uv erasable proms be recognized?

- a. There is a small window on the chip.
- b. They will have a small violet dot next to the #1 pin.
- c. Their part number always starts with a "u", such as in u12.
- d. They are not readily identifiable, since they must always be kept under a small cover.

Answer: option A

82. What part of a flash memory architecture manages all chip functions?

- a. I/o pins
- b. Floating-gate MOSFET
- c. Command code
- d. Program verify code

Answer: option B

83. An 8-bit address code can select _____.

- a. 8 locations in memory
- b. 256 locations in memory
- c. 65,536 locations in memory
- d. 131,072 locations in memory

Answer: option B

84. Eight bits of digital data are normally referred to as a:

- a. Group.
- b. Byte.
- c. Word.

d. Cell.

Answer: option B

85. Which is not a hard disk performance parameter?

- a. Seek time**
- b. Break time**
- c. Latency period**
- d. Access time**

Answer: option B

Explanation:-

Seek time is measured defines the amount of time it takes a hard drive's read/write head to find the physical location of a piece of data on the disk. Latency is the average time for the sector being accessed to rotate into position under a head, after a completed seek.

86. The ideal memory _____.

- a. Has high storage capacity**
- b. Is nonvolatile**
- c. Has in-system read and write capacity**
- d. Has All of the above characteristics**

Answer: option D

87. To which pin on the ram chip does the address decoder connect in order to signal which memory chip is being accessed?

- a. The address input**
- b. The output enable**
- c. The chip enable**
- d. The data input**

Answer: option C

88. EEPROM stands for _____.

- a. Encapsulated electrical programmable read-only memory**
- b. Elementary electrical programmable read-only memory**
- c. Electrically erasable programmable read-only memory**
- d. Elementary erasable programmable read-only memory**

Answer: option C

89. L1 is known as _____.

- a. Primary cache**
- b. Secondary cache**
- c. Dram**
- d. SRAM**

Answer: option A

- 90. Describe the timing diagram of a write operation.**
- a. First the data is set on the data bus and the address is set, then the write pulse stores the data
 - b. First the address is set, then the data is set on the data bus, and finally the read pulse stores the data.
 - c. First the write pulse stores the data, then the address is set, and finally the data is set on the data bus.
 - d. First the data is set on the data bus, then the write pulse stores the data, and finally the address is set.

Answer: option A

- 91. What is the bit storage capacity of a rom with a 1024×8 organization?**

- a. 1024
- b. 2048
- c. 4096
- d. 8192

Answer: option D

Explanation:-

$$1024 = 2^{10}.$$

$$2^{10} \cdot 2^3 = 1024 \cdot 8 = 8192.$$

- 92. Which of the following is one of the basic characteristics of drams?**

- a. Drams must have a constantly changing input.
- b. Drams must be periodically refreshed in order to be able to retain data.
- c. Drams have a broader "dynamic" storage range than other types of memories.
- d. Drams are simpler devices than other types of memories.

Answer: option B

- 93. The main advantage of semiconductor ram is its ability to:**

- a. Retain stored data when power is interrupted OR turned off
- b. Be written to and read from rapidly
- c. Be randomly accessed
- d. Be sequentially accessed

Answer: option B

- 94. Which of the following describes the action of storing a bit of data in a mask rom?**

- a. A 1 is stored in a bipolar cell by opening the base connection to

- the address line.
- b. A 0 is stored in a bipolar cell by shorting the base connection to the address line.
 - c. A 1 is stored by connecting the gate of a mos cell to the address line.
 - d. A 0 is stored by connecting the gate of a mos cell to the address line.

Answer: option C

95. Address decoding for dynamic memory chip control may also be used for:

- a. Controlling refresh circuits
- b. Read and write control
- c. Chip selection and address location
- d. Memory mapping

Answer: option C

True/false

1..static memory will maintain storage even if power is removed.

- a. True
- b. False

Answer: option B

2. Static rams (srams) use internal capacitors as basic storage elements.

- a. True
- b. False

Answer: option B

Explanation:-

Mainly transistors.

3. A burst refresh and a normal memory operation of a dram can be interspersed.

- a. True
- b. False

Answer: option B

4. Roms are used to store data that generally cannot be easily changed.

- a. True
- b. False

Answer: option A

5. Ram stands for readily accessible memory.

- a. True
- b. False

Answer: option B

6. If a memory design allows a storage location to be accessed without first sequencing through other locations, it is called random access memory.

- a. True
- b. False

Answer: option A

7. An optical disk is an example of magnetic storage.

- a. True
- b. False

Answer: option B

8. The address-decoding scheme for a 16k-bytEEPROM memory system requires a 1-to-8-address decoder when $4k \times 8$ memory is used.

- a. True
- b. False

Answer: option A

9. The time from the beginning of a read cycle to the point when the data output is valid is called propagation delay.

- a. True
- b. False

Answer: option B

10. Due to their ability to be easily erased and reused, magnetic memory devices are widely used for ram.

- a. True
- b. False

Answer: option B

11. The tms44100 4m \times 1 dram does not have a chip select (sc) input.

- a. True
- b. False

Answer: option A

12. The highest-speed magnetic storage is achieved by using a floppy disk.

- a. True
- b. False

Answer: option B

13. The floating-gate MOSFET is the actual storage element for eeproms. An electron charge will remain on the floating gate for more than 10 years unless drained off electrically.

- a. True
- b. False

Answer: option A

14. Roms are used to store data on a permanent basis.

- a. True
- b. False

Answer: option A

15. The time delay called access time, t_{ac} , is a measure of the rom's operating speed.

- a. True
- b. False

Answer: option B

16. A typical ram will read (place stored data on its outputs) whenever the chip select line is active and the write enable line is inactive.

- a. True
- b. False

Answer: option A

17. A group of 6 bits is also known as 1 byte.

- a. True
- b. False

Answer: option B

18. Erasing OR programming a flash memory device is a one-step operation.

- a. True
- b. False

Answer: option B

Explanation:-

No it's not one step operation because although flash memory is technically a type of **EEPROM**, the term "**EEPROM**" is generally used to refer specifically to non-flash **EEPROM** which is erasable in small blocks, typically

bytes. [citation needed] because erase cycles are slow, the large block sizes used in flash memory erasing give it a significant speed advantage over non-flash **EEPROM** when writing large amounts of data.

19. EEPROM and flash memory are electrically erasable.

- a. True
- b. False

20. RAMs must have a READ/WRITE input, in addition to data in.

- a. True
- b. False

Answer: option A

21. EEPROM is strictly a mos device.

- a. True
- b. False

Answer: option A

22. A term often used commercially to refer to read/write memory is sequential-access memory.

- a. True
- b. False

Answer: option B

23. DRAM chips can be combined for larger capacity and word sizes using the same methods as for other memory types.

- a. True
- b. False

Answer: option A

24. More than one bit of data can occupy each memory cell.

- a. True
- b. False

Answer: option B

25. Flash memories are frequently used in place of floppy OR small-capacity hard disk drives in portable computers.

- a. True
- b. False

Answer: option A

26. A nibble is a group of eight bits.

- a. True

b. False

Answer: option B

27. Fusible-link proms are programmed by removing the desired fuse links using a microscope and tweezers.

a. True

b. False

Answer: option B

28. When a computer is executing a program of instructions, the cpu continually fetches information from those locations in memory that contain (1) the program codes representing the operations to be performed and (2) the data to be operated upon.

a. True

b. False

Answer: option A

29. A rom that allows the user to program data into the chip by permanently opening fusible links is the EEPROM.

a. True

b. False

Answer: option B

30. A write operation may also be referred to as a "fetch" operation.

a. True

b. False

Answer: option B

31. Address multiplexing is used to reduce the number of address lines.

a. True

b. False

Answer: option A

32. Proms are basically the same as mask roms, once they have been programmed.

a. True

b. False

Answer: option A

33. Ram is nonvolatile.

a. True

b. False

Answer: option B

34. Cache memory is used in high-speed systems.

- a. True
- b. False

Answer: option A

35. Dynamic memories, such as the 2118 16k × 1 ram, have to multiplex the address bus.

- a. True
- b. False

Answer: option A

36. Rom is a type of memory in which data are stored permanently OR semipermanently.

- a. True
- b. False

Answer: option A

37. Eeproms can be electrically erased and reused.

- a. True
- b. False

Answer: option A

Explanation:-

EEPROM (also written e2prom and pronounced "EEPROM", "doubl**E**EPROM", "e-squared", OR simply "EEPROM") stands for electrically erasable programmable read-only memory and is a type of non-volatile memory used in computers and other electronic devices to store small amounts of data that must be saved when power is removed.

38. Dram uses a cross-transistor configuration.

- a. True
- b. False

Answer: option B

Explanation:-

Dynamic random-access memory (dram) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit.

39. Main computer memory is usually dram because of its high density and low cost; cache memory is usually SRAM because of its high speed.

- a. True
- b. False

Answer: option A

40. Information stored in an EEPROM can be erased by prolonged exposure to ultraviolet light.

a. True

b. False

Answer: option A

41. A cd player is an example of a device that has random access capability.

a. True

b. False

Answer: option A

42. The most widespread application of roms is in the storage of data and program codes that must be available on power-down in the microprocessor-based systems. These data and program codes are called firmware because they are firmly stored in hardware.

a. True

b. False

Answer: option B

43. One of the advantages of drams is their ability to store data without needing periodic refreshment of the memory contents.

a. True

b. False

Answer: option B

44. A typical ram will write (store data internally) whenever the chip select line is active and the write enable line is inactive.

a. True

b. False

Answer: option B

45. When two OR more devices try to send their own digital levels to a shared data bus at the same time, bus contention will take place.

a. True

b. False

Answer: option A

46. The main advantage of bipolar (TTL) memories over mos memories is speed.

a. True

b. False

Answer: option B

47. Testing and troubleshooting the decoding logic will not reveal problems with the memory chips and their connections to the cpu busses.

- a. True
- b. False

Answer: option A

48. Once a PROM is programmed it can be changed by applying a small electrical charge.

- a. True
- b. False

Answer: option B

49. In a register stack, data moves up but not down.

- a. True
- b. False

Answer: option B

50. Most flash chips use a bulk erase operation in which all cells on the chip are erased simultaneously.

- a. True
- b. False

Answer: option A

FILL IN THE BLANKS

1. Assume a rom to be tested is compared with a known good rom. If the checksums differ, the rom is _____.

- a. Very likely to be good
- b. Definitely good
- c. Very likely to be bad
- d. Definitely bad

Answer: option D

2. The checkerboard pattern test is used to test _____.

- a. Rom
- b. EEPROM
- c. FPLA
- d. Ram

Answer: option D

3. Information that is stored in an EEPROM _____.

- a. Can be modified by performing a memory write operation
- b. Is stored by the manufacturer and cannot be changed
- c. Is lost if power is interrupted
- d. Can be erased by applying high voltage to each storage location

Answer: option D

4. The difference between ram and rom is that _____.

- a. Ram has a read/write signal and rom doesn't
- b. Ram will lose data when the power is removed and rom won't
- c. Ram has random address access and rom uses sequential address access
- d. Ram has a read/write signal and rom doesn't; ram will lose data when the power is removed and rom won't.
- e. All of the above

Answer: option D

5. The tms44100 has _____ address inputs.

- a. 10
- b. 11
- c. 12
- d. 13

Answer: option B

6. A type of memory that is accessed serially (one location after the other) is a _____.

- a. Rom
- b. Read/write memory
- c. Shift register
- d. PLD

Answer: option C

7. The basic purpose of Tri-State OR open-collector outputs on a memory is to _____.

- a. Isolate devices connected to a common bus
- b. Simplify the circuitry
- c. Provide faster transitions of the output
- d. Increase the output current

Answer: option A

8. The checksum method is used to test _____.

- a. Rom
- b. EEPROM

c. FPLA

d. Ram

Answer: option A

9. Because $4096 = 2^{12}$, a $4k \times 1$ ram requires _____ address bits to access all locations.

a. 4096

b. 10

c. 12

d. 1024

Answer: option C

10. To reduce the number of pins on high-capacity dram chips, address _____ is used so that a single pin can accommodate two different address bits.

a. Conversion

b. Programming

c. Multiplexing

d. Firmware

Answer: option C

11. The number of $16k \times 4$ memories needed to construct a $128k \times 8$ memory is _____.

a. 4

b. 8

c. 12

d. 16

Answer: option D

Explanation:-

Here 16k represents the address lines and 4 represents data lines. And thus the memory size will be $16 \times 4 = 64k$.

Similarly required memory size is $128 \times 8 = 1024k$.

Now $64k \times 16 = 1024k$ = required memory size. Hence 16.

12. The minimum number of address lines needed for a $64k$ memory is _____.

a. 10

b. 12

c. 14

d. 16

Answer: option D

Explanation:-

$2^{10} = 1024$ (~1000), 10 address line,

$64 = 2^6$ = 6 address line

$64000 = 64k = (2^6) * (2^{10})$

$= 2^{(10+6)}$;

$= 2^{16}$;

so it requires 16 address lines

13. The 2147 4k × 1 static ram contains 4096 storage locations storing one bit each. _____ 2147 ram memory chip(s) is/are needed to configure an 8k × 8 memory.

- a. One
- b. Four
- c. Eight
- d. Sixteen

Answer: option D

Explanation:-

$$4k * 1 = 4 * 1024 * 1$$

$$= 4096.$$

Similarly

$$8k * 8 = 8 * 1024 * 8$$

$$= 65536.$$

$$2147 \text{ 4k} * 1 = 4096$$

$$2147 \text{ 8k} * 8 = 65536 / 4096$$

$$= 16.$$

14. A CD-ROM is a form of read-only memory in which data are stored as _____.

- a. Magnetic "bubbles"
- b. Magnetized spots
- c. "pits" on an optical disk
- d. Tiny "pinholes" in an opaque substance

Answer: option C

15. A type of read/write memory available with mos technology is _____.

- a. SRAM
- b. DRAM
- c. Both of the above
- d. None of the above

Answer: option C

16. All rows in a 2118 dynamic ram need to be refreshed _____.

- a. Every second

- b. Every millisecond
- c. Every 50 milliseconds
- d. Every 2 milliseconds

Answer: option D

- 17. Rom access time is defined as _____.**
- a. How long it takes to program the rom chip
 - b. Being the difference between the read and write times
 - c. The time it takes to get valid output data after a valid address is applied
 - d. The time required to activate the address lines after the enable line is at a valid level

Answer: option C

- 18. In dram operations, it is assumed that r/w is in its _____ state during a _____ operation.**
- a. High, read
 - b. Hi-z, write
 - c. High, write
 - d. Hi-z, read

Answer: option A

- 19. The major advantage of dynamic ram over static ram is _____.**
- a. Cost
 - b. Speed
 - c. Storage density
 - d. Cost and storage density

Answer: option D

- 20. The address space of a ram memory can be expanded using a decoder and additional memory ics. The output of the decoder should be connected to which input line of the memory?**
- a. The most significant address inputs
 - b. The most significant data inputs
 - c. The read/write line
 - d. The chip enable

Answer: option D

- 21. The memory operation that presents data on the memory outputs after entering a new address is called _____.**
- a. A read cycle
 - b. A write cycle
 - c. A refresh cycle

d. A chip select

Answer: option A

22. Dynamic memory is memory _____.

- a. That will maintain storage even if power is removed**
- b. Whose data can never be altered**
- c. That must be refreshed periodically OR it will lose storage**
- d. That maintains storage as long as power is applied**

Answer: option C

23. Because of their nonvolatility, high speed, low power requirements, and lack of moving parts, _____ have become feasible alternatives to magnetic disk storage.

- a. CD-ROMs**
- b. Flash memory modules**
- c. Roms**
- d. Eproms**

Answer: option B

24. The memory operation that stores data into a memory location after entering a new address is called _____.

- a. A read cycle**
- b. A write cycle**
- c. A refresh cycle**
- d. Chip select**

Answer: option B

25. A dimm _____.

Is available in 30-pin OR 72-pin packages

- a. Has contact pins on only one side of the module**
- b. Has less memory than the newer simm modules**
- c. Has contact pins on both sides of the module for larger data paths**

Answer: option C

26. When the term ram is used with semiconductor memories, it usually means _____ as opposed to rom.

- a. Random-access memory**
- b. Read/write memory (rwm)**
- c. Flash memory**
- d. Temporary storage**

Answer: option B

27. Dynamic rams store information by using _____.

- a. Magnetism
- b. Flip-flops
- c. Latches
- d. Capacitors

Answer: option D

28. When more than one ic is used to provide all the addressable locations in a memory, a technique called _____ is used to identify which ic is being accessed.

- a. Address decoding
- b. Memory refresh
- c. Data encoding
- d. Memory paging

Answer: option A

29. The periodic recharging of dynamic ram memory cells is called _____.

- a. Reinstalling
- b. Revitalizing
- c. Refreshing
- d. Reinstating

Answer: option C

30.a(n) _____ is user programmable and can also be erased electronically and reprogrammed as often as desired.

- a. PROM
- b. Rom
- c. EEPROM
- d. EEPROM

Answer: option C

31. A fifo _____.

- a. Allows data to be clocked in and out at different clock rates
- b. Outputs the data in the same order that it was input
- c. Can be used to smooth out bursts of data into a continuous stream
- d. All of the above

Answer: option D

32. Proms are programmed by _____ fuses.

- a. Zapping
- b. Blowing
- c. Charging
- d. Inputting

Answer: option A

33. A dram has a ras and a cas because _____.

- a. The address lines are multiplexed to reduce pin count
- b. The ras determines the operation mode and the cas enables the Tri-State outputs
- c. The ras latches in the address and the cas latches in data
- d. None of the above

Answer: option A

34. Floppy disks are organized into concentric rings called _____.

- a. Tracks
- b. Arrays
- c. Sectors
- d. Cells

Answer: option A

35. Read-only memory is memory _____.

- a. That has unlimited storage capacity
- b. Whose data can never be altered by the user
- c. That must be refreshed periodically OR it will lose storage
- d. That maintains storage as long as power is applied

Answer: option B

36. A _____ is user-programmable memory that cannot be erased and reprogrammed.

- a. Rom
- b. EEPROM
- c. EEPROM
- d. PROM

Answer: option D

37. A device that needs constant refreshing to avoid losing data is a(n) _____.

- a. SRAM
- b. Dram
- c. Rom
- d. EEPROM

Answer: option B

38. Information that is stored in a mask rom _____.

- a. Can be modified by using special equipment
- b. Is stored by the manufacturer and cannot be changed

- c. Is lost if power is interrupted**
- d. Can be modified by using special equipment and is lost if power is interrupted**

Answer: option B

39. Flash memories are so called because of the rapid _____ times.

- a. Read and write**
- b. Format and erase**
- c. Erase and read**
- d. Erase and write**

Answer: option D

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21.MSI LOGIC CIRCUITS

1.Which statement below best describes the function of a decoder?

A decoder will convert a decimal number into the proper binary equivalent.

- a) A decoder will convert a binary number into a specific output representing a particular character OR digit.
- b) Decoders are used to prevent improper operation of digital systems.
- c) Decoders are special ics that are used to make it possible for one brand of computer to talk to another.

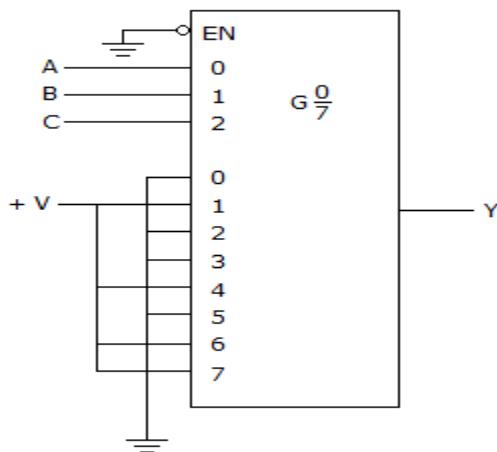
Answer: option B

2.One can safely state that the output lines for a Demultiplexer are under the direct control of the:

- a) Input data select lines.
- b) The internal AND Gates.
- c) The internal OR Gate.
- d) Input data line.

Answer: option A

3.Refer to the figure given below. The logic function generator being implemented with the multiplexer in this circuit produces a constant low on the output. The *abc* inputs are checked and appear to be pulsing; also, the 0-7 and en inputs are checked with the scope and all appear to be at 0v. A check with the dmm confirms that power is on. What is the problem, and what should be done to correct it?



- a) The output is shorted to v_{cc} ; replace the ic.
- b) The scope's vertical input is in the ac mode and the common connection for the 0,2,3 and 5 inputs is bad. Set the scope's

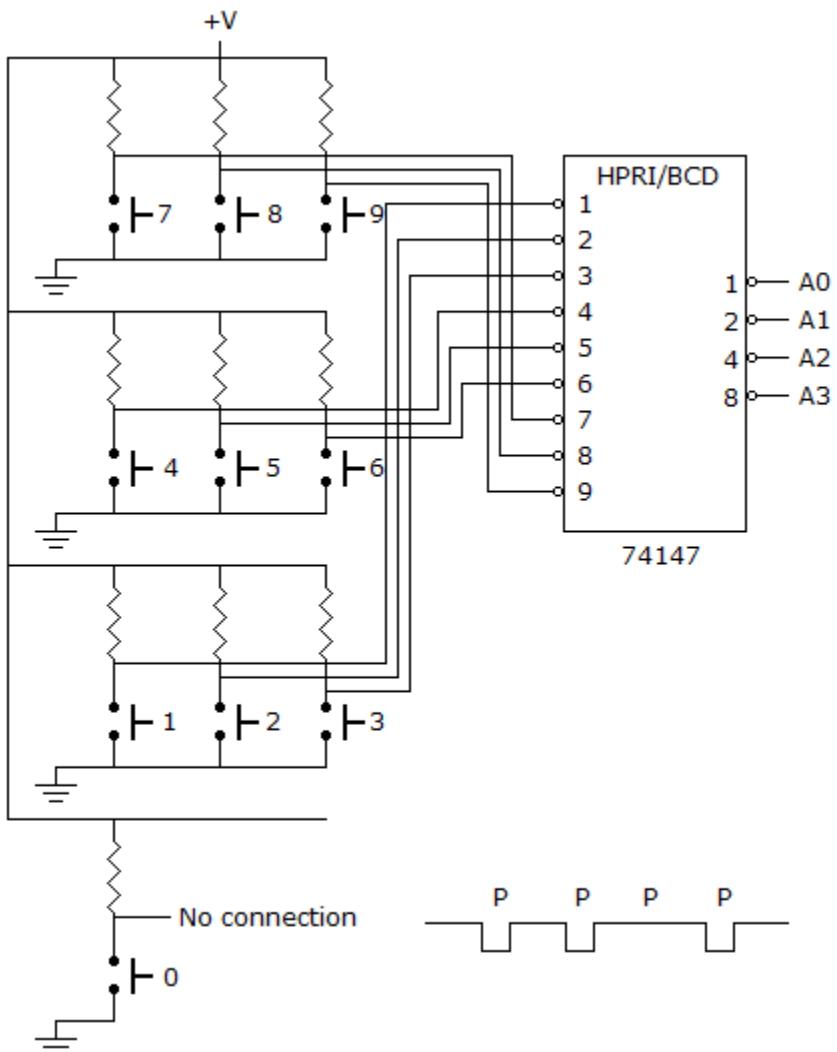
vertical input mode to dc, and repair the bad solder connection.

c) Power has not been applied to the circuit; apply power.

d) The output is shorted to ground; replace the ic.

Answer: option B

4. Refer to the keyboard encoder in figure (a). Sometimes when the 5 key is pressed, the system attached to the keypad does not respond. The 5 input on the 74147 is monitored with a digital storage scope while repeatedly pressing the 5 key, and the waveform in figure (b) is obtained; the p above the trace indicates the points at which the technician pressed the key. What is most likely wrong with the circuit?



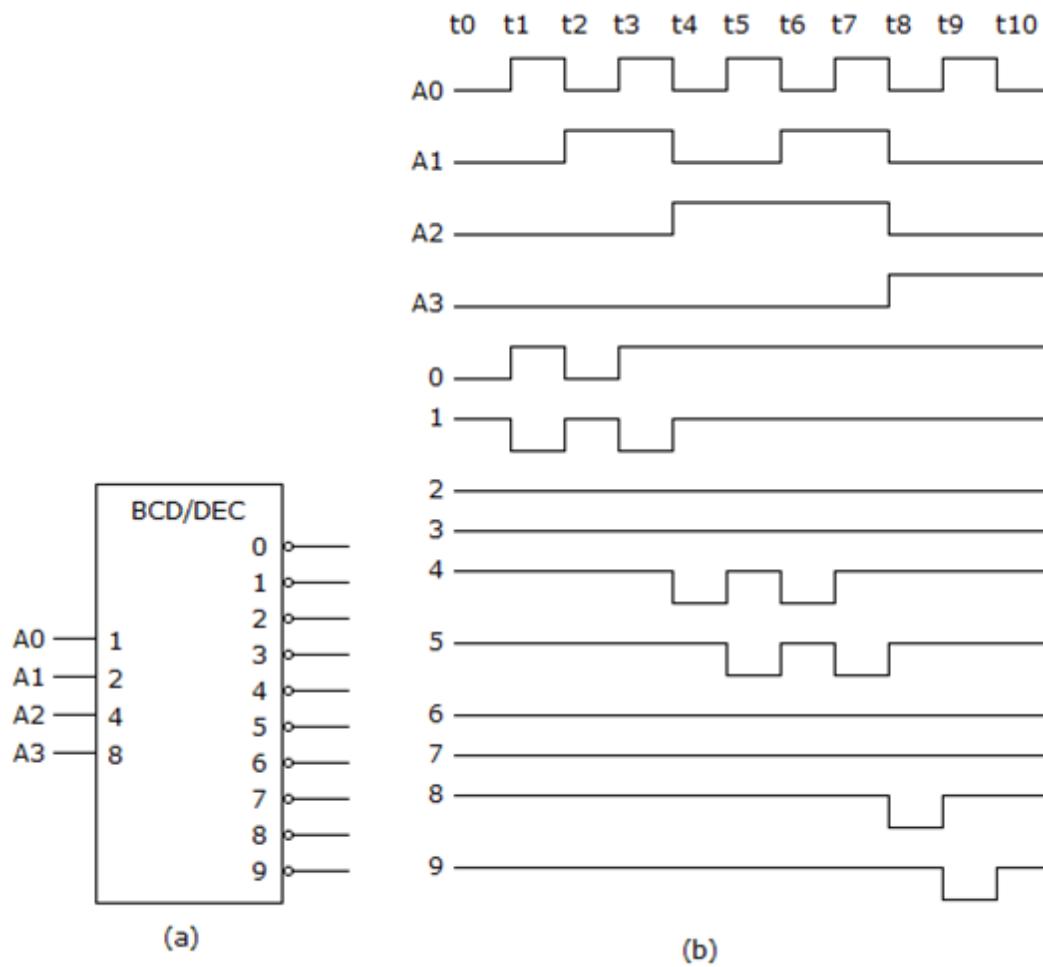
a) The switches on the 5 key are intermittent; the contacts need to be cleaned OR the switch replaced.

b) The pull-up resistor connected to the 5 key is bad and should be replaced.

- c) The common ground connection at the bottom of the 0 key has a bad solder connection; repair the connection.

Answer: option A

5. The BCD/dec decoder shown in figure (a) is examined with a logic analyzer and the results are shown in the waveforms in figure (b). What, if anything, is wrong with the circuit?



- a) The "2" output is shorted to V_{cc} .
b) The a1 input is internally open.
c) The a1 input node is internally stuck low.
d) Nothing is wrong with the circuit.

Answer: option C

6. A 16-input multiplexer is to be used to perform parallel-to-serial data conversion. Which of the following counters would be required to provide the data select inputs?

- a) Mod 8
b) Mod 16

- c) Mod 4
- d) Mod 2

Answer: option B

Explanation:-

We require counter that can go up to 16. Mod 16 = count 16.

7.A breadboard-circuit design using a BCD-to-decimal decoder has a problem wherein the operation of the system is erratic. The technician uses his scope to examine the waveforms throughout the system and doesn't really see any problems. While he's scratching his head, what helpful advice can you offer him as to what might be wrong and what to do to correct the problem? The decoder is thermally intermittent; replace it.

- a) The decoder is thermally intermittent; replace it.
- b) There is probably a bad connection on the wire wrap protoboard; recheck the wiring.
- c) Glitches are probably the culprit; strobe the decoder.
- d) The decoder is thermally intermittent and must be replaced; OR there is probably a bad connection on the wire wrap protoboard, and the wiring must be rechecked.

Answer: option C

8.Output 5 of a 74138 octal decoder is selected when it is enabled by a data input of:

$$A_0 = 1$$

$$A_1 = 1$$

a) $A_2 = 0$
 $A_0 = 1$

$$A_1 = 0$$

b) $A_2 = 1$
 $A_0 = 0$

$$A_1 = 1$$

c) $A_2 = 0$
 $A_0 = 1$

$$A_1 = 0$$

d) $A_2 = 0$

Answer: option B

Explanation:-

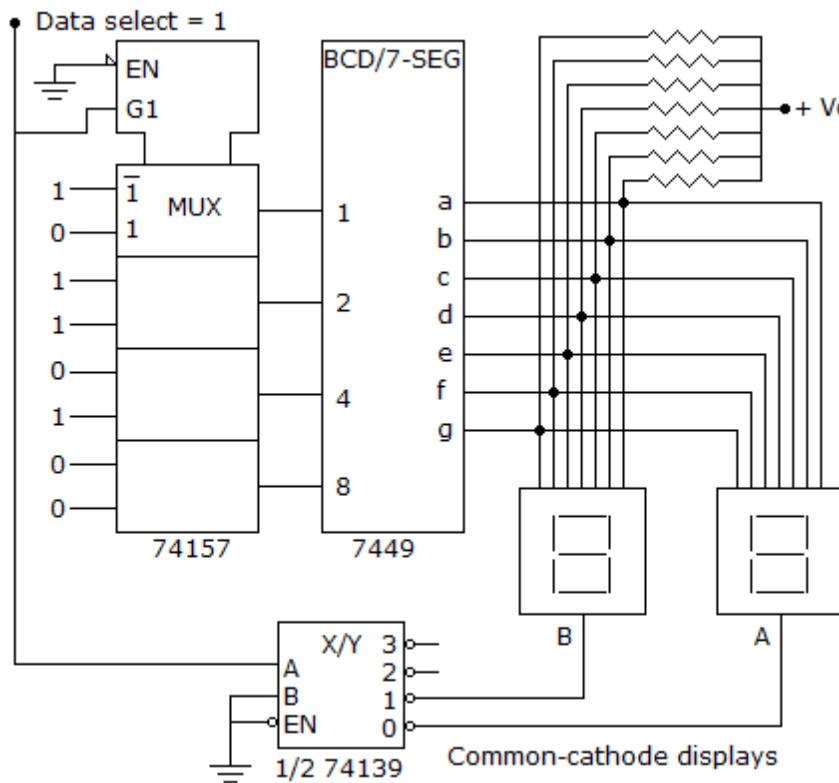
This is because 101 in octal = 5

9.How is the number one (1) indicated on the outputs of a 7447 BCD-to-seven-segment code converter?

- a) Segment a is active.
- b) Segment b is active.
- c) Segments a and b are active.
- d) Segments b and c are active.

Answer: option D

10.For the input values (a_0-a_3 , b_0-b_3 , data select = 1) given for the circuit given below, what will be indicated on the displays?

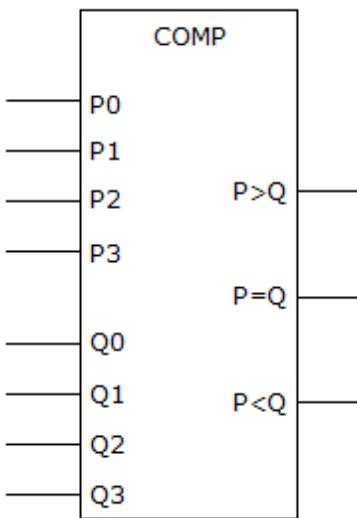


- a) $A = 0, b = 5$
- b) $A = 5, b = 0$
- c) $A = 6, b = 0$
- d) $A = 0, b = 6$

Answer: option D

11.It is suspected that the comparator in the figure given below has a problem. The inputs are activated in the table shown below and the corresponding outputs noted. What is most likely wrong with the circuit?

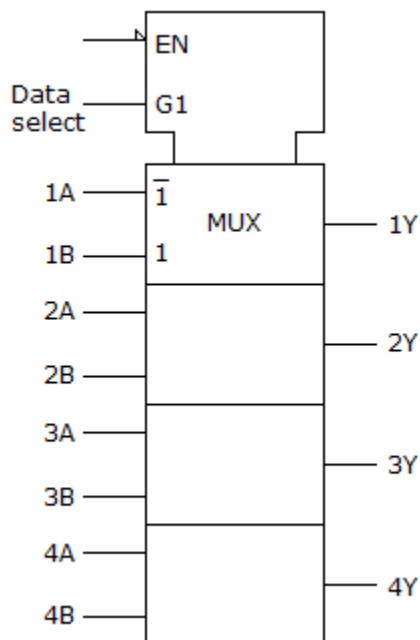
For $p_0 - p_3 = 1$ and $q_0 - q_3 = 0$, $p > q = 1$, $p = q = 1$, $p < q = 0$
for $p_0 - p_3 = 0$ and $q_0 - q_3 = 1$, $p > q = 0$, $p = q = 1$, $p < q = 1$
for $p_0 - p_3 = 1$ and $q_0 - q_3 = 1$, $p > q = 0$, $p = q = 1$, $p < q = 0$



- a) The p_0-p_3 inputs are defective.
- b) One OR more of the q inputs is bad.
- c) The $p = q$ output is shorted to v_{cc} .
- d) Nothing is wrong; the circuit is functioning properly.

Answer: option C

12. Which statement best describes the given figure, and what is the function of the terminal labeled en?

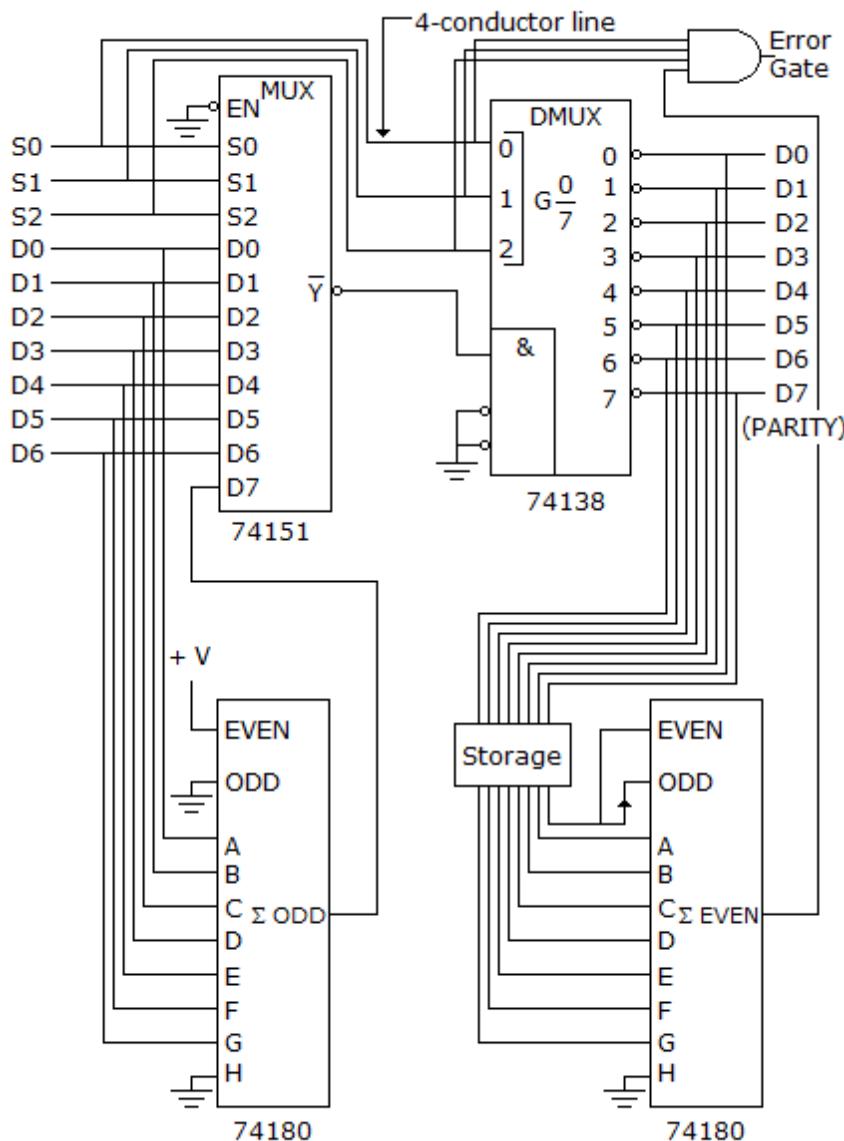


- a) Quad two-input multiplexer. En is the enable input, which

- requires an active low for the device to work.
- Quad two-bit multiplier, en is the active high trigger.
 - Dual quad-input multiplexer, which requires an active low on the en terminal for the device to work.
 - Quad two-input AND Gate, which requires an active low on the en input to enable all the gates.

Answer: option A

13. The data transmission system shown in below has a problem; the parity error output is always high. A logic analyzer is used to examine the system and shows that the data in on the left matches the data out on right. What might be causing the problem?



- The errOR Gate could be defective.

- b) The storage circuit could be defective.
- c) The parity checker could be bad.
- d) Any of the above.

Answer: option D

14. The ieee/ansi symbol for a decoder has the internal designation BCD/dec. This means the decoder is a:

- a) Decimal-to-BCD decoder with ten inputs and four outputs.
- b) BCD-to-decimal decoder with ten inputs and four outputs.
- c) Decimal-to-BCD decoder with four inputs and ten outputs.
- d) BCD-to-decimal decoder with four inputs and ten outputs.

Answer: option D

15. Multiplexing of digital signals is usually required when:

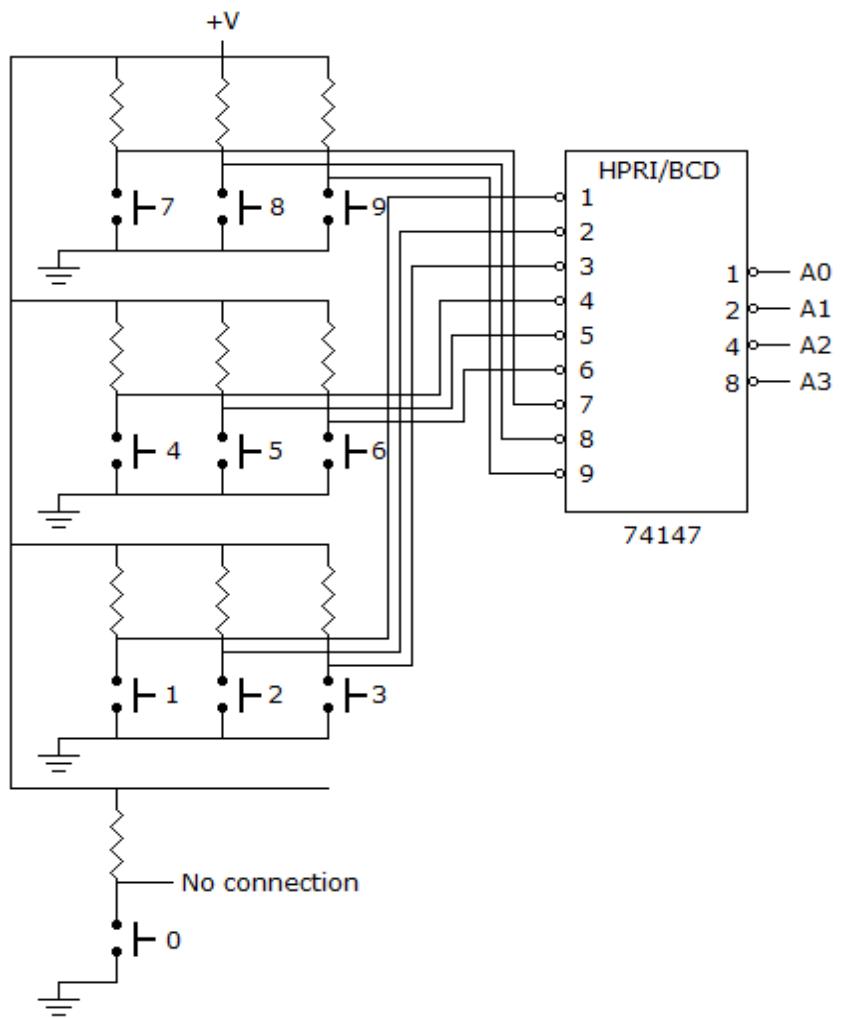
- a) Moving data internally within a microprocessor.
- b) Moving data between memory and storage registers in a microprocessor.
- c) Moving data over long distance transmission lines.
- d) Moving data internally within a microprocessor OR between memory and storage registers.

Answer: option C

Explanation:-

For long distance transmission we use modulation means super imposing base band signal on carrier signal. If we need to send 2 OR more than 2 base band signal then multiplexing is required. While in case of data transfer in microprocessor we have to multiplex for address and data bus. So right answer should be d.

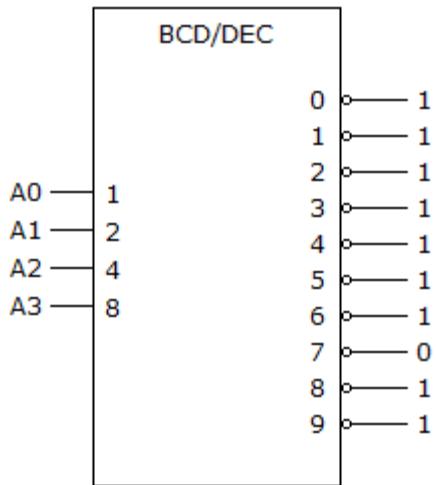
16. Referring to the figure given below, what output code will appear on the output (a₃,a₂,a₁,a₀) when the 5 key is pressed?



- a) 1010
 - b) 0101
 - c) 1101
 - d) 1011

~~Answer: option A~~

17.What type of device is shown in the given figure, and what inputs (a_3, a_2, a_1, a_0) are required to produce the output levels as shown?



- a) A binary-to-decimal encoder; 0,1,1,1
- b) A decimal-to-binary decoder; 1,1,1,0
- c) A BCD-to-decimal decoder; 0,1,1,1
- d) A decimal-to-BCD encoder; 1,1,1,0

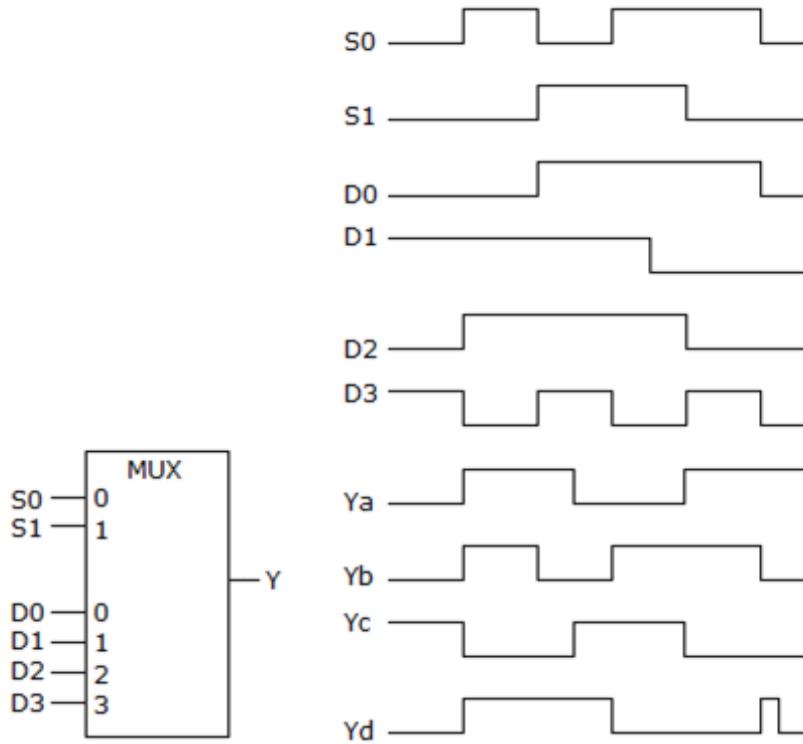
Answer: option C

18.What are the outputs of a 7485 four-bit magnitude comparator when the inputs are $a = 1001$ and $b = 1010$?

- a) $A < b$ is 1
 $a = b$ is 0
 $a > b$ is 1
- b) $A < b$ is 0
 $a = b$ is 1
 $a > b$ is 0
- c) $A < b$ is 0
 $a = b$ is 0
 $a > b$ is 1
- d) $A < b$ is 1
 $a = b$ is 0
 $a > b$ is 0

Answer: option D

19.Determine the correct output for the multiplexer and its associated timing diagram given below.



- a) Ya
- b) Yb
- c) Yc
- d) Yd

Answer: option D

20. Which is the decimal number for the BCD number, 10110110?

- a) 182
- b) 36
- c) 116
- d) 10110110 is not a valid BCD number.

Answer: option D

21. In an aHDL BCD to binary code converter, how is multiplication by 10 accomplished?

- a) By using the shifting of bits
- b) By using the library multiplication function
- c) By using integer types
- d) By using the multiplication operator

Answer: option A

22. What is the HDL key issue in the design of the mux and demux?

- a) Having the mux and demux part of the library
- b) Using the case statement in the process

- c) Describing the functions
- d) Assigning signals under certain conditions

Answer: option D

23.Why are control inputs included in an HDL magnitude comparator?

- a) For cascading the chips
- b) For control signal input
- c) For signal control
- d) For internal interconnections

Answer: option A

24.What VHDL techniques are used to describe a priority encoder?

- a) Integer outputs and priority coding
- b) Signal outputs and priority coding
- c) Tri-State outputs and priority coding
- d) Variables and priority coding

Answer: option C

25.What is an important attribute of the conditional signal assignment statement?

- a) Its Tri-State outputs
- b) Its sequential evaluation
- c) Its use of library components
- d) Its fast activation times

Answer: option B

26.There appears to be a problem with a 7-segment display on a dmm sometimes skipping certain numbers. How would you test the display?

- a) Remove the display unit and check each segment diode with an ohmmeter. Replace the defective segments.
- b) Apply 5v directly to each segment of the display and check for individual segment operation. Replace any segment that has voltage applied but is not lit.
- c) Tie all of the segments together and connect to V_{cc} ; the number 8 should appear on the display. Now check the display supply voltage to determine if the display is receiving the correct voltage.
- d) Connect the dmm to a variable supply and very slowly increase the voltage, while observing for missing digits. Then check the segment voltage to determine whether the display OR the display driver is bad.

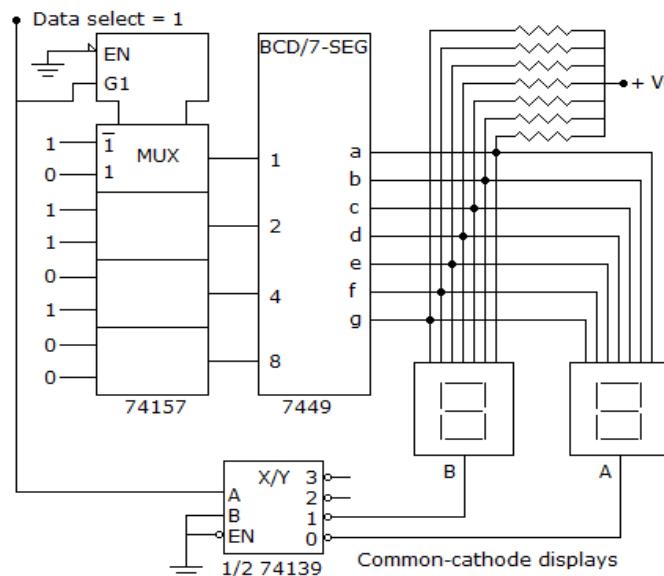
Answer: option D

27.What is the purpose of a decoder's inputs?

- a) To allow the decoder to respond to the inputs to activate the correct output gate.
- b) To disable the decoder outputs so that all outputs will be inactive.
- c) To disable the inputs and activate all outputs.
- d) To allow the decoder to respond to the inputs to activate the correct output gate, and to disable the inputs and activate all outputs.

Answer: option D

28.Refer to the display multiplexer given below. The msd display is blank, while the lsds seems to be ok. The input and output lines to the 74157 and 7449 are checked with a scope and can be seen changing levels. The a input on the 74139 also changes; however, the 0 output on the 74139 is always low and the 1 output is always high. The b and en inputs on the 74139 are always low. What could cause the problem and what should be done to correct it?



- a) The 74139 is defective; replace it.
- b) The en pin on the 74139 could have a bad connection; check the connection.
- c) The 74139 is defective and must be replaced; OR the en pin on the 74139 could have a bad connection, which should be checked.
- d) The msd display is bad; replace it.

Answer: option C

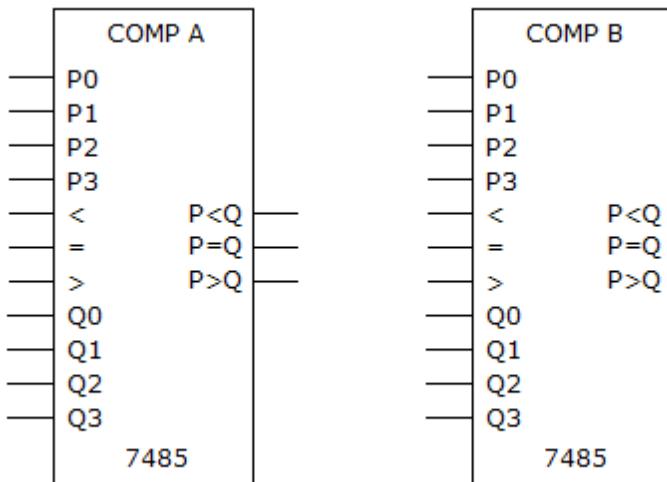
29.The circuit in figure 9-8 is defective; data is not appearing on the

output lines. A check with the scope shows data pulses on the serial data line and multiplex control lines, s_0-s_2 ; no parity error is indicated. A further check with a logic probe indicates that v_{cc} and ground appear to be present. What might be wrong with the circuit?

- a) The Demultiplexer may be bad.
- b) The parity checker is defective.
- c) The parity generator may be bad.
- d) The parity checker is defective, OR the parity generator may be bad.

Answer: option A

30. What must be done in the given figure in order to use two 7485 4-bit comparators to compare two 8-bit numbers?



- a) The $p < q$, $p = q$, and $p > q$ outputs of comp a must be connected to the same outputs of comp b.
- b) The $p < q$, $p = q$, and $p > q$ outputs of comp a must be connected to the $<$, $=$, and $>$ inputs of comp b. The $=$ input of comp a must be connected to v_{cc} , and the $<$ and $>$ inputs must be connected to ground.
- c) The $p < q$, $p = q$, and $p > q$ outputs of comp a must be connected to the $<$, $=$, and $>$ inputs of comp b, the $=$ input of comp a must be connected to v_{cc} , and the $<$ and $>$ inputs must be connected to ground.

Answer: option D

TRUE/FALSE

1. A device that selects one of several inputs to be placed on the output is a multiplexer.

A) True

B)False

Answer: option A

2.A logic circuit that determines if one input is equal to another is called a comparator.

A)True

B)False

Answer: option A

3.A variable can be thought of as a piece of scrap paper used to write down some numbers that can be used later.

A)True

B)False

Answer: option A

4.Output 3 of a 74138 octal decoder is selected when it is enabled by a data input of:

$a_0 = 1$

$a_1 = 1$

$a_2 = 0$

A)True

B)False

Answer: option A

Explanation:-

Output y_3 is enabled but that isn't really output 3 as the inputs for 000 are output 1 so 010 should be output 3 surely? Even though binary 3 is 011.

5.When data input i_1 of a 74148 octal-to-binary encoder is active, the data output is:

$A_0 = 0$

$a_1 = 0$

$a_2 = 1$

A)True

B)False

Answer: option B

6.A four-line multiplexer must have as inputs four data inputs and two select inputs.

A)True

B)False

Answer: option A

7.In HDL, a process is usually thought of as a wire connecting two points in a circuit.

A)True

B)False

Answer: option B

8.A Demultiplexer is a device that converts some code to a recognizable number OR character.

A)True

B)False

Answer: option B

9.Output 6 of a 74138 octal decoder is selected when it is enabled by a data input of:

$A_0 = 1$

$a_1 = 1$

$a_2 = 0$

A)True

B)False

Answer: option B

10.A circuit that converts some binary code into a singular active output representing its numerical value is a comparator.

A)True

B)False

Answer: option B

11.All outputs of the 74138 octal decoder are disabled (high) when the enable inputs are:

$\bar{E}_1 = 0, \bar{E}_2 = 0, \text{ and } \bar{E}_3 = 0$

$\bar{E}_1 = 0, \bar{E}_2 = 1, \text{ and } \bar{E}_3 = 1$

$\bar{E}_1 = 1, \bar{E}_2 = 1, \text{ and } \bar{E}_3 = 0$

A)True

B)False

Answer: option A

12.Incandescent 7-segment displays are especially well suited for use in portable battery-operated devices.

A)True

B)False

Answer: option B

13.The device that is an application of SOP logic is a multiplexer.

A)True

B)False

Answer: option A

14. Adhl does not offer a multiplication operator.

- A)True**
- B)False**

Answer: option A

15. The outputs of a 7485 four-bit magnitude comparator when the inputs are $a = 0110$ and $b = 1010$ are:

- A $< b$ is 1**
- $a = b$ is 0**
- $a > b$ is 1**
- A)True**
- B)False**

Answer: option B

Explanation:-

Because the decimal equivalent of 0110 is 6 and the decimal equivalent of 1010 is 10.

16. In order to select data input i_3 of a 74151 eight-line multiplexer, the select inputs must be:

- $\bar{E} = 0$**
- $\bar{S}_0 = 1$**
- $\bar{S}_1 = 1$**
- $\bar{S}_2 = 0$**

- A)True**
- B)False**

Answer: option A

17. A very important attribute of the conditional signal assignment statement is its sequential operation.

- A)True**
- B)False**

Answer: option A

18. The outputs of the 74138 octal decoder are enabled when the enable inputs are

- $\bar{E}_1 = 0, \bar{E}_2 = 0,$ and $\bar{E}_3 = 1$**

- A)True**
- B)False**

Answer: option A

19.A multiplexer is a device that converts some code into a recognizable number OR character.

- A)True**
- B)False**

Answer: option B

20.A Demultiplexer takes an input and turns it into a binary number.

- A)True**
- B)False**

Answer: option B

21.In order to select data input i_1 of a 74151 eight-line multiplexer, the select inputs must be:

$$\bar{E} = 0$$

$$\bar{S}_0 = 1$$

$$\bar{S}_1 = 0$$

$$\bar{S}_2 = 0$$

- A)True**
- B)False**

Answer: option A

22.A device that determines which of two numbers is greater is a comparator.

- A)True**
- B)False**

Answer: option A

23.When outputs a, BCD, and g of a 7447 BCD-to-seven-segment code converter are active, the number displayed is 5.

- A)True**
- B)False**

Answer: option B

Explanation:-

Those segments displays 3

24.When data input i_4 of a 74148 octal-to-binary encoder is active, the data output is:

- $a_0 = 1$
- $a_1 = 1$
- $a_2 = 0$

A)True

B)False

Answer: option A

25.It is normal for more than one decoder output to be active at the same time.

A)True

B)False

Answer: option B

26.When data input i_5 of a 74148 octal-to-binary encoder is active, the data output is:

$a_0 = 1$

$a_1 = 0$

$a_2 = 0$

A)True

B)False

Answer: option B

27.Basically, a multiplexer changes parallel data inputs to a serial output.

A)True

B)False

Answer: option A

28.The 74139 dual four-line Demultiplexer functions as a Demultiplexer if data input is on the \bar{E} line.

A)True

B)False

Answer: option A

29.Modern computers transfer data between different devices over a common set of connecting lines called a data bus.

A)True

B)False

Answer: option A

30.The select inputs to a multiplexer may also be called address lines.

A)True

B)False

Answer: option A

Fill in the blank

1.A(n) _____ is a combinational logic circuit that compares two

input binary quantities and generates outputs to indicate which one has the greater magnitude.

- a) Demultiplexer
- b) Code converter
- c) Magnitude comparator
- d) E-mos

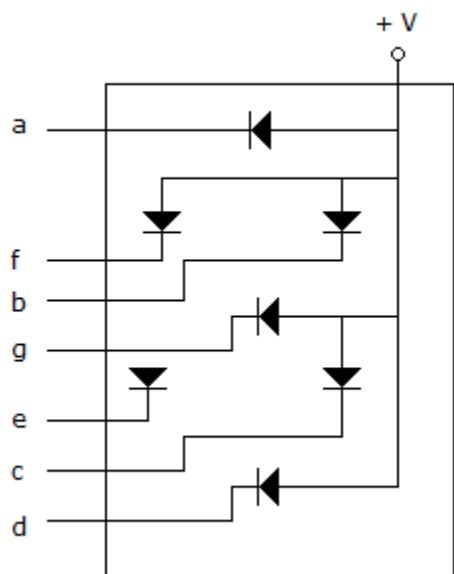
Answer: option C

2.If by chance more than one of the inputs in an HDL encoder is activated at the same time, the priority encoder _____.

- a) Enters a fault mode
- b) Ignores the least significant input
- c) Resamples the data
- d) Finds some other input

Answer: option B

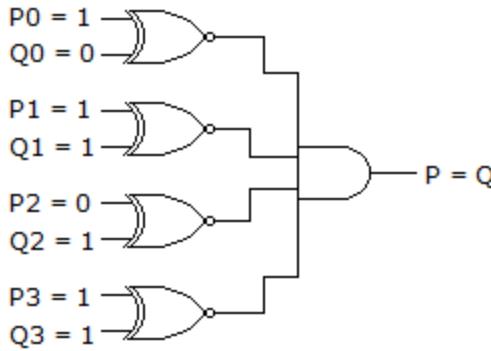
3.The diagram given below shows a _____, and in order for the decimal number 3 to be displayed, terminals _____ must be _____.



- a) Common-cathode seven-segment display, ef, low
- b) Common-anode seven-segment display, aBCDg, high
- c) Common-anode seven-segment display, aBCDg, low
- d) Common-cathode seven-segment display, aBCDg, high

Answer: option C

4.The circuit shown below is a(n) _____.



- a) 4-bit magnitude comparator
- b) 4-bit half adder
- c) 8-bit comparator
- d) 8-bit binary adder

Answer: option A

5. The device that generates a coded output from a single active numeric input line is _____.

- a) A decoder
- b) A multiplexer
- c) A comparator
- d) An encoder

Answer: option D

6. The 74139 dual four-line Demultiplexer functions as a decoder if _____.

- a) The \bar{E} line is grounded
- b) Data input is on the \bar{E} line
- c) Data input is on the a_0 line
- d) The a_0 line is grounded

Answer: option A

7. In HDL, the operation of the demux is exactly described using a _____.

- a) Function
- b) Process
- c) Variable type
- d) Number of conditional signal assignment statements

Answer: option D

8. When an application, such as an encoder, calls for a unique response from a circuit corresponding to a combination of its input variables, the two methods that best serve this purpose are the _____ and the _____.

- a) Case construct, truth table
- b) If then statement, elif statement
- c) Variable, process
- d) Function, type

Answer: option A

9.A(n) _____ is a logic circuit that accepts a set of inputs that represents a binary number, and activates only the output that corresponds to that input number.

- a) Decoder
- b) Led
- c) Encoder
- d) Demultiplexer

Answer: option A

10.A 1-of-8 octal decoder has eight outputs and decodes an input of _____ bit(s).

- a) Three
- b) Two
- c) Four
- d) One

Answer: option A

11.An everyday illustration of a multiplexer is _____.

The volume control in a stereo receiver
The function switch on a stereo receiver
The balance control on a stereo receiver
The treble-bass control on a stereo receiver

Answer: option B

12.The binary value of the BCD number 1000 0001 (81) is

- _____.
- a) 0101 0001
 - b) 0110 0011
 - c) 0100 0001
 - d) 1000 0000

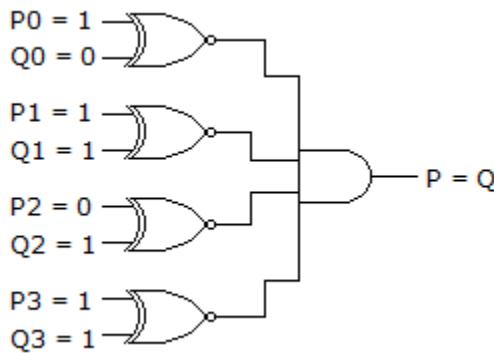
Answer: option A

13.A decimal-to-BCD encoder has _____ data inputs.

- a) Two
- b) Four
- c) Five
- d) Ten

Answer: option D

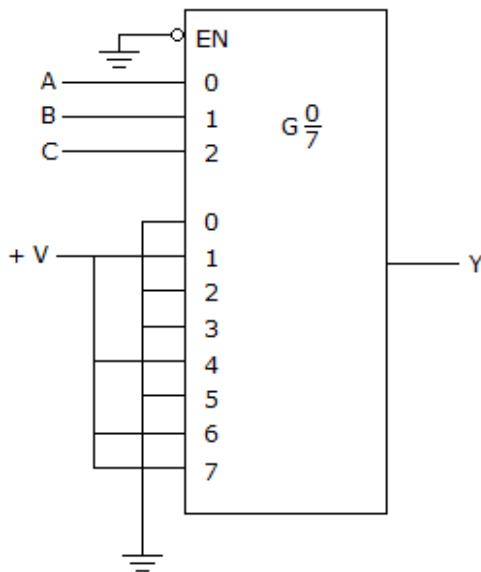
14. For the inputs shown in the given figure, the output is _____.



- a) 1
- b) 0

Answer: option B

15. The diagram given below shows a _____ being used as a(n) _____ and $y = \text{_____}$.



- a) Multiplier, divider, 2.25
- b) Multiplexer, encoder, 7641
- c) Multiplexer, logic function generator, $abc + abc + abc + abc$
- d) Logic function generator, multiplexer, 1467

Answer: option C

16. In most modern computers, the transfer of data takes place over a common set of connecting lines called a _____.

- a) Data bus
- b) Bus line
- c) Bus cable

d) Data line

Answer: option A

17. An octal-to-binary encoder has eight data inputs and encodes an output of _____ bits.

- a) Two
- b) Three
- c) Four
- d) Five

Answer: option B

18. A typical VHDL comparator follows an algorithm described as _____.

- a) Function constructs
- b) Case constructs
- c) If/else constructs
- d) Process constructs

Answer: option C

19. Another name for a multiplexer is _____.

- a) Encoder
- b) Decoder
- c) Code converter
- d) Data selector

Answer: option D

20. When data input i_6 of a 74148 octal-to-binary encoder is active, the data output is _____.

$$A_0 = 0$$

$$A_1 = 0$$

a) $A_2 = 1$
 $A_0 = 0$

$$A_1 = 1$$

b) $A_2 = 1$
 $A_0 = 1$

$$A_1 = 0$$

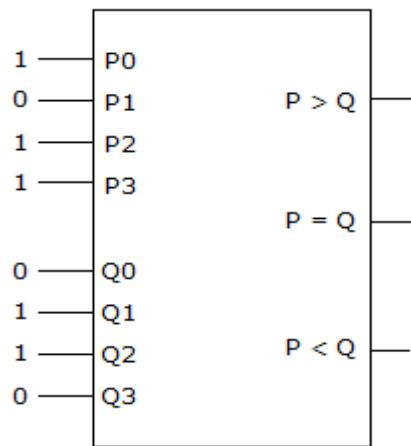
c) $A_2 = 0$
 $A_0 = 0$

$$A_1 = 1$$

d) $A_2 = 0$

Answer: option C

21.For the inputs shown in the given figure, the outputs for $p > q$, $p = q$, and $p < q$ are _____, _____, and _____, respectively.



- a) 1,1,1
- b) 1,0,1
- c) 1,0,0
- d) 0,1,0

Answer: option C

22.A 75154 1-of-16 decoder has 16 outputs and decodes an input of _____ bits.

- a) Two
- b) Three
- c) Four
- d) Six

Answer: option C

23.In an aHDL BCD to binary coded converter, multiplication by 10 is performed by _____.

- a) A multiplication operator
- b) Shifting bits
- c) A library function
- d) A variable type

Answer: option A

24.A(n) _____ display controls the reflection of available light.

- a) Mos
- b) Lcd
- c) led
- d) lsc

Answer: option B

25.The device that places its input data onto one of several outputs is a _____.

- a) Demultiplexer
- b) Multiplexer
- c) Comparator
- d) Counter

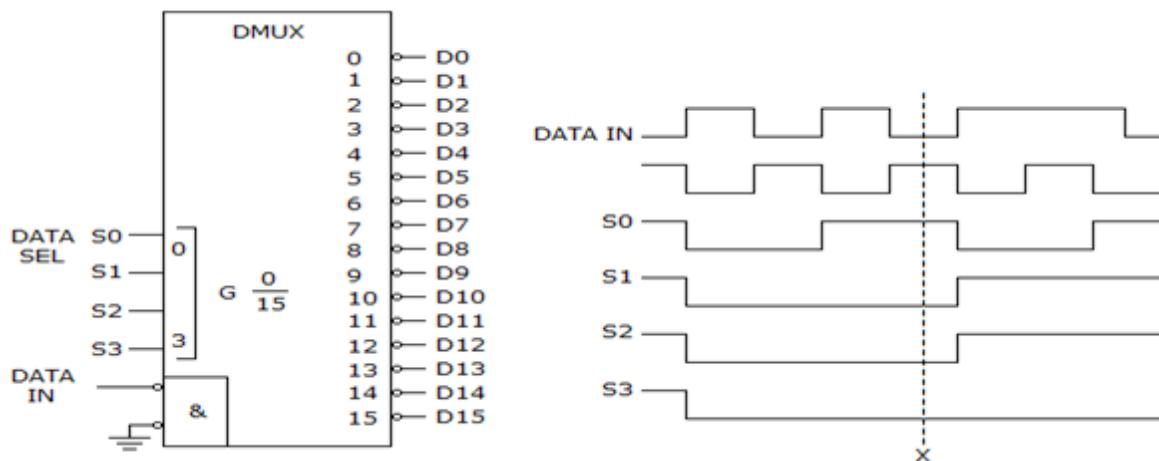
Answer: option A

26.A(n) _____ has a number of input lines, only one of which is activated at a given time, and produces an n-bit output code, depending on which input is activated.

- a) Encoder
- b) Code converter
- c) Demultiplexer
- d) Decoder

Answer: option A

27.The device shown in below is a _____ and for the waveforms shown in the accompanying diagram, the _____ output at point x will be _____ and all others will be _____.



- a) Multiplexer, d4, high, low
- b) Demultiplexer, d3, low, high
- c) Demultiplexer, d3, high, low
- d) Decoder, d12, low, low

Answer: option B

28.The normal outputs of a magnitude comparator are _____.

- a) $A < b$, $a = b$, and $a > b$
- b) Sum, difference, and carry
- c) C_{in} , C_{out} , and sum
- d) $A = b$, $a + b$, and carry

Answer: option A

29.An eight-line multiplexer must have as inputs _____.

- a) Four data inputs and three select inputs
- b) Eight data inputs and two select inputs
- c) Eight data inputs and three select inputs
- d) Eight data inputs and four select inputs

Answer: option C

30.In order to select data input i5 of a 74151 eight-line multiplexer, the select inputs must be _____.

$$\bar{E} = 0$$

$$\bar{S}_0 = 1$$

$$\bar{S}_1 = 0$$

a) $\bar{S}_2 = 1$
 $\bar{E} = 0$

$$\bar{S}_0 = 1$$

$$\bar{S}_1 = 1$$

b) $\bar{S}_2 = 0$
 $\bar{E} = 0$

$$\bar{S}_0 = 0$$

$$\bar{S}_1 = 0$$

c) $\bar{S}_2 = 1$
 $\bar{E} = 1$

$$\bar{S}_0 = 1$$

$$\bar{S}_1 = 1$$

d) $\bar{S}_2 = 0$

Answer: option A

22.DIGITAL SYSTEM PROJECTS USING HDL

1. In a frequency counter, what happens at high frequencies when the sampling interval is too long?

- a. The counter works fine.
- b. The counter undercounts the frequency.
- c. The measurement is less precise.
- d. The counter overflows.

Answer: Option D

Explanation:-

Consider an example. Let the sampling time be 1 sec. This means the counter will count number of pulses from the unknown signal for 1sec duration and would display it after 1 sec. thus if the signal is of 800 Hz, at the end of 1 sec, counter would have counted up to 800.

Thus in case of high frequencies and high sampling time, counter might count beyond its limit and overflows

2. In the digital clock project, when does the PM indicator go high?

- a. Never
- b. Going from 11:59:59 to 12:00:00
- c. Going from 12:59:59 to 01:00:00
- d. On the falling edge of the clock after enable goes high

Answer: Option B

Explanation:-

Because of it is PM after immediate of 11:59:59 it will enter to AM state so that this is the correct one.

3. How is the output frequency related to the sampling interval of a frequency counter?

- a. Directly with the sampling interval
- b. Inversely with the sampling interval
- c. More precision with longer sampling interval
- d. Less precision with longer sampling interval

Answer: Option C

4. In an HDL application of a stepper motor, after an up/down counter is built what is done next?

- a. Build the sequencer

- b. Test it on a simulator**
- c. Test the decoder**
- d. Design an intermediate integer variable**

Answer: Option B

5. In a digital clock application, the basic frequency must be divided down to:

- a. 1 Hz.**
- b. 60 Hz.**
- c. 100 Hz.**
- d. 1000 Hz.**

Answer: Option A

Explanation:-

Because of Minimum count is 1 sec.

And time = 1/freq.

So 1 Hz is answer.

6. In the keypad application, what does the data signal define?

- a. The row and column encoded data**
- b. The ring encoded data**
- c. The freeze locator data**
- d. The ring counter data**

Answer: Option A

7. What does the ring counter in the HDL keypad application do when a key is pressed?

- a. Count to find the row**
- b. Freeze**
- c. Count to find the column**
- d. Start the D flip-flop**

Answer: Option B

8. In the digital clock project, the purpose of the frequency prescaler is to:

- a. find the basic frequency.**
- b. transform a 60 pps input to a 1 pps timing signal.**
- c. prevent the clock from exceeding 12:59:59.**
- d. allow the BCD display to have a value from 00–59.**

Answer: Option B

9. Which is not a step that should be followed in project management?

- a. Overall definition**

- b. System documentation**
- c. Synthesis and testing**
- d. System integration**

Answer: Option B

10. In the keypad application, what does the preset state of the ring counter define?

- a. The proper output of the column encoder**
- b. The NANDing of the rows**
- c. The NANDing of the columns**
- d. The proper output of the row encoder**

Answer: Option D

11. In an HDL stepper motor design, why is there more than one mode?

- a. To change the speed of the stepper motor**
- b. To change the direction of the stepper motor**
- c. To direct drive the stepper motor**
- d. All of the above**

Answer: Option D

12. Which is not a major block of an HDL frequency counter?

- a. Display register**
- b. Decoder/display**
- c. Timing and control unit**
- d. Bit shifter**

Answer: Option D

13. In a full-step sequence involving two flip-flops driving four coils of a stepper motor, how far will the stepper motor step?

- a. 90°**
- b. 45°**
- c. 30°**
- d. 15°**

Answer: Option D

14. Which is not a step used to define the scope of an HDL project?

- a. Are the inputs and outputs active HIGH or active LOW?**
- b. A clear vision of how to make each block work**
- c. What are the speed requirements?**
- d. How many bits of data are needed?**

Answer: Option B

15. In the digital clock project, what is the frequency of the MOD-6 counter in the minutes section?

- a. 1 pulse per minute
- b. 6 pulses per minute
- c. 10 pulses per minute
- d. 1 pulse per hour

Answer: Option A

16. Why should a real hardware functional test be performed on the HDL stepper motor design?

- a. To check the speed of the software
- b. To check the current levels in the motor
- c. To check the voltage levels of the real outputs
- d. To provide a fully operational system

Answer: Option A

17. What does the major block of an HDL code emulation of a keypad include?

- a. A sequencer
- b. A clock
- c. A multiplexer
- d. A ring counter

Answer: Option D

18. The accuracy of the frequency counter depends on the:

- a. system clock frequency.
- b. number of displayed digits.
- c. sampling rate.
- d. display update rate.

Answer: Option A

19. In the frequency counter, if the clock generator produces a 100 kHz system clock signal, how many decade counters are required to measure 1 Hz?

- a. 6
- b. 5
- c. 4
- d. 3

Answer: Option B

20. What must a stepper motor HDL application include?

- a. Variables and processes
- b. Types and bits
- c. Counters and decoders

d. Sequencers and multiplexers

Answer: Option C

21. Which is not a step in strategic planning for HDL development?

- a. There must be a way to test each piece.
- b. Each block must fit together to make up the whole system.
- c. The names of each input and output must be known.
- d. The exact operation of each block must be thoroughly defined and understood.

Answer: Option C

22. In the frequency counter, when is the new count stored in the display register?

- a. After disabling the counter
- b. When the count buffer is full
- c. After the sample interval is set
- d. When the timing and control block has put it there

Answer: Option A

23. What are two ways to remember the current state of a counter in VHDL?

- a. With FUNCTIONS and PROCESS
- b. With counters and timers
- c. With SIGNAL and VARIABLE
- d. With bit types

Answer: Option C

24. In the digital clock project, what type of counter is used to count to 59 seconds?

- a. MOD-60
- b. MOD-6
- c. BCD
- d. BCD followed by a MOD-6

Answer: Option D

25. In the keypad application, when all columns are HIGH, the ring counter is enabled and counting, and *dav* is LOW, what is the status of the *d* outputs?

- a. On
- b. Off
- c. Hi-Z
- d. 1011

Answer: Option C

26. In the frequency counter, what is the function of the Schmitt trigger circuit?

- a. To reduce input noise
- b. To condition the input signal
- c. To convert non-square waveforms
- d. To provide a usable signal to the display unit

Answer: Option C

27. List three basic blocks in the digital clock project.

- a. MOD-60, MOD-12 counters
- b. MOD-5, MOD-10, MOD-12 counters
- c. MOD-60, MOD-10 counters
- d. MOD-6, MOD-12, and MOD-10 counters

Answer: Option D

28. When designing an HDL digital system, which is the worst mistake one can make?

- a. Concluding that a fundamental block works perfectly
- b. Failing to provide proper documentation
- c. Adding blocks of code prior to testing them
- d. Overlooking a possible VARIABLE

Answer: Option A

29. In the keypad application, just after the 4 ms mark the simulation imitates the release of the key by changing the column value back to F hex, which causes the d output to go into its Hi-Z state. On the next rising clock edge, what happens to dav?

- a. It goes HIGH.
- b. It goes LOW.
- c. It goes to Hi-Z.
- d. It goes to 1111H.

Answer: Option B

30. For the frequency counter, which is not a control signal from the control and timing block?

- a. Clear
- b. Enable
- c. Reset
- d. Store

Answer: Option C

TRUE/FALSE

1. Top-down design means that we start at the highest level of the hierarchy, or that the entire project is considered to exist in a closed dark box with inputs and outputs.

- a. True
- b. False

Answer: Option A

2. The frequency counter measures frequency by enabling a counter to count the number of pulses of the incoming waveform during a precisely specified period of time called the sampling time.

- a. True
- b. False

Answer: Option B

3. In the digital clock project, frequency prescaling is used to take a 1 pps input and transform it into a 60 pps timing signal.

- a. True
- b. False

Answer: Option B

4. The half-step sequence of a stepper motor is created by inserting a start with only one coil energized between full steps.

- a. True
- b. False

Answer: Option A

5. One of the first steps in any HDL project is to define its scope by knowing the nature of all the signals that are interconnected to pieces of the project.

- a. True
- b. False

Answer: Option B

6. In HDL, one of the strategies used in strategic planning is to find a way to test each piece of the project.

- a. True
- b. False

Answer: Option A

7. A very critical dimension in project management is the time your boss will give you to complete the HDL project.

- a. True
- b. False

Answer: Option A

8. In the keypad HDL encoder, the data signal is used to combine the row and column encoder data to make a 4-bit value representing the key that was pressed.

- a. True
- b. False

Answer: Option A

9. One CASE construct inside another CASE construct is called a do-loop.

- a. True
- b. False

Answer: Option B

10. A frequency counter is a circuit that can measure and display the frequency of a signal.

- a. True
- b. False

Answer: Option A

11. In the digital clock project, a MOD-60 BCD counter is made from a MOD-10 counter cascaded to a MOD-6 BCD counter.

- a. True
- b. False

Answer: Option A

12. The full-step sequence always has two coils of the stepper motor energized in any state of the sequence and typically causes 30° of shaft rotation per step.

- a. True
- b. False

Answer: Option B

13. The direct drive mode of a stepper motor allows for less control by the operator.

- a. True
- b. False

Answer: Option B

14. In the frequency counter, a pulse shaper block is needed to ensure that the unknown signal, whose frequency is to be measured, will be compatible with the clock input for the counter block.

- a. True
- b. False

Answer: Option A

15. In the digital clock project, the AHDL block codes are connected using graphic design files.

- a. True
- b. False

Answer: Option A

16. In HDL, one of the strategies used in strategic planning is to find the speed requirements.

- a. True
- b. False

Answer: Option B

17. In the keypad HDL encoder, the *ts* bit array represents a tristate buffer.

- a. True
- b. False

Answer: Option A

18. In the VHDL code of the stepper motor, the *cout* outputs are *bit_vector* type because they are binary bit patterns.

- a. True
- b. False

Answer: Option A

19. In the keypad HDL encoder, as long as all columns are high the ring counter is enabled and counting.

- a. True
- b. False

Answer: Option A

20. In the frequency counter, the pulse width of the enable signal is very critical for taking an accurate frequency measurement.

- a. True
- b. False

Answer: Option A

21. One of the first steps in any HDL project is to define its scope by naming each input and output.

- a. True
- b. False

Answer: Option A

22. The wave-drive sequence of a stepper motor has more torque and operates more smoothly than the full-step sequence at moderate speeds.

- a. True
- b. False

Answer: Option B

23. In the digital clock project, the ENT input and RCO output can be used for synchronous counter cascading.

- a. True
- b. False

Answer: Option A

24. In the digital clock project, the 60 Hz signal is sent through a Schmitt-trigger circuit to produce sine wave pulses at the rate of 60 pps.

- a. True
- b. False

Answer: Option B

25. In the digital clock project HDL, the 1 pps signal is used as a synchronous clock for all of the counters' stages, which are synchronously cascaded.

- a. True
- b. False

Answer: Option A

26. In the digital clock project, when it is 11:59:59, AND Gate 1 detects that the tens of hours is 1 and the edge trigger clock moves the display to 12:00:00.

- a. True
- b. False

Answer: Option B

27. In the keypad HDL encoder, after releasing a key the ring counter resumes its counting sequence.

- a. True
- b. False

Answer: Option A

28. In the keypad HDL encoder, the freeze bit detects when a key is released.

- a. True
- b. False

Answer: Option B

29. In HDL when a circuit is simulated on a computer, the designer must create all the different scenarios that will be experienced by the actual circuit and must also know the proper response to those inputs.

- a. True
- b. False

Answer: Option A

30. In the keypad HDL encoder, NANDing of the columns is used to activate the freeze bit.

- a. True
- b. False

Answer: Option B

FILL IN THE BLANKS

1. In the digital clock project, the 1 pps signal is used as a synchronous clock for all of the counter stages, which are _____.

- a. advanced BCD counters
- b. MOD-6 counters
- c. synchronous cascaded
- d. 1 pulse per second

Answer: Option C

2. In the keypad encoder, the _____ must hold in its current state until a key is released.

- a. ring counter
- b. MOD-6 counter
- c. BCD counter
- d. freeze bit

Answer: Option A

3. The interface of the stepper motor needs to operate in one of _____ mode(s).

- a. One
- b. Two
- c. Three
- d. Four

Answer: Option D

4. In the digital clock project, the 60 Hz signal is sent through a Schmitt-trigger circuit to produce square pulses at the rate of _____.

- a. 1 pps
- b. 60 pps
- c. 100 pps
- d. 600 pps

Answer: Option B

5. A frequency counter _____ a signal.

- a. Measures
- b. Displays
- c. measures and displays
- d. measures, displays, and generates

Answer: Option C

6. When coming up with a strategy for dividing the overall project into manageable-size pieces one must _____.

- a. name each input and output
- b. fully understand how the device should operate
- c. define successful completion of the project
- d. know the nature of all the signals that interconnect all the pieces

Answer: Option D

7. VARIABLES are considered to be updated _____ within a sequence of statements in a PROCESS, whereas SIGNALS referred to in a PROCESS are updated when the PROCESS _____.

- a. once, starts
- b. immediately, suspends
- c. twice, ends
- d. never, starts

Answer: Option B

8. The major blocks of the frequency counter are the counter, _____, decoder/display, and the timing and control unit.

- a. signal prescaler
- b. control inputs
- c. signal generator
- d. display register

Answer: Option D

9. In the keypad encoder, just after the 4 ms mark, the simulation initiates the release of the key by changing the column value to _____, which causes the d output to go into its Hi-Z state.

- a. 0 hex
- b. 4 hex

- c. 8 hex
- d. F hex

Answer: Option D

10. One aspect of project planning and management is the selection of _____ that will best fit the application.

- a. hardware platform
- b. software
- c. personnel
- d. time

Answer: Option A

11. In the keypad encoder, the ring counter is implemented using _____ that responds to the c/k input.

- a. SIGNAL
- b. FUNCTION
- c. CASE
- d. PROCESS

Answer: Option D

12. In the digital clock project, when it is 11:59:59, AND Gate 1 detects that the tens of hours is 1 and the enable input is active. On the next clock pulse the AM/PM flip-flop will _____.

- a. Set
- b. Reset
- c. Toggle
- d. Clear

Answer: Option C

13. In the frequency counter, the control clock is derived from the _____ by frequency dividers controlled in the control and timing block.

- a. BCD counters
- b. system clock signal
- c. display register
- d. decoder/display

Answer: Option B

14. Using one case construct inside another is known as _____.

- a. Doping
- b. Functioning
- c. Freezing
- d. Nesting

Answer: Option D

15. In the frequency counter, the length of time for the _____ to be enabled can be selected with the range select input.

- a. display register
- b. frequency prescaler
- c. BCD counter
- d. signal generator

Answer: Option C

16. In the digital clock project HDL code, the MOD-12 counter is using _____.

- a. a BCD counter followed by a MOD-2 counter
- b. a single HDL module
- c. a MOD-6 counter followed by a MOD-2 counter
- d. a MOD-12 counter followed by a D flip-flop

Answer: Option B

17. Each _____, starting at the simplest level, should be built in HDL.

- a. subsystem
- b. block
- c. circuit
- d. function

Answer: Option A

18. In the keypad encoder, the _____ activate(s) the freeze bit only when one column is low.

- a. NAND columns
- b. CASE structure
- c. freeze function
- d. BCD counter

Answer: Option B

19. In a real project, the first step of definition often involves some _____ on the part of the project manager.

- a. Time
- b. Skill
- c. Research
- d. Management

Answer: Option C

Explanation:-

I think it must be time. Because due to lack of time one cannot close a project.

20. One of the first steps in small-project management is to determine _____.

- a. how many devices are controlled by the outputs
- b. a way to test each block
- c. if each block fits together
- d. how each block works

Answer: Option A

21. The timing and control block provides the _____ for the frequency counter.

- a. brains
- b. BCD counters
- c. display register
- d. six different frequency measurement ranges

Answer: Option A

22. The stepper motor HDL will ignore its counter inputs and pass control inputs directly to the output when set in mode _____.

- a. 1
- b. 2
- c. 3
- d. 4

Answer: Option A

23. The full-step sequence of a stepper motor always has two coils energized in any state of the sequence and typically causes _____ of shaft rotation per step.

- a. 5°
- b. 10°
- c. 15°
- d. 20°

Answer: Option C

24. Depending on the _____ the IC is in, the output of the stepper motor HDL will respond to each pulse by changing state.

- a. Mode
- b. Make
- c. Input
- d. Output

Answer: Option A

25. The step rate of the simulation of a stepper motor is probably _____ the actual stepper motor.

- a. slower than
- b. more than
- c. almost the same as
- d. exactly the same as

Answer: Option A

26. A very critical dimension in project management is _____.

- a. Cost
- b. Skill
- c. Time
- d. Personnel

Answer: Option C

27. In the digital clock design, the hours section is different from the seconds and minutes section in that it never goes to _____.

- a. the 0 state
- b. 13
- c. the ring counter
- d. the BCD counter

Answer: Option A

28. In the digital clock project, a 60 pps input is transformed into a 1 pps timing signal. The block is called _____.

- a. a BCD counter
- b. a MOD-60 counter
- c. frequency divider
- d. frequency prescaling

Answer: Option D

29. In the stepper motor, the half-step sequence is used when _____.

- a. less torque is needed
- b. larger steps are desired
- c. smaller steps are desirable
- d. more torque is needed

Answer: Option C

30. In the keypad encoder, the _____ detects when a key is pressed.

- a. ring counter
- b. MOD-6 counter
- c. BCD counter
- d. freeze bit

Answer: Option D

23.DIGITAL DESIGN

1. The _____ circuit overcomes the problem of switching caused by jitter on the inputs.

- a) astable multivibrator**
- b) bistable multivibrator**
- c) Schmitt trigger**

Answer: Option D

Explanation:-

Schmitt trigger reshapes a pulse suppose a jitter is cause and is less than the threshold value of the trigger it maintains its current state but bistable multi vibrators are also use these are usually called switch debouncing circuit so both D and C are correct.

2. Why would a delay gate be needed for a digital circuit?

- a. A delay gate is never needed.**
- b. to provide for setup times**
- c. to provide for hold times**
- d. to provide for setup times and hold times**

Answer: Option D

Explanation:-

In a digital circuit, sequential elements are constrained by timing parameters like set up and hold time, it is necessary to meet them, if not they will lead to violations and metastable states, so in order to avoid those conditions we use delay gates to meet the requirement in setup and hold time.

3. An optocoupler is an integrated circuit with an LED and a zener diode encased in the same package.

- a. True**
- b. False**

Answer: Option B

Explanation:-

LED & photo diode are encased in same package.

or

An optocoupler not having Zener diode. It has photo transistor and LED inside the same package.

or

It should be photo diode or photo transistor instead of the zener diode.

4. A Schmitt trigger has $V_{T+} = 2.0 \text{ V}$ and $V_{T-} = 1.2 \text{ V}$. What is the hysteresis voltage of the Schmitt trigger?

- a. 0.4 volt
- b. 0.6 volt
- c. 0.8 volt
- d. 1.2 volts

Answer: Option C

Explanation

$$(V_{t+}) - (V_{t-}) = 2.0 - 1.2 = 0.8 \text{ volts}$$

5. Which of the following circuit parameters would be most likely to limit the maximum operating frequency of a flip-flop?

- a. setup and hold time
- b. clock pulse HIGH and LOW time
- c. propagation delay time
- d. clock transition time

Answer: Option C

6. A 0.01- μF capacitor is recommended by TTL manufacturers for _____ the power supply.

- a. decoupling
- b. filtering
- c. rectifying
- d. grounding

Answer: Option A

7. Why does the data sheet for the 7476 only give a minimum value for the clock pulse width (both HIGH and LOW)?

- a. nominal value
- b. best-case condition
- c. worst-case condition

Answer: Option C

8. Why is the Schmitt trigger needed in the 60-Hz TTL-level clock pulse generator?

- a. to provide a triangle wave
- b. to provide a sine wave
- c. to provide a rounded pulse waveform
- d. to provide a sharp pulse waveform

Answer: Option D

9. The main concern when using a pull-down resistor is:

- a. the low power dissipation of the resistor
- b. it will keep a floating terminal LOW
- c. the high power dissipation of the resistor
- d. it will cause false triggering

Answer: Option C

10. Look up the propagation delay from the clock to the output for the 7476. Are the HIGH-to-LOW and LOW-to-HIGH propagation delays the same?

- a. Yes
- b. no, $t_{PLH} = 25 \text{ ns}$, $t_{PHL} = 40 \text{ ns}$
- c. no, $t_{PLH} = 40 \text{ ns}$, $t_{PHL} = 25 \text{ ns}$
- d. no, $t_{PHL} = 25 \text{ ns}$, $t_{PLH} = 40 \text{ ns}$

Answer: Option B

11. What would be the output voltage of a 7814 voltage regulator?

- a. -14 V dc
- b. +14 V dc
- c. -8 V dc
- d. +8 V dc

Answer: Option B

Explanation:-

7814 means:

78 - positive(+).

14 - Voltage.

If 7914 means:

79 - negative(-).

14 - voltage.

12. The purpose of a pull-up resistor is to keep a terminal at a _____ level when it would normally be at a _____ level.

- a. LOW, float
- b. HIGH, float
- c. clock, float
- d. pulsed, float

Answer: Option B

Explanation:-

In digital IC, a high is 5v while low is 0v. If we have 3.4v at the output of an IC, it is said to be a float for it is neither High nor Low. To keep such an output voltage to a High condition, we need a pull-up resistor (a resistor connected from +5v to the output of the IC).

If we want to keep the floating output to a constant Low condition, then we connect a pull-down resistor (a resistor connected from 0v to the output of the IC).

13. Setup time specifies:

- a. the minimum time the control levels need to be maintained on the inputs prior to the triggering edge of the clock in order to be reliably clocked into the flip-flop
- b. the maximum time interval required for the control levels to remain on the inputs before the triggered edge of the clock in order for the data to be reliably clocked out of the flip-flop
- c. how long the operator has to get the flip-flop running before the maximum power level is exceeded
- d. how long it takes the output to change states after the clock has transitioned

Answer: Option A

14. Can the automatic RC circuit be used to set a flip-flop rather than reset the flip-flop?

- a. Yes
- b. No

Answer: Option A

15. Can the automatic RC circuit be used to set a flip-flop rather than reset the flip-flop?

- a. Yes
- b. No

Answer: Option A

16. A Schmitt trigger:

- a. has two trip points
- b. is a zero crossing detector
- c. has positive feedback
- d. has two trip points and positive feedback

Answer: Option D

16. A settable flip-flop's normal starting state when power is first applied to a circuit is always the _____ state.

- a. Reset
- b. Set
- c. Toggle
- d. Dual

Answer: Option B

17. In the automatic reset circuit for a flip-flop, how long does it take the capacitor to completely charge?

- a. 1 time constant (RC)
- b. 2 time constants (RC)
- c. 5 time constants (RC)

d. 10 time constants (RC)

Answer: Option C

18. The output of a standard TTL NAND Gate is used to pull an LED indicator LOW. The LED is in series with a 470- Ω resistor. What is the current in the circuit when the LED is on?

- a. 7.02 mA**
- b. 8.51 mA**
- c. 10.63 mA**
- d. 5.32 mA**

Answer: Option A

19. When the inputs to a flip-flop are changing at the same time that the active trigger edge of the input clock is making its transition, this condition is called:

- a. racing**
- b. toggling**
- c. slave loading**
- d. pulse timing**

Answer: Option A

20. Is the propagation delay from the clock to the output for the 7476 the same as the delay from the set or reset to the output?

- a. Yes**
- b. No**

Answer: Option A

21. What is the difference between setup time and hold time?

- a. Setup time occurs after the active clock edge, hold time occurs before the active clock edge.**
- b. Setup time occurs before the active clock edge, hold time occurs after the active clock edge.**
- c. Setup time and hold time both occur at the active clock edge.**

Answer: Option B

22. Define a race condition for a flip-flop.

- a. The inputs to a trigger device are changing slightly before the active trigger edge.**
- b. The inputs to a trigger device are changing slightly after the active trigger edge.**
- c. The inputs to a trigger device are changing at the same time as the active trigger edge.**

Answer: Option C

23. Which of the following flip-flop timing parameters indicates the time it takes a Q output to respond to a C_p input?

- a. t_s , th
- b. $tPHL$, $tPLH$
- c. $tw(L)$, $tw(H)$
- d. f_{max}

Answer: Option B

24. How much setup time (t_s) is required for the 74LS76?

- a. 5 ns
- b. 10 ns
- c. 20 ns
- d. 40 ns

Answer: Option C

25. Why should a LED be pulled LOW from a logic gate rather than pulled HIGH?

- a. LOW-level current is smaller.
- b. LOW-level current is larger.
- c. HIGH-level current is larger.
- d. LOW-level current is smaller and HIGH-level current is larger.

Answer: Option B

26. What is the major advantage of the J-K flip-flop over the S-R flip-flop?

- a. The J-K flip-flop is much faster.
- b. The J-K flip-flop does not have propagation delay problems.
- c. The J-K flip-flop has a toggle state.
- d. The J-K flip-flop has two outputs.

Answer: Option C

27. Decoupling capacitors should be tied from V_{CC} on one device to ground on a different device.

- a. True
- b. False

Answer: Option B

28. One example for the use of a Schmitt trigger is as a(n):

- a. switch debouncer
- b. racer
- c. astable oscillator
- d. transition pulse generator

Answer: Option A

TRUE/FALSE

1. TTL requires a constant supply voltage of 8.0 V.

- a. True
- b. False

Answer: Option B

2. A transfer function graph illustrates the most important specifications for the Schmitt trigger devices.

- a. True
- b. False

Answer: Option A

3. The input levels to a flip-flop must be maintained for a minimum time period both before and after the edge of the clock signal is applied.

- a. True
- b. False

Answer: Option A

4. There is no way to eliminate the effects of a switch bounce.

- a. True
- b. False

Answer: Option B

5. Pull-up resistors and pull-down resistors are used to keep a floating terminal HIGH.

- a. True
- b. False

Answer: Option B

6. The output of a phototransistor is determined by the presence or absence of light at its base input.

- a. True
- b. False

Answer: Option A

7. The term *race condition* describes the time that an active signal must be present at the input to a flip-flop before an active clock edge is applied.

- a. True
- b. False

Answer: Option B

8.A Schmitt trigger has a positive feedback circuit and experiences a phenomenon called *hysteresis*.

- a. True
- b. False

Answer: Option B

9.A series RC circuit can be used to generate a power-up (automatic) reset signal.

- a. True
- b. False

Answer: Option B

10.The 7805 will get very hot if your circuit draws more than 0.5 A.

- a. True
- b. False

Answer: Option B

24.DIGITAL SIGNAL PROCESSING

1. In a flash analog-to-digital converter, the output of each comparator is connected to an input of a _____.

- a. Decoder
- b. Priority encoder
- c. Multiplexer
- d. Demultiplexer

Answer: option B

Explanation:-

An n bit flash ADC has 2^n comparators. When an unknown input v_{in} is applied to its input, all comparators whose reference voltage is less than v_{in} will give output 1 while others will give output 0. The highest reference valued comparator is nearest to v_{in} . Thus a priority encoder will convert it to binary.

2. Which term applies to the maintaining of a given signal level until the next sampling?

- a. Holding
- b. Aliasing
- c. Shannon frequency sampling
- d. "stair-stepping"

Answer: option A

Explanation:-

Holding is the operation to hold the signal level of the previous sample until and unless next sample arrives.

An ideal sampler consists of two circuits i. E,

1. Sampler circuit &
2. Hold circuit.

So from that conclusion i came to the answer as holding. That's it.

3. An op-amp has very _____.

- a. High voltage gain
- b. High input impedance
- c. Low output impedance
- d. All of the above

Answer: option D

Explanation:-

The op-amp characteristics are:

high voltage gain, high input impedance, low output impedance, infinite bandwidth and input offset voltage is low.

4. For a 4-bit DAC, the least significant bit (LSB) is _____.

- a. 6.25% of full scale
- b. 0.625% of full scale
- c. 12% of full scale
- d. 1.2% of full scale

Answer: option A

Explanation:-

N=4-bit

$$\text{LSB} = (1/2^n) * 100$$

$$= (1/2^4) * 100$$

$$= (1/16) * 100$$

$$= 0.0625 * 100$$

$$= 6.25$$

5. The dual-slope analog-to-digital converter finds extensive use in _____.

- a. Digital voltmeters
- b. Function generators
- c. Frequency counters
- d. All of the above

Answer: option D

Explanation:-

The correct answer should be a - digital voltmeter. This application can allow long conversion time. Dual slope method gives good accuracy at low cost but long conversion time. Function generator and frequency counters do not need ADC

Or

The analog to digital converters converts an analog signal into a digital value. In these converters resolution is the important. To get accurate digital value for respective analog signal resolution should be high, dual slope ADC has high resolution because it's used in digital voltmeters, function generators, frequency counters and etc.

6. The ADC0804 is an example of a _____.

- a. Single-slope analog-to-digital converter
- b. Dual-slope analog-to-digital converter
- c. Digital-ramp analog-to-digital converter

d. Successive-approximation analog-to-digital converter

Answer: option D

Explanation:-

From ADC0801 to ADC0805 are CMOS 8 bit ADC.

7. In a digital representation of voltages using an 8-bit binary code, how many values can be defined?

- a. 16
- b. 64
- c. 128
- d. 256

Answer: option D

Explanation:-

Since the base of the binary number system is 2 and it is said that in digital representation of voltages we need to show in 8-bit binary code

so, 2 to the power 8 will be the answer.....

I.e, $2^8 = 256$

(or $2 \times 2 = 256$)

Or

That seems to be quite the thing.

That is, if there are 8 bits in the signal and there are 2 possible representations of voltage levels in a binary number system. Then every bit has the possibility of being represented by any of those 2 numbers.

Hence, $2 \times 2 = 2^8 = 256$.

That was some Explanation:-.

8. A 4-bit r/2r ladder digital-to-analog converter uses _____.

- a. One resistor value
- b. Two resistor values
- c. Three resistor values
- d. Four resistor values

Answer: option B

Explanation:-

It doesn't matter how many bit ADC.

The r-2r ladder ADC requires only 2 resistors values.

9. A binary-weighted-input digital-to-analog converter has a feedback resistor, r_f , of 12 k Ω . If 50 μ A of current is through the resistor, voltage out of the circuit is _____.

- a) 0.6 V

- b) -0.6 V
- c) 0.1 V
- d) -0.1 V

Answer: option B

Explanation:-

$$V = i * r_f$$

$$v = (50 * 10^{-6})(12 * 10^3)$$

$$v = 0.6 \text{ volt}$$

how the negative sign came? If any one know the answer please reply me?

Or

If you use positive reference voltage, which is assumed here, then output is negative because opamp is acting as inverting amplifier. For positive output, you need to use negative reference voltage.

Or

Negative sign due to the negative ref voltage of opamp.

Or

Because of negative feedback used for amplifier. So that we get the answer in negative.

10. The resolution of a 6-bit DAC is _____.

- a. 63%
- b. 64%
- c. 15.9%
- d. 1.59%

Answer: option D

Explanation:-

Resolution of DAC(n bits) in % is given by

$$(1 / ((2^n) - 1)) * 100$$

for 6 bits,

$$(1 / ((2^6) - 1)) * 100 = 1.58\%$$

Or

$$\% \text{ resolution} = (\text{step size} / \text{full scale}) * 100$$

now n bit DAC has total 2^n values possible with total $2^n - 1$ steps to reach full scale value from smallest value, with each step of 1 unit. Therefore
resolution = $(1 / 2^n - 1) * 100$

11. Which type of ADC quantizes the analog signal into a stream of bits whose amount corresponds to the signal level?

- a. Successive approximation
- b. Sigma-delta
- c. Dual-slope

- d. None of the above

Answer: option B

Explanation:-

Sigma is symbol for the summation, and delta you know it ;).

12. A binary-weighted-input digital-to-analog converter has an input resistor of 100 k Ω . If the resistor is connected to a 5 v source, current through the resistor is _____.

- a. 50 ma
- b. 50 μ a
- c. 5 ma
- d. 500 μ a

Answer: option B

Explanation:-

$$V = i * r.$$

$$I = v/r.$$

$$I = 5/(100*10^3).$$

$$I = 0.00005.$$

$$I = 50*10^{-6}.$$

$$I = 50 \text{ microa.}$$

13. In troubleshooting a DAC, we check its performance characteristics, such as _____.

- a. Nonmonotonicity
- b. Differential nonlinearity
- c. Low and high gain
- d. All of the above

Answer: option D

14. In a digital reproduction of an analog curve, accuracy can be increased by _____.

- a. Sampling the curve more often
- b. Sampling the curve less often
- c. Decreasing the number of bits used to represent each sampled value
- d. All of the above

Answer: option A

Explanation:-

To get more accuracy the sampling frequency of the ADC have to be increased

Or

For accuracy, sampling as well as more bits to digitize are necessary.

15. In a 4-bit r/2r ladder digital-to-analog converter, because of negative feedback, the operational amplifier keeps the inverting (minus) input near _____.

- a. 5 volts
- b. Zero volts
- c. A voltage determined by the binary weighted input
- d. None of the above

Answer: option B

Explanation:-

Positive input of opamp is grounded. So opamp gives negative feed back in such a way that its negative input is also ground and the differential signal is zero.

16. What is the result of taking more samples during the quantization process?

- a. More errors in the analog-to-digital conversion
- b. More bit requirements
- c. More accurate signal representation
- d. More bit requirements and more accurate signal representation

Answer: option D

Explanation:-

The correct answer is more accurate signal representation.

17. Which a/d conversion method has a fixed conversion time?

- a. Single-slope analog-to-digital converter
- b. Dual-slope analog-to-digital converter
- c. Digital-ramp analog-to-digital converter
- d. Successive-approximation analog-to-digital converter

Answer: option D

Explanation:-

Successive approximation method requires n clock cycles for n bit conversion. Slope based methods require variable number of clock cycles depending on the input voltage.

18. Which is a typical application of digital signal processing?

- a. Noise elimination
- b. Music signal processing
- c. Image processing
- d. All of the above

Answer: option D

19. If a DAC has a full-scale, or maximum, output of 12 v and accuracy of $\pm 0.1\%$, then the maximum error for any output voltage is _____.

- a. 12 v
- b. 120 mv
- c. 12 mv
- d. 0 v

Answer: option C

Explanation:-

$$12v * 0.1 = 1.2 / 100 = 12mv$$

20. What do we call the manipulation of an analog signal in a digital domain?

- a. Analog-to-digital conversion
- b. Digital-to-analog conversion
- c. Digital signal processing
- d. Signal filtering

Answer: option B

Explanation:-

The question is asked in somewhat reverse manner.

At first sight when we read and come into mind that he is asking manipulation of data from analog to digital

But all this is the game of words.

It is said in last word the domain i. E, digital domain means in actual we are practicing in digital domain and in that domain we are manipulating the analog data.

So from digital to analog is digital to analog conversion.

That's it.

21. How are unwanted frequencies removed prior to digital conversion?

- a. Pre-filters
- b. Digital signal processing
- c. Sample-and-hold circuits
- d. All of the above

Answer: option A

22. Which type of programming is typically used for digital signal processors?

- a. Assembly language

- b. Machine language**
- c. C**
- d. None of the above**

Answer: option A

Explanation:-

This answer would have been correct 20 years ago. All dsp processors nowadays use c and c++.

23. Which of the following best defines nyquist frequency?

- a. The frequency of resonance for the filtering circuit**
- b. The second harmonic**
- c. The lower frequency limit of sampling**
- d. The highest frequency component of a given analog signal**

Answer: option D

Explanation:-

Nyquist frequency is twice the maximum frequency in the signal.

24. Which is not an a/d conversion error?

- a. Differential nonlinearity**
- b. Missing code**
- c. Incorrect code**
- d. Offset**

Answer: option A

25. SeTTing time is normally defined as the time it takes a DAC to seTTLe within _____.

- a) $\pm 1/8$ LSB of its final value when a change occurs in the input code**
- b) $\pm 1/4$ LSB of its final value when a change occurs in the input code**
- c) $\pm 1/2$ LSB of its final value when a change occurs in the input code**
- d) 1 LSB of its final value when a change occurs in the input code**

Answer: option C

TRUE/FALSE

1. Digital signal processors must be programmed to perform specific tasks.

- a. True**
- b. False**

Answer: option A

2. The flash method of analog-to-digital conversion uses comparators that compare reference voltages with the analog input voltage.

- a. True
- b. False

Answer: option A

3. Offset is the characteristic of a DAC defined by the absence of any incorrect step reversals.

- a. True
- b. False

Answer: option B

Explanation:-

Offset errors cause the DAC to produce an output voltage other than 0 v for a digital input of 0. The offset error can be measured and removed by adding or subtracting an equivalent digital number to the DAC input.

4. Digital filtering is faster than analog filtering.

- a. True
- b. False

Answer: option B

5. Successive-approximation is perhaps the most widely used method of a/d conversion.

- a. True
- b. False

Answer: option A

Explanation:-

A successive approximation a/d conversion is the most common and popular direct a/d conversion method used in data acquisition systems because it allows high sampling rates and high resolution, while still being reasonable in terms of cost.

6. Digital signal processing must be at least half as fast as the incoming signal to be processed.

- a. True
- b. False

Answer: option B

7. The flash converter is the fastest analog-to-digital conversion method.

- a. True

b. False

Answer: option A

8. The ADC0804 is an example of a successive-approximation ADC.

a. True

b. False

Answer: option A

9. Incorrect codes are a form of output error for a DAC.

a. True

b. False

Answer: option B

10. In a binary-weighted-input digital-to-analog converter, the values of the input resistors are chosen to be proportional to the binary weights of the corresponding input bits.

a. True

b. False

Answer: option A

FILL IN THE BLANKS

1. An offset error in a DAC will show up as an incorrect analog output _____.

a. Only for higher value inputs

b. Only for lower value inputs

c. Only for certain (scattered) inputs

d. For all inputs

Answer: option D

2. An ADC that compares each bit, one at a time, with the input analog signal is a _____.

a. Single-slope ramp converter

b. Dual-slope ramp converter

c. Successive-approximation converter

d. Tracking converter

Answer: option C

3. A standard logic device can be connected on a bus system as an open-collector logic device by connecting each output to a _____.

a. Discrete transistor

b. 10 k Ω series resistor

c. Light-emitting diode

d. CMOS buffer

Answer: option A

4. A monotonicity error in a DAC will show up as an incorrect analog output _____.

- a. Only for higher value inputs
- b. Only for lower value inputs
- c. Only for certain (scattered) inputs
- d. For all inputs

Answer: option C

5. Of the methods listed, the fastest a/d conversion is done by a _____.

- a. Single-slope ramp converter
- b. Dual-slope ramp converter
- c. Successive-approximation converter
- d. Tracking converter

Answer: option C

25. MULTIVIBRATORS AND 555 TIMER

1. When a capacitor charges:

- a. The voltage across the plates rises exponentially
- b. The circuit current falls exponentially
- c. The capacitor charges to the source voltage in $5 \times rc$ seconds
- d. All of the above

Answer: option D

Explanation:-

In $5rc$ it is nearly equal to supply voltage.

To get same voltage it requires infinite time.

Or

Time constant is rc seconds in which it reaches 63% of max. Voltage(supply voltage)

3. The _____ is defined as the time the output is active divided by the total period of the output signal.

- a. On time
- b. Off time
- c. Duty cycle
- d. Active ratio

Answer: option C

Explanation:-

The ratio of working time to total time for an intermittently operating device is called duty cycle.

Or

$$D = t/p * 100\%$$

Where d is the duty cycle, t is the time the signal is active, and p is the total period of the signal.

It is used to describe the percent time of an active signal in an electrical device.

4. A 22-k Ω resistor and a 0.02- μ F capacitor are connected in series to a 5-v source. How long will it take the capacitor to charge to 3.4 v?

- a. 0.44 ms
- b. 0.501 ms
- c. 0.66 ms

d. 0.70 ms

Answer: option B

Explanation:-

$$V = v_o [\{ \exp(-t/rc) \} - 1]$$

where

v = voltage across capacitor at any time t

v_o = supply voltage

Or

$$V(c) = v(s)[1-e((-t)/rc)].$$

$$3.4 = 5[1-e((-t)/rc)].$$

$$3.4/5 = [1-e((-t)/rc)].$$

$$0.68 = 1-e((-t)/rc).$$

$$e((-t)/rc) = 0.32.$$

Taking natural log both sides, we have

$$-t/rc = -1.139.$$

$$T = 1.139 * 0.02u * 22k.$$

$$T = 0.501ms.$$

Or

$$T = rc * \ln(v_c/v_s).$$

5. What does the discharge transistor do in the 555 timer circuit?

- a. Charge the external capacitor to stop the timing**
- b. Charge the external capacitor to start the timing over again**
- c. Discharge the external capacitor to stop the timing**
- d. Discharge the external capacitor to start the timing over again**

Answer: option D

6. Pulse stretching, time-delay, and pulse generation are all easily accomplished with which type of multivibrator circuit?

- a. Astable**
- b. Monostable**
- c. Multistable**
- d. Bistable**

Answer: option B

Explanation:-

We can realize pulse stretching and pulse generation by using all the options. But time delay circuit required a trigger pulse. This is available only in the mono stable multi-vibrator.

7. The internal circuitry of the 555 timer consists of _____, an r-s flip-flop, a transistor switch, an output buffer amplifier, and a voltage divider.

- a. A comparator
- b. A voltage amplifier
- c. Two comparators
- d. A peak detector

Answer: option C

8. With most monostable multivibrators, what is the q output when no input trigger has occurred?

- a. Low
- b. +5 v
- c. Set
- d. High

Answer: option A

9. An astable multivibrator requires:

- a. Balanced time constants
- b. A pair of matched transistors
- c. No input signal
- d. Dual j-k flip-flops

Answer: option C\

Explanation:-

Used as an oscillator as it doesn't need any external pulse.
May also be used as a square wave generator.

11. What is the difference between an astable multivibrator and a monostable multivibrator?

- a. The astable is free running.
- b. The astable needs to be clocked.
- c. The monostable is free running.
- d. None of the above

Answer: option A

Explanation:-

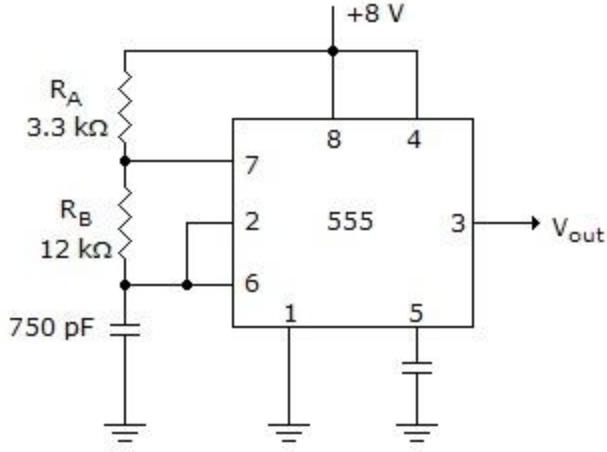
External triggering is given to mono stable.

12. Is there any limit to the number of times that a 74123 can be retriggered?

- a. Yes
- b. No

Answer: option B

13. Determine t_{hi} and t_{lo} for the circuit given below.



- a. $T_{hi} = 7.95 \mu s$, $t_{lo} = 6.24 \mu s$
- b. $T_{hi} = 6.24 \mu s$, $t_{lo} = 7.95 \mu s$
- c. $T_{hi} = 3.97 \mu s$, $t_{lo} = 3.21 \mu s$
- d. $T_{hi} = 3.21 \mu s$, $t_{lo} = 3.97 \mu s$

Answer: option A

Explanation:-

$$\text{High time} = \ln(2) * C * (R_A + R_B)$$

$$\text{low time} = \ln(2) * C * R_B$$

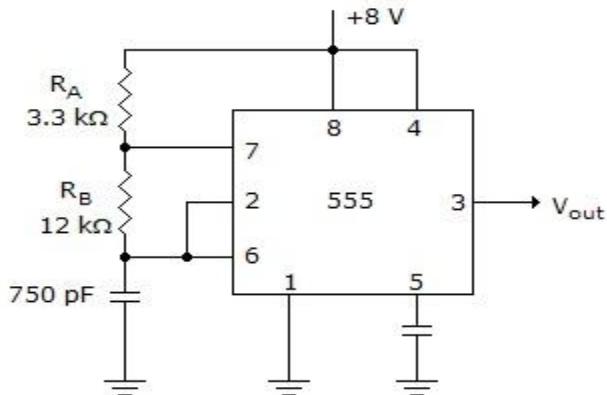
all values given.. Just subs

14. The output of the astable circuit _____.

- a. Constantly switches between two states
- b. Is low until a trigger is received
- c. Is high until a trigger is received
- d. Floats until triggered

Answer: option A

15. If a diode is connected across resistor r_b (positive end up) in the given figure, what is the new duty cycle of the output waveform?



- a. 56%

- b. 44%
- c. 21.6%
- d. 17.4%

Answer: option C

Explanation:-

$$T_m = 0.7 * r_1 * c, \quad t_s = 0.7 * r_2 * c$$

$$\text{duty cycle} = r_1 / (r_1 + r_2) \text{ or } t_m / (t_m + t_s)$$

Or

Ees ths is correct. If we want 50% duty cycle this is perfect ckt..only one 10k pot'll be connected betwn ra & rb., because for 50% duty cycle ra must be equal zero.

If we directly connected pin 7 to vcc ckt may be damaged. (down transistor damaged/)

Or

If you want less then 50% duty cycle then rb is bypassed by a diode. This left out 56% out of box. The duty cycle can now be calculated (in this configuration) as:

$$d.c = [r_a / (r_a + r_b)] * 100.$$

Or

When we connect a diode, the main purpose is to get the duty cycle < 0.5 . Before connecting the diode the $d = (r_a + r_b) / (r_a + 2r_b)$. By the time we connect diode, the d becomes $r_a / (r_a + r_b)$.

16. Design a circuit using a 74121 to convert a 33-khz, 30% duty cycle waveform to a 33-khz, 60% duty cycle waveform.

- a. $R_{int} = 2 \text{ k}\Omega, C_{ext} = 0.012 \text{ nf}$
- b. $R_{int} = 2 \text{ k}\Omega, C_{ext} = 0.012 \mu\text{f}$
- c. $R_{int} = 4 \text{ k}\Omega, C_{ext} = 0.012 \text{ nf}$
- d. $R_{int} = 4 \text{ k}\Omega, C_{ext} = 0.012 \mu\text{f}$

Answer: option B

17. What controls the output pulse width of a one shot?

- a. The clock frequency
- b. The width of the clock pulse
- c. An r/l time constant
- d. An rc time constant

Answer: option D

18. Does the 74123 one shot have an internal timing resistor?

- a. Yes
- b. No

Answer: option B

19. In a typical ic monostable multivibrator circuit, at the falling edge of the trigger input, the output switches high for a period of time determined by the _____.

- a. Value of the *rc* timing components
- b. Amplitude of the input trigger
- c. Frequency of the input trigger
- d. Magnitude of the dc supply voltage

Answer: option A

20. A monostable 555 timer has the following number of stable states:

- a. 0
- b. 1
- c. 2
- d. 3

Answer: option B

21. What is the difference between a retriggerable one shot and a nonretriggerable one shot?

- a. The nonretriggerable can only be triggered once.
- b. The retriggerable can be triggered many times
- c. The output pulse can be stretched with a nonretriggerable.
- d. The output pulse can be stretched with a retriggerable.

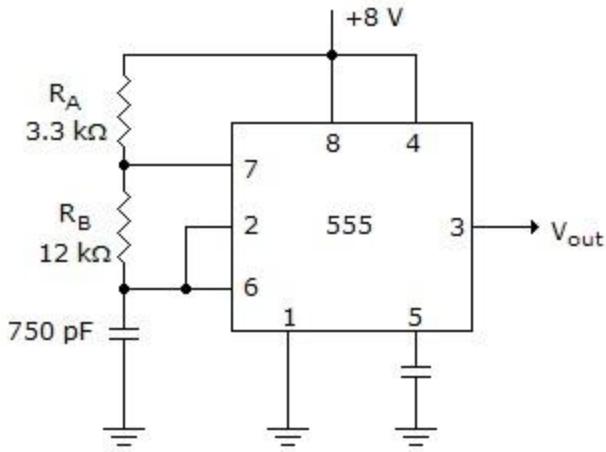
Answer: option D

22. Triggering a retriggerable one shot during pulse generation will:

- a. Time out the original pulse
- b. Extend the pulse to this trigger width
- c. Have no effect
- d. Double the original pulse width

Answer: option B

23. What is the duty cycle of the waveform at the output of the circuit given below?



- a. 78%
- b. 56%
- c. 50%
- d. 44%

Answer: option B

Explanation:-

$$\text{Duty cycle} = \frac{r_A + r_B}{r_A + 2 \cdot r_B}$$

$$= \frac{(3.3 + 12) \cdot 10^6}{(3.3 + 2 \cdot 12) \cdot 10^6}$$

$$= \frac{(3.3 + 12)}{(3.3 + 2 \cdot 12)}$$

$$= \frac{15.3}{27.3} = .56 = 56\%$$

24. The monostable multivibrator circuit is not an oscillator because _____.

- a. Its output switches between two states
- b. It requires a trigger to obtain an output signal
- c. It requires a sine wave input signal
- d. The circuit does not require ADC power supply

Answer: option B

25. A retriggerable one shot has a pulse of 10 ms. 3 ms after being triggered, another trigger pulse is applied. The resulting output pulse will be _____ ms.

- a. 3
- b. 7
- c. 10
- d. 13

Answer: option D

26. What is the pulse width of the output of a 74123 if an external 4.7-k Ω resistor and a 0.022- μF capacitor are used?

- a. 290 ms

- b. 29 ms
- c. 33.3 μ s
- d. 290 μ s

Answer: option C

Explanation:-

$T_1 = 0.693 * r$. Formula gives the pulse width.

Or

$$T_w = k * r * C_{ext}$$

When $C_{ext} > 1 \mu F$, the output pulse duration is defined as:

$$T_w = 0.33 * r * C_{ext}$$

Or

$$T_w = k * r * C_{ext} (1 + 0.7 / r_x)$$

27. To obtain a 50% duty cycle in an astable 555 timer circuit:

- a. $T_{lo} = t_{hi}$
- b. $R_a = R_b$ and short R_b with a diode during the capacitor charging cycle
- c. Capacitor voltage must rise above $1/3 V_{cc}$
- d. $T_{lo} = t_{hi}$, $R_a = R_b$, and short R_b with a diode during the capacitor charging cycle

Answer: option A

28. What is another name for a bistable multivibrator?

- a. An on-off switch
- b. An oscillator
- c. A flip-flop

Answer: option C

29. An astable 555 timer has the following number of stable states:

- a. 0
- b. 1
- c. 2
- d. 3

Answer: option A

30. Which mode of operation is being used when a 555 timer chip has two external resistors and an external capacitor?

- a. Monostable
- b. Pulse stretching
- c. Schmitt triggering
- d. Astable

Answer: option D

31. A 0.3- μ F capacitor has an initial charge of 2.7 v. If it is discharged through a 10-k Ω resistor for 6.5 ms, how much voltage will be left across the capacitor?

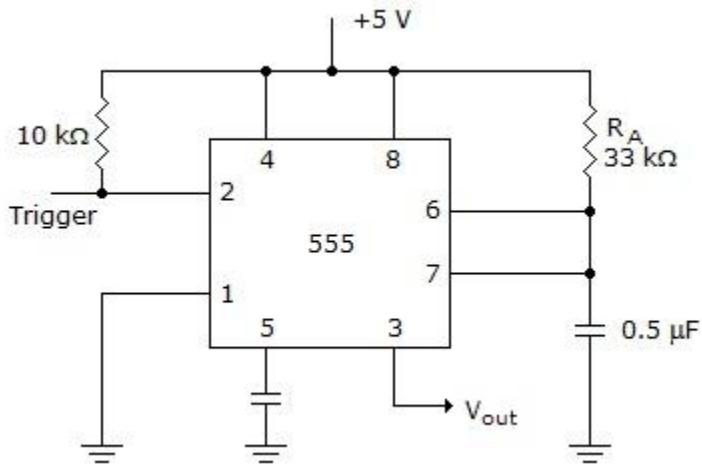
- a. V
- b. 0.309 v
- c. 2.7 v
- d. 2.295 v

Answer: option B

Explanation:-

The voltage formula is given as $v_c = v(1 - e^{-t/RC})$
which equals: $v_c = 2.7(1 - e^{-0.0065/0.003})$ [rc = .003 seconds from above]
therefore, $v_c = 2.39$ volts
voltage will be left across the capacitor is $2.7v - 2.39v = 0.31v$

32. Is the circuit given below an astable multivibrator or a monostable multivibrator?



- a. Monostable
- b. Astable

Answer: option A

Explanation:-

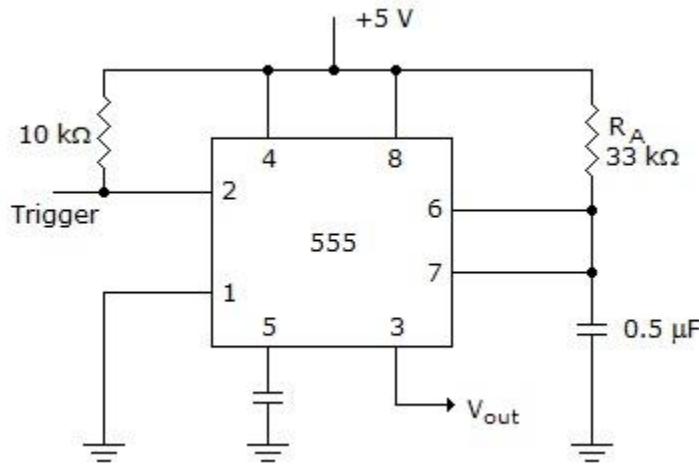
Circuit contains two external resistors and two external capacitors. Hence it is monostable

33. Which of the following is not a characteristic of a retriggerable monostable multivibrator?

- a. It is a dual multivibrator.
- b. It has an active-high reset, which terminates all timing functions.
- c. It has no internal timing resistor.
- d. None of the above

Answer: option B

34. What is the output pulse width of the waveform at the output of the circuit in the given figure?



- a. 1.65 ms
- b. 18.2 ms
- c. 4.98 ms
- d. 54.6 ms

Answer: option B

Explanation:-

Monostable multivibrator output = $1.1 \times r \times C$

35. The pulse width out of a one-shot multivibrator increases when the:

- a. Supply voltage increases
- b. Timing resistor decreases
- c. Utp decreases
- d. Timing capacitance increases

Answer: option A

Explanation:-

Is this the right answer? What if the timing capacitance increased? The equation is $t = 1.1 \text{ rc}$.

That means pulse width is proportional to the resistance and capacitance only.

Hence if the value of capacitor increased, pulse width increases and supply voltage has no relation with it.

Or

I thought so it was the capacitor. But there is also an equation related with time. $V_c = V_m(1 - e^{-t/\tau})$ i guess its because of this equation?

36. If V_{cc} of a 555 timer circuit is set to +10 v what is the level of output voltage from the circuit?

- a. $V_{oh} = 10$ v, $V_{ol} = 0$ v
- b. $V_{oh} = 10$ v, $V_{ol} = 0.1$ v
- c. $V_{oh} = 8.5$ v, $V_{ol} = 0$ v
- d. $V_{oh} = 8.5$ v, $V_{ol} = 0.1$ v

Answer: option D

37. If the resistor in the schmitt trigger astable multivibrator is a variable resistor, what part of the output voltage waveform will change when the resistance is changed?

- a. The shape of the waveform
- b. The amplitude of the waveform
- c. The period of the waveform
- d. None of the above

Answer: option C

TRUE/FALSE

1. When extremely critical timing is required, a quartz crystal can be used.

- a. True
- b. False

Answer: option A

2. In the 74121, which is nonretriggerable, any triggers that come in before the end of the timing cycle are ignored.

- a. True
- b. False

Answer: option A

3. A comparator simply outputs a high or low based on a comparison of the voltage levels at its input.

- a. True
- b. False

Answer: option A

4. The 74s124 TTL chip is a voltage-controlled oscillator that will generate a specific frequency at V_{out} .

- a. True
- b. False

Answer: option B

5. A single schmitt trigger inverter is all that is needed to build a simple astable multivibrator.

- a. True
- b. False

Answer: option B

6. The bistable multivibrator is an r-c flip-flop.

- a. True
- b. False

Answer: option B

7. When the 74123, a retriggerable monostable multivibrator device, ends its timing cycle it must be started all over again.

- a. True
- b. False

Answer: option B

8. Timing accuracy of more than eight significant digits can be easily achieved by using quartz crystals.

- a. True
- b. False

Answer: option B

9. A multivibrator is a circuit that changes between two digital levels on a continuous, free-running basis or on demand.

- a. True
- b. False

Answer: option A

10. A monostable multivibrator is commonly called a two shot.

- a. True
- b. False

Answer: option B

26. MICROPROCESSOR FUNDAMENTALS

1. The devices that provide the means for a computer to communicate with the user or other computers are referred to as:

- a. Cpu
- b. Alu
- c. I/o
- d. None of the above

Answer: option C

Explanation:-

Input/output devices as the name only indicate is used for communication purpose in microprocessors.

Or

Because through i/o devices we can provide user input. So these are acting like an interface between the user and computer.

Or

Obviously it is i/o because without providing input we can not communicate & without o/p can not analysis result.

Or

Its only input/output devices are there which can communicate with users, it can neither be alu nor cpu.

2. The software used to drive microprocessor-based systems is called:

- a. Assembly language
- b. Firmware
- c. Machine language code
- d. Basic interpreter instructions

Answer: option A

Explanation:-

Assembly language program is helpful software for user to access mp, mp understands machine language to help user we use assembly language, which is very compact than higher level language like embedded c language.

Or

Actually machine language is in the form of 0s and 1s so it doesn't understand by the user. That's why we will use assembly language is it in the form of codes.

Or

Technically, the software is called firmware. Machine language code can be considered arguably as an explicit answer. Assembly language is not a software.

Or

But assembly language is coding language but firmware refers to software.v

Or

Its just a mnemonic. Instead of using binary digits we are using this hexadecimal code to make us easier to deal with the instructions.

3. The circuits in the 8085a that provide the arithmetic and logic functions are called the:

- a. Cpu
- b. Alu
- c. I/o
- d. None of the above

Answer: option B

Explanation:-

Alu means arithmetic and logical unit, by using this unit arithmetic (i.e add, sub, div, mul) , logical (i.e and, or, nor) operation are perform in microprocessor.

Or

Alu is the right answer.

Because all the arithmetic and logical operation like add, sub, increment by 1, decrements by 1 and the logical operation like logical and, logical or, logical ex-or, logical ex-nor, complement, rotate right and rotate left can be performed by the alu operation.

4. How many buses are connected as part of the 8085a microprocessor?

- a. 2
- b. 3
- c. 5
- d. 8

Answer: option B

Explanation:-

For the 8085 microprocessor there are 3 buses..

They are

- 1.adress bus
- 2.data bus
- 3.control bus

Before knowing about the buses that are available in 8085 it is better to know the literal meaning of bus.

The bus is nothing but a group of wires used to process(or)communicate between different parts of the processor as well as computer.

In 8085 we have three buses that are 1) address bus 2) data bus 3) control bus.

The point we need to know here is out of these three buses which is unidirectional and which is comes under bidirectional buses.

Out of these three buses the address bus is bidirectional and remaining two buses are unidirectional.

I hope this information is useful to you.

Or

Address bus is unidirectional as address is generated by microprocessor and it is provided to i/o devices as well as memory when a read and write operation is done.

Data bus is bidirectional as data signal can flow from microprocessor to i/o devices, memory and vice versa.

Or

The address bus is unidirectional because it is the CPU that tells the external hardware what address to use, not the other way around.

To communicate with memory the microprocessor sends an.

Address on the address bus, eg 0000000000000011 (3 in decimal), to the memory. The memory selects box number 3 for reading or writing data.

Address bus is unidirectional, ie numbers only sent from microprocessor to memory, not other way.

Or

Address bus is unidirectional, and its obvious because, only MPU needs to know the address of data or peripheral device, so it is unidirectional.

Data bus is bidirectional, because data must be send or receive by the MPU and peripheral device, so its bidirectional.

Or

It is called microprocessor because processor is designed with micro-technology. Because of quantum tunneling to make size more small micro technology is not possible. Nano processors are in invention stage. You can invent it.

Microprocessor has 3 buses :

1. Address bus.
2. Control bus.
3. Data bus.

Address bus is unidirectional, data bus is bidirectional and control bus can be either unidirectional or bidirectional depends upon the processor.

5. The _____ ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus.

- a. Control bus

- b. Control instructions**
- c. Address decoder**
- d. Cpu**

Answer: option C

Explanation:-

Decoder is a type of logic device that uses different control signal along with buses to give a suitable logic that enable or disable i/o, memory whatever required.

Or

Why means it has 2 IC but at the address location based on the decoder of the output can be appears.

Ex:

let us take,

IC1

IC2

IC1 adds location -2001 to 2090.

IC2 adds location-4000 to 8500.

The selection of address is 3500 so it goes to the address location of IC2 so IC2 indicates the output.

Or

Control bus just used to pass the control to the processor or to the devices connected (i.e.) In read operation control is given to devices to write on the address, whereas on the write operation the processor is given control to write on the memory. Thus is the work of control bus, but whereas address decoder only correctly decodes the address and identifies which is needed to be operated and sends the signal to the control bus.

6. How many bits are used in the data bus?

- a. 7**
- b. 8**
- c. 9**
- d. 16**

Answer: option B

Explanation:-

Ad0-ad15 & a8-a15

therefore databus using 8 bits only

Or

In 8085 microprocessor data bus is 8 bit. That is why 8085 is called 8 bit microprocessor.

Or

In 8085 up the address & data bus are multiplexed with each other ad0-ad7, using demultiplexing i.e. latch we get data bits d0-d7

Or

In 8085 data bus is of 8 bit and.

In 8086 data bus is of 16 bit.

Or

Ad0-ad7 i.e. Lower bank.

Ad8-ad15 i.e. Higher bank.

So, each bank contain 8 bit. That's why 8 bit is used in data bus.

8085 - 8 bit.

8086 - 16 bit.

7. The items that you can physically touch in a computer system are called:

- a. Software
- b. Firmware
- c. Hardware
- d. None of the above

Answer: option C

Explanation:-

Computer hardware is any physical device, something that you are able to touch and software is a collection of instructions and code installed into the computer and cannot be touched, whereas firmware is a software program or set of instructions programmed on a hardware device.

8. Single-bit indicators that may be set or cleared to show the results of logical or arithmetic operations are the:

- a. Flags
- b. Registers
- c. Monitors
- d. Decisions

Answer: option A

Explanation:-

Usually flags contains only one bit.

Hence answer is flags.

9. When referring to instruction words, a mnemonic is:

- a. A short abbreviation for the operand address
- b. A short abbreviation for the operation to be performed
- c. A short abbreviation for the data word stored at the operand address
- d. Shorthand for machine language

Answer: option B

Explanation:-

We know that instruction register referred as ir. Only opcode (operation code) goes in ir not operand (data) and ir does not accessible by user. That is why (b) sort abbreviation for operation to be performed answer is right answer.

Or

Mnemonic is a combination of letters to suggest the operation of an instruction.

10. The technique of assigning a memory address to each i/o device in the computer system is called:

- a. Memory-mapped i/o
- b. Ported i/o
- c. Dedicated i/o
- d. Wired i/o

Answer: option A

Explanation:-

In memory mapped i/o the address are shared. It means some address of memory provide to i/o devices. Note that same address doesnot assign to memory or i/o device.

Or

Memory mapping mean the process of interfacing memory with micro processor. And allocating address for each memory location.

Or

There are two ways to assign a address of i/o.

- 1) peripheral i/o.
- 2) memory mapped i/o.

In peripheral i/o, 8 bit address lines are there for assigning.

And in memory mapped i/o, 16 bit address lines are there for assigning.

Or

Memory mapped i/o:

- 16-bit device address.
- data transfer between any general-purpose register and i/o port.
- the memory map (64k) is shared between i/o device and system memory.
- more hardware is required to decode the 16-bit address.
- the arithmetic or logic operation can be directly performed with i/o data .

Peripheral mapped i/o:

- 8-bit device address.
- data is transfer only between accumulator and i.o port.
- the i/o map is independent of the memory map; 256 input device and 256. The output device can be connected.

- less hardware is required to decode the 8-bit address.
- arithmetic or logical operation cannot be directly performed with i/o data.

11. When was the first 8-bit microprocessor introduced?

- a. 1969
- b. 1974
- c. 1979
- d. 1985

Answer: option B

Explanation:-

In 1974 the intel company introduces 1st 8bit mp which is 8080

The intel 8008 was an early byte-oriented microprocessor designed and manufactured by intel and introduced in april 1972.

Or

Intel introduced its first 8-bit microprocessor was on 1972 i.e. Intel 8008 by using p-mos technology.

12. What type of circuit is used at the interface point of an output port?

- a. Decoder
- b. Latch
- c. Tristate buffer
- d. None of the above

Answer: option B

Explanation:-

A feedback loop in a symmetrical digital circuit, such as a flip-flop, used to maintain a given state is known as latch but at interface point of o/p port there should b decoder.is it true ?

Or

Decoder with bus latch operation such data for corresponding address can be differentiated.

Or

As latch stores the result by refreshing itself & is transparent while changing the result (o/p) , latch is used @ o/p section.

Or

A microprocessor needs its output head to blink 0 or 1 and more importantly, previous values should not affect the present output value. Meanwhile, a latch has no feedback; so latch is used.

Please correct me if i'm wrong.

Or

Latches can be memory devices, and can store one bit of data for as long as the device is powered. As the name suggests, latches are used to "latch onto" information and hold it in place. Latches are very similar to flip-flops, but are not synchronous devices, and do not operate on clock edges as flip-flops do.

Or

The reason for using the latch in an output port is simple. You do not want to lose the result of any operation. So, in order to not lose it, we use a latch, so that it holds the information as long as new information is overwritten onto it.

Or

Tristate buffer (>> inverted >> non-inverted >> high impedance) can be used at interfacing.

13. I/o mapped systems identify their input/output devices by giving them a(n) _____.

- a. **8-bit port number**
- b. **16-bit port number**
- c. **8-bit buffer number**
- d. **8-bit instruction**

Answer: option A

Explanation:-

In i/o mapped 8 bit addresses are provided to i/o devices .

Or

In memory mapped i/o the addresses of i/o ports are of 16 bits. And in i/o mapped i/o scheme the address of i/o ports is of 8 bits.

14. What type of circuit is used at the interface point of an input port?

- a. **Decoder**
- b. **Latch**
- c. **Tristate buffer**
- d. **None of the above**

Answer: option C

Explanation:-

A latch will hold a logic level that's been clocked into it. It always outputs either a high or a low logic level and continues to output its last state when it's no longer being clocked.

A tristate buffer will output the value that's currently applied to it. It doesn't latch the input in response to a clock. As long as the buffer's 'enable' signal is present, it will output either a high or low logic level. When its 'enable'

signal goes false, it will appear as a high-impedance at its output. That's the third state referred to in the term 'tristate' (high-low-disconnected).

15. The register in the 8085a that is used to keep track of the memory address of the next op-code to be run in the program is the:

- a. Stack pointer
- b. Program counter
- c. Instruction pointer
- d. Accumulator

Answer: option B

Explanation:-

Program counter is one which tells about the next instruction.

Or

Program counter is 16 bit which stores the address of next instruction.

Or

Program counter is denoted by pc.

It is 16 bit reg.

It hold memory adderssof next instruction to be executed.

Instruction pointer (ip).

Intel's term for the register that points to the next instruction to fetch.

Actually, at intel it is properly the pair cs:ip, code segment and instruction pointer, but since intel's 8086 and 80286 era segments are deprecated the term ip by itself will often be used.

Program counter (pc).

Another popular term for the register that points to the next instruction to fetch.

The meaning of both ip and pc is extended beyond that register to the address, the contents of the register. E.g. We may say "the instruction has ip=...."

up until the late 1990s i would estimate that the term pc was more common than the term ip for essentially the same concept. But with the dominance of intel in the 1990s and 2000s, the term ip may have become more common.

Or

Program counter is used to hold the address of the next instruction to be executed where as a stack pointer is used to hold the address of the top of the stack for a program.

16. The control bus and memories share a bidirectional bus in a typical microprocessor system.

- a. True
- b. False

Answer: option B

Explanation:-

he data bus and memory can share the a bidirectional bus... But this will not allowed... Its false...

Or

Bidirectional bus = data bus.

Memory share data bus to transfer operands, opcodes. Etc.

By control bus only control signals read write. Etc will be transferred.

Or

Among 1)address bus 2)data bus 3)control bus of a microprocessor.

Address bus is unidirectional as address is generated by microprocessor and is passed to i/o devices.

Data bus is bidirectional as data signal can flow from microprocessor to i/o devices, memory and from memory to i/o device.

Control bus is bidirectional as it transfer the control signals from control unit to all the i/o devices and vice versa.

17. All computer programs for a machine are called:

- a. Software
- b. Firmware
- c. Hardware
- d. None of the above

Answer: option A

Explanation:-

Generally a machine is a hardware device and inorder to make it run a s/w is required which is a program

Or

What is firmware?

In electronic systems and computing, firmware is "the combination of a hardware device, eg. An integrated circuit, and computer instructions and data that reside as read only software on that device". As a result, firmware usually cannot be modified during normal operation of the device.

Typical examples of devices containing firmware are embedded systems (such as traffic lights, consumer appliances, and digital watches), computers, computer peripherals, mobile phones, and digital cameras. The firmware contained in these devices provides the control program for the device.

18. The 8085a is a(n):

- a. 16-bit parallel cpu
- b. 8-bit serial cpu
- c. 8-bit parallel cpu
- d. None of the above

Answer: option C

Explanation:-

ADC converts analog to digital....so it is serial to parallel conversion

Or

All the micro processors communicate data in parallel lines.

19. Because microprocessor cpus do not understand mnemonics as they are, they have to be converted to _____.

- a. Hexadecimal machine code
- b. Binary machine code
- c. Assembly language
- d. All of the above

Answer: option B

Explanation:-

Because computer can understand only in binary format, it can not be consider hexadecial

Or

Computer only understand binary i.e. 0, 1.

Or

No actually it is hexadecimal we even write mnemonic like 72, 32, 7f, etc. ,

20. A register in the microprocessor that keeps track of the answer or results of any arithmetic or logic operation is the:

- a. Stack pointer
- b. Program counter
- c. Instruction pointer
- d. Accumulator

Answer: option D

Explanation:-

Accumulator stores the first operand (data) and also stores the result that is produce by alu.

Or

-the stack pointer is a sixteen bit register used to point at the stack.

- in read write memory the locations at which temporary data and return addresses are stored is known as the stack.

- in simple words stack acts like an auto decrement facility in the system.

- the initialization of the stack top is done with the help of an instruction lxi sp.

21. What is the difference between a mnemonic code and machine code?

- a. There is no difference.

- b. Machine codes are in binary, mnemonic codes are in shorthand english.**
- c. Machine codes are in shorthand english, mnemonic codes are in binary.**

Answer: option B

Explanation:-

Mnemonic is just like command i.e, mov a,b

where as

machine code is one which is understand only by the system

Or

Yes machine code is a binary no. 0 or 1. But mnemonic is shorten english. But comp is understand only binary code.

21. Which bus is a bidirectional bus?

- a. Address bus**
- b. Data bus**
- c. Address bus and data bus**
- d. None of the above**

Answer: option B

Explanation:-

22.

Xyz you are wrong. Only data bus is bidirectional because cpu retrieving and writing data on memory or i/o devices. And cpu only generates the address not accept the address.

Or

Data bus is bidirectional and address bus is unidirectional.

22. Which of the following buses is primarily used to carry signals that direct other ics to find out what type of operation is being performed?

- a. Data bus**
- b. Control bus**
- c. Address bus**
- d. Address decoder bus**

Answer: option B

Explanation:-

Control bus is incorrect reference it should be control lines, since each line performs individual operations unlike bus.

24. What kind of computer program is used to convert mnemonic code to machine code?

- a. Debug**

- b. Assembler**
- c. C++**
- d. Fortran**

Answer: option B

Explanation:-

Because assembler converts assembly language (mnemonics codes) into machine language code.

25. Which of the following are the three basic sections of a microprocessor unit?

- a. Operand, register, and arithmetic/logic unit (alu)**
- b. Control and timing, register, and arithmetic/logic unit (alu)**
- c. Control and timing, register, and memory**
- d. Arithmetic/logic unit (alu), memory, and input/output**

Answer: option B

Explanation:-

Cpu (microprocessor) divides in three parts control and timing, register and alu. So these are the basic section of microprocessor.

Or

Micro controllers have more bits than a microprocessors (but include a microprocessor in its bits) and option d mentions some of the extra bits.

TRUE/FALSE

1. The stack is a data storage area in ram used by certain microprocessor operations.

- a. True**
- b. False**

Answer: option A

2. A microprocessor with the necessary support circuits will include at least two memory ics: rom or eprom, and a ram.

- a. True**
- b. False**

Answer: option A

Explanation:-

Because it has rom for system software storage and ram for application software storage.

3. I/o-mapped systems identify their input and output devices by giving them an 8-bit port number.

- a. True**

b. False

Answer: option A

4. A microcontroller integrates multichip systems with ram, rom, and i/o.

a. True

b. False

Answer: option A

5. Programs written for the 8080a must have slight modifications to run on the 8085a.

a. True

b. False

Answer: option B

Explanation:-

8085 is software compatible to 8080.

8085 is upgrade version of 8080

Or

The sim and rim instructions in the 8085 microprocessor are used to set (sim) and read (rim) the interrupt mask. With sim, you can mask or unmask rst5.5, rst6.5, and rst7.5, you can reset the pending rst7.5 flip flop, and you can set or reset the sod (serial output data) pin.

6. The software used to drive a microprocessor-based system is called fortran.

a. True

b. False

Answer: option B

Explanation:-

Fortran is a general-purpose, procedural, imperative programming language that is especially suited to numeric computation and scientific computing.

Or

Assembly language is a software used to drive a microprocessor-based system.

7. Conversion from assembly language to machine language can be done by the programmer through a process called hand assembly.

a. True

b. False

Answer: option A

8. Assembly language is written using mnemonics: mvi, dcr, jz.

a. True

b. False

Answer: option A

Explanation:-

Mvi = move immediately, dcr = decrement jz = jump if zero.

9. The 8085 software is compatible with the 8080a.

a. True

b. False

Answer: option A

Explanation:-

They are software compatible hence instructions will be more or less the same. Basic differences arise in terms of power supply, build, clock rates etc.

10. Lda addr and sta addr are fortran language instructions stored in an external memory ic for a microprocessor.

a. True

b. False

Answer: option B

Explanation:-

Fortran language is previous version of C. It is high level language.

Microprocessor uses assembly language only.

Or

These are the assembly language instruction to load/store from/to memory.

27. THE 8051-MICROCONTROLLER

1. The internal ram memory of the 8051 is:

- a. 32 bytes
- b. 64 bytes
- c. 128 bytes
- d. 256 bytes

Answer: option C

Explanation:-

128 byte fixed ram memory. It is declared by intel and this memory location further devide in four more part.

Or

As i had gone through datashhet alongwith mazidi book on microcontroller it is clearly written that for 8051 family microcontroller ram is of 128bytes & for 8052 ram is 258 bytes.

Or

I have done 6 projects on 8051 and the internal ram of 8051 is pakka 128 bytes and another 128 bytes is reserved for sfrs, but 8052 has 256 their it will parallelly shares the memory and we can access that memory using indirect addressing by using registers r0 and r1.

Or

128 bytes..which is divided as:

- 1) 32 bytes-from 00 to 1f for register banks
- 2) 16 bytes-from locations 20h to 2fh for bit-addressable memory
- 3) 80 bytes-from locations 30h to 7fh for read and write storage called as scratch pad

Or

128 bytes for user ram.

And 128 bytes for sfr's.

Or

Actually ram is 256 bytes but for user it is 28 bytes and for sfr (special function registers) it is 128 bytes.

2. This program code will be executed continuously:

Stat: Mov a, #01h

Jnz stat

- a. True

b. False

Answer: option A

Explanation:-

Since there is no loop available or there is no inc/dcr is available.

Or

represents immediate addressing to a. #01 is an imediate value to a..jnz jump if not zero will satisfy the condition and continuopusly jmps to stat flag.. Its a loop.

Or

#01 signifies value..that means 1 is been stored in accumulator..jnz means jump if not zero. As accumlator has value 1..this process will continue with execution whenevr it checks the condition.

Or

First instruction copies the immediate data 01h to a (no flag is effected) , second instruction compares the content of carry flag with zero if it is not equal to zero then it becomes infinite loop otherwise it executes next instruction.

Or

Jnz instruction checks the contents of accumulator(a) register.

It's value is greater than zero every time... Because it is not decrmenting. So, the loop will infinitely repeats...

Or

Jnz instruction checks the contents of accumulator(a) register.

It's value is greater than zero every time... Because it is not decrmenting. So, the loop will infinitely repeats...

Or

First instruction is a constant value with 01h so, it will never be zero hence it always jumps.

3. The 8051 has _____ 16-bit counter/timers.

- a. 1
- b. 2
- c. 3
- d. 4

Answer: option B

Explanation:-

These are the pc and dptr, each is used to hold the address of a byte in a memory.

Pc: holds the memory address of the next instruction. It gets incremented after every instruction.

Dptr: is made up of two 8 bit registers named dph and dpl. It is used in

operations regarding external ram mostly.

Or

64 pins in 8051 5 stage 4 is bank other one is general purpose.

Or

It has 40 pins. Pc and dptr are the 16 bit registers. It has 2 timers-t1 and t2.

Or

The micro-controller has two 16 bit registers i.e. Program counter and the data pointer.the 8051 has 40 pins,in which 32 i/o pins and 8 are the non mask able pins.

Or

Mc has two 16-bit register (pc and dptr) with 40-pin's and 4 port's p0, p1, p2 and p3 respectively.

Or

8051-mc has 40 pins with 4 digital i/o ports, power supply, gnd, 2 timers (t0, t1 in basic microcontroller) &2 external interrupts.

Or

8051 has 40 pins, it is also called as dip (dual inline package) because the chip contains one side 20 pins another side 20 pins that's it is called as dip, with four ports p0, p1, p2, p3 and it has two 16 bit registers pc & dptr.

Or

The 8051 has two 16 bit timer. This two timers are basically a 16 bit register. Which is incremented based on the clock pulse applied on it. The timers are accessible to programmer through the corresponding sfr registers. The main three function of counters are: 1. Producing a delay for a definite time. 2. Counting the transitions on an external pin. 3. Generating baud rates for the serial port.

Or

The 8051 have 40 pin ic. It has 4 port. It also has 2 timer is available.

Or

Pc - program counter.

Dptr - data pointer.

Or

Once the program dumped into the 8051 and removed from the kit does it retain the program.

Or

The two timers are timer1 and timer0.

4. The address space of the 8051 is divided into four distinct areas: internal data, external data, internal code, and external code.

a. True

b. False

Answer: option A

Explanation:-

Bank addresses 0 , 1 ,2 ,3 ,4

Or

8051 has two types of memories that are rom ,ram

ram stores temporary data

rom stores permanent data i.e)code

8051 has internally 128 bytes ram,4 kbytes rom

we are connecting to externally ram,rom up to 64kbyte of memory

so the answer is option a.

Or

8051 consists of program memory and data memory. That is 256 kbytes out of which 128 bytes are for internal memory and other 128 kbytes are for external memory. These 128 kbytes are divided into 64 kbytes for program memory and other 64 kbytes for data memory.

Program memory can be accessed through program counter and fetch instructions and data memory can be accessed using dptr.

5. Data transfer from i/o to external data memory can only be done with the movx command.

- a. True
- b. False

Answer: option A

Explanation:-

Mov is used when data is to be transferred internally .

Movx is used when there concern with external datas.

Movx instruction is used only if any data is worked upon i/o to a external memory connected to 8051

Or

Movx is for accessing the external memory,
but mov is not deals with external data.

Or

As per the gui (graphical user interference) each controller has its own gui or designer use only that instruction in instruction set.

Or

Movx instruction is used for external data.

Or

Movx instruction is used for accessing the external data only because it is indirect addressing mode.

6. The 8051 can handle _____ interrupt sources.

- a. 3

- b. 4**
- c. 5**
- d. 6**

Answer: option C

Explanation:-

There are five interrupt sources for the 8051, which means that they can recognize 5 different events that can interrupt regular program execution. Each interrupt can be enabled or disabled by setting bits of the ie register. Likewise, the whole interrupt system can be disabled by clearing the ea bit of the same register.

Or

There are 6 interrupts in 8051.

1. Reset.
2. Timer 0.
3. Timer 1.
4. Int 0.
5. Int 1.
6. Serial communication interrupt common to both transfer and receive.
(r1 + t1).

Or

There are 6 interrupts in 8051 and " reset " is one of them.

Or

There are six interrupt sources for the 8051 that are:

- 1) reset.
- 2) external interrupt 0.
- 3) timer0 interrupt.
- 4) external interrupt 1.
- 5) timer1 interrupt.
- 6) uart (tx/rx) interrupts.

Or

External interrupts: int0, int1

internal interrupts: timer0, timer1, uart

7. The special function registers are maintained in the next 128 locations after the general-purpose data storage and stack.

- a. True**
- b. False**

Answer: option A

Explanation:-

Total space in stack memory 0 to 7f.

7f means 127 in decimal.

So 0 to 127 means 128 locations

Or

The uc has a total of 256 bytes of memory in which 128 bytes are allocated for the user defined purpose and the remaining 128 bytes are for the sake of sfr's.

Or

If we consider from 00h to ffh totally we have 272 decimal bit location. But in that the internal ram memory of microprocessor is up to 128 decimal locations. Remaining we consider as special function register memory.

Or

Sfr (special function registers) are acc, b, psw, dptr.

Acc is stored at 0e0h and b at 0f0h.

Sfr are stored at 80h-ffh location.

Or

To avoid the confusion when we access the register or function, it is necessary that memories and registers have unique addresses and at the same time how the stack memory is used to load and store the contents of register/memory is also to be considered.

When we push on 8051 the address pointed by stack pointer reduces by one. And that will not affect the sfrs.

Or

Since internal ram address range from 00h to 7fh so next memory location is 80h. Sfr register have address range from 80h to ffh ie next 128 location.

8. This statement will set the address of the bit to 1 (8051 micro-controller):

setb 01h

a. True

b. False

Answer: option B

Explanation:-

Setb instruction is used to set flag bit not to set address bit.

Or

01h is address of r1 register of bank0 Which is not a bit addressable

Or

Setb works only to set/reset(0 to 1 or 1 to 0) bit addressable and flag registers..it cannot be used for set/reset of address

Or

In order to access the 128 bits of ram location and other bit addressable space of 8051 individually, we can use single bit instruction such as setb.

Or

Now a days many companies write the program for development of

embedded product in c language there are some macros available to write and read the bit.

Write=set_bit (px, bit no) ; /* x=either 0 or 1 or 2or 3*/.

Read=is_bit_set (px, bitno) ;

Or

01h is byte address but setb is bit addressable instruction.

If you want to change the 01h data then you will use byte addressable instruction not use bit addressable instruction.

20h to 2fh have bit address so we will use this address.

Or

Setb bit is used to set the indicated bit high. The bit can be carry or any directly addressable bit of a port, register, or ram location. So it does not set the address of the bit high.

9. Mov a, @ r1 will:

- a. Copy r1 to the accumulator**
- b. Copy the accumulator to r1**
- c. Copy the contents of memory whose address is in r1 to the accumulator**
- d. Copy the accumulator to the contents of memory whose address is in r1**

Answer: option C

Explanation:-

Its an indirect mode of addressing. @ acts as a pointer to the contents of the memory of which address is in r1..and thus being source..it copies that data to accumlator being destination.

Or

Ri=register (r0 to r1)

rn=register (r0 to r7)

= immediat data

@ = indirect ram

Or

This is indirect addressing mode.

Ex: r=register(r1-r3)

@ indictes content of register(indirectly)

its an indirect mode of addressing. @ acts as a pointer
it copies that data to accumlator being destination

Or

It is an indirect addressing mode,

assume,

mov r1,#1000

mov a,@r1

what it explain is in the first instruction value 1000 moves into r1
(immediate address), in the second instruction, the value present in the

1000 (here thousand acts as an address) moves into the a reg.

10. A label is used to name a single line of code.

- a. True
- b. False

Answer: option A

Explanation:-

I think that a label is used when you need any jump or loop condition.

Or

Answer is true because label is used for our reference when the code is executed assembler replaces this with the address, which is unique.

Example code:

```
add a,r1  
jnz skip  
mov r2,a  
skip: mov r2,b
```

as shown in the above sample program assembler replaces this skip label with the address of the instruction mov r2,b which is unique so label is used to name a single line of code.

Or

A label is a special type of symbols used to represent a textual version of an address in rom or ram memory. They are always placed at the beginning of a program line. It is very complicated to call a subroutine or execute some of the jump or branch instructions without them. They are easily used:..

A symbol (label) with some easily recognizable name should be written at the beginning of a program line from which a subroutine starts or where jump should be executed.

It is sufficient to enter the name of label instead of address in the form of 16-bit number in instructions calling a subroutine or jump.

During the process of compiling, the assembler automatically replaces such symbols with appropriate addresses.

Or

Assembler is converts the assembly language into machine code language.

11. The following program will receive data from port 1, determine whether bit 2 is high, and then send the number ffh to port 3:

```
read: mov a,p1  
anl a,#2h  
cjne a,#02h,read  
mov p3,#ffh  
a. True  
b. False
```

Answer: option A

Explanation:-

1st : copied to accumulator

2nd : anding operation

3rd : compare jump if not equal
its always not equal

4th : copied to port3 instruction

Or

Contents of port1 should be mentioned clearly, so that we can perform or take decision on cjne instruction rite !

Or

Line1. A = p1 'read p1 then save in acc.

Line2. A = a and 00000010 'and operation.

Line3. If a <> 00000010 goto line1 'compare.

Line4 else p3 = #0ffh 'send ffh to port 3.

Or

Line 1: we will move the content of p1 to accumulator.

Line2: why to and with 2h please reply, they have asked to find whether second bit is high, so what's the necessary of adding here.

Or

In 0000 00010 the second bit is active high to know whether the second bit is active high adding with 02 that is 0000 0010 will help us to know because an and operation output is active high only if both the inputs are active high.

Or

Only when and operation is performed we will be able to identify if bit no-2 is high or not.

12. Device pins xtal1 and xtal2 for the 8051 are used for connections to an external oscillator or crystal.

- a. True
- b. False

Answer: option A

Explanation:-

Either oscillator or crystal can be connected to this pins but for accurate clock crystal is used.

Or

If some1 wants to drive the connected peripheral device with some different clock speed then he may use these pins in order to have expected speed (clk) for his peripheral device...

Or

If the timer in 8051 is used as counter (c/t = 1) the clock pulse to the timer from the crystal oscillator is cut off.

So we need an external pulse from outside device in order to trigger on the counter, which will be done through the crystal pins.

Or

Microcontroller has internal clock circuit. It must be triggered with help of crystal or oscillator. Thus external crystal is used.

Or

In 8051 crystal oscillator is connected to two capacitors of 33pf, here we can use capacitors which are having values different, what will happen?

13. When the 8051 is reset and the \overline{EA} line is high, the program counter points to the first program instruction in the:

- a. Internal code memory
- b. External code memory
- c. Internal data memory
- d. External data memory

Answer: option A

Explanation:-

Because when external access is high means "0" because showing bar so it can access only internal memory that's why pc points internal code memory.

Or

When $ea=0$ no interrupt will be acknowledged but I'm confused because they are saying ea bar is high.

Or

Because pc always points to code memory.

Or

[a] internal code memory :ram location means pc

[b]. External code memory :rom location ($ea=0, pSEN=connect$)

[c]. Internal data memory :I think rom location

[d]. External data memory :rom location ($ea=0, RD=connect$)

Or

When ea pin is low it uses internal code memory.

But when ea pin is high use for external code memory.

But starting address 0x0000h to 4k use internal then use external memory.

Or

When it goes high the internal rom memory will be executed then answer should be c.

14. An alternate function of port pin p3.4 in the 8051 is:

- a. Timer 0
- b. Timer 1
- c. Interrupt 0
- d. interrupt 1

Answer: option A

Explanation:-

Because the p3.4 pin is reserved for timer 0 register.

Or

P0=rx
p1=tx
p2=int0
p3=int1
p4=timer0
p5=timer1
p6=wr
p7=rd
Or
P3.4 is the timer 0 (t0).

15. Both registers tl0 and tl1 are needed to start timer 0.

- a. True
- b. False

Answer: option B

Explanation:-

Th0 is required only if mode 2

Or

Because whenever we want to run timer the tr register we will run.

Or

To start or stop the timer tr flag is used.

Tl0 and th0 are linked with the timer0, they indicate the timer0 where to start its value

tl0/tl1= we wont to start the program in starting/middle/ending stages used tl0

th0/th1=we wont to stop the program in starting/middle/ending stages used th0

Or

Either (tl0 / th0) or (tl1 / th1) is needed to start the timer. Because (tl0 / th0) corresponding to timer 0 and (tl1 / th1) corresponding to timer 1. We must able to use only one timer at a time.

Or

Tl0 is used for to start the timer 0 and tl1 is used for to start the timer 2 so both need not be set for to start the timer 0.

16. The i/o ports that are used as address and data for external memory are:

- a. Ports 1 and 2
- b. Ports 1 and 3
- c. Ports 0 and 2

d. Ports 0 and 3

Answer: option C

Explanation:-

Because port 0 and 2 have both address and data lines. Where as port 1 and 3 have only data lines.

Or

Port0 used both address and data lines.

Port1 used simple i/o operations

port2 used only address lines

port3 used timers,counters,serial port and etc

Or

Port0 used both address and data lines.

Port1 used simple i/o operations

port2 used only address lines

port3 used timers,counters,serial port and etc

Or

P0 = a0 - a7 for lower bit with data multiplexer.

P2 = only a8 - a15 for higher 8 bit.

17. The last 96 locations in the internal data memory are reserved for general-purpose data storage and stack.

a. True

b. False

Answer: option B

Explanation:-

Because if we start from 00h then first 32 locations out of 128 are allocated for register banks, then 16 locations for bit-addressable area so now left 80 ($128 - 32 - 16 = 80$) all this remaining locations are assigned for general purpose.

Or

30 to 7f are allocated as general purpose locations.

So $7f - 30 = 79$ (d)....means 0-79...total 80 locations.

Or

32 locations out of 128 are allocated for 4 register banks, than 16 locations for bit-addressable area. So now 80 ($128 - 32 - 16 = 80$) remaining locations are assigned for general purpose.

Or

Its 80 bytes.

Internal data memory of 128 bytes is divided as,

1. Four register banks, each of 8 bytes. I.e $8 \times 4 = 32$ bytes.
2. Bit addressable memory of 16 bytes.

3. Remaining for general purpose data storage and stack, i.e 4.
128 - (32+16) = 80 bytes.

18. Microcontrollers often have:

- a) Cpus
- b) Ram
- c) Rom
- d) All of the above

Answer: option D

Explanation:-

Because, the microcontroller will be the type of specific microcomputer. It is integrated with all internal and external ram and rom and cpu all those.

19. The 8051 has _____ parallel i/o ports.

- a. 2
- b. 3
- c. 4
- d. 5

Answer: option C

Explanation:-

The 8051 has 4 i/o ports they are:

port 0.

Port 1.

Port 2.

Port 3.

Or

Because 4 ports we can access at the same point of time.

20. The total external data memory that can be interfaced to the 8051 is:

- a. 32k
- b. 64k
- c. 128k
- d. 256k

Answer: option B

Explanation:-

As the number of address lines of 8051 is 16 therefore
total memory that can b interfaced=($2^{16}=65536$) i.e. 64k

Or

Program counter(pc) size = 16 bit in binary.

=> can store addresses up to $2^{16} = 65536$ (total memory space) in

decimal.

I.e. From 0 to 65535 in decimal and 0000h to fffffh in hex.

1 kb=1024 bytes.

Converting 65536 bytes to kilo bytes.

pc can store 65536 'bytes' of memory space = $65536/1024 = 64k$.

21. Which of the following instructions will load the value 35h into the high byte of timer 0?

- a. **Mov th0, #35h**
- b. **Mov th0, 35h**
- c. **Mov t0, #35h**
- d. **Mov t0, 35h**

Answer: option A

Explanation:-

In 8051 microcontroller '#' symbol is the indication of moving immediate data into the register mentioned in the instruction.

Or

'#' Symbol is used for indication of number. When number is used without '#' symbol it means that the same number is representing address.

E.g.

#35h - hex number 35.

35h - hex number indicating address.

Or

To is a timer pin used to give delay pulses whereas tho is special function register where we can store data.

22. Bit-addressable memory locations are:

- a. **10h through 1fh**
- b. **20h through 2fh**
- c. **30h through 3fh**
- d. **40h through 4fh**

Answer: option B

Explanation:-

Register banks: 00 to 1f(32 bytes)

bit memory: 20 to 2f(16 bytes)

stack and for users : 30 to 7f(80 bytes)

total: 128 bytes(internal ram)

after internal ram after 80h to ffh : sfr (addressed using direct addressing mode)

23. The 8-bit address bus allows access to an address range of:

- a. 0000 to ffffh
- b. 000 to fffh
- c. 00 to ffh
- d. 0 to fh

Answer: option C

Explanation:-

$$2^8 = 256 = \text{ffh}$$

Or

1 digit in hexadecimal is treated as 1 nibble(4 bits) so 8 bit address bus can be accessed by two digits which is of hexa decimal part (h).

24. The contents of the accumulator after this operation

mov a,#0bh

anl a,#2ch

will be

- a. 11010111
- b. 11011010
- c. 00001000
- d. 00101000

Answer: option C

Explanation:-

First you convert 0b value into binary values after that same 2c value also and add and operation

$$0b = 0000\ 1011$$

$$2c = 0010\ 1100$$

and do and operation = 00001000

Or

Question is not there to ask why you are using and operation.....

By seeing program u v to do....

First of all.... Value of 0b will move to accumulator..

I.e.. A=0b=0000 1011

in 2nd step again the value of 2c will move to accu.. Where we r using and operation..

Anl is nothing but logical and operation...

Finally

$$a=0b=0000\ 1011$$

$$a=2c=0010\ 1100$$

at last after using and operation

a=0000 1000 is answer.

Or

The first command move the immediate value 0b into accumulator,

2nd command do and operation with the immediate value 2c with

accumulator.

0b= 0000 1011

2c= 0010 1000

and=0000 1000 it is equivalent to 08.

Or

We generally use and logic to set a particular bit in active high condition.
And or logic in viceverse condition.

Or

Truth table.

A b o/p

0 0 0

0 1 0

1 0 0

1 1 1

25. The start-conversion on the ADC0804 is done by using the:

- a. \overline{SC}
- b. Cs line
- c. Intr line
- d. $V_{ref/2}$ line

Answer: option A

Explanation:-

Sc (bar) means start of conversion pin. If we enable that pin on the ic the conversion starts.

26. This program code will be executed once:

Stat: Mov a, #01h

Jnz stat

- a. True
- b. False

Answer: option B

Explanation:-

Here 01h will get stored in acc, it is not a counter

Or

This code will hang down the processor.

Jnz - jump if not zero.

But, a will hold value 1 (not zero condition satisfies), so continuous loop will occur.

Or

Jnz-jumpnonzero is a loop command..
Display the output until its be zero..
Here the accumulator just get the input as one..
Or
Infinite loop will generate.

27. Which of the following instructions will move the contents of register 3 to the accumulator?

- a. Mov 3r, a
- b. Mov r3, a
- c. Mov a, r3
- d. Mov a, 3r

Answer: option C

Explanation:-

Both are registers. Hence we can use register addressing mode.

28. Which of the following statements will add the accumulator and register 3?

- a. Add @r3, @a
- b. Add @a, r3
- c. Add r3, a
- d. Add a, r3

Answer: option D

Explanation:-

Add always come with a register. Accumulator register will be the destination.

So ans is = add a, r3.

Or

For arithmetic operations the first operand must be accumulator.

29. Data transfer from i/o to external data memory can only be done with the mov command.

- a. True
- b. False

Answer: option B

Explanation:-

It is throw the movx.
But mov used for internal.
Or
External code memory movc.
External data memory movx.

30. Which of the following commands will move the number 27h into the accumulator?

- a. Mov a, p27
- b. Mov a, #27h
- c. Mov a, 27h
- d. Mov a, @27

Answer: option B

Explanation:-

The answer is mova,#27h

because it directly move the data into accumulator
and command mova,27h move d data from memory location 27h into
accumulator ok

31. This program code will read data from port 0 and write it to port 2, and it will stop looping when bit 3 of port 2 is set:

Stat: Mov a, po

Mov p2,a

Jnb p2.3, stat

- a. True
- b. False

Answer: option A

Explanation:-

Because

1st step: reads data frm port0

2nd step: writes data to port2

3rd step: it checks for bit 3 of port2 if it z '0' it will go to stat label this repeats until bit 3 sets.

Jnb means jump if not bit(means it cheks whether that particular bit zero or not).

Or

Jnb is jump if not set then how come the answer is true? As question is about set jb.

32. Which of the following commands will move the value at port 3 to register 2?

- a. Mov p2, r3
- b. Mov r3, p2
- c. Mov 3p, r2
- d. Mov r2, p3

Answer: option D

Explanation:-

To move value of port3 to r2; r2 should be in destination position of the move operation and p3 in source position.

33. The number of data registers is:

- a. 8
- b. 16
- c. 32
- d. 64

Answer: option C

Explanation:-

Data registers are register banks.

4 register banks and each having r0 to r7.

Totally 32.

Or

But we can access only single bank at a time while programming so mention it that how many data reg available in controller.

Or

There are four register bank(bank 0,1,2,3),each register bank store 8 bit data.therefore $4 \times 8 = 32$ data registers.

34. When the 8051 is reset and the ea line is low, the program counter points to the first program instruction in the:

- a. Internal code memory
- b. External code memory
- c. Internal data memory
- d. External data memory

Answer: option B

Explanation:-

I think it should be a psen (low) line.

Or

Here ea bar is low mean ea is 1... So external memory...(may be)..

Or

It is external code memory because when ea bar is low means ea is high so it will access data from external code section only.

35. The designs of a centigrade thermometer and a pwm speed-control circuit can be implemented by the 8051.

- a. True
- b. False

Answer: option A

Explanation:-

One of the practical examples of the use of pwm technique is the speed control of dc motor.

36. What is the difference between the 8031 and the 8051?

- a. The 8031 has no interrupts.
- b. The 8031 is rom-less.
- c. The 8051 is rom-less.
- d. The 8051 has 64 bytes more memory.

Answer: option B

Explanation:-

In 8031 rom is not necessary but we can attach an external rom...

37. The i/o port that does not have a dual-purpose role is:

- a. Port 0
- b. Port 1
- c. Port 2
- d. Port 3

Answer: option B

Explanation:-

P0 & p2 have address and data lines (dual - role).

P3 have i/o and serial, interrupt, timer role, p2, p0 have address role for external access (dual - role).

But p1 only has data lines only.

So answer is p1.

38. To interface external eprom memory for applications, it is necessary to demultiplex the address/data lines of the 8051.

- a. True
- b. False

Answer: option A

Explanation:-

Yes, because when we are accessing eeprom that time we have need 16 bit address line as well as 8 bit data line also we can use it. Both operation we can perform it.

39. The following command will copy the accumulator to the location whose address is 23h:

`mov 23h,a`

- a. True
- b. False

Answer: option A

Explanation:-

The accumulator value will be shifted to the address mentioned i.e 23h

Or

It is direct addressing mode. So address is mentioned in dest i.e 23h.

40. The special function registers can be referred to by their hex addresses or by their register names.

- a. True
- b. False

Answer: option A

Explanation:-

It's true,

each sfr is stored at fixed memory location (0x80h to 0xffh) in internal memory of 8051. So we can access them by using sfr names or by the hex value of its memory location. After compilation each sfr name is converted into its hex address value.

E.g.

Mov a, #0ffh is can be written as,

mov 0e0h, #0ffh.

Also you can check lst (file extension) file in your project directory.

41. The contents of the accumulator after this operation

mov a,#2bh

orl a,00h

will be:

- a. 1b h
- b. 2b h
- c. 3b h
- d. 4b h

Answer: option B

Explanation:-

Orl means logical or when perform the or operation between high value and low value then output always high value.

Or

0010 1011 =2bh

0000 0000 =00h

0010 1011 =2bh (orl logiacl or)answer

Or

Because the truth table of or operation is.

1 or with 0, 1 or with 1, 0 or with 1 gives result 1.

0 or with 0 = 0.

Then, 2bh or with 00h = 2bh.

42. The following program will cause the 8051 to be stuck in a loop:

Loop: Mov a, #00h

Jnz loop

- a. True
- b. False

Answer: option B

Explanation:-

Actually jnz means jump if accumulator is not zero means if accumulator is one only it jump the loop otherwise end the loop.

Or

If it is

mov ,#2ch

jnz lop

then what will be the answer?

Or

Accumulator value is not zero so loop continue.

43. Which of the following commands will copy the contents of ram whose address is in register 0 to port 1?

- a. Mov @ p1, r0
- b. Mov @ r0, p1
- c. Mov p1, @ r0
- d. Mov p1, r0

Answer: option C

Explanation:-

'@' Indicates the address of register.

So the address of r0 will move to p1.

44. The statement lcall read passes control to the line labelled read.

- a. True
- b. False

Answer: option A

Explanation:-

Call statement is of two type

- 1.) Acall label
- 2.) Lcall label

45. Which of the following commands will copy the contents of location 4h to the accumulator?

- a. Mov a, 04h
- b. Mov a, l4

- c. Mov I4, a
- d. Mov 04h, a

Answer: option A

Explanation:-

According to direct addressing mode, the contents of location 4h will be copied into accumulator.

46. The microcontroller is useful in systems that have nonvariable programs for dedicated applications.

- a. True
- b. False

Answer: option A

47. The total amount of external code memory that can be interfaced to the 8051 is:

- a. 32k
- b. 64k
- c. 128k
- d. 256k

Answer: option B

Explanation:-

We can use 16 lines for external memory interface.
So $2^{16} = 65536 \Rightarrow 64k$.

48. The ADC0804 has _____ resolution.

- a. 4-bit
- b. 8-bit
- c. 16-bit
- d. 32-bit

Answer: option B

49. A high on which pin resets the 8051 microcontroller?

- a. Reset
- b. Rst
- c. Psen
- d. Rset

Answer: option B

Explanation:-

How does that occurs i think option a is the right one as rst pin is not present in pin diagram of 8051.

Or

Reset bar is available for 8051, so we should make it logic 0 to active.

50. An alternate function of port pin p3.1 in the 8051 is:

- a. Serial port input
- b. Serial port output
- c. Memory write strobe
- d. Memory read strobe

Answer: option B

Explanation:-

P3.0,p3.1=r*d,t*d

p3.2&p3.3=external interrupts

p3.4&p3.5=t0,t1

p3.6,p3.7=wr,rd

Or

P3.0 and p3.1 are for serial mode communication. P3.0 (rxd) receives the serial data given at the port and p3.1 (txd) transfers the serial data through the port.

So rxd is serial port input whereas txd is serial port output.

51. Which of the following instructions will move the contents of the accumulator to register 6?

- a. Mov 6r, a
- b. Mov r6, a
- c. Mov a, 6r
- d. Mov a, r6

Answer: option B

53. An alternate function of port pin p3.0 (rxd) in the 8051 is:

- a. Serial port input
- b. Serial port output
- c. Memory write strobe
- d. Memory read strobe

Answer: option A

Explanation:-

P3.0 and p3.1 are for serial mode communication. P3.0 (rxd) receives the serial data given at the port and p3.1 (txd) transfers the serial data through the port. So rxd is serial port input whereas txd is serial port output.

TRUE/FASLE

1. Analog output current must be converted into a usable voltage. To perform this current-to-voltage conversion a 700 op amp may be used.

- a. True
- b. False

Answer: option A

2. A celsius thermometer is an application for the 8051 microcontroller.

a. True

b. False

Answer: option A

Explanation:-

Lm35 is the temperature sensor ic which is interface with ADC to microcontroller.

3. The rst pin requires a high to reset the 8051 microcontroller.

a. True

b. False

Answer: option A

4. A microcontroller is called a computer on a chip.

a. True

b. False

Answer: option A

5. In an 8051 program da a adjusts the value in the accumulator resulting from an addition into two BCDs.

a. True

b. False

Answer: option A

6. Different instruction sets must make up for the various members of the 8051 family.

a. True

b. False

Answer: option B

Explanation:-

I think different memories will make different members of 8051. Because 8031 doesn't have rom.

7. The ADC 0804 is an analog-to-digital converter that provides 8-bit output resolution that can be directly interfaced to a microcontroller.

a. True

b. False

Answer: option A

8. Writing counter/loop programs is much more difficult with the introduction of the djna and the cjne instructions.

- a. True
- b. False

Answer: option B

9. The 8051 is a 40-pin ic. Twenty-two pins are needed for the four i/o ports.

- a. True
- b. False

Answer: option B

Explanation:-

8051 is a 40-pin ic.

8051 needs 8 pins to one i/o ports.

So, $(4 \times 8 \text{ pins}) = 32$ pins will be needed for 4 i/o ports.

Hence it is false.

10. Up to 65k of code memory and 65k of data memory can be added to any of the 8051 family members.

- a. True
- b. False

Answer: option B

Explanation:-

Answer is false.

Because, for 8051 family variants we can connect 64 kbytes of memory externally.

We can use that external memory for code memory and as well as data memory.

So there is no external code or data memory. Its depends on us how we use it.

Or

2^8 code memory and 2^{16} data memory.

28.COMPUTERS

1. Which of the following is not a basic element within the microprocessor?

- a. Microcontroller
- b. Arithmetic logic unit (alu)
- c. Register array
- d. Control unit

Answer: option A

Explanation:-

Microcontroller is not part of the mp, because it is own ic and thier functions.

Or

Alu,control unit and register arrey is built in microprocessor while microcontroller is advanced version of microprocessor. Therefore microcontroler is not a integral part of microprocessor.

Or

A microcontroller is an device which comprises of microprocessor, ram, rom.
Etc.

A microcontroller can have microprocessor but not vice versa.

Or

Microprocessor is "cpu on chip" but microcontroller is "computer on chip" which consist of cpu itself.

2. Which method bypasses the cpu for certain types of data transfer?

- a. Software interrupts
- b. Interrupt-driven i/o
- c. Polled i/o
- d. Direct memory access (dma)

Answer: option D

Explanation:-

Whenever we need to interrupt or pass data dma control will have buses required.

3. Which of the following is not an enhancement to the pentium that was unavailable in the 8086/8088?

- a. "pipelined" architecture
- b. Expansion of cache memory
- c. Inclusion of an internal math coprocessor
- d. Data/address line multiplexing

Answer: option D

4. Which bus is bidirectional?

- a. Address bus
- b. Control bus
- c. Data bus
- d. None of the above

Answer: option C

Explanation:-

Control bus is also bidirectional.

4. Which bus is bidirectional?

- a. Address bus
- b. Control bus
- c. Data bus
- d. None of the above

Answer: option C

Explanation:-

Control bus is also bidirectional.

5. Dma is particularly suited for data transfer between the _____.

- a. Disk drive and cpu
- b. Disk drive and ram
- c. Disk drive and rom
- d. Disk drive and i/o

Answer: option B

Explanation:-

"direct memory access." dma is a method of transferring data from the computer's ram to another part of the computer without processing it using the cpu. While most data that is input or output from your computer is processed by the cpu, some data does not require processing, or can be processed by another device. In these situations, dma can save processing time and is a more efficient way to move data from the computer's memory to other devices.

6. The first microprocessor had a(n)_____.

- a. 1-bit data bus
- b. 2-bit data bus
- c. 4-bit data bus
- d. 8-bit data bus

Answer: option C

Explanation:-

Intel 4004 is the world's 1st up. Made by intel corporation in 1971 which has 4-bit data bus.

7. Which microprocessor has multiplexed data and address lines?

- a. 8086/8088
- b. 80286
- c. 80386
- d. Pentium

Answer: option A

8. Which is not an operand?

- a. Variable
- b. Register
- c. Memory location
- d. Assembler

Answer: option D

Explanation:-

Assembler is used to convert assembly language to binary language so it can be an operand.

9. Which is not part of the execution unit (eu)?

- a. Arithmetic logic unit (alu)
- b. Clock
- c. General registers
- d. Flags

Answer: option B

Explanation:-

The eu receives program instruction codes and data from the biu, executes these instructions, and store the results in the general registers. By passing the data back to the biu, data can also be stored in a memory location or written to an output device. Note that the eu has no connection to the system buses. It receives and outputs all its data through the biu.

Or

Biu means bus interface unit by which data and address are passed.

10. A 20-bit address bus can locate _____.

- a. 1,048,576 locations
- b. 2,097,152 locations
- c. 4,194,304 locations
- d. 8,388,608 locations

Answer: option A

Explanation:-

$$2^{20} = 1048576$$

Or

With 20-bit bus we can locate 2^{20} locations. 00000000000000000000 to 11111111111111111111 is the address range.

Or

$$1024 * 1024 = 1048576.$$

11. What is occurring when two or more sources of data attempt to use the same bus?

- a. Bus contention
- b. Direct memory access
- c. Bus interruption
- d. Ppi

Answer: option A

Explanation:-

Is an undesirable state of the bus in which more than one device on the bus attempts to place values on the bus at the same time.

12. Which of the following is not a jump instruction?

- a. Jb (jump back)
- b. Ja (jump above)
- c. Jo (jump if overflow)
- d. Jmp (unconditional jump)

Answer: option A

13. Which of the following was not a design improvement for the 8086/8088 over the 8085?

- a. Execution unit (eu)
- b. 16-bit data bus
- c. Arithmetic logic unit (alu)
- d. Bus interface unit (biu)

Answer: option C

14. Polled i/o works best when _____.

- a. There are no priority considerations
- b. Priority considerations are frequent
- c. The polling rate exceeds 1000 s
- d. The polling rate is below 1000 s

Answer: option A

Explanation:-

Polling means continuously scanning of data lines for i/o devices. If there are no priority considerations it works best.

15. Which of the following is not an arithmetic instruction?

- a. Inc (increment)
- b. Cmp (compare)
- c. Dec (decrement)
- d. Rol (rotate left)

Answer: option D

Explanation:-

Compare uses subtraction operation thus it is arithmetic instruction, while rol is logical.

16. During a read operation the cpu fetches _____.

- a. A program instruction
- b. Another address
- c. Data itself
- d. All of the above

Answer: option D

17. The first intel microprocessor to contain on-board cache memory was the _____.

- a. 80386
- b. 80486
- c. Pentium
- d. Pentium pro

Answer: option B

18. Which of the following is not an 8086/8088 general-purpose register?

- a. Code segment (cs)
- b. Data segment (ds)
- c. Stack segment (ss)
- d. Address segment (as)

Answer: option D

19. Which of the following is not a computer bus?

- a. Data bus
- b. Control bus
- c. Timer bus
- d. Address bus

Answer: option C

20. With interrupt-driven i/o, if two or more devices request service at the same time, _____.

- a. The device closest to the cpu gets priority
- b. The device that is fastest gets priority
- c. The device assigned the highest priority is serviced first
- d. The system is likely to crash

Answer: option C

21. The pentium can address _____.

- a. 1 mb
- b. 1 gb
- c. 2 gb
- d. 4 gb

Answer: option D

Explanation:-

On the pentium processor, the 4gb address space is split into two regions: a large-space area (of, say, 2gb), and a small-space area, which makes up the remainder of the hardware address space. The small-space area is itself split into a number of small-space regions, each of which can hold a small address space. A process which is to run in a small address space is assigned a small-space number, identifying which of the small-space regions it is to use. The segmentation registers are then used to relocate the process's address space into that region. A "large" process is not relocated and has access to the whole large-space area. The number of small processes is limited to the number of small-space regions.

Or

Pentium 4 processor i.e. 4gb.

22. A port can be _____.

- a. Strictly for input
- b. Strictly for output
- c. Bidirectional
- d. All of the above

Answer: option D

23. Which of the following is not a computer functional block?

- a. Analog-to-digital converter
- b. Central-processing unit
- c. Memory
- d. Input/output ports

Answer: option A

24. The pentium microprocessor has a data bus of _____.

- a. 16 bits
- b. 32 bits
- c. 64 bits
- d. 128 bits

Answer: option C

25. The process of jointly establishing communication is called _____.

- a. Dma
- b. Bidirectional addressing
- c. Multiplexing
- d. Handshaking

Answer: option D

TRUE/FALSE

1. A mnemonic is an english-like instruction that is converted by an assembler into a machine code for use by a processor.

- a. True
- b. False

Answer: option A

2. Chip designers are always trying to increase the clock speed.

- a. True
- b. False

Answer: option A

Explanation:-

Greater clock speed means better performance (in terms of execution of instructions).

3. Instructions for the 80x86 family are downward compatible.

- a. True
- b. False

Answer: option B

4. The pentium can execute two instructions at once.

- a. True
- b. False

Answer: option A

5. A coprocessor is a microprocessor designed with a limited instruction set optimized to perform arithmetic operations very quickly.

- a. True

b. False

Answer: option A

6. The original pentium was the first cpu to feature separate data and instruction caches.

a. True

b. False

Answer: option A

7. Machine language is independent of the type of microprocessor in a computer system.

a. True

b. False

Answer: option B

8. The pci bus is a good example of an external bus for personal computers

a. True

b. False

Answer: option A

9. The power pc can effectively execute up to ten instructions per clock cycle.

a. True

b. False

Answer: option B

10. Polling is the process of pausing the normal sequence of instructions to cause the processor to execute a separate set of i/o instructions instead.

a. True

b. False

Answer: option B

Explanation:-

It is called interrupt not polling.

FILL IN THE BLANKS

1. The and, or, and test instructions are all part of which type of instruction?

a. Data transfer

b. Arithmetic

c. Bit manipulation

d. Loops and jumps

Answer: option C

2. A mini-program that can be used repeatedly, but is programmed only once is called a(n) _____.

- a. String**
- b. Subroutine**
- c. Interrupt**
- d. Processor control**

Answer: option B

3. Contiguous sequences of bytes or words are called _____.

- a. Data transfer**
- b. Arithmetic**
- c. Loops and jumps**
- d. Strings**

Answer: option D

4. An interrupt method that requires the cpu to test each peripheral device in sequence is called _____.

- a. Vectored i/o**
- b. Polled i/o**
- c. Programmed interrupt**
- d. Interrupt-driven i/o**

Answer: option B

5. An example of a unidirectional bus in a microcomputer system is the _____.

- a. Address bus**
- b. Data bus**
- c. Control bus**
- d. All of the above**

Answer: option A

Explanation:-

Control bus is also unidirectional

6. The add, cmp, and mul instructions are all part of which type of instruction?

- a. Data transfer**
- b. Arithmetic**
- c. Bit manipulation**
- d. Loops and jumps**

Answer: option B

7. Instructions that allow direct control of the processor's flags are called _____ instructions.

- a. Data transfer
- b. Arithmetic
- c. Bit manipulation
- d. Processor control

Answer: option D

8. The mov, push, and pop instructions are all part of which type of instruction?

- a. Data transfer
- b. Arithmetic
- c. Bit manipulation
- d. Loops and jumps

Answer: option A

9. The jnz, ja, and loop instructions are all part of which type of instruction?

- a. Data transfer
- b. Arithmetic
- c. Bit manipulation
- d. Loops and jumps

Answer: option D

10. During a memory read operation, the cpu fetches _____.

- a. A program instruction
- b. An address
- c. Data
- d. All of the above

Answer: option D