Question # 1

a) What is understood by computer architecture and organization? Explain the detail

Computer architecture refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program

Examples: Instruction set, the number of bits used to represent various data types (e.g., numbers, characters), I/O mechanisms etc.

It is an architectural design issue whether a computer will have a multiply instruction or not.

Computer organization refers to the operational units and their interconnections that realize the architectural specifications

Organizational attributes include those hardware details transparent to the programmer

Examples: Control signals; interfaces between the computer and peripherals; and the memory technology used.

It is an organizational issue whether that instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.

b) State the key concept of von-Neumann architecture

All computers today have von Neumann architecture which means the following key concepts

- Data and instruction are stored in a single read/write memory
- The content of this memory addressable by location without regard to the type of the data contain.
- Execution occurs in a sequential functions unless explicatively modified. From one instruction to the next

Question # 2

a) Name the four elements that an instruction must contain implicitly and explicitly

Operation code (Op code)

Source Operand reference

Result Operand reference

Next Instruction Reference

b) List types of operation an instruction an instruction set must have

Data processing (Arithmetic & Logical)

Data storage

Data movement (I/O)

Control (test and branch structure)

Question # 3

a) What are the drawbacks of signed magnitude representation?

i) Has the problem of double representing the 0 (â€“0 and +0),
ii) Complicates the design of the logic circuits that handle signed-numbers arithmetic,
iii) This is because each of the sign and magnitude parts has to be processed separately,
iv) Also, the sign of both numbers have to be examined before the actual operation (addition or subtraction) is determined,
v) Separate circuits are required to do the addition and subtraction operations

b) State the overflow rule of addition of two numbers represented in 2's complement notation

1) If the sum of two positive numbers yields a negative result, the sum has overflowed.
2) If the sum of two negative numbers yields a positive result, the sum has overflowed.
3) Otherwise, the sum has not overflowed.

Question # 5

a) Identify and list types of exchanges that are needed or memory modules, I/O modules Processors

Nature of operation (read / write)

Address (location of operator)

Data (read/write)

Control signal

Interrupt

b) Identify and discuss the elements that must be considered for bus design

Type: dedicated and multiplexed

Method of arbitration:

Centralized: A single hardware device called the bus controller.

Distributed: Each module contains access central logic and the modules act together.

Timing

Synchronous: Occurrence of event on the bus is determined by clock

Asynchronous: Occurrence of event follows and depend on occurrence of pre event

Bus width

Address Bus Width: maximum possible devices connect

Data Bus Width: the greater number of bit transferred at one time.

Data transfer type: Read, write, read modify write, read after write, block transfer

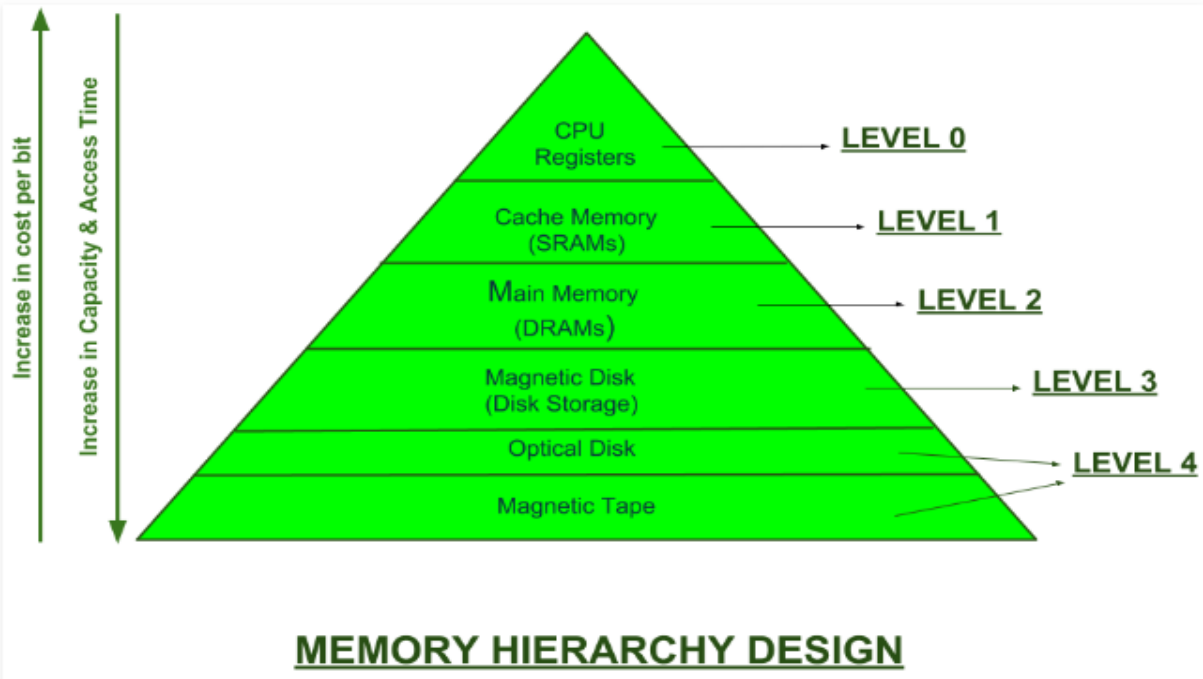
Question # 4

a) **What is thrashing in cache and what suggestions designers suggest to overcome this problem?**

If a program reference words repeatedly from two different blocks that's maps into same line, then the blocks will be continuously swapped and the hit ratio will be low, this continuous swapping is known as thrashing in cache.

b) **What is meant by memory hierarchy? What does it represent as you move down from top?**

In the Computer System Design, Memory Hierarchy is an enhancement to organize the memory such that it can minimize the access time. The Memory Hierarchy was developed based on a program behaviour known as locality of references.



MEMORY HIERARCHY DESIGN

Question # 6

a) **How instruction pipelining enhance system performance and what factors serve to limit the performance enhancement**

Factors serve to limit the performance enhancement.

- If all the stages are not of equal duration, there will be some waiting involved at various pipeline stages.
- In case of a conditional branch instruction, several instruction fetches can be invalidated.
- An interrupt can also invalidate several instruction fetches

b) Describe the following types of hazards

I) Structural (ii) data (iii) control

DATA HAZARDS: A data hazard occurs when there is a conflict in the access of an operand location.

CONTROL HAZARDS: A control hazard, also known as a branch hazard, occurs when the pipeline makes the wrong decision on a branch prediction and therefore brings instructions into the pipeline that must subsequently be discarded

RESOURCE HAZARDS: A resource hazard occurs when two (or more) instructions that are already in the pipeline need the same resource. The result is that the instructions must be executed in serial rather than parallel for a portion of the pipeline. A resource hazard is sometime referred to as a structural hazard.

Question # 7

a) Explain how precision of floating point number can be improved, and how to increase range. Use examples to support your answer

Representation of Floating-Point numbers = $-1^S \times M \times 2^E$

Bit No	Size	Field Name
31	1 bit	Sign (S)
23-30	8 bits	Exponent (E)
0-22	23 bits	Mantissa (M)

A Single-Precision floating-point number occupies 32-bits, so there is a compromise between the size of the mantissa and the size of the exponent.

These chosen sizes provide a range of approximate: $\pm 10^{-38} \ldots 10^{38}$

Overflow: The exponent is too *large* to be represented in the Exponent field

Underflow: The number is too *small* to be represented in the Exponent field

To reduce the chances of underflow/overflow, can use 64-bit **Double-Precision** arithmetic

Bit No	**Size**	**Field Name**
63	1 bit	Sign (S)
52-62	11 bits	Exponent (E)
0-51	52 bits	Mantissa (M)

providing a range of approx

$$\pm 10^{-308} \ldots 10^{30}$$

b) Explain what is understood by 'biased exponent' representation? How does it take into account the sign of component? What are the advantages of this kind of representation?

In floating-point arithmetic, a biased exponent is the result of adding some constant (called the bias) to the exponent chosen to make the range of the exponent nonnegative

The biased exponent has advantages over other negative representations in performing bitwise comparing of two floating point numbers for equality. The range of exponent in single precision format is -128 to +127. Other values are used for special symbols

Question # 8

a) Two floating point numbers X & Y, as shown below in IEEE format, are multiplied together to get the product Z. show the bit pattern of product in IEEE format.

X= 0 0101 0000 0000 0000 0000 0000 0000 000

Y= 1 1010 0101 0000 0000 0000 0000 0000 000

Question # 9

(a) Describe the significant characteristics of point-to-point interconnect scheme

The following are significant characteristics of QPI and other point-to-point interconnect schemes:

■ Multiple direct connections: Multiple components within the system enjoy direct pairwise connections to other components. This eliminates the need for arbitration found in shared transmission systems.

■ Layered protocol architecture: As found in network environments, such as TCP/IP-based data networks, these processor-level interconnects use a layered protocol architecture, rather than the simple use of control signals found in shared bus arrangements.

■ Packetized data transfer: Data are not sent as a raw bit stream. Rather, data are sent as a sequence of packets, each of which includes control headers and error control codes.

b) Compare working of following access methods. Also identify applications

i) **Linear or sequential access method**: time to access an arbitrary record is highly variable depending on read write head's current and desired location

ii) **Direct access method:** In direct access method individual blocks of record have unique address based on physical location access is direct to the desired block then sequential for the required address

iii) **Random Access:** Each addressable location have a unique addressing mechanism access time is constant. Any location can be selected at random.

iv) Associative Access Method: In a storage device in which a location is identified by what is in it rather than by its position is known as associative access method.

Question # 10

(a) Explain how the presence of cache improves the system performance why do the transfers between main memory and cache memory take place in the form of block consisting of few memory locations? What is the purpose of TAG part of cache slot?

Cache is a small amount of memory which is part of the CPU which is physically closer to the CPU than RAM.

The cache size has a significant impact on performance. The larger a cache is, the less chance there will be of a conflict.

TAG identify which block of main memory is in each cache slot.

b) Explain the function of replacement algorithm in the implementation of cache memory. Discuss how LRU is implemented.

When Cache is full, a decision is to be made about which block should be removed to make room for the other block from the main memory, such a decision can potentially affect the system performance.

Thus the block that has stayed for long without being referenced should be removed. Such a block is known as LEAST RECENTLY USED (LPU) Block and the algorithm to determine such a block is known as LRU Algorithm.

Question # 11

a) What is understood by write through and write back policies? Which is commonly employed? What are the advantages and disadvantages of two policies