Design and Implementation of Power Efficient 8:1 Multiplexer using PTL Technology

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***Abstract*— The development in the methodologies of fundamental functional units of digital systems have raised the attention due to advancement in CMOS technology. Continuous demand of battery-powered portable electronics like cell phones, PDAs, and notebook computers has forced us to ensure low power dissipation in the CMOS circuits. One of the fundamental building blocks in digital design, MUX has been a major area of research interest for many years. System designers are showing a great emphasis on functional unit energy efficiency and technology scaling as a result. Ensuring low power consumption and building low power systems is a great challenge in the design of VLSI chips today and has become one of the key aspects of the electronic industries. In this article, fredkin gate is created using traditional PTL for developing an 8:1 MUX. The circuit's power consumption is decreased as it is having fewer transistors. Initially in conventional 8:1 MUX the number of transistors used was more than 42. [1] In our article we have fredkin gate and hence the number of transistors can be reduced to 42. Hence a drop considerable drop in power consumption of 5-15 percent is observed.**

Keywords—VLSI, PTL, Multiplexer.

I. Introduction

The property of reversible logic says that the synthesis techniques can be used for it, in both the conventional forward manner (where output signals are acts of input signals) and the reverse method (where input signals are acts of output signals). It suggests that by inverting the K-map for the output function and utilising it as a function to get inputs back from the output, we can get the inverse function for backtracking. Charge recovery is an underlying idea of reversible circuits. This results in significant power savings because switching nodes are used whenever there is a transition from small to superior or vice versa is necessary instead of adding split nodes to satisfy the requirements. In order to prevent resistive losses, the number of inputs and outputs in the circuits is constantly kept as constant. Without a question, one of the most important issues now facing nanoscale scale PTL technology is leakage power losses. [2]

Reversible logic gates which are commonly used work with binary numbers or bits. Quantum bits, or qubits, are affected by quantum gates. A qubit is a discrete quantum information unit. Reversible logic circuits also have definitions for some quantum gates, such as the Feynman gate and both universal logic gates, fredkin gate and Toffoli gate. Any reversible logic gate can only have a single fan-out. This merely means that only one input of a different gate may be driven by each output of a reversible logic gate. Quantum price, prejudiced number of gates, number of steady inputs, trash outputs, and lag are the common metrics of merit for quantum gates.

A multiplexer, sometimes referred to as a MUX, is a circuit that combines several analogue or digital input signals and sends them to a single output path. Electronic components that pick one of several analogue or digital input signals before sending it to a single output line are commonly referred to as data selectors. To determine which input line should be delivered to a multiplexer's output, select lines are employed. Multiplexers are typically used to increase the quantity of data that can be sent across the network in a given period of time and bandwidth. [3]

The use of multiplexers may also be used to build boolean functions with a large number of variables. Multiplexers enable numerous signals to share a single device or resource, such as an A/D converter or communication line, instead of using separate devices for each of the input signals.. In contrast, a demultiplexer (also known as a DEMUX) is a component that accepts one input and selects signals from the compatible mux's output that is linked to the single input as well as from a common selection line. It is common practise to pair a multiplexer with a corresponding demultiplexer at the receiving end. A demultiplexer is a single-input multiple-output control, whereas an electronic multiplexer is a multiple -input, single-output control.

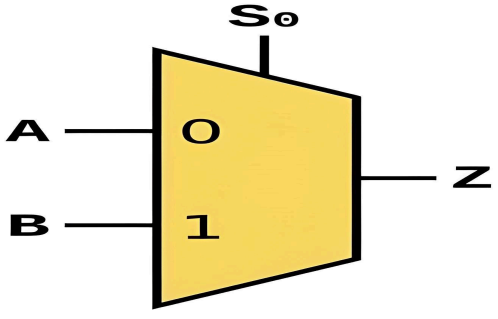

Fig.1 2:1 Multiplexer

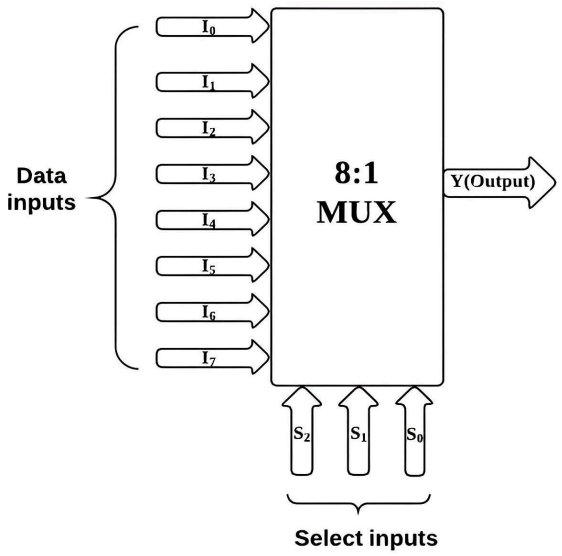

Fig.2 8:1 Multiplexer Block Diagram

II. Comparision (conventional vs new)

The most frequently utilised logic component in virtually all computational circuits is a multiplexer. The fundamental function of a multiplexer is data selection through various combinations of choose line inputs. They function as data selectors, choosing one of available inputs for output based on input chosen by the select line. The availability of tools that can carry out numerous tasks is highly desirable. It is essential to conserve energy when using a circuit, especially when using a unit repeatedly. It is a crucial part of communication systems as well. At all levels, every communication circuit must have a multiplexer and a demultiplexer. [4]

The typical fredkin gate operates as 2:1 multiplexer by itself. First input serves as the choose line to decide which of the second and third inputs will be the output. Fredkin gates are fault tolerant due to their inherent ability to preserve parity, which completely removes possibility of any outputs non concurrence for a given set of inputs.

Fig. 2 shows the suggested 8:1 multiplexer which comprises of seven 2: 1 multiplexers, giving it 11 inputs and 1 output. The truth table will have 2048 rows, which is a lot of data. Using the three selectors X0, X1, and X2, Table I links the 8 inputs to 1 output. As a result, according to Table-I, the output A is chosen whenever the sum of X0, X1, and X2 values is zero bits. The remaining combination of chosen lines is organised similarly. [5]

Selectors			Result
0	0	0	P
0	0	1	Q
0	1	0	R
0	1	1	S
1	0	0	T
1	0	1	U
1	1	0	V
1	1	1	X

Table 1. Truth Table of 8:1 Multipexer

Table 1 above illustrates the suggested QCA configuration for the 8:1 multiplexer, which was built using seven multiplexer gates. The 8 inputs in this block are P, Q, R, S, T, U, V, and X. The 3 select lines are X0, X1, and X2 and the ultimate result of the whole multiplexer is RESULT. The selector chooses P as the output when X0 X1 X2 equals 000, Q as the output when X0 X1 X2 equals 001, R as the output when X0 X1 X2 equals 010, S as the output when X0 X1 X2 equals 011, S as the output when X0 X1 X2 equals 100, T as the output when X0 X1 X2 equals 101, and U as the output when X0 X1 X2 equals 110 When X0 X1 X2 = 111, X is chosen. RESULTS = X0'.X1'.X2'.P + X0'.X1'.X2.Q + X0'.X1.X2'.R + X0'X1 X2 S +X0 X1'X2' T +X0 X1'X2' U + X0 X1' X2' V + X0 X1 X2 X is the suggested QCA layout's logic.

The output pin is located in the shorter parallel side and the input pins are located in the longer parallel side of an isosceles trapezoid, which is the schematic representation of a multiplexer. The intended input and output are connected by this wire. The choice of materials utilized in first circular design has a distinct value. A two-to-one multiplicator is a logical conclusion from the fact that there is zero. This number is for inputs. As an example, 9 to 16 participants would require at least 4 selection points, whereas 1 in 7 to 3 in participants would require at least 5 selection points. [6]

III. previous research

A review of the literature in the field under consideration is provided below after a number of research articles published in different journals and conferences have been examined:

Sumithi Manickam and others (2007) This study examines the various complementary metal-oxide semiconductor (CMOS) multiplexer architectures from the standpoint of performance. Positive Feedback Adiabatic Logic (PFAL), Cascade Voltage Switch Logic (CVSL), and Transmission Gate Based logic styles are used to build the multiplexer architectures. The designs' power consumption, delay, supply voltage, and transistor count are tallied and compared. In order to conduct the performance investigation, 0.18-m CMOS technology is used. By employing the CAD tools of DSCH3 and Micro wind 3. 1, thorough transistor-level simulations are used to distinguish between these various logic approaches. [7]

Dr. M. Sumati and others (2007) The standard single-ended LNA and differential LNA design theories based on CMOS technology are presented in this study. The design ideas serve as a helpful guide for understanding the trade-offs between NF, gain, and impedance matching. Four LNAs have been created utilising the TSMC's technical design guidelines. [8]

This work is primarily proposed for IEEE 802.11 applications and uses 0.18 m CMOS technology. [9] The suggested LNAs produce a gain more than 19dB, a noise figure less than 4dB, and impedance matching less than

-10dB at 5GHz frequency with 1.8 V supply voltage. In order to simultaneously achieve gain, noise reduction, and input matching at low supply voltage, this paper's objective is to highlight the effective LNA design. Using the Electronic Design Automation tools in Agilent's Advanced Design System, the performance of each LNA is evaluated and compared. Rajeev Kumar and others (2014) The performance of several complete adder circuits that were created utilising methods like XOR, transmission gates, multiplexers, etc. is evaluated and compared in this research. Additionally, a complete adder circuit made with multiplexers is suggested. At a supply voltage of 2.5V, the performance of these circuits is based on the 180 nm process model. The results of the SPICE simulation demonstrate that the suggested circuit performs better than circuits that are assessed from the literature. [10]

In This paper we will also try to reduce power consumption of MUX.

IV. Fredkin Gate

According to conventional logic, this gate is essentially a multiplexer that has been flipped, and control input A determines the output. Ed Fredkin and Tomasso Toffoli debuted it in 1982. It is required to first talk about the components of the Fredkin gate, particularly the V, V+, and CNOT gates, before describing the quantum circuit for this gate. [11]

Having a quantum cost of 1, the controlled NOT (CNOT) gate is a 22 gate. Gates that are 1-1 reversible have no quantum cost. The NOT gate's square root is the V gate, and its Hermitian is V+. Figure 1 depicts the quantum implementation of the CNOT gate. The following three equations give an explanation of the characteristics of V and V+ quantum gates: [12]

1. V × V=NOT
2. *V* × *V*+ =*V*+ × V=I
3. V+ × V+=NOT

The Feynman gate is a conservative, reversible, 3x3 gate. Each rectangle with a dot pattern serves as a Feynman diagram with a quantum value of 1. As a consequence, when two dot-filled rectangles, one IV gate, and two CNOT gates are added together, the total quantity of a Fredkin gate equals 5. The quantitative implementation of the Fredkin Gate is shown in the FIGURE. Due to the fact that most arithmetic operations do not retain the parity, the parity-checking capability of this gate is extremely helpful in the error detection process.

It may be used to find both ongoing and passing faults. Although it could be challenging to find many faults, it is completely effective in finding single faults. Additionally, it reduces the complexity of the circuit by eliminating the requirement for a separate error detection circuit. By using just one gate, we can create a 2:1 multiplexer that preserves parity, making it fault tolerant because error detection is not required at every stage. [13]

Each circuit contains exactly zero constant inputs. This is because higher level circuits are created using a 2:1 multiplexer, which is the smallest block employed in this system. Since the number of inputs at the first stage is exactly equal to the number needed in a 2:1 multiplexer, there is no longer any need to maintain any of the inputs constant.

The functionality of Fredkin gate can be described with the help of the following figure:

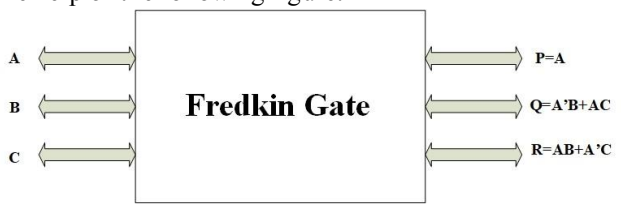

Fig.3 Fredkin Gate Block Diagram

The inverter with bulk-driven technology is used in the implementation of Fredkin gate.

Edward Fredkin was the first to develop the digital structure known as the Fredkin gate, which has three inputs and three outputs (A, B`, C) and the output vector is

- P = A
- Q = compA*B + AC
- R = AB + compAC.

Only the Fredkin gate, which has a quantum cost of 5 and is a universal reversible gate, may be used to build any logical function.

V. Implementation Methodology

The output is provided by the above-implemented Fredkin gate. Identical to a 2:1 multiplexer in every way. This suggests if the Fredkin gate's first input is used as a select line, then we can use this gate as a multiplexer itself. Afterward, this gate can be used as a multiplexer on its own. This acts as the building component for a 4:1 multiplexer. The 2:1 multiplexers are usually referred to as applied to create an 8:1 multiplexer.

It is abundantly obvious from the Fredkin gate's operation that it functions as a multiplexer in and of itself. It is not regarded as garbage value when the output bit is the same as the input bit. This suggests that the initial result was not a waste. The multiplexer output is provided by the second terminal, and the output in the event that the circuit's inputs B and C are switched is provided by the third terminal. [14]

In this methodology, it is defined that different types of technologies are used to design a multiplexer. Modern era of transportable devices such as cell phones, Laptops

power dissipation has turn out to be main concern in VLSI Design. Because batteries supplied partial power, the circuits are designed to consume least power and dimension of electronic devices are getting reduced day by day. The PTL circuit consume very less power consumption, but a major power issue of the PTL circuit is the dynamic power. One of the most widely employed technologies in the VLSI shape fabrication is PTL expertise, which is now used to form integrated circuits in a broad variety of applications. For designing of PTL circuit there are many tools and software which provides the best simulation results. This is the standard semiconductor technology for microprocessors, microcontrollers, memories such as RAM, ROM, EEPROM, and application-specific integrated circuits (ASICs). In PTL technology, we directly implement our circuit through either PMOS or NMOS or sometimes both. This characteristic allows for the design of logical actions using only basic switches without the need for an interruptible up-resistor. The only disadvantage of PTL is that we don't get rail to rail output but in the implementation of this circuit we have used body bias in such a way that we can get rail to rail output. [15]

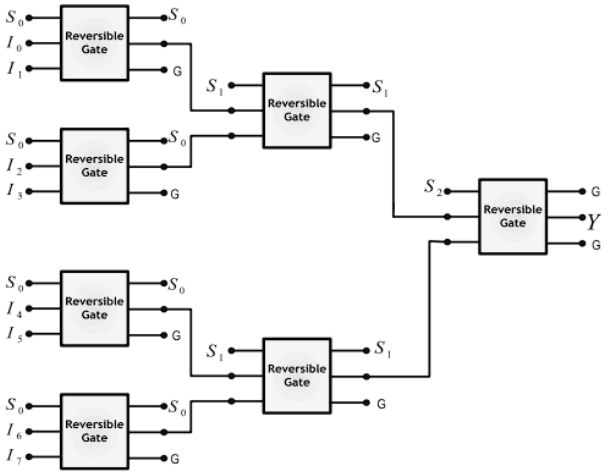

FIGURE 4: DESIGN REPRESENTATION OF 8:1 REVERSIBLE MULTIPLEXER BY USING FREDKIN GATES.

One network is turned on and the other is turned off depending on the input pattern. SIMULATION imitates the operation of an electrical device or circuit using mathematical models. Simulation software is a crucial analytical tool that enables modelling of circuit operation. Simulating a circuit's behaviour before constructing it may greatly improve design efficiency by spotting mistakes and illuminating the behaviour of electrical circuit designs. In instance, breadboards are not practicable for integrated circuits, photomasks are expensive, and it is extremely difficult to predict the behaviour of internal signals.

Hence, almost all IC design relies broadly on simulation. Simulation process results in test and verify the schematic circuit and accordingly the output waveforms are generated. If the output results and waveform are not matching with the desired output then the modification is needed in the required design and accordingly again the process continue till, we get the actual output. The moment we got the desired output it will end the process and hence the layout is obtained by the waveform. Hence in this way the loop will be continue till we got the desired output.

VI. SOFTWARES USED

LTSpice

The LTSpice application serves as both a simulator and an assessor of purposefulness. The limbic system's functionality is assessed using LTSpice before the microelectronic design is finalized. Designing and assessing complement logic structures is made possible by LTSpice's user-friendly environment for hierarchical logic design and simulation utilising delay arithmetic.

VII. PROBLEM IDENTIFICATION

Low power is a concern. Analysis and optimization are the two main categories into which VLSI design may be generally divided. The proper assessment of power or energy dissipation during the various circuit-design phases is what analysis is concerned with. The accuracy and effectiveness of different analysis methodologies varies. The information that was used to create a certain design affects how accurate the analysis is. Given an optimization aim, optimization is the process of developing the optimum design while adhering to design criteria. the transistor's off-state current. Assume that there are N transistors in the circuit, and that Ioff represents the ith transistor's off-state current. The circuit's overall leakage power may then be calculated using the following formula: [16]

$$P\ Leakage = VDD \sum_{i=1,N} Ioff$$

Leakage power consumption is a crucial design restriction for low power portable devices with nanoscale size CMOS technology. Recent developments in wireless communications technology have demonstrated the fusion of networks and terminals that offer real-time and multimedia applications. Obviously, this puts a tremendous amount of strain on any device's battery. Several strategies have been used to address the issue, and many more are constantly being developed. As a result, the designers must choose a specific approach based on the application and product needs.

Because power consumption is absorbing a lot of attention in the design of VLSI chips nowadays, building low power systems has become one of the key topics of the electronic industries. A vital primary problem of VLSI technology is the design of low power circuits for high performances. This project shows how to create an 8:1 MUX using a Fradkin gate and traditional PTL drawings. The circuit's power consumption will be further decreased by using fewer transistors.

VIII. Delay Calculation

The circuit delay is the longest total amount of time required for any output to be derived from an input with the greatest frequency. It directly affects the circuit's speed, so this parameter is calculated using a standard simulation time of 150 ns. The power dissipated across MOSFETs also rises with the frequency. By altering the substrate bias dc voltage supply, the fluctuation in delay with the change in threshold voltage can be studied. [17]

IX. Power Delay Product

Speed and the normal power waste are typically trade-offs. Thus, rather than comparing the metrics separately, the Power-Latency Product, which is the result of the circuit's power dissipation and delay, provides us a better picture of the circuit efficiency. It stands for the typical energy lost during a single switching event. As can be predicted from the results, for higher level circuits, the power delay product will be minimal for shorter channel lengths. [18]

X. Result

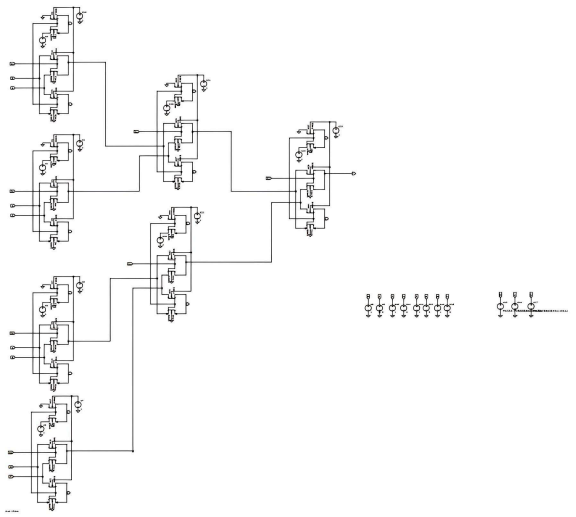

Fig.5 Schematic of 8:1Multiplexer

This circuit helps in making transmission circuit economical and less complex, simplifies logic design, reduces no. of wires that's why dealing with multiplexers is quite easy and useful. In this circuit first Fradkin Gate is implemented using PTL then after arranging all Fradkin Gate in such a way that it forms 8:1 MUX. Also, the output waveform snap is included which justifies that it is a Multiplexer.

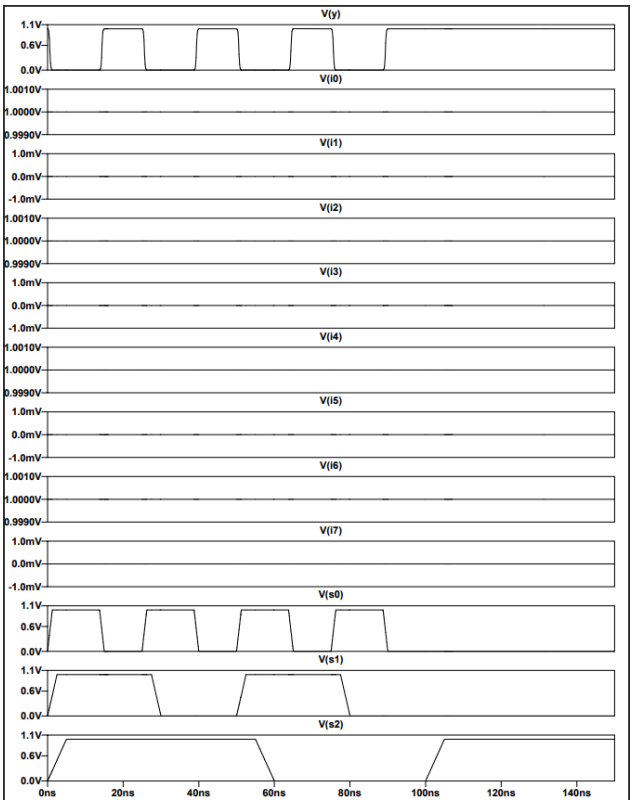

Fig.6 Output Waveform of 8:1Multiplexer

Table 2. Comparison Table (comparison with static CMOS 2:1 MUX)

Digital Circuit	Technology	Supply Voltage	No. of Tx(s)	Average Power	Power Delay Product	Type Of Design
2:1 MUX (Ref 14)	120nm static CMOS	1	12	53 uW	7.22 E-15	Classic
8:1 MUX	90nm PTL		42	22.45 uW	5.47 E-14	Using Fradkin Gate PTL

Table 3. Power Consumption Table.

Channel Length, (L)	Element	Delay (Seconds)	Power Dissipation	Power Delay Product (PDP)
180nm	Fredkin Gate	4.79E-11	78.3 uW	3.75 E-15
	8:1MUX	1.99E-10	1.97 mW	3.92 E-13
90nm	Fredkin Gate	1.75E-10	22.45 uW	3.92 E-15
	8:1MUX	3.29E-10	166.4 uW	5.47 E-14

XI. Conclusion

Different literary styles of multiple authors have been examined and compared in this report. We looked at several multiplication factor designs using complementary metal-oxide semiconductors (CMOS linear) and performance evaluation. The mux function is quite beneficial and has many uses.

The multiplexer structures are realized using PTL gate-based logic styles. The delay, supply voltage, power consumption and the number of transistors present in the design are tabulated and compared.

We have also used Fredkin Gate for more power reduction and making our design more efficient. The Fredkin gate is a circuit or device having three inputs and three outputs that, if and only if, the first bit is a 1, sends the first bit unmodified and switches the following two bits.

Reduced number of transistors results in energy savings. The findings also demonstrate that, when compared to previous technology this one has the lowest power dissipation across all circuits. The use of Fradkin Gate reduces the power to a significant amount. Also, when Fradkin Gate is implemented used PTL it again decreases the power and delay due to a smaller number of transistors.

XII. Future Scope

Further efforts can be given for increasing the more input lines and more selection lines. To achieve high efficiency of the switching between the input lines.

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