

Assignment - 1

Ques 1

$$\text{Clock signal} = 2 \text{ MHz} = 0.5 \times 10^{-6} \text{ sec}$$

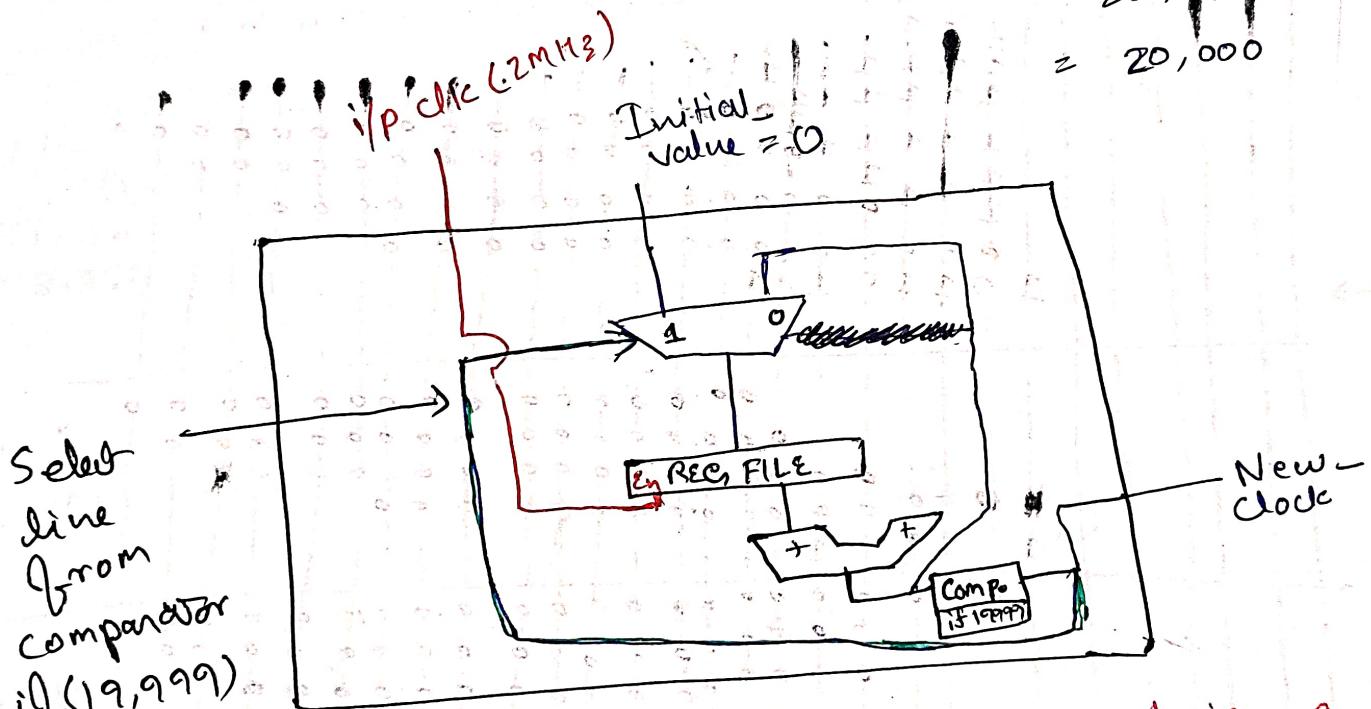
~~Required clock period = 10ms~~

$$\text{Required clock} = 10 \text{ ms} = 10 \times 10^{-3} \text{ sec}$$

pulse.

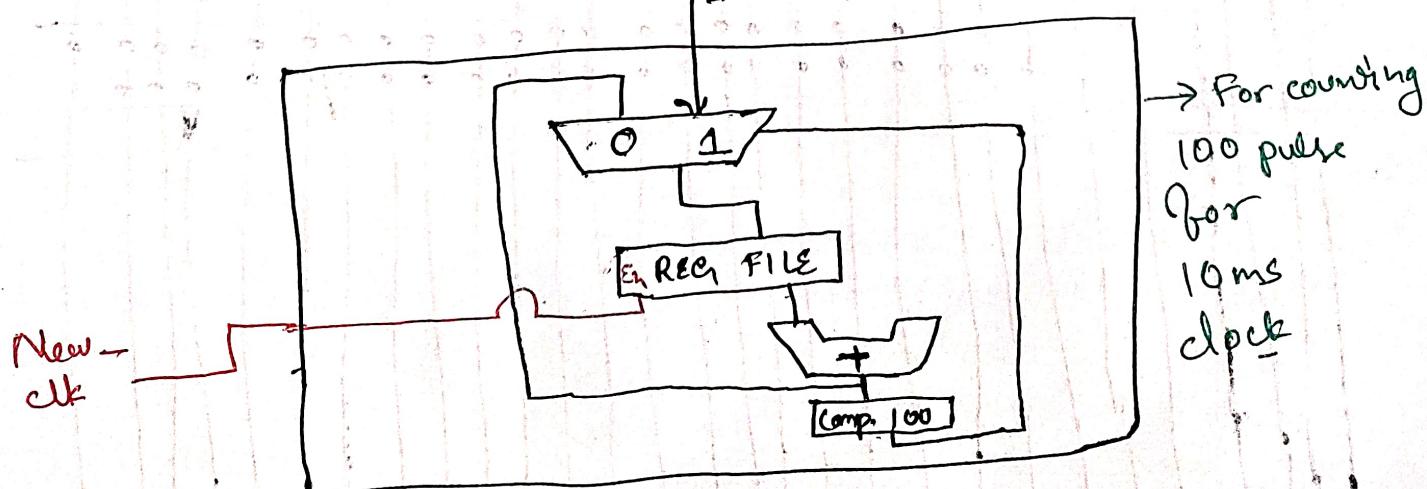
Counter / clock divider for required time period

$$\begin{aligned}
 &= \frac{20}{10 \times 10^{-3}} \\
 &= \frac{20}{0.5 \times 10^{-6}} \\
 &= 20 \times 10^3 \\
 &= 20 \times 10^3 \\
 &= 20,000
 \end{aligned}$$



* This new_clock we have to design a counter which counts 100 pulses

Initial value = 0



* For comparator design we can do AND operation with i/p(s) and with an XNOR gate.

Ques 2 (Add last)

Ques 3 Given numbers in format

Suppose

$$x_1 = Q_{2.14}$$

$$x_2 = Q_{3.13}$$

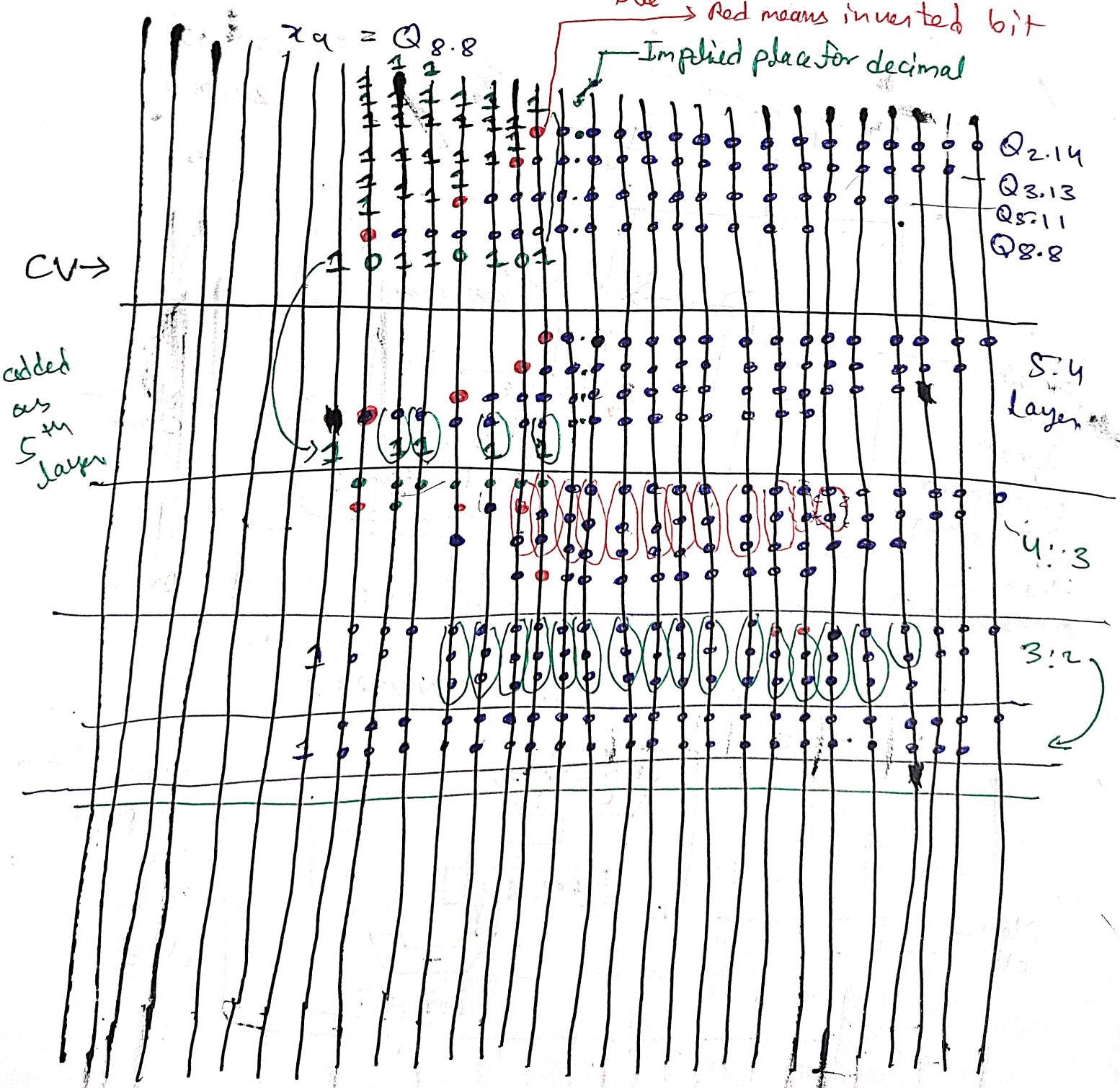
$$x_3 = Q_{5.11}$$

$$x_4 = Q_{8.8}$$

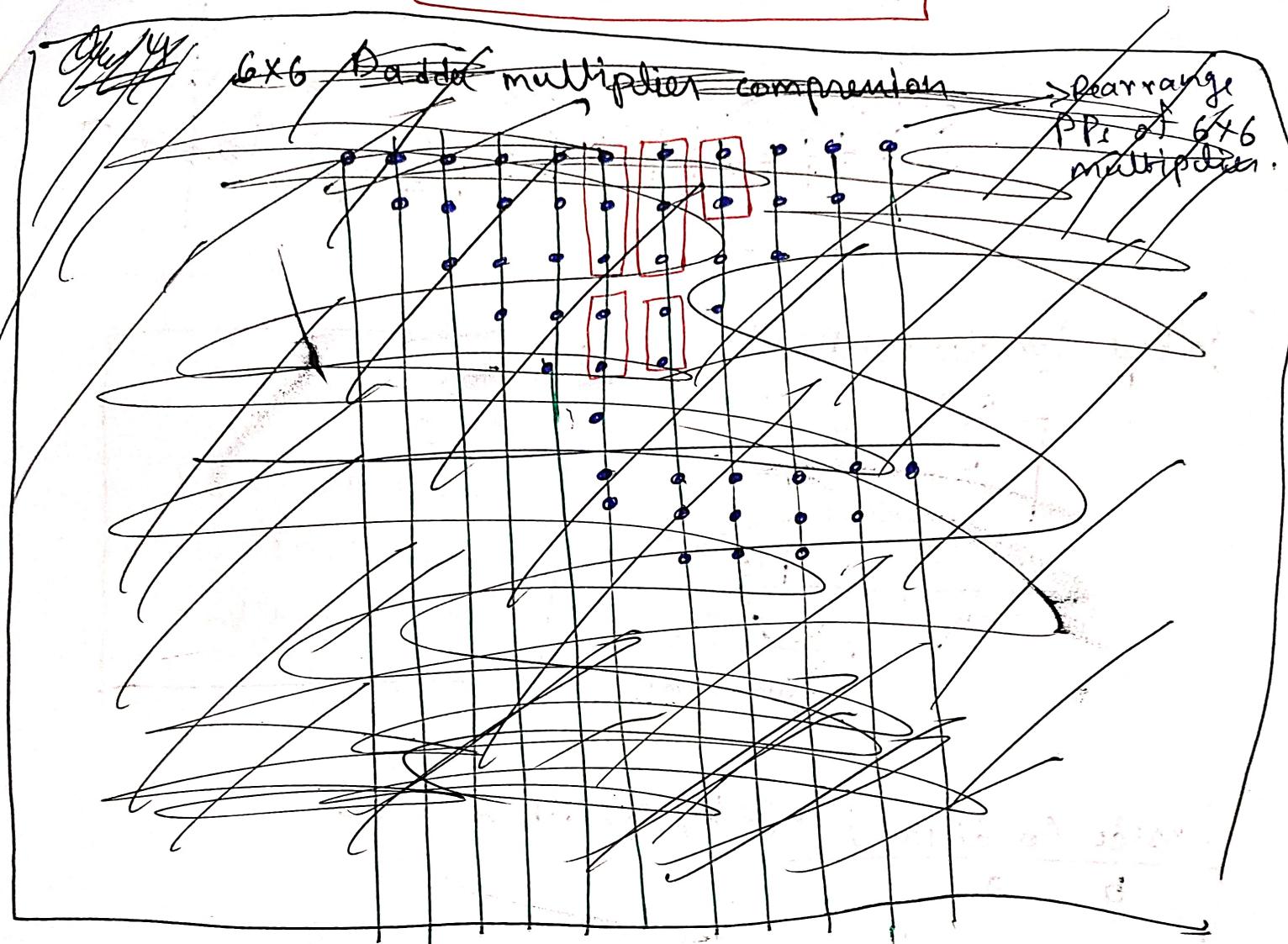
* Here we can use multi-operand comparison tree

Red means inverted bit

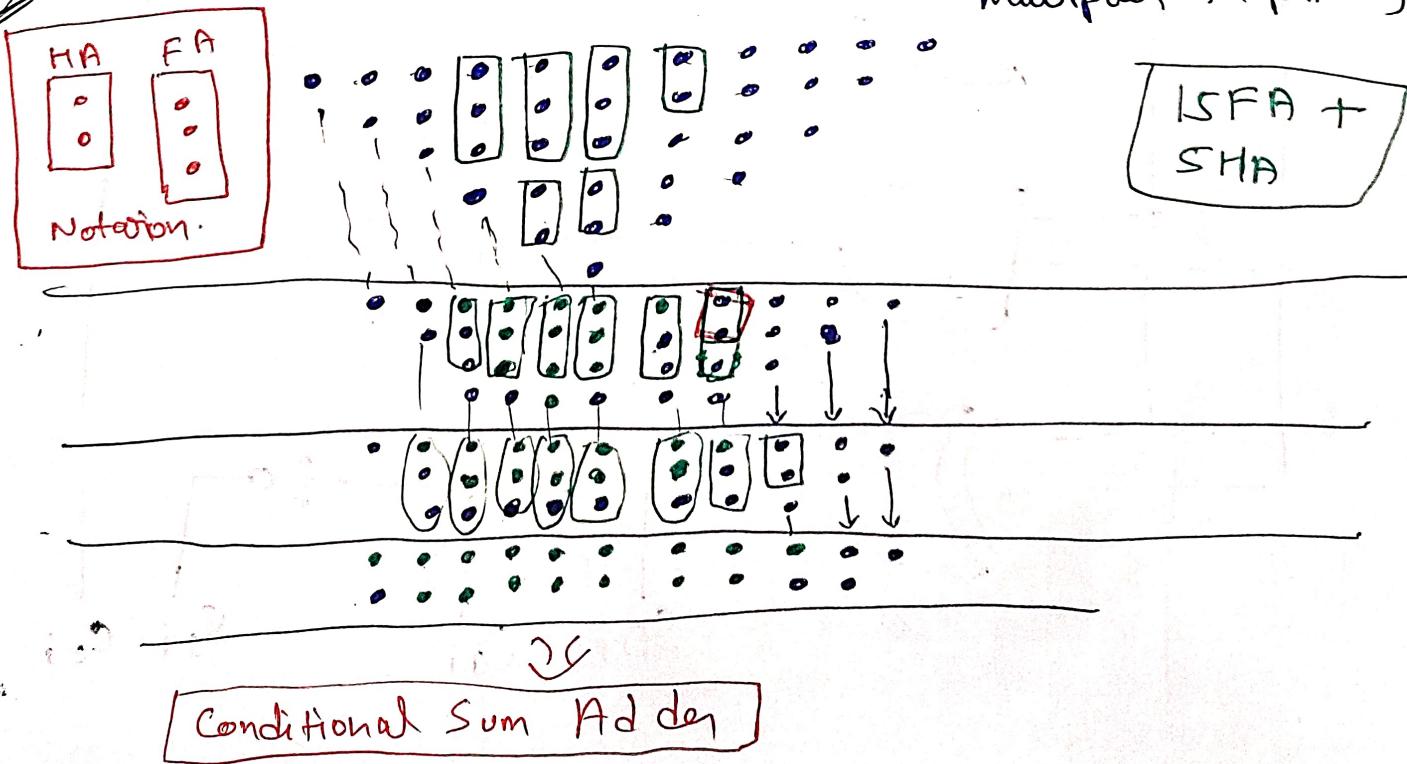
Implied place for decimal



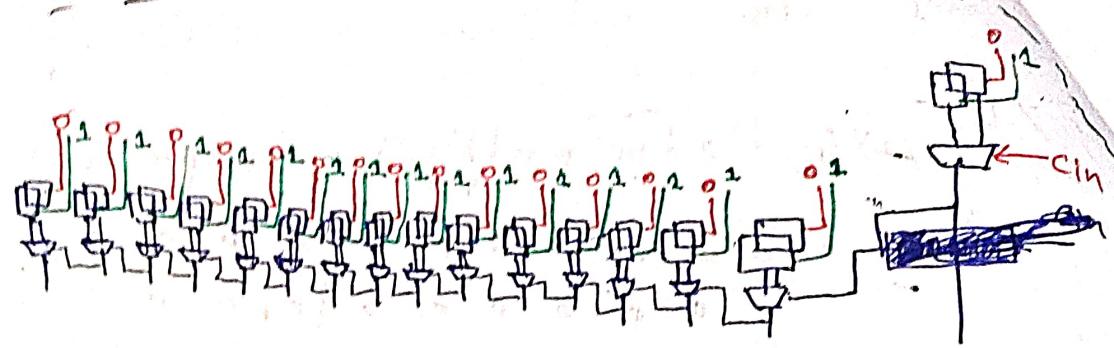
* After comprehension of operand we can simply use ~~can~~ Conditional Sum Adder.



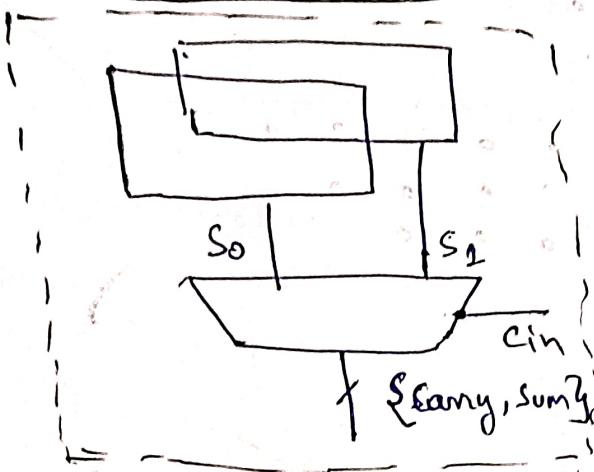
(a) 6x6 dadda multiplier comprehension (Rearrange PPs of 6x6 multiplier in prism)



Ques 4 (b) 16-bit conditional Sum Adder.

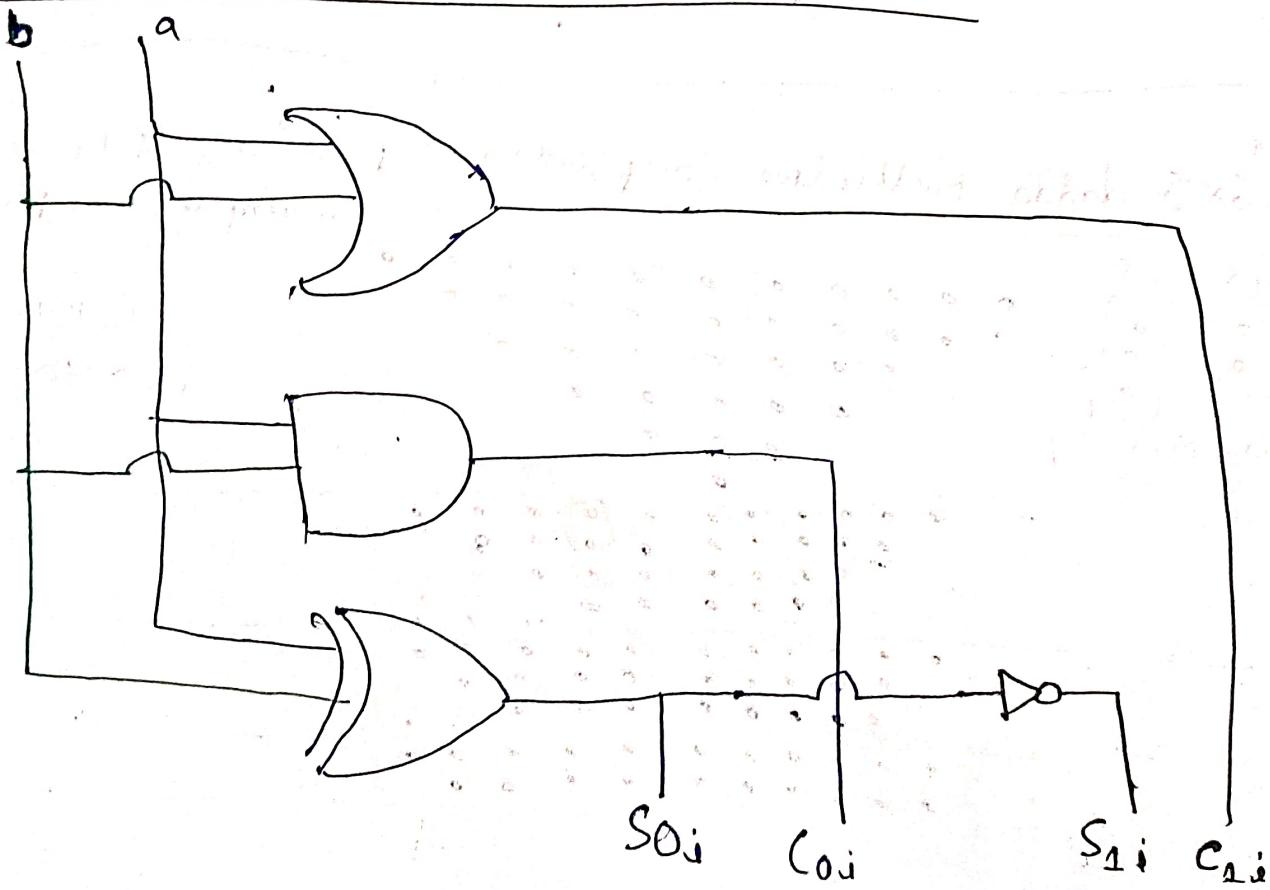


Where Conditional Block



* Here
 $S0i = a_i \oplus b_i$
 $S1i = a_i \wedge b_i$
 $C0i = a_i b_i$
 $C1i = a_i' + b_i$

Inside Conditional Block / Conditional Cell



Ques 4 part 2 (At last of PDF)

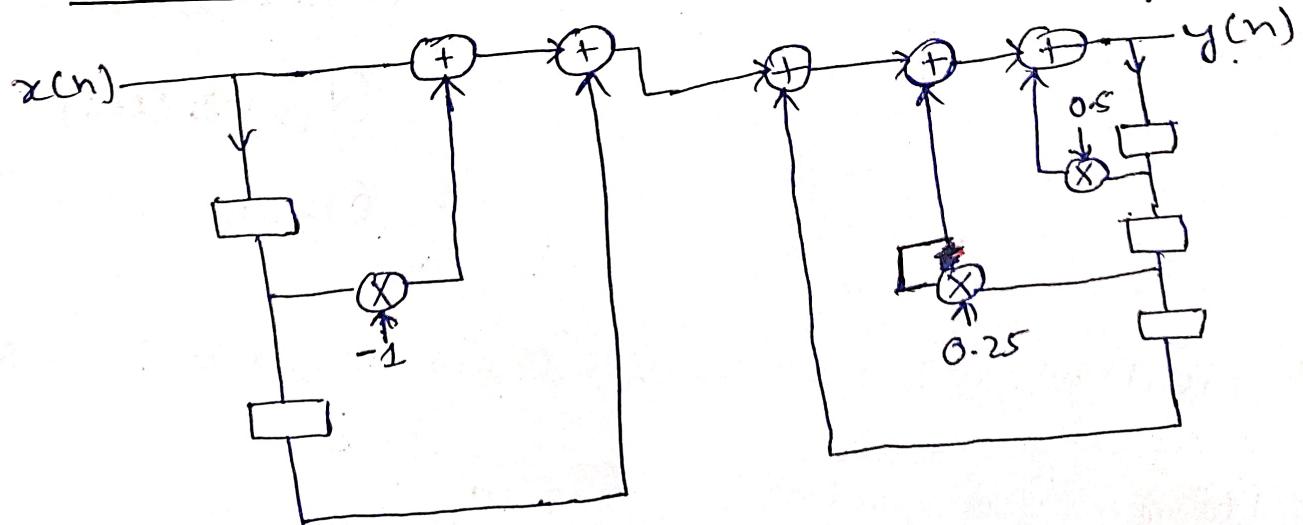
$$\text{Ques 5} \quad A = 1001 - 1101$$

$$B = 1101 - 1011$$

$a_i \rightarrow$	1 0 0 1 1 1 0 1
$b_d \rightarrow$	1 1 0 1 1 0 1 1
Group width is 1	0 1 0 0 0 1 1 0 1 0 0 1 1 0 0 1 1 0 1 1 1 0 0 1 1 1 0 1 1 1 1 1
Group width is Two	0 1 1 0 0 1 0 0 1 0 0 1 1 0 1 1 1 0 1 1 1 0 0 0 1 0 1 1 1 0 1 1
Group width is 4	0 1 1 0 1 0 0 0 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0
Final Answer.	$0 1 1 1 - 1 0 0 0$ <hr/> CSA Final Sum

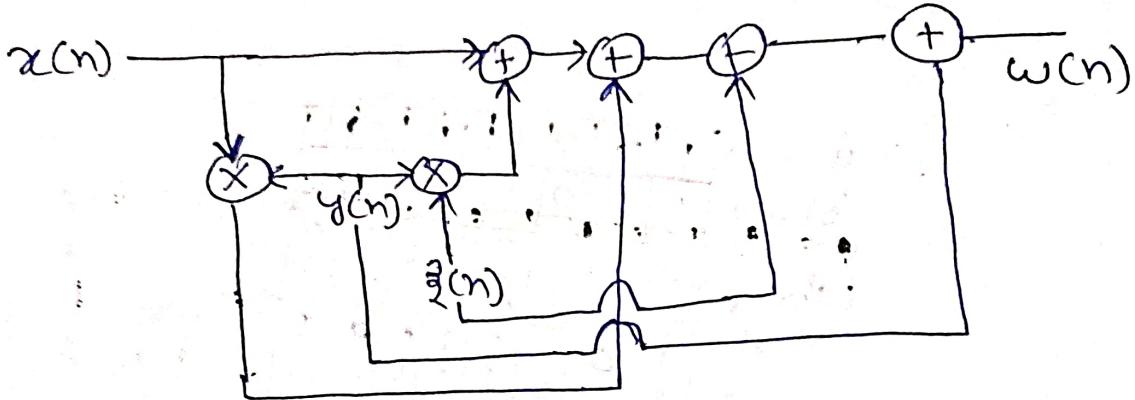
Since given no. has i/p zero as carry.

$$\text{Ques 6} \quad \text{Architecture!} - y(n) = x(n) - x(n-1) + x(n-2) + y(n-3) + 0.5y(n-1) + 0.25y(n-2)$$



* Verilog code is at the last of PDF

$$\text{Q7} \quad w(n) = x(n) \cdot y(n) + y(n) \cdot z(n) + x(n) + y(n) + \varepsilon(n)$$



For $x(n) \cdot y(n)$ Equivalent $Q_{m,n} = Q_{1,7} * Q_{2,6}$
 (Signed \times Signed)

$$\begin{aligned}
 &= Q_{(m_1+1)} \cdot (m_1+n_2+1) \\
 &= Q_{(1+2-1)} \cdot (7+6+1) \\
 &= Q_{2,14} \text{ (Resultant form)}
 \end{aligned}$$

For $y(n) \cdot z(n)$ Equivalent $Q_{m,n} = Q_{2,6} * Q_{0,8}$
 (Signed \times Unsigned)

$$\begin{aligned}
 &= Q_{(m_1+m_2)} \cdot (n_1+n_2) \\
 &= Q_{(2+0)} \cdot (8+6) \\
 &= Q_{2,14}
 \end{aligned}$$

* resultant $w(n) = Q_{2,14} + Q_{2,14} + Q_{1,7} + Q_{2,6} + Q_{0,8}$

* Hence $Q_{m,n}$ of $w(n)$ = $Q_{2,14}$

Rohit Sir - 7

$$C(n) = Q_2 \cdot 14 + Q_2 \cdot 14 + Q_0 \cdot 8 + Q_1 \cdot 7 + Q_2 \cdot 6$$

Designing Comprehension tree

