Lab 6: Series/Parallel MOS Networks and MOS Current Dividers

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Experiment 1: Transistor Matching

In this experiment, we measured the channel current as a function of gate voltage for nMOS transistors. We set the drain voltage to Vdd and the source voltage to ground.

Table 1.1

Name	Is	Kappa	VT0
Transistor 1	2.005e-6	.6545	.6766
Transistor 2	1.888e-6	.6556	.6758
Transistor 3	1.896e-6	.6566	.6763
Transistor 4	1.968e6	.6576	.6740

As shown in table 1.1, we used the EKV model to extract the saturation current, the threshold voltage, and the divider ratio. From this, we were able to find the theoretical fits for channel current as a function of gate voltage. This can be represented by the following equation.

$$I_{sat} = I_s \cdot log^2(1 + e^{\kappa \cdot \frac{V_G - V_{T0} - V_S}{2 \cdot U_T}})$$

Using this equation and the values we found using ekvfit, we were able to plot the four nMOS theoretical fits for the current-voltage characteristics.

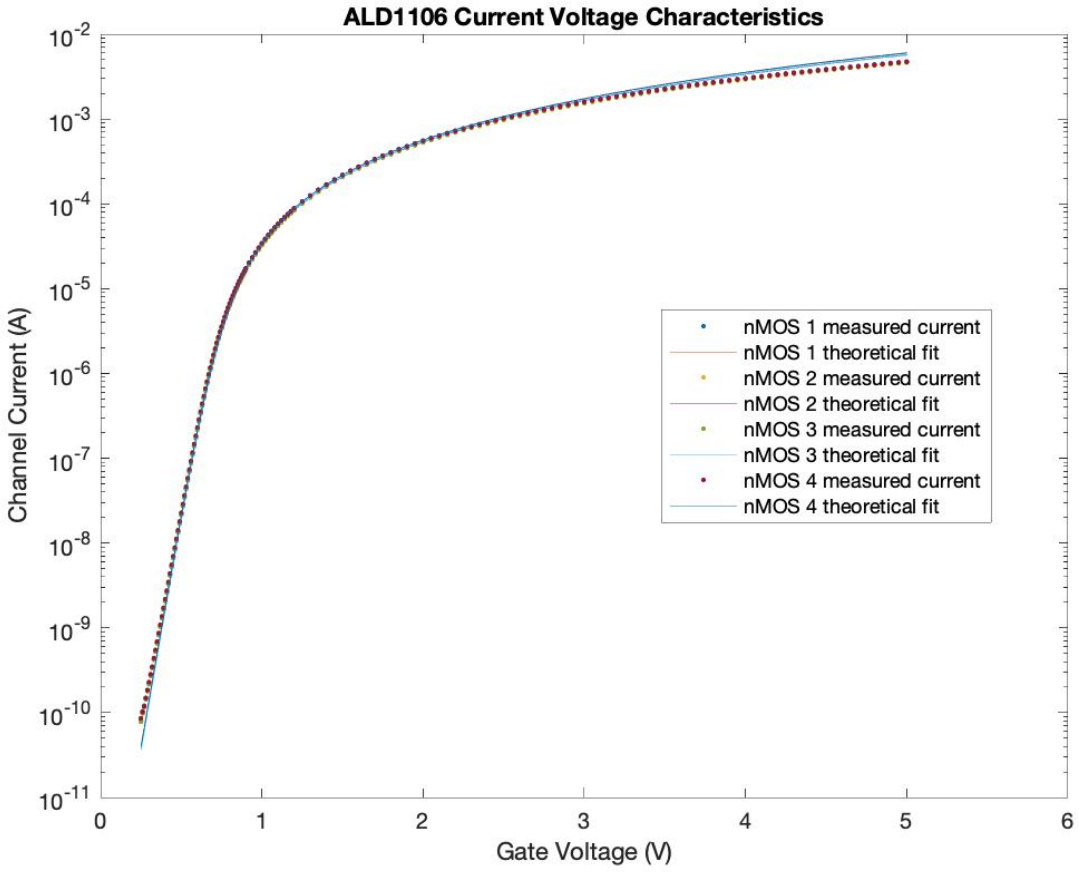

Figure 1: Semilog plot showing the I-V characteristic for the four transistors tested.

Then, we plotted by what percent the channel current deviated from the collective mean as a function of the mean value of the four channel currents.

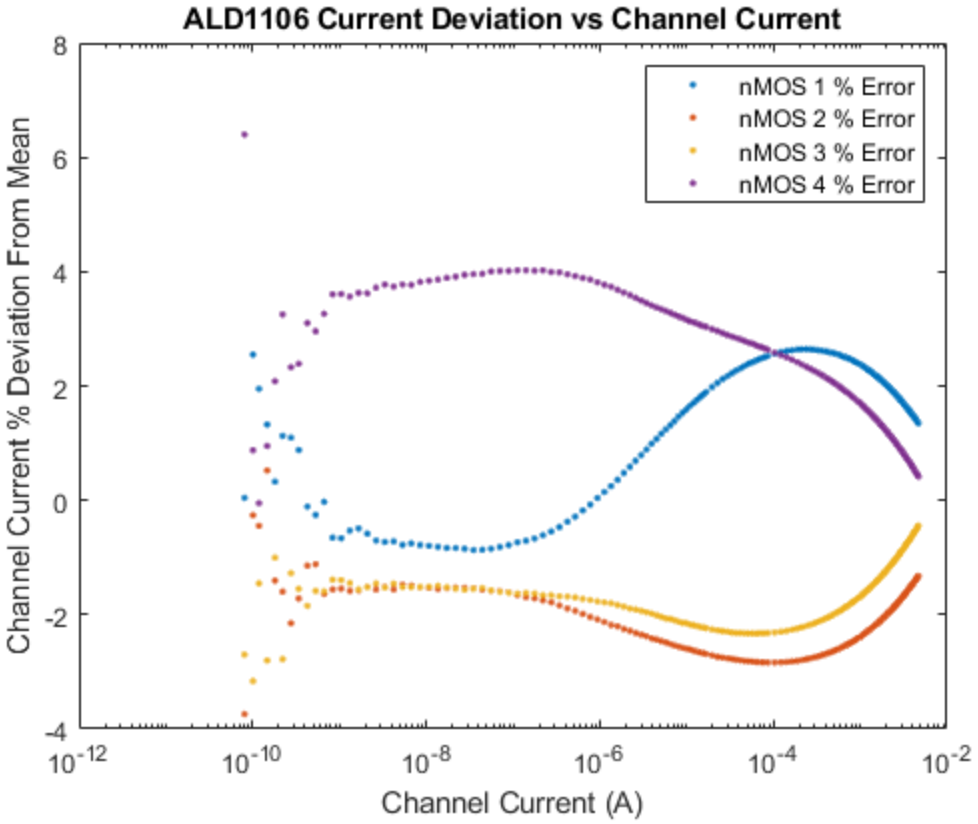

Figure 2: Semilog plot showing the percentage differences between the channel current and the mean value of all of the transistor's channel currents.

As you can see in figure 2, the percent deviation of the channel current from the collective mean seems to vary quite a bit. The error seems to lie mainly in the ±4% range. In addition, we can see that as the channel current increases, it seems to all approach 0%. This means that the closer the channel current gets to the saturation current, the lower the error is. Lastly, looking at figure 2 again, it seems that transistor 1 and 4 seem to match each other closely while transistor 2 and 3 follow similar patterns.AL

Experiment 2: MOS Transistors in Series and Parallel

In this experiment, we measured channel current as a function of the gate voltage for two cases of Vds: 10 mV and Vdd. After this, we connected a matched pair of nMOS transistors in parallel with each other and measured the channel current as a function of gate voltage for the same two cases of Vds. Lastly, we connected the same matched pairs of nMOS transistors in series with each other and measured the channel current as a function of gate voltage for the same two cases of Vds.

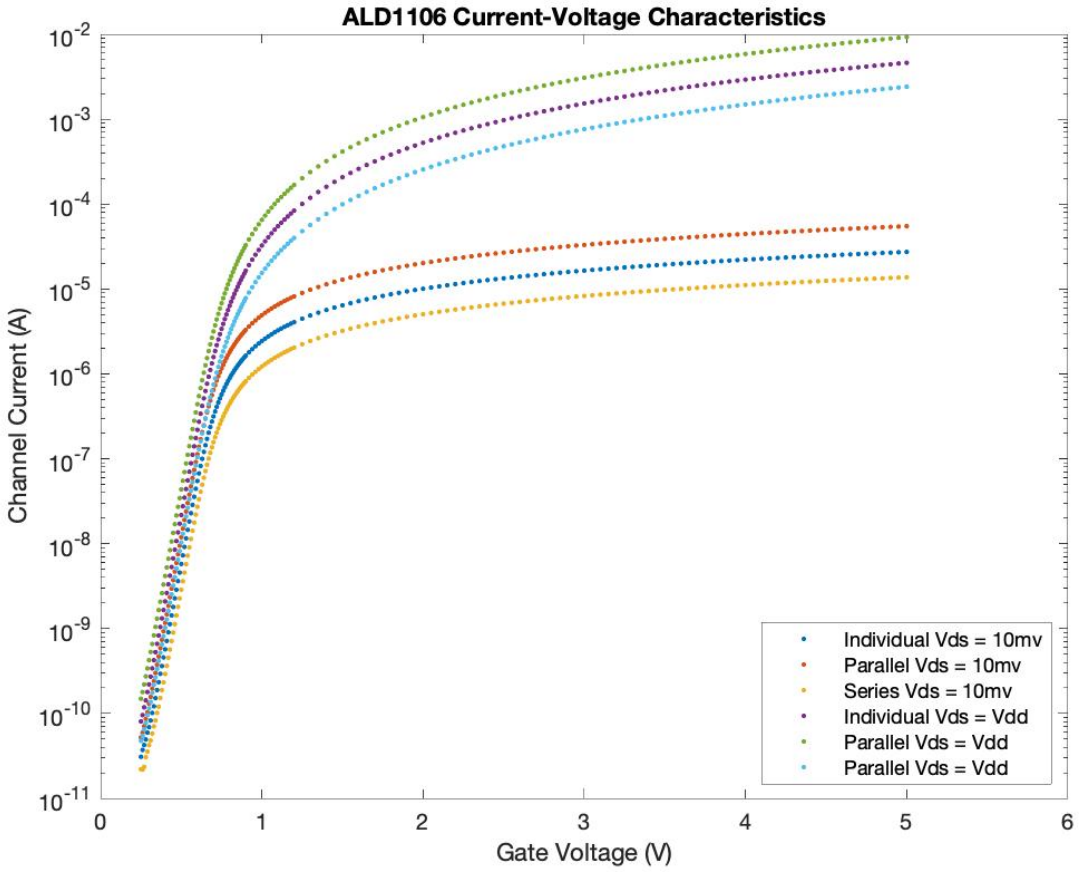

Figure 3: Channel current as a function of gate voltage for the three arrangements of MOS transistors at a 10 mV Vds and a 5 mV Vds.

The channel current for the parallel nMOS transistors should be double that in the individual transistor. The channel current for the series nMOS transistors should be half that of the individual transistor. Looking at figure 3, we can see just this. At lower gate voltage values, the ratio is smaller than what it should be, but at higher gate voltage values, the ratio stabilizes.

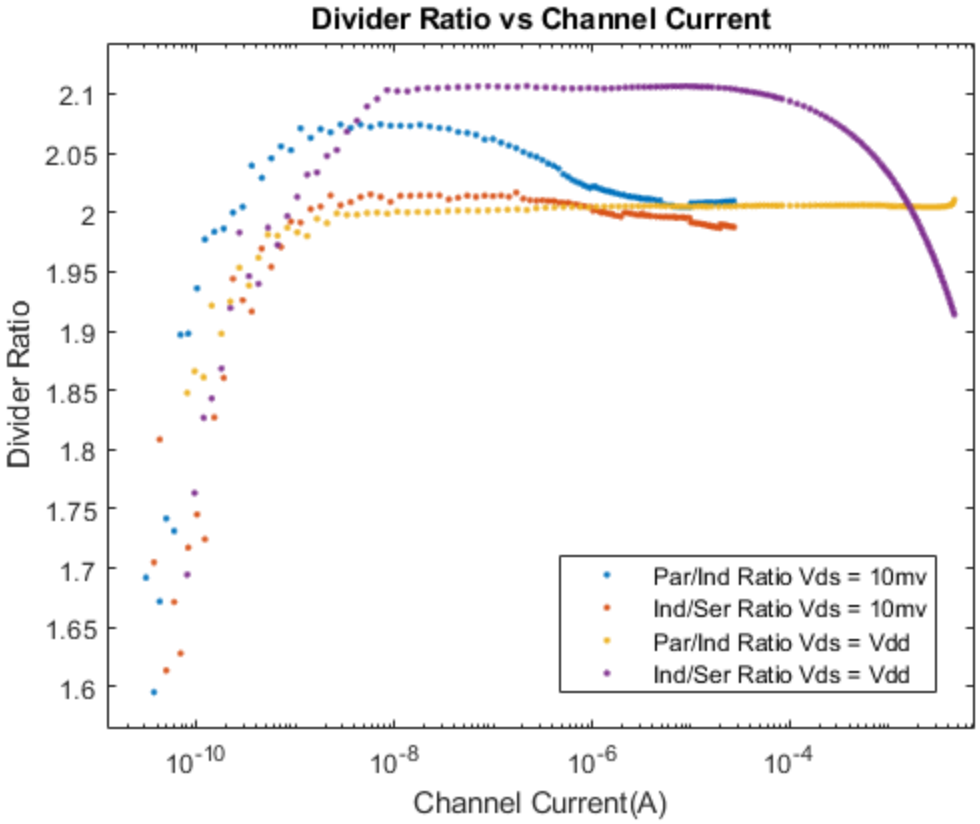

Figure 4: Ratio of measurements from the parallel and series connections with reference to the individual transistors.

In the ohmic region, the ratio is significantly smaller than what it should be and is increasing. in the saturation region, the ratio stabilizes to what it should be around. The one exception to this observation is that the ratio between the individual transistor to the series connection when Vds is Vdd, seems to stabilize at a slightly higher value than where it should be and drops off the greater the channel current gets.

The series/parallel equivalences work more accurately to how they should in the saturation region.

Experiment 3: MOS Current Dividers

In this experiment, we constructed a two-way current divider with a divider ratio of 0.5. We set the drain voltage high enough such that the transistor was in the saturation mode. This means that the input current is sunk at the source and the output current is taken at the drain. We measured the output current as a function of the input current.

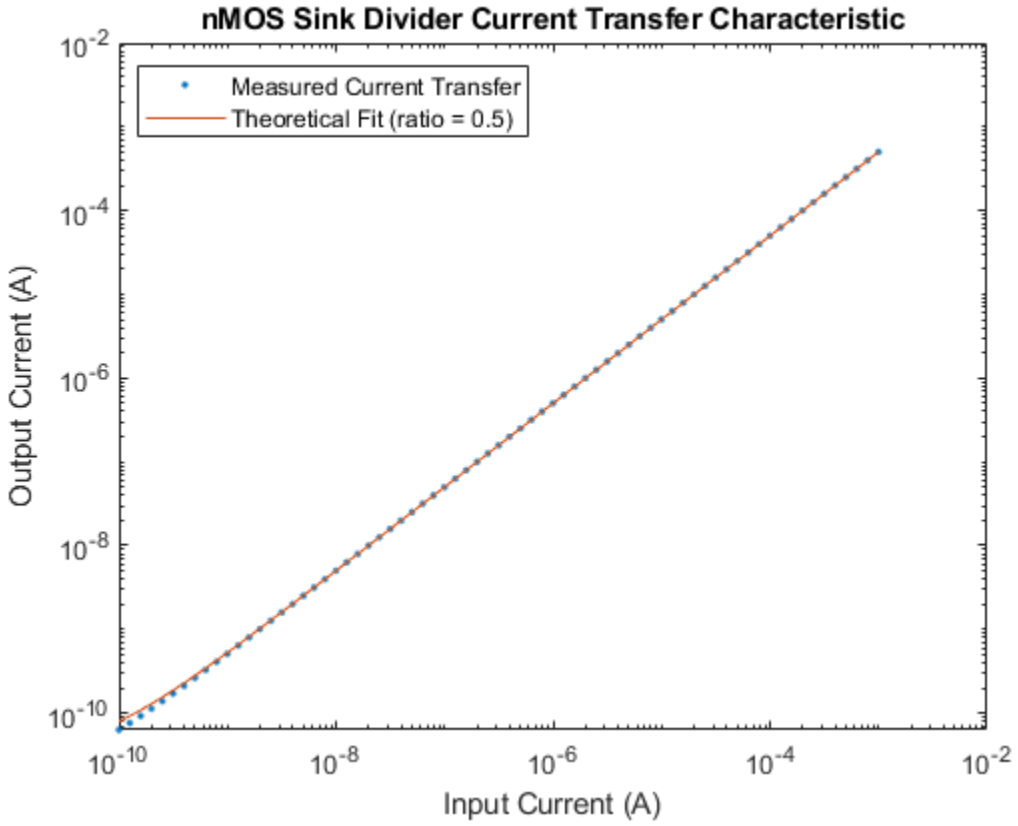

Figure 5: Output current as a function of the input current for an nMOS sink divider.

Looking at the figure 5, we can see that the actual divider ratio is exactly what it was intended to be. At really low currents, the divider ratio is slightly off. Very quickly, however, the intended and measured behavior matches perfectly. This could be due to the fact that we are using a circuit simulation software.

Next, we constructed another two-way current divider where the gate voltage was set to Vdd. In this current divider, the input current is sourced into the drain and the output current is taken at the source.

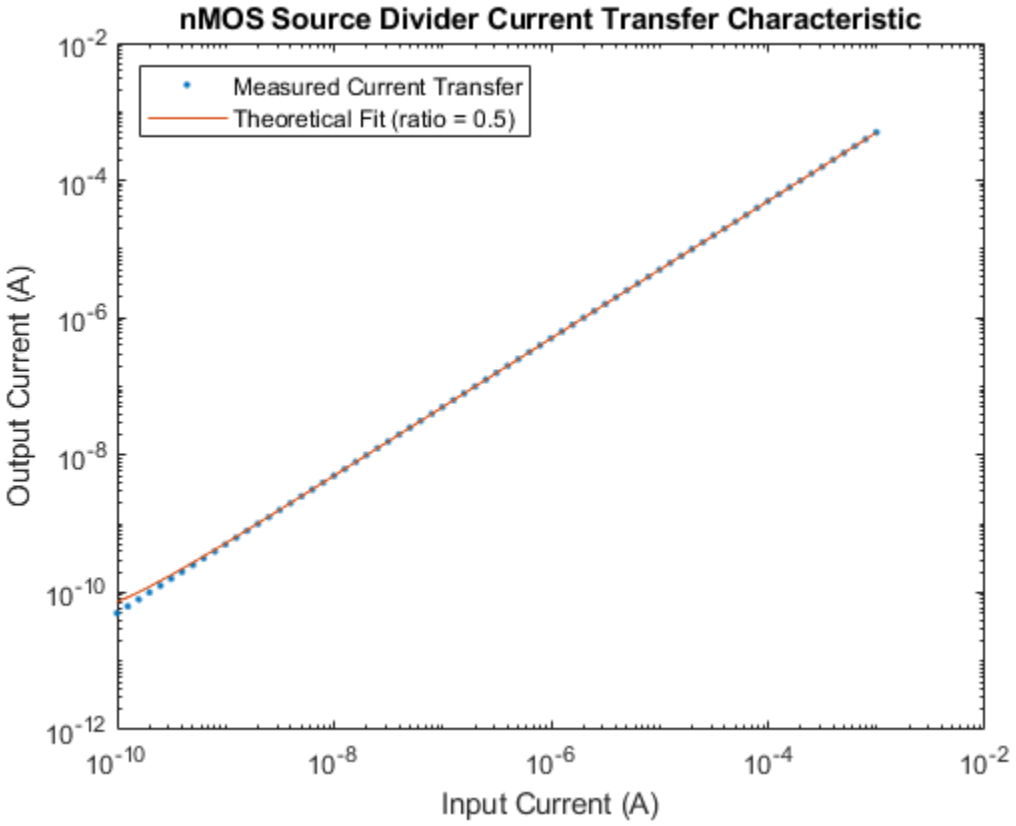

Figure 6: Output current as a function of input current for an nMOS source divider.

Looking at figure 6, we can see that the actual divider ratio is, again, exactly what it was intended to be. At really low currents, the divider ratio is slightly off, as seen in the last one. Again, very quickly the two lines match up. This high level of measurement accuracy is due to the fact that this is in simulation.