Lab 5: MOS Transistor Characteristics

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Experiment 1: Gate Characteristics

In this experiment, we measured the channel current as a function of gate voltage of a pMOS and nMOS transistor. We set the source voltage at ground and the drain voltage enough above ground such that the transistor is in saturation for the nMOS transistor. For the pMOS transistor, we measured channel current as a function of gate voltage with the source voltage at Vdd and the drain voltage enough below Vdd to make sure that the transistor is in saturation. We swept gat voltage values between 0V and 5V.

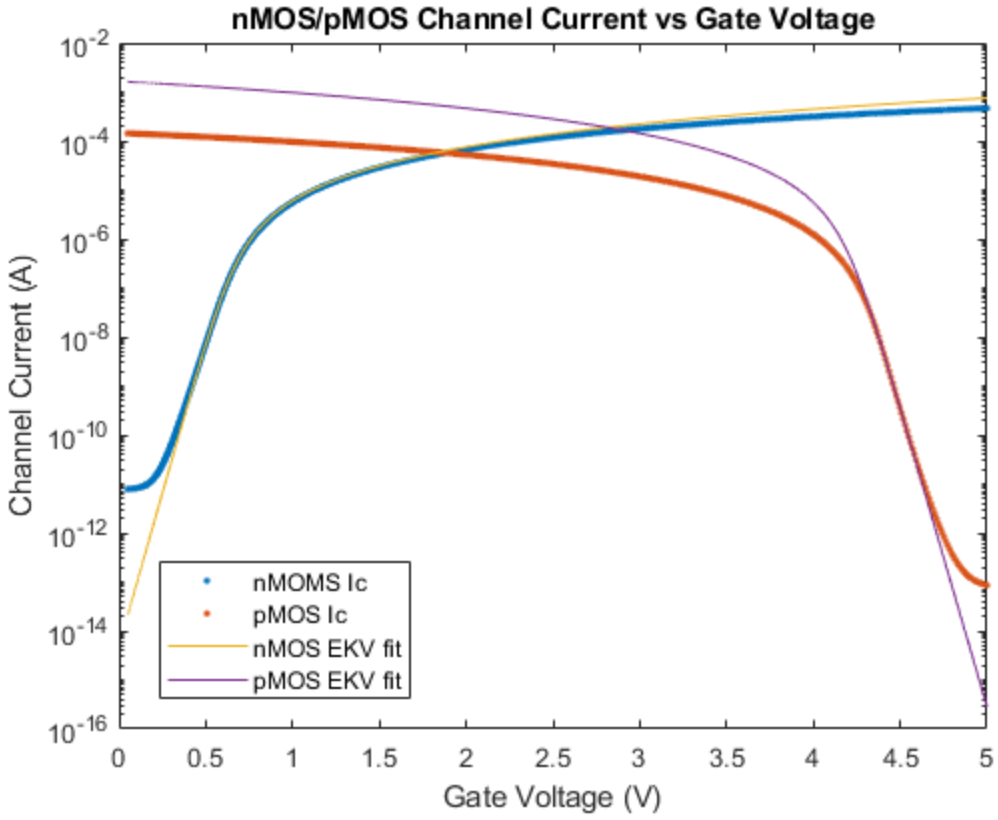

Figure 1: The channel current as a function of gate voltage for the nMOS and pMOS transistors.

In order to find the fits for the nMOS and pMOS transistors, we used the MATLAB's ekvfit function. The values given to us from the program for the nMOS transistor are that Is is 1.89e-7, kappa is .7411 and Vto is .6076. For the pMOS transistor, Is is 1.89e-7, kappa is -.7241, and Vto, is 4.2439.

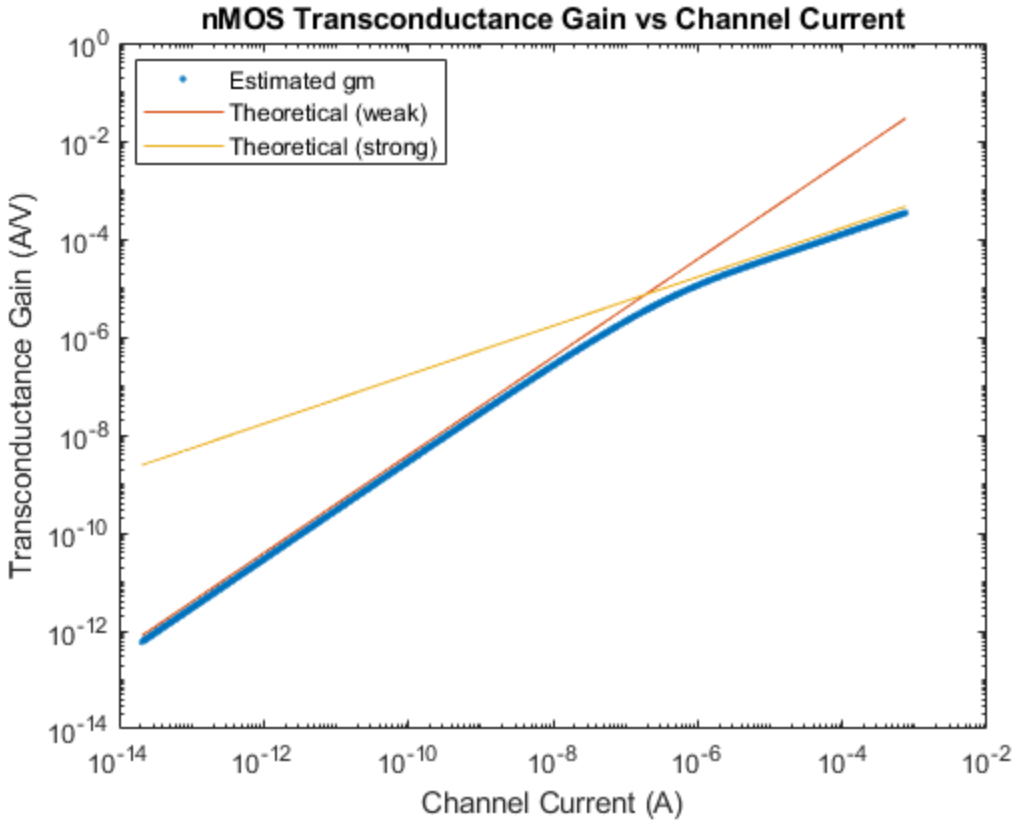

Figure 2: The transconductance gain as a function of the channel current with the theoretical weak and strong inversion transconductance gains for an nMOS transistor.

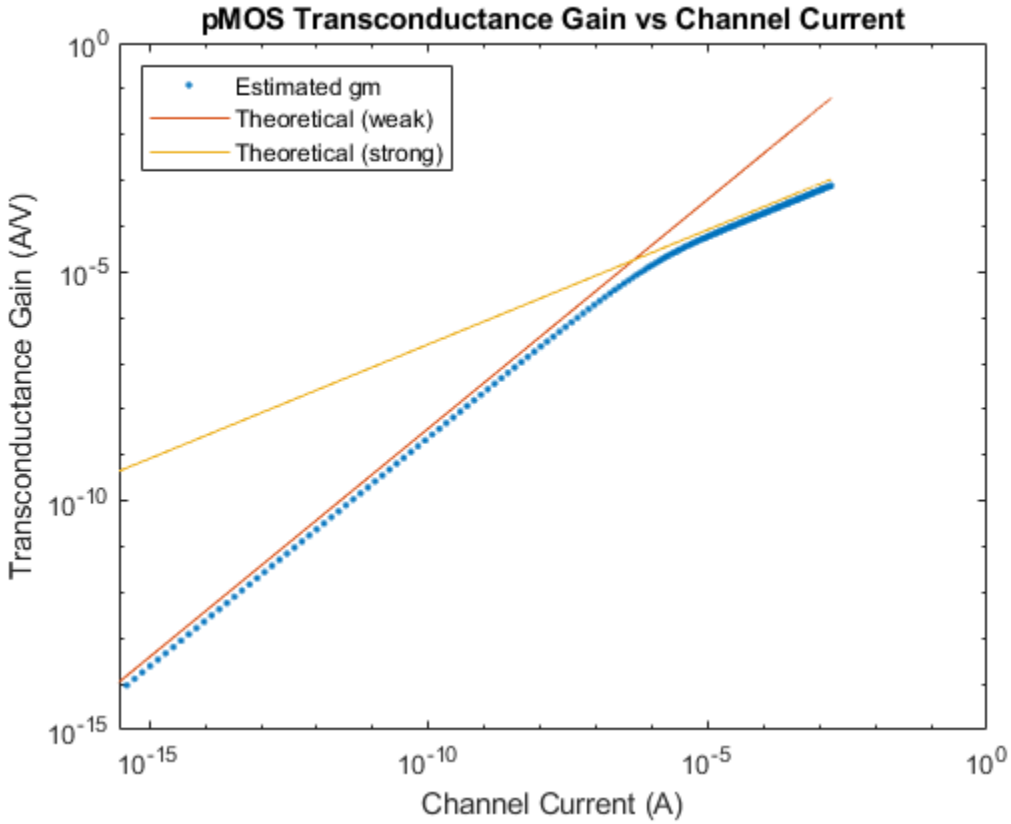

Figure 2: The transconductance gain as a function of the channel current with the theoretical weak and strong inversion transconductance gains for a pMOS transistor.

Note: The plots were very difficult to figure out what was going on if it was all in one log log plot, so we split it up.

We used the equations found in the EKV MOS Transistor Model Summary equations tables in order to find the weak and strong inversion transconductance gains fits. The equations are the same for the nMOS and pMOS transistors

$$weak: g_m = \kappa \cdot \frac{I_{sat}}{U_T}$$

$$strong: g_m = \kappa \cdot \frac{\sqrt{I_s \cdot I_{sat}}}{U_T}$$

From looking at the two graphs, it does seem like the theoretical fits match the weak and strong inversion regions of the graphs.

Experiment 2: Source Characteristics

In this experiment, we measured the channel current as a function of source voltage for both the nMOS and pMOS transistor. For the nMOS transistor, we set the gate and drain voltages to Vdd. For the pMOS transistor, we set the gate and drain voltages to ground.

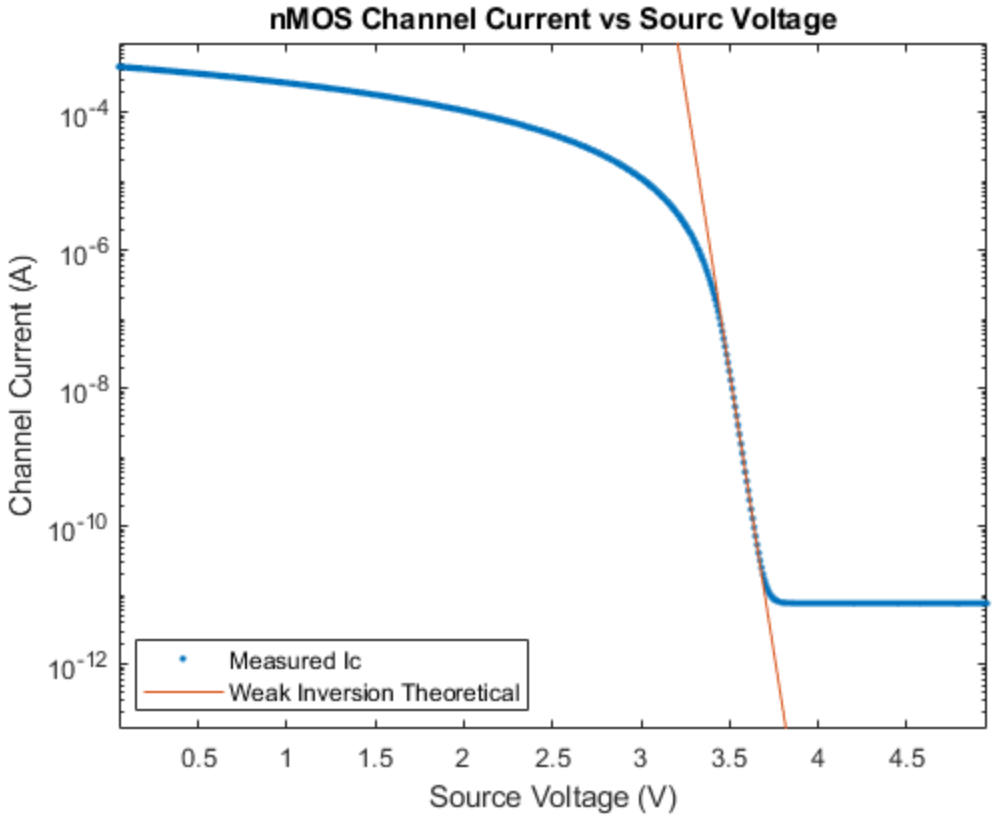

Figure 3: The channel current as a function of the source voltage for nMOS transistors.

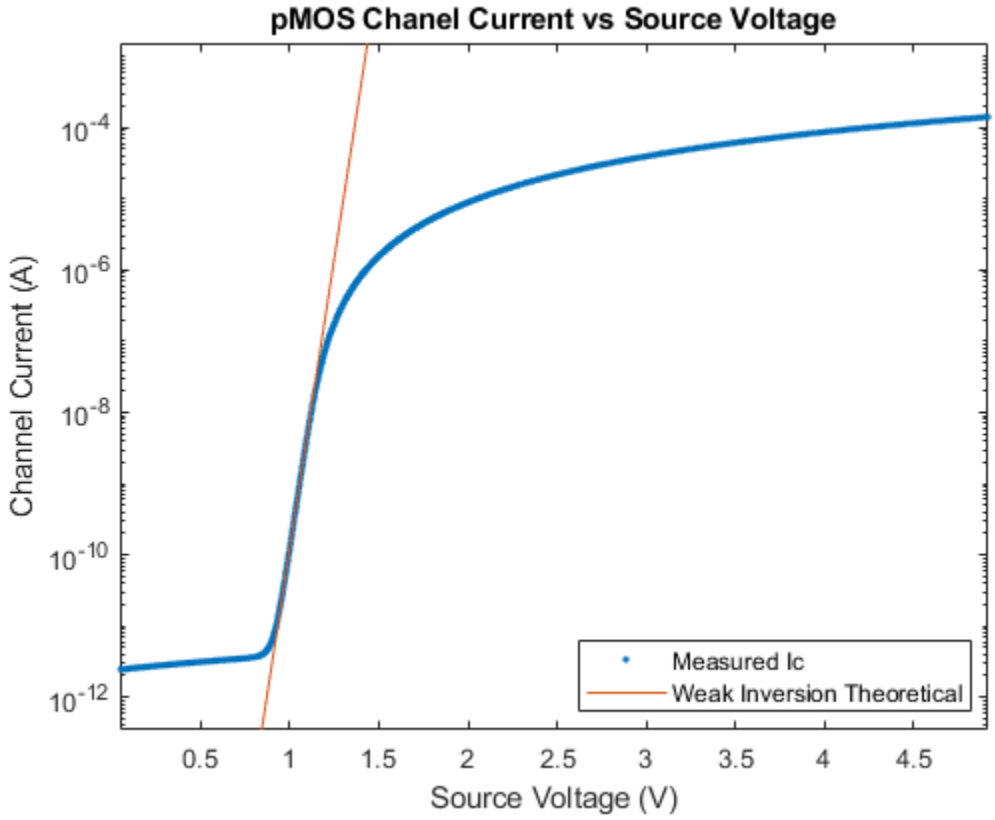

Figure 4: The channel current as a function of the source voltage for pMOS transistors.

The slope at the exponential region in the nMOS transistors is -37.39 A/V. The slope at the exponential region in the pMOS transistors is 37.42 A/V. In figure 1, we can see that the channel current increases as gate voltage increases for the nMOS transistor. This seems to be the opposite for the pMOS transistor. The source voltage follows the opposite pattern with channel current. These characteristics are the opposite from what is found in experiment 1.

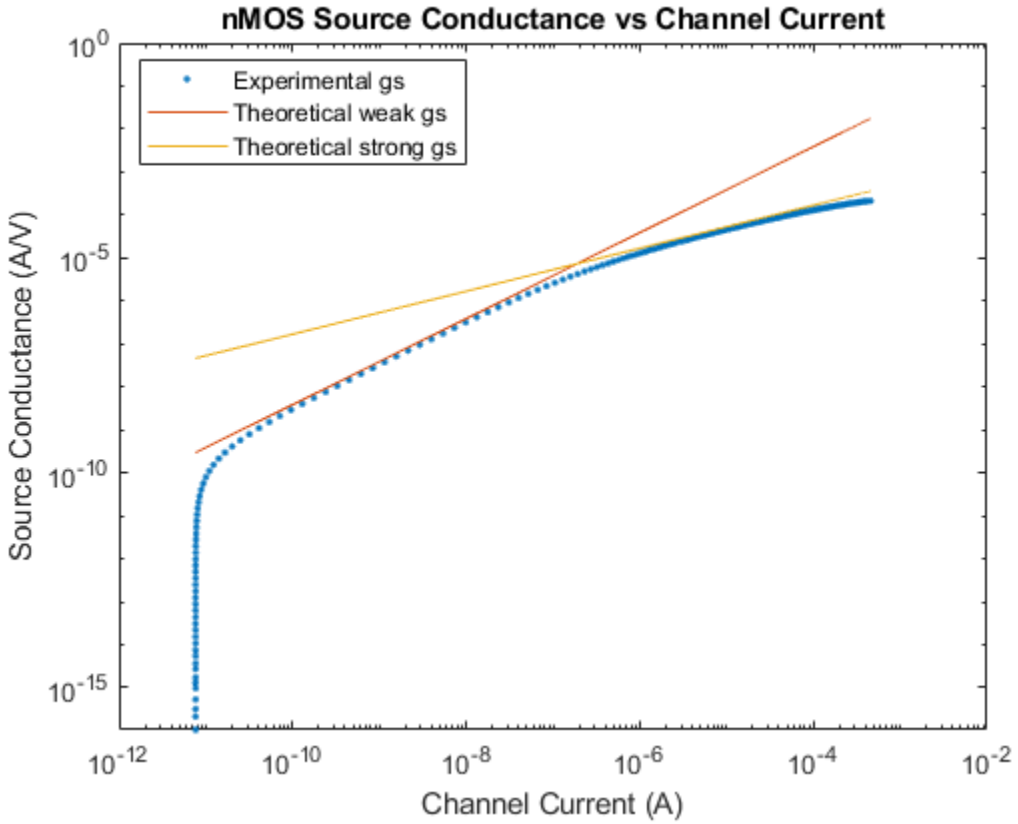

Figure 5: Incremental source conductance as as function of current flowing through the channel for an nMOS transistor.

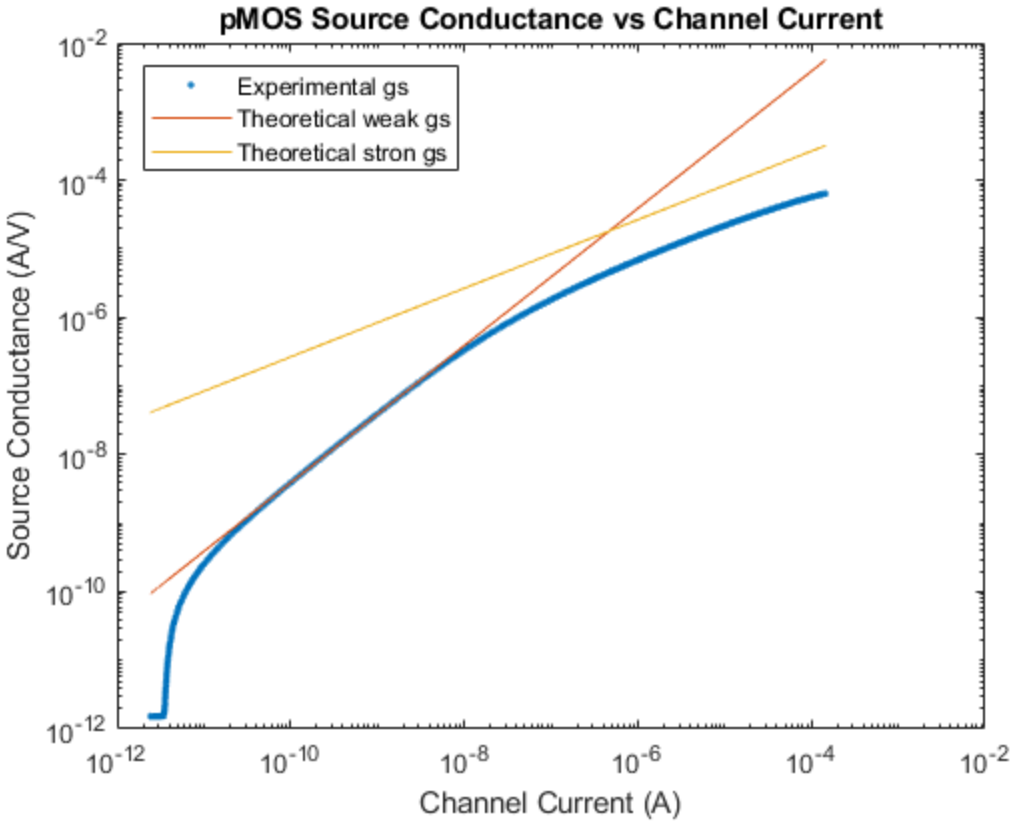

Figure 6: Incremental source conductance as as function of current flowing through the channel for an pMOS transistor.

For the nMOS transistor, the weak and strong source conductances fit well as seen in figure 5. In figure 6, we can see that the weak and strong source conductances fit well for the pMOS transistor.

Experiment 3: Drain Characteristics

In this experiment, we measured channel current as a function of drain voltage for three different gate voltage values. The first scenario was when the gate voltage was at a weak inversion, the second at a moderate inversion, and the last at a strong inversion. For the nMOS case, we set the source voltages to ground consistently. For the pMOS case, we set the source voltages to Vdd consistently.

```
pMOS Gate Voltages              nMOS Gate Voltages
++++++++++++++++++              +++++++++++++++
weak: 4.35 V                    weak: 0.5 V
moderate: 4.25 V                moderate: 0.6 V
strong: 0 V                     strong: 5 V
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From the data that we collected, we were able to calculate the saturation current, early voltages, and intrinsic gails for different inversion levels for the pMOS and nMOS transistors.

Table 1: nMOS Inversion Levels and Values

Name	Saturation Current (A)	Early Voltage (V)	Intrinsic Gain
Weak Inversion	6.216e-9	22.8529	810.01
Moderate Inversion	6.537e-8	24.5567	719.36
Strong Inversion	4.557e-4	218.5612	172.52

Table 2: pMOS Inversion Levels and Values

Name	Saturation Current (A)	Early Voltage (V)	Intrinsic Gain
Weak Inversion	4.437e-09	26.01	1008.1
Moderate Inversion	1.105e-07	37.52	1151.9
Strong Inversion	0.0001324	57.28	131.09

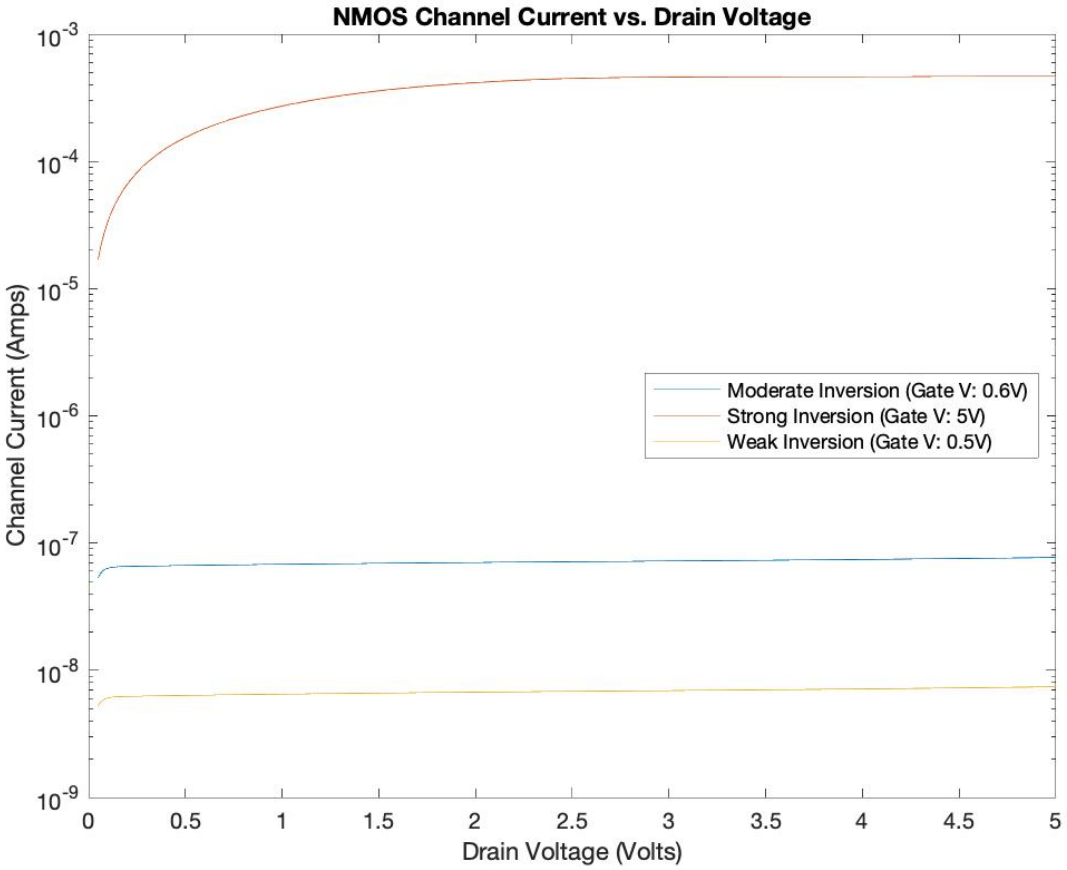

Figure 7: nMOS channel current as a function of drain voltage for three different inversion levels.

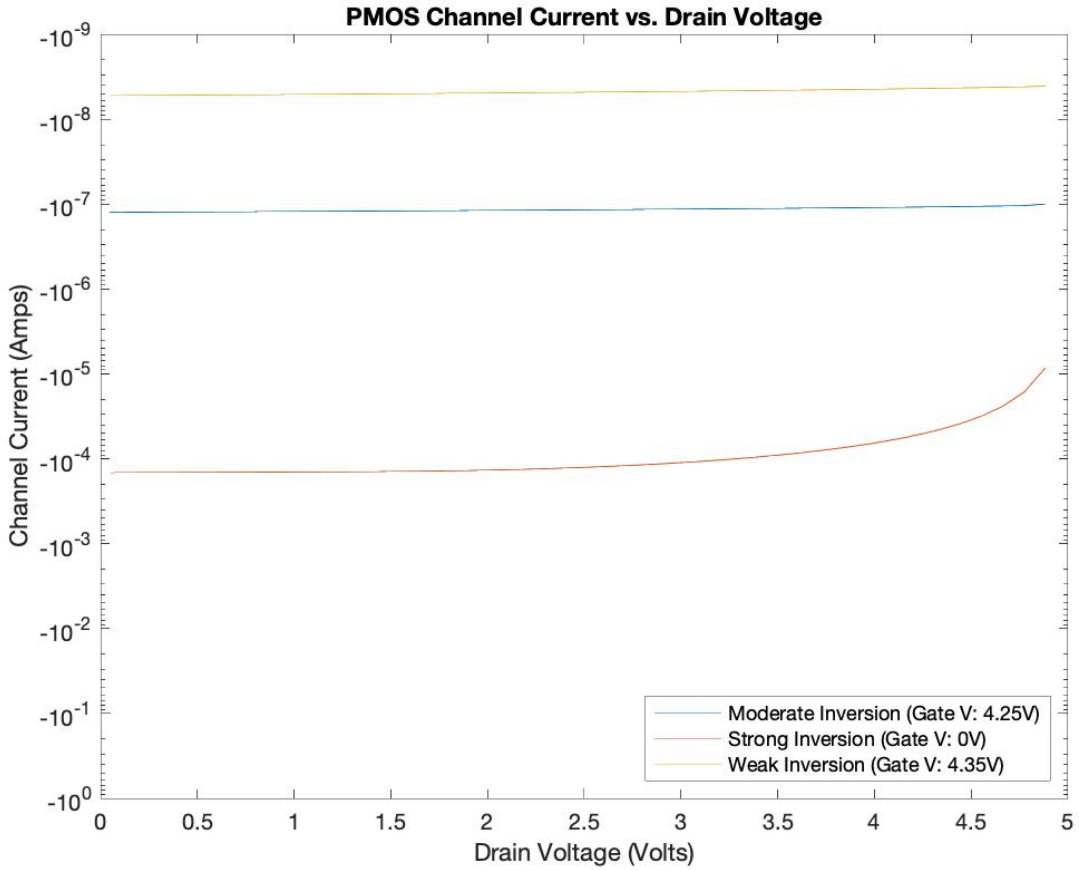

Figure 8: pMOS channel current as a function of drain voltage for three different inversion levels.

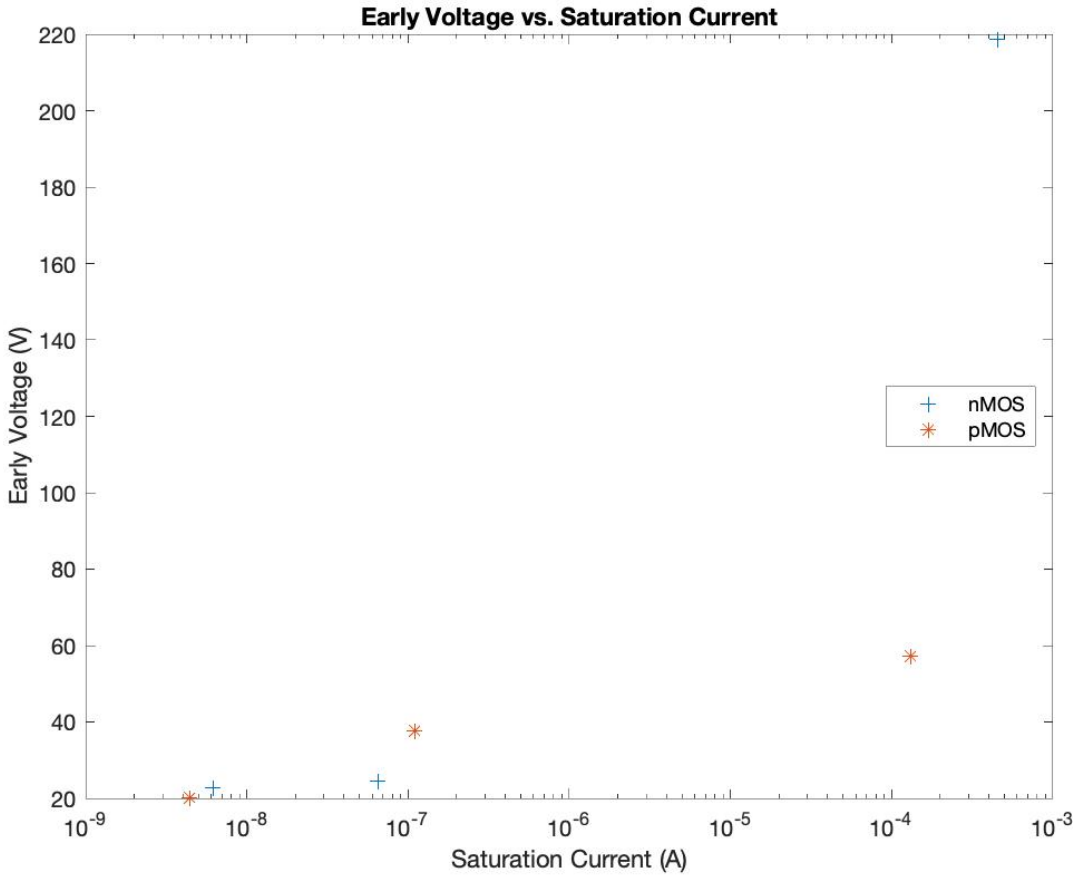

Figure 9: Early voltage as a function of saturation current for the nMOS and pMOS transistors in weak, moderate, and strong inversions.

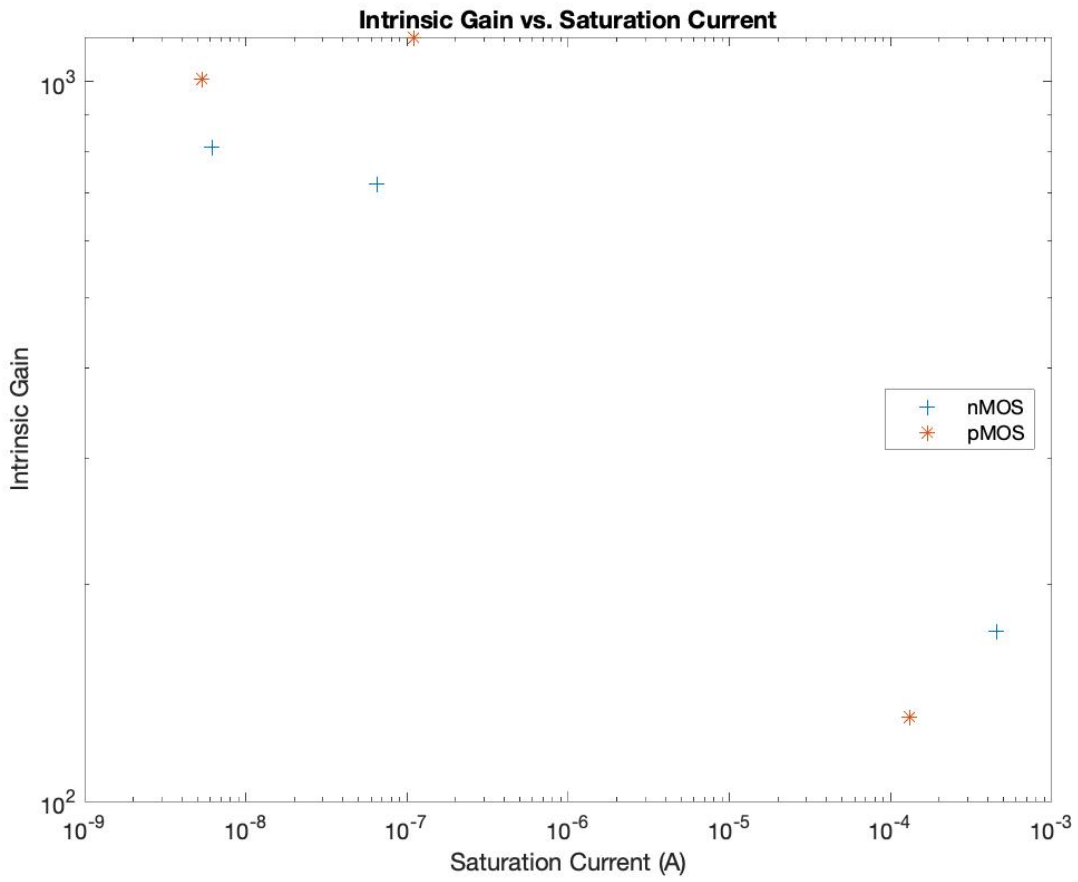

Figure 10: Intrinsic Gain as a function of saturation current for the nMOS and pMOS transistors in weak, moderate, and strong inversions.

From the data shown in tables 1 and 2, it is safe to assume that a transistor's intrinsic gain is significantly larger than unity for the weak and moderate cases. It does seem like this value dips quite considerably for the strong inversion cases, so it would not be correct to assume that a transistor's intrinsic gain is significantly larger than unity for this case.

We know that when going from weak to strong inversions that gs (and gm) increase. And we also know that early voltage and r0 are inversely proportional. So, if early voltage increases when going from weak to strong inversions that r0 will decrease when going from weak to strong inversions. So, we can say that gm*r0 decreases when going from weak to strong inversions.