

A chip is a system completely realised on a piece of Si.
(On a Si disc of dia. \approx 18 inches, 'chips' chopped off').

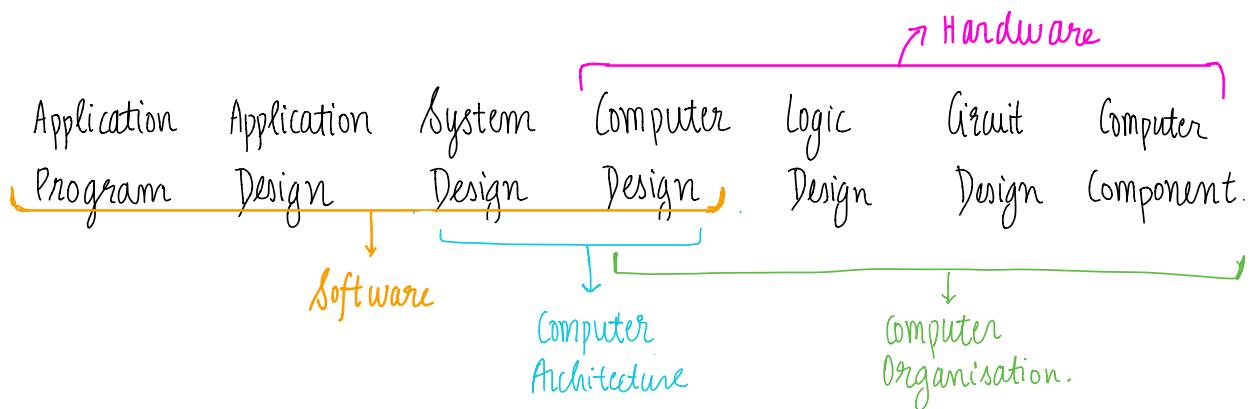
DC
Abhay
No Plag

. Computer Architecture:

A functional description of requirements and design for various parts of a computer.

. Computer Organisation:

How operational attributes, features are linked to realise Computer architecture.

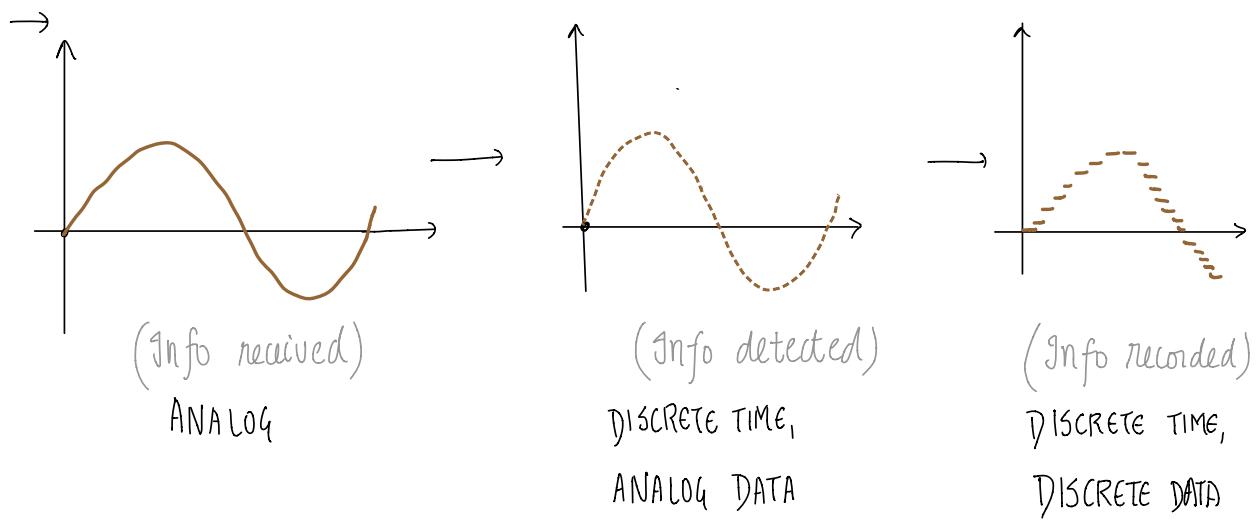


. SIGNALS:

Any variation in physical quantity wrt time.

. Analog Signals:

The diff. b/w successive values of time and amplitude is not discernable.



- All observed signals are discrete time signals.

Digital Signal:

If difference b/w successive values of time and amplitude of discrete signal is an integral multiple of a least count.
(Values are rounded off to nearest multiple of least count).

- Accuracy \propto no. of amplitude levels
 \propto sampling time.

Digital v/s Analog:

- **Flexibility:** (accuracy of digital signals can be varied).
- **Upgradability:** (digital req. partial redesign, analog req. complete redesign)
- **Delay:** (response time of analog << digital).

. BINARY NO. SYSTEM:

→ In hexadecimal system, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F are digits.

. Conversion:

→ To convert decimal → binary,

$$(5)_{10} \rightarrow \text{remainder}$$

$$\begin{array}{r} 5 \\ \hline 2 \\ \rightarrow 1 \\ \downarrow \\ 2 \\ \hline 1 \end{array}$$

this way.

∴ 101

$$0.625 \rightarrow \text{integer}$$

$$\begin{array}{r} 0.625 \\ \times 2 \rightarrow 1 \\ \downarrow \\ 0.25 \\ \times 2 \rightarrow 0 \\ \downarrow \\ 0.5 \\ \times 2 \rightarrow 1 \\ \downarrow \\ 0 \end{array}$$

this way.

∴ 0.101

=X=

→ Analog signal → ADC → Digital Signal Processing → DAC → Analog Signal Processing

=X=

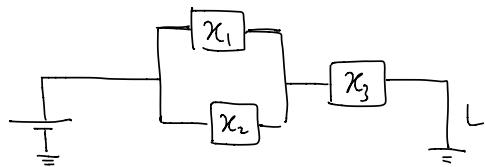
→ 4 bits: nibble, 8 bits: byte , 2^{10} : Kilo, 2^{20} : Mega, 2^{30} : Giga - CIM

→ A byte can accommodate one keyboard character.

LOGIC FUNCTIONS:

'Yes' or 'No'.

→ Union, Intersection, complement : logic operations.



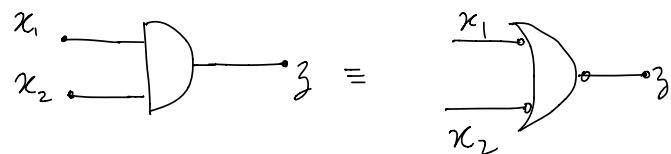
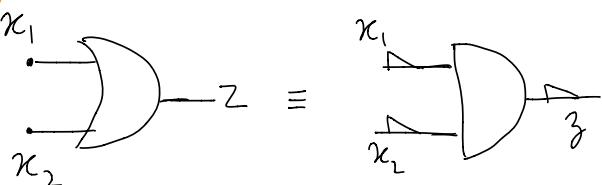
$$L = (X_1 + X_2) \cdot X_3$$

Precedence of Operations:

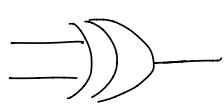
→ Order (), NOT, AND, OR {BNAO}.

Basic logic gates. → NAND, NOR are universal

→ Negative Logic symbol:



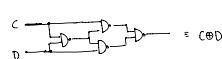
→ XOR:



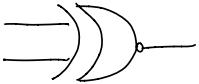
XOR

$$Z = X_1 \oplus X_2 \equiv X_1 \bar{X}_2 + \bar{X}_1 X_2$$

CIM



= COD

→ XNOR: 

$$\boxed{Z = \overline{x_1 \oplus x_2} \quad | \text{GM}}$$

$$= x_1 x_2 + \bar{x}_1 \bar{x}_2$$

• logical Analysis:

Consists of Truth Table, logical function and Timing diagram.

$$Z = (x_1 + x_2) \cdot x_3 \\ \text{etc.}$$

• BOOLEAN ALGEBRA:

→ Mathematical methods that simplify circuits rely primarily on Boolean Algebra.

• Huntington's Postulates:

i) Closure wrt + & .

ii) $x+0=x$, $x \cdot 1=x$.

iii) $x+y=y+x$, $x \cdot y=y \cdot x$.

iv) $x \cdot (y+z) = x \cdot y + x \cdot z$.

$x+(y \cdot z) = (x+y) \cdot (x+z)$.

v) $x+x'=1$, $x \cdot x'=0$.

vi) There exist at least 2 elements $x, y \in B$, s.t. $x \neq y$.

NOTE: → No inverse elements, ∴ no subtraction & division.

Duality:

Every algebraic expression deducible from Boolean Algebra is valid if operators and identity elements are interchanged (see postulates written in pairs).

Basic Theorems:

$$\begin{aligned}
 \rightarrow x + x &= x & , & x \cdot x = x & \rightarrow \left[\begin{array}{l} \text{Postf: } (x+x) \cdot 1 \\ \text{Postf: } (x+x) \cdot (x+x') \\ \text{Postf: } x \cdot (x+x') \end{array} \right] \xrightarrow{\text{Duality}} \left[\begin{array}{l} x \cdot x \\ x \cdot x + x \cdot x' \\ x \cdot (x+x') \end{array} \right] \\
 \rightarrow x + 1 &= 1 & , & x \cdot 1 = x & \rightarrow \left[\begin{array}{l} (x+1) \cdot (x+x') \\ x+1 \cdot x' \\ x+x' = 1 \end{array} \right] \xrightarrow{\text{Element}} \left[\begin{array}{l} x+1 + x \cdot x' \\ x \cdot (1+x') \\ x \end{array} \right] \\
 \rightarrow (x')' &= x & & & \rightarrow [x+x'=1 \quad \& \quad x \cdot x'=0 \quad \therefore (x')'=x] \\
 \rightarrow (x+y)+z &= x+(y+z) & , & x(yz) &= (xy)z. \\
 \rightarrow (x+y)' &= x'y' & \left[\begin{array}{l} \text{To prove, show that: } (xy) \cdot x'y' = 0 \quad \& \quad (x+y) \cdot x'y' = 1 \\ = x'y'x + x'y'y \\ = 0+0 \quad \therefore 1 \\ = (x+y)(x+y') \end{array} \right] & (xy)' &= x'+y'. \\
 \rightarrow x + xy &= x. & , & x \cdot (x+y) &= x. \\
 & \boxed{x(1+y)} & & \boxed{x \cdot x + x \cdot y}. \text{ or dual.} & \\
 & & & = x = &
 \end{aligned}$$

- A Boolean function corresponds to a circuit.
 \therefore Simplification of the expression \rightarrow Simplification of circuit.
- Each variable in each term constitutes an input, and is called a literal.

. Consensus Theorem:

$$\begin{aligned}
 & \rightarrow xy + x'z + yz = xy + x'z \\
 & \rightarrow (x+y) \cdot (x'+z) \cdot (y+z) = (x+y) \cdot (x'+z) \cdot yz(x+\bar{x}) \\
 & \rightarrow A \oplus 0 = A, \quad A \oplus 1 = \overline{A} \quad \text{CTM}
 \end{aligned}$$

use duality.

. Generalised Form of De Morgan's Theorem:

$$\begin{aligned}
 & \rightarrow (A+B+C \dots)^1 = A^1 \cdot B^1 \cdot C^1 \dots \\
 & \rightarrow (ABC \dots)^1 = A^1 + B^1 + C^1 \dots
 \end{aligned}$$

i.e., the complement of a func. is obtained by taking its dual and complementing each literal.

. LOGIC SYNTHESIS:

→ Implementing a given function using AND, OR, NOT
 or NAND only
 or NOR only.

. Normal Term:

Product/sum term in which no literal appears more than once.

- . Minterm: For a function of 'n' variables, minterm is a product term of 'n' literals. (denoted by m_0, m_1, \dots)

- Maxterm:** For a function of 'n' variables, Maxterm is a sum term with 'n' literals. (denoted by M_1, M_2, \dots).

- ### • Canonical Sum of Product (CSOP):

Every product term is a minterm.

- ## Sum of Products :

Set of AND terms connected by sum

- ### . Canonical Product of sum (CPOS):

Every sum term is a minterm.

- ### Product of Sum:

Set of OR terms connected by product.

∴ Given a truth table, we can form a func.

$$F = \sum_{(CSOP)} m(i,j,k\dots) = \prod_{(CP0S)} M(i,j,\dots).$$

→ Decimal equivalence for numbering is followed:



e.g;

	x	y	z
0 :	0	0	0
1 :	0	0	1
2 :	0	1	0
			...



To convert $f = a+d$ to POS.

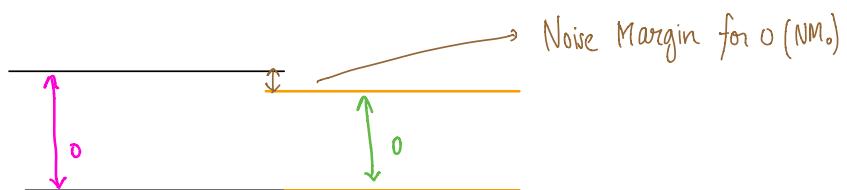
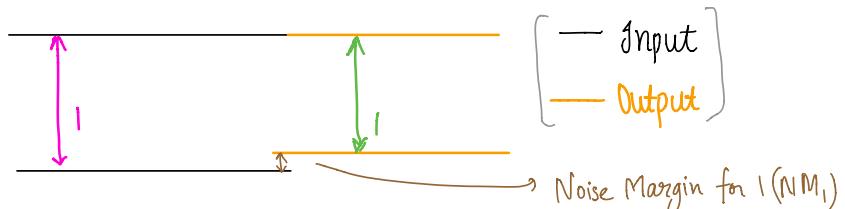
$$\begin{aligned}
 &= a+d + b\cdot\bar{b} + c\cdot\bar{c} \\
 &= a + b\cdot\bar{b} + d + c\cdot\bar{c} \\
 &= (a+b)(a+\bar{b}) + (d+c)(d+\bar{c}) \\
 &= [(a+b) \cdot (a+\bar{b}) + d+c] \cdot [(a+b) \cdot (a+\bar{b}) + d+\bar{c}] \\
 &= (d+c+a+b) \cdot (d+c+a+\bar{b}) \cdot (a+b+d+\bar{c}) \cdot (a+\bar{b}+\bar{c}+d).
 \end{aligned}$$

Logic Circuit:

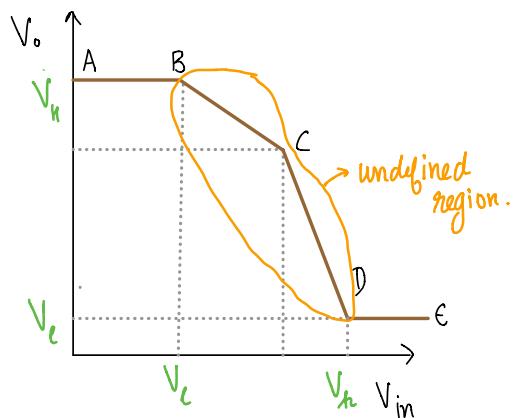
Any circuit in which the signals are constrained to have some no. of discrete values is called logic circuit.

If only 2 values: binary logic.

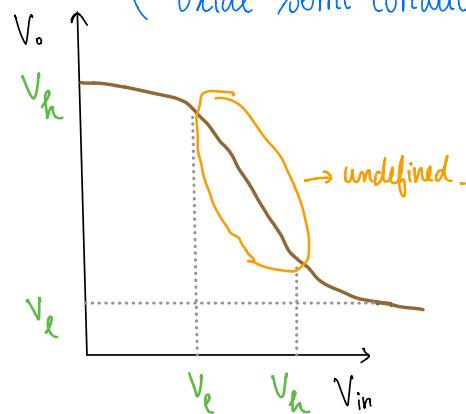
Binary levels:



. TTL: (Transistor-Transistor logic)



. CMOS: (Complementary Metal Oxide Semi-conductor)



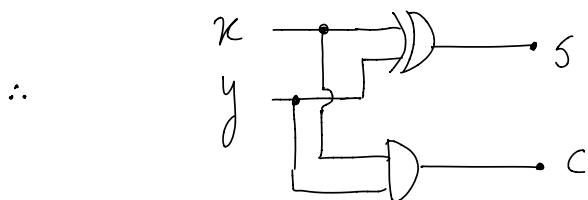
$$\rightarrow n^2 n^1 n^0 \cdot n^{-1} n^{-2}$$

\curvearrowleft radix point

. Half Adder:

x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$s = x \oplus y$ CTM
 $c = xy$.



. Full Adder:

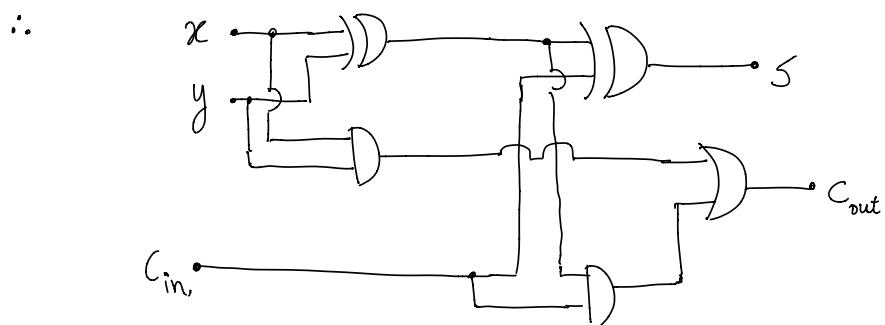
C_{in}	x	y	s	C_{out}
----------	-----	-----	-----	-----------

0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

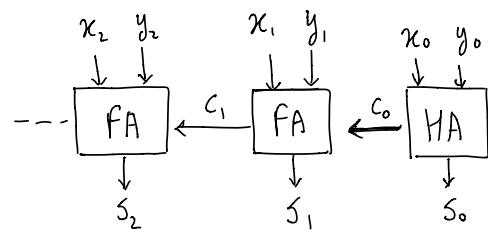
$$S = C_{in} \oplus (x \oplus y).$$

$$C = x \cdot y + C_{in} \cdot (x \oplus y).$$

(CTM)



. n-Bit Full Adder:

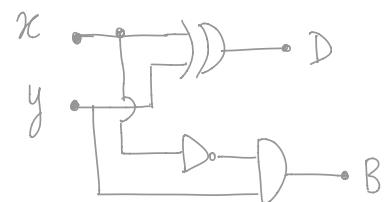


. Half-Subtractor:

	x	y	D	B
→	0	0	0	0
	0	1	1	1
	1	0	1	0
	1	1	0	0

$$D = x \oplus y \quad \text{CTM}$$

$$B = \bar{x} \cdot y.$$

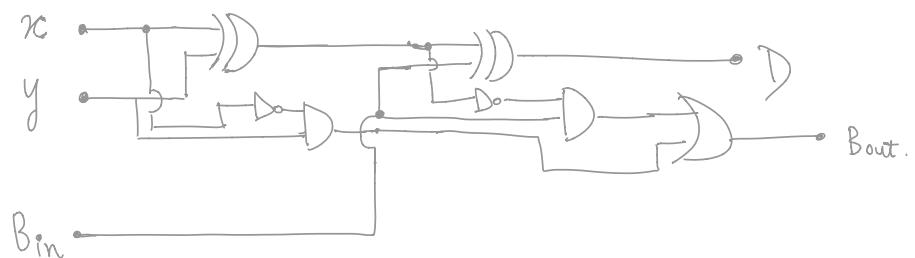


. Full Subtractor:

	B_{in}	x	y	D	B_{out}
0	0	0	0	0	0
0	0	0	1	1	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	0	0	1
1	1	0	0	0	0
1	1	1	1	1	1

$$D = B_{in} \oplus (x \oplus y) \quad \text{CTM}$$

$$B_{out} = (\bar{x} \oplus \bar{y}) \cdot B_{in} + \bar{x} \cdot y$$



. SIGNED NUMBERS:

i) Sign & Magnitude Representation:

- Easy to understand, but diff. for hardware realisation.

→ Complements are used to simplify operations, leading to less expensive circuits.

ii) (n-1)'s complement representation:

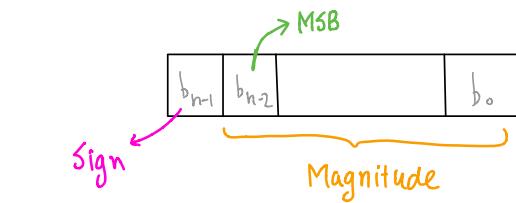
- (n-1)'s complement of a no. is taken by complementing every bit. (for eg; in decimal, 9's complement of 2 is 7).
- It is actually subtracting the no. from (n-1)(n-1) ...
(e.g., $999 - 048 = 951$).

$$\text{eg; } 176 - 048$$

$$= 176 + 951 - 999$$

$$= 1127 - 1000 + 1$$

$$= 128.$$



Sign MSB

Magnitude

$$\text{eg; } 176 - 1348$$

$$= -(1348 - 176)$$

$$= - (1348 + 9823 - 9999)$$

$$= - (11172 - 10000)$$

$$= - 1172.$$

- In case of binary, the complement is obtained by subtracting from 111....

iii) r 's Complement:

→ r 's complement is obtained by adding 1 to $(r-1)$'s complement.

$$\begin{aligned} \text{eg, } & 176 - 048 \\ & 176 + 952 - 1000. \\ & = 1128 - 1000 \\ & = 128. \end{aligned}$$

$$\begin{aligned} \text{eg, } & 048 - 176 \\ & - (176 - 048) \\ & = - (176 + 952 - 1000). \\ & = - (1128 - 1000). \end{aligned}$$

→ To find r 's complement for binary nos.;
Start from LSB Keep all zeroes and first 1, after which, take
complement of all digits.

Shortcut:

→ To find r 's complement of any no. of radix ' r ',
Keep all least significant zeroes. Subtract the first non-zero
least significant bit from r and rest all from $(r-1)$.

→ Ignore radix point while finding complement.

→ Algorithm for Subtraction Using r 's Complement:

If $M-N$. M, N are unsigned numbers.
 $\rightarrow M + (r^n - N) - r^n$

$$= M + N' - r^n$$

↓ ↓
 $M \geq N$ $M < N$

- sum produces carry, discard it.
- no carry.
→ Take complement of result of $(M+N')$ & put '-'.

→ Algorithm for Subtraction Using $(r-1)$'s Complement:

$$\begin{aligned} & M - N \\ &= M + ((r^n - 1) - N) - (r^n - 1). \\ &= M + N' - (r^n - 1). \end{aligned}$$

↓ ↓
 $M + N'$ produces carry, No carry.
 • Do end around carry. Take $(r-1)$'s complement of
 $M + N'$.
 $= X =$

→ Signed r 's and $(r-1)$'s complement is obtained by complementing the no., including the signed bit.

→ In case of signed binary nos., if there is no carry, the no. is obtained in complement form.

. BINARY CODES:

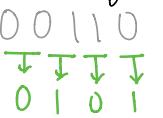
- Discrete, distinct among group info. can be represented as binary code. Computer bits usually represent coded info., not plain binary digits.
- Binary codes consist of bits, each combination representing an element from the set that is coded.

. Decimal Codes:

- If 4 bits, 16 diff. combinations. 10 needed for decimal.
Different arrangements yield diff. codes.
 - Straight binary assignment = BCD. (used for decimals, encoded in form of bits)
- BCD, 2421 are **weighted codes**.
- 2421, excess 3, 8.4-2-1 code are self complementing.
- Excess 3 is obtained by adding 3 to BCD.
 - Diff symbols give same value to 2421, hence only those chosen which are self complementary.

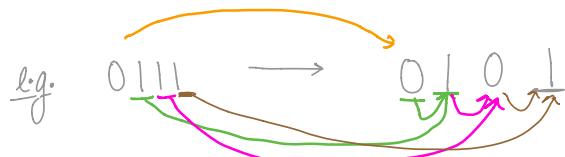
• Binary \rightarrow Gray:

- Add 0 to left of MSB.
- XOR consecutive digits to obtain gray code (MSB first).

e.g. $0110 \rightarrow$ 
 $\begin{array}{r} 00110 \\ \text{\scriptsize\textbf{T T T T}} \\ \hline \text{\scriptsize 0 1 0 1} \end{array}$
↳ gray code.

• Gray \rightarrow Binary:

- MSBs are identical.
- To obtain a given index, consider XOR of gray code at that index and previous binary bit.



• KARNAUGH MAP:

- K-Map is a diagram made of squares, each square representing one minterm / maxterm of the function that is to be minimised.

- 2 minterms / maxterms , OR/AND \rightarrow 1 variable removed.

4

$\rightarrow 2$

8

$\rightarrow 3$

:

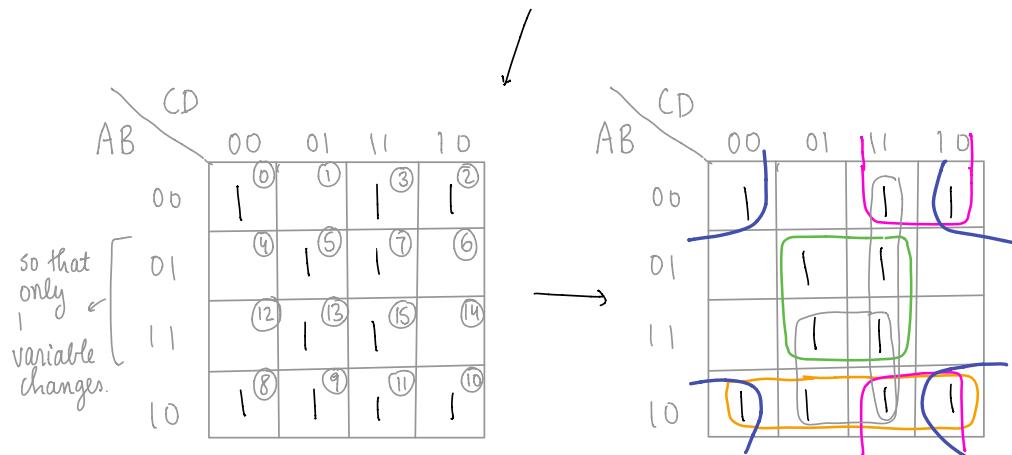
→ Squares must be combined horizontally or vertically or squared (including cyclic pairs), in powers of 2 only ($2, 4, 8, 16 \dots$). Such combinations called adjacent squares.

→ Prime Implicant:

Term obtained by combining maximum possible adjacent squares.

If the prime implicant is the only one covering 1/more minterms, it's called essential prime implicant.

$$\text{eg; } f(A, B, C, D) : \sum m(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15).$$



: EPI : P.I.

Hint: Just check variables with same value across all squares.

$$\rightarrow \underline{\overline{BD}} + \underline{BD} + \underline{A\overline{B}} + \underline{\overline{B}C}$$

$$\therefore f = \overline{BD} + BD + A\overline{B} + \overline{B}C.$$

→ For POS:

i) By Minterms:

- Complement the func. by replacing all 0's with 1's & vice-versa
- Form SOP.
- Take complement. ($\overline{\text{SOP}} = \text{POS}$).

ii) By Maxterms:

- Fill 0's in maxterms given for func.
- Form PI & EPI as usual.
- Write func. in POS form

$$[A=0, B=1 \rightarrow (A+\overline{B})]$$

↳ when written in POS.

• Don't Care:

→ For certain func., outputs are not specified for certain inputs.

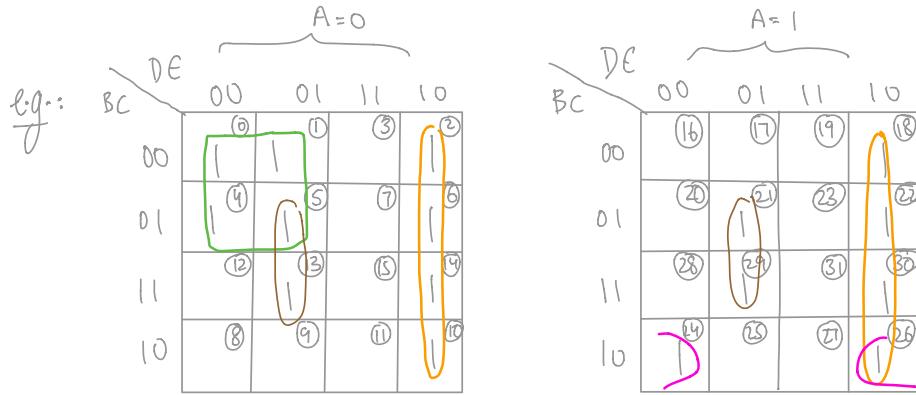
We DON'T CARE what the output is for those inputs. and assume it to be 0 or 1 based on our convenience. (so as to simplify as many terms as possible in K Maps).

- Same don't care condition can be assumed 1 in SOP & 0 in POS, or vice-versa.

. 5 Variable K-Map:

→ Shannon's Theorem:

$$f(x_1, x_2, \dots, x_n) = \bar{x}_1 \cdot f_1(x_2, x_3, \dots, x_n) + x_1 \cdot f_1^*(x_2, \dots, x_n).$$



- . Find overlap of 2 squares, eliminate A from those terms.
- . Write other terms as usual.

$$f = \underline{D\bar{E}} + \underline{\bar{A}\bar{B}\bar{D}} + \underline{C\bar{D}E} + \underline{AB\bar{C}\bar{E}}.$$