Rubric:
A1:
Equation for QA or Q1: 1 mark
Equation for QB or Q2: 1 mark
Equation for z: 1 mark
State table: 2 marks
Sequence detection and explanation: 5 marks

A2:
QA: 1 mark
QB: 1 mark
QC: 3 marks.

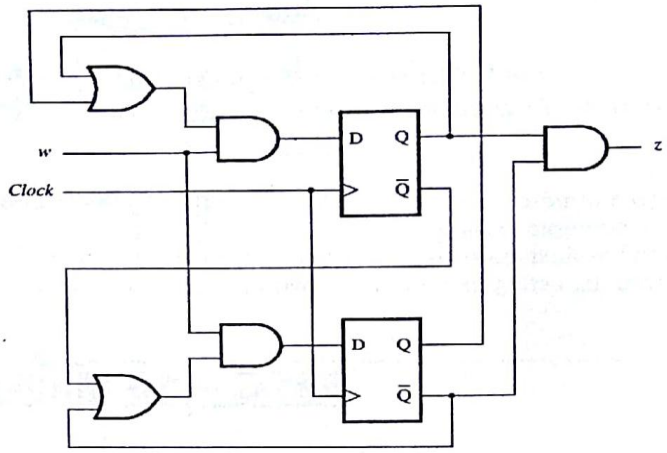
ECE111: Digital Circuits: End-Semester Exam

Date: Nov. 28, 2018

Set A – 15 Marks

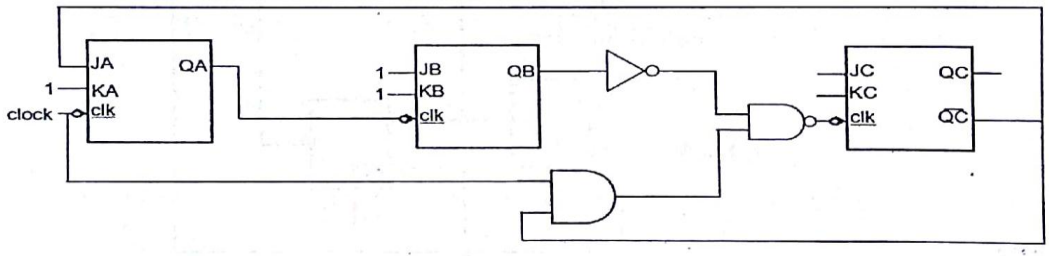
Jasmine

A1. Derive the state table for the circuit given below. What sequence of input values on wire *w* is detected by this circuit?



10 Marks

A2. For the circuit given below, draw the timing diagram (for at least 10 clock cycles), starting with QA = QB = QC = 0. All FFs are JK FF and triggered on negative edge.



5 Marks

Please note that for set-B, all flip-flops should be D-type only.
Rubric for B1:
Circuit diagram: 4 marks
Explanation: 2 marks

Rubric for B2:
Mod10 counter design and circuit: 3 marks
Integration with B1: 1 mark

Rubric for B3:
state table: 2 marks
FF input expressions : 3 marks or circuit diagram: 3 marks

Set B – 15 Marks

Jab hadup

B1. A sequential circuit has two inputs, $w1$ and $w2$, and an output, z. Its function is to compare the input sequences on the two inputs. If $w1 = w2$ during any four consecutive clock cycles, the circuit produces $z = 1$; otherwise, $z = 0$.
For example
$w1$: 0110111000110
$w2$: 1110101000111
z : 0000100001110

6 Marks

B2. Extend the circuit in B1 to count the number of times the output is 1. The count should be from 0 to 10. After 10, it resets to 0.

4 Marks

B3. Design a *three-bit* counter like circuit controlled by the input w. If $w = 1$, then the counter adds 2 to its contents, wrapping around if the count reaches 8 or 9. Thus if the present state is 6 or 7, then the next state becomes 0 or 1, respectively. If w = 0, then the counter subtracts 1 from its contents, acting as a normal down-counter. Use D flip-flops in your circuit.

5 Marks

Rubric For C1:

Compute time period as 1ns or 1000 ps: 0.5 marks

Path from F1 to F3:
Setup Analysis: 1000 > 10+50+30: No violation [0.5 mark]
Hold Analysis: 10+50 > 20: No violation [0.5 Mark]

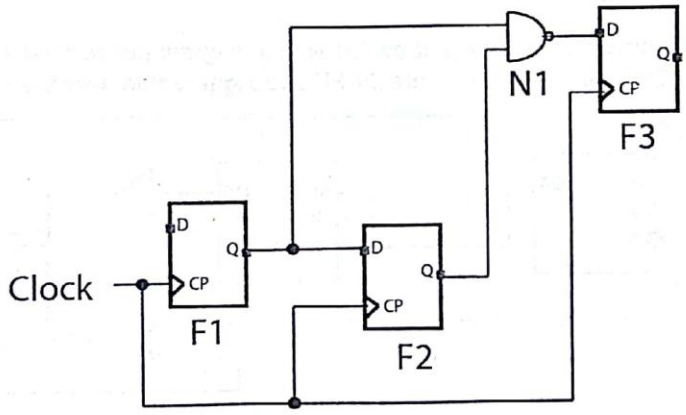
Path from F2 to F3:
Setup Analysis: 1000 > 10+50+30: No violation [0.5 mark]
Hold Analysis: 10+50 > 20: No violation [0.5 Mark]

Path from F1 to F2:
Setup Analysis: 1000 > 10+30: No violation [0.5 mark]
Hold Analysis: 10 > 20: Violated [2 Mark]

Set C – 10 Marks

Vaibhav.

C1.



A sequential circuit is shown above. The following data is valid for all the flip-flops F1, F2 and F3:

Setup Time = 30 ps
Hold Time = 20 ps
Clock-to-Q Delay = 10 ps

The delay of the NAND gate N1 is 50 ps.
The frequency of "Clock" is 1 GHz.
Ignore the delay of all the wires.
Find if there is any timing problem in the above circuit.

5 Marks

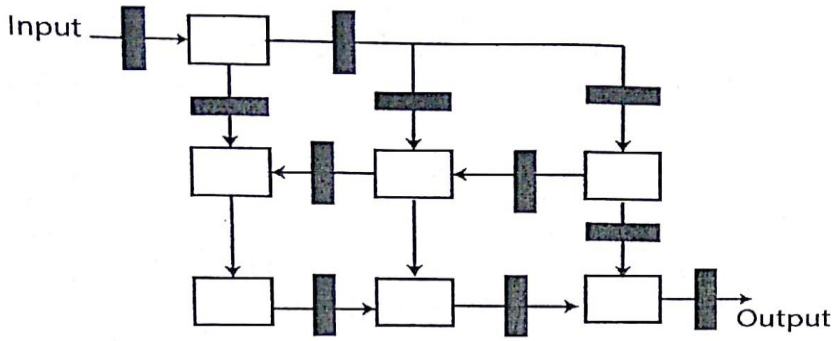
Rubric For C2:

Circuit 1: 0.5 Marks For Identifying that this is not a well-formed K-stage pipeline
2 Marks for explanation (Two paths must be shown/described that have different number of registers in the path)

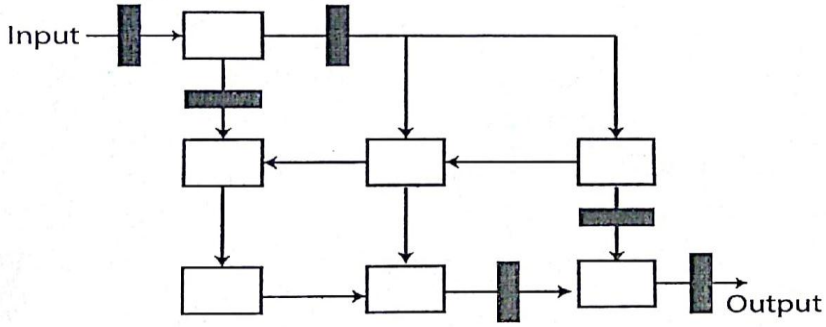
Circuit 2: 0.5 Marks For Identifying that this is a well-formed K-stage pipeline
1 Mark for explanation that all paths have same number of registers
1 Mark for identifying that K=3 or K=4

C2. In the following two circuits, the combinational elements are shown as unshaded rectangles with non-zero propagation delay and the flip-flops are shown as fully-shaded black rectangles. For each of the two circuit state whether they represent well-formed K-stage pipeline. If a circuit represent a well-formed k-stage pipeline then find the value of K If a circuit does not represent a well-formed k-stage pipeline then explain the reason for it.

1. Circuit-1



2. Circuit 2



5 Marks