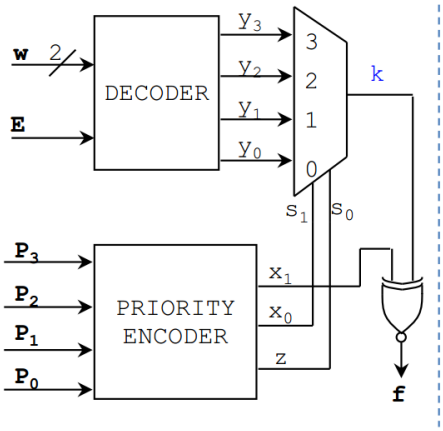
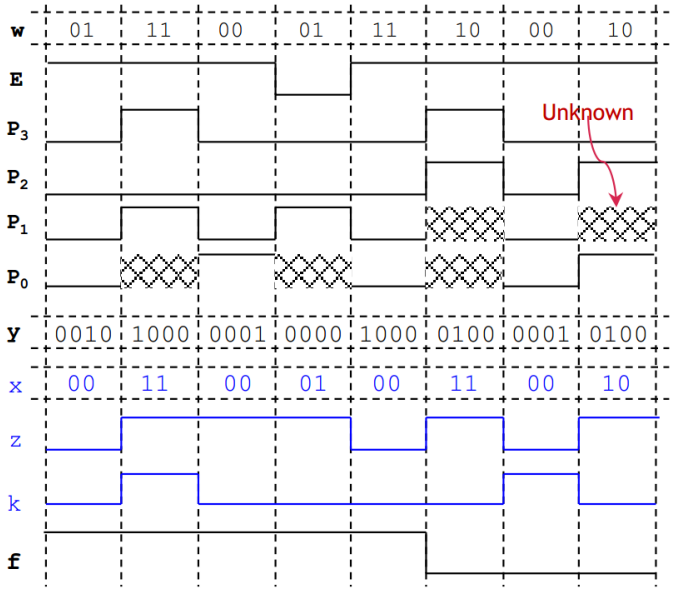
Digital Circuits Quiz-2 (3rd October, 2018)

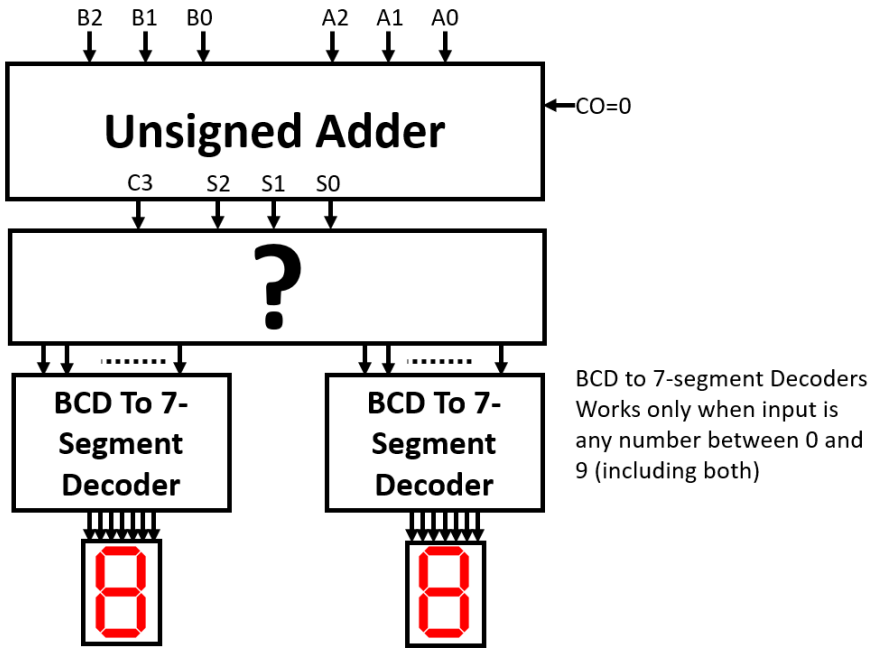
Time: 30 minutes

1. Complete the timing diagram of the circuit shown below. The output z of the priority encoder is the valid bit indicator. The signal x and y is to be represented compactly as x_1x_0 and $y_3y_2y_1y_0$, respectively. **[5 Marks]**





2. Consider the circuit shown below where the output of a 3-bit adder needs to be displayed on the two digits of the 7-segment display. For example, if the adder output is 9, then circuit should display 09 where 0 should be displayed on left display and 9 on right display. Existing BCD-to-7 segment decoder works only when input number is between 0 and 9 and we have to use it since it has been hardwired to 7-segment display board. You need to design combinational circuit between Adder and 7-segment decoder (shown as question mark in the Figure below) so that the adder output is correctly displayed on the 7-segment display. **[5 Marks]**



Approach 1:

Soln 2.

O/P of Unsigned Adder is i/P to the Question mark Block. According to the input we have to differentiate the o/p.

eg: 14 — $C_3S_2\ S_1S_0$ = 1110 → $X_3X_2X_1X_0$ = 0001 ; $Y_3Y_2Y_1Y_0$ = 0100.

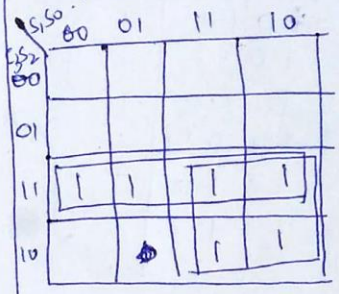
More over, Addition can never be (1) (4) 15 ∴ Take dont care.

Similarly for all combinations.

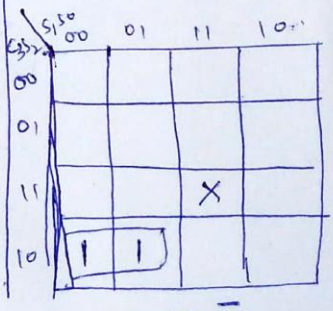
C_3	S_2	S_1	S_0	X_3	X_2	X_1	X_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0				0	0	0	0	0
0	0	0	1				0	0	0	0	1
0	0	1	0				0	0	0	1	0
0	0	1	1				0	0	0	1	1
0	1	0	0				0	0	1	0	0
0	1	0	1				0	0	1	0	1
0	1	1	0				0	0	1	1	0
0	1	1	1				0	0	1	1	1
1	0	0	0				0	1	0	0	0
1	0	0	1				0	1	0	0	1
1	0	1	0				0	0	0	0	0
1	0	1	1				0	0	0	0	1
1	1	0	0				0	0	0	1	0
1	1	0	1				0	0	0	1	1
1	1	1	0				0	0	1	0	0
1	1	1	1				X	X	X	X	X

← all are zero

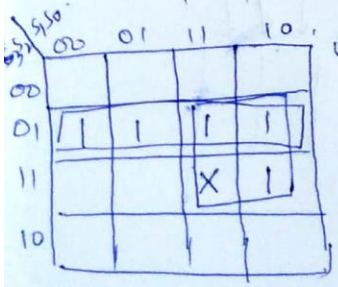
K-map for X_0.



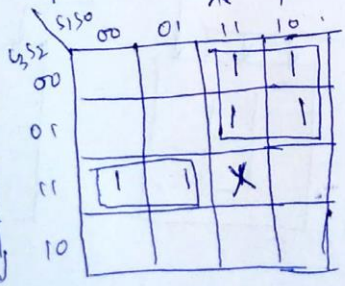
$X_0 = C_3S_2 + C_3S_1$.



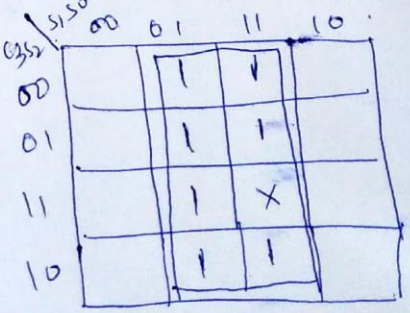
$Y_3 = C_3\bar{S}_2\bar{S}_1$



$Y_2 = \bar{C}_3S_2 + S_2S_1$



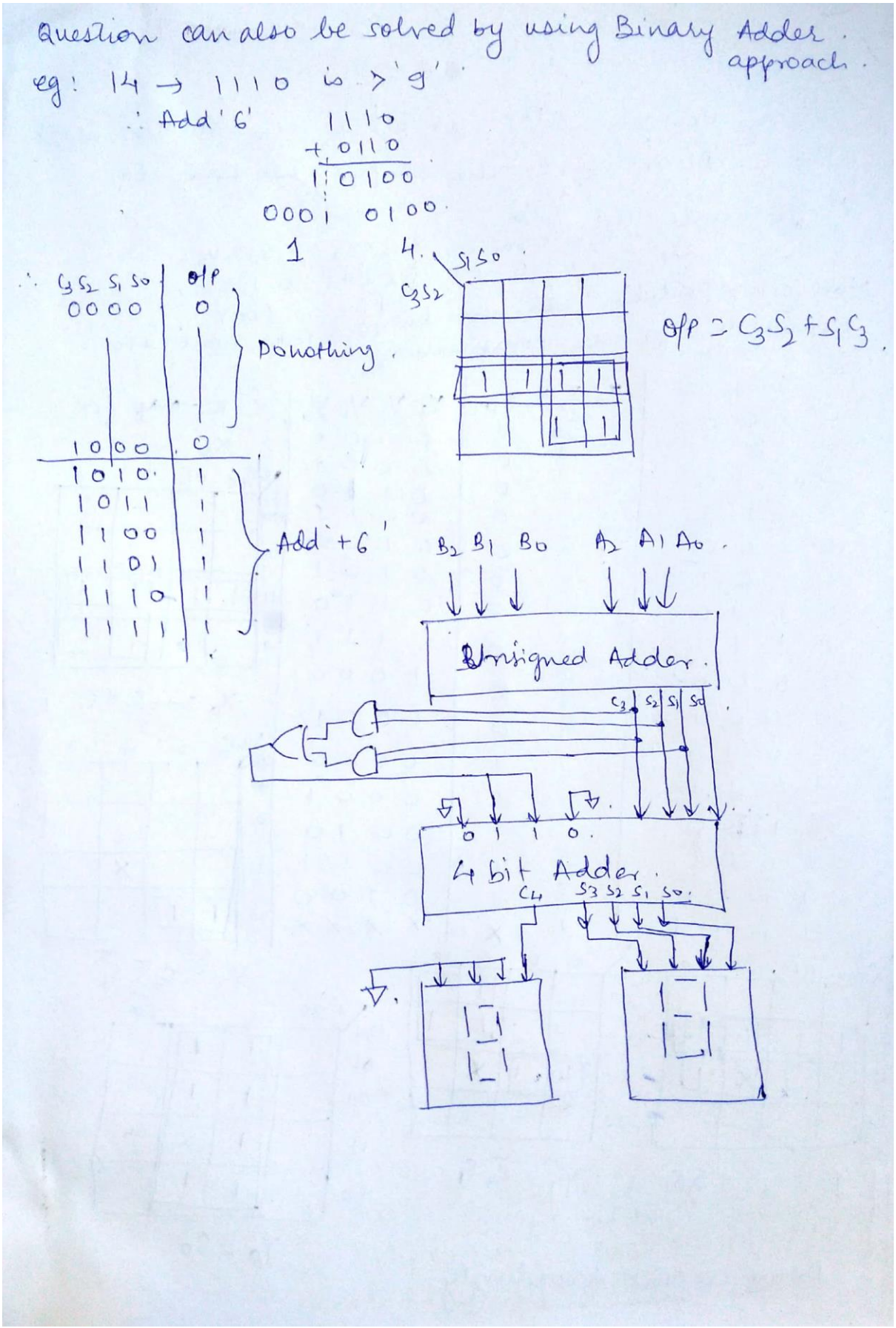
$Y_1 = \bar{C}_3S_1$



$Y_0 = S_0$.

Draw circuit Accordingly.

Approach 2:


Question can also be solved by using Binary Adder approach.
eg: 14 → 1110 is > '9'.
∴ Add '6'
1110
+0110
10100
0001 0100
1
$C_3 S_2 S_1 S_0$ | Op
0000 | 0
Do nothing.
1000 | 0
1010 | 1
1011 | 1
1100 | 1
1101 | 1
1110 | 1
1111 | 1
Add '+6'
4. $S_1 S_0$
$C_3 S_2$
Op = $C_3 S_2 + S_1 C_3$.
$B_2 B_1 B_0$ $A_2 A_1 A_0$
Unsigned Adder.
C_3 S_2 S_1 S_0
0 1 1 0
4 bit Adder.
C_4 $S_3 S_2 S_1 S_0$