SET A

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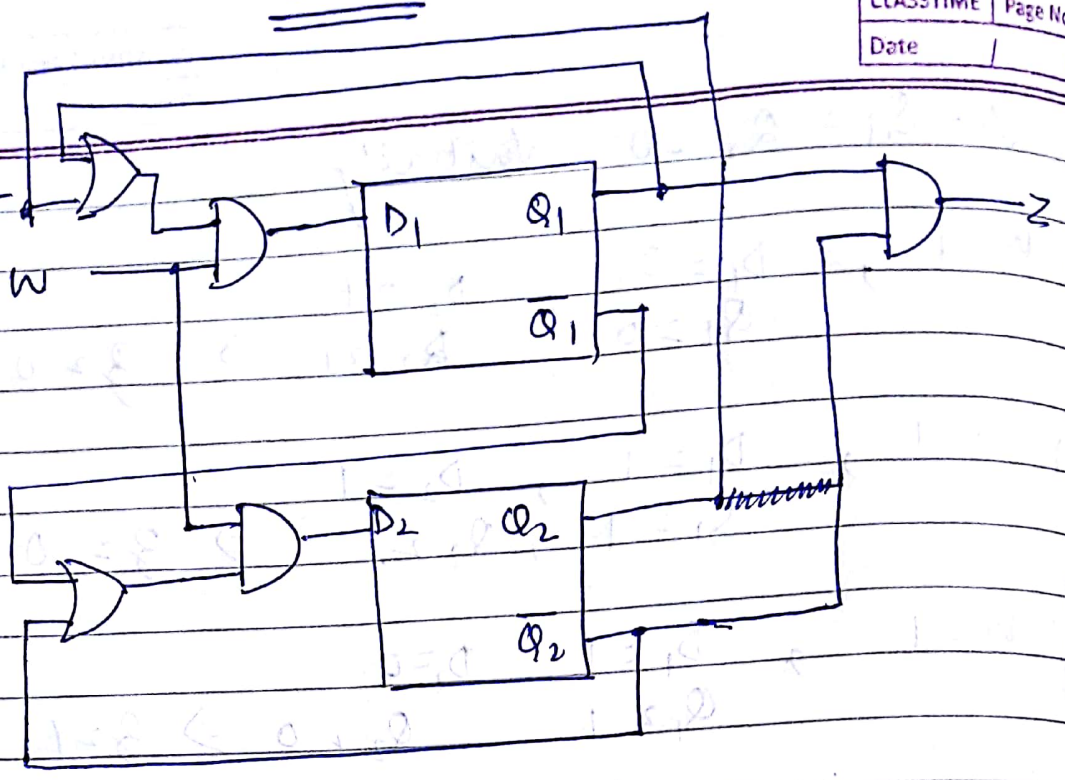
A1:-

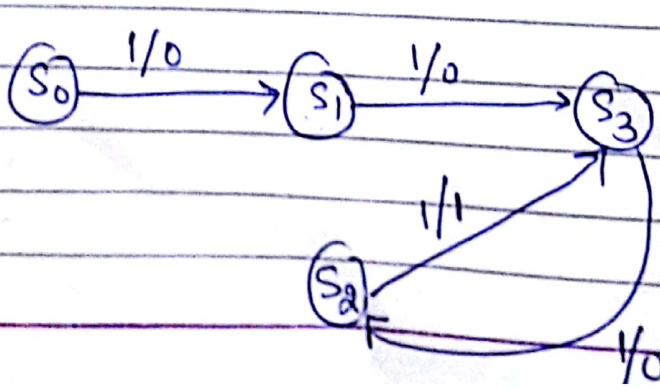


$Q_1^+ = w(Q_1 + Q_2)$

$Q_2^+ = w(\overline{Q_1} + \overline{Q_2})$

$z = Q_1^+ \cdot Q_2^+$

w	Q_1	Q_2	Q_1^+	Q_2^+	z
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	1	0	0



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Let $Q_1 = Q_2 = 0$ initially

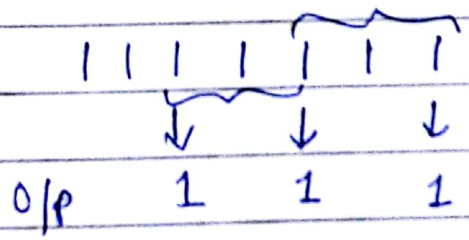
(1) $w = 1$, $D_1 = 0$, $D_2 = 1$
$Q_1 = 0$, $Q_2 = 1 \Rightarrow z = 0$

(2) $w = 1$, $D_1 = 1$, $D_2 = 1$
$Q_1 = 1$, $Q_2 = 1 \Rightarrow z = 0$

(3) $w = 1$, $D_1 = 1$, $D_2 = 0$
$Q_1 = 1$, $Q_2 = 0 \Rightarrow z = 1$

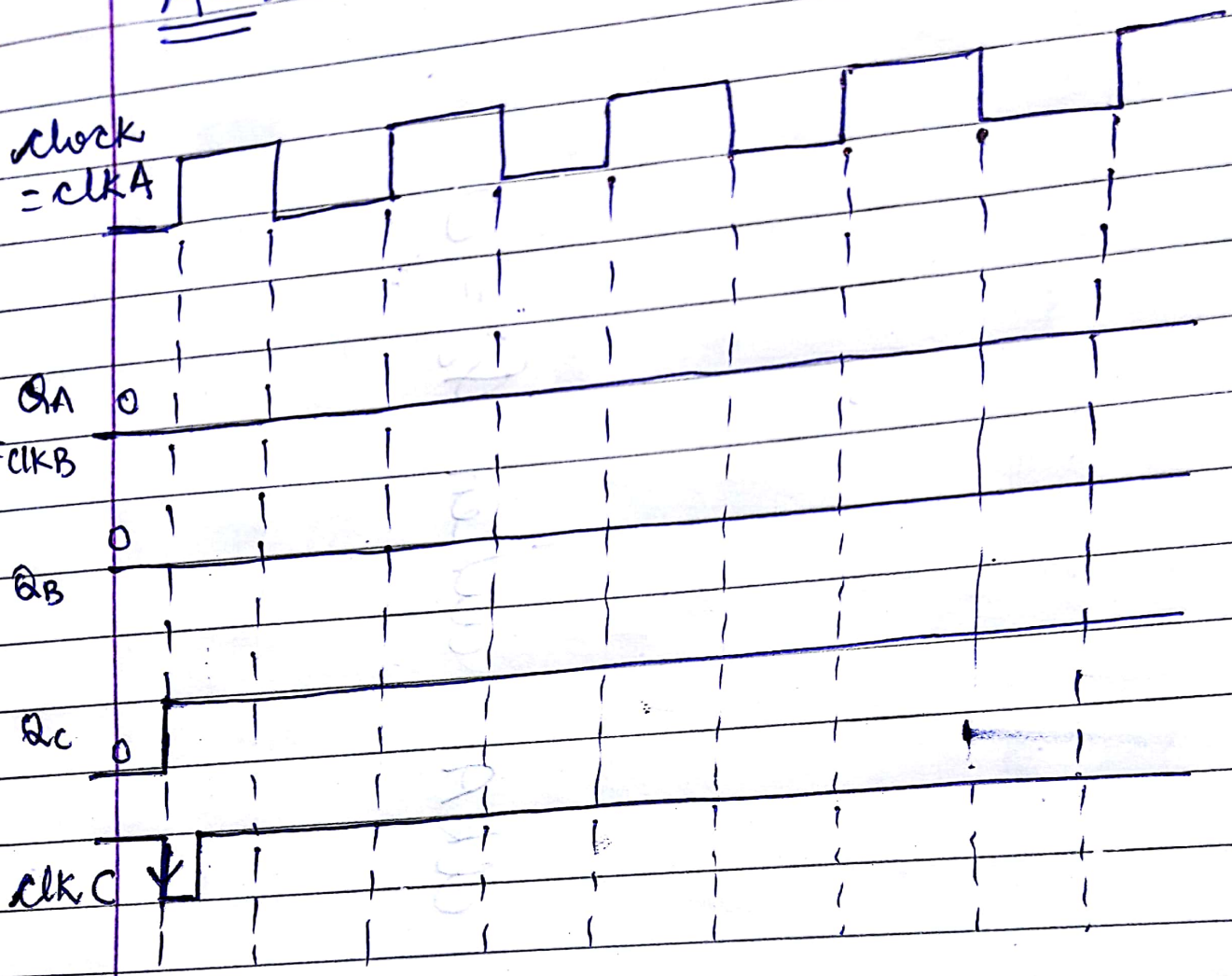
(4) $w = 1$, $D_1 = 1$, $D_2 = 1$
$Q_1 = 1$, $Q_2 = 1 \Rightarrow z = 0$

(5) $w = 1$, $D_1 = 1$, $D_2 = 0$
$Q_1 = 1$, $Q_2 = 0 \Rightarrow z = 1$



Detecting '111'

A2:



$$clk\,C = \overline{\overline{Q_B} \cdot clk_A \cdot \overline{Q_C}}$$

$$= Q_B + \overline{clk_A} + Q_C$$

Set - B

(Manish Agrawal).

B1.

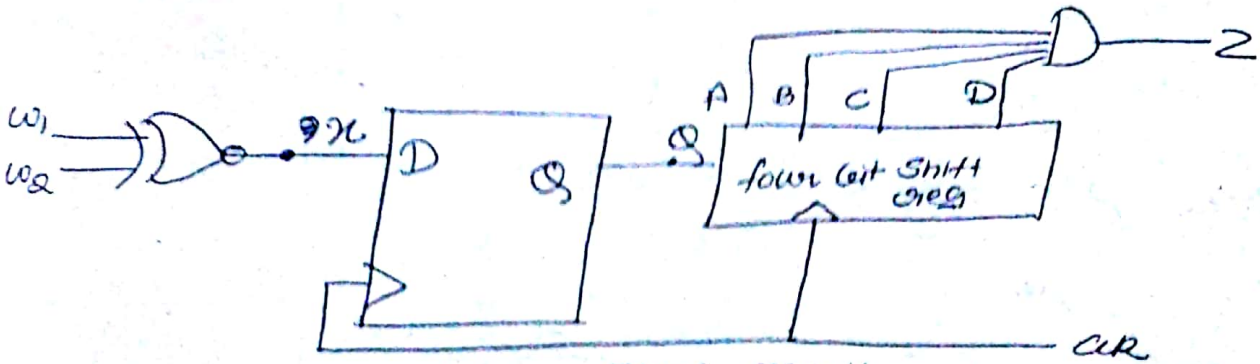
$w_1 = 0110111000110$

$w_2 = 1110101000111$

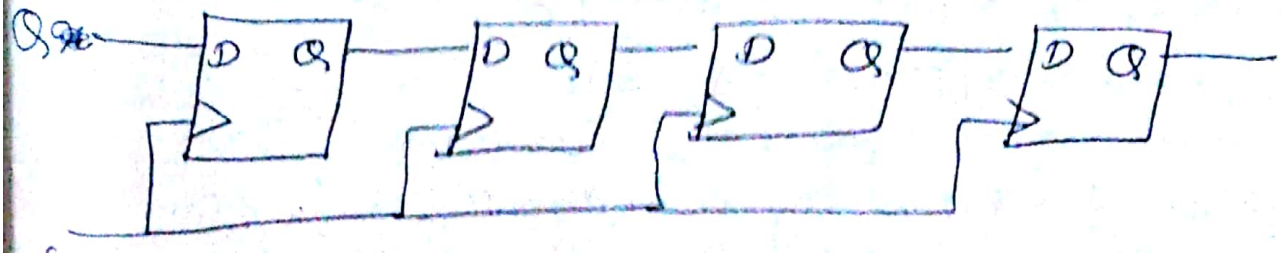
$b2 = 0000100000110$

When $w_1 = w_2$ => then XNOR will give 1.

w_1	w_2	O/P
0	0	1
0	1	0
1	0	0
1	1	1



Final circuit.



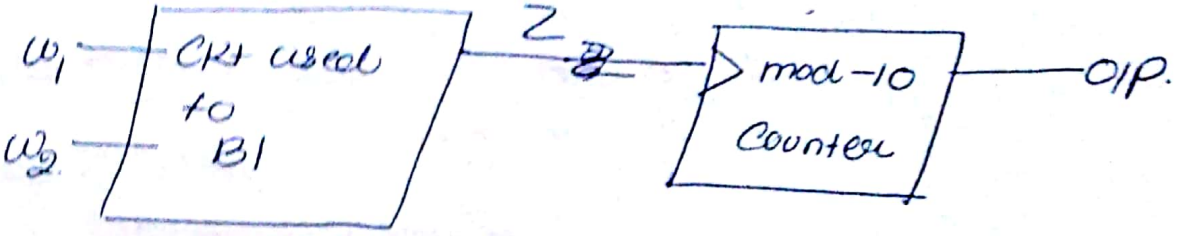
four-bit shift register.

When A, B, C, D will be 1 Simultaneously, then O/P Z = 1.

B2

For counting the no. of times Z is one, we can implement a ~~decade~~ mod-10 counter ~~of~~ whose clock will be triggered by Z.

When Z=1, clock will get triggered and counter will count +1.



B3. Four UP Counting →

Present State			next state			D. i/p.		
A	B	C	A	B	C	D_1	D_2	D_3
0	0	0	0	1	0	0	1	0
0	0	1	0	1	1	0	1	1
0	1	0	1	0	0	1	0	0
0	1	1	1	0	1	1	0	1
1	0	0	1	1	0	1	1	0
1	0	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0
1	1	1	0	0	1	0	0	1

Four down Counting

Present state			next state			D-i/p		
A	B	C	A+	B+	C+	D_{1d}	D_{2d}	D_{3d}
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0
1	0	0	0	1	1	0	1	1
1	0	1	1	0	0	1	0	0
1	1	0	1	0	1	1	0	1
1	1	1	1	1	0	1	1	0

Four UP ⇒

D_{1w} ⇒

A \ BC	00	01	11	10
0	0	0	1	1
1	1	1	0	0

⇒ $AB' + A'B$

$= A \oplus B$

D_{2w} ⇒

A \ BC	00	01	11	10
0	1	1		
1	1	1		

⇒ $\bar{B}$

D_{3w} ⇒

A \ BC	00	01	11	10
0		1	1	
1		1	1	

⇒ C

foo down ⇒

D_{1C} ⇒

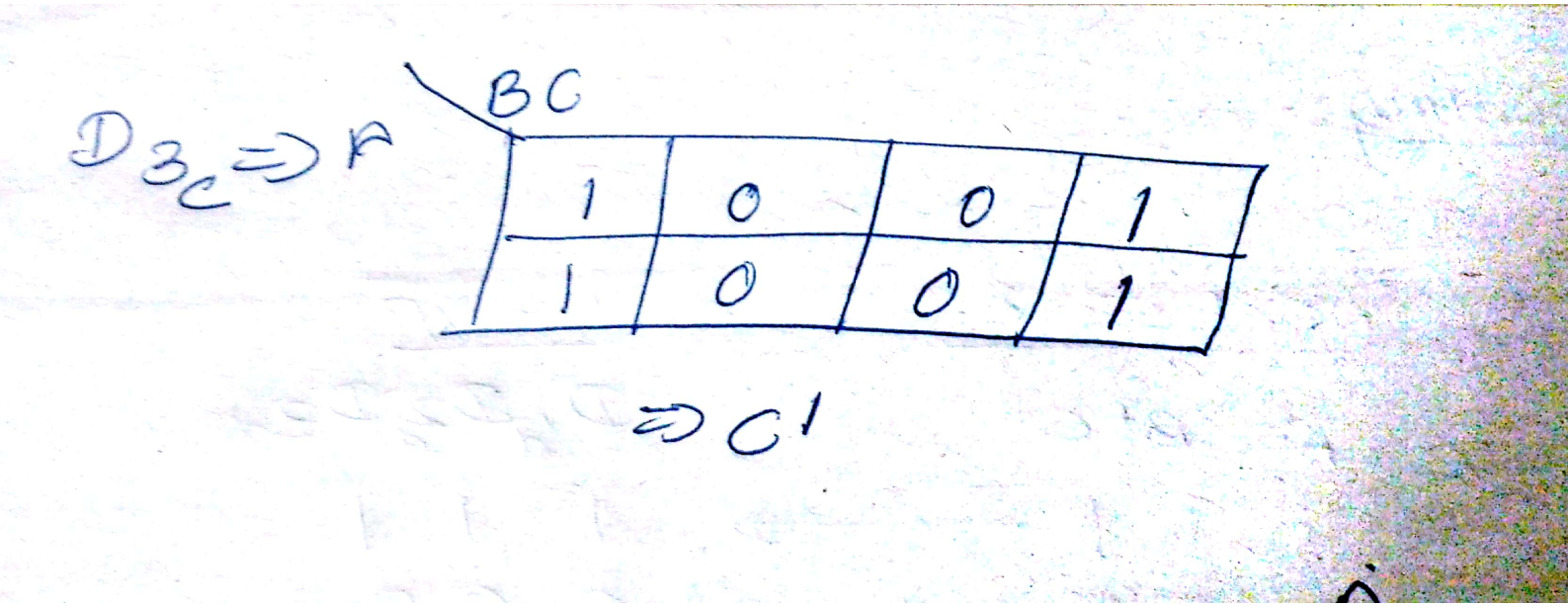
A \ BC				
1				
	1	1	1	

⇒ $A'BC + AC + AB$

D_{2C} ⇒

A \ BC				
1	0	1	0	
1	0	1	0	

⇒ $B\bar{C} + BC = B \odot C$



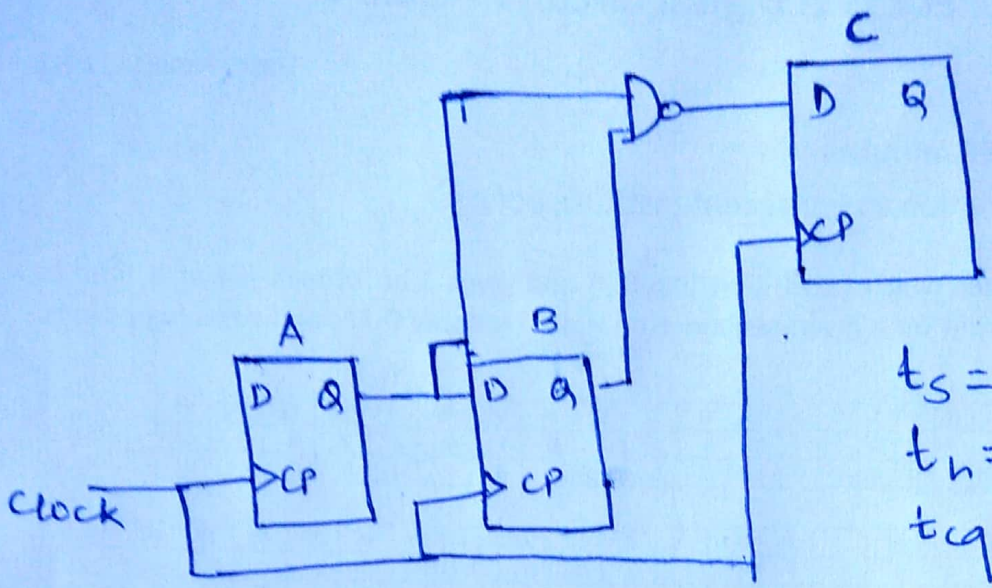
$\Rightarrow C_1$

now implementation →

mux will pass the logic of up count if $w=1$

and the logic of docun count if $w=0$.

C1.



$t_s = 30ps$.
$t_h = 20ps$.
$t_{cq} = 10ps$.
$t_{n1} = 50$.
$t_{clk} = 1/1GHz$
$= 1ns$.

Consider the path between FFB to FFC.

$t_{clk} \geq t_{cq} + t_{n1} + t_{setup}$.

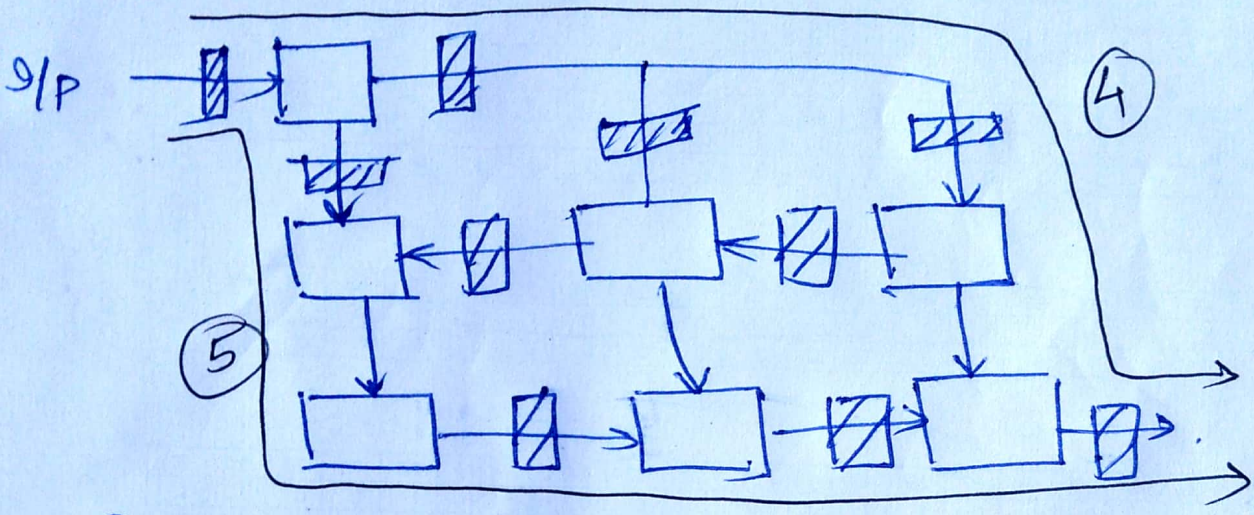
$10 + 50 + 30$.

$1ns \geq 90ps$ ∴ No setup Violation

Consider the path FFA to FFB.
As per Hold Def^n, data should be stable till 20ps (Hold time of FFB) after the clock edge. In above case, consider clock is arriving at both FFA & FFB at 10ns. then the Data at FFB should be present there for more 20ps to get captured. But it will be overwritten by FF_A data in 10ps as t_{cq} of FFA is 10ps.
∴ Hold Violation exists.

C_2.

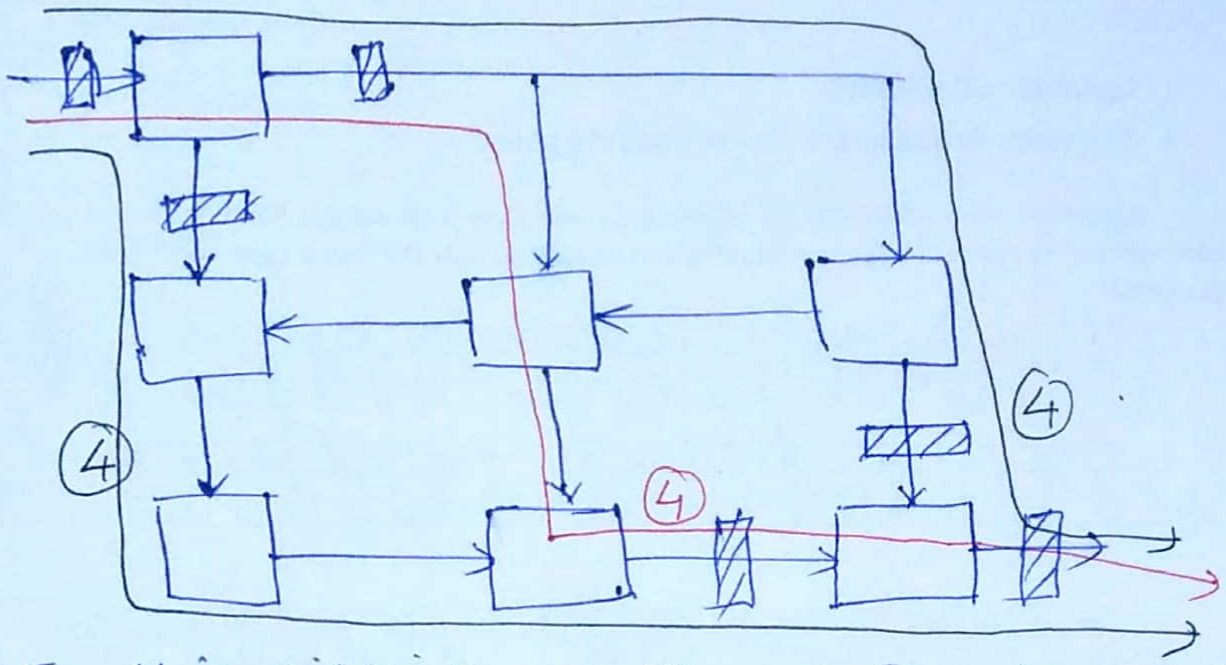
In circuit 1



for well formed k stage pipeline the no. of registers on ~~the~~ all the paths betw^n i/p and o/p should be same.

As they are not equal. Its not a well formed k stage pipeline.

In circuit 2.



In this circuit all the paths from i/p to o/p have same no. of registers.

~~But, for a well formed pipeline — Every pipeline stage, has a register on it's o/p & not on i/p.~~

~~∴ This circuit is not a wellformed pipelined circuit.~~

The circuit is well formed pipe line.
Now, The input at the circuit is with register, ~~xxxxx xxxx~~ It can be considered as pipeline register or can be ignored saying it to be o/p register of the circuit connected at the input of this circuit.

∴ Here k can be 3 or 4.