

INDRAPRASTHA INSTITUTE *of*

INFORMATION TECHNOLOGY

DELHI

Department

of

Electronics & Communication Engineering

ECE111|Digital Circuits

**Dr. Sudhanshu Shekhar Jamuar**

Lab\_8:

Student Name: Navidha Jain

Roll No.: 2020223

Date: 23/03/2021

Aim:

A) To verify the functionality of JK FlipFlop using the characteristic table and excitation truth table and its corresponding kmap.

B) To verify the functionality of D FlipFlop using the characteristic table and excitation truth table and its corresponding kmap.

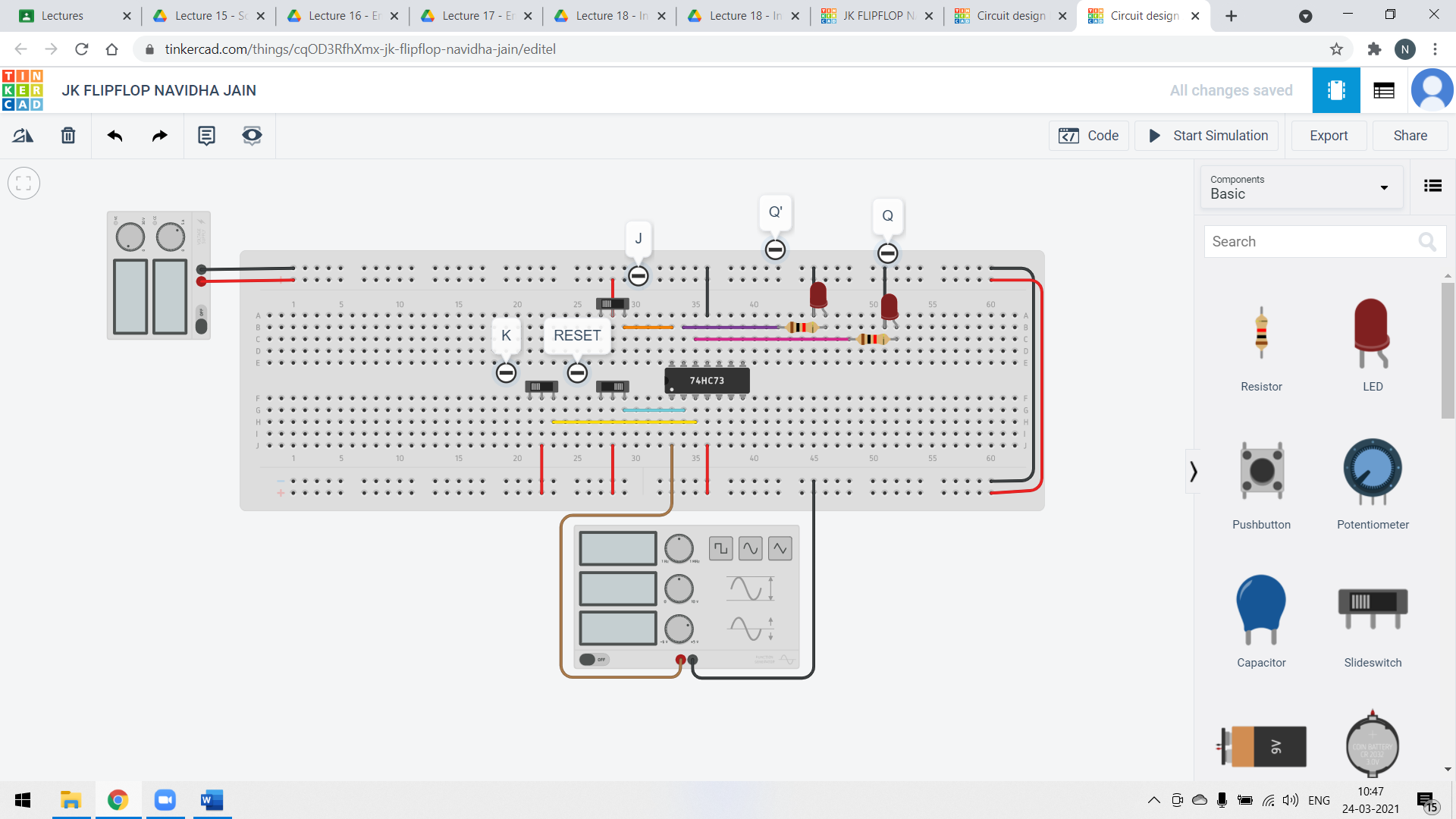
Components/ICs Used:

A) Breadboard, JK FlipFlop (74HC73), resistors, function generator, LEDs, supply, wires, slideswitches.

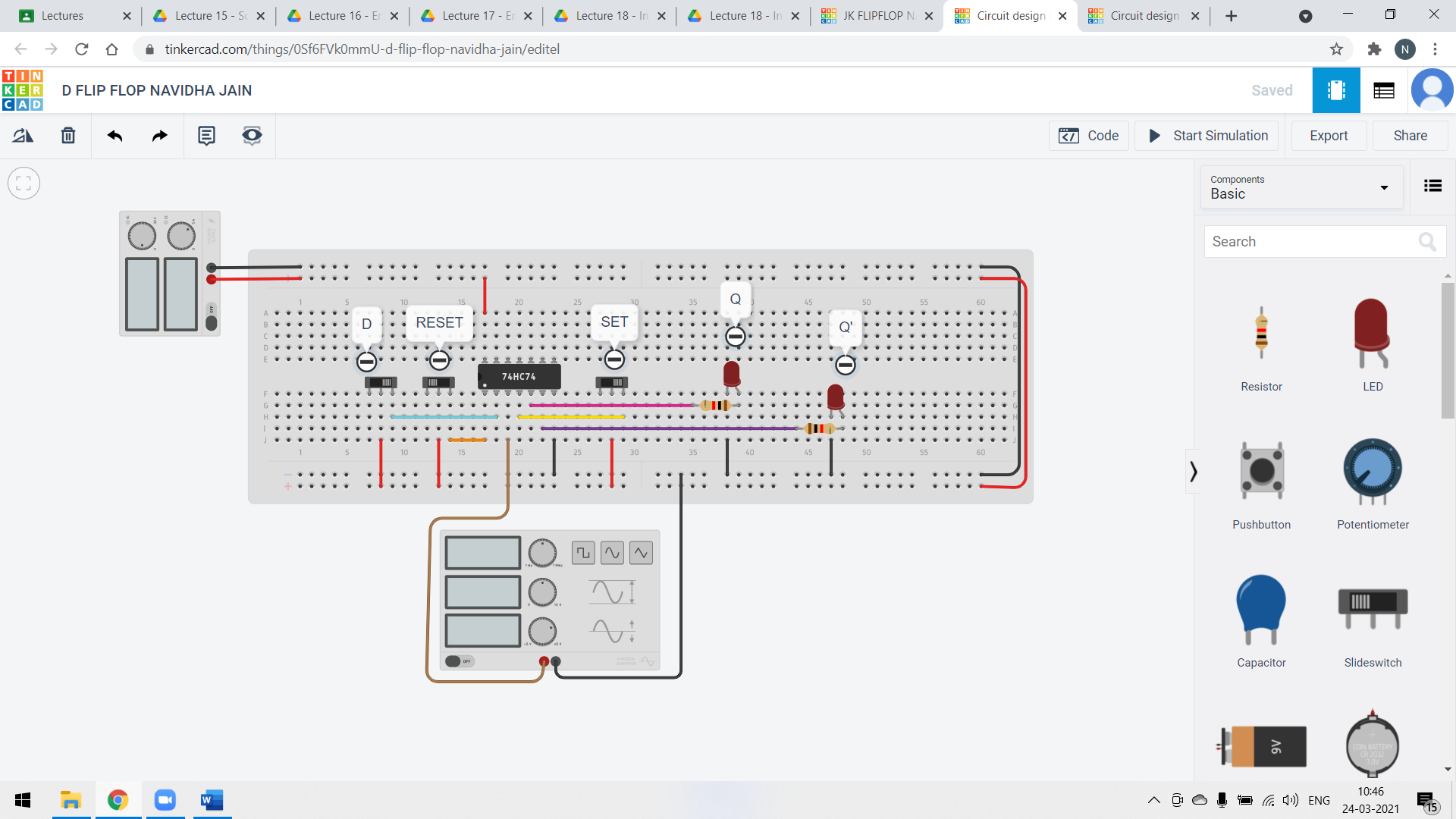
B) Breadboard, D FlipFlop (74HC74), resistors, function generator, LEDs, supply, wires, slideswitches.

Tinkercad screenshot:

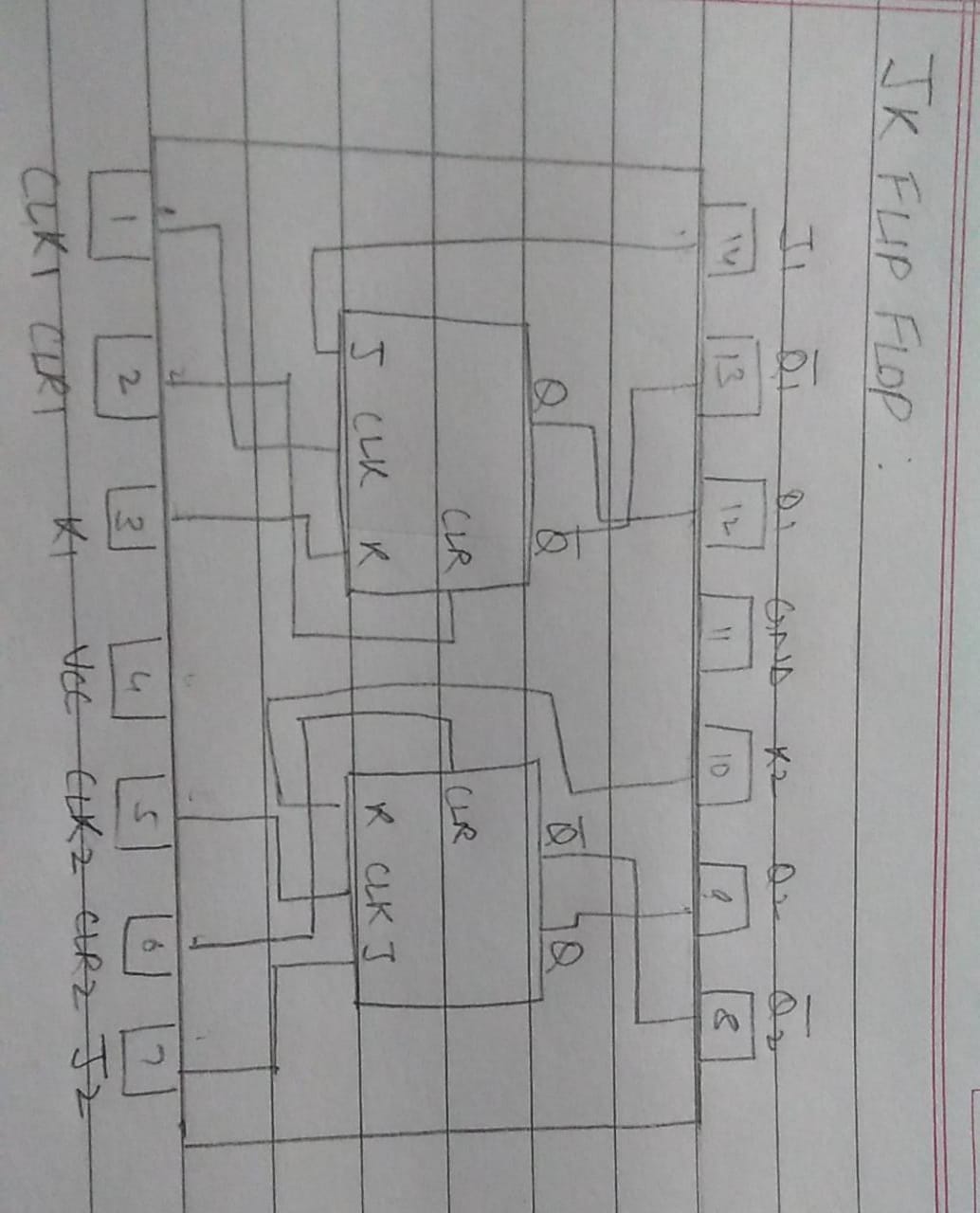
A)

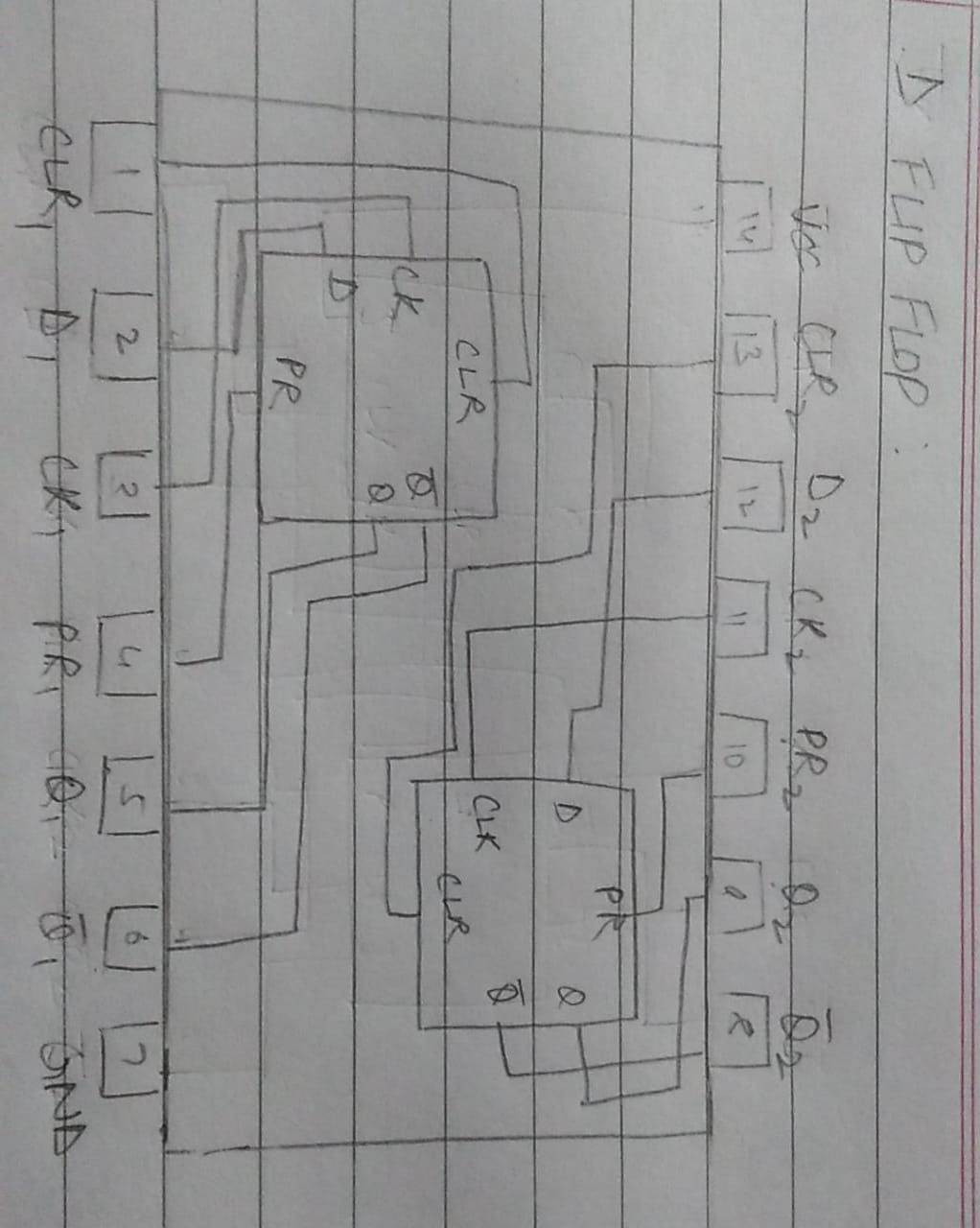


B)



Pin Configuration:

A)



B)

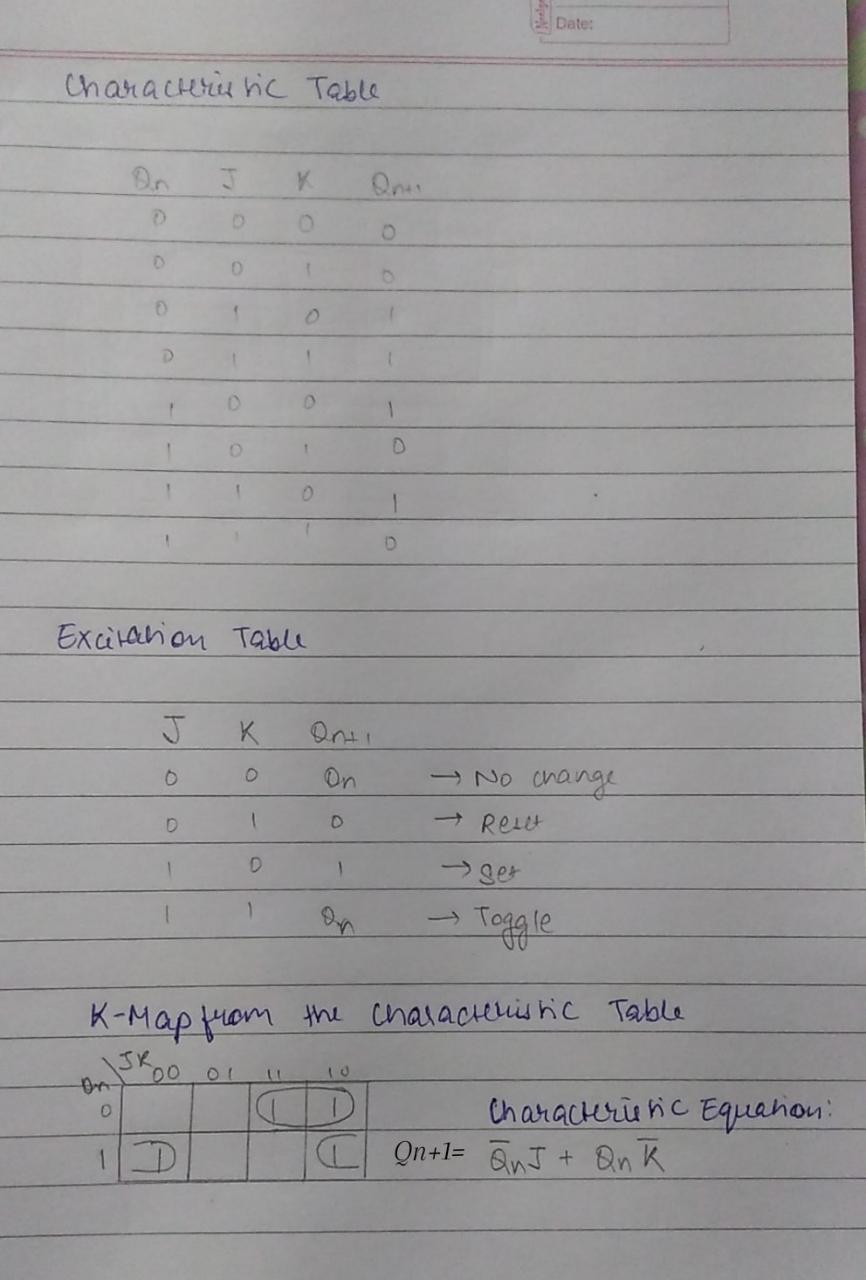
TinkerCad link:

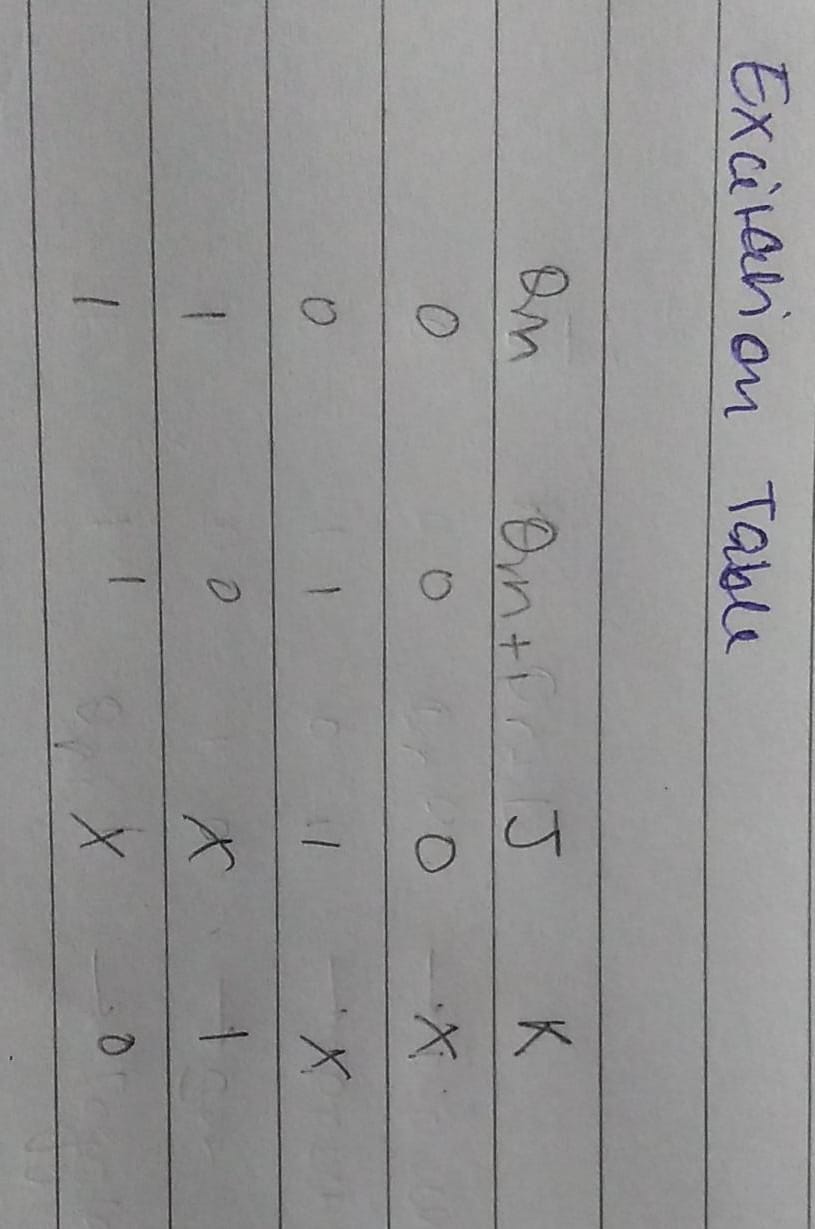
A) <https://www.tinkercad.com/things/cqOD3RfhXmx-jk-flipflop-navidha-jain/editel?sharecode=ul1VA9S5MOubh56ejBzih3Cpmws0_h5Z3HWyA8yX6U0>

B) <https://www.tinkercad.com/things/0Sf6FVk0mmU-d-flip-flop-navidha-jain/editel?sharecode=_9d_m45TzpfHxlCTi-CZ6b2HastIkTjnmTMXvGecQY8>

Truth Tables and Kmaps:

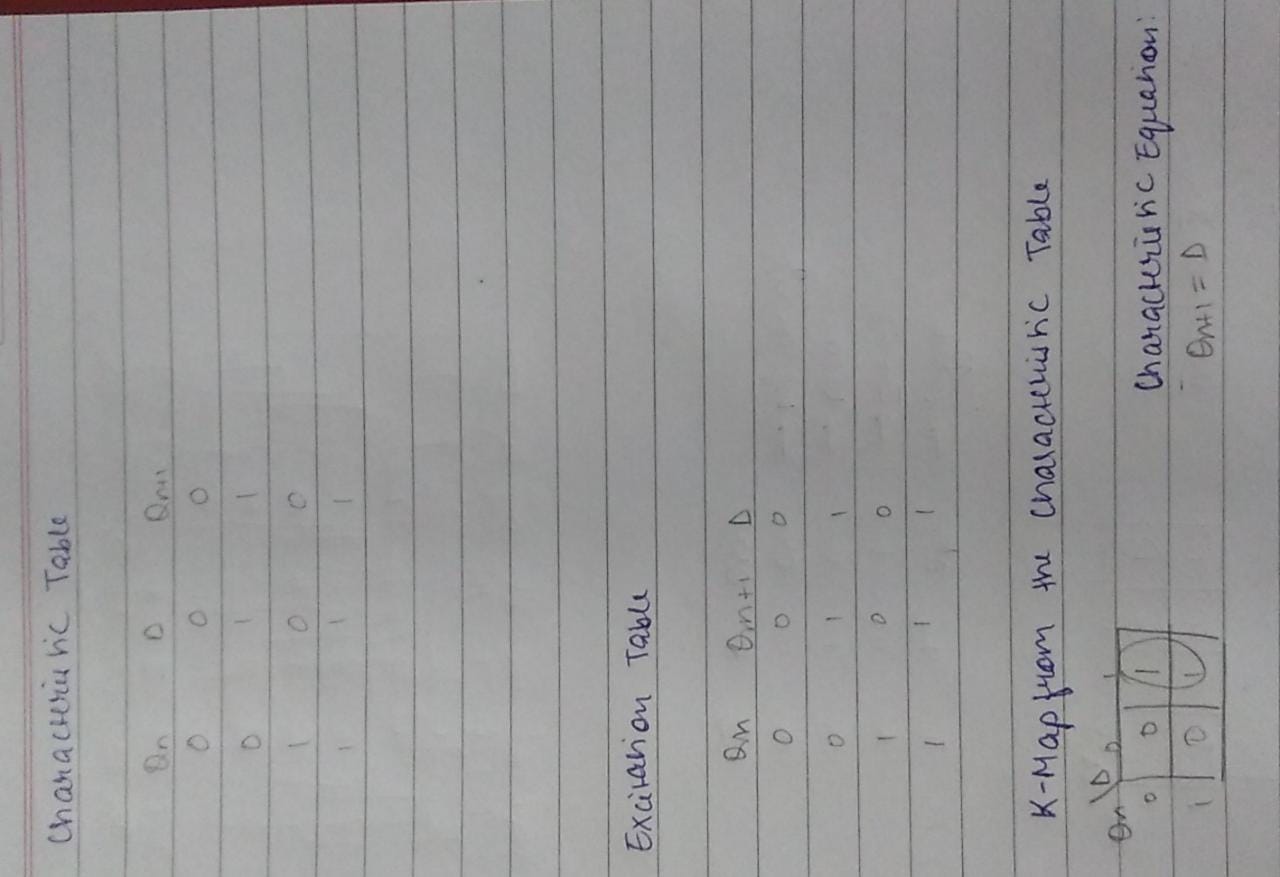
A)





---

B)



Justification:

A) The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic “1” in the NOR Gate flipflop and logic “0” in the NAND Gate flipflop. Due to this additional clocked input, a JK flip-flop has four possible output combinations, “logic 1”, “logic 0”, “no change” and “toggle” unlike the SR flip flop in which we had a forbidden state as well.

B) The D-type flip flop are constructed from a gated SR flip-flop with an inverter added between the S and the R inputs to allow for a single D (Data) input. If this data input is held HIGH the flip flop would be “SET” and when it is LOW the flip flop would change and become “RESET”.

Observations:

We have verified the functionality of the JK FlipFlop and D FlipFlop using the truth tables and kmaps above.

Applications of the experiment:

A) JK FlipFlop:

-used in Counters, Registers, frequency divider, Sequence detector, Shift Registers, Data storage, Data transfer, Counters, Frequency Dividers, Bounce elimination [switch](https://www.theengineeringprojects.com/2019/10/transistor-as-a-switch.html), Storage Registers, etc.

- used in electronic circuits with the main aim to store the state information of the device.

B) D FlipFlop:

-used to create delay-lines which are used in digital signal processing systems.

-used as a Frequency Divider.

-used to create delay-lines which are used in digital signal processing systems.

-used as event detectors.

Sources referred:

<https://www.electrical4u.com/application-of-flip-flops/#:~:text=D%20flip%2Dflop%20can%20be,delayed%20by%20one%2Dclock%20cycle>.

<https://www.electronics-tutorials.ws/sequential/seq_4.html>