Navid Mir

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Education

ELECTRICAL AND COMPUTER ENGINEERING M.S. | *UNIVERSITY OF CALIFORNIA, LOS ANGELES (UCLA)* JUNE '23
- 3.95 GPA
- Emphasis on *Circuits and Embedded Systems*

ELECTRICAL ENGINEERING B.S. | *UNIVERSITY OF CALIFORNIA, SANTA BARBARA (UCSB)* JUNE '21
- 4.0 GPA
- Emphasis on *Digital Hardware Design* and *Digital Signal Processing (DSP)*
- 11 x Dean's Honors List for Engineering, College of Engineering Honors, Tau Beta Pi Honors, Outstanding EE Senior Award
- Activities: Undergraduate Research in Signal Processing, IEEE UCSB Chapter, Intramural Basketball, Pop's Orchestra

Work Experience

MODEM HW DESIGN INTERN | *QUALCOMM* JUNE '22 – SEPTEMBER '22
- Worked on 5G modem PDSCH decoding block implementation on custom DSP core using assembly instruction set
- Implemented descrambling, de-interleaving, de-rate matching and HARQ using 38.212 3GPP specification
- Analyzed throughput and provided recommended instructions to add to enhance performance by 8X

EMBEDDED SYSTEMS ENGINEER | *METROTECH* JUNE '21 – JUNE '22
- Wrote C firmware to interface with new sensor in embedded system
- Designed new mixed-signal circuit board using Altium Designer
- Updated analog front end and adding desired functionality from scratch, centered around new processor

ASIC VERIFICATION INTERN | *WESTERN DIGITAL* JUNE '20 – AUGUST '20
- Worked on automation tool for verification of ASIC SSD flash controller used in conjunction with Cadence verification tools
- Wrote SystemVerilog UVM testbenches for error correction code module

ELECTRICAL ENGINEERING INTERN | *METROTECH* JULY '19 – SEPTEMBER '19
- Tested and optimized RFID transmitter circuit to attain required antenna output power while maximizing efficiency
- Used Altium Designer for PCB design of several configurations of RFID transmitter circuit
- Designed efficient high voltage switching power supply for D-class amplifier, controlled with C code on ARM-based MCU

Projects

A portfolio of my projects can be found at my website: navidmir.com

MACHINE LEARNING HARDWARE ACCELERATOR | *ECE M216A: VLSI SYSTEMS* NOVEMBER '21 – DECEMBER '21
- Wrote Verilog RTL for neural network to perform number classification from images (trained with MNIST dataset)
- Performed synthesis using Synopsys Design Compiler and verified design with ModelSim gate-level simulation
- Optimized design for minimum power and area and performed word-length simulation

BINARY MULTIPLIER IC DESIGN | *ECE 120B: SEMICONDUCTOR DEVICE PROCESSING II* APRIL '21 – JUNE '21
- Fabricated 2 by 2 binary multiplier, inverter, NAND, common-source amplifier circuits with 100 um x 20 um NMOS
- Designed photolithography mask for circuits and fabricated in clean room

Skills

SOFTWARE: Verilog, Cadence Virtuoso, Assembly, Altium Designer**,** C/C++, Python, MATLAB, Java, Linux, Git, Jira, LTspice

HARDWARE: Analog and digital circuit design, embedded systems, microcontrollers (Raspberry Pi, Arduino), FPGAs, oscilloscopes, spectrum analyzers, through-hole and surface mount soldering

Awards

EXCELLENCE IN ELECTRICAL ENGINEERING | *UCSB CAPSTONE PROGRAM* JUNE '21

JOSEPH SAYOVITZ SCHOLARSHIP | *UCSB COLLEGE OF ENGINEERING* JANURARY '21

TBP SCHOLARSHIP | *TAU BETA PI (TBP) ENGINEERING HONORS SOCIETY* JUNE '20