Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

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Course Number:	**ELE 404**
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Instructor:	Fei Yuan

Assignment/Lab Number:	**8**
Assignment/Lab Title:	**Amplifier Design Project**

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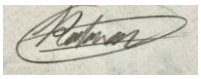
Rahman	Taskin	500973553	11	

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Objective

The objective of this Design Project was to build a BJT amplifier circuit that meets the following specifications:

- Power Supply: +**10V** relative to the ground;
- Quiescent current drawn from the power supply: **no larger than 10mA;**
- No-load voltage gain (at 1kHz): $|\boldsymbol{A_{vo}}| = \mathbf{50}(\pm\mathbf{10}\%)$**;**
- Maximum no-load output voltage swing (at 1kHz): **no smaller than 8V peak to peak;**
- Loaded voltage gain (at 1kHz and with $R_L = 1k\Omega$): **no smaller than 90% of the no-load voltage gain;**
- Maximum loaded output voltage swing (at 1kHz and $R_L = 1k\Omega$): **no smaller than 4V peak to peak;**
- Input resistance (at 1kHz): **no smaller than 20kΩ;**
- Amplifier type: **inverting or non-inverting;**
- Type of transistors: **BJT;**
- Number of transistors (stages): **no more than 3;**
- Resistances permitted: **values smaller than 220kΩ from the E24 series;**
- Capacitors permitted: **0.1uF, 1uF, 2.2uF, 4.7uF, 10uF, 47uF, 100uF, 220uF;**
- Other components (BJTs, diodes, Zener diodes etc.): **only from your ELE404 lab kit.**
- Source resistance must be 600Ω for all tests.

Description

The configuration of the circuit I chose is a CC stage followed by CE, which is followed by another CE stage. I chose this circuit to easily achieve the desired gain of amplifier circuit that was specified. I chose the CC stage to be the first stage to meet the required input resistance. Common-collector amplifier circuits have high input resistance and low output resistance which is why I chose the CC amplifier to be

the initial stage. For the second and third stage I chose a CE amplifier to reach a high voltage gain of 50. The second stage amplified the signal by about 5. This gain was then further amplified by about 10 by the CE amplifier in the third stage with total gain being around 50. The full amplifier circuit can be found in Figure 1.

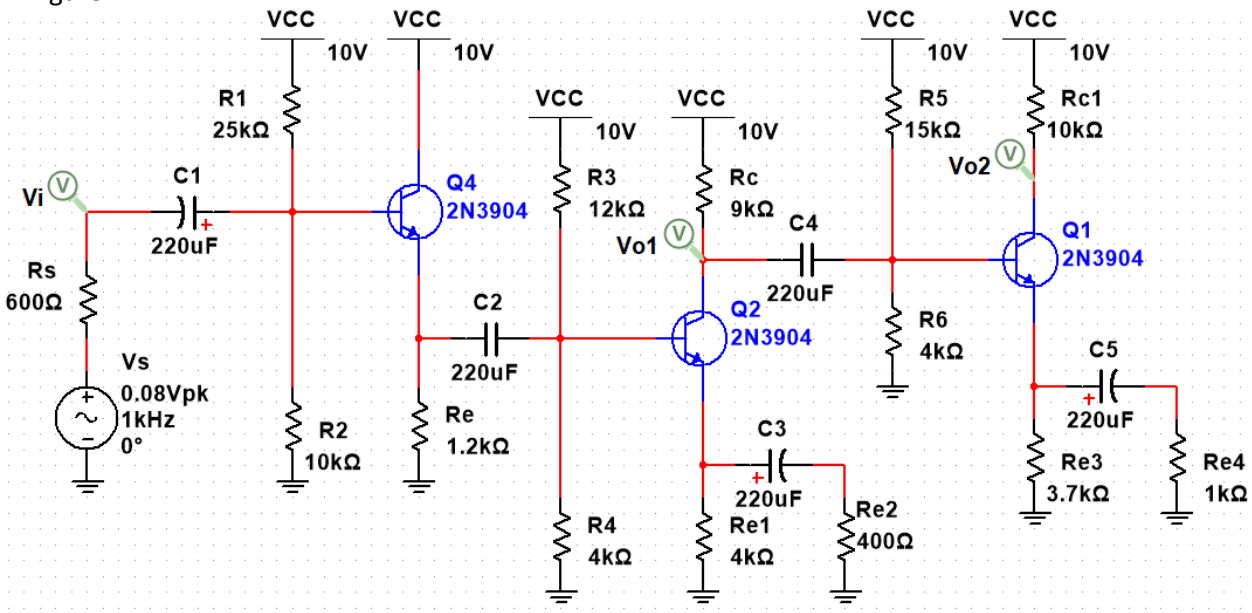

Figure 1: Complete CC-CE-CE BJT amplifier circuit.

Manual Calculations

Note: For some of the stages the values differ from the manual calculations this was done to avoid distortions in the graph.

P1

EIE404 Design Project

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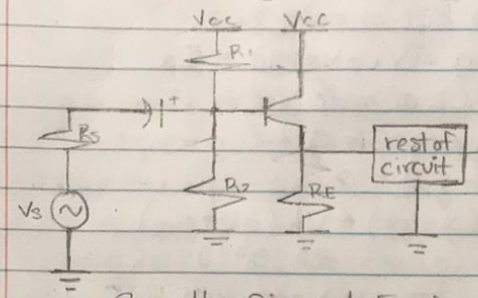
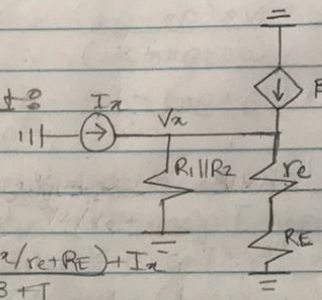
18/04/2021

1) The First Stage: CC Amplifier



• The purpose of this amplifier circuit to attain the required input resistance. So we simply dc bias it in the active region.

Small-Signal Equivalent:



KCL @ node V_x:

$$V_x/r_e+R_E + V_x/(R_1\|R_2) \neq \beta I_B + I_x$$

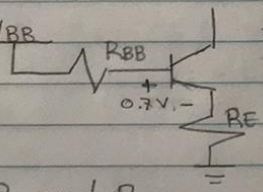
$$\Rightarrow V_x\left[1/r_e+R_E+(R_1\|R_2)\right] = \beta\left(\frac{V_x}{r_e+R_E}\right)+I_x$$

$$\Rightarrow \frac{V_x}{r_e+R_E}\left(1-\frac{\beta}{\beta+1}\right) + V_x/R_1\|R_2 = I_x \Rightarrow V_x\left[\left(\frac{1-\beta/\beta+1}{r_e+R_E}\right)+\left(\frac{1}{R_1\|R_2}\right)\right] = I_x$$

$$\Rightarrow V_x/I_x = R_{in} = 1/\left[\left(\frac{1-\frac{\beta}{\beta+1}}{r_e+R_E}\right)+(1/R_1\|R_2)\right]$$

$r_e = V_T/I_B(\beta+1) \Rightarrow V_{BE} = V_B - V_E = 0.7V$

$V_{BB} = V_{CC}(R_2/R_1+R_2)$



$\Rightarrow V_{BB} - I_B R_{BB} - 0.7V - I_B(\beta+1)R_E = 0$

$\Rightarrow V_{BB} - 0.7V = I_B\left[R_{BB}+(\beta+1)R_E\right]$

$\Rightarrow I_B = (V_{BB}-0.7V)/\left[R_{BB}+(\beta+1)R_E\right]$

• If we pick resistor values in the kΩ range for R_1 and R_2. It will no longer matter what our DC bais voltage is as it will barely change our base current. As long as we choose a DC bias voltage that is well above 0 we should have a successfull CC amp.

Lets take R_1 and R_2 to be 56kΩ and 45kΩ respectively.

Then our base current will be:

$V_{BB} = V_{cc}(45k\Omega / 56k\Omega + 45k\Omega) \simeq 4.455V \Rightarrow R_{BB} = R_1R_2/R_1+R_2 \simeq 24.95k\Omega$

$I_B = V_{BB} - 0.7V / [24.95k\Omega + (101)R_E]$

• We want R_E to be small because when we cascade the multiple stage together the small signal equivalent circuit's eqn for I_B becomes: $I_B = V_{BB} - 0.7V / [R_{BB} + (101)(R_E \| R_L)]$.

If R_E is small then I_B is small and so it does not affect re. Lets take R_E to be 1.2kΩ, then

$I_B = V_{BB} - 0.7V / [24.95k\Omega + (101)(1.2k\Omega)] = 25.6927\mu A$

$r_e = V_T / I_B(\beta+1) = 10.02\Omega.$

$R_{in} = 1/\left[\left(1 - \frac{\beta/\beta+1}{r_e + R_E}\right) + (1/R_{BB})\right] = 1/[8.1825\mu\Omega + 40.08\mu\Omega]$

$\simeq 20.72k\Omega$

The gain of the CC Amp:

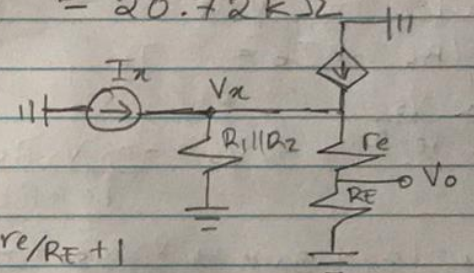
KCL @ node V_o:

$V_o/R_E + V_o - V_x/r_e = 0$

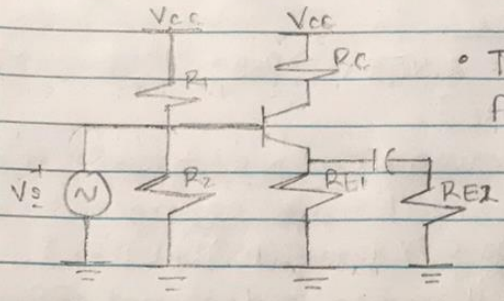
$V_o(1/R_E + 1/r_e) = V_x/r_e$

$\Rightarrow V_o/V_x = 1/r_e(1/R_E + 1/r_e) = 1/r_e/R_E + 1$

$\Rightarrow V_o/V_x = R_E \| r_e / r_e \simeq 0.9917$ ∴ The gain is about 1.

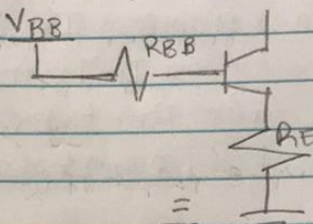


P2) The Second and Third Stage:



• This amplifier provides the first stage of the gain.

Voltage Divider:



$V_{BB} = V_{cc}(R_2/(R_1+R_2))$

$R_{BB} = R_1 \| R_2$

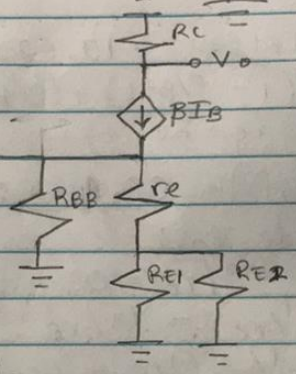
Small Signal Equivalent:

$R_E = R_{E1} \| R_{E2}$

KCL @ node V_o:

$V_s/R_c = -\beta I_B = \frac{\beta}{\beta+1} I_E$

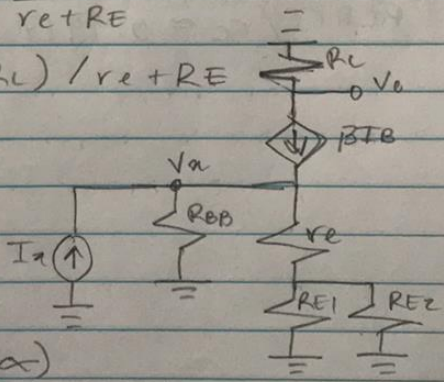
$= -\alpha \frac{V_s}{r_e + R_E} \Rightarrow V_s = -\frac{\alpha V_s R_c}{r_e + R_E}$



No-load gain $\Rightarrow V_o/V_s = \frac{-\alpha R_c}{r_e + R_E}$

Loaded-gain:

$\Rightarrow V_o/V_s = -\alpha(R_c \| R_L)/(r_e + R_E)$



Input Resistance

$R_{in} = V_a/I_a$

KCL @ node V_a:

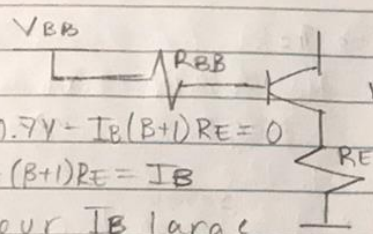
$I_a = V_a/R_{BB} + I_E(1-\alpha)$

$= V_a/R_{BB} + V_a/(r_e + R_E)(1-\alpha)$

$= V_a/R_{BB} + V_a/(r_e + R_E)(1 - \beta/(\beta+1)) = V_a/R_{BB} + V_a/(r_e+R_E) \cdot (1/(\beta+1))$

$\Rightarrow V_a/I_a = R_{in} = R_{BB} \| (\beta+1)(r_e + R_E)$

KVL:



$V_{BB} - I_B R_{BB} - 0.7V - I_B(\beta+1)R_E = 0$

$\Rightarrow V_{BB} - 0.7 / R_{BB} + (\beta+1)R_E = I_B$

$\Rightarrow$ To keep our I_B large we need a relatively small R_{E1} in the kΩ range. Lets take $R_{E1} = 4k\Omega$, this is necessary to properly dc bias the CE Amp. Let's also take relatively small R_1 and R_2 to keep our I_B large, ($R_1 = 12k\Omega$, $R_2 = 4k\Omega$) so $R_{BB} = 3k\Omega$. We need a large I_B to decrease our r_e which will increase our gain. To increase our gain during AC signal lets take a small R_{E2} relative to R_C. $R_{E2} = 400\Omega$

$r_e = V_T / I_B(\beta+1)$

- Since we made sure to meet the required input resistance of 20kΩ for the full amplifier, we are no longer concerned about input resistance unless it affects the gain.

$V_{BB} = 10\left(\frac{4}{12+4}\right) = 1/4(10) = 0.4V$

$I_B = \frac{3.3V}{3k\Omega + 101(41\Omega 0.4)} \cong 0.08306636mA$

$r_e = \frac{0.026V}{8.389702517} = 3.099\Omega$

$A_{V_0} = -\alpha \frac{R_C}{r_e + R_E} = \frac{-\alpha R_C}{366.7\Omega} \Rightarrow A_{V_L} = \frac{-\alpha(R_C \| R_L)}{366.735\Omega}$

To Avoid distortions we take $R_C = 9k\Omega$.

$A_{V_0} \cong 24.2979 \Rightarrow A_{V_L}$ depends on the input resistance of the Third Stage. We will calculate this gain after taking that input resistance

Input Resistance of Third Stage CE Amp:

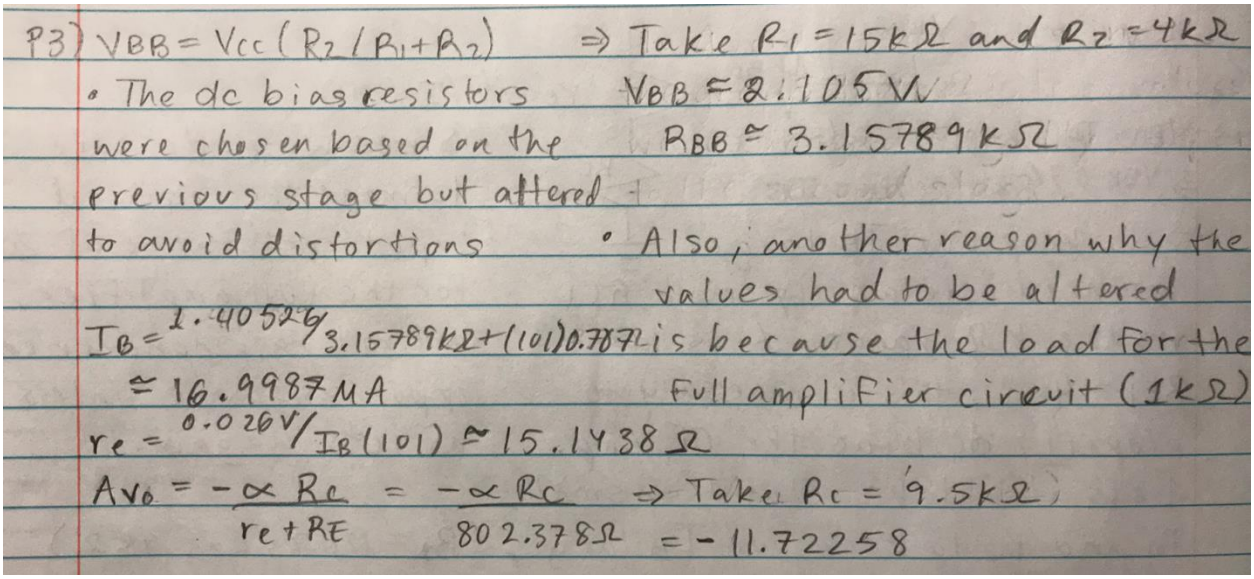
$R_{in} = R_{BB} \| (\beta+1)(r_e + R_E)$

$R_{in} = 2.9679 \| (101)(15.1438\Omega + 787.23\Omega)$

$= 2.9679 \| 81.04 = 2.863 k\Omega$

A_{V_L} of stage 2: $\frac{-\alpha(9k\Omega \| 2.863k\Omega)}{366.735\Omega} \cong -5.864$

P3



Experimental Results

E1

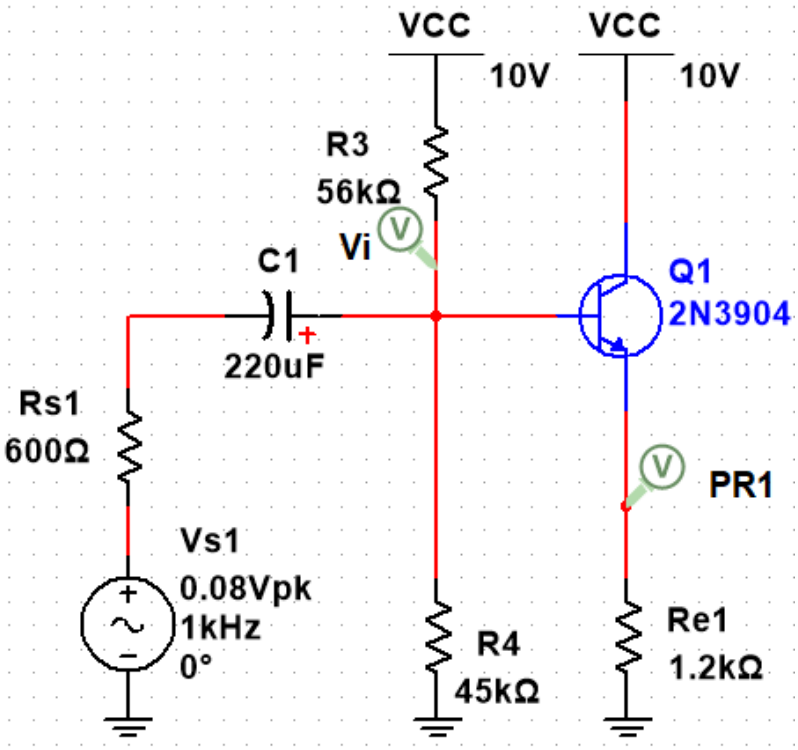


Figure 2: Stage 1 CC-Amplifier circuit.

Stage 1: CC Amplifier Graph

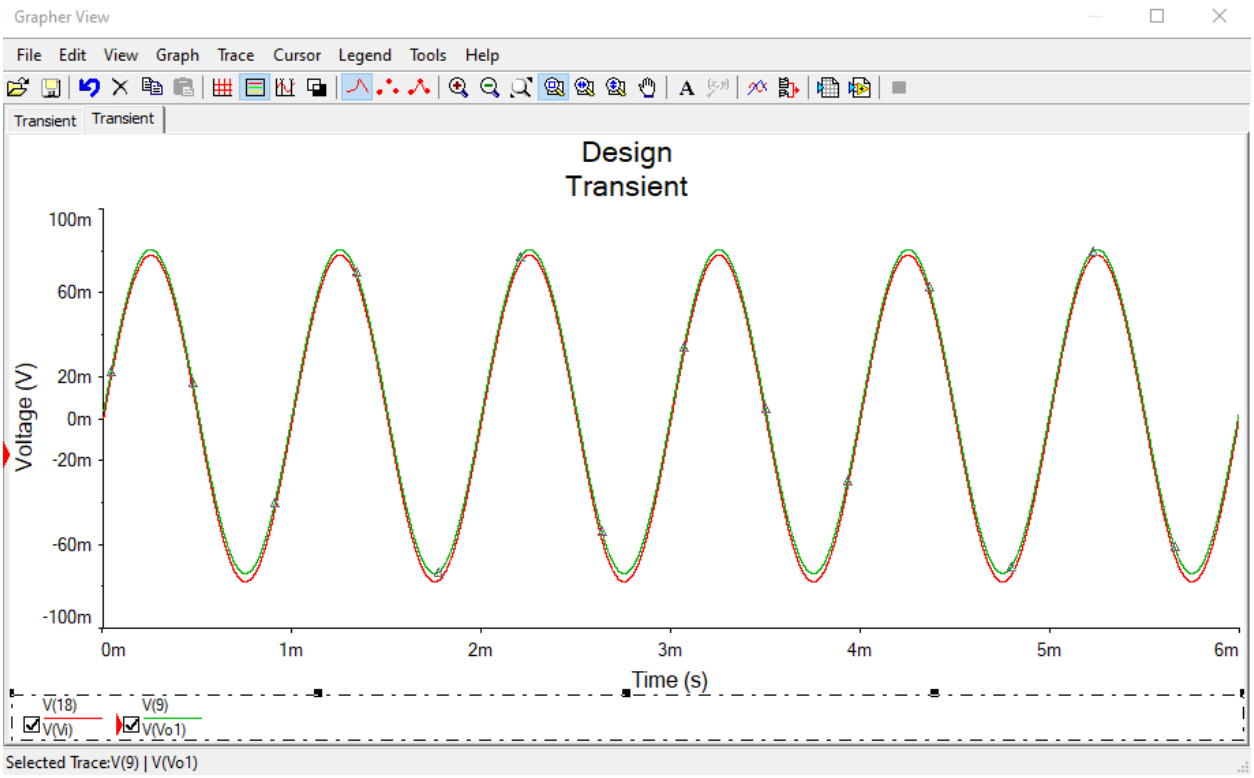


Figure 3: Input and Output voltage waveforms of stage 1 amplifier seen in Figure 2.

The manual calculations in this stage agree with the experimental results, as the gain of amplifier is about equal to 1.

E2

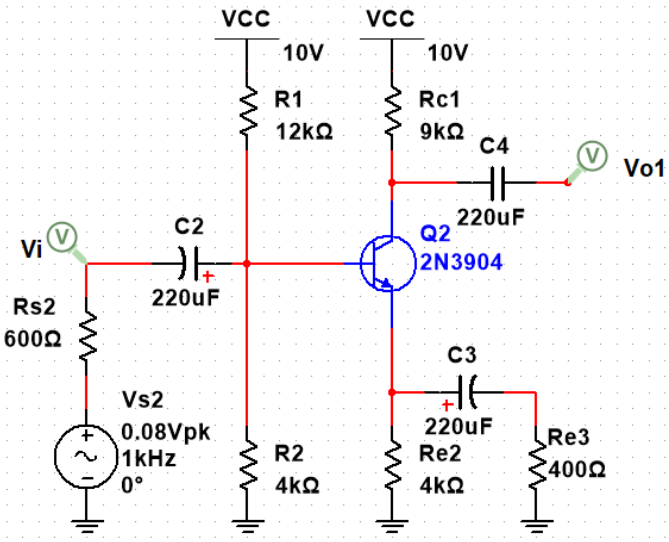


Figure 4: Stage 2 CE amplifier circuit.

Stage 2: CE Amplifier Graph

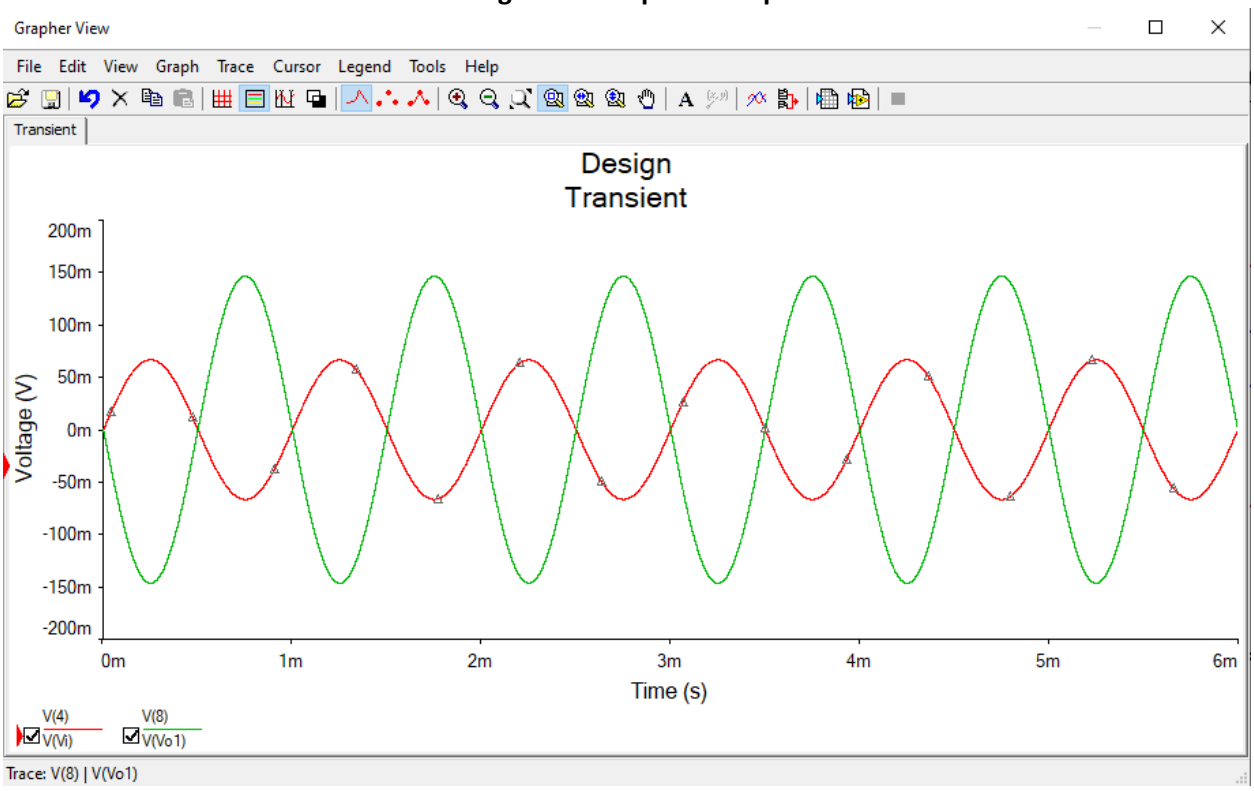


Figure 5: Input and Output waveforms of Stage 2 CE amplifier as a function of time.

E3

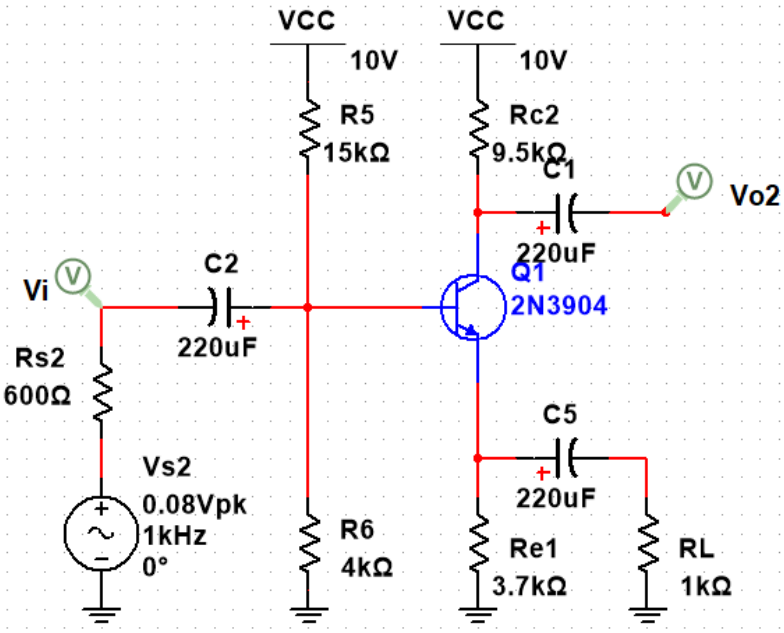


Figure 6: Stage 3 CE Amplifier circuit.

Stage 3: CE Amplifier Graph

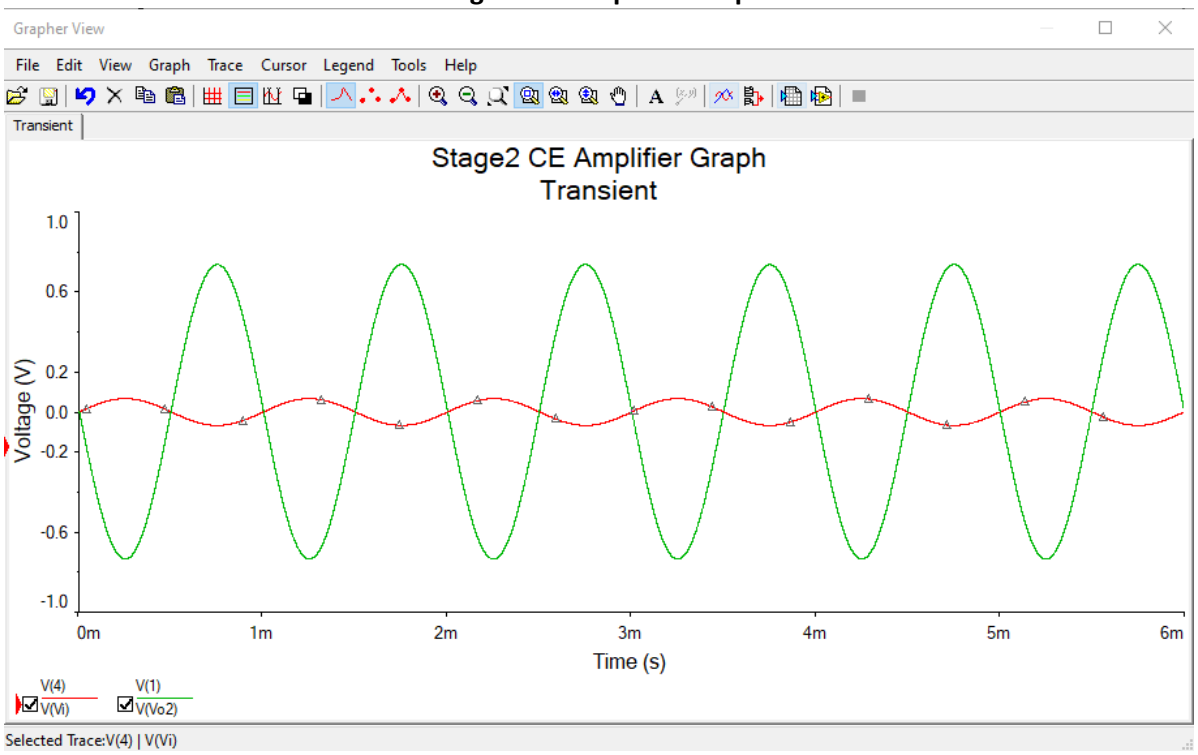


Figure 7: Input and Output waveforms of CE amplifier in Figure 6 as a function of time.

E4

Full Amplifier Circuit Graph

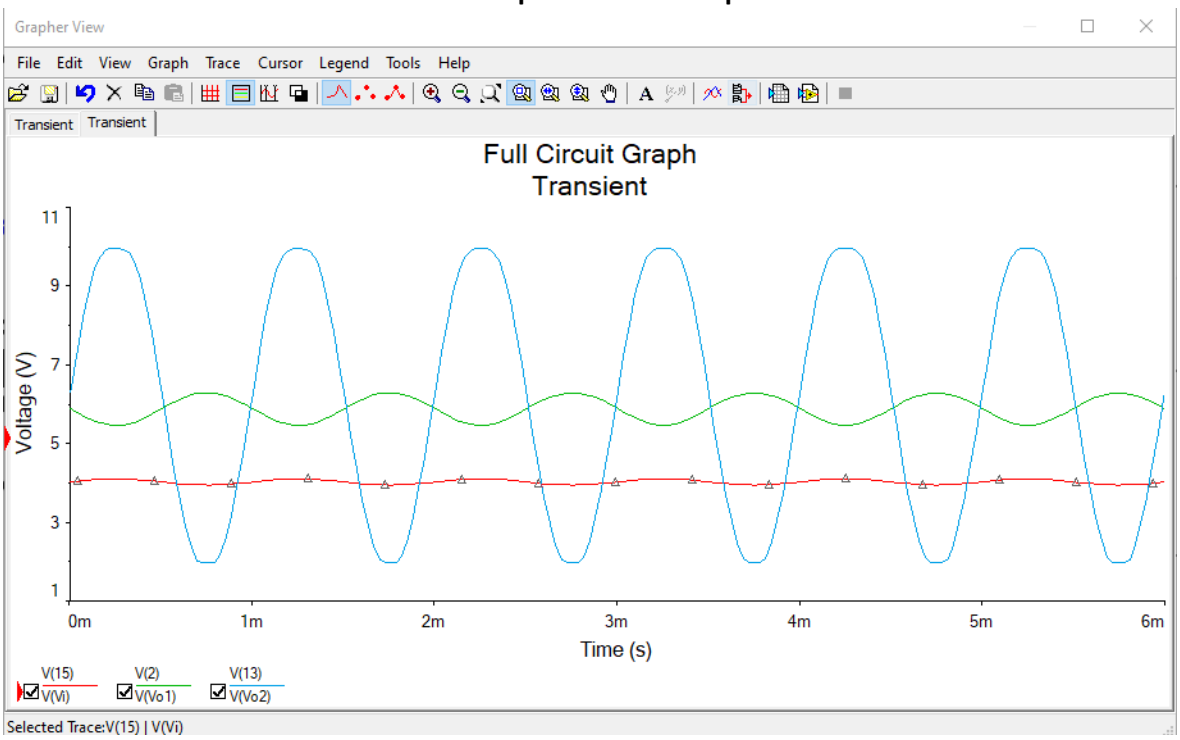


Figure 8: Input and Output waveforms of both stage2 and stage3 circuits cascaded together with stage 1, from Figure 1.

Full Circuit Frequency Response

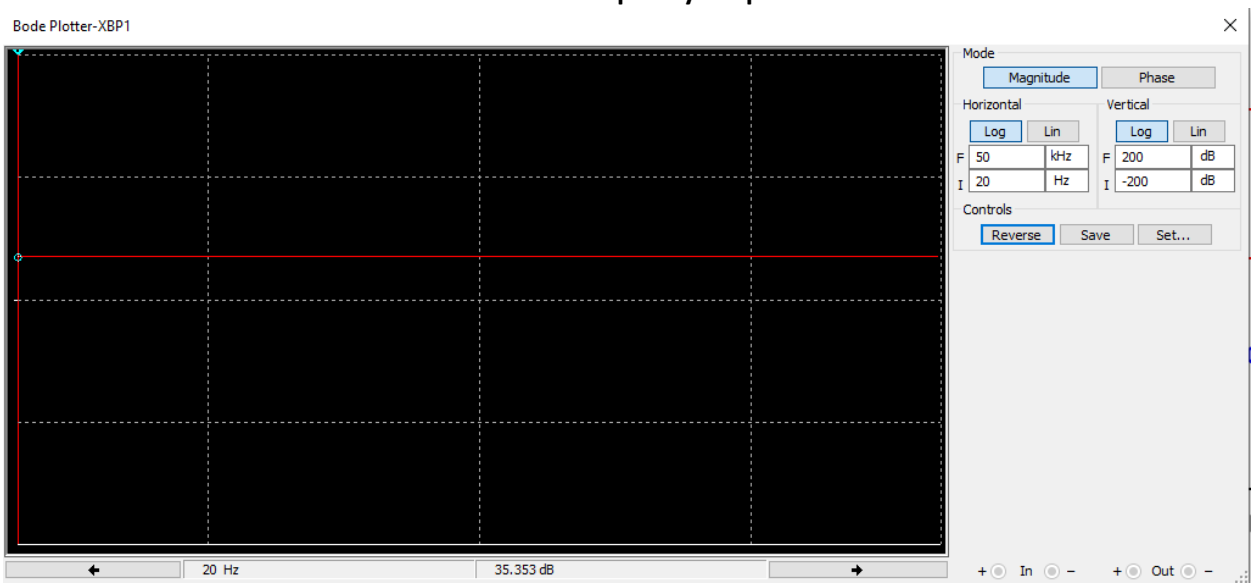


Figure 9: Frequency response of the amplifier circuit from 20Hz-50kHz.

Conclusion and Remarks

I can verify that the circuit meets the required standards, although there were slight discrepancies in the waveforms as the final output waveform was slightly distorted. Although the rest of the circuit seems to meet the required standards.

Compared to the manual calculation the only stage that has identical values was the first stage (CC amplifier), this is because this stage was only used to meet the required input resistance of the circuit and was not impacted by the rest of the circuit very significantly because of the emitter resistance value.

The CE amplifier in stage2 met the expected results from the manual calculations. If we look at the gain of the amplifier compared to the source waveform we see that the gain is consistent with the calculated value. The source waveform amplitude was about $77.7mV \pm 5mV$, and the output waveform of the 2nd stage amplifier was about $406mV \pm 5mV$. We can see that the amplitude increased by about 5.225, which is consistent with the calculated value of 5.864.

The CE amplifier in stage3 did not exactly meet the expected results from the manual calculations, and different resistor values were used to avoid distortions. The amplitude of the stage2 amplifier was $406mV \pm 5mV$, and the amplitude of the final output waveform was about $4V \pm 5mV$. We can see that the gain according to the experimental results was 9.8. The expected vs measured value of the gain is slightly off and this is mainly due to the minor distortion in the graph.