ELE404 Design Project W2021

Table of Contents

Prelab

Circuit Overview

For the project I decided to go with a CE-CC two stage configuration. The common-emitter amplifier was the main source on the voltage gain for the circuit, and then I used a common-collector amplifier to invert the gain. In the next section of the prelab, I will go over the calculations I followed in order to come up with he values for the circuit.

Figure P1

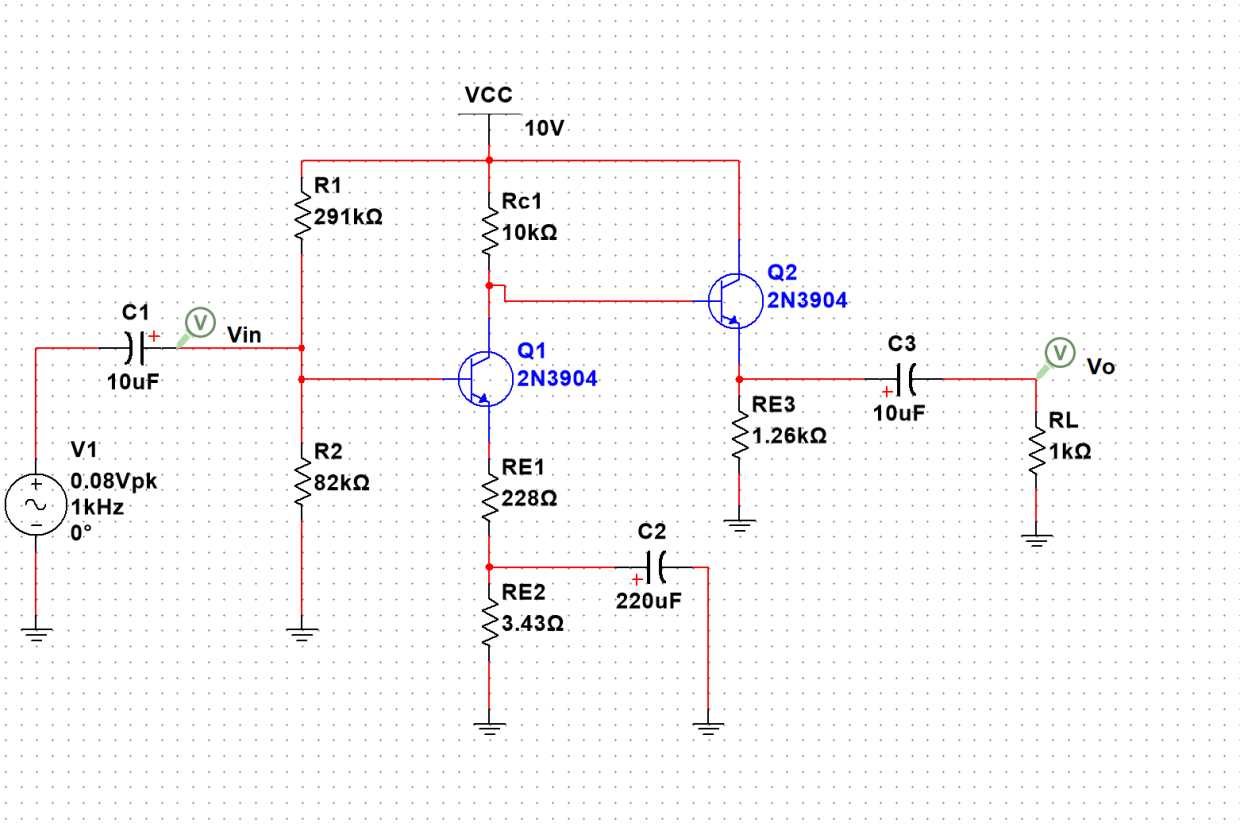
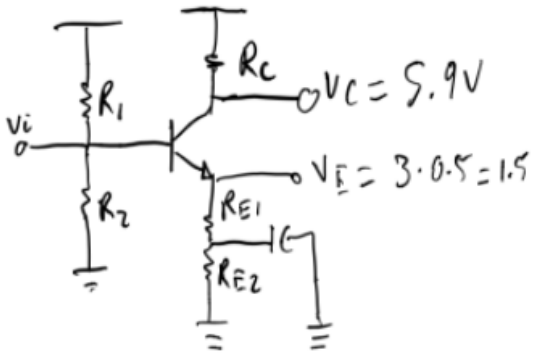


Figure P1: Circuit designed based on specifications provided for the project.

Manual Calculations

Design Calculations

Stage 1: CE



$V_C = 5.9V \quad S = \frac{1}{2}(10 + 1.5 + 0.3)$

$V_E = 3 \cdot 0.5 = 1.5$

Set $R_C = 10k\Omega$

$$I_C = \frac{10 - 5.9}{10k\Omega} \simeq 0.41\,mA$$

$$\rightarrow 1.5V = 0.41(R_{E1} + R_{E2})$$

$$R_{E1} + R_{E2} \simeq 3.66k$$

AC Analysis

$$R_i = r_{BE} + (\beta+1)R_{E1}$$

$$g_m = 40 I_C = 40(0.41) = 16.4\ mS$$

$$A_{V_0} = \frac{-g_m R_C}{1 + g_m R_{E1}}$$

$$50 = \frac{(16.4)(10)}{1 + (10)R_{E1}}$$

$$50 + 500 R_{E1} = 164$$

$$R_{E1} = 0.228\ k\Omega = 228\ \Omega$$

Recall $\rightarrow R_{E1} + R_{E2} = 3.66\ k$

$$R_{E2} = 3.432\ k\Omega$$

Constraint: $R_{in} \geq 20k\Omega$

$$\rightarrow R_i = \frac{\beta}{g_m} + (\beta+1)R_{E1} = \frac{100}{16.4} + (\beta+1)(0.228)$$

$$\boxed{R_i = 29.13\ k\Omega}$$

$$R_{in} = R_1 \| R_2 \| R_i$$

$$\frac{1}{20k} \leq \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{29.1k}$$

$$R_1 \| R_2 \geq \left(\frac{1}{20k} - \frac{1}{29.1k}\right)^{-1}$$

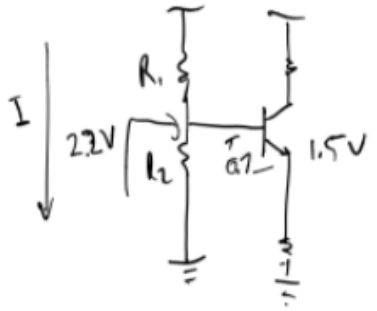
$$R_1 \| R_2 \geq 63.81\ k\Omega$$

$$I_B = \frac{I_C}{\beta} = 0.0041\ mA$$

$I_B << I_C$

$\rightarrow$ Set $R_1 \| R_2 = 64\ k\Omega$

$$\frac{R_1 R_2}{R_1 + R_2} = 64k \quad \cdots (1)$$



Voltage division

$$22 = \frac{10\ R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = 0.22 \quad \cdots (2)$$

sub ② into ①

$$0.22R_1 = 64k$$

$$\boxed{R_1 = 291k\Omega} \quad \cdots ③$$

sub ③ into ①

$$\frac{(291)R_2}{(291)+R_2} = 64$$

$$291R_2 = (64)(291) + 64R_2$$

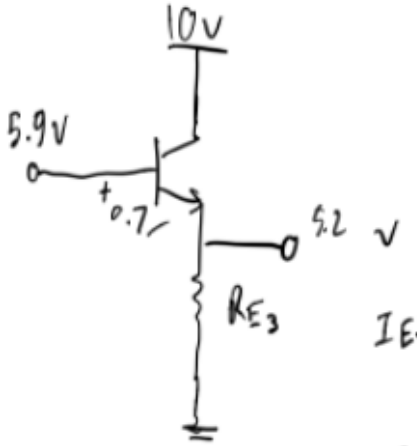
$$R_2 = \frac{(64)(291)}{(291-64)}$$

$$\boxed{R_2 = 82\,k}$$

Quiescent Current

$$I \approx \frac{10}{291+82} = 0.02\,mA = 20\,\mu A$$

Stage 2: CC



$$I_{E2} = (\beta+1) I_{B2}$$
$$\simeq 101 \left(\frac{0.41}{10}\right)$$
$$I_{E2} = 4.14 \text{ mA}$$

$$R_{E3} = \frac{5.2}{4.14} = 1.26 \text{ k}\Omega$$

$$g_{m2} = 40 I_C = 40(4.14) = 165.6 \text{ mS}$$

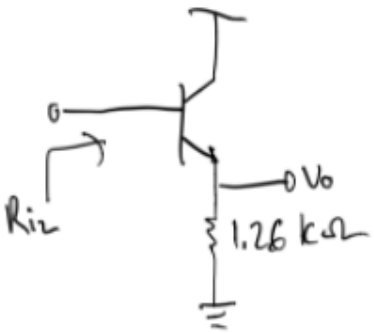
$$r_{BE} = \frac{1}{g_{m2}} = 6\ \Omega \qquad R_o = R_{E3} \,||\left(r_{BE} + \frac{R_C}{\beta+1}\right)$$

$$R_o = 1.26\text{k} \,||\, \left(6 + \frac{10\text{k}}{101}\right)$$

$$R_o = 1.26\text{k} \,||\, 0.105\text{k}$$

$$R_o = 97\ \Omega$$

Analysis



$$R_{in2} = r_{BE2} + (\beta+1)R_{E3}$$

$$= \frac{100}{165.6} + (101)(1.26)$$

$$R_{in2} = 128\ k\Omega$$

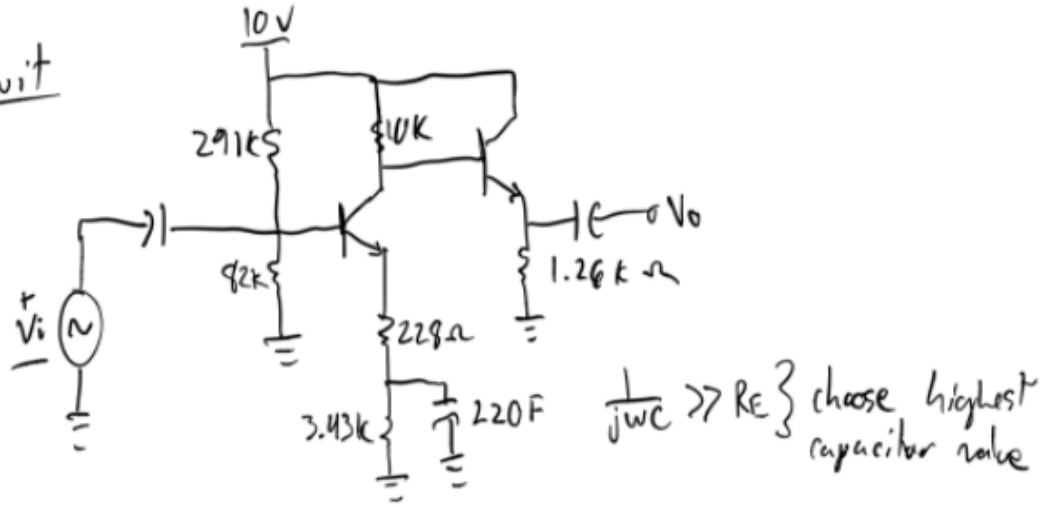
$$\frac{V_{c1}}{V_i} = \frac{-g_{m1}(R_C \| R_{in2})}{1 + g_{m1}R_{E1}} = \frac{-16.4\ (10 \| 128)}{1 + 16.4(0.228)} = \boxed{47.1}$$

$$\frac{V_o}{V_{c1}} = \frac{g_{m2}R_{E3}}{1 + g_{m2}R_{E3}} = \frac{(165.6)(1.26)}{1 + (165.6)1.26} = 0.995$$

$$A_{vo} = 47.1 \times 0.995 = 46.9$$

Final Circuit Design

Circuit



Experiment

Objective

The objective of this lab is to simulate the designed BJT circuit and check if the predicted theoretical results matched up with the simulated results. If there are any discrepancies, we will address them at the end of the lab in the conclusion section.

Simulation Results

This section covers the results from running various simulations option on Multisim. I have included transient, AC sweep, and DC transfer characteristic simulation results below. At the end I have also included screenshot of the results gathered from the probes.

Figure E1

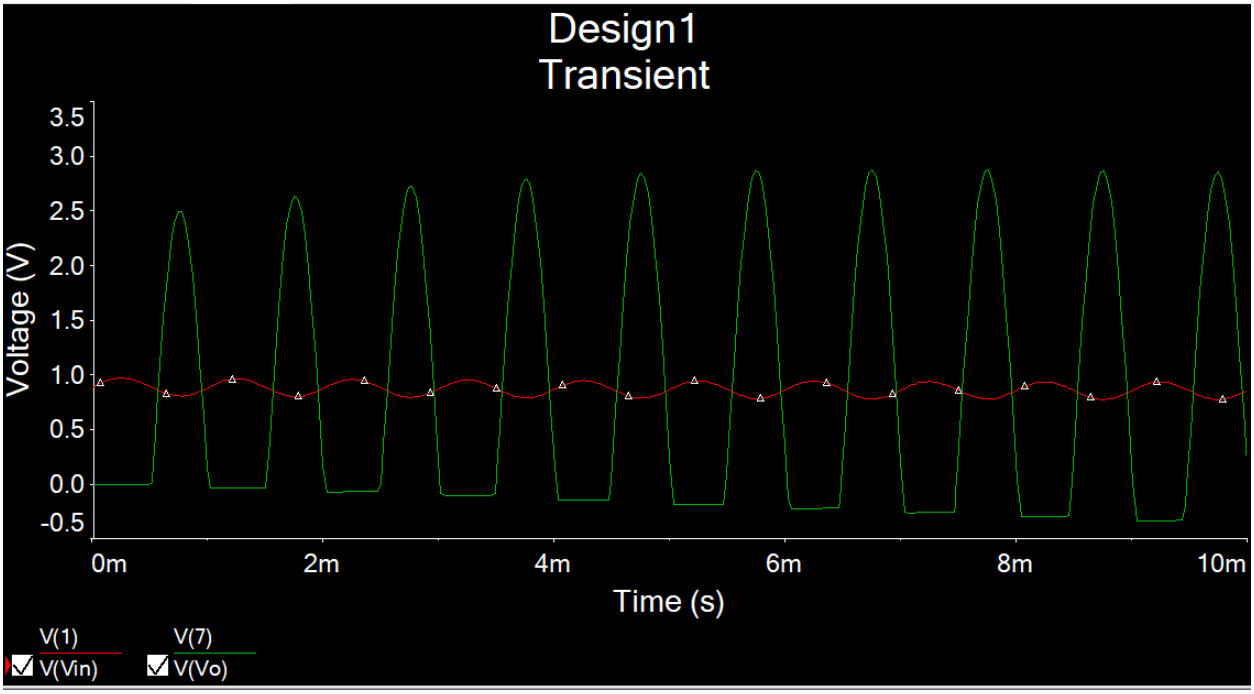


Figure E1: Includes the transient graph of both Vin and Vo of the two-stage (CE-CC) amplifier.

Figure E2

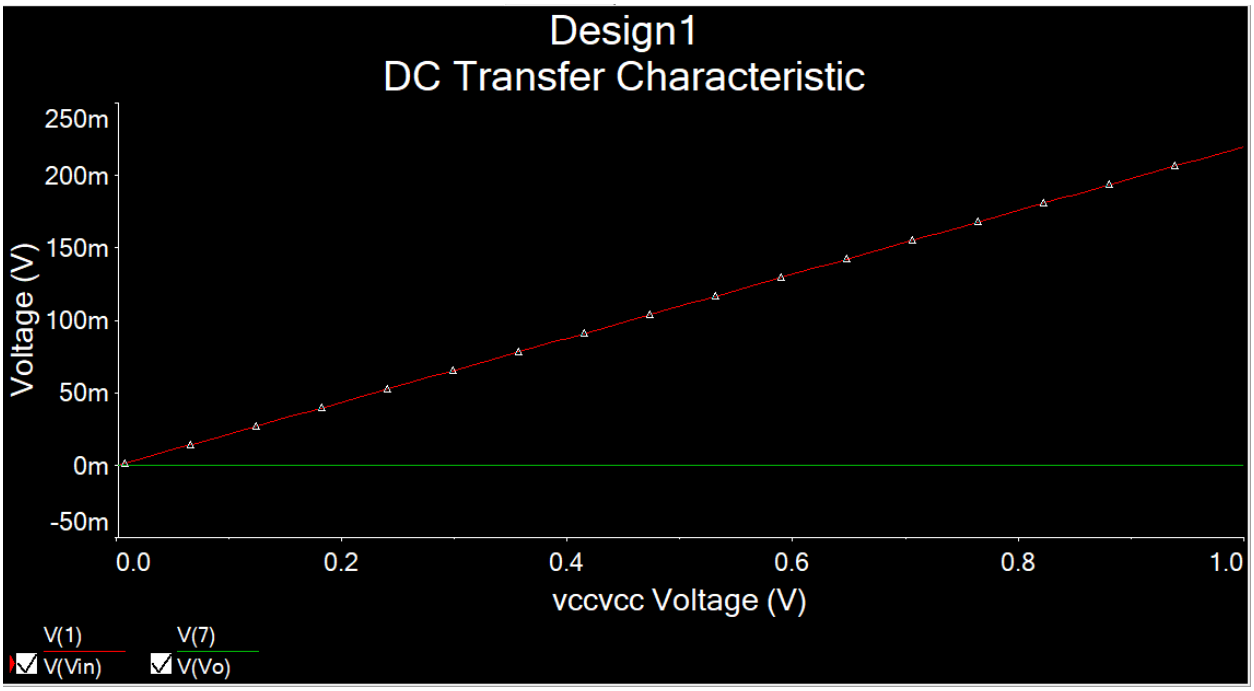


Figure E2: Includes the DC transfer characteristics of both Vin and Vo of the two-stage (CE-CC) amplifier.

Figure E3

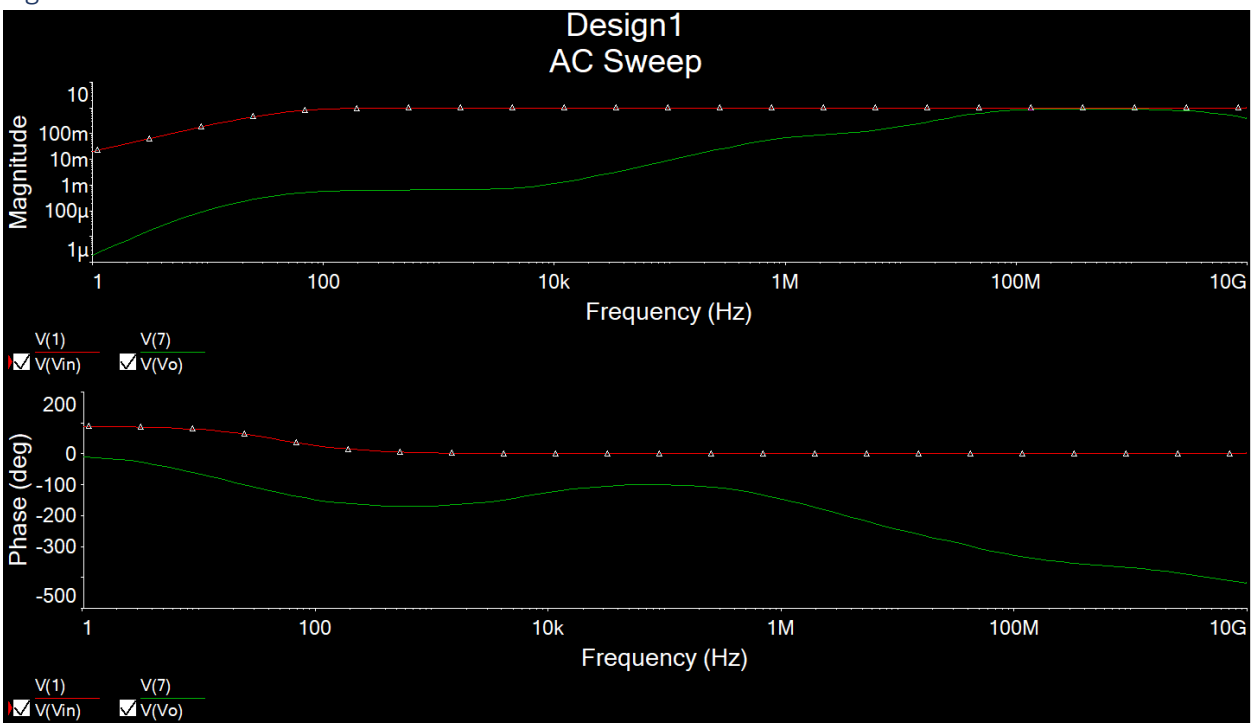


Figure E3: Includes the frequency response both Vin and Vo of the two-stage (CE-CC) amplifier.

Figure E4

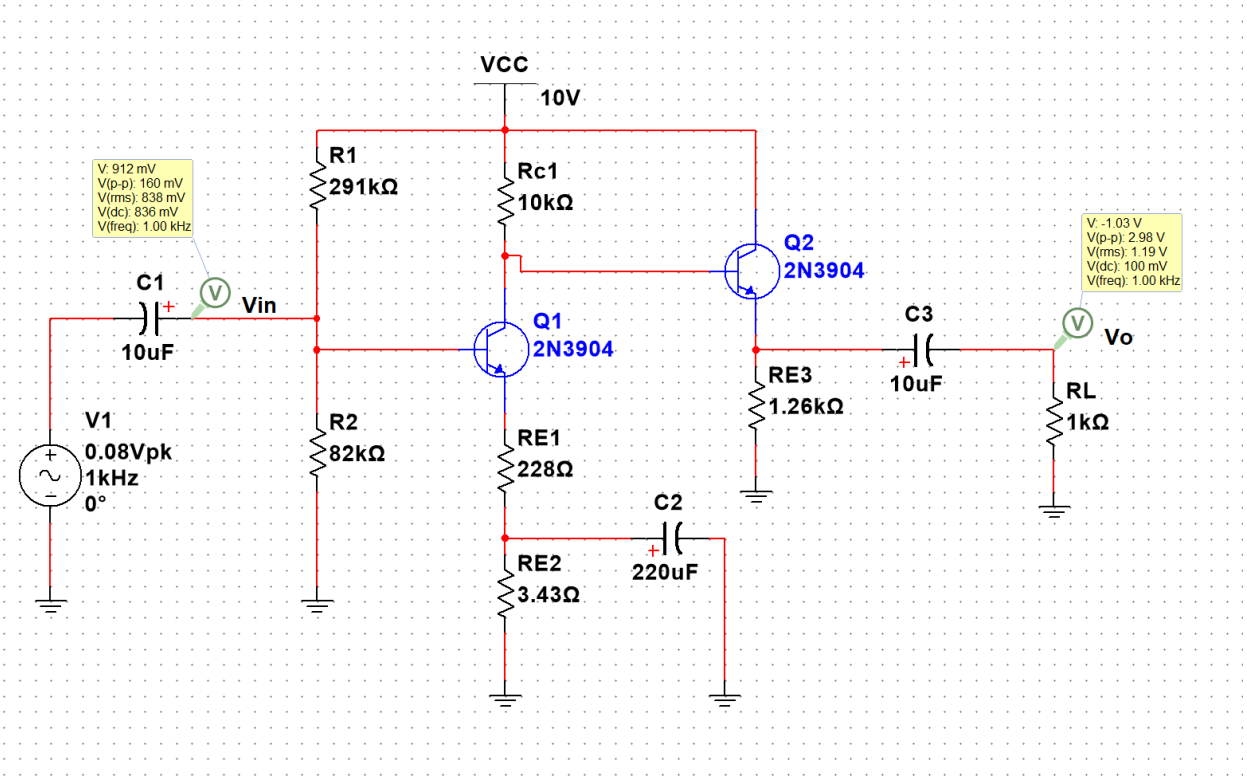


Figure E4: Circuit overview and placement of probes for the simulations.

Conclusion

Requirement Analysis

This was a tough project and I have struggled with meeting the requirements of the assignment. However, I believe I have met a good amount of the specifications for the project for submission.

Requirements met:

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$**;**
- No-load voltage gain (at $1\ kHz$): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10}\%)$**;**
- Maximum no-load output voltage swing (at $1\ kHz$): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at $1\ kHz$ and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90}\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at $1\ kHz$ and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at $1\ kHz$): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (−3dB response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$**,** $\mathbf{1.0}\ \boldsymbol{\mu F}$**,** $\mathbf{2.2}\ \boldsymbol{\mu F}$**,** $\mathbf{4.7}\ \boldsymbol{\mu F}$**,** $\mathbf{10}\ \boldsymbol{\mu F}$**,** $\mathbf{47}\ \boldsymbol{\mu F}$**,** $\mathbf{100}\ \boldsymbol{\mu F}$**,** $\mathbf{220}\ \boldsymbol{\mu F}$**;**
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

I have verified these requirements via observation of the circuit itself, and partial outputs of the simulations.

Calculations vs Simulation

While a good portion of the calculations matched up with simulation results, there was definitely some noticeable differences regarding the overall output of the circuit. I assume this is a result of improperly building/designing the circuit. It can also be a result of my own calculation errors. As a result, a good portion of the results did not quite match up to expectations and did not meet some of the design requirements.

Closing remarks

This project was a great introduction in an application of the various analysis and design techniques we have learned from our lectures/labs/tutorials. We had the opportunity to not only apply these newfound skills, but we also were able to test how well we could meet the requirements for a circuit that had specific constraints. I found the project to be quite challenging, but it gave me a great idea on the basic techniques. I strongly believe if I keep taking on similar design-oriented projects on my own. I will be able to become quite good at ensuring the project meets the requirements. This was a great change of pace from our usual lab structure. I've quite enjoyed the learning experience.