EE 5313 MICROPROCESSOR PROJECT

SPRING 2016

SDRAM CONTROLLER DESIGN

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INTRODUCTION:

80386DX has only asynchronous memory support. In this project we are basically designing a SDRAM controller that interfaces the MT48LC8M8A2 SDRAM (2M X 8 X 4banks) memory with 80386DX microprocessor. The SDRAM controller located between the processor and memory and enables the conversion of 80386 commands into synchronous SDRAM memory command and control words. A burst length of 4 is supported by this design. In the project, we have used -75 MT48LC8M8A2 SDRAM Configuration. Our 80386DX microprocessor is working at 25MHz frequency (CLK2 = 50 MHz).

Fig 1. Shows the basic interference diagram between the 80386DX processor, the SDRAM controller and SDRAM memory.

INTERFACING DIAGRAM:

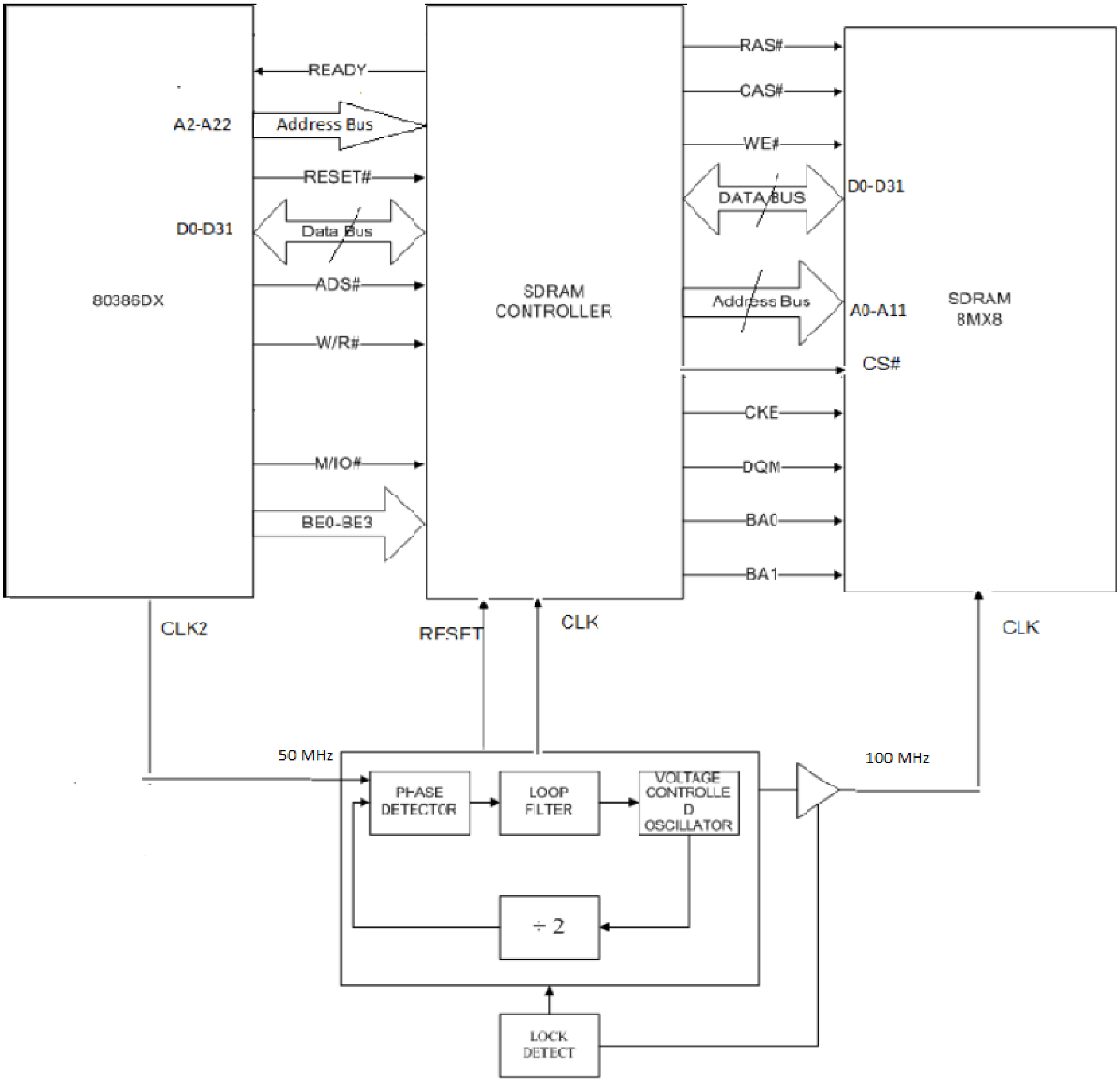


Fig 1: Basic Block diagram of SDRAM – 80386DX Interface

MEMORY INITIALIZATION:

NOP_{1} = t_{rcd} NOP_{3} = t_{rp} NOP_{5} = Start Auto Precharge NOP_{7} = 100 us state NOP_{9} = t_{mrd}

NOP_{2} = t_{cl} NOP_{4} = t_{wr} NOP_{6} = Clock Stable NOP_{8} = Auto Refresh Delay

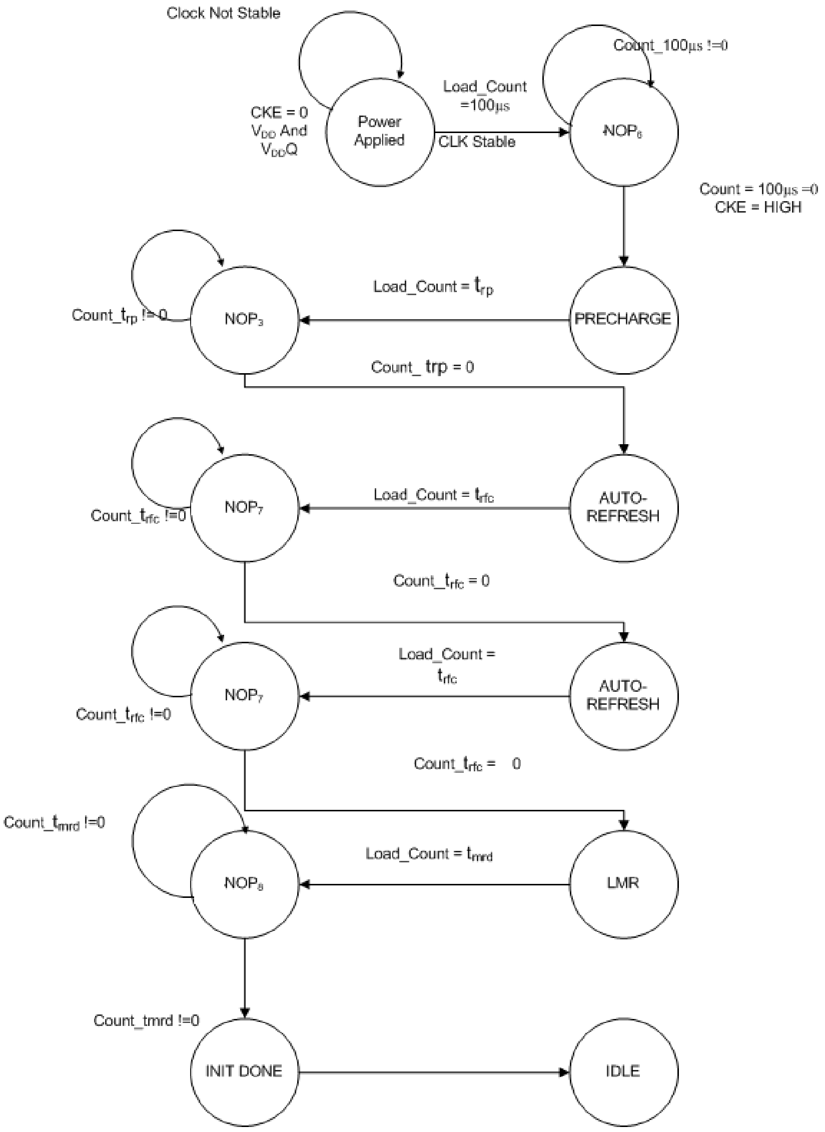


Fig 2: State diagram: FSM initialization

Initialization Transition Table

Current State	Conditions	Next State
X	Vdd,Vddq,CKE=0,CLK Stable	NOP6
NOP6	Count_100µs=0	Precharge
Precharge	X	NOP3
NOP3	Count_trp=0	Auto-Refresh
Auto Refresh	X	NOP8
NOP8	Count_trfc=0	Auto-Refresh
Auto-Refresh	X	NOP8
NOP8	Count_trfc=0	LMR
LMR	X	NOP8
NOP8	Count_tmrd=0	INIT DONE

Load Mode Register Fields:

1. Burst Length (BL) = 4 : 0 1 0
2. Burst Type (BT) = Sequential : 0
3. CAS Latency = 2 : 0 1 0
4. Op Mode = Standard Operation : 0 0
5. WB = Programmed Burst Length : 0
6. Reserved : 0 0

READ OPERATION WITH AUTO PRECHARGE:

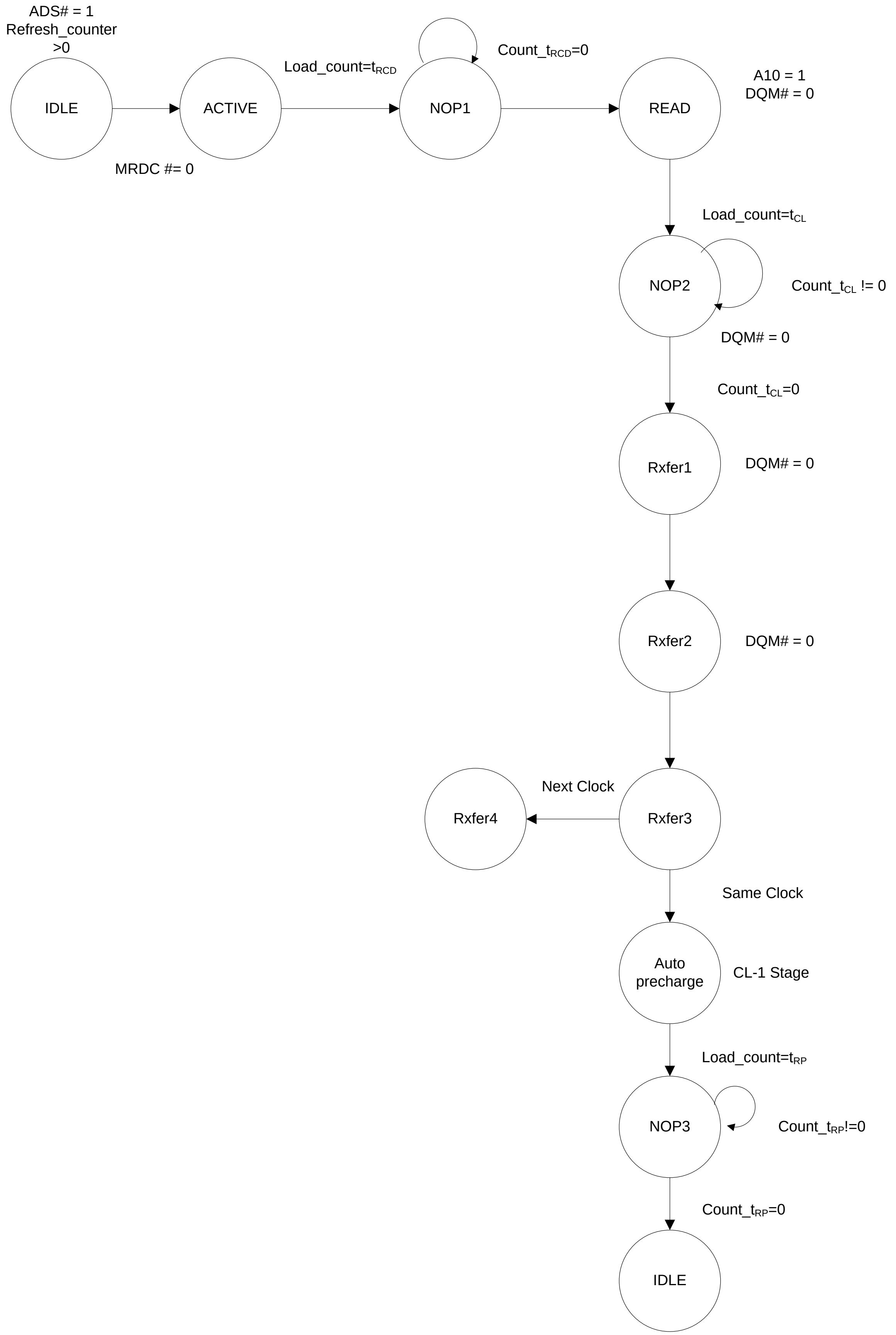


Fig 3: State diagram: Reading from SDRAM memory (with auto precharge)

READ WITH AUTO PRECHARGE TRANSISTION TABLE:

PRESENT STATE	CONDITION	NEXT STATE
ACTIVE	LOAD VALUE t_{RCD}	NOP1
NOP1	Count_t_{RCD} = 0	READ
READ	LOAD VALUE t_{CL}	NOP2
NOP2	t_{CL} VALUE = 0	Rxfer1
Rxfer1	X	Rxfer2
Rxfer2	X	Rxfer3
Rxfer3	X (next clock)	Rxfer4
Rxfer3	X(same clock)	AUTO PRECHARGE (A10 = 1)
AUTO PRECHARGE	Load_count=t_{RP}	NOP3
NOP3	Count_t_{RP} = 0	IDLE

Fig 4: State Table: Read with Auto Precharge

READ OPERATION WITH MANUAL PRECHARGE*:*

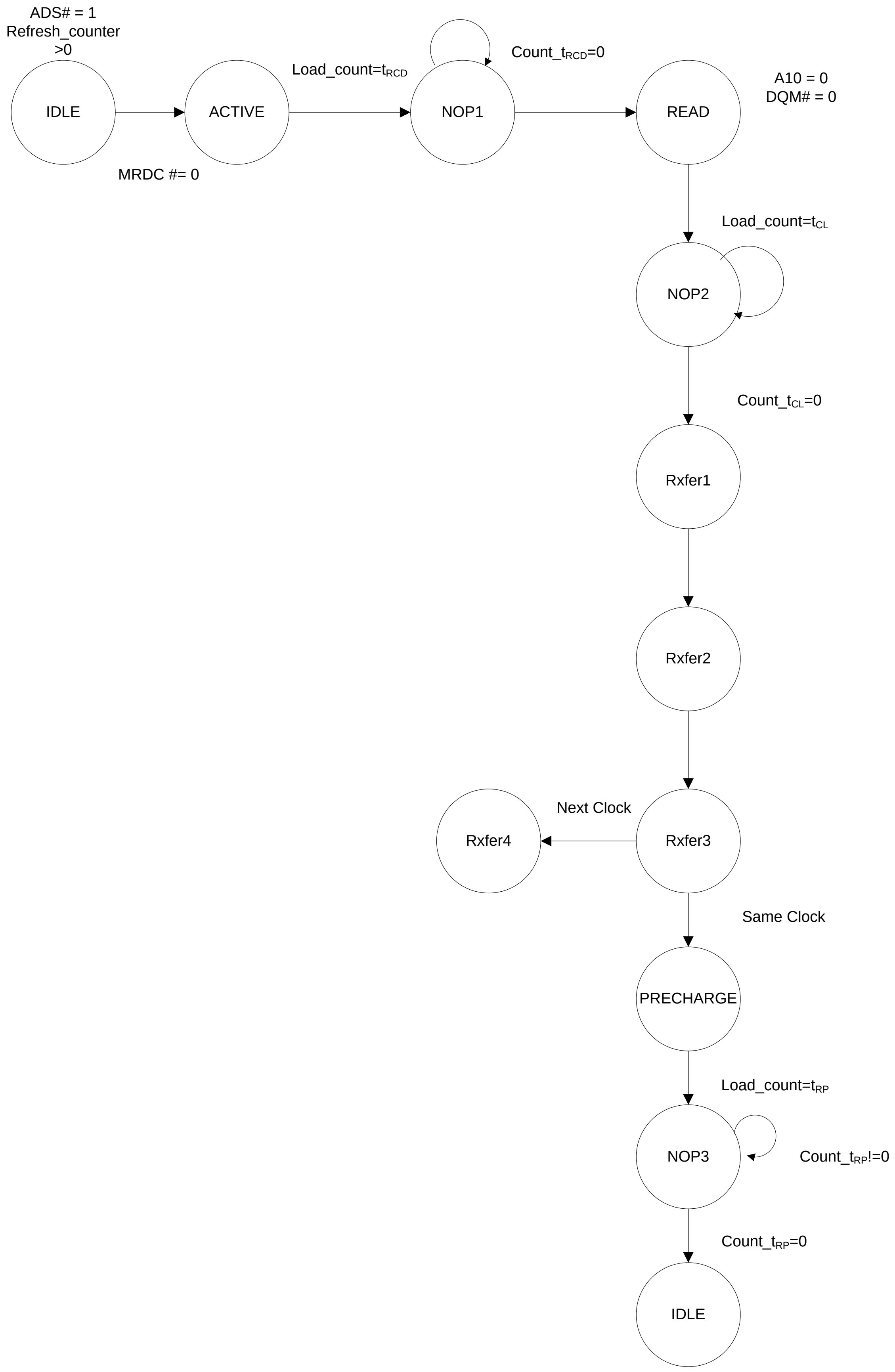


Fig 5: State diagram: Reading from SDRAM memory (with manual precharge)

READ WITH MANUAL PRECHARGE TRANSISTION TABLE:

PRESENT STATE	CONDITION	NEXT STATE
ACTIVE	LOAD VALUE t_{RCD}	NOP1
NOP1	t_{RCD} VALUE = 0	READ
READ	LOAD VALUE t_{CL}	NOP2
NOP2	t_{CL} VALUE = 0	Rxfer1
Rxfer1	X	Rxfer2
Rxfer2	X	Rxfer3
Rxfer3	X (next clock)	Rxfer4
Rxfer3	X(same clock)	PRECHARGE (A10 = 0)
PRECHARGE	Load_count=t_{RP}	NOP3
NOP3	t_{RP} VALUE = 0	IDLE

Fig 6: State Table: Read with Manual Precharge

WRITE OPERATION WITH AUTO PRECHARGE:

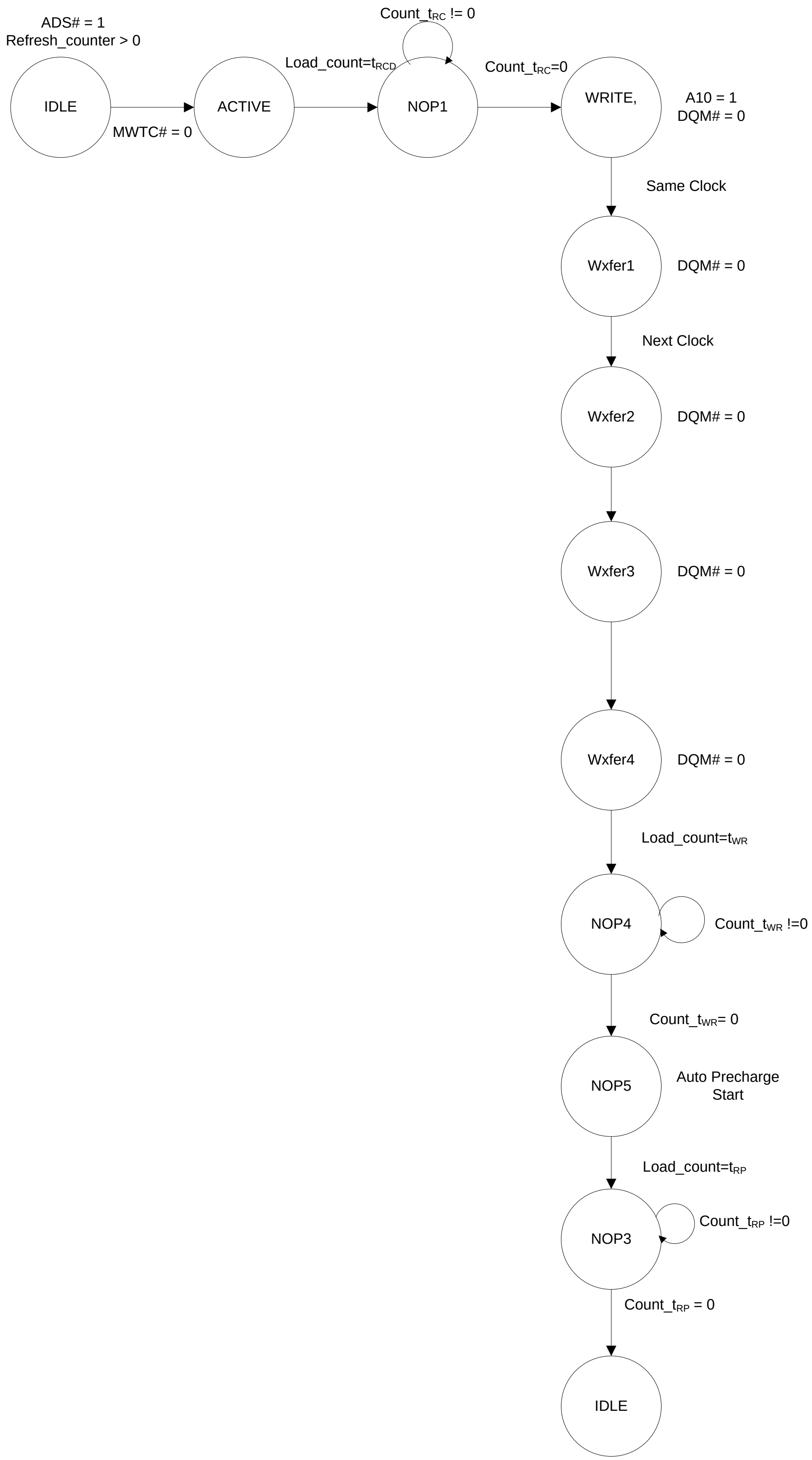


Fig 7: State diagram: Writing to SDRAM memory (with auto precharge)

WRITE WITH AUTO PRECHARGE TRANSISTION TABLE:

PRESENT STATE	CONDITION	NEXT STATE
ACTIVE	LOAD VALUE t_{RCD}	NOP1
NOP1	t_{RCD} VALUE = 0	WRITE ,
WRITE	X(same clock)	Wxfer1
Wxfer1	X(next clock)	Wxfer2
Wxfer2	X	Wxfer3
Wxfer3	X	Wxfer4
Wxfer4	LOAD VALUE t_{WR}	NOP4
NOP4	t_{WR} VALUE = 0	NOP5
NOP5	LOAD VALUE t_{RP}	NOP3
NOP3	t_{RP} VALUE = 0	IDLE

Fig 8: State Transition Table: Write with auto precharge

WRITE OPERATION WITH MANUAL OPERATION:

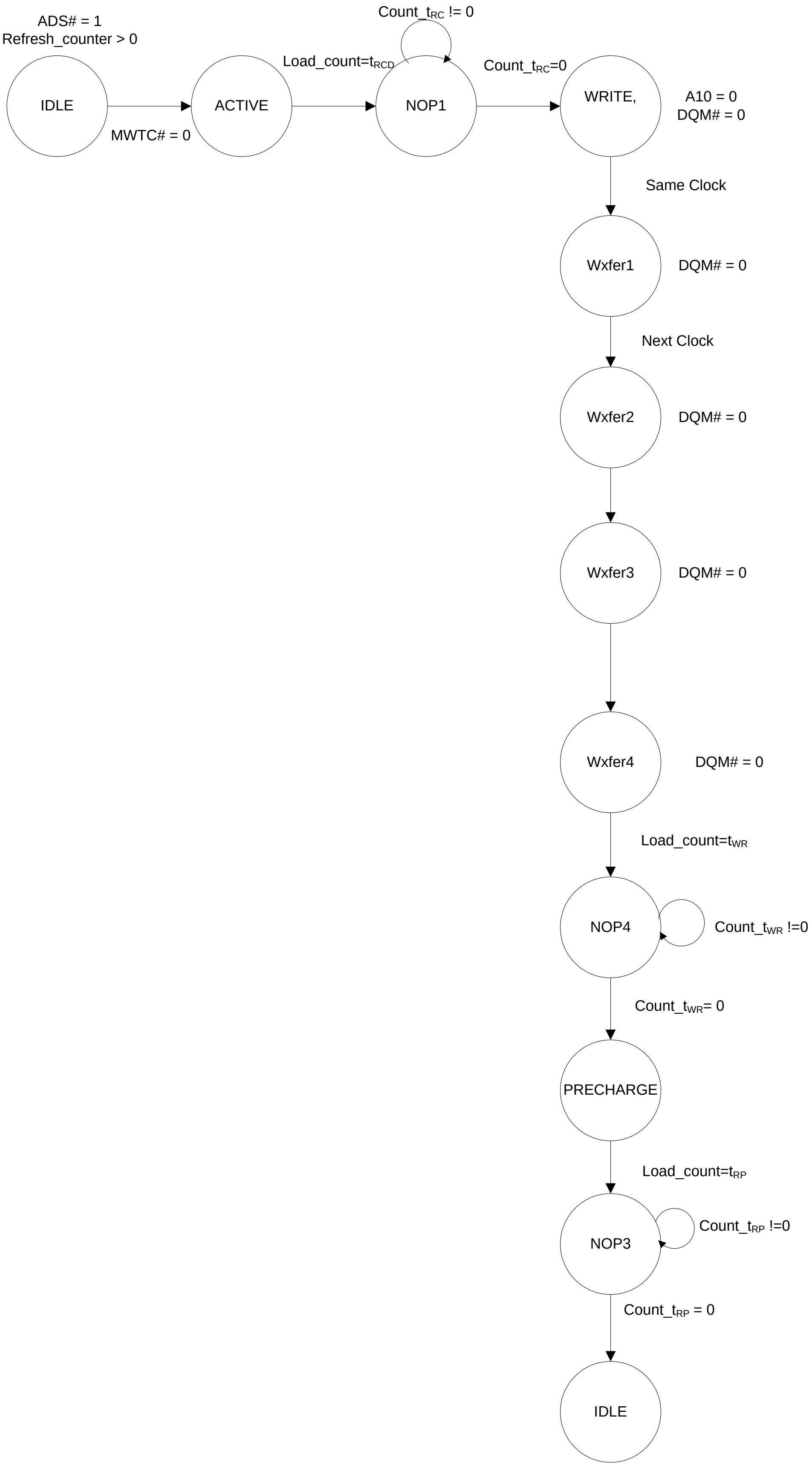


Fig 9: State diagram: Writing to SDRAM memory(with manual precharge)

WRITE WITH MANUAL PRECHARGE TRANSISTION TABLE:

PRESENT STATE	CONDITION	NEXT STATE
ACTIVE	LOAD VALUE t_{RCD}	NOP1
NOP1	t_{RCD} VALUE = 0	WRITE ,
WRITE	X(same clock)	Wxfer1
Wxfer1	X(next clock)	Wxfer2
Wxfer2	X	Wxfer3
Wxfer3	X	Wxfer4
Wxfer4	LOAD VALUE t_{WR}	NOP4
NOP4	t_{WR} VALUE = 0	PRECHARGE
NOP5	LOAD VALUE t_{RP}	NOP3
NOP3	t_{RP} VALUE = 0	IDLE

Fig 10: State Transition Table: Write with manual precharge

AUTO REFRESH:

1. This command must be issued each time a refresh is required. All active banks must be precharged before issuing an auto refresh command.
2. Address bits are “Don’t Care” during AUTO REFRESH since the internal refresh controller does the addressing part.
3. Regardless of the SDRAM memory configuration, there are 4096 rows. Hence it requires 4096 auto refresh cycles every 64ms (commercial and industrial) and 16ms (automotive).

NOTE: SELF REFRESH command is initiated like AUTO REFRESH command except CKE is disabled (LOW).

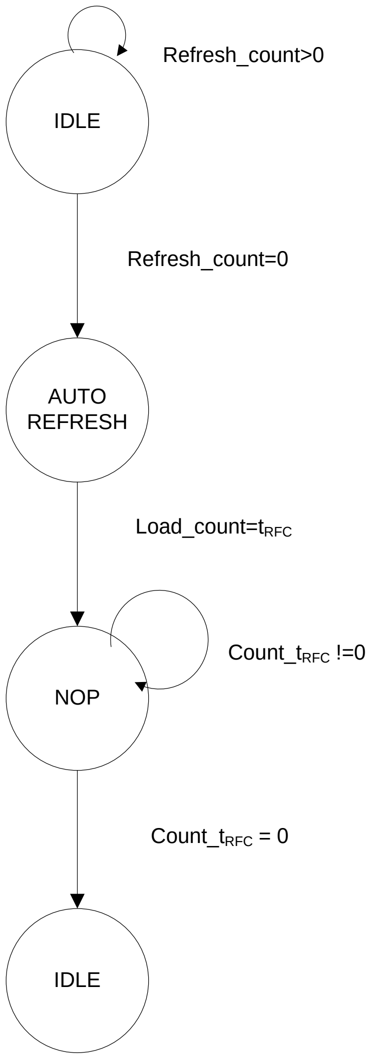


Fig 11: State Diagram: Auto Refresh

AUTO REFRESH TRANSISTION TABLE:

PRESENT STATE	CONDITION	NEXT STATE
IDLE	X	AUTO REFRESH
AUTO REFRESH	LOAD VALUE t_{RFC}	NOP
NOP	t_{RFC} VALUE = 0	IDLE

Fig 12: State Transition Diagram: Auto Refresh

Address Signal Generation:

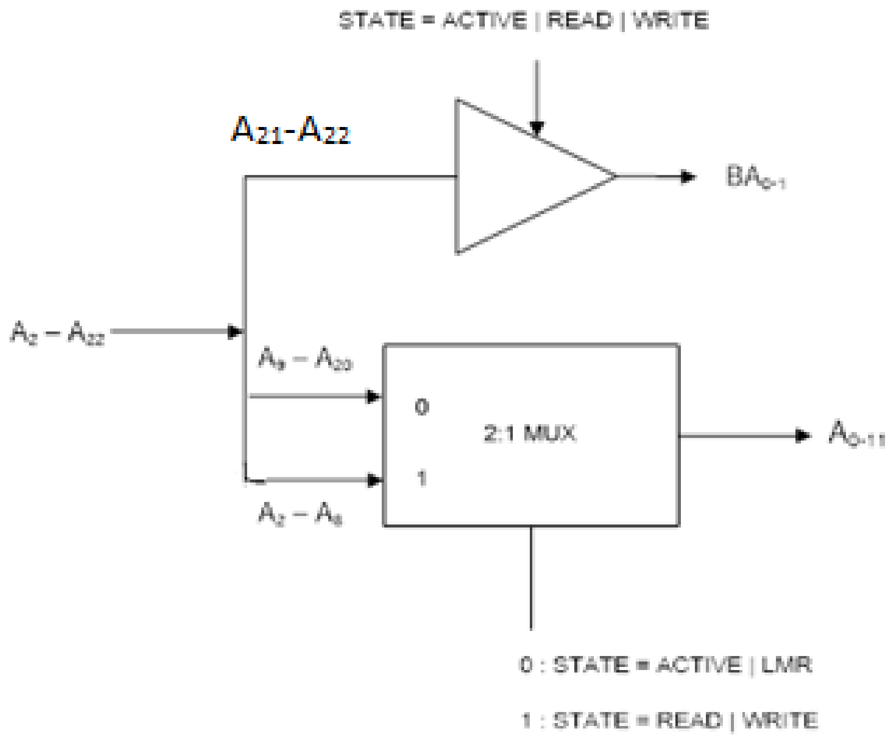


Fig 13: Block Diagram for Address Generation

In this memory address latching with microprocessor is done as following: A2-A8 forms column address (LSBs of column are hardcoded), A9-A20 forms row address and A21-A22 forms BA0-BA1 signals to the memory.

Data Path Module (For Read):

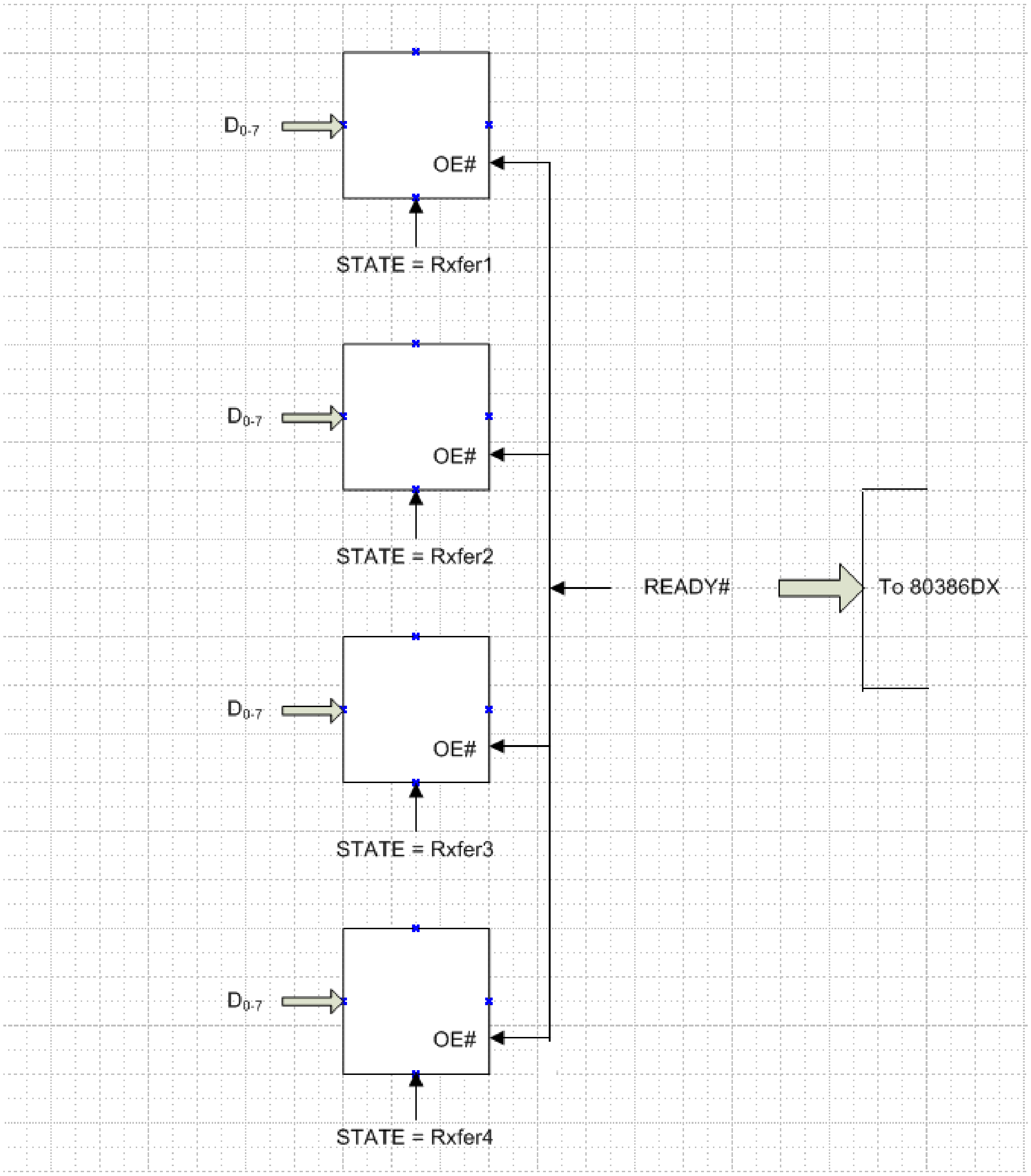


Fig 14: Block Diagram of Data Flow (READ)

In data line interface, while reading the data from the memory is latched byte by byte to 4 different latches corresponding to 4 different data for BL=4 and is outputted simultaneously from all 4 latches on READY# signal to give 32-bit data to the microprocessor.

Data Path Module (For write):

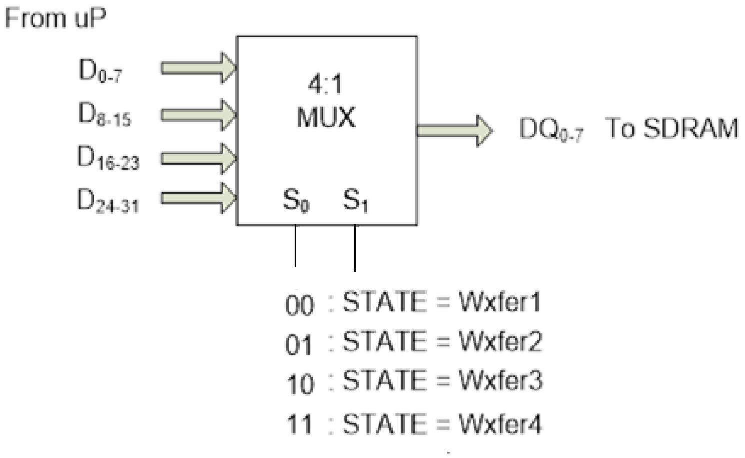


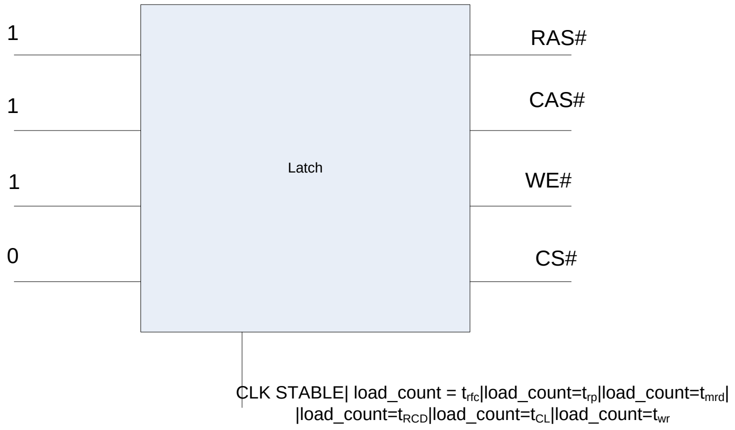
Fig 15: Block Diagram of Data Flow (WRITE)

Similarly, while writing each eight bit- data is given to the memory using a 4:1 multiplexer.

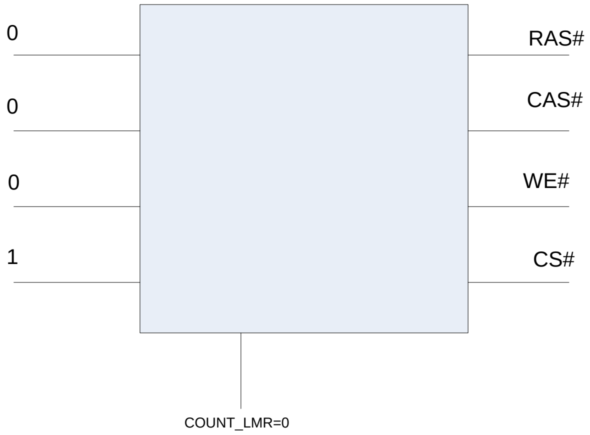
Command Signals:

Depending upon our state we are enabling various command signals such as:

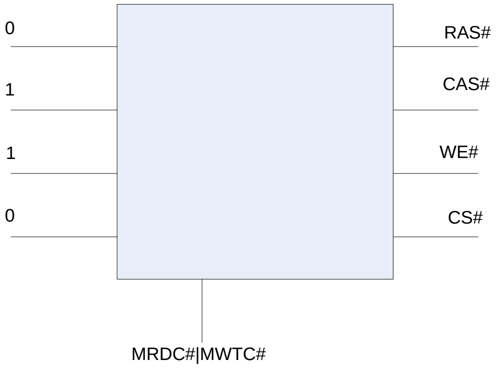
NOP:


1
1
1
0
Latch
RAS#
CAS#
WE#
CS#
CLK STABLE| load_count = t_{rfc}|load_count=t_{rp}|load_count=t_{mrd}|
|load_count=t_{RCD}|load_count=t_{CL}|load_count=t_{wr}

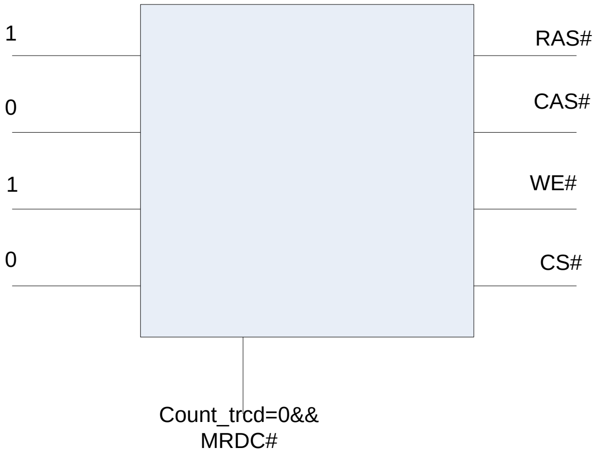
LMR (LOAD MODE REGISTER):



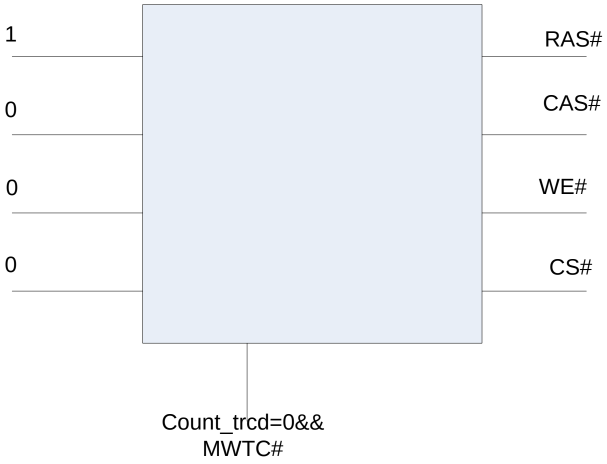
ACTIVE:



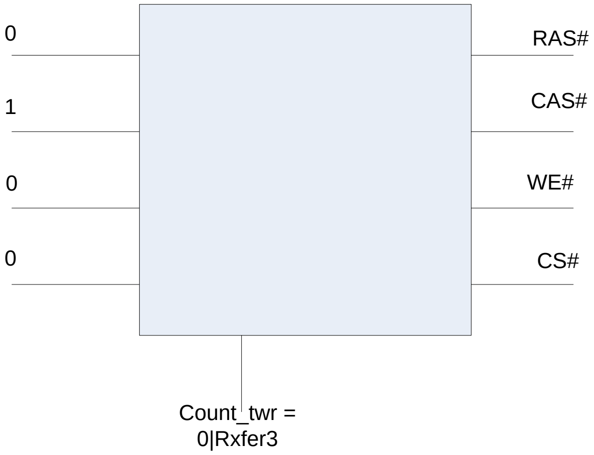
READ:



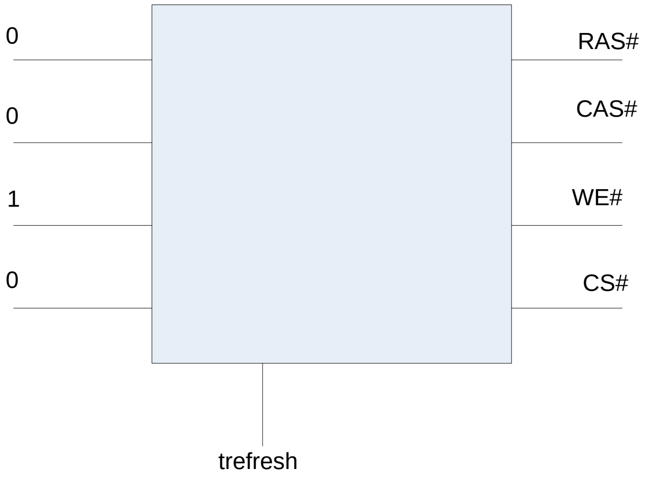
Write:



Precharge:

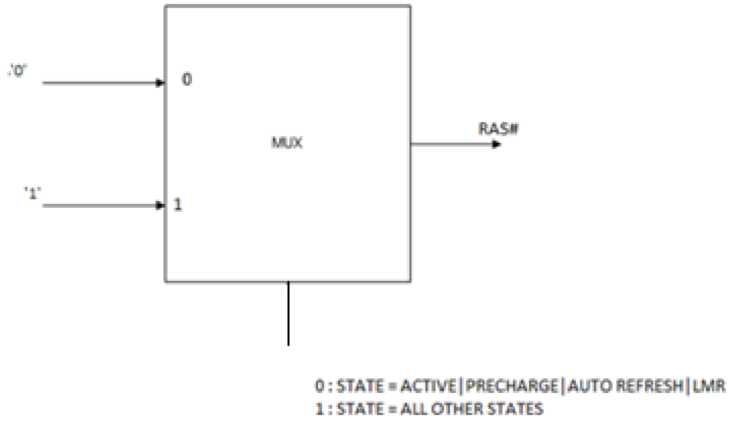


Refresh:

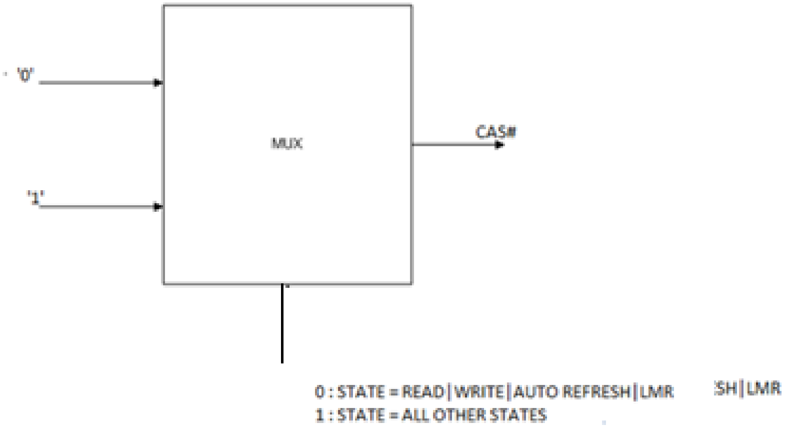


CONTROL SIGNALS:

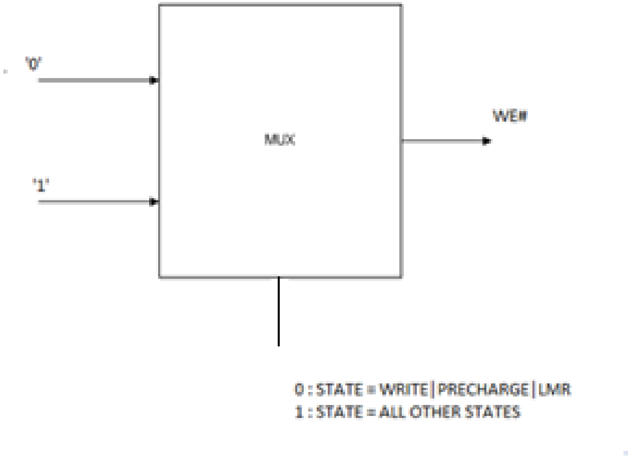
1. **RAS (Row Address Strobe):**


'0'
0
'1'
1
MUX
RAS#
0 : STATE = ACTIVE|PRECHARGE|AUTO REFRESH|LMR
1 : STATE = ALL OTHER STATES

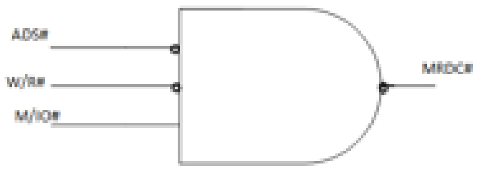
2. **CAS (Column Address Strobe):**


'0'
'1'
MUX
CAS#
0 : STATE = READ|WRITE|AUTO REFRESH|LMR
1 : STATE = ALL OTHER STATES
SH|LMR

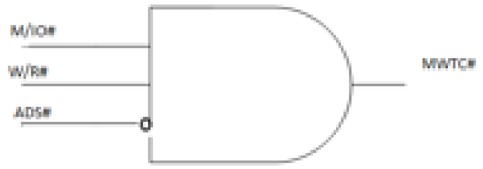
3. **WE (Write Enable):**



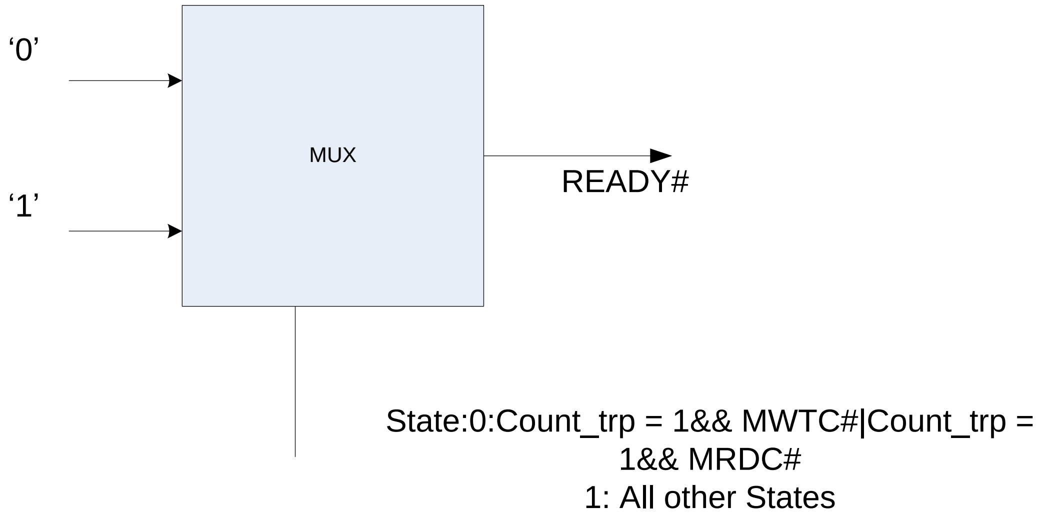
4. **MRDC (Memory Read Control)#:**
   80386DX does not have MRDC# and MWTC# signals so we need to generate these signals using these logics.



5. **MWTC (Memory Write Control)#:**

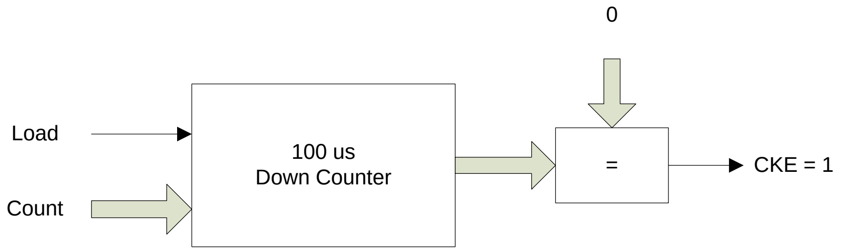


6. **READY SIGNAL**



Design of Various Delay Counters:

1. Count to be loaded = 100 µs / 10 ns = 2710H

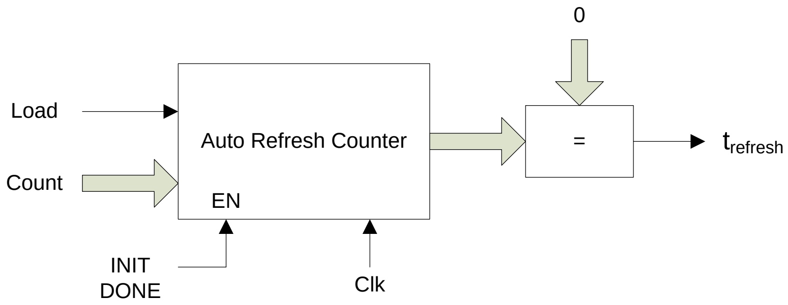


2. Auto Refresh Counter:

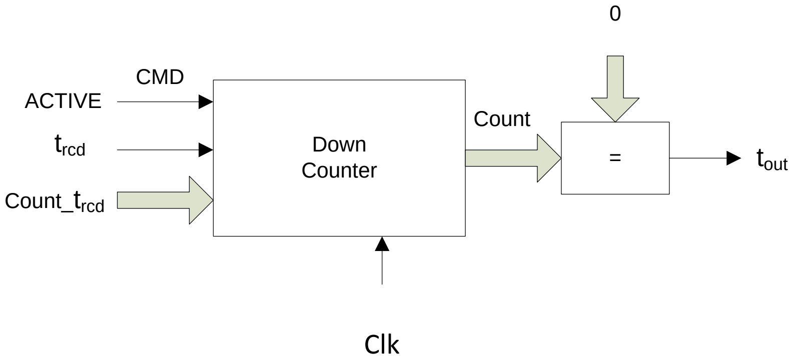
   $t_{refresh}$ = 64 ms / (No of rows)

   = 64 ms / 4096

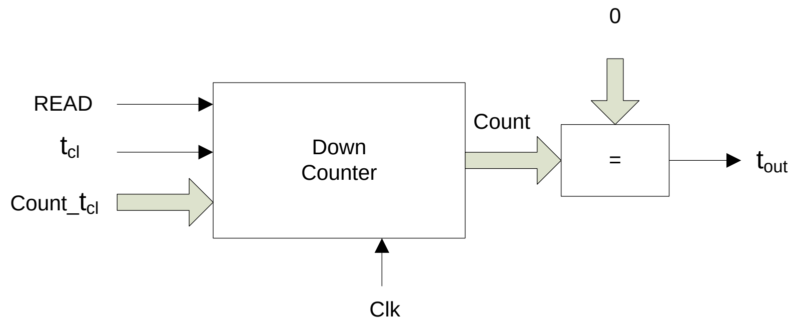
   = 15.6 µs (Count to be loaded 0820H)



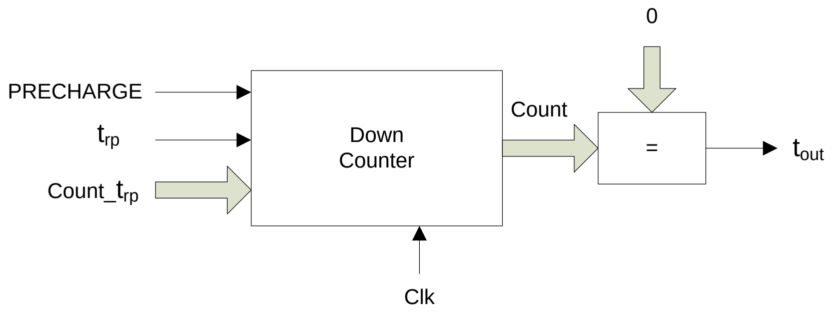
3. t_{rcd} = 15 ns / 10 ns = 2 clock cycles



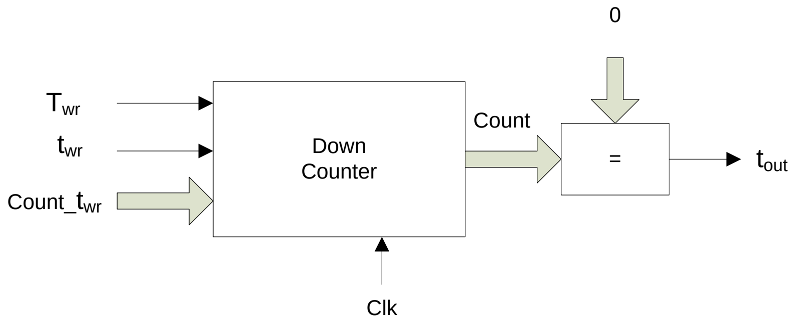
4. t_{cl} = 15 ns / 10 ns = 2 clock cycles



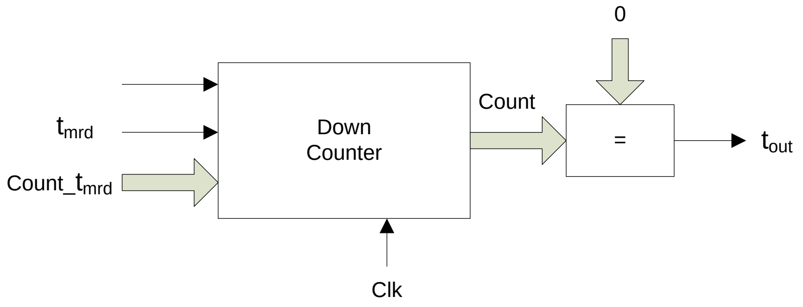
5. t_{rp} = 15 ns / 10 ns = 2 clock cycles



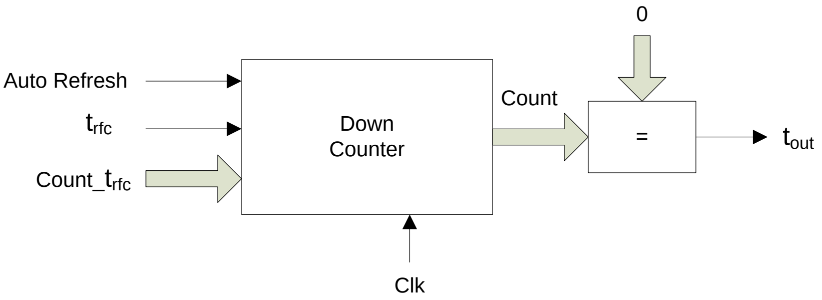
6. t_{wr}



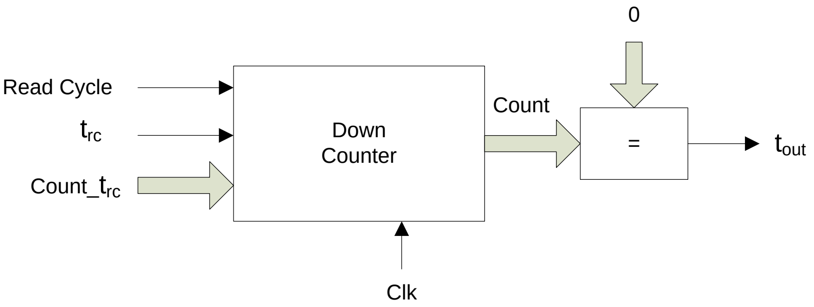
7. LMR: t_{mrd} = 15 ns / 7.5 ns = 2 clock cycles



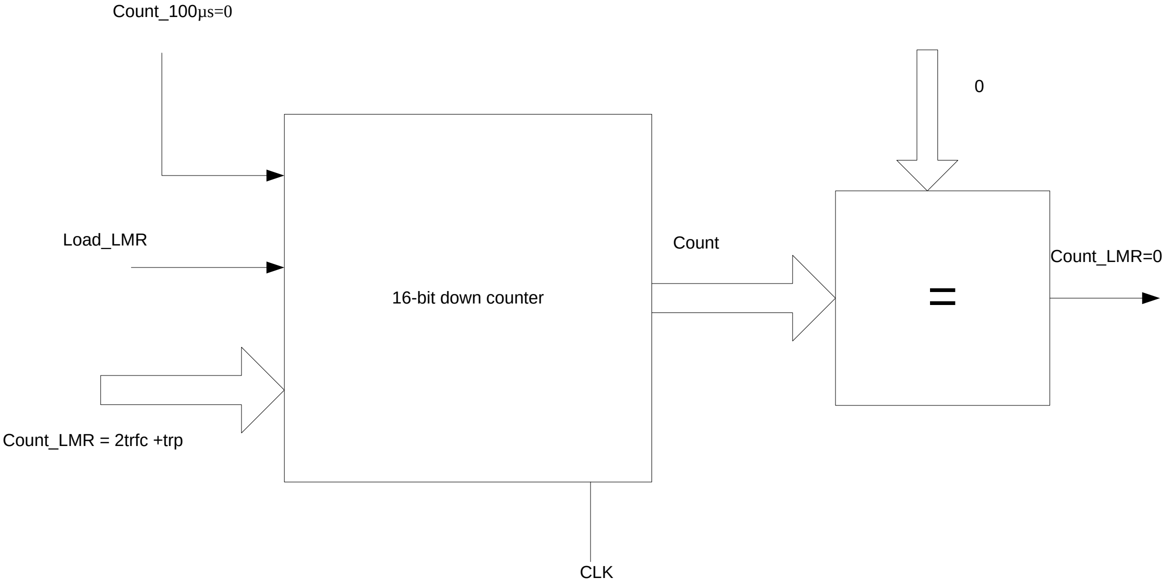
8. t_{rfc} = 66 / 10 = 7 clock cycles



9. t_{rc} = 60/10 = 6 clock cycles

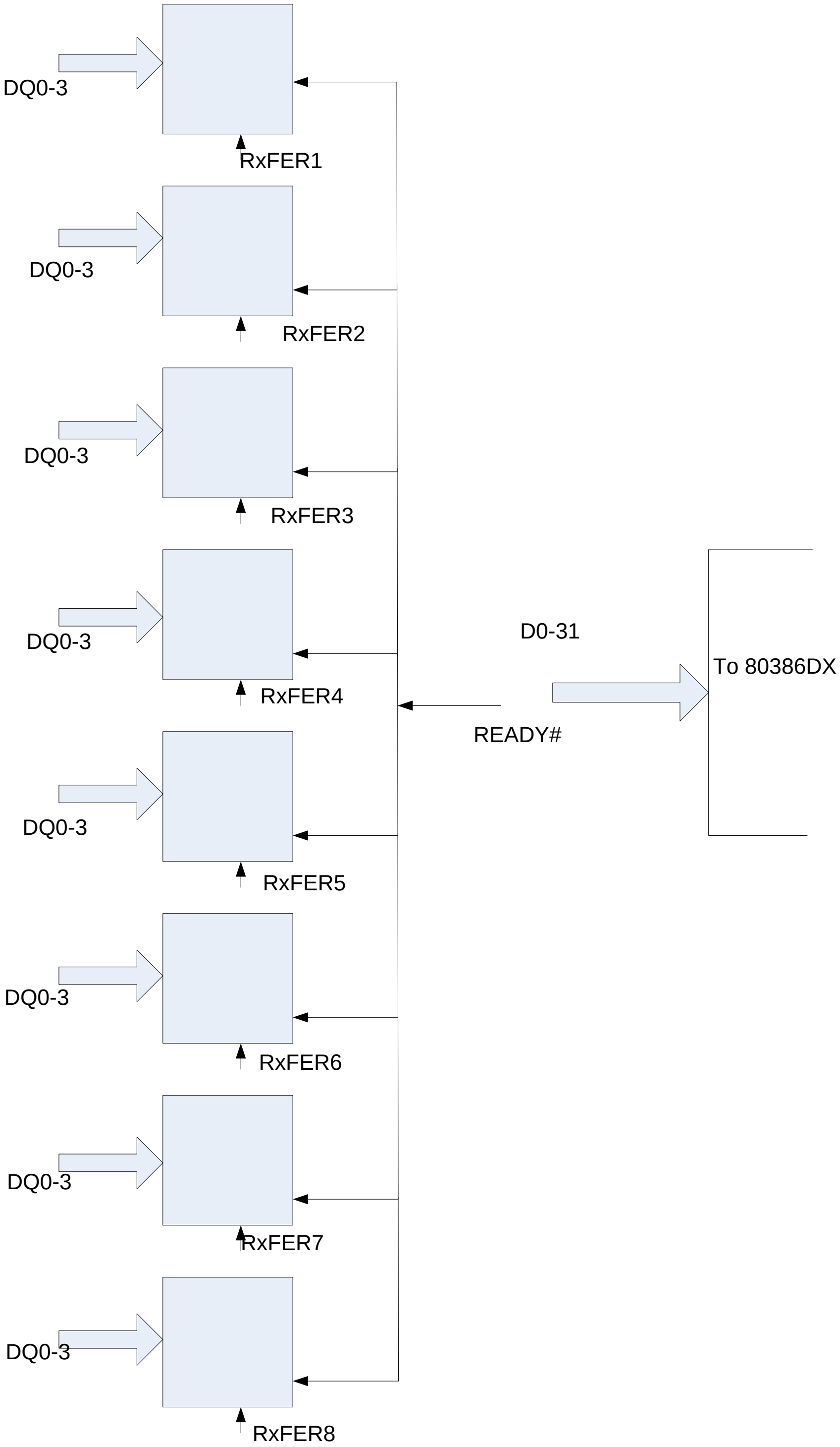


10. t_{LMR} = 2trfc + trp

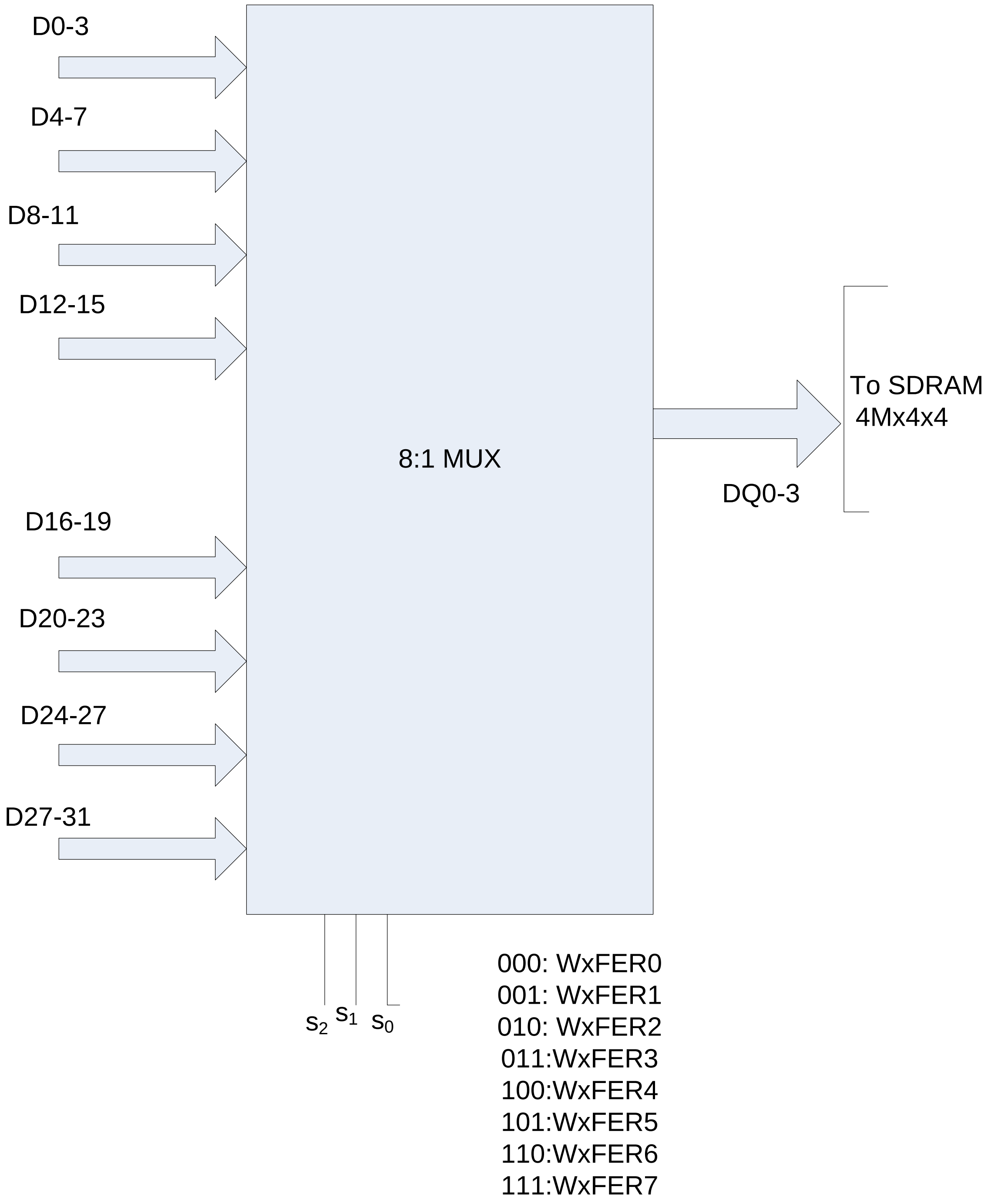


EXTRA CREDITS:

Showing Support for MT48LC16M4A2 – 4 Meg x 4 x 4 banks with higher burst length (BL=8). Here, we will interface a 4bit width memory with 80386DX microprocessor.
Showing Data-Path Module(For Read Operation):

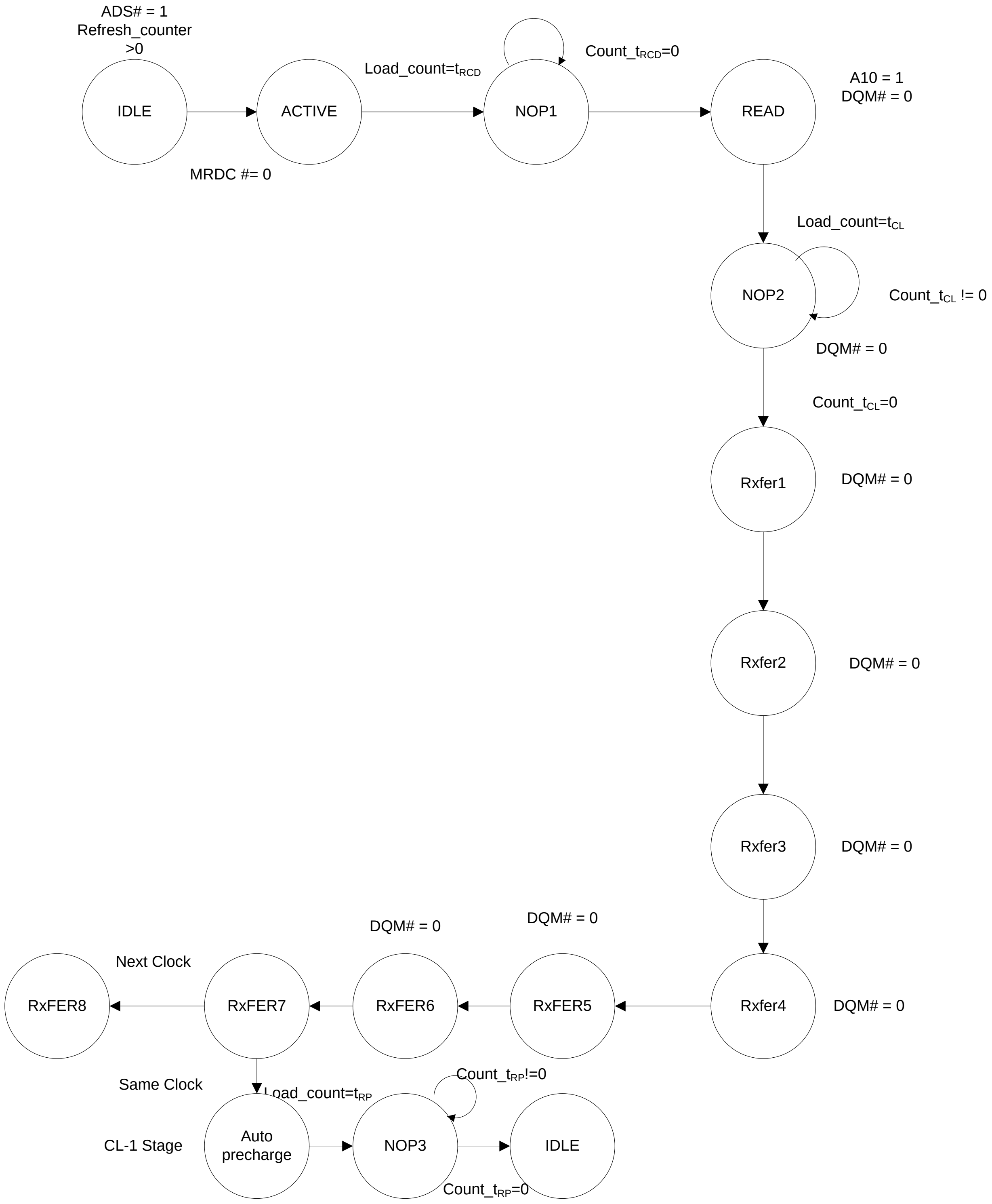


Data Path Module (For Write Operation):

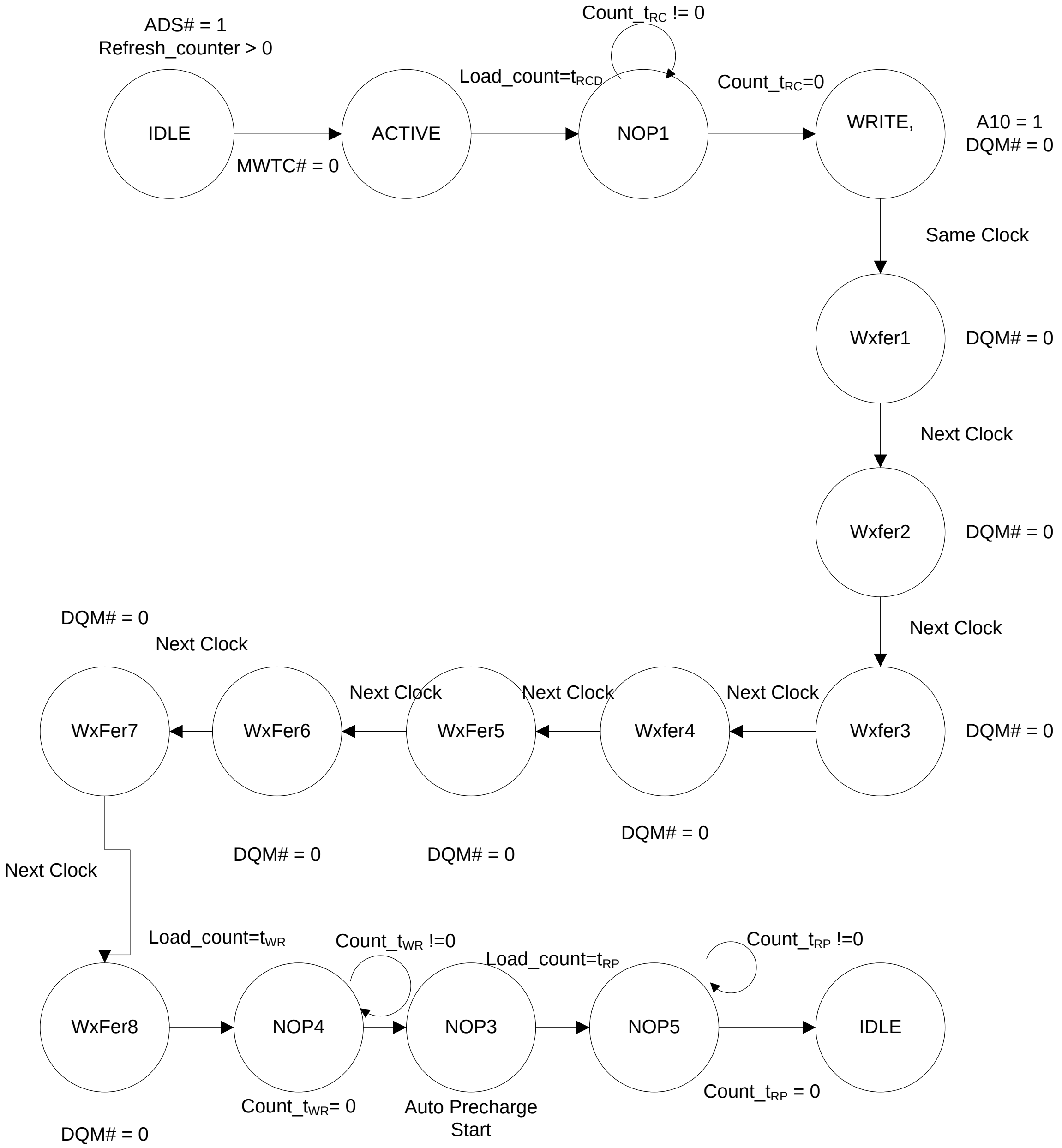


Finite State Diagram:

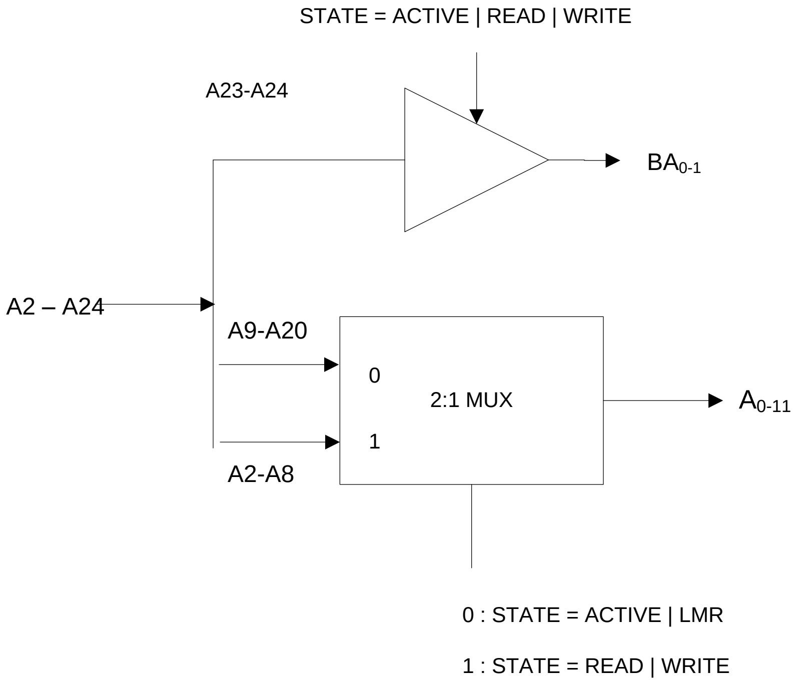
1) Read Cycle:



2) Finite State Machine (Write Cycle):



Address Generation(for X 4 mode) :


STATE = ACTIVE | READ | WRITE
A23-A24
BA0-1
A2 – A24
A9-A20
0
2:1 MUX
1
A0-11
A2-A8
0 : STATE = ACTIVE | LMR
1 : STATE = READ | WRITE