EE337: MICROCONTROLLERS AND MICROPROCESSORS

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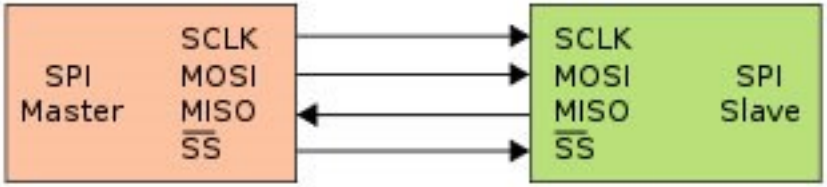
Serial Peripheral Interface

Serial Peripheral Interface

- What is it?
- Basic SPI
- Capabilities
- Protocol
- Pros and Cons
- Uses

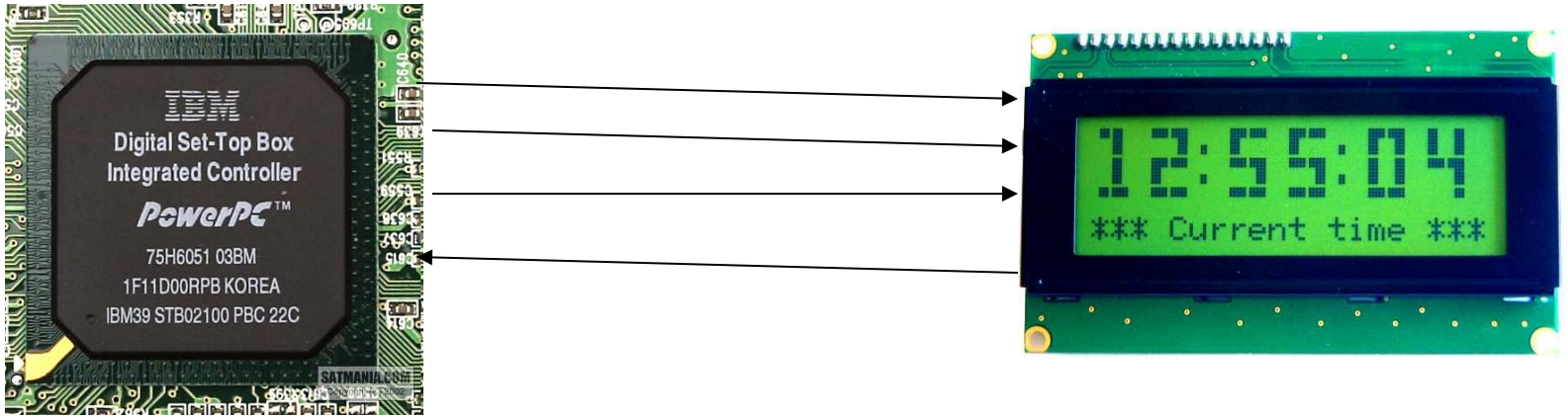


Serial Peripheral Interface

http://upload.wikimedia.org/wikipedia/commons/thumb/e/ed/SPI_single_slave.svg/350px-SPI_single_slave.svg.png

What is SPI?

- Serial bus protocol
- Fast, easy to use, and simple
- Very widely used
- Not “standardized”



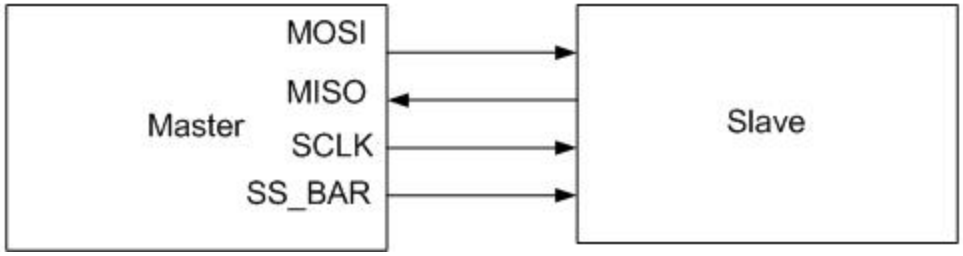
SPI Basics

- A 4-wire communications bus
- Typically communicate across short distances
- Supports
  - Single master
  - Multiple slaves
- Synchronized
  - Communications are “clocked”

SPI Capabilities

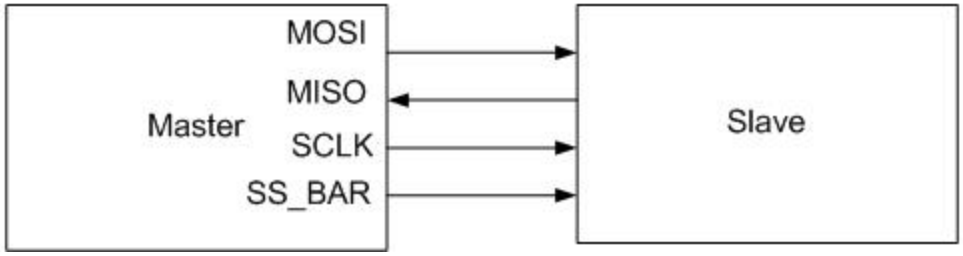
- Always full-duplex
  - Communicates in both directions simultaneously
  - Transmitted (or received) data may not be meaningful
- Multiple Mbps transmission speeds
  - 0-50 MHz clock speeds not uncommon
- Transfer data in 4 to 16 bit characters
- Supports multiple slaves

SPI bus wiring



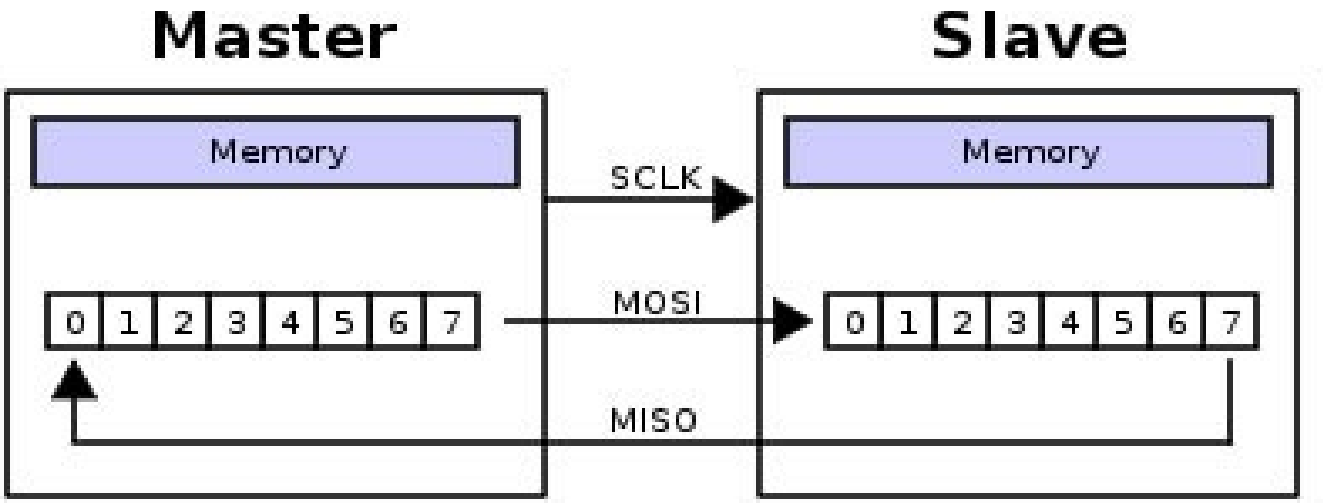
- Bus wires
  - Master-Out, Slave-In (MOSI)
  - Master-In, Slave-Out (MISO)
  - System Clock (SCLK)
  - Slave Select/Chip Select (SS1#, …, SS#n or CS1, …, CSn)
- Master asserts slave/chip select line
- Master generates clock signal
- Shift registers shift data in and out

SPI signal functions



- MOSI – carries data out of master to slave
- MISO – carries data out of slave to master
  - Both MOSI and MISO are active during every transmission
- SS# (or CS) – unique line to select each slave chip
- SCLK – produced by master to synchronize transfers

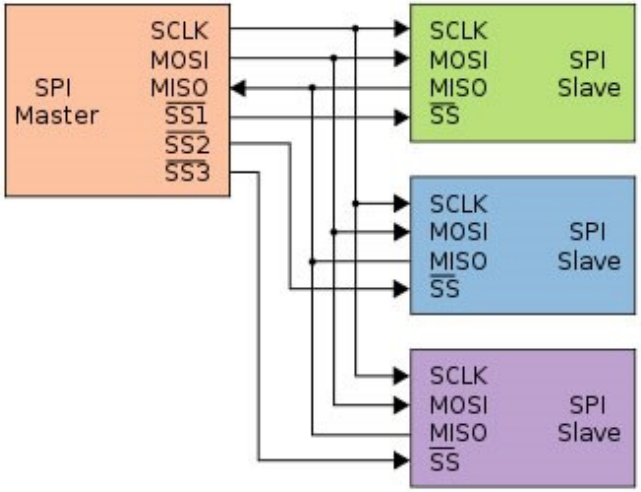
SPI uses a "shift register" model of communications



Master shifts out data to Slave, and shifts in data from Slave

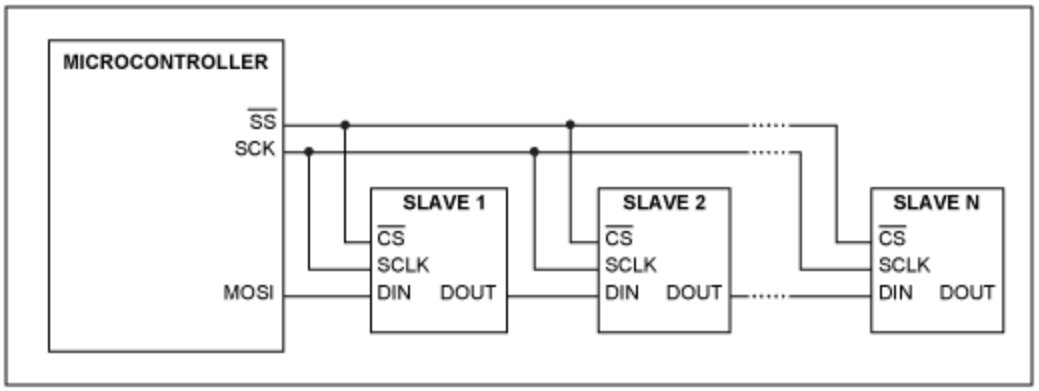
http://upload.wikimedia.org/wikipedia/commons/thumb/b/bb/SPI_8-bit_circular_transfer.svg/400px-SPI_8-bit_circular_transfer.svg.png

Two bus configuration models



Master and multiple independent slaves

http://upload.wikimedia.org/wikipedia/commons/thumb/f/fc/SPI_three_slaves.svg/350px-SPI_three_slaves.svg.png



Some wires have been renamed

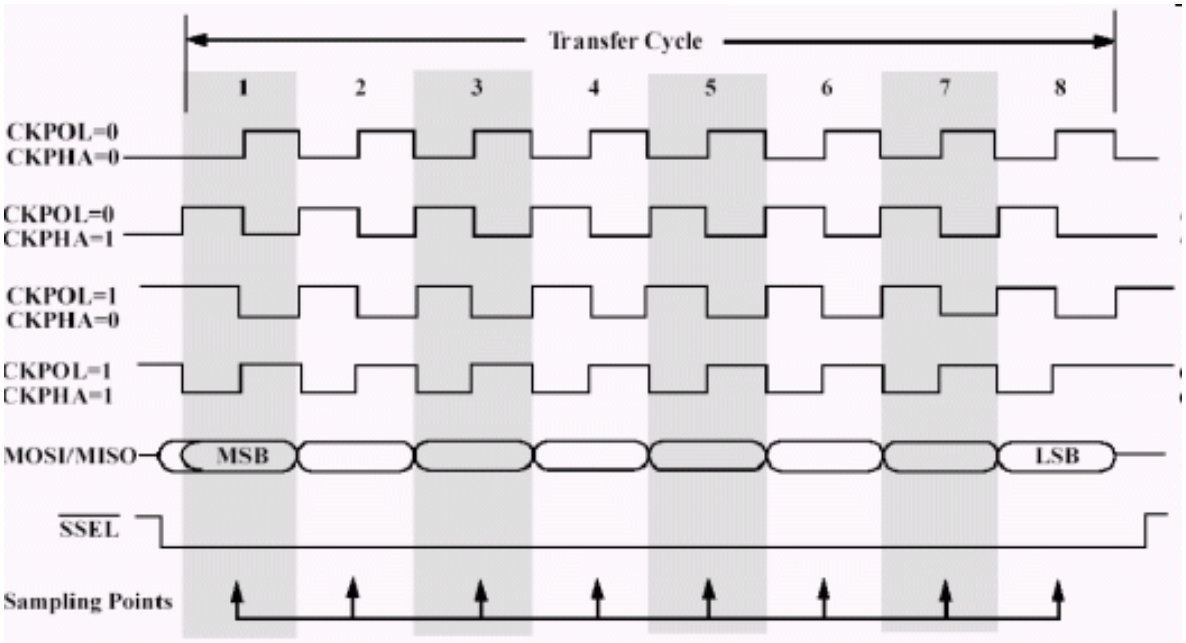
Master and multiple daisy-chained slaves

http://www.maxim-ic.com/appnotes.cfm/an_pk/3947

SPI clocking: there is no "standard way"

- Four clocking "modes"
  - Two phases
  - Two polarities
- Master and *selected* slave must be in the same mode
- During transfers with slaves A and B, Master must
  - Configure clock to Slave A's clock mode
  - Select Slave A
  - Do transfer
  - Deselect Slave A
  - Configure clock to Slave B's clock mode
  - Select Slave B
  - Do transfer
  - Deselect Slave B
- Master reconfigures clock mode on-the-fly!

SPI timing diagram



Timing Diagram – Showing Clock polarities and phases

http://www.maxim-ic.com.cn/images/appnotes/3078/3078Fig02.gif

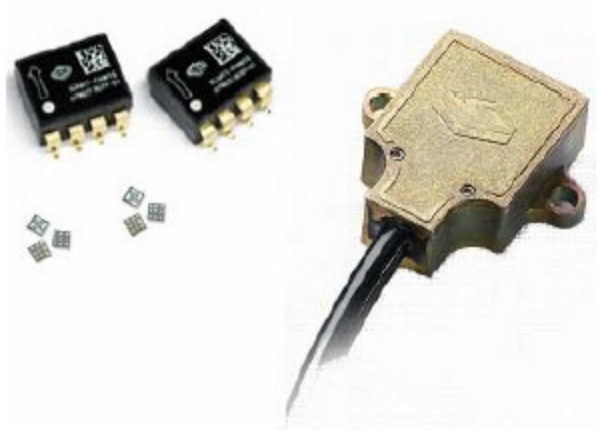
SPI tradeoffs: the pros and cons

- Pros
  - Fast for point-to-point connections
  - Easily allows streaming/constant data inflow
  - No addressing in protocol, so it's simple to implement
  - Broadly supported

- Cons
  - Slave select/chip select makes multiple slaves more complex
  - No acknowledgement (can't tell if clocking in garbage)
  - No inherent arbitration
  - No flow control (must know slave speed)

SPI is used everywhere!

- Peripherals
  - LCDs
  - Sensors
  - Radios
  - Lots of other chips



- Microcontrollers
  - Almost all MCUs have SPI masters
  - Some have SPI slaves