Scholastic Achievements

- Nationwide **top 1.5%** in **JEE Main** among 1.5 million candidates with **AIR 418** (SC) [2016]
- Secured **AIR 172** (SC) in **IIT JEE Advanced**, top 4.7% in general category(among 0.2 million) [2016]
- Qualified for **interview stage** of the Kishore Vaigyanik Protsahan Yojana **(KVPY)** (among 50 thousand) [2015]
- Recipient of **Scholar Badge** given to **high-performing** class 12 students of **DPS Bokaro** (among 600) [2015]
- Achieved **International Rank 634** in the 16th National Science Olympiad, 2013 conducted by **SOF** [2013]

Internships and Research Project

Ubisoft India Studios | *Automation Intern* *May 2019-July 2019*

Quality Control Team | ***Project:*** *Bug detection in graphic images*

- Researched on **Deep Learning** algorithms: R-CNN, faster R-CNN and Mask R-CNN, to **detect clipping** bugs
- **Implemented** a Mask R-CNN based model for **detection** and **segmentation**, achieved **77%** accuracy
- Reduced false positives by using **data augmentation**, test time augmentation and improved model performance

Hopfield Network for Optimization Problems *Autumn 2019*

Supervised Research Project | ***Guide:*** *Prof. Udayan Ganguly*

- **Understanding** the capability of Hopfield networks to find **optimal** solution to the **traveling salesman** problem
- **Investigated** the mapping of graph to **network** of sinusoidal oscillators and performed cicuit simulations
- Explored the **phasor arithmetic method** for phase evolution to ensure energy **function minimization**

Key Academic Projects

Authentication system for Vehicle Identification *Spring '19*

Digital Signal Processing *Course Project*

- **Extracted** number plate of malefactor car using **image processing**, under Make in India programme
- Used **bounding box detecting** techniques and alphabet dataset **correlation** to read the text in the plate

Latency and Scheduling using Graph Algorithms *Autumn'18*

Foundations of VLSI CAD *Course Project*

- Used **Topological Sort** to find optimal ordering of circuit elements in a combinational multi-level **Boolean network**
- Implemented resource scheduling with time constraints, estimated latency using **longest path** algorithm in a DAG

Analog Audio Equalizer *Spring'18*

Analog Laboratory *Course Project*

- Built a **6-channel tunable** audio equalizer to adjust the frequency components within an **audio signal** input
- **Implemented** features to **boost** and **cut** the energy of specific frequency bands using **Bandpass filters**
- Added **LM386 amplifier** to amplify output signal and introduced **volume controller** for Equalizer

Design and Verification of 16 Bit Dadda Multiplier *Autumn'19*

VLSI Design *Course Project*

- **Designed** and tested **16-bit Dadda multiplier** in **VHDL** for multiplication of two 16-bit unsigned integers
- Used **Brent Kung Logarithmic Adder** as **final stage** and identified, computed **critical path delay** in simulation

Movie Recommendation System *Spring'20*

Source: Kaggle *Self Project*

- Explored candidate generation methods : **content-based** and **collaborative filtering** to build recommender system
- **Represented** items and queries as **embeddings**, built a regularised **Matrix Factorization** model and trained it
- Implemented a **softmax** model and inspected its learned embeddings by looking at **nearest neighbours** and **norms**

Intelligent Power Board *Spring'19*

Electronics Design Laboratory *Course Project*

- Developed power board prototype capable of **logging** voltage, current and power consumption on a remote computer over bluetooth, to **monitor power surges** (achieved 1V resolution over 150-250V and 10mA resolution above 30mA)

Employee Attrition Analysis and Prediction *Spring'20*
Introduction to Machine Learning *Course Project*
- Built a **machine learning** pipeline to predict employee attrition on the basis of their performance
- **Analysed data**, employed supervised classification algorithms viz.**Random Forest**, **SVM**, achieved **87%** accuracy

IITB RISC Microprocessor *Autumn'18*
Microprocessors *Course Project*
- Designed **multi-cycle processor**, capable of implementing **15** instructions using Hardware Flowchart method in VHDL and implemented **microcoded based architecture** with **control store** for storing encoded control signals
- **Optimized flowcharts** of instructions for reducing size of **control words** and generated required **control signals**

Reaction Game *Spring'18*
Digital Circuits Laboratory *Course Project*
- **Implemented** a game on Krypton board which uses **Altera's Max V CPLD** device
- Added feature for **score calculation** based on time difference between LED 'ON instant' and **reaction time** of player for eight iterations to display **total delay** as score on LCD Display
- Designed **RTL** machine in **VHDL** to meet game specifications, simulated and tested implementation on **ModelSim**

Digital Stopwatch *Spring '17*
Introduction to Electronics *Course Project*
- **Developed** a basic **prototype** of digital stopwatch with **pause**, **play**, **record** features for **tracking time**
- Used **LM555 timer**, MOD-6 **counter** and 7-segment **decoder** and displayed output on a set of 7-segment display

Technical Skills

Programming	C, C++, Python, VHDL
Software Tools	Git, NumPy, Pandas, Matplotlib, TensorFlow, MATLAB, LaTeX
Design Tools	Cadence Virtuoso, Intel Quartus, NGspice, TCAD, TI CCS

Relevant Coursework

Digital	Digital Systems, VLSI Design, Systems Design, Testing & Verification of VLSI Circuits, VLSI CAD, VLSI Design Lab, Microprocessors, VLSI Technology
Electives	Machine Learning, Data Analysis & Interpretation, Probability & Random Processes, Digital Signal Processing, Image Processing & Remote Sensing, Linear Algebra, Calculus
Computer Science	Computer Programming and Utilization, Data Structures*

* Online Course

Positions of Responsibility

Teaching Assistant | Introduction to Electrical and Electronic Circuits *Aug'20 - Present*
- Responsible for setting assignments, organising tutorials and evaluating answer sheets for a batch of **28 s**tudents

Class Representative | Electrical Dual Degree Batch 2016-21 *July'17-July'18*
- Represented a batch of **64 students** for a year, acting as a link between professors and students
- **Handled** logistical issues faced by students in courses offered by ***Electrical Department*, IIT Bombay**

Coordinator, Team Pronites | Mood Indigo 2017 *May-Dec'17*
*Asia's largest college cultural festival with **141,000** footfall, **210+events**, **160+**international artists, **30+venues***
- Worked in **team** of **20** and responsible for execution of concerts with footfall **20,000**
- **Ideated** and revamped the structure for **LiveWire**, India largest and oldest semi-professional band event
- Lead a team of **20+** to execute India's largest student organized concerts attended by a crowd of **20,000**

Extra-Curriculars

- Volunteered for **Green Campus, IIT Bombay** under the **National Service Scheme** (NSS), IIT Bombay *[2016]*
- Conducted **Bio-Diversity Mapping** along Main Gate Road in association with **NSS**, IIT Bombay *[2016]*
- Participated in **RC Plane** and **Line Follower Bot** Competition organised by the **STAB**, IIT Bombay *[2017]*
- Attended **workshops** on Arduino and AVR microcontroller, conducted by **Electronics Club**, IIT Bombay *[2018]*
- Attended and successfully completed **Communication Workshop** by **Indian Training Co.** *[2020]*
- Contributed to **Open source** projects and successfully completed the **Hacktoberfest challenge** *[2019]*