**EE 6313 Advanced Microprocessors**

**Fall 2018 Project 2**

**Determination of best architecture for a Cache Controller used for signal processing**

**Submitted By:**

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**Overview:**

The goal of this project is to determine the best architecture for a cache controller that interfaces to a 16- bit microprocessor that is used for signal processing. While the microprocessor is general purpose in design and performs a number of functions, it is desired to speed up certain signal processing functions, such as those calculating the eigenvalues and eigenvectors of a system.

Here we check the largest hit in the performance was seen in the functions called choldc() and cholsl() functions.

The goal is to determine the best architecture for the 256 kB cache. The three degrees of freedom in the design are n-way set associativity,(N) burst length(bl), and write strategy(WS) (write-back or write-through) and Least Recently used strategy (LRU).Assume that the DRAM data bus is limited to 16 bits in width and bytes in data Block(B)

Equations for Calculations:

1. Size of the Cache: S= L\*N\*B
2. No of bits in the data block b= log(L)/log(2)
3. No .of line bits in the 24 bit address Bus l= log(L)/log(2)
4. No. of Tag bits in the 24 bit address bus = 24-l-b
5. No. of ways in the associativity= N
6. No of bytes in the memory= pow(2,w)/pow(2,b), Here w= no. of address bits
7. Read miss time= (90+ (BL-1)17)read\_miss\_count +1ns
8. Read hit time = (read\_cache\_count – read\_miss\_count) ns
9. Read dirty time = ( 90+(BL-1)17 )read\_dirty\_count ns
10. WS =1 ; Write miss time = ( 90+(BL-1)17 )write\_miss\_count+ 1 ns  
     Write dirty time =( 90+(BL-1)17 )write\_dirty\_count ns  
     Write hit time = (write\_line\_count – write\_miss\_count) ns  
     Write flush time = ( 90+(BL-1)17 )flush\_count ns  
     Total time = Write miss time + write dirty time + write hit time + write flush time
11. WS = 2; Write miss time = ( 90 )write\_miss\_count  
     Write dirty time =( 90+(BL-1)17 )write\_dirty\_count ns  
     Write hit time = (write\_line\_count – write\_miss\_count) \* 90 ns  
     Write through time = 90(write\_through\_mem) ns  
     Total time = Write miss time + write dirty time + write hit time + write through time
12. WS = 3; Write miss time = ( 90+(BL-1)17 )write\_miss\_count+ 1 ns  
     Write dirty time =( 90+(BL-1)17 )write\_dirty\_count ns  
     Write hit time = (write\_cache\_count – write\_miss\_count) \* 90 ns  
     Write through time = 90(write\_through\_mem) ns  
     Total time = Write miss time + write dirty time + write hit time + write through time
13. Total read time = read miss time + read dirty time + read hit time
14. Total time = Total read time + Total write time
15. The total Average Minimum Access Time can be calculated separately for a read and write hits occur in respective caches let us say (L1 cache, L2 cache)
16. Given by the general formula:

TAMACT = Thit  (on L1 cache)+ P miss (of cache L1(Thit (cache L2) +Pmiss (cache L2) T hit\_mem)