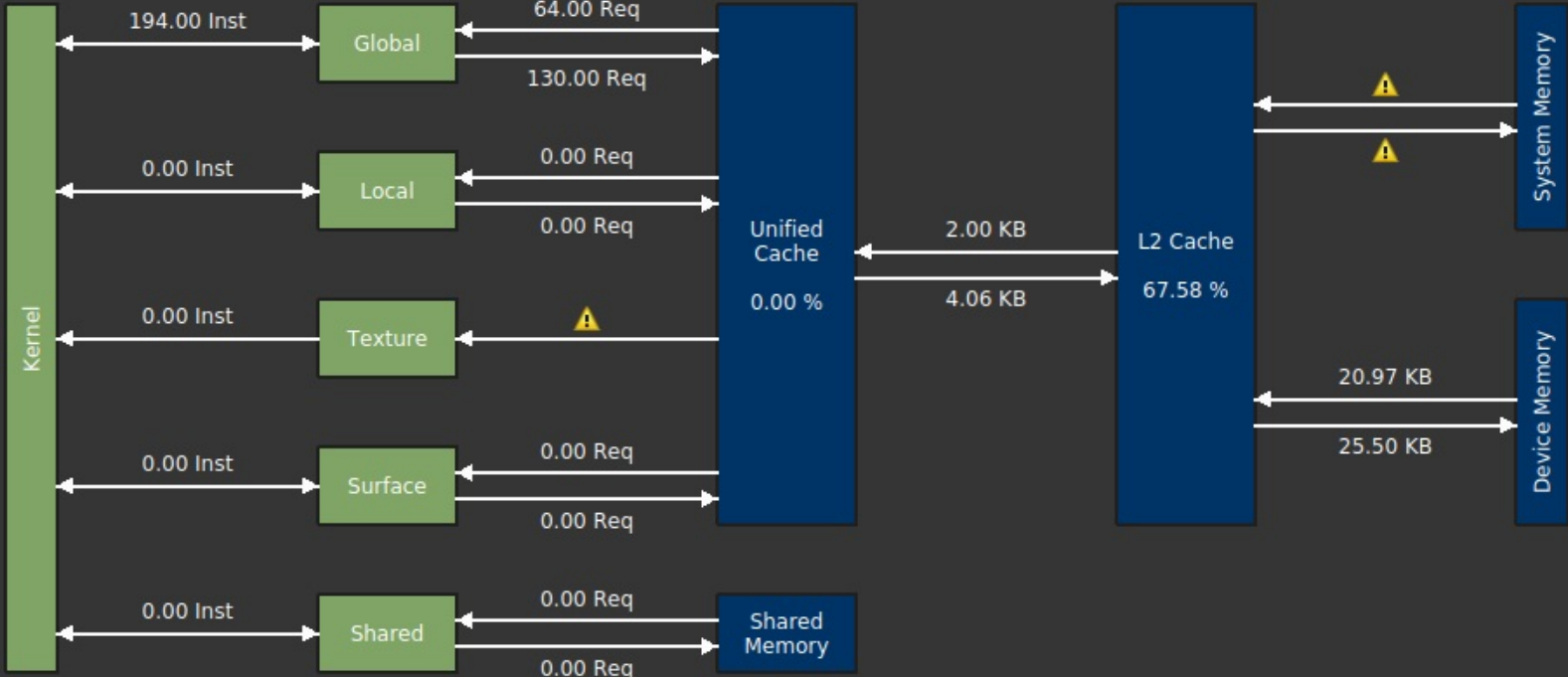


▼ Memory Workload Analysis

Detailed analysis of the memory resources of the GPU. Memory can become a limiting factor for the overall kernel performance when fully utilizing the involved hardware units (Mem Busy), exhausting the available communication bandwidth between those units (Max Bandwidth), or by reaching the maximum throughput of issuing memory instructions (Mem Pipes Busy). Detailed chart of the memory units. Detailed tables with data for each memory unit.

| | | | |
|----------------------------------|--------|--------------------|------|
| Memory Throughput [Mbyte/second] | 558.60 | Mem Busy [%] | 0.17 |
| L1 Hit Rate [%] | 0 | Max Bandwidth [%] | 0.17 |
| L2 Hit Rate [%] | 67.58 | Mem Pipes Busy [%] | 0.16 |

Memory Chart



Shared Memory

| | Instructions | Requests | % Peak | Bank Conflicts |
|---------------|--------------|----------|--------|----------------|
| Shared Load | 0 | 0 | 0 | 0 |
| Shared Store | 0 | 0 | 0 | 0 |
| Shared Atomic | 0 | - | - | - |
| Total | 0 | 0 | 0 | 0 |

First-Level (Unified) Cache

| | Instructions | SM->TEX Requests | % Peak | Hit Rate | TEX->L2 Requests | % Peak | L2->TEX Returns | % Peak | TEX->SM Returns | % Peak |
|----------------------|--------------|------------------|--------|----------|------------------|--------|-----------------|--------|-----------------|--------|
| Global Load Cached | 64 | 0 | 0 | 0 | - | - | 0 | 0 | 64 | 0.00 |
| Global Load Uncached | | 64 | 0.06 | - | - | - | 64 | 0.00 | | |
| Local Load Cached | 0 | 0 | 0 | 0 | - | - | 0 | 0 | | |
| Local Load Uncached | 0 | 0 | 0 | - | - | - | 0 | 0 | | |
| Surface Load | 0 | 0 | 0 | - | - | - | 0 | 0 | | |
| Texture Load | 0 | | | | | | | | | |
| Global Store | 130 | 130 | 0.12 | - | 130 | 0.00 | - | - | - | - |
| Local Store | 0 | 0 | 0 | - | 0 | 0 | - | - | - | - |
| Surface Store | 0 | 0 | 0 | - | 0 | 0 | - | - | - | - |
| Global Reduction | 0 | 0 | 0 | - | 0 | 0 | - | - | - | - |
| Surface Reduction | 0 | 0 | 0 | - | 0 | 0 | - | - | - | - |
| Global Atomic | | 0 | 0 | - | | | | | 0 | 0 |
| Global Atomic Cas | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 |
| Surface Atomic | | 0 | 0 | - | | | | | 0 | 0 |
| Surface Atomic Cas | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 |
| Loads | 64 | 64 | 0.06 | 0 | - | - | 64 | 0.00 | 64 | 0.00 |
| Stores | 130 | 130 | 0.12 | - | 130 | 0.00 | - | - | - | - |
| Total | 194 | 194 | 0.18 | 0 | 130 | 0.00 | 64 | 0.00 | 64 | 0.00 |

Second-Level (L2) Cache

| | TEX->L2 Requests | % Peak | L2->TEX Returns | % Peak | Total Bytes | Total Throughput |
|----------------------|------------------|--------|-----------------|--------|-------------|------------------|
| Global Load Cached | - | - | 0 | 0 | 0 | 0 |
| Global Load Uncached | - | - | 64 | 0.00 | 2,048 | 2,40,42,073.63 |
| Local Load Cached | - | - | 0 | 0 | 0 | 0 |
| Local Load Uncached | - | - | 0 | 0 | 0 | 0 |
| Surface Load | - | - | 0 | 0 | 0 | 0 |
| Texture Load | | | | | | |
| Global Store | 130 | 0.01 | - | - | 4,160 | 4,88,35,462.06 |
| Local Store | 0 | | - | - | 0 | 0 |
| Surface Store | 0 | 0 | - | - | 0 | 0 |
| Global Reduction | 0 | 0 | - | - | 0 | 0 |
| Surface Reduction | 0 | 0 | - | - | 0 | 0 |
| Global Atomic | | | 0 | 0 | | |
| Global Atomic Cas | 0 | 0 | 0 | 0 | 0 | 0 |
| Surface Atomic | | | | | | |
| Surface Atomic Cas | 0 | 0 | 0 | 0 | 0 | 0 |
| Loads | - | - | 64 | 0.00 | 2,048 | 2,40,42,073.63 |
| Stores | 130 | 0.01 | - | - | 4,160 | 4,88,35,462.06 |
| Total | 130 | 0.01 | 64 | 0.00 | 6,208 | 7,28,77,535.69 |

Device Memory (FB)

| | L2<->FB Sectors | % Peak | Bytes | Throughput |
|-------|-----------------|--------|--------|-----------------|
| Load | 671 | 0.08 | 21,472 | 25,20,66,115.70 |
| Store | 816 | 0.09 | 26,112 | 30,65,36,438.77 |
| Total | 1,487 | 0.17 | 47,584 | 55,86,02,554.47 |