Nayan Ramam

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Education

Georgia Institute of Technology | Atlanta, GA *August 2024 – Present*

B.S. in Electrical Engineering, GPA 4.00, Dean's List, IEEE-Eta Kappa Nu Honor Society Expected Graduation, December 2027

Relevant Coursework: Analog CMOS IC Design, HW/SW Programming (RISC-V & C), Signal Processing, Circuit Analysis

Research Experience

Analog Mixed-Signal Researcher | Integrated Computational Electronics Lab *October 2025 – Present*

- Designed schematic for current starved inverter-based envelope generator
- Compiled circuit on FPAA using proprietary RASP30 toolchain
- Testing/developing novel methodology to compile custom Python-HDL hybrid to floating-gate circuit for FPAA

Image Processing/Deep Learning Researcher | Intelligent Vision and Automation Lab *August 2025 – Present*

- Converting MATLAB codebase for indoor building mapping and routing to Python (12k+ LOC)
- Optimizing adaptive routing system to accommodate varying accessibility requirements
- Overhauling image processing and annotation capabilities with keypoint deep networks & convolutional neural networks

Lead Engineer + Project Manager | Interactive Music Group *August 2025 – Present*

- Leading development of Daisy Seed based drum machine/synthesizer
- Prototyping PCBs in KiCAD for MCU, SPI/I2C networked I/O (potentiometers, audio jacks, LCD, etc), and power circuitry
- Designing a novel force sensitive drum pad using mechanical keyboard switches and hall effect ICs
- Overseeing development of AI based patch generation software with integrated Daisy compiler

Digital Design/Hardware Systems Researcher | San José State University *May 2025 – August 2025*

- Adapted Analog Devices' IP for JESD204B to Lattice's Holoscan sensor bridge FPGA board
- Wrote Verilog link + physical layer to stream sensor data @ 6.125 Gbps to a host GPU for autonomous driving inference
- Used Lattice Radiant for comprehensive EDA toolflow (synthesis, place-&-route, timing analysis, simulation)

Team Lead + Lead Researcher | Math Modeling Student Research Group *August 2024 – Present*

- Leading mechanistic interpretability research team of 10 undergraduates and PhD candidates
- Architected a framework to quantify the polysemanticity of neurons in convolutional neural networks
- Developed a pipeline to generate and embed feature visualizations via gradient ascent
- Clustered embeddings of 5k+ feature visualizations with a modified Bayesian Information Criterion implementation
- Formulated a novel scoring metric that incorporates cluster count, angular separation, and density metrics
- Heading a second paper exploring feature steering through generalized circuit detection in large language models
- Creating a custom implementation of GPT2-Small with cross layer transcoders using TransformerLens & OpenCLT libraries

Academic Extracurriculars

Analog Mixed-Signal Design Engineer | Silicon Jackets *October 2025 – Present*

- Built and verified a digital inverter and a single stage amplifier (schematic, layout, DRC/LVS) in Cadence Virtuoso
- Learned MOSFET physics, modeling, & behaviors (Ohmic/saturation regions, channel length modulation, etc.)
- Designed, simulated, and verified a ring oscillator to meet power and frequency specifications (<1 mW avg. power draw, 500 MHz frequency) along with inverter-based buffer to drive 1 pF C_{load}

Digital Design Engineer | Silicon Jackets *January 2025 – Present*

- Engineered a SystemVerilog module through full stack (RTL, testbench, static timing analysis, P&R) to calculate greatest common denominator using the Euclidean algorithm (99.62% DUT coverage)
- Designing a fast divider module in SystemVerilog using Newton-Raphson & Goldschmidt algorithms
- Created a lightweight, hardware efficient look up table for calculating Newton-Raphson initial guesses
- Implemented block diagrams, state machines, Python code, and RTL for 4 division algorithms
- Performed constrained random verification across 10k+ test points to determine efficiency for RISC-V 32-bit processors

Skills

Programming Languages: Python, SystemVerilog, Verilog, VHDL, RISC-V, C, MATLAB

Software/Platforms: Cadence Virtuoso, KiCAD, PyTorch, SciPy, NumPy, Linux, Scilab, Lattice Radiant, Git

Hardware: FPAA, FPGA, Oscilloscope, DMM, Arduino/Teensy, Daisy Seed, Raspberry Pi, NI MyDAQ