Nayan Ramam

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Education

Georgia Institute of Technology | Atlanta, GA *August 2024 – Present*

B.S. in Electrical Engineering, GPA 4.00, Dean's List, IEEE-Eta Kappa Nu Honor Society Expected Graduation, December 2027

Relevant Coursework: Analog CMOS IC Design, Microelectronics/Semiconductor Physics, Signal Processing, Circuit Analysis

Skills

Programming Languages: Python, SystemVerilog, Verilog, VHDL, RISC-V, C, MATLAB

Software/Platforms: Cadence Virtuoso/ADE/Spectre/Pegasus, Siemens Calibre, KiCAD, PyTorch, sk-learn, Linux, Quartus, Git

Hardware: Field Programmable Analog Array (FPAA), FPGA, Oscilloscope, DMM, Arduino/Teensy, Raspberry Pi, Daisy Seed

Experience

Analog Mixed-Signal Researcher | Integrated Computational Electronics Lab *October 2025 – Present*

- Designed schematic for envelope generator circuit and compiled on FPAA using RASP30 toolchain
- Debugged and tested circuit using Digilent Analog Discovery and DMM
- Developing Python to Verilog netlist to GDSII compiler to allow ASIC synthesis

Lead Engineer + Project Manager | Interactive Music Group *August 2025 – Present*

- Leading development of Daisy Seed based drum machine/synthesizer
- Designing PCB in KiCAD for MCU, SPI/I2C networked I/O (potentiometers, audio jacks, LCD, etc), and power circuitry
- Prototyping a force and position sensitive drum pad using Velostat (piezoresistive film) and copper trace matrices
- Overseeing development of AI based patch generation software with integrated Daisy compiler

Digital Design/Hardware Systems Researcher | San José State University *May 2025 – August 2025*

- Adapted Analog Devices' IP for JESD204B to Lattice's Holoscan sensor bridge FPGA board
- Wrote Verilog link + physical layer to stream sensor data @ 6.125 Gbps to a host GPU for autonomous driving inference

Team Lead + Lead Researcher | Math Modeling Student Research Group *August 2024 – Present*

- Leading mechanistic interpretability research team quantifying polysemanticity in convolutional neural networks
- Developed a pipeline to generate and embed feature visualizations via gradient ascent
- Formulated a novel scoring metric that incorporates cluster count, angular separation, and density metrics

Image Processing/Deep Learning Researcher | Intelligent Vision and Automation Lab *August 2025 – February 2026*

- Converting MATLAB codebase for indoor building mapping and routing to Python with NumPy, SciPy, OpenCV (14k+ LOC)
- Generated 10+ unit tests to verify detection, extraction, and parsing functionality

Academic Extracurriculars

Analog Mixed-Signal Design Engineer | Silicon Jackets *October 2025 – Present*

- Learned MOSFET physics, modeling, & behaviors (Ohmic/saturation regions, channel length modulation, etc.)
- Engineered schematic & layout for ring VCO, buffer, single stage amplifier, and digital inverter using Cadence Virtuoso/Pegasus, simulated using Maestro (ADE Explorer/Assembler)

Digital Design Engineer | Silicon Jackets *January 2025 – Present*

- Developed a SystemVerilog module through full stack (RTL, testbench, static timing analysis, P&R) to calculate greatest common denominator using the Euclidean algorithm (99.62% DUT coverage)
- Implemented block diagrams, state machines, Python code, and RTL for a fast divider module
- Performed constrained random verification across 10k+ test points to determine efficiency for RISC-V 32-bit processors

Projects

Mixed-Signal CPU (Innovate ECE @ Georgia Tech) *February 2026 – Present*

- Leading a team of 6 building a RISC-V CPU with a mixed-signal accelerator to compute dot product
- Building and simulating switched capacitor and op-amp based implementations of Multiply-Accumulate (MAC)

Teleoperated Pipe-Building Robot (Robotech Hackathon) *January 2026*

- Implemented electrical & software systems for a robot with 3 DOF arm for IEEE Robotech hackathon (earned 2nd place)
- Built low-latency comms/telemetry stack including bidirectional ESP-NOW @ 100 Hz, USB serial @ 921600 baud
- Developed real-time monitoring GUI using PySide6 & PySerial to display servo position and packet loss
- Designed power distribution and control circuitry (PWM driver for servos, H-bridge for motors) driven by 4s LiPO battery