

C O M P U T E R A R C H I T E C T U R E P R O J E C T

32-BIT 5-STAGE PIPELINED RISC-V PROCESSOR

P R E S E N T E D B Y :

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WHY RISC-V PROCESSOR

RISC-V is an open-source, modular instruction set architecture. It is friendly to both industry and academia. Our project implements the RV32I base integer ISA.

OPEN-SOURCE ADVANTAGE

- Community-driven
- Flexible and adaptable
- Reduces licensing costs

OUR IMPLEMENTATION

- RV32I (base integer ISA)
- 5 pipeline stages
- Focus on efficiency

PIPELINE BREAKDOWN

Each stage processes instructions in one clock cycle. This enables the concurrent execution of up to five instructions, significantly enhancing performance.

IF (Instruction Fetch)

Reads instruction from memory (PC)

ID (Instruction Decode)

Decodes instruction, reads register operands

EXE (Execute)

Performs ALU operations, calculates branch targets.

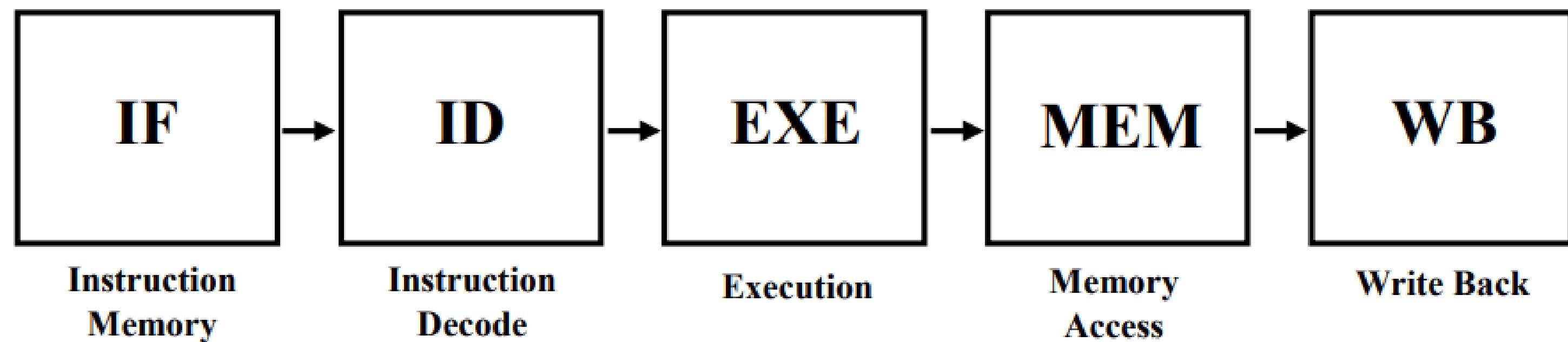
MEM (Memory Access)

Loads or stores data from/to memory

WB (Write Back)

Writes results back to the register file

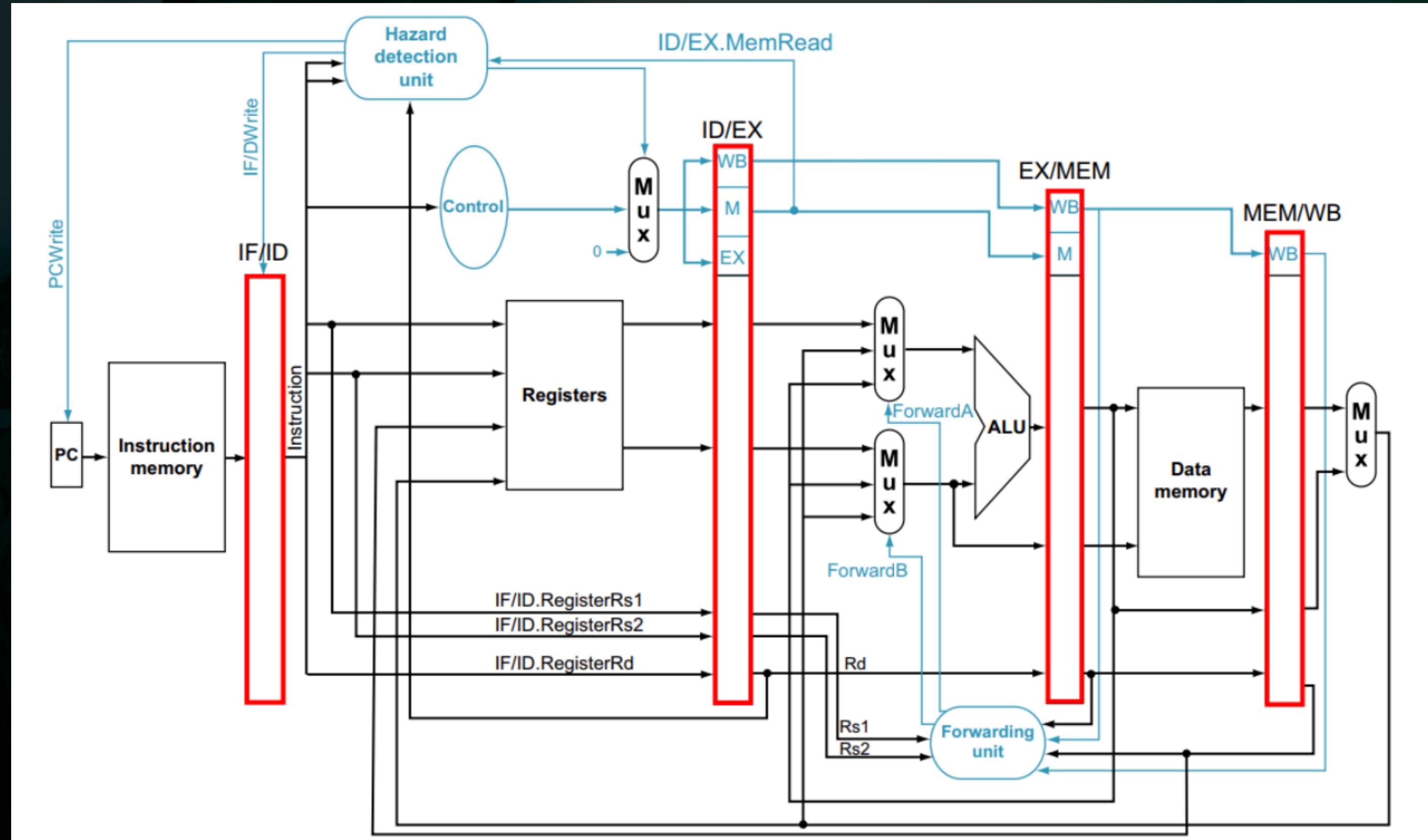
BLOCK DIAGRAM



INSTRUCTION FORMAT

31	27	26	25	24	20	19	15	14	12	11	7	6	0	
funct7		rs2		rs1		funct3			rd			opcode		R-type
	imm[11:0]			rs1		funct3			rd			opcode		I-type
imm[11:5]		rs2		rs1		funct3		imm[4:0]				opcode		S-type
imm[12 10:5]		rs2		rs1		funct3		imm[4:1 11]				opcode		B-type
	imm[31:12]								rd			opcode		U-type
	imm[20 10:1 11 19:12]								rd			opcode		J-type

PIPELINE DIAGRAM



MAJOR MODULES

Our processor integrates several crucial components. These modules ensure seamless data flow and control within the pipeline, including handling inter-stage communication and instruction processing.

- **Core Processing Units**

Program Counter, PC Mux, Instruction & Data Memory, Register File & ALU.

- **Control & Generation**

IF/ID, ID/EX, EX/MEM, MEM/WB registers ensure data integrity.

- **Hazard Management**

Control Unit and Immediate Generator for instruction handling.

- **Pipeline Interconnects**

Hazard Detection & Forwarding Units for optimal performance.

CONTROL AND DATA HAZARDS

Effective hazard handling is key to pipeline efficiency. Our design includes sophisticated units to mitigate data dependencies and manage control flow disruptions. This ensures correct program execution even with pipelining.

- **Forwarding Unit**

Resolves Read-After-Write (RAW) dependencies.

- **Pipeline Flush**

Flushed when a branch is taken to avoid incorrect instructions.

- **Hazard Detection**

Stalls pipeline on load-use hazards.

- **Branch Evaluation**

Evaluated in the MEM stage to determine target.

SUPPORTED INSTRUCTIONS

Our processor supports a comprehensive set of RV32I instructions. This includes arithmetic, logical, data transfer, and control flow operations, ensuring broad compatibility with RISC-V software.

R-Type

add, sub, and, or, sll,
srl, xor, slt, sltu

I-Type

addi, ori, slli, srli, xori,
slti, sltiu, jalr, lw, lb, lh

S-Type

sw, sb, sh

B-Type

beq, bne, blt, bge,
bltu, bgeu

J-Type

jal

U-Type

lui, auipc

SIMULATION AND TESTING

Rigorous simulation and testing confirmed processor functionality. We used Verilog testbenches in ModelSim. Display statements facilitated debugging. Waveforms were generated for detailed analysis.

Verilog Testbench

Waveform Analysis

Debugging Tools

Components Verified

PERFORMANCE METRICS

Our RISC-V processor demonstrates excellent performance. The low CPI indicates high efficiency. The impressive maximum frequency highlights its speed capabilities, making it suitable for various applications.

29 Instructions Executed

Total instructions processed during test.

1.31 CPI

Cycles per instruction, indicating efficiency.

38 Clock Cycles

Total cycles for execution.

4GHz Max F

Achievable operating speed based on clock period.

KEY TAKEAWAYS

We have successfully designed and verified a 32-bit pipelined RISC-V CPU. Its modular design allows for future enhancements. This project provides a robust foundation for more complex processor designs.

Fully Functional

Complete 32-bit pipelined RISC-V CPU.

Modular Design

Scalable architecture for future expansion.

Hazard Handling

Includes robust hazard and branch management.

Future Scope

Branch prediction, and cache integration.

WEB SIMULATIONS

RISC-V 5-Stage Pipelined Processor

Control Panel

Start Auto Simulation

Reset

Cycle: 5

Pipeline Stages

IF: sw x4, 4(x2)

ID: lw x4, 0(x2)

EX: sub x3, x2, x1

MEM: add x2, x1, x1

WB: addi x1, x0, 5

WEB SIMULATIONS

Registers

x0: 0	x1: 2	x2: 4	x3: 6	x4: 8	x5: 10	x6: 12	x7: 14	x8: 16
x9: 18	x10: 20	x11: 22	x12: 24	x13: 26	x14: 28	x15: 30	x16: 32	x17: 34
x18: 36	x19: 38	x20: 40	x21: 42	x22: 44	x23: 46	x24: 48	x25: 50	x26: 52
x27: 54	x28: 56	x29: 58	x30: 60	x31: 62				

Data Memory

M[0]: 0	M[4]: 4	M[8]: 8	M[12]: 12	M[16]: 16	M[20]: 20	M[24]: 24	M[28]: 28	M[32]: 32
M[36]: 36	M[40]: 40	M[44]: 44	M[48]: 48	M[52]: 52	M[56]: 56	M[60]: 60		

WEB SIMULATIONS

Control Signals

RegWrite: 1

MemRead: 0

MemWrite: 0

Statistics

Instructions: 7

Stalls: 0

CPI: 1.71

THANK YOU...!

