32-bit 5-Stage Pipelined RISC-V Processor

WaveForm Analysis Report

By

1	Muhammad Yasir	Roll No 37
2	Rehan Ali (Lead)	Roll No 15
3	Shariq Khan	Roll No 39
4	Rayan Badar	Roll No 18



Department of Computer Sciences

Namal University Mianwali, Pakistan

Submission Date: 13th June, 2025

1 Simulation Waveforms

1.1 Program Counter (PC)

⇒ clk	0										
→ rst	0										
→ PCWrite → pc_in → pc_out	1										
⊕ 🌧 pc_in	20	4				8			12		
+ > pc_out	16	0				4			8		
,											

1.2 PC Adder and PC Mux

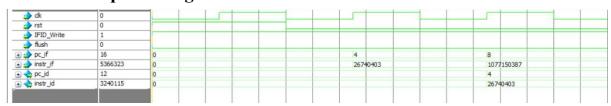


					8			12		
pc_branch	4	0								
pc_select	0									
pc_in pc_branch pc_select pc_out	20	4			8			12		

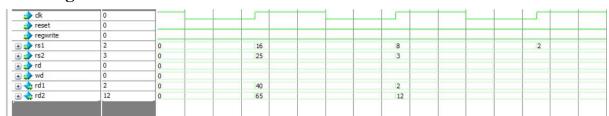
1.3 Instruction Memory



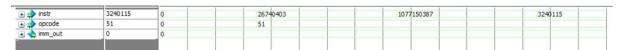
1.4 IF/ID Pipeline Register



1.5 Register File



1.6 Immediate Generator



1.7 Control Unit

🛨 🌧 instrct	51	0	51		
branch	0				
memread	0				
memtoreg	0				
memwrite	0				
alusrc 🔷	0				
regwrite	1				
🕁 🔷 aluop	2	0	2		

1.8 Hazard Detection Unit

DEX_rd DEX_rd DEX_rs1 DEX_memRead PCWrite	5	0					13			5	
± 🍁 IFID_rs1	2	0		16			8			2	
→ IFID_rs2	3	0		25			3				
	0										
PCWrite	1										
♣ IFID_Write ♣ stall	1										
🔷 stall	0										
V											

1.9 Hazard Control Mux



1.10 ID/EX Pipeline Register

→ dk	0				
→ rst	0				
± pc_id pc_id	12	0	4	8	12
± 🍁 rd1_id	2	0	40	2	
± 🔷 rd2_id	12	0	65	12	
+ 🍁 immGen_id	0	0			
🛨 🧼 inst_id	3240115	0	26740403	1077150387	3240115
branch_id	0				
memread_id	0				
memtoreg_id	0				
memwrite_id	0				
alusrc_id	0				
regwrite_id	1				
→ aluop_id	2	0	2		
± 🔷 pc_ex	8	0		4	8
🛨 🔷 rd1_ex	2	0		40	2
+ 🔷 rd2_ex	12	0		65	12
→ immGen_ex	0	0			
+ 🔷 inst_ex	1077150387	0		26740403	1077150387
branch_ex	0				
♠ memread_ex	0				
memtoreg_ex	0				
memwrite_ex	0				
alusrc_ex	0				
regwrite_ex	1				
+ 🔷 aluop_ex	2	0		2	
+ 🔷 rd_ex	5	0		13	5
+ 🔷 rs1_ex	8	0		16	8
± 🔷 rs2_ex	3	0		25	3

1.11 Forwarding Unit

★ rs1_IDEX	8	0				16		8	
→ → rs2_IDEX	3	0				25	10	3	1
<u>→</u>	13	0						13	
<u>→</u>	0	0							
EXMEM_RegWrite	1								
♠ MEMWB_RegWrite	0								
± 🔷 fwd_A	0	0							
→ 🏠 fwd_B	0	0							-

1.12 ALU and ALU Control

± 💠 A	2	0				40		2	
± 🗼 B	12	0				65		12	
+ 🔷 ALUcontrol_In	1	0						1	
	4294967286	0				105		429	967286
Zero	0								

	2	0				2				
<u>→</u>	32	0							32	
<u>→</u> op_select	0	0								
→ control_signal	1	0							1	

1.13 ALU Input Muxes

ex_data ex_data ex_data ex_data ex_data	2	0				40			2	
→ mem_data	0	0								
ex_data	105	0							105	
→ fwd_A	0	0								
→ dalu_A → alu_A	2	0				40			2	
V										

★ reg_data 12 0 65 12 ★ mem_data 0 0 105 ★ mm_data 0 0 105 ★ ALUSerc 0 0 105 ★ alu_B 12 0 65 12 ★ base_data 12 0 65 12								105	
	0 0							105	
→ imm_data 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0							1	
★ prod B 0 0 ★ alu_B 12 0 ★ base_data 12 0 65 12 12 0									
• ♦ alu_B 12 0 65 12 • ♦ base_data 12 0 65 12	0								
• base_data 12 0 65 12	2 0					65		12	
	2 0					65		12	
	_	0 0	0 0	0 0	0 0	0 0			

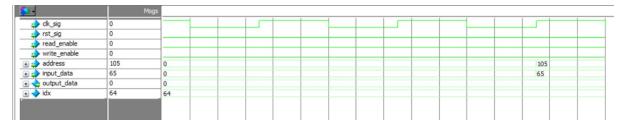
1.14 Branch Adder



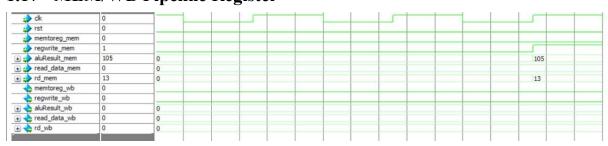
1.15 EX/MEM Pipeline Register

			1	1		1	1			1	1			
	0													
	0													
branch_ex	0													
memread_ex	0													
→ memtoreg_ex	0													
memwrite_ex	0													
regwrite_ex	1								0					
zero_ex	0													
	8	0						4				8		
<u>→</u> aluResult_ex	4294967286	0						105				429	967286	
→ rd2_ex	12	0						65				12		
→ → rd_ex	5	0						13				5		
branch_mem	0													
memread_mem	0													
memtoreg_mem	0													
memwrite_mem	0													
regwrite_mem	1													
zero_mem	0													
<u>→</u> jumpSum_mem	4	0										4		
	105	0										105		
→ rd2_mem	65	0										65		
→ rd_mem	13	0										13		

1.16 Data Memory



1.17 MEM/WB Pipeline Register



1.18 Writeback Mux

	0	0			105			4294	967286		
mem_data	0	0									
memtoreg	0										
⊕ 💠 wb_data	0	0			105			4294	967286		
,											