

# **32-bit 5-Stage Pipelined RISC-V Processor**

## **WaveForm Analysis Report**

**By**

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# 1 Simulation Waveforms

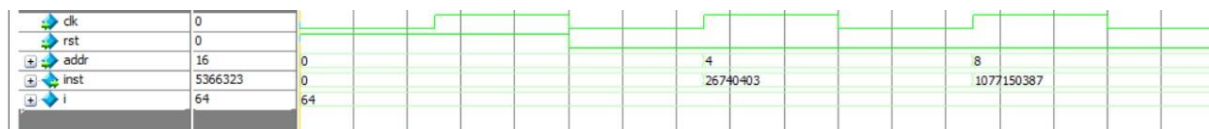
## 1.1 Program Counter (PC)



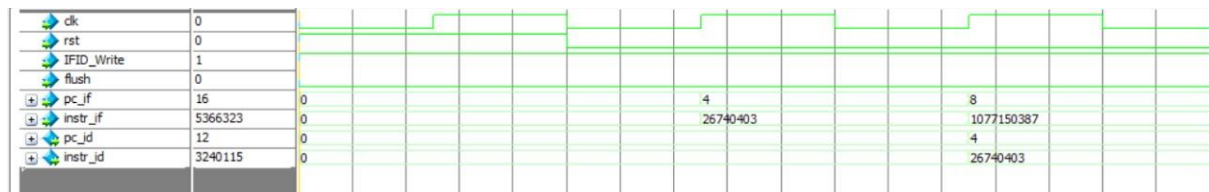
## 1.2 PC Adder and PC Mux



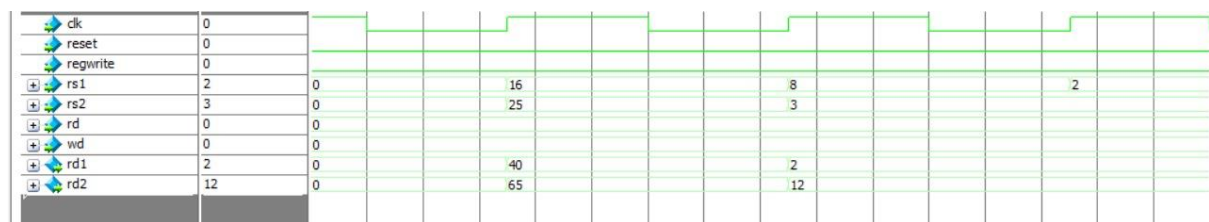
## 1.3 Instruction Memory



## 1.4 IF/ID Pipeline Register



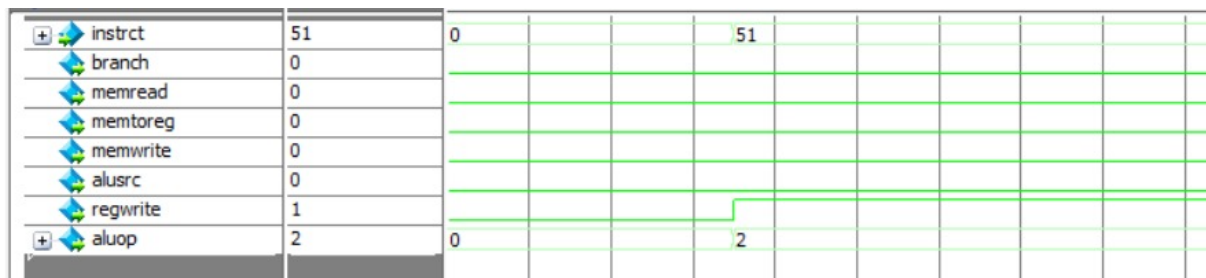
## 1.5 Register File



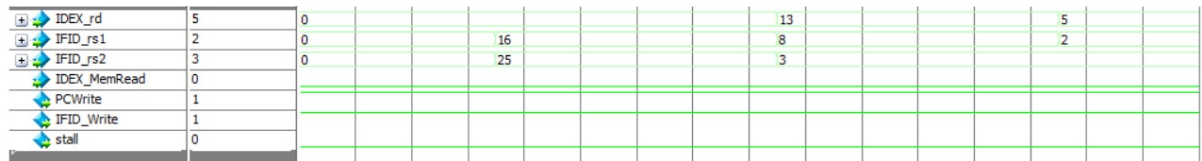
## 1.6 Immediate Generator



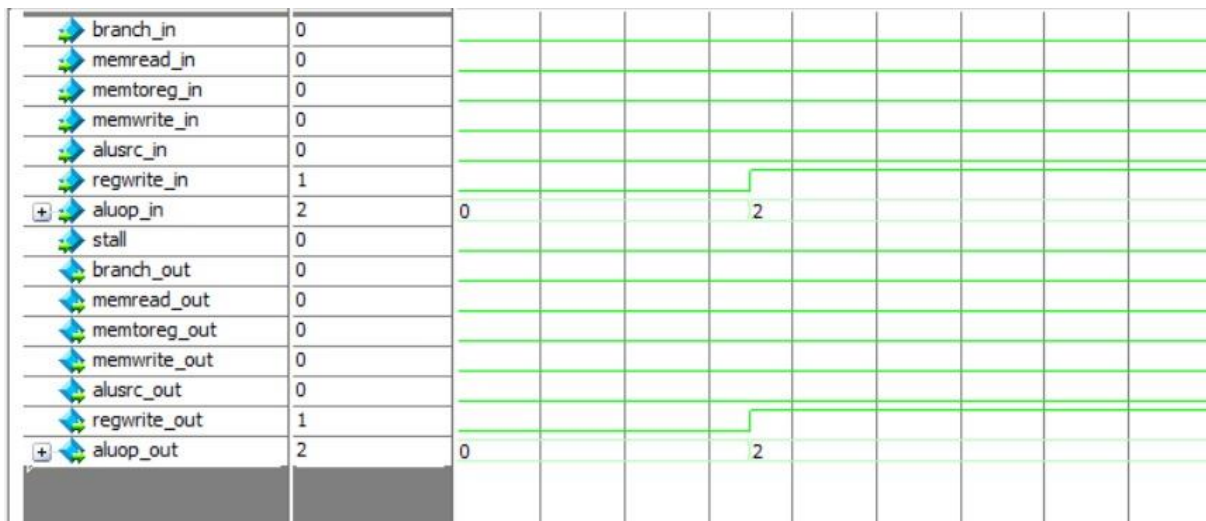
## 1.7 Control Unit



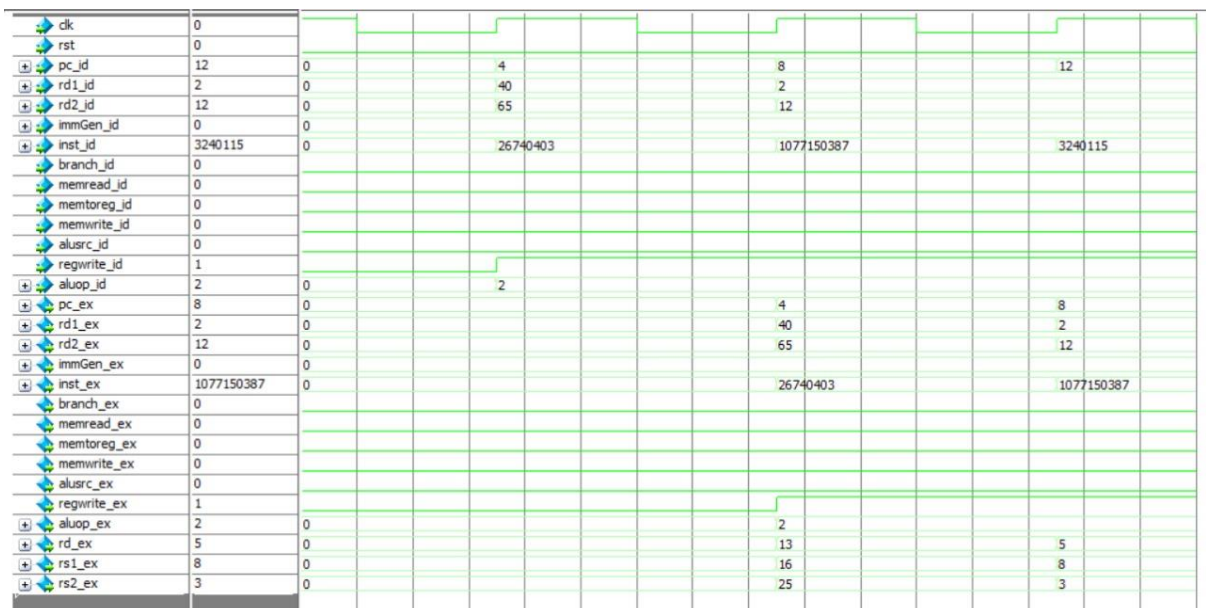
## 1.8 Hazard Detection Unit



## 1.9 Hazard Control Mux



## 1.10 ID/EX Pipeline Register



## 1.11 Forwarding Unit

[illegible]

## 1.12 ALU and ALU Control

[illegible][illegible]

### 1.13 ALU Input Muxes

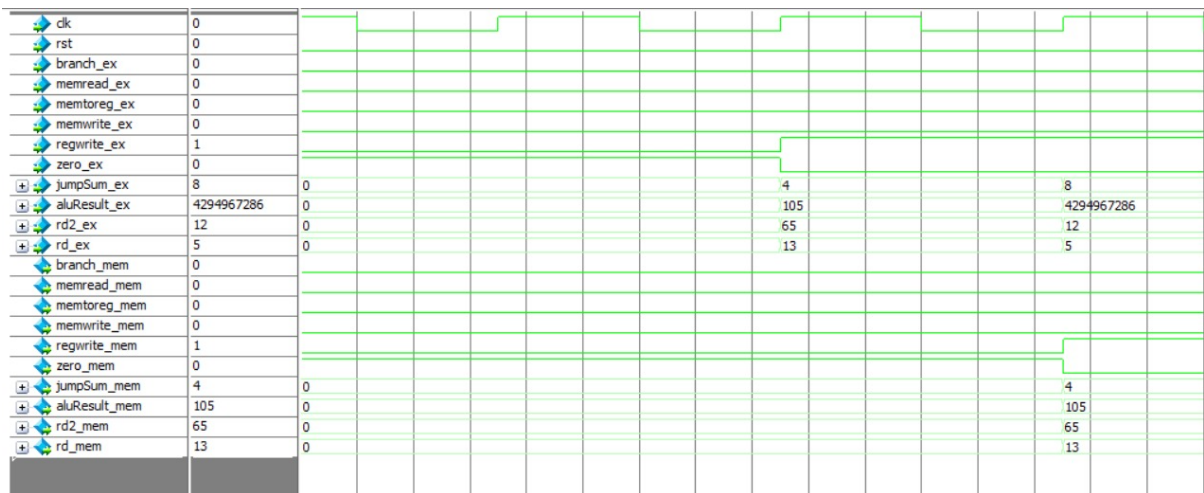
+ reg_data	2	0							-40				2		
+ mem_data	0	0													
+ ex_data	105	0											105		
+ fwd_A	0	0													
+ alu_A	2	0							-40				2		

+	reg_data	12	0						65					12	
+	mem_data	0	0												
+	ex_data	105	0											105	
+	imm_data	0	0												
	ALUSrc	0													
+	fwd_B	0	0												
+	alu_B	12	0						65					12	
+	base_data	12	0						65					12	

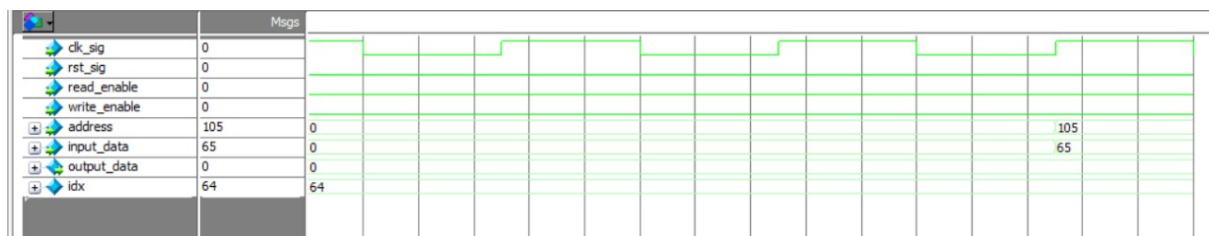
### 1.14 Branch Adder

[illegible]

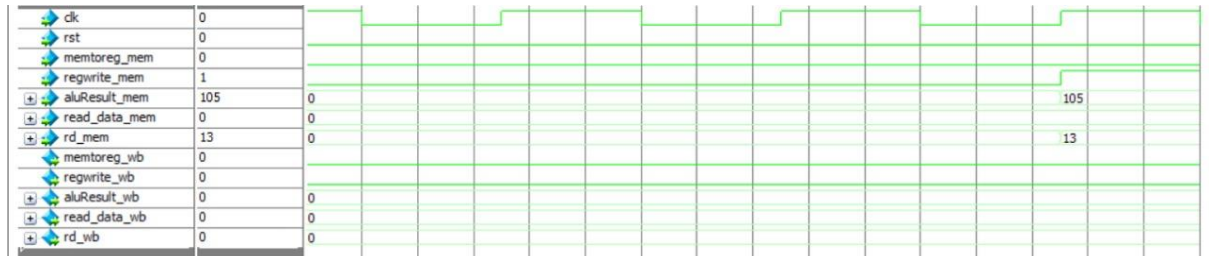
## 1.15 EX/MEM Pipeline Register



## 1.16 Data Memory



## 1.17 MEM/WB Pipeline Register



## 1.18 Writeback Mux

