32-bit 5-Stage Pipelined RISC-V Processor

WaveForm Analysis Report

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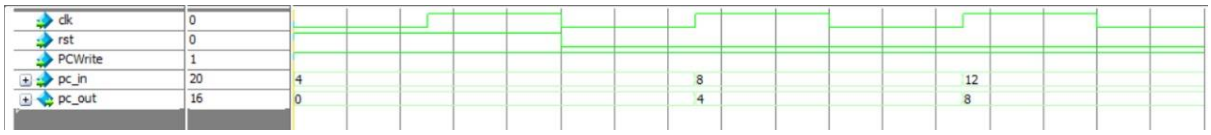
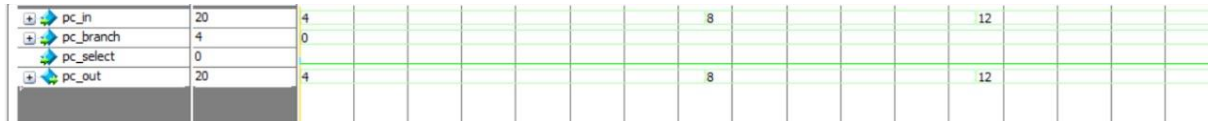
1 Simulation Waveforms

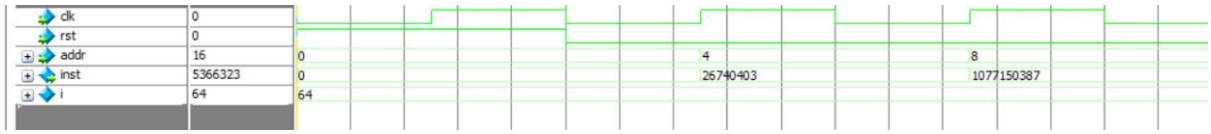
1.1 Program Counter (PC)



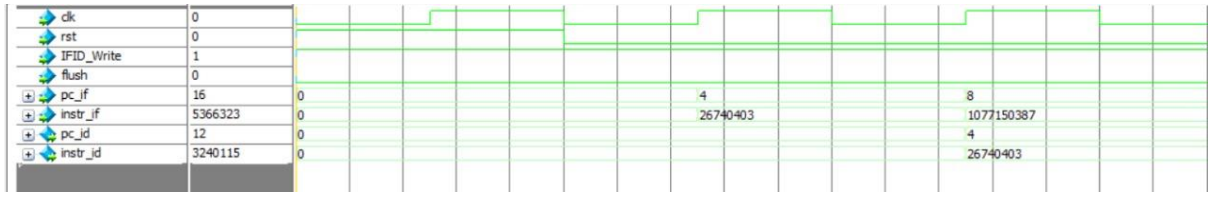
1.2 PC Adder and PC Mux



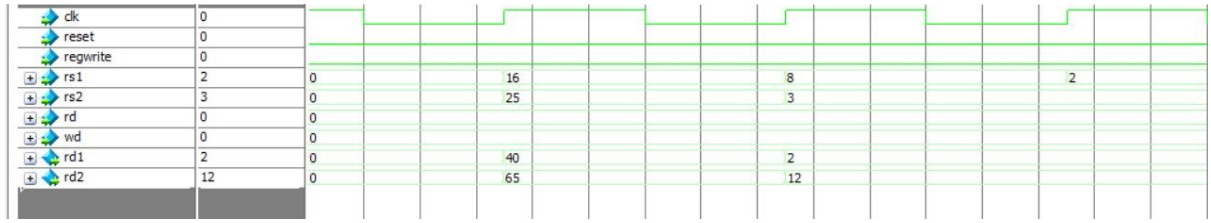
1.3 Instruction Memory



1.4 IF/ID Pipeline Register

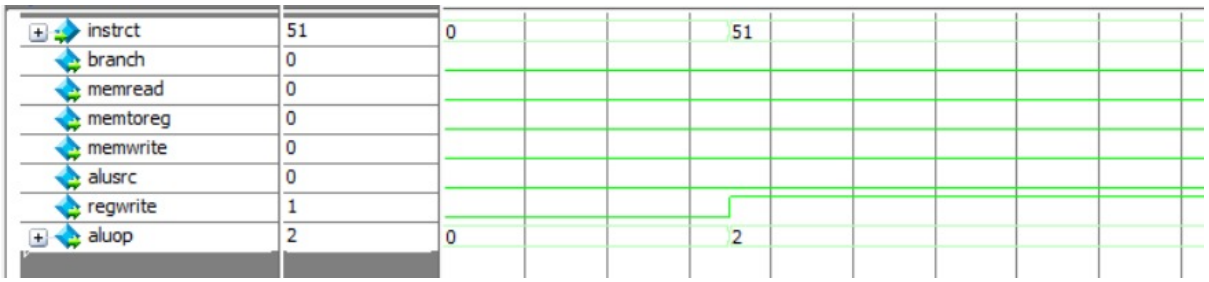


1.5 Register File

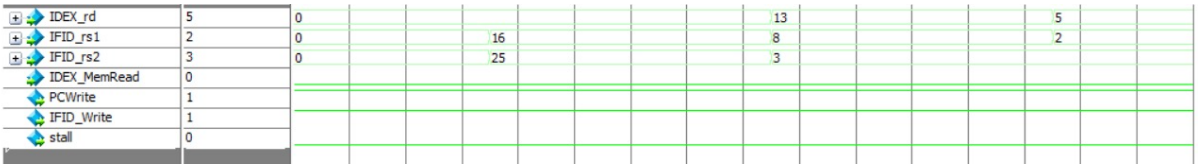


1.6 Immediate Generator

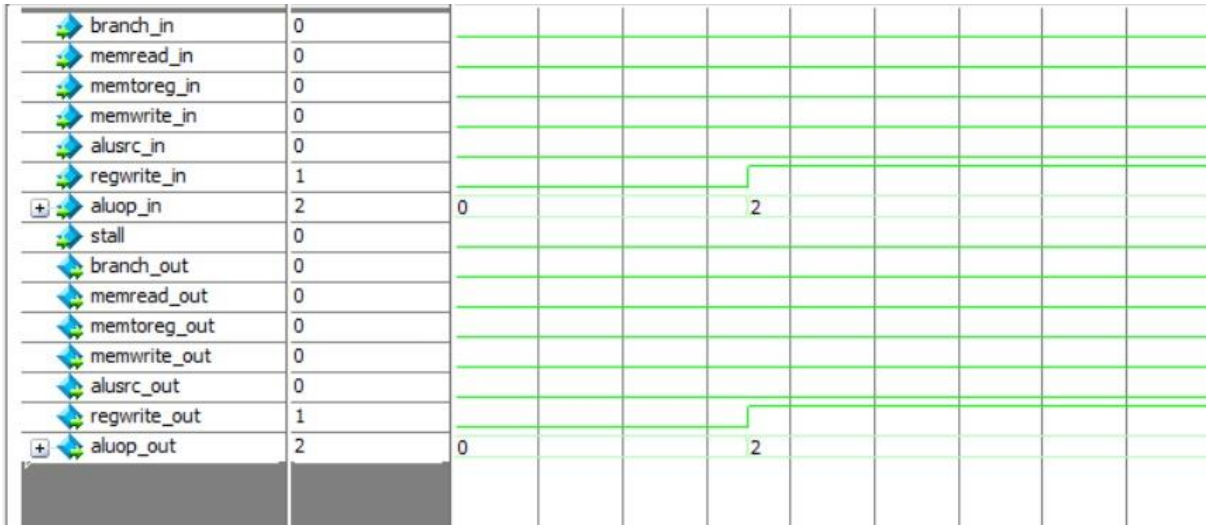
1.7 Control Unit



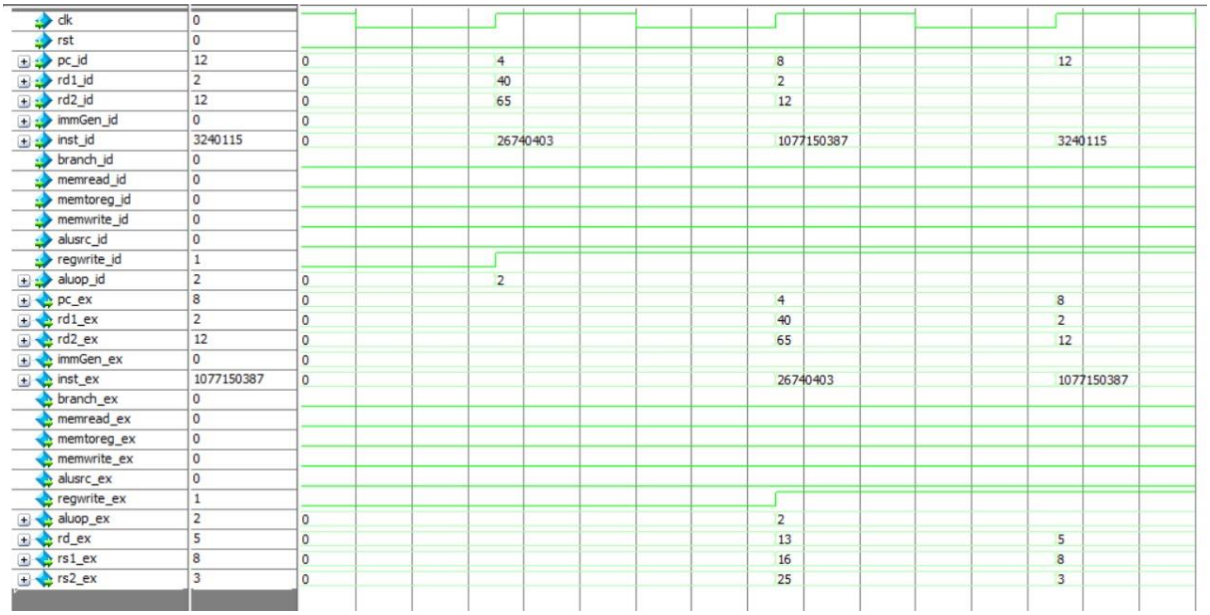
1.8 Hazard Detection Unit



1.9 Hazard Control Mux

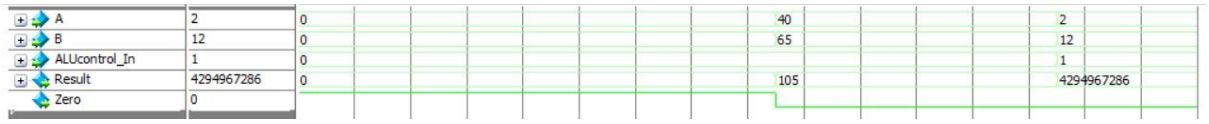


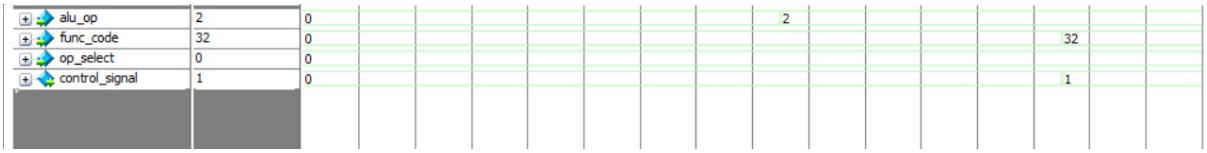
1.10 ID/EX Pipeline Register



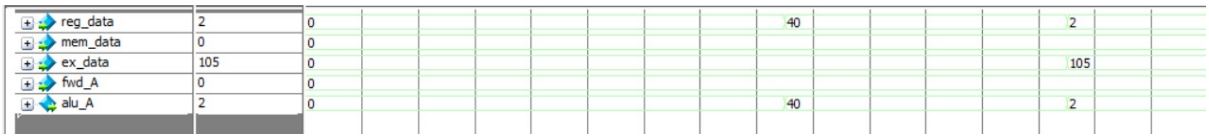
1.11 Forwarding Unit

1.12 ALU and ALU Control



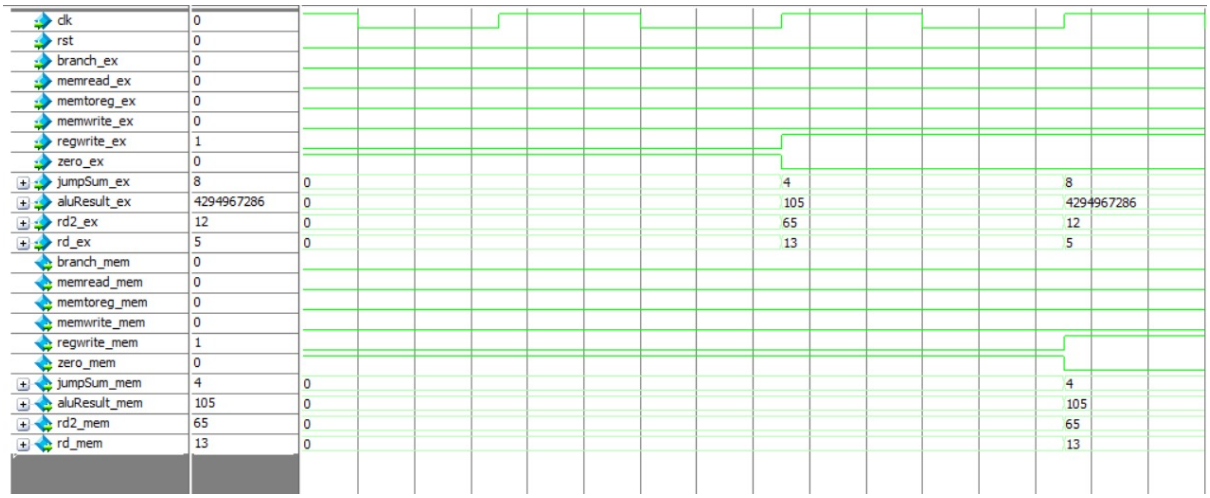


1.13 ALU Input Muxes

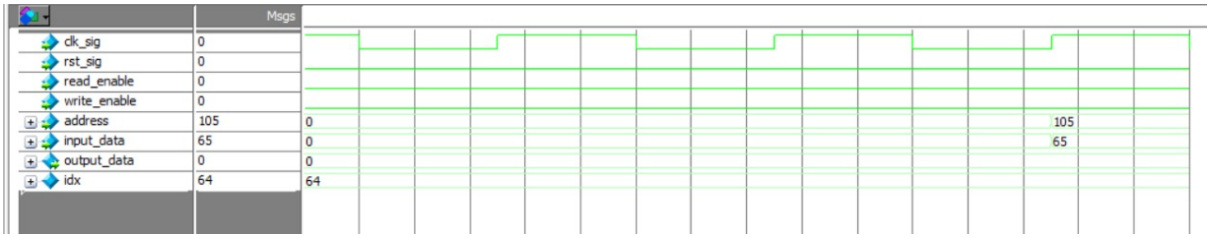


1.14 Branch Adder

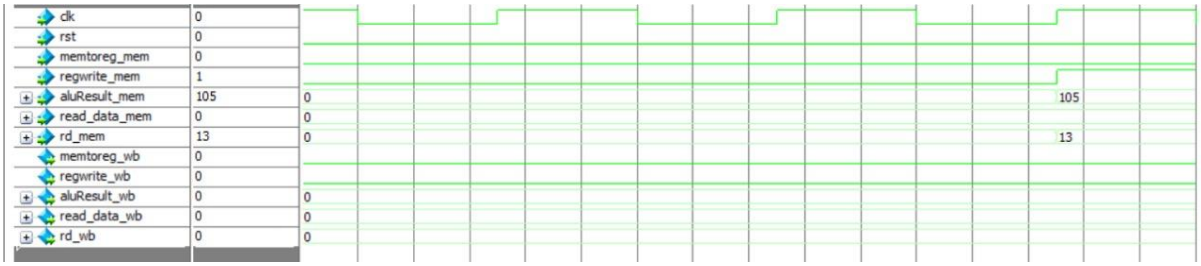
1.15 EX/MEM Pipeline Register



1.16 Data Memory



1.17 MEM/WB Pipeline Register



1.18 Writeback Mux