**Subject Code : 17MCA1C3**

**JAMAL MOHAMED COLLEGE (Autonomous)**

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**Objective Type Questions**

**Department of COMPUTER SCIENCE**

**Semester : First UG / PG : PG - MCA**

**Title of the Paper : Core III : COMPUTER ORGANISATION AND ARCHITECTURE**

**UNIT-I**

1. The base of an octal number system is \_\_\_\_\_\_.

a. 2 b. 4 c. 8 d. 16

2. What number system has a base of 16?

a. Decimal b. Binary c. Octal d. Hexadecimal

3. A binary system has \_\_\_\_ digits.

a. 2 b. 4 c. 8 d. 16

4. The binary equivalent of the decimal number 15 is \_\_\_\_\_\_.

a. 1101 b. 1111 c. 1010 d. 1110

5. The decimal equivalent of the binary number 1011 is \_\_\_\_\_\_.

a. 10 b. 13 c. 12 d. 11

6. The number of digits in octal system is \_\_\_\_\_\_.

a. 2 b. 4 c. 8 d. 16

7. The digit F in hexadecimal system is equivalent to \_\_\_ in decimal system.

a. 15 b. 13 c. 12 d. 10

8. The number BCA is a \_\_\_\_\_\_ number.

a. Decimal b. Binary c. Octal d. Hexadecimal

9. The value of 101 + 110 is \_\_\_\_\_\_\_.

a. 1101 b. 1011 c. 1010 d. 1110

10. The value of 11 x 11 is \_\_\_\_\_\_\_.

a. 1101 b. 1011 c. 1001 d. 1110

11. The value of 1010 - 0101 is \_\_\_\_\_\_\_.

a. 0100 b. 0011 c. 0001 d. 0101

12. The value of 1001 / 11 is \_\_\_\_\_\_\_.

a. 10 b. 11 c. 01 d. 00

13. The 2421 code of 9 is \_\_\_\_\_\_.

a. 1111 b. 1100 c. 1001 d. 1110

14. What is the Excess-3 value of decimal 6?

a. 1111 b. 1100 c. 1001 d. 1110

15. Which of the following is an alphanumeric code?

a. BCD b. ASCII c. Gray d. 2421

16. EBCDIC is a \_\_\_\_\_ code.

a. 8-bit b. 7-bit c. 6-bit d. 4-bit

17. The BCD equivalent of 98 is \_\_\_\_\_\_\_\_.

a. 10001001 b. 10011000 c. 1001 1001 d. 11101010

18. Which of the following is an even parity word?

a. 11110 b. 11001 c. 10011 d. 11100

19. Which of the following is an odd parity word?

a. 11110 b. 11001 c. 10010 d. 11101

20. Which of the following concept is used for error detection?

a. inversion b. logic c. parity d. complement

**UNIT-II**

21. A NOT gate is also called \_\_\_\_\_\_\_.

a. subtractor b. adder c. inverter d. multiplier

22. The Boolean expression of an AND gate is \_\_\_\_\_\_.

a. AB b. A+B c. AB’ d. A’B

23. A NAND gate is constructed using \_\_\_\_\_ and \_\_\_\_\_ gates.

a. OR, NOT b. AND, NOT c. XOR, NOT d. OR, AND

24. Which one of the following is a universal gate?

a. OR b. AND c. XOR d. NAND

25. The NOR gate is OR gate followed by \_\_\_\_\_\_\_ gate.

a. NOT b. AND c. XOR d. NAND

26. The output of a NAND gate is 0 if \_\_\_\_\_\_\_\_.

a. all the inputs are 1s b. all inputs are 0s

c. any input is 0 d. any input is 1

#### 27. How many truth table entries are necessary for a three-input AND gate?

a. 2 b. 4 c. 16 d. 8

28. In the Boolean algebra, a variable has \_\_\_\_\_\_\_\_ different states.

a. 1 b. 4 c. 2 d. 3

29. X + X.Y = ?

a. 1 b. Y c. X d. X+Y

30. A + Ā = ?

a. 1 b. A c. 0 d. Ā

31. A + Ā.B = ?

a. A b. A+B c. B d. Ā

32. A(B+C) = ?

a. A b. B+C c. AB+AC d. ABC

33. (A+B+C)’ = ?

a. A+B+C b. A’.B’.C’ c. AB+AC d. ABC’

34. Which of the following circuits is suitable for SOP expression?

a. OR-AND b. NOT-AND c. NAND-OR d. AND-OR

35. Which of the following circuits is suitable for POS expression?

a. OR-AND b. NOT-AND c. NAND-OR d. AND-OR

36. There are \_\_\_\_ minterms for three variables.

a. 2 b. 4 c. 8 d. 16

37. A group of two adjacent 1’s is called a \_\_\_\_\_\_\_.

a. quad b. pair c. octet d. map

38. A \_\_\_\_\_ is a group of eight adjacent 1’s.

a. quad b. pair c. octet d. map

39. There are \_\_\_\_\_ cells in a 4-variable Karnaugh map.

a. 4 b. 12 c. 8 d. 16

40. A group is said to be \_\_\_\_\_\_\_ if all its 1’s are used by other groups.

a. overlapped b. redundant c. folded d. adjacent

**UNIT-III**

41. A multiplexer is also called as a \_\_\_\_\_\_\_\_.

a. decoder b. encoder c. data selector d. multiplier

42. A 4-to-1 multiplexer consists of \_\_\_\_\_\_ select signals.

a. 4 b. 2 c. 1 d. 5

43. Multiplexing means transmitting a number of inputs signals over \_\_\_\_\_\_.

a. 1 line b. 2 lines c. many lines d. 3 lines

44. Which of the following represent single input multiple output switch?

a. Multiplexer b. Demultiplexer c. decoder d. encoder

45. A 1-to-8 demultiplexer consists of \_\_\_\_\_\_ select signals.

a. 4 b. 3 c. 2 d. 8

46. Demultiplexing means transmitting a single input signal over \_\_\_\_\_\_.

a. 1 line b. 2 lines c. many lines d. 3 lines

47. A decoder with 3 inputs consists of \_\_\_\_\_\_ output lines.

a. 8 b. 2 c. 4 d. 16

48. An octal encoder consists of \_\_\_\_\_\_\_ output lines.

a. 8 b. 2 c. 4 d. 3

49. A \_\_\_\_\_\_\_ is a combinational logic circuit that converts binary information from *n* coded inputs to a maximum of *2n*unique outputs.

a. Multiplexer b. Demultiplexer c. decoder d. encoder

50. A ­­­­\_\_\_\_\_\_\_is a combinational circuit that performs the reverse operation of a decoder.

a. Multiplexer b. Demultiplexer c. decoder d. encoder

51. A half adder has two inputs and \_\_\_\_\_\_ outputs.

a. 1 b. 2 c. 4 d. 3

52. A combinational circuits that finds the sum of two bits is called \_\_\_\_\_\_\_.

a. half adder b. half subtractor c. decoder d. full adder

53. A combinational circuits that finds the difference between two bits is called \_\_\_\_\_\_\_.

a. half adder b. half subtractor c. decoder d. full adder

54. The outputs of a full adder are sum and \_\_\_\_\_\_\_\_.

a. borrow b. difference c. carry d. add

55. A full adder has \_\_\_\_\_\_inputs and two outputs.

a. 1 b. 2 c. 4 d. 3

56. A combinational circuits that finds the sum of three bits is called \_\_\_\_\_\_\_.

a. half adder b. half subtractor c. full subtractor d. full adder

57. A combinational circuits that finds the sum of two binary words is called \_\_\_\_\_\_\_\_\_.

a. parallel adder b. half subtractor c. half adder d. full adder

58. The 2’s complement of 10010 is \_\_\_\_\_\_\_.

a. 10011 b. 01101 c. 10010 d. 01110

59. Which of the following gates is used as a controlled inverter \_\_\_\_\_\_\_\_.

a. OR b. AND c. XOR d. NAND

60. A BCD adder finds the sum of two \_\_\_\_\_\_ numbers.

a. binary b. BCD c. decimal d. hexadecimal

**UNIT-IV**

61. Sequential circuits are made up of \_\_\_\_\_\_\_\_.

a. flipflops b. decoders c. combinational circuits d. multiplexers

62. A \_\_\_\_\_\_\_  is one whose outputs depend not only on its current inputs, but also on the precious inputs.

a. combinational circuit b. sequential circuit c. logic circuit d. adder circuit

63. Which one of the following is an example of a sequential circuit?

a. Multiplexer b. Demultiplexer c. register d. encoder

64. A ­­­­\_\_\_\_\_\_ is a circuit with two stable states, used to store binary data.

a. flipflop b. decoder c. encoder d. multiplexer

65. In flipflop one output is \_\_\_\_\_\_\_.

a. greater than the other b. complement of the other

c. lesser than the other d. same as the other

66. When an inverter is placed between both inputs of the SR flipflop, then the resulting flipflop is \_\_\_\_\_\_\_\_\_.

a. T flipflop b. D flipflop c. JK flipflop d. RS flipflop.

67. In SR flipflop, S stands for \_\_\_\_\_\_\_.

a. Static b. Stable c. Systematic d. Set

68. A D flipflop consists of \_\_\_\_\_\_\_\_.

a. one inverter b. two inverters c. one buffer d. two buffers

69. Placing an inverter between J and K inputs results in a \_\_\_\_\_\_.

a. T flipflop b. D flipflop c. JK flipflop d. RS flipflop.

70. Flip flop when storing logic 0 is considered as \_\_\_\_\_\_.

a. static b. set c. rest d. reset

71. S=0, R=0 in a SR flipflop results in \_\_\_\_\_\_\_ state.

a. set b. reset c. no change d. indeterminate

72. J=0, K=0 in a JK flipflop results in \_\_\_\_\_\_\_ state.

a. set b. reset c. no change d. indeterminate

73. J=1, K=1 in a JK flipflop results in \_\_\_\_\_\_\_ state.

a. set b. reset c. no change d. toggle

74. In a T-flipflop, T stands for \_\_\_\_\_\_\_.

a. Toggle b.Trigger c. Timing d. Test

75. When the clock input is low, the flipflop is in \_\_\_\_\_\_\_\_ state.

a. set b. previous c. reset d. indeterminate

76. A register that is designed to allow the bits of its contents to be moved to left or right is called as \_\_\_\_\_\_\_\_.

a. shift register b. counter c. flipflop d. buffer

77. A circulating register is also called as a \_\_\_\_\_\_\_\_\_.

a. shift register b. ripple counter c. ring counter d. buffer

78. How many flipflops are required to construct a mod-5 counter?

a. 5 b. 2 c. 4 d. 3

79. A \_\_\_\_\_\_\_\_ counter is also called as a parallel counter.

a. synchronous b. asynchronous c. ring d. shift

80. A \_\_\_\_\_\_\_\_ counter is also called as a serial counter.

a. synchronous b. asynchronous c. ring d. shift

**UNIT-V**

81. A stack is a \_\_\_\_\_\_\_ memory.

a. FIFO b. LIFO c. FILO d. LILO

82. The register that holds the address of the top element of stack is called \_\_\_\_\_\_\_\_.

a. stack pointer b. program counter c. pointer register d. instruction register

83. In a stack, the operation of insertion is called \_\_\_\_\_\_\_\_.

a. pop b. adjust c. select d. push

84. In a stack, the operation of deletion is called \_\_\_\_\_\_\_\_.

a. pop b. adjust c. select d. push

85. The \_\_\_\_\_\_ points at the address of the next instruction in the program.

a. stack pointer b. program counter c. pointer register d. instruction register

86. Reverse Polish notation is also referred to as \_\_\_\_\_\_\_\_ notation.

a. infix b. prefix c. postfix d. Polish

87. The expression A \* B + C \* D is written in reverse Polish notation as \_\_\_\_\_\_\_\_.

a. ABCD\*\*+ b. AB\*CD\*+ c. AB\*\*+CD d. \*AB\*+CD

88. The \_\_\_\_\_\_ field of an instruction specifies the way the operand of the effective address is determined.

a. operation code b. address c. mode d. data

89. RISC stands for \_\_\_\_\_\_\_\_\_\_\_\_\_.

a. Relevant Instruction Set Computer b. Reduced Instruction Set Converter

c. Register Instruction Set Computer d. Reduced Instruction Set Computer

90. In the \_\_\_\_\_\_ mode the operands are specified implicitly in the definition of the instruction.

a. implied b. indirect c. immediate d. relative

91. In the \_\_\_\_\_\_ mode the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

a. implied b. indirect address c. immediate d. relative address

92. The \_\_\_\_\_\_ instruction designates a transfer from a processor register into memory.

a. load b. store c. push d. pop

93. The \_\_\_\_\_\_ instruction swaps information between two registers.

a. push b. store c. exchange d. move

94. Which one of the following is an example of indexed addressing?

a. LD ADR(X) b. LD ADR c. LD @ADR d. LD $ADR

95. Which one of the following is an arithmetic instruction?

a. ST b. POP c. NEG d. BR

96. The \_\_\_\_\_\_ instruction is used to clear a bit or a selected group of bits of an operand.

a. OR b. XOR c. COM d. AND

97. The \_\_\_\_\_\_ instruction is used to set a bit or a selected group of bits of an operand.

a. OR b. XOR c. COM d. AND

98. Which one of the following is not a program control instruction?

a. BR b. SKP c. ROR d. JMP

99. The test instruction performs the logical \_\_\_\_\_\_ of two operands and updates certain status bits without retaining the result or changing the operands.

a. OR b. XOR c. COM d. AND

100. Traps are also called \_\_\_\_\_\_\_\_\_\_.

a. external interrupts b. hardware interrupt c. software interrupts d. priority interrupts

**MCA – First Semester**

**Core III : COMPUTER ORGANISATION AND ARCHITECTURE**

**(17MCA1C3)**

**Answer with Expansion**

**UNIT-I**

1. c. 8

2. d. Hexadecimal

3. a. 2

4. b. 1111

5. d. 11

6. c. 8

7. a. 15

8. d. Hexadecimal

9. b. 1011

10. c. 1001

11. d. 0101

12. b. 11

13. a. 1111

14. c. 1001

15. b. ASCII

16. a. 8-bit

17. b. 10011000

18. a. 11110

19. b. 11001

20. c. parity

**UNIT-II**

21. c. inverter

22. a. AB

23. b. AND, NOT

24. d. NAND

25. a. NOT

26. a. all the inputs are 1s

#### 27. d. 8

28. c. 2

29. c. X

30. a. 1

31. b. A+B

32. c. AB+AC

33. b. A’.B’.C’

34. d. AND-OR

35. a. OR-AND

36. c. 8

37. b. pair

38. c. octet

39. d. 16

40. b. redundant

**UNIT-III**

41. c. data selector

42. b. 2

43. a. 1 line

44. b. Demultiplexer

45. b. 3

46. c. many lines

47. a. 8

48. d. 3

49. c. decoder

50. d. encoder

51. b. 2

52. a. half adder

53. b. half subtractor

54. c. carry

55. d. 3

56. d. full adder

57. a. parallel adder

58. d. 01110

59. c. XOR

60. b. BCD

**UNIT-IV**

61. a. flipflops

62. b. sequential circuit

63. c. register

64. a. flipflop

65.b. complement of the other

66. b. D flipflop

67. d. Set

68. a. one inverter

69. b. D flipflop

70. d. reset

71. c. no change

72. c. no change

73. d. toggle

74. a. Toggle

75. b. previous

76. a. shift register

77. b. ripple counter

78. d. 3

79. a. synchronous

80. b. asynchronous

**UNIT-V**

81. b. LIFO

82. a. stack pointer

83. d. push

84. a. pop

85. b. program counter

86. c. postfix

87. b. AB\*CD\*+

88. c. mode

89. d. Reduced Instruction Set Computer

90. a. implied

91. d. relative address

92. b. store

93. c. exchang

94. a. LD ADR(X)

95. c. NEG

96. d. AND

97. a. OR

98. c. ROR

99. d. AND

100. b. hardware interrupt

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