Course Title	**:**	Digital Logic Design
Course Code	**:**	CSE345
Section	**:**	(03)
Semester	**:**	Summer 2021

Project Report

Project Name: 4-bit Binary to Even Parity Code Converter.

Submitted To

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1. Problem Statement

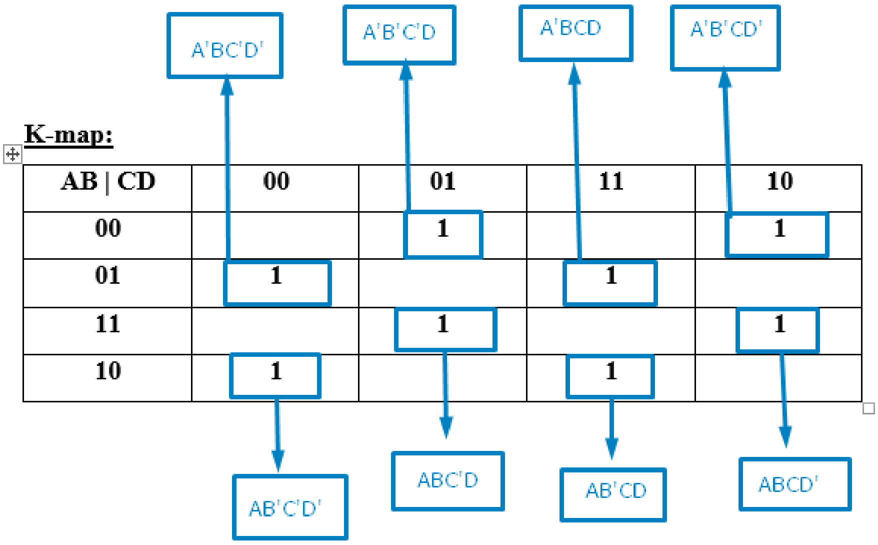
A 4-bit code converter for even parity converts the 4-bit input to 5-bit output so that even parity is ensured.

2. Design Details

Truth Table:

ABCD	F
0000	0
0001	1
0010	1
0011	0
0100	1
0101	0
0110	0
0111	1
1000	1
1001	0
1010	0
1011	1
1100	0
1101	1
1110	1
1111	0

K-map:



AB | CD	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

So,

F = A'B'C'D + A'B'CD' + A'BC'D' + A'BCD + ABC'D + ABCD' + AB'C'D' + AB'CD

= A'B' (C'D + CD') + A'B (C'D' + CD) + AB (C'D + CD') + AB' (C'D' + CD)

= A'B' (C XOR D) + A'B (C XNOR D) + AB (C XOR D) + AB' (C XNOR D)

= (C XOR D) (A'B' + AB) + (C XNOR D) (A'B + AB')

= (C XOR D) (A XNOR B) + (C XNOR D) (A XOR B)

= (A XNOR B) (C XOR D) + (A XOR B) (C XNOR D)

= (A XOR B)' (C XOR D) + (A XOR B) (C XOR D)'

Assuming,

x = (A XOR B),

y = (C XOR D)

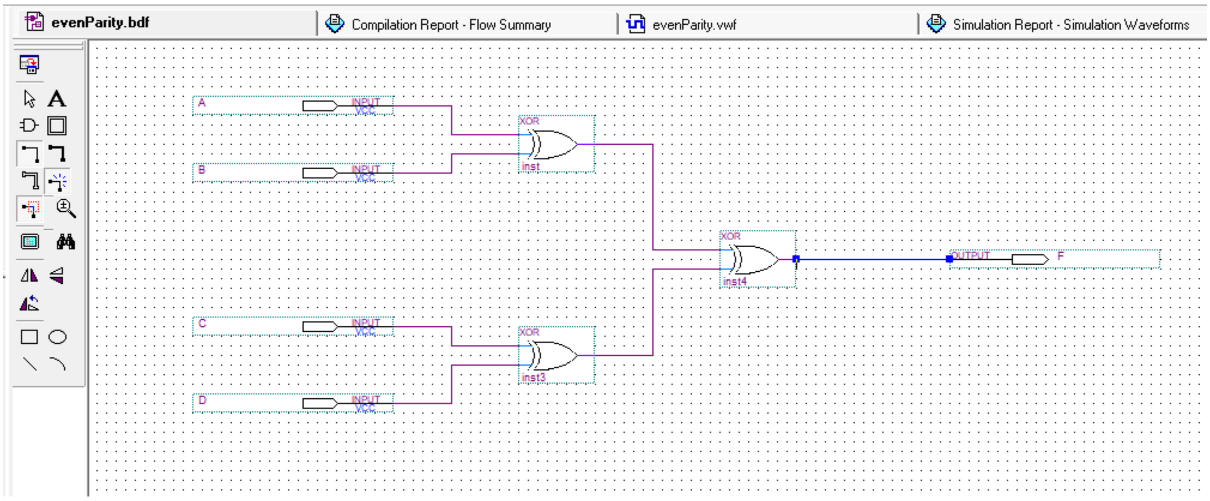
So,

F = x'y + xy'

= x XOR y

= (A XOR B) XOR (C XOR D)

3. Circuit Diagram:

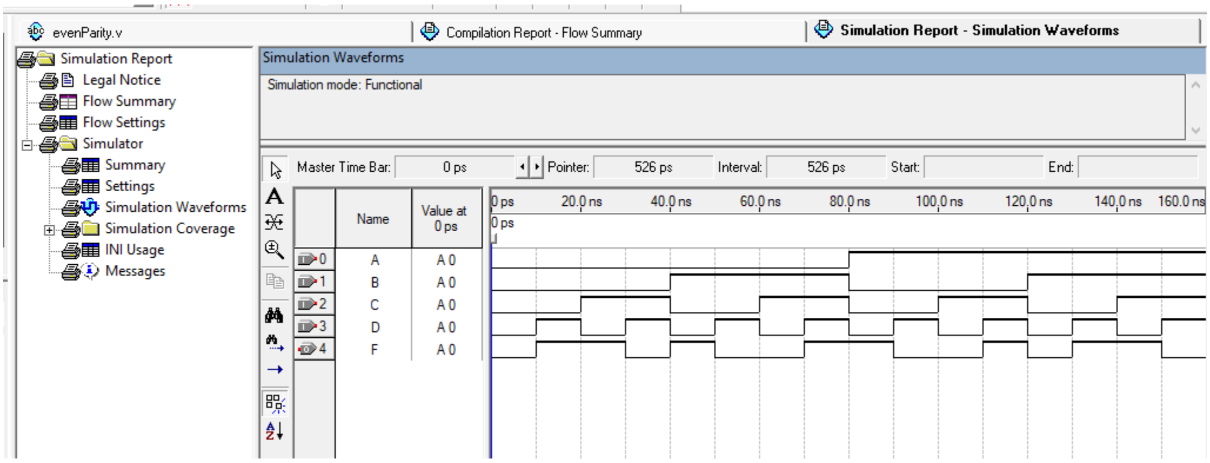


4. Structural and Behavioral Verilog Code and Simulation Results:

Structural Verilog Code:

```
module evenParity(input A,B,C,D, output F);
wire w1,w2;
xor g1(w1,A,B),
   g2(w2,C,D);
xor g3(F,w1,w2);
endmodule
```

Simulation Result:



Simulation mode: Functional

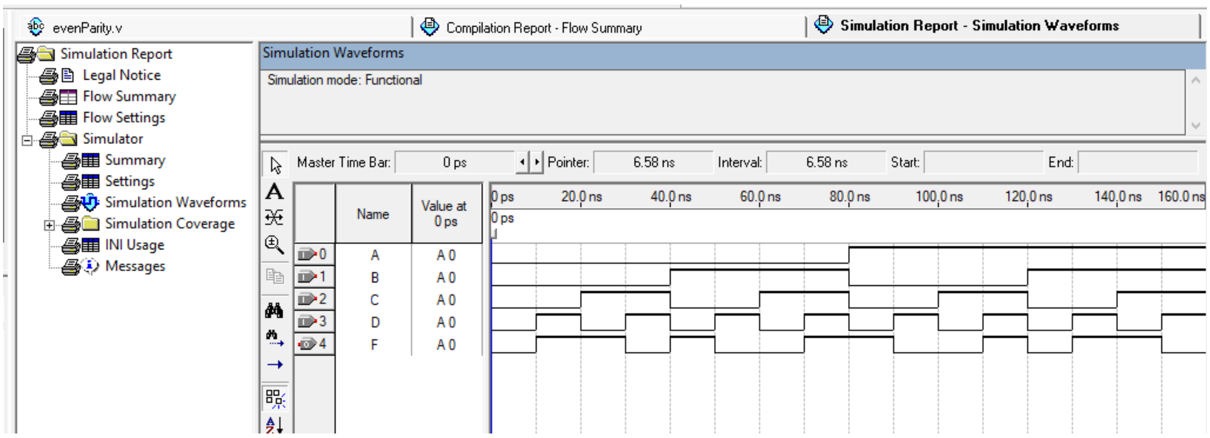
Master Time Bar: 0 ps Pointer: 526 ps Interval: 526 ps Start: End:

	Name	Value at 0 ps
0	A	A 0
1	B	A 0
2	C	A 0
3	D	A 0
4	F	A 0

Procedural Model:

```
module evenParity(input A, B, C, D, output reg F);
always @(A, B, C, D)begin
F=0;
if(~A&~B&~C&D) F=1;
if(~A&~B&C&~D) F=1;
if(~A&B&~C&~D) F=1;
if(~A&B&C&D) F=1;
if(A&B&~C&D) F=1;
if(A&B&C&~D) F=1;
if(A&~B&~C&~D) F=1;
if(A&~B&C&D) F=1;
end
endmodule
```

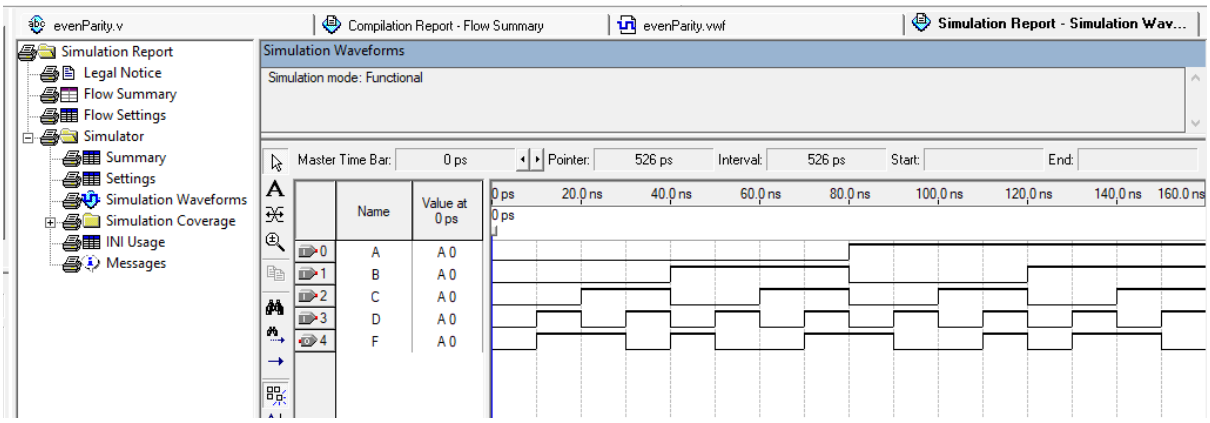
Simulation Result:



Continuous Assign Statement:

```
module evenParity(input A,B,C,D, output F);
assign
F=(~A&~B&~C&D) | (~A&~B&C&~D) | (~A&B&~C&~D) | (~A&
B&C&D) | (A&B&~C&D) | (A&B&C&~D) | (A&~B&~C
&~D) | (A&~B&C&D);
endmodule
```

Simulation Result:


evenParity.v
Compilation Report - Flow Summary
evenParity.vwf
Simulation Report - Simulation Wav...
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 0 ps
Pointer: 526 ps
Interval: 526 ps
Start:
End:
Name
Value at 0 ps
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
160.0 ns
0 ps
0 A A 0
1 B A 0
2 C A 0
3 D A 0
4 F A 0