PE Project Status (10/21/2015 - 12:58:05)			
Project File:	PriorityEncoder.xise	**Parser Errors:**	No Errors
Module Name:	PE	**Implementation State:**	Programming File Generated
Target Device:	xc3s250e-5cp132	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:		• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	5	4,896	1%	
Number of occupied Slices	3	2,448	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Total Number of 4 input LUTs	5	4,896	1%	
Number of bonded IOBs	13	92	14%	
IOB Flip Flops	4			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	1.46			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report

Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed 21. Oct 11:34:24 2015	0	0	0
Translation Report	Current	Wed 21. Oct 12:25:42 2015	0	0	0
Map Report	Current	Wed 21. Oct 12:49:27 2015	0	0	2 Infos (0 new)
Place and Route Report	Current	Wed 21. Oct 12:49:49 2015	0	0	1 Info (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed 21. Oct 12:49:58 2015	0	0	6 Infos (0 new)
Bitgen Report	Current	Wed 21. Oct 12:57:47 2015	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
ISIM Simulator Log	Current	Wed 21. Oct 13:38:33 2015
WebTalk Report	Current	Wed 21. Oct 12:57:49 2015
WebTalk Log File	Current	Wed 21. Oct 12:58:03 2015

Date Generated: 10/21/2015 - 13:48:16