Lecture#13:

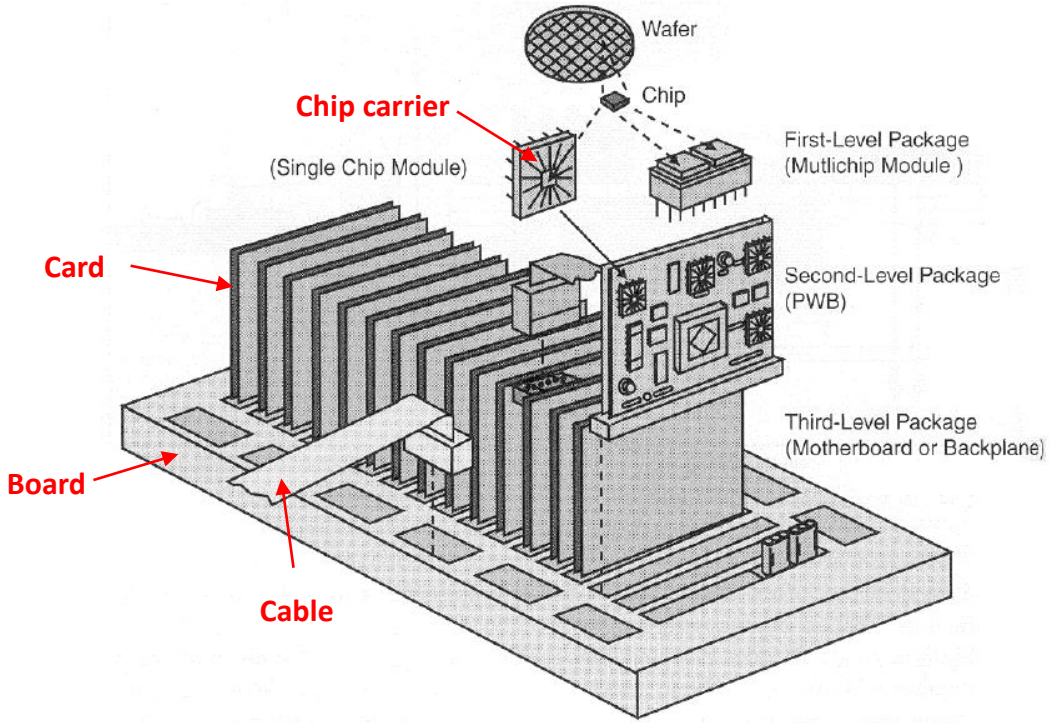
Process Integration (2)

Process Integration (2)

- **IC packaging**
  - The final series of operations to transform the wafer into individual chips, ready to connect to external circuits and prepared to withstand the harsh environment of the world outside the clean room.
  - Electrical connections to external circuits
  - Materials to encase chip and protect it from the environment (humidity, corrosion, temperature,
  - vibration, mechanical shock)
  - Heat dissipation

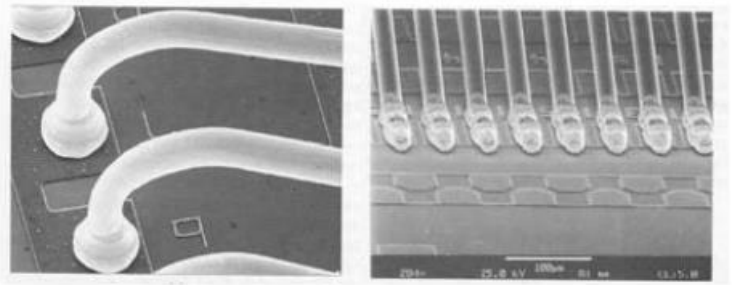
<Levels of package>

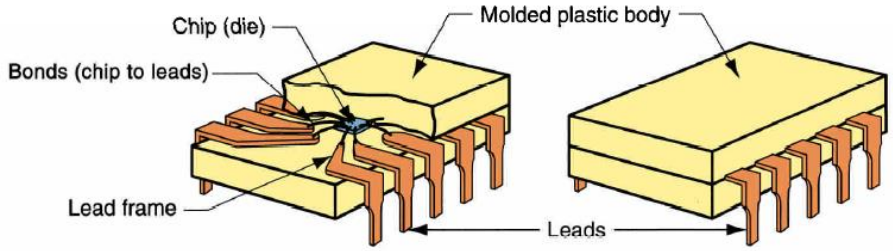
LV.0: Features on chip
LV.1: Chip
LV.2: Chip carrier
LV.3: Card
LV.4: Board
LV.5: Cables



Wire bonding (leadframe type)

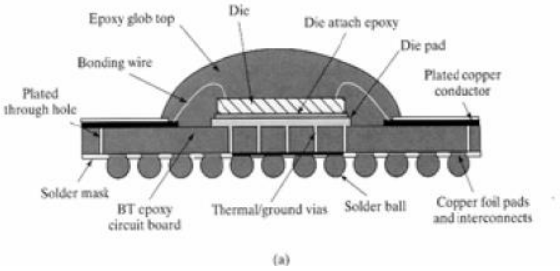
- Thermocompression bonding was originally used with gold wire, and ultrasonic bonding is used with aluminum wire.
- A combination of the two is called thermosonic bonding.
- The bonding can achieve a 50 ~ 70 μm pitch

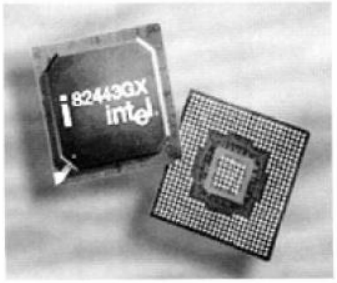


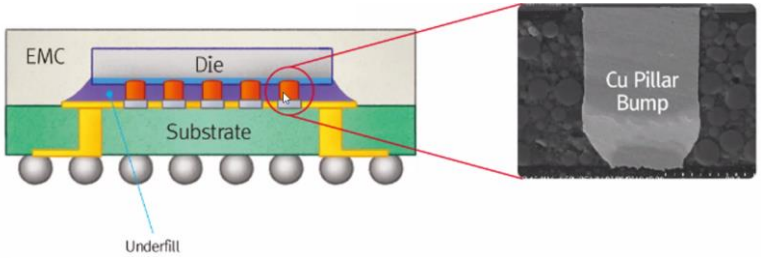


Flip chip bonding (substrate type)

- Fine-pitch ball-grid arrays (FBGA, or μBGA) are projected to decrease a pitch



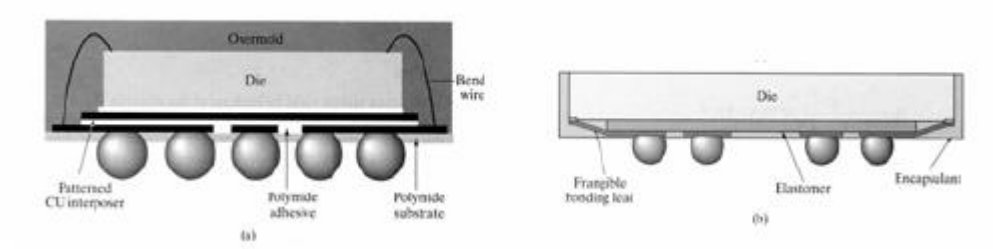




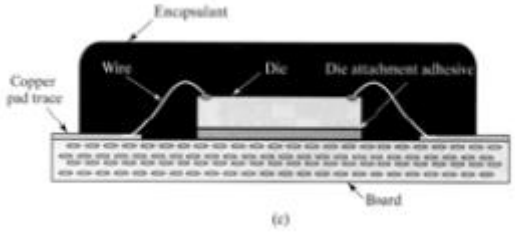
Type of Packaging (2)

Process Integration (2)

- **Chip scale package (CSP)**
  - In Chip Scale Package (CSP), the package area is no longer than the die itself.

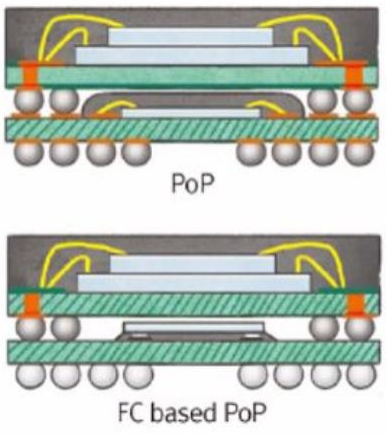


- **Chip on board (COB)**
  - To eliminate the package altogether by mounting the bare die directly on the PCB or flexible substrate.
  - The final structure is encapsulated with an epoxy coating.

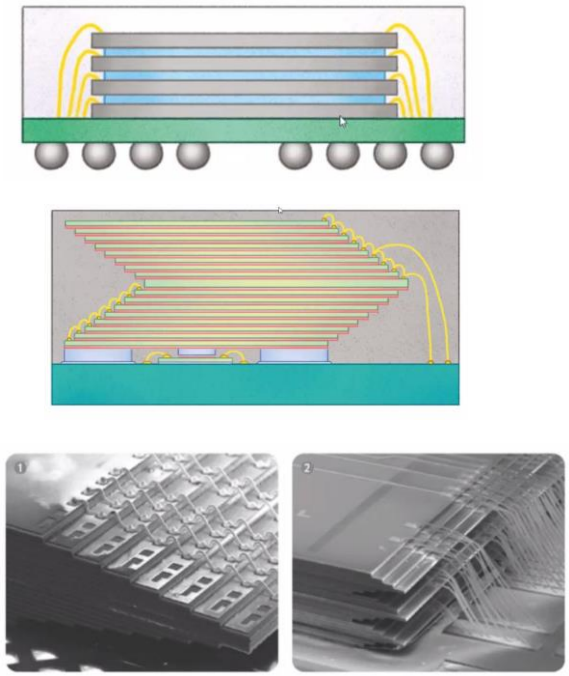


- **Stack package**

(Package on Package)

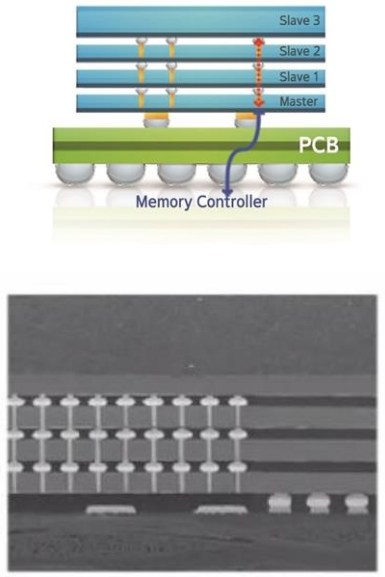


(Chip level 3D stack package)



Source: SK hynix

(Through Silicon Via, TSV)



Source: SK hynix

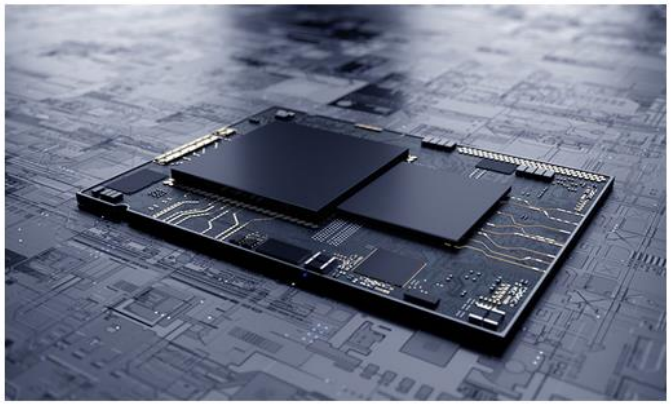
Integration Technology (2)

Process Integration (2)

세계일보

삼성전자, EUV 시스템 반도체에 3차원 패키징 기술 'X-Cube' 적용

입력 2020-08-13 15:05:27, 수정 2020-08-13 20:42:25



삼성전자가 7나노 EUV 시스템반도체에 3차원 적층 패키지 기술인 'X-Cube(eXtended-Cube)'를 적용한 테스트칩 생산에 성공했다고 13일 밝혔다. 삼성전자 제공

삼성전자가 업계 최초로 EUV(극자외선) 7나노 공정의 시스템 반도체에 3차원 패키징 기술인 'X-Cube'(eXtended-Cube)를 적용했다.

13일 삼성전자에 따르면 최근 X-Cube를 적용한 테스트칩 생산에 성공했다. X-Cube는 여러 개의 칩을 얇게 쌓아서 하나의 반도체를 만드는 기술로, EUV 7나노 공정에서는 삼성전자가 업계 최초로 구현했다.

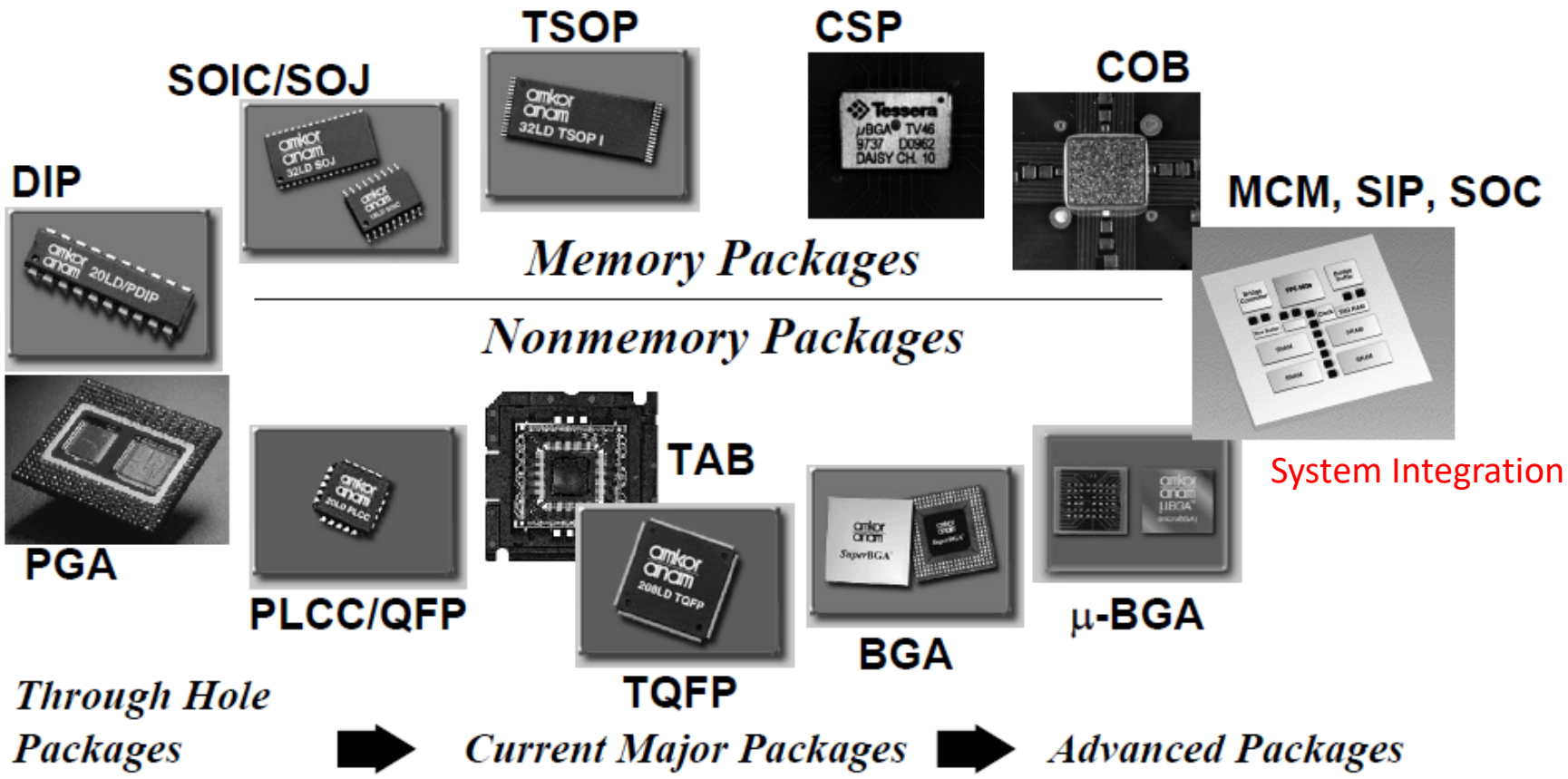
통상 시스템 반도체에는 두뇌 역할의 로직과 저장 공간인 에스램(SRAM)이 병렬로 배치되는데, X-Cube 구현으로 로직과 에스램을 쌓아올릴 수 있게 됐다. 반도체는 크기가 작을수록 공간 활용도가 높아지고 수율이 개선되는데, X-Cube로 이 같은 효율성을 극대화할 것으로 보인다.

https://www.segye.com/newsView/20200813520910?OutUrl=naver

Integration Technology (3)

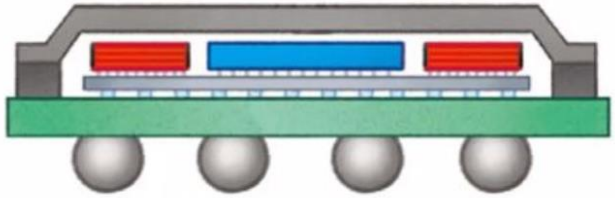
Process Integration (2)

- Trend in packaging technology

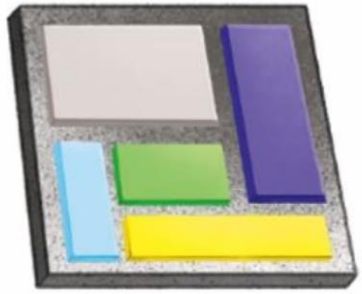


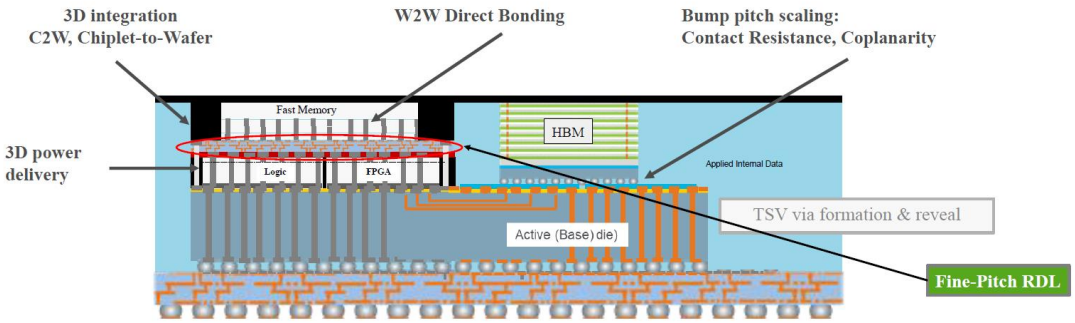
- SiP vs SoC

SiP : System in Package



SoC : System on Chip





- SiP is suitable for products of small volume and various kinds
- It is advantageous for products that require rapid market entry
- SoC is advantageous for large quantity and long-term products

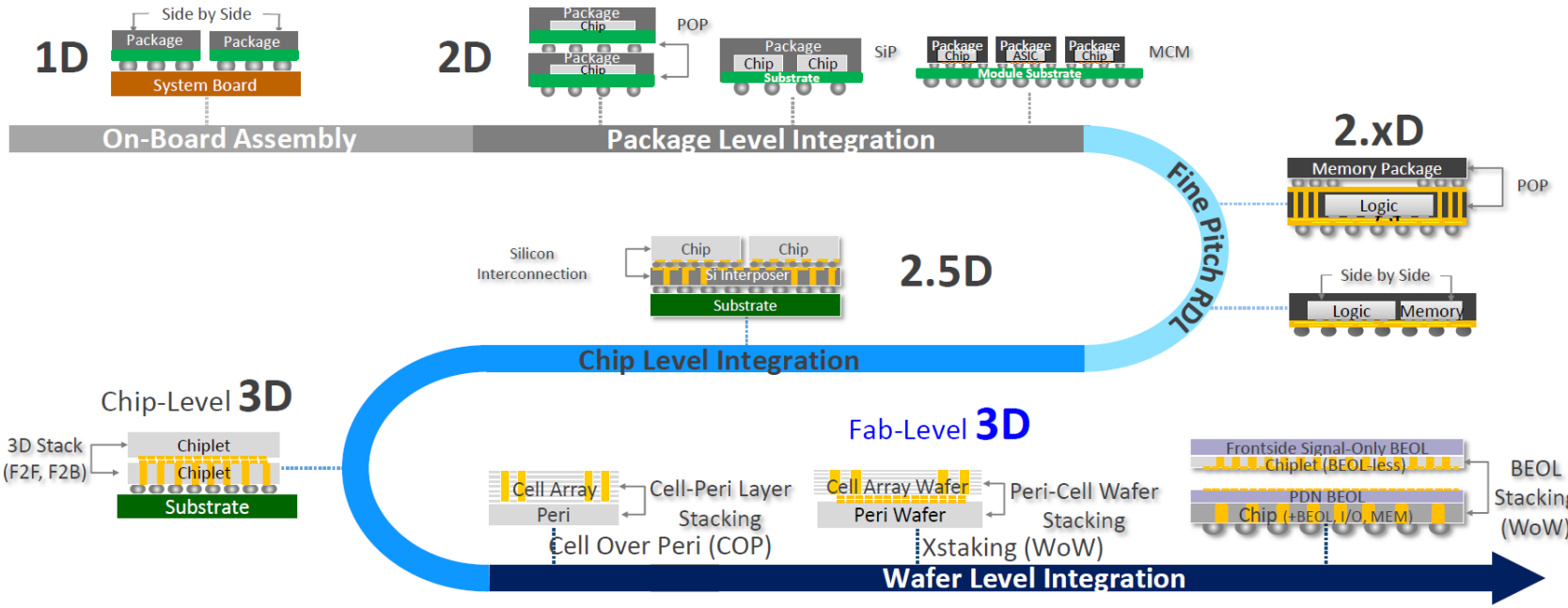
System Integration Technology (2)

Process Integration (2)

- **Chiplet technology shifts to 3D from 2.5D**

(Conventional packaging)

(Wafer level packaging)



Fusion of Fab & Package

System Integration Technology (3)

Process Integration (2)

- **3D system integration technology**