Lecture#12:

Process Integration (1)

Overview

Process Integration (1)

Trends of a electrical devices

- As devices (cell phones, TVs, etc.) get smaller and more complex, the chips needed are smaller and more complex.

1983

10 inches
28 oz

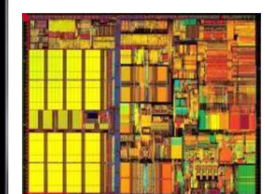
Calls only,
60 minutes of calls,
then 10 hours to recharge

30 years

2013

Example: Apple iPhone 5s

<5 inches
<4 oz



Calls, digital camera, video camera, email, calendar, address book, music, movies, internet, clock, maps & GPS, calculator, etc.

Source: Wikipedia, Apple

Integrated Circuit

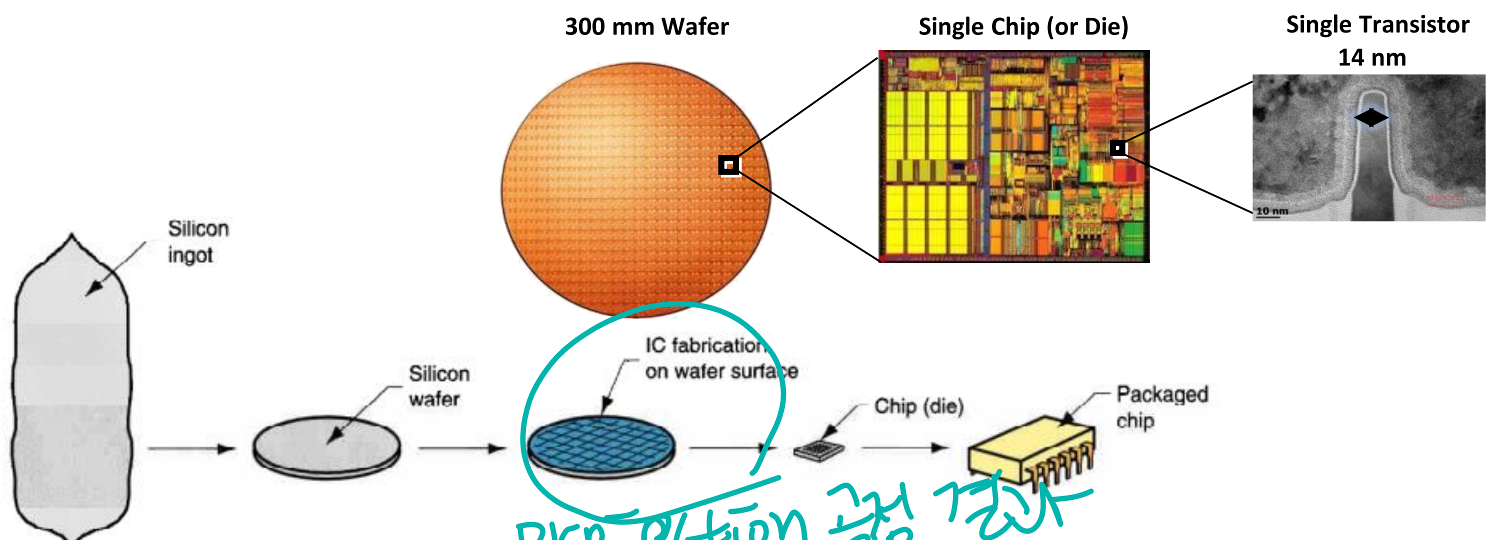
Process Integration (1)

Integrated Circuit (IC)

- An ensemble of both active (transistor, etc.) and passive (resistor, capacitor, and inductor) devices formed on and within a single crystal substrate.

- Fabrication of active and passive components in ICs using micro fabrication process

- An integrated circuit consists of hundreds, thousands, or millions of microscopic electronic devices that have been fabricated and electrically interconnected on the surface of a silicon chip.



projection 공정 결과

<Sequence of processing steps in the production of integrated circuits>

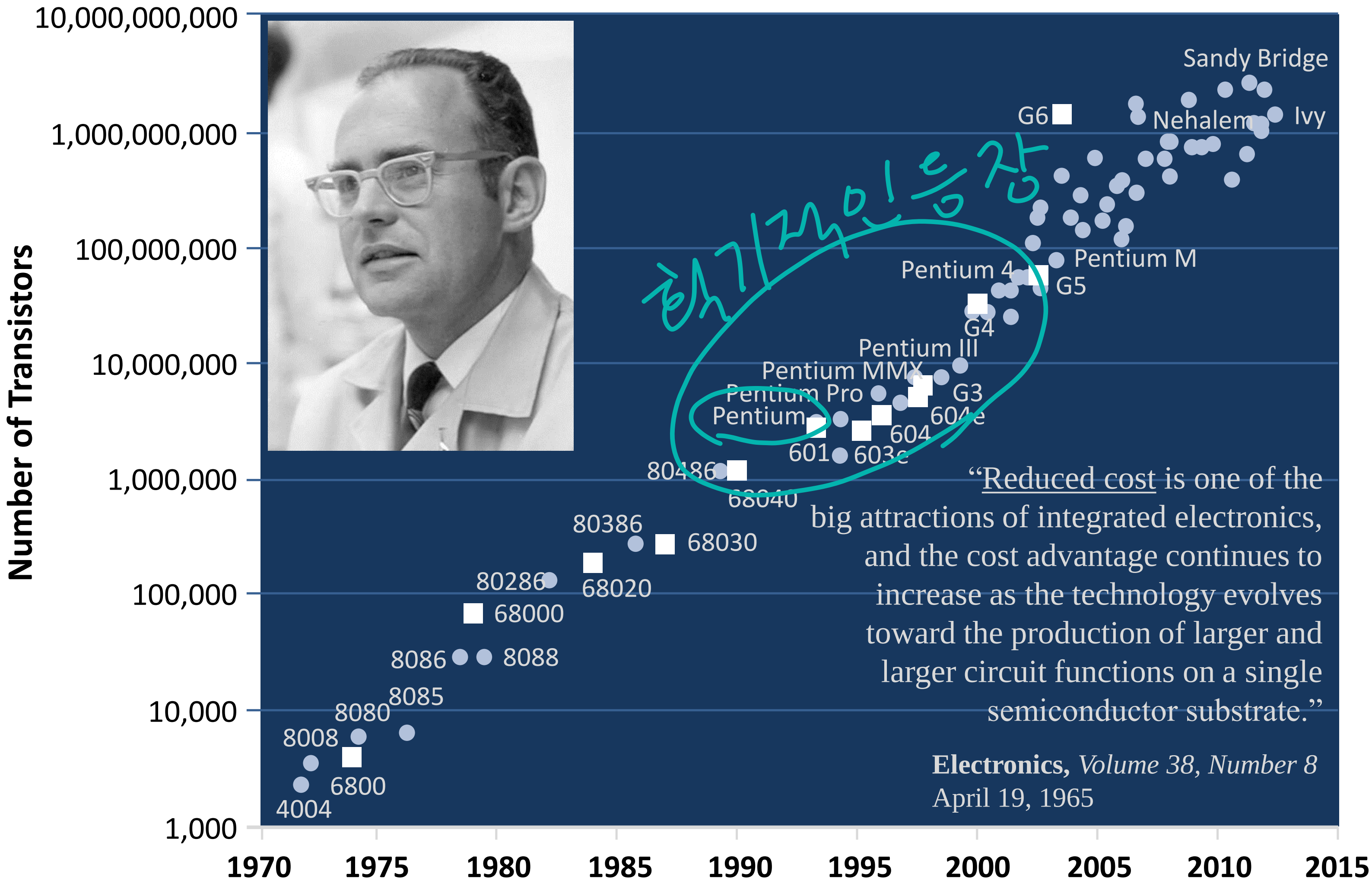
Level of Integration in Microelectronics

Process Integration (1)

Integration level	Number of devices	Approx. year
Small scale integration (SSI)	10-50	1959
Medium scale integration (MSI)	50 - 10^3	1960s
Large scale integration (LSI)	10^3 - 10^4	1970s
Very large scale integration (VLSI)	10^4 - 10^6	1980s
Ultra large scale integration (ULSI)	10^6 - 10^8	1990s
Giga scale integration	10^8 - 10^{10}	2000s

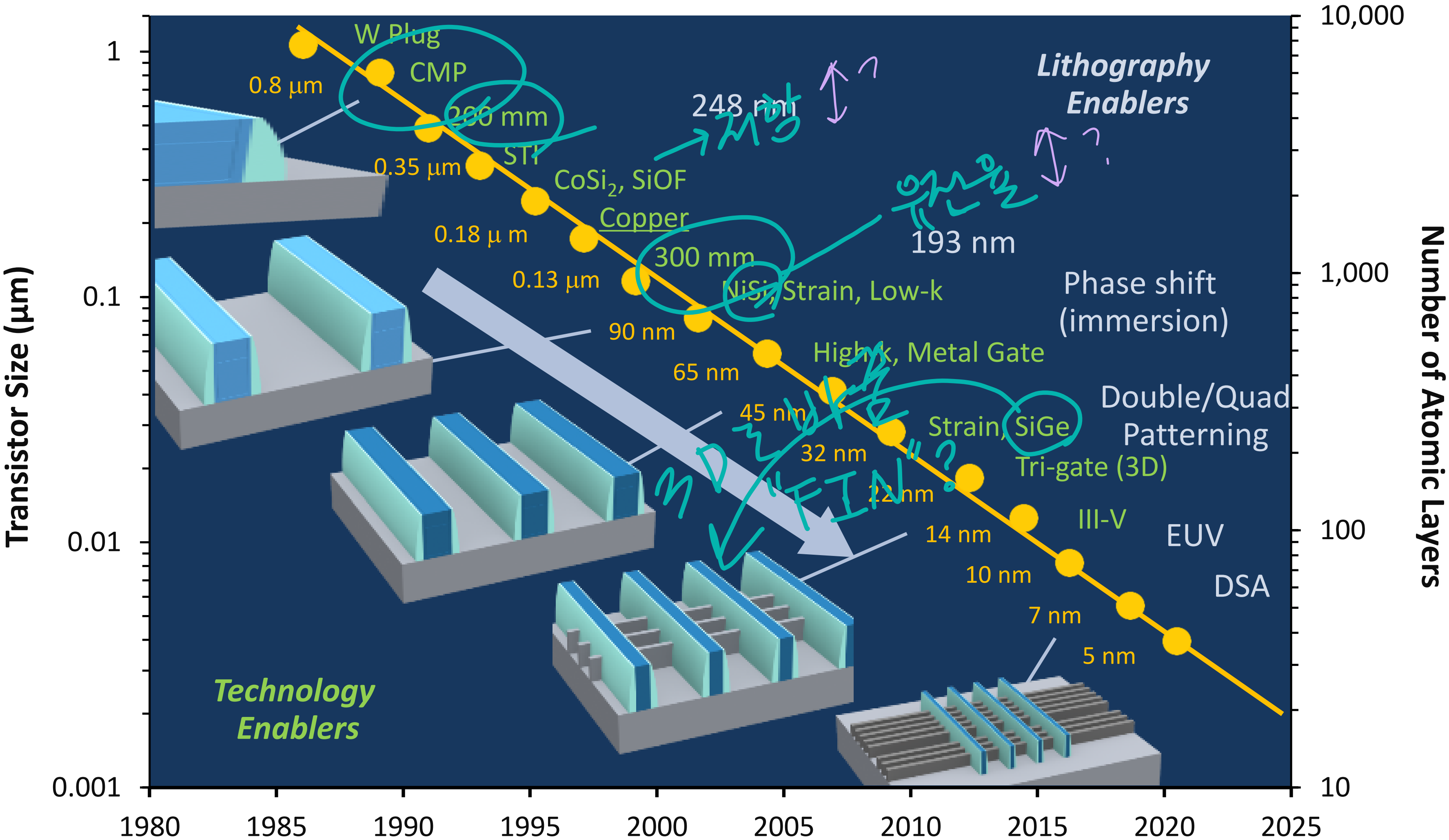
Classic View of Moore's Law

Process Integration (1)



Continuous Innovation Enables Continuation of Moore's Law

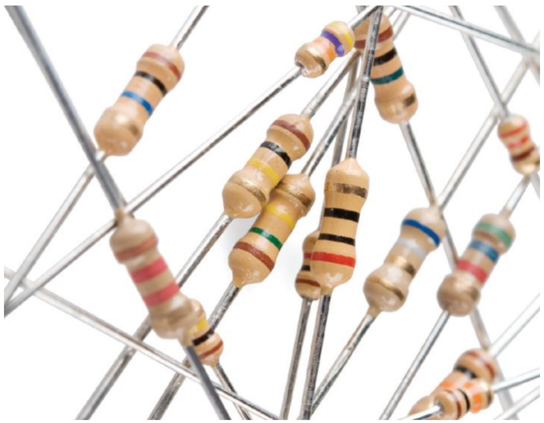
Process Integration (1)



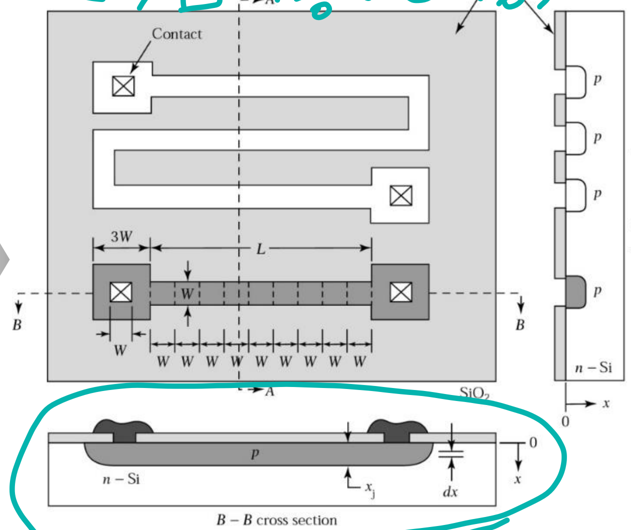
Passive Components (1)

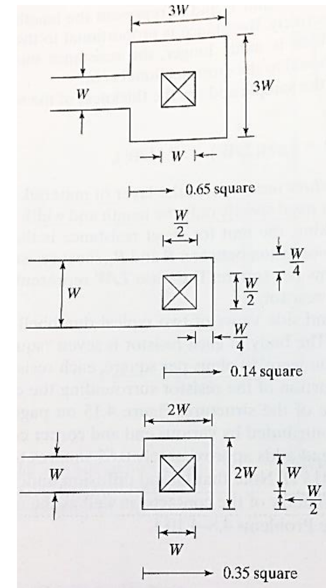
Process Integration (1)

- **Resistor** Ω

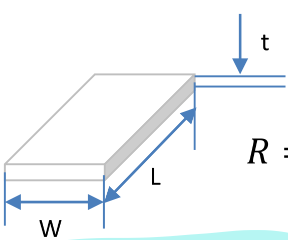


Ω/□ 사용 (면저항)





Deposit oxide layer → Pattern by Photolithography and etching → Formation of junction (n or p) by diffusion or implantation



$$R = \rho L/wt = (\rho/t)(L/w)$$

→ Sheet resistance : R_s

Unit - R:Ω Rs :Ω/□
(□ , there is no meaning – to avoid confusion)

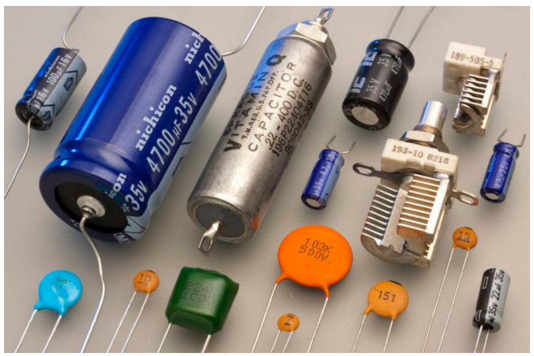
- The portion of the resistor surrounding the contacts also contributes to the total resistance of the structure.
- Many resistors in an IC are fabricated simultaneously by defining different geometric patterns in the mask.

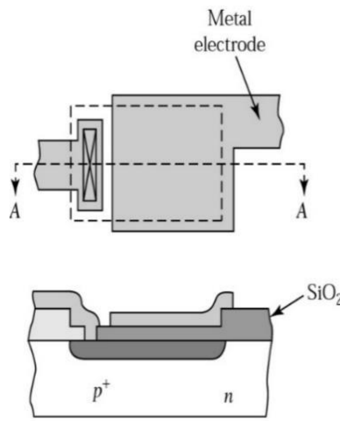
Passive Components (2)

Process Integration (1)

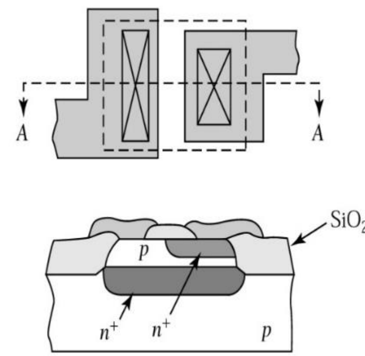
Capacitor

- Two types of capacitors are used in ICs: Metal-Oxide-Semiconductor (MOS) capacitors and p-n junctions.
- MOS capacitor: fabricated by using a heavily doped region, the top metal electrode, and oxide layer.





Metal-Oxide-Semiconductor (MOS) capacitor



p-n junction capacitor

(MOS capacitor)

Formation of highly doped junction (n+, or p+) ➡ SiO_2 formation and pattern ➡ Metal deposition and pattern

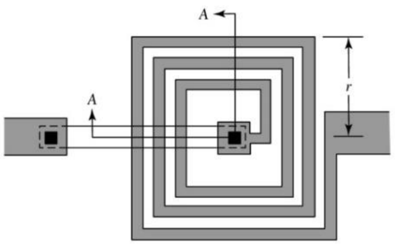
$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

ε_0 : Permittivity in vacuum = 8.85 x 10^{-14} F/cm
ε_r : Dielectric constant (SiO_2 : ~4, Si_3N_4: ~7, Ti_2O_5:~25)
A : Area of capacitor
d : Thickness of insulator film (gap between electrodes)

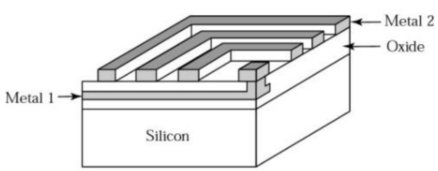
Process Integration (1)

Inductor

- An inductor (or reactor) can store energy in a magnetic field created by the electric current passing through it.
; Typically an inductor is a conducting wire shaped as a coil
; Inductance results from the magnetic field forming around a current-carrying conductor which tends to resist changes in the current.



(a)



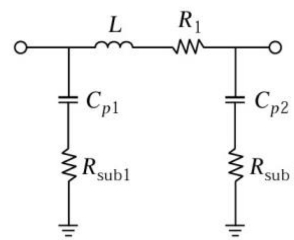
(b)

- **Quality factor**: High Q means the low loss from resistance and the better performance

$$Q = \frac{L\omega}{R}$$

L : inductance
ω : frequency
R : resistance

Formation of Oxide layer
⬇
Metal deposition and etching (Metal1)
⬇
Other oxide layer deposition
⬇
Via hole etching
⬇
Metal deposition and etching (Metal2)



$R1$: inherent resistivity of the metal

$Rsub$: resistances of the silicon substrate associated with the metal lines

Cp : coupling capacitance between the metal lines and the substrate

For High Q :
i) Reduce Cp - low dielectric material
ii) Reduce R1 - Thick film metal or low resistivity metal
iii) Reduce Rsub - Insulating substrate

$$L \approx \mu_0 n^2 r \approx 1.2 \times 10^{-6} n^2 r$$

μ_0 : the permeability of vacuum
n : the number of turns
r : radius

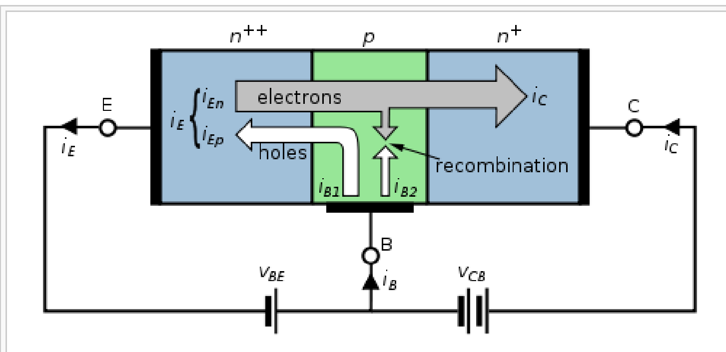
Active Components: BJT (1)

Process Integration (1)

Bipolar junction transistors (BJT)

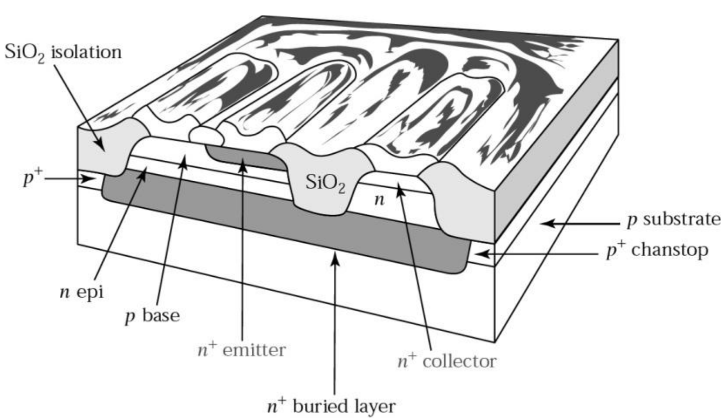
- Bipolar operation involves both electrons and holes.
- Diffusion mechanism
- Amplifying or switch application

c.f.) Transistor
- just electron or hole carrier (unipolar)
- Drift mechanism



NPN BJT with forward-biased E–B junction and reverse-biased B–C junction

- BJTs are manufactured in two types: n-p-n and p-n-p.
- The majority of BJTs are n-p-n type because the higher mobility of minority carriers (electrons) in the base region.

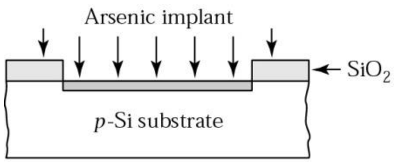


- Lateral isolation is provided by oxide walls
- Vertical isolation is provided by the n^+ - p junction

Active Components: BJT (2)

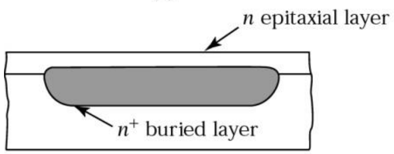
Process Integration (1)

Fabrication process: BJT



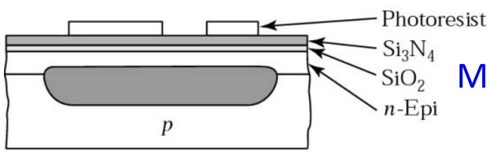
(a)

n-junction fabrication (As)



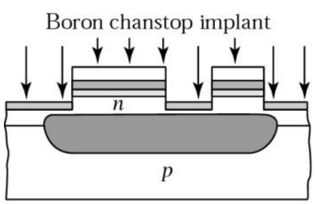
(b)

Annealing (drive-in) & Epitaxial growth (n-type layer)



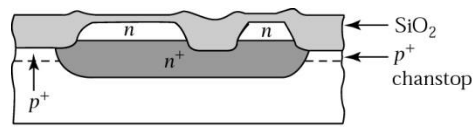
(c)

Masking and etching



(d)

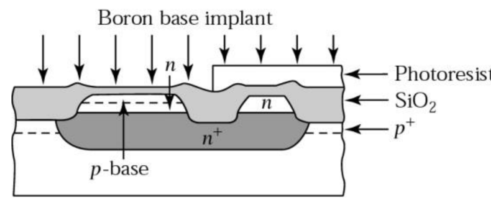
Implantation for p-junction (B)



(a)

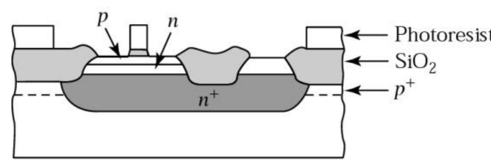
PR remove
Oxidation
Nitride etching

*local oxidation of silicon: LOCOS
p+ channel stop: chanstop



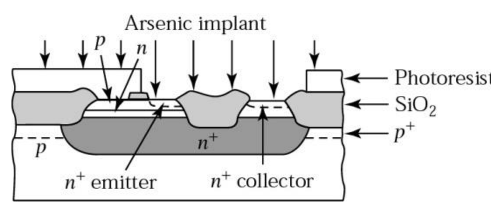
(b)

Masking
p-Implantation (B)



(c)

Open E,B,C contact area



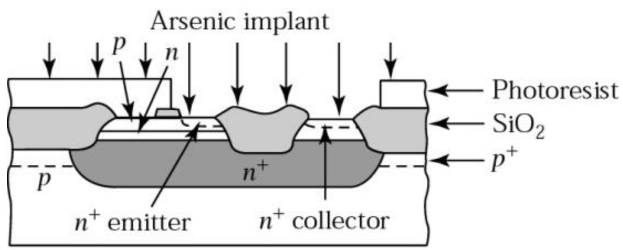
(d)

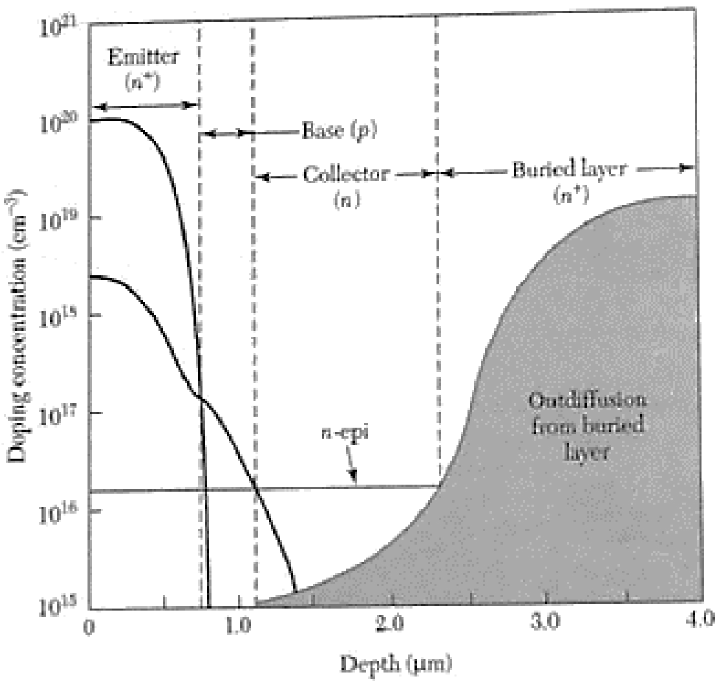
E,C area highly doped implantation (As)
& Metal contact formation

**six film formation process + six lithographic process + four ion implantation*

Process Integration (1)

Doping profile



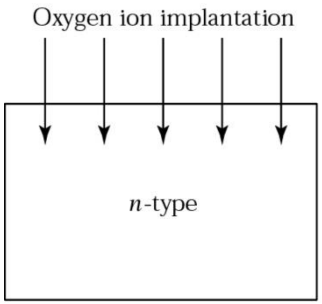


- **Emitter profile** is abrupt because of the concentration-dependent diffusivity of arsenic.
- **Base profile** beneath the emitter can be approximated by a Gaussian distribution for limited source diffusion.
- **Collector doping** is given by the epitaxial doping level

Process Integration (1)

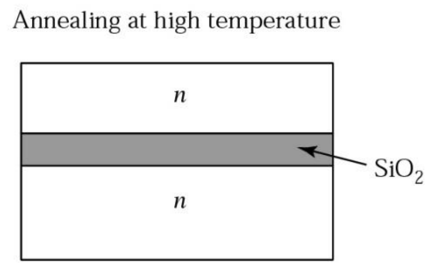
Dielectric isolation

- General isolation : n^+ p^+ junction
- High voltage application : **dielectric isolation** (forming insulating tubs to isolate a number of pockets of single crystal semiconductors)



(a)

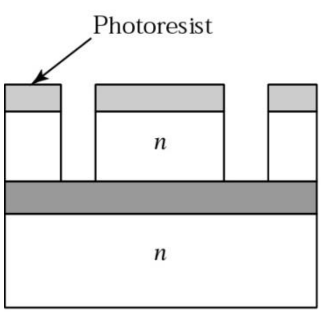
Implantation



(b)

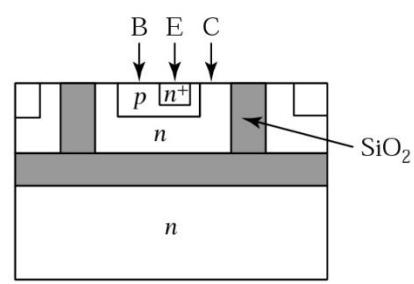
Thermal annealing to make SiO2 : Silicon on insulator (SOI)

**separation by implanted oxygen: SIMOX*



(c)

Masking & Etching



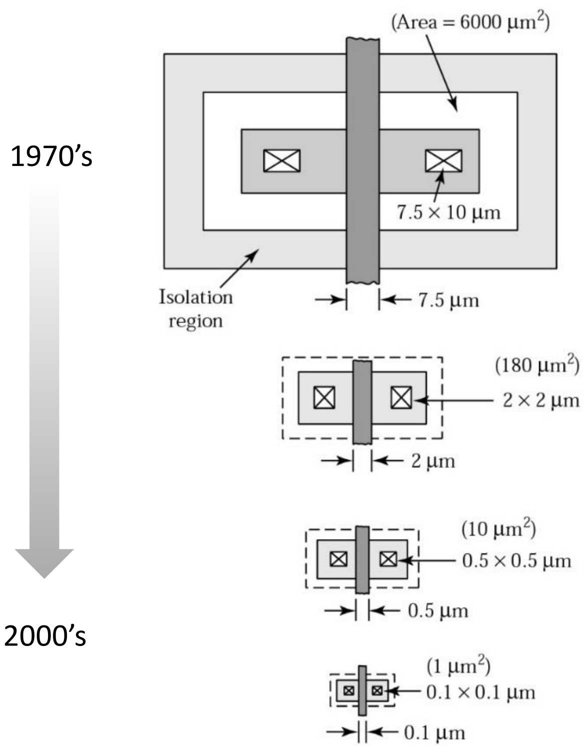
(d)

Ion implantation for B,E,C

**LOCOS*

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

- MOSFET is a type of field-effect transistor.
- The dominant technology for MOSFET is CMOS (complementary MOSFET) technology, in which both n-channel and p-channel devices. (called NMOS and PMOS, respectively) are provided on the same chip.



Cell size shrinkage

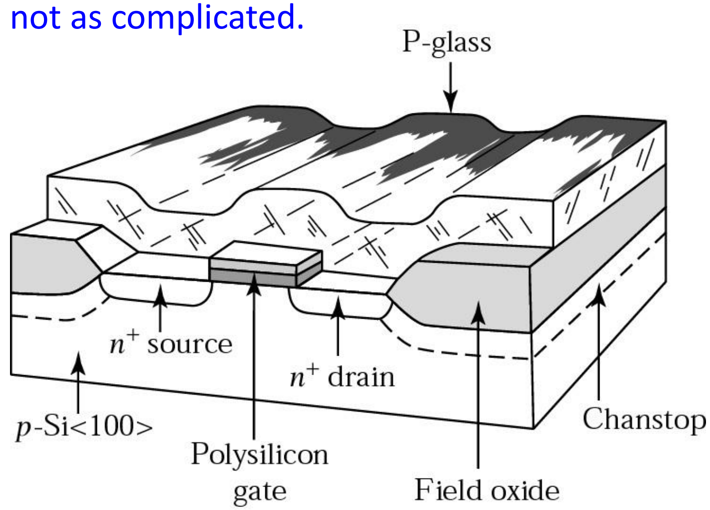
As the device is scaled down, there is a drastic reduction in the device area.

<n-channel MOSFET (NMOS)>

; MOSFET is considerably simpler in its basic structure, compared with BJTs.

; there is no need for vertical isolation

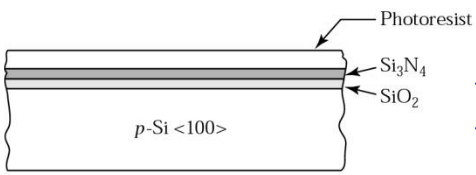
; doping profile is not as complicated.



Active Components: MOSFET (2)

Process Integration (1)

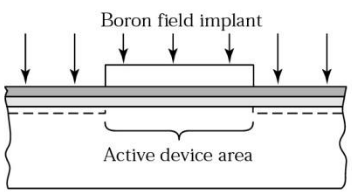
Fabrication process: NMOS



(a)

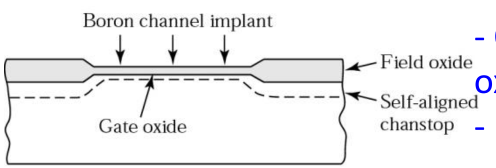
- Film depositions
- Photo lithography

*LOCOS



(b)

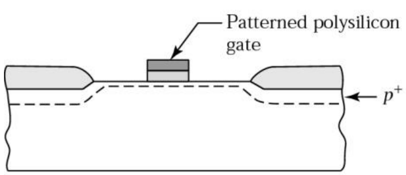
- Pattern for active area
- Ion implantation (B) for chanstop layer



(c)

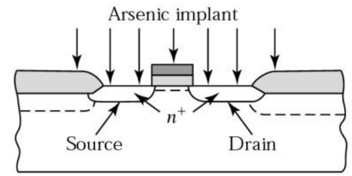
- Etching (SiN) & PR strip
- Oxide formation (field oxide)
- Implantation (B)

*For enhanced mode n-channel device c.f.) for depletion mode, As ions are implanted



(d)

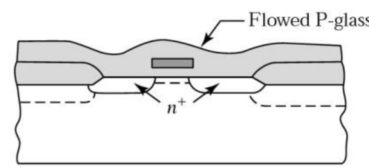
- Poly-Si (heavily doped by P) formation
- Pattern for poly-Si (gate)



(a)

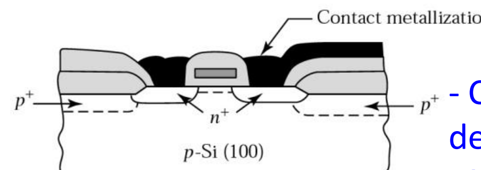
- Implantation (As) for source and drain

** Source and drain are self aligned.*
** Low temp processes are used to minimize lateral diffusion*



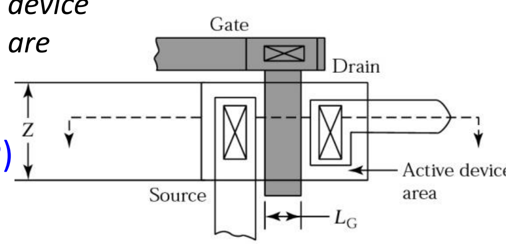
(b)

- Oxide deposition (phosphorus-doped oxide)



(c)

- Contact windows are defined.
- Metal contact formation



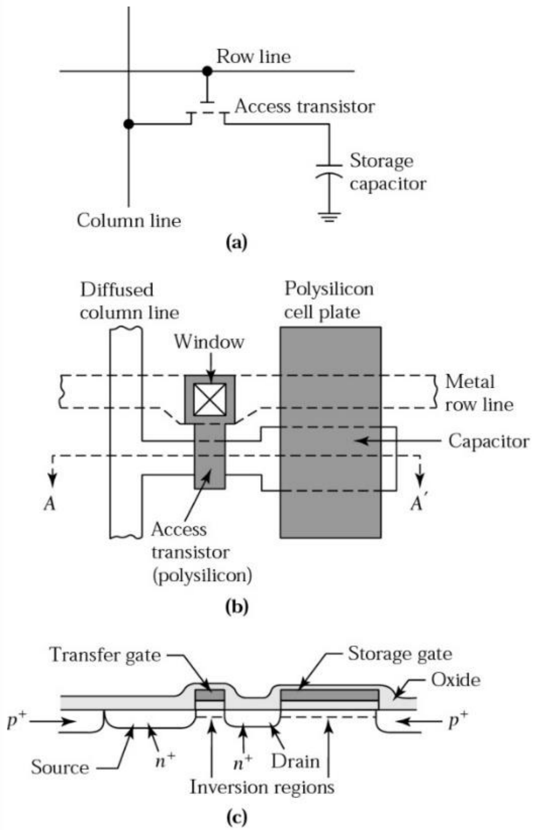
(d)

Active Components: Memory (1)

Process Integration (1)

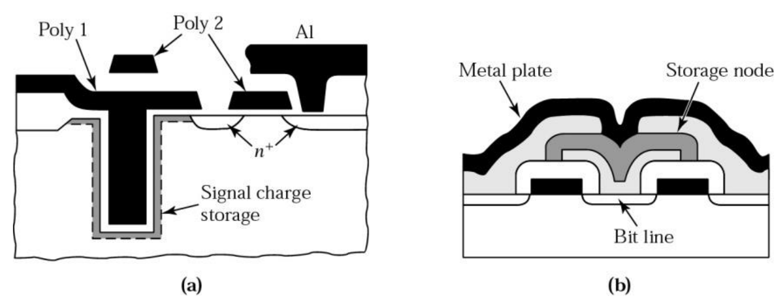
Memory devices

- Storage device of digital information in terms of bits.
- In a random access memory (RAM), memory cells are organized in a matrix structure.
- To reduce the cell area and power consumption, the dynamic random access memory (DRAM) has been developed.



<Single transistor DRAM cell with a storage capacitor>
; the voltage level on the capacitor determines the state of the cell
(e.g. +1.5 V -> logic 1, and 0 V -> logic 0)

* Trench and stack capacitor structure for high density DRAM

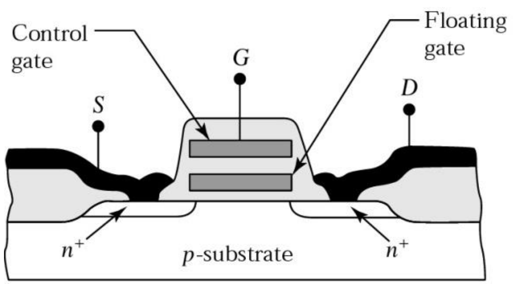


- The capacitance of the cell can be increased by increasing the depth of the trench.
- Difficulty: etching of the deep trench, growth of a uniform dielectric film

- The stacked cell process is easier than the trench-type process

Non volatile memory (Flash)

- Storage device of digital information in terms of bits.

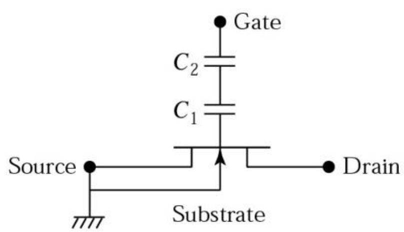


Floating gate nonvolatile memory

; The composite gate has a regular gate and a floating gate that is surrounded by insulators.

; When a large positive voltage is applied to the control gate, charge will be injected from the channel region through the gate oxide into the floating gate.

; When the applied voltage is removed, the injected charge can be stored in the floating gate for a long time.

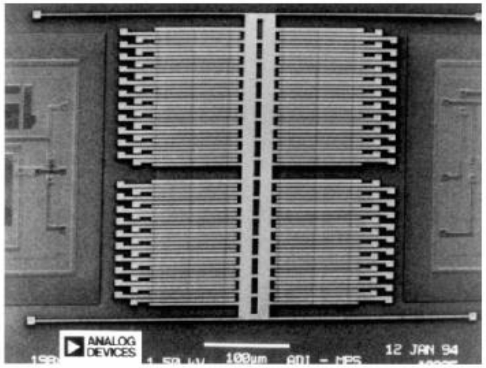


; The charge stored in the capacitor (C1) causes a shift in the threshold voltage, and the device remaining at the higher threshold voltage state (logic 1).

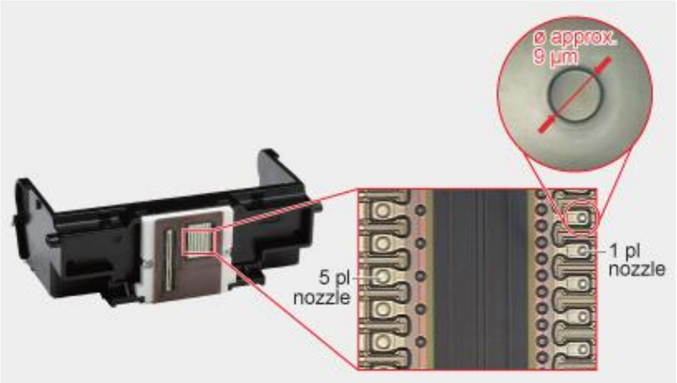
MEMS Technology

Process Integration (1)

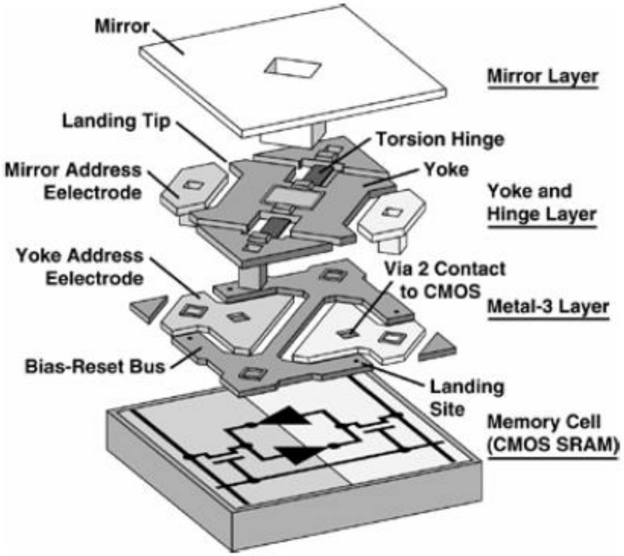
- **Micro electromechanical system (MEMS)**
  - The technology of microscopic devices, particularly those with moving parts.



Accelerometer for activation air-bag sensor



Ink-jet head



Texas Instrument's Digital Micro-mirror Device (DMD)