Design Requirements
- requirements for the design
- Lab document/client needs
- This is the preliminary input, and the output of this stage is the design specifications

Design Specifications
- Numerically specifying the requirements and the constraints for the design
- Requirements and the designer
- This takes requirements and outputs specifications

Design Entry
- Implementation of the design in VHDL/Verilog/Any other hardware description language
- VHDL/Verilog/etc.
- Design specifications are inputted and the output consists of a virtual implementation

Simulation
- Simulate the implemented design in code to verify that it meets the requirements
- ModelSim
- Provided implementation of design and the output is a message to the designer about whether or not the design meets the requirements

Logic Synthesis
- Converts the implemented design into gates and flip flops
- Vivado
- The input is the implemented design and the output is a hardware implementation of the code using gates and flip flops

Post Synthesis Simulation
- Checks if design meets timing requirements
- Vivado
- The input is the synthesized design and the output is the timing summary report

Mapping, Placing, Routing
- Builds the design in the FPGA
- Basys-3 Board
- The input is the RTL and the output is the bitstream

ASIC Masks
- When you request a provider to built a specific circuit that meets your needs
- At some company, this did not happen in the lab
- The input is the RTL design and the output is the chip

FPGA Programming Unit
- The board containing the FPGA that can be programmed
- On the board
- The input is the bitstream and the output is the configured FPGA

Configured FPGAs
- Loaded FPGAs that have been programmed appropriately
- On the FPGA board
- The input is the configured FPGA, and the output is something to field test with