

| Tool Version : Vivado v.2016.2 (win64) Build 1577090 Thu Jun 2 16:32:40 MDT 2016
| Date   : Thu Feb 16 20:35:59 2017
| Host   : DESKTOP-JK482SK running 64-bit major release (build 9200)
| Command   : report_timing_summary -warn_on_violation -max_paths 10 -file lab3top_timing_summary_routed.rpt -rpx lab3top_timing_summary_routed.rpx
| Design   : lab3top
| Device   : 7a35t-cpg236
| Speed File   : -1 PRODUCTION 1.14 2014-09-11

Timing Summary Report

| Timer Settings
| --------------

  Enable Multi Corner Analysis   : Yes
  Enable Pessimism Removal   : Yes
  Pessimism Removal Resolution   : Nearest Common Node
  Enable Input Delay Default Clock   : No
  Enable Preset / Clear Arcs   : No
  Disable Flight Delays   : No
  Ignore I/O Paths   : No
  Timing Early Launch at Borrowing Latches   : false

  Corner Analyze   Analyze
  Name   Max Paths Min Paths
  ------ --------- ---------
  Slow   Yes   Yes
  Fast   Yes   Yes

check_timing report

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----

2. checking constant_clock
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7. checking multiple_clock
8. checking generated_clocks
9. checking loops
10. checking partial_input_delay
11. checking partial_output_delay
12. checking latch_loops

1. checking no_clock

There are 5 register/latch pins with no clock driven by root clock pin: convert1hz/slowClk_reg/C (HIGH)

There are 3 register/latch pins with no clock driven by root clock pin: convert2hz/slowClk_reg/C (HIGH)

2. checking constant_clock

There are 0 register/latch pins with constant_clock.

3. checking pulse_width_clock

There are 0 register/latch pins which need pulse_width check

4. checking unconstrained_internal_endpoints

There are 13 pins that are not constrained for maximum delay. (HIGH)

There are 0 pins that are not constrained for maximum delay due to constant clock.

5. checking no_input_delay

There is 1 input port with no input delay specified. (HIGH)

There are 0 input ports with no input delay but user has a false path constraint.

6. checking no_output_delay

There are 8 ports with no output delay specified. (HIGH)

There are 0 ports with no output delay but user has a false path constraint

There are 0 ports with no output delay but with a timing clock defined on it or propagating through it

7. checking multiple_clock

There are 0 register/latch pins with multiple clocks.

8. checking generated_clocks

There are 0 generated clocks that are not connected to a clock source.

9. checking loops

There are 0 combinational loops in the design.

10. checking partial_input_delay

There are 0 input ports with partial input delay specified.

11. checking partial_output_delay

There are 0 ports with partial output delay specified.

12. checking latch_loops

There are 0 combinational latch loops in the design through latch input

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| Design Timing Summary
| ---

WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
4.895	0.000	0	56	0.264	0.000	0	56	4.500	0.000	0	30

All user specified timing constraints are met.

| Clock Summary
| ---

Clock	Waveform(ns)	Period(ns)	Frequency(MHz)
sys_clk_pin	{0.000 5.000}	10.000	100.000

| Intra Clock Table
| ---

Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints WPWS(ns) TPWS(ns) TPWS Failing Endpoints TPWS Total Endpoints

Clock	WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
sys_clk_pin	4.895	0.000	0	56	0.264	0.000	0	56	4.500	0.000	0	30

| Inter Clock Table

| ----------------

From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints
---------- -------- ------- ------- ------------------- ------------------ ------- -------
------------------- ------------------

| Other Path Groups Table
| ----------------------

Path Group From Clock To Clock WNS(ns) TNS(ns) TNS Failing Endpoints TNS Total Endpoints WHS(ns) THS(ns) THS Failing Endpoints THS Total Endpoints
---------- ---------- -------- ------- ------- ------------------- ------------------ ------- -------
------- ------------------- ------------------

| Timing Details
| --------------

From Clock: sys_clk_pin
  To Clock: sys_clk_pin

Setup : 0 Failing Endpoints, Worst Slack 4.895ns, Total Violation 0.000ns
Hold : 0 Failing Endpoints, Worst Slack 0.264ns, Total Violation 0.000ns
PW : 0 Failing Endpoints, Worst Slack 4.500ns, Total Violation 0.000ns
---

Max Delay Paths

Slack (MET) : 4.895ns (required time - arrival time)
  Source: convert2hz/counter_reg[3]/C
  (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination: convert2hz/counter_reg[25]/R

(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group: sys_clk_pin
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 4.611ns (logic 1.058ns (22.944%) route 3.553ns (77.056%))
Logic Levels: 3 (LUT3=1 LUT4=1 LUT6=1)
Clock Path Skew: -0.029ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 4.853ns = (14.853 - 10.000)
Source Clock Delay (SCD): 5.155ns
Clock Pessimism Removal (CPR): 0.273ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock sys_clk_pin rise edge)	0.000	0.000 r	
W5		0.000	0.000 r	clk (IN)
	net (fo=0)	0.000	0.000	clk
W5	IBUF (Prop_ibuf_I_O)	1.458	1.458 r	clk_IBUF_inst/O
	net (fo=1, routed)	1.967	3.425	clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.096	3.521 r	clk_IBUF_BUFG_inst/O
	net (fo=29, routed)	1.634	5.155	convert2hz/clk_IBUF_BUFG
SLICE_X5Y8	FDRE		r	convert2hz/counter_reg[3]/C
SLICE_X5Y8	FDRE (Prop_fdre_C_Q)	0.456	5.611 f	convert2hz/counter_reg[3]/Q
	net (fo=2, routed)	0.857	6.468	convert2hz/counter_reg_n_0_[3]
SLICE_X4Y8	LUT4 (Prop_lut4_I2_O)	0.152	6.620 f	convert2hz/counter[27]_i_6/O
	net (fo=1, routed)	0.936	7.556	convert2hz/counter[27]_i_6_n_0
SLICE_X4Y13	LUT6 (Prop_lut6_I5_O)	0.326	7.882 f	convert2hz/counter[27]_i_2/O
	net (fo=2, routed)	0.963	8.845	convert2hz/counter[27]_i_2_n_0
SLICE_X4Y10	LUT3 (Prop_lut3_I0_O)	0.124	8.969 r	convert2hz/counter[27]_i_1/O
	net (fo=27, routed)	0.797	9.766	convert2hz/slowClk
SLICE_X5Y14	FDRE		r	convert2hz/counter_reg[25]/R

```
  -------------------------------------------------------------------    -------------------

                    (clock sys_clk_pin rise edge)
                                         10.000    10.000 r
    W5                                    0.000    10.000 r  clk (IN)
                    net (fo=0)            0.000    10.000    clk
    W5                IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                    net (fo=1, routed)          1.862    13.250    clk_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.091    13.341 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)         1.512    14.853    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y14         FDRE                                 r  convert2hz/counter_reg[25]/C
                    clock pessimism             0.273    15.126
                    clock uncertainty          -0.035    15.091
    SLICE_X5Y14         FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[25]
  -------------------------------------------------------------------
                    required time                         14.662
                    arrival time                          -9.766
  -------------------------------------------------------------------
                    slack                                 4.895

Slack (MET) :             4.895ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[26]/R
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.611ns  (logic 1.058ns (22.944%)  route 3.553ns (77.056%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter         (DJ):    0.000ns
    Phase Error             (PE):    0.000ns
```

```
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                      (clock sys_clk_pin rise edge)
                                                 0.000     0.000 r
  W5                                             0.000     0.000 r  clk (IN)
                      net (fo=0)                   0.000     0.000    clk
  W5                    IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
                      net (fo=1, routed)           1.967     3.425    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.096     3.521 r
clk_IBUF_BUFG_inst/O
                      net (fo=29, routed)          1.634     5.155    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y8          FDRE                                   r  convert2hz/counter_reg[3]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y8          FDRE (Prop_fdre_C_Q)         0.456     5.611 f
convert2hz/counter_reg[3]/Q
                      net (fo=2, routed)           0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8          LUT4 (Prop_lut4_I2_O)        0.152     6.620 f
convert2hz/counter[27]_i_6/O
                      net (fo=1, routed)           0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13         LUT6 (Prop_lut6_I5_O)        0.326     7.882 f
convert2hz/counter[27]_i_2/O
                      net (fo=2, routed)           0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10         LUT3 (Prop_lut3_I0_O)        0.124     8.969 r
convert2hz/counter[27]_i_1/O
                      net (fo=27, routed)          0.797     9.766    convert2hz/slowClk
  SLICE_X5Y14         FDRE                                   r  convert2hz/counter_reg[26]/R
 -------------------------------------------------------------------    -------------------

                      (clock sys_clk_pin rise edge)
                                                10.000    10.000 r
  W5                                            0.000    10.000 r  clk (IN)
                      net (fo=0)                   0.000    10.000    clk
  W5                    IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                      net (fo=1, routed)           1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.091    13.341 r
clk_IBUF_BUFG_inst/O
                      net (fo=29, routed)          1.512    14.853    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y14         FDRE                                   r  convert2hz/counter_reg[26]/C
                      clock pessimism              0.273    15.126
                      clock uncertainty           -0.035    15.091
  SLICE_X5Y14         FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[26]
```

```
  -------------------------------------------------------------------
                    required time                         14.662
                    arrival time                          -9.766
  -------------------------------------------------------------------
                    slack                                  4.895

Slack (MET) :             4.895ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[27]/R
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.611ns  (logic 1.058ns (22.944%)  route 3.553ns (77.056%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter         (DJ):    0.000ns
    Phase Error             (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                         0.000     0.000 r
    W5                                   0.000     0.000 r  clk (IN)
                    net (fo=0)           0.000     0.000    clk
    W5                  IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
                    net (fo=1, routed)           1.967     3.425    clk_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.096     3.521 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          1.634     5.155    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y8          FDRE                                 r  convert2hz/counter_reg[3]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y8          FDRE (Prop_fdre_C_Q)         0.456     5.611 f
convert2hz/counter_reg[3]/Q
```

```
                net (fo=2, routed)           0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8          LUT4 (Prop_lut4_I2_O)        0.152     6.620 f
convert2hz/counter[27]_i_6/O
                net (fo=1, routed)           0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13         LUT6 (Prop_lut6_I5_O)        0.326     7.882 f
convert2hz/counter[27]_i_2/O
                net (fo=2, routed)           0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10         LUT3 (Prop_lut3_I0_O)        0.124     8.969 r
convert2hz/counter[27]_i_1/O
                net (fo=27, routed)          0.797     9.766    convert2hz/slowClk
  SLICE_X5Y14         FDRE                                 r  convert2hz/counter_reg[27]/R
 ----------------------------------------------------------------------    -------------------

                (clock sys_clk_pin rise edge)
                                    10.000    10.000 r
  W5                                 0.000    10.000 r  clk (IN)
                net (fo=0)           0.000    10.000    clk
  W5                IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk_IBUF_inst/O
                net (fo=1, routed)           1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.091    13.341 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          1.512    14.853    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y14         FDRE                                 r  convert2hz/counter_reg[27]/C
                clock pessimism              0.273    15.126
                clock uncertainty           -0.035    15.091
  SLICE_X5Y14         FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[27]
 ----------------------------------------------------------------------
                required time                         14.662
                arrival time                          -9.766
 ----------------------------------------------------------------------
                slack                                  4.895

Slack (MET) :             5.034ns  (required time - arrival time)
 Source:                 convert2hz/counter_reg[3]/C
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[21]/R
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Setup (Max at Slow Process Corner)
 Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
```

```
  Data Path Delay:        4.473ns  (logic 1.058ns (23.654%)  route 3.415ns (76.346%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter         (DJ):    0.000ns
    Phase Error             (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                         net (fo=0)                 0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)       1.458     1.458 r  clk_IBUF_inst/O
                         net (fo=1, routed)         1.967     3.425    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)       0.096     3.521 r
clk_IBUF_BUFG_inst/O
                         net (fo=29, routed)        1.634     5.155    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y8           FDRE                                 r  convert2hz/counter_reg[3]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y8           FDRE (Prop_fdre_C_Q)       0.456     5.611 f
convert2hz/counter_reg[3]/Q
                         net (fo=2, routed)         0.857     6.468    convert2hz/counter_reg_n_0_[3]
    SLICE_X4Y8           LUT4 (Prop_lut4_I2_O)      0.152     6.620 f
convert2hz/counter[27]_i_6/O
                         net (fo=1, routed)         0.936     7.556    convert2hz/counter[27]_i_6_n_0
    SLICE_X4Y13          LUT6 (Prop_lut6_I5_O)      0.326     7.882 f
convert2hz/counter[27]_i_2/O
                         net (fo=2, routed)         0.963     8.845    convert2hz/counter[27]_i_2_n_0
    SLICE_X4Y10          LUT3 (Prop_lut3_I0_O)      0.124     8.969 r
convert2hz/counter[27]_i_1/O
                         net (fo=27, routed)        0.659     9.628    convert2hz/slowClk
    SLICE_X5Y13          FDRE                                 r  convert2hz/counter_reg[21]/R
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                   10.000    10.000 r
    W5                                             0.000    10.000 r  clk (IN)
```

```
                net (fo=0)                   0.000    10.000    clk
  W5                IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk_IBUF_inst/O
                net (fo=1, routed)           1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.091    13.341 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          1.512    14.853    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y13         FDRE                                 r  convert2hz/counter_reg[21]/C
                clock pessimism              0.273    15.126
                clock uncertainty           -0.035    15.091
  SLICE_X5Y13         FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[21]
 -------------------------------------------------------------------
                required time                         14.662
                arrival time                          -9.628
 -------------------------------------------------------------------
                slack                                  5.034

Slack (MET) :             5.034ns  (required time - arrival time)
 Source:                 convert2hz/counter_reg[3]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[22]/R
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Setup (Max at Slow Process Corner)
 Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:        4.473ns  (logic 1.058ns (23.654%)  route 3.415ns (76.346%))
 Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
 Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
   Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
   Source Clock Delay      (SCD):    5.155ns
   Clock Pessimism Removal (CPR):    0.273ns
 Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
   Total System Jitter     (TSJ):    0.071ns
   Total Input Jitter      (TIJ):    0.000ns
   Discrete Jitter         (DJ):    0.000ns
   Phase Error             (PE):    0.000ns

   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                (clock sys_clk_pin rise edge)
                                      0.000     0.000 r
```

```
  W5                                        0.000     0.000 r  clk (IN)
                    net (fo=0)                  0.000     0.000    clk
  W5                  IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
                    net (fo=1, routed)          1.967     3.425    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.096     3.521 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)         1.634     5.155    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y8          FDRE                                         r  convert2hz/counter_reg[3]/C
 ----------------------------------------------------------------    -------------------
  SLICE_X5Y8          FDRE (Prop_fdre_C_Q)        0.456     5.611 f
convert2hz/counter_reg[3]/Q
                    net (fo=2, routed)          0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8          LUT4 (Prop_lut4_I2_O)       0.152     6.620 f
convert2hz/counter[27]_i_6/O
                    net (fo=1, routed)          0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13         LUT6 (Prop_lut6_I5_O)       0.326     7.882 f
convert2hz/counter[27]_i_2/O
                    net (fo=2, routed)          0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10         LUT3 (Prop_lut3_I0_O)       0.124     8.969 r
convert2hz/counter[27]_i_1/O
                    net (fo=27, routed)         0.659     9.628    convert2hz/slowClk
  SLICE_X5Y13         FDRE                                         r  convert2hz/counter_reg[22]/R
 ----------------------------------------------------------------    -------------------

                    (clock sys_clk_pin rise edge)
                                               10.000    10.000 r
  W5                                           0.000    10.000 r  clk (IN)
                    net (fo=0)                  0.000    10.000    clk
  W5                  IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                    net (fo=1, routed)          1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.091    13.341 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)         1.512    14.853    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y13         FDRE                                         r  convert2hz/counter_reg[22]/C
                    clock pessimism             0.273    15.126
                    clock uncertainty          -0.035    15.091
  SLICE_X5Y13         FDRE (Setup_fdre_C_R)      -0.429    14.662
convert2hz/counter_reg[22]
 ----------------------------------------------------------------
                    required time                         14.662
                    arrival time                          -9.628
 ----------------------------------------------------------------
                    slack                                  5.034
```

```
Slack (MET) :             5.034ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[23]/R
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.473ns  (logic 1.058ns (23.654%)  route 3.415ns (76.346%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter         (DJ):    0.000ns
    Phase Error             (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                         (clock sys_clk_pin rise edge)
                                                    0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                         net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)         1.458     1.458 r  clk_IBUF_inst/O
                         net (fo=1, routed)           1.967     3.425    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.096     3.521 r
clk_IBUF_BUFG_inst/O
                         net (fo=29, routed)          1.634     5.155    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y8           FDRE                                   r  convert2hz/counter_reg[3]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y8           FDRE (Prop_fdre_C_Q)         0.456     5.611 f
convert2hz/counter_reg[3]/Q
                         net (fo=2, routed)           0.857     6.468    convert2hz/counter_reg_n_0_[3]
    SLICE_X4Y8           LUT4 (Prop_lut4_I2_O)        0.152     6.620 f
convert2hz/counter[27]_i_6/O
                         net (fo=1, routed)           0.936     7.556    convert2hz/counter[27]_i_6_n_0
```

```
    SLICE_X4Y13          LUT6 (Prop_lut6_I5_O)        0.326     7.882 f
convert2hz/counter[27]_i_2/O
                         net (fo=2, routed)           0.963     8.845    convert2hz/counter[27]_i_2_n_0
    SLICE_X4Y10          LUT3 (Prop_lut3_I0_O)        0.124     8.969 r
convert2hz/counter[27]_i_1/O
                         net (fo=27, routed)          0.659     9.628    convert2hz/slowClk
    SLICE_X5Y13          FDRE                                       r  convert2hz/counter_reg[23]/R
  -------------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                                     10.000    10.000 r
    W5                                               0.000    10.000 r  clk (IN)
                         net (fo=0)                  0.000    10.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                         net (fo=1, routed)          1.862    13.250    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.091    13.341 r
clk_IBUF_BUFG_inst/O
                         net (fo=29, routed)          1.512    14.853    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y13          FDRE                                       r  convert2hz/counter_reg[23]/C
                         clock pessimism              0.273    15.126
                         clock uncertainty           -0.035    15.091
    SLICE_X5Y13          FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[23]
  -------------------------------------------------------------------
                         required time                         14.662
                         arrival time                          -9.628
  -------------------------------------------------------------------
                         slack                                  5.034

Slack (MET) :             5.034ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[24]/R
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.473ns  (logic 1.058ns (23.654%)  route 3.415ns (76.346%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.029ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.853ns = ( 14.853 - 10.000 )
```

```
  Source Clock Delay      (SCD):    5.155ns
  Clock Pessimism Removal (CPR):    0.273ns
Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
  Total System Jitter     (TSJ):    0.071ns
  Total Input Jitter      (TIJ):    0.000ns
  Discrete Jitter         (DJ):    0.000ns
  Phase Error             (PE):    0.000ns

  Location           Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                   (clock sys_clk_pin rise edge)
                                              0.000     0.000 r
  W5                                          0.000     0.000 r  clk (IN)
                   net (fo=0)                   0.000     0.000    clk
  W5                 IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
                   net (fo=1, routed)           1.967     3.425    clk_IBUF
  BUFGCTRL_X0Y0      BUFG (Prop_bufg_I_O)        0.096     3.521 r
clk_IBUF_BUFG_inst/O
                   net (fo=29, routed)          1.634     5.155    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y8         FDRE                                   r  convert2hz/counter_reg[3]/C
-------------------------------------------------------------------    -------------------
  SLICE_X5Y8         FDRE (Prop_fdre_C_Q)        0.456     5.611 f
convert2hz/counter_reg[3]/Q
                   net (fo=2, routed)           0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8         LUT4 (Prop_lut4_I2_O)       0.152     6.620 f
convert2hz/counter[27]_i_6/O
                   net (fo=1, routed)           0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13        LUT6 (Prop_lut6_I5_O)       0.326     7.882 f
convert2hz/counter[27]_i_2/O
                   net (fo=2, routed)           0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10        LUT3 (Prop_lut3_I0_O)       0.124     8.969 r
convert2hz/counter[27]_i_1/O
                   net (fo=27, routed)          0.659     9.628    convert2hz/slowClk
  SLICE_X5Y13        FDRE                                   r  convert2hz/counter_reg[24]/R
-------------------------------------------------------------------    -------------------

                   (clock sys_clk_pin rise edge)
                                             10.000    10.000 r
  W5                                          0.000    10.000 r  clk (IN)
                   net (fo=0)                   0.000    10.000    clk
  W5                 IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                   net (fo=1, routed)           1.862    13.250    clk_IBUF
```

```
   BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.091    13.341 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          1.512    14.853    convert2hz/clk_IBUF_BUFG
   SLICE_X5Y13          FDRE                                         r  convert2hz/counter_reg[24]/C
                    clock pessimism              0.273    15.126
                    clock uncertainty           -0.035    15.091
   SLICE_X5Y13          FDRE (Setup_fdre_C_R)       -0.429    14.662
convert2hz/counter_reg[24]
  -------------------------------------------------------------------
                    required time                         14.662
                    arrival time                          -9.628
  -------------------------------------------------------------------
                    slack                                  5.034

Slack (MET) :             5.045ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[10]/R
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.465ns  (logic 1.058ns (23.697%)  route 3.407ns (76.303%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.026ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter         (DJ):    0.000ns
    Phase Error             (PE):    0.000ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
   W5                                             0.000     0.000 r  clk (IN)
                    net (fo=0)                    0.000     0.000    clk
   W5                 IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
```

```
                net (fo=1, routed)           1.967     3.425    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.096     3.521 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          1.634     5.155    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y8          FDRE                                 r  convert2hz/counter_reg[3]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y8          FDRE (Prop_fdre_C_Q)         0.456     5.611 f
convert2hz/counter_reg[3]/Q
                net (fo=2, routed)           0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8          LUT4 (Prop_lut4_I2_O)        0.152     6.620 f
convert2hz/counter[27]_i_6/O
                net (fo=1, routed)           0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13         LUT6 (Prop_lut6_I5_O)        0.326     7.882 f
convert2hz/counter[27]_i_2/O
                net (fo=2, routed)           0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10         LUT3 (Prop_lut3_I0_O)        0.124     8.969 r
convert2hz/counter[27]_i_1/O
                net (fo=27, routed)          0.651     9.620    convert2hz/slowClk
  SLICE_X5Y10         FDRE                                 r  convert2hz/counter_reg[10]/R
 -------------------------------------------------------------------    -------------------

                (clock sys_clk_pin rise edge)
                                    10.000    10.000 r
  W5                                  0.000    10.000 r  clk (IN)
                net (fo=0)                   0.000    10.000    clk
  W5                  IBUF (Prop_ibuf_I_O)         1.388    11.388 r  clk_IBUF_inst/O
                net (fo=1, routed)           1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.091    13.341 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          1.515    14.856    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y10         FDRE                                 r  convert2hz/counter_reg[10]/C
                clock pessimism              0.273    15.129
                clock uncertainty           -0.035    15.094
  SLICE_X5Y10         FDRE (Setup_fdre_C_R)       -0.429    14.665
convert2hz/counter_reg[10]
 -------------------------------------------------------------------
                required time                         14.665
                arrival time                          -9.620
 -------------------------------------------------------------------
                slack                                  5.045

Slack (MET) :             5.045ns  (required time - arrival time)
 Source:                 convert2hz/counter_reg[3]/C
```

(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Destination: convert2hz/counter_reg[11]/R
(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group: sys_clk_pin
Path Type: Setup (Max at Slow Process Corner)
Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 4.465ns (logic 1.058ns (23.697%) route 3.407ns (76.303%))
Logic Levels: 3 (LUT3=1 LUT4=1 LUT6=1)
Clock Path Skew: -0.026ns (DCD - SCD + CPR)
Destination Clock Delay (DCD): 4.856ns = (14.856 - 10.000)
Source Clock Delay (SCD): 5.155ns
Clock Pessimism Removal (CPR): 0.273ns
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ): 0.071ns
Total Input Jitter (TIJ): 0.000ns
Discrete Jitter (DJ): 0.000ns
Phase Error (PE): 0.000ns

Location	Delay type	Incr(ns)	Path(ns)	Netlist Resource(s)
	(clock sys_clk_pin rise edge)	0.000	0.000 r	
W5		0.000	0.000 r	clk (IN)
	net (fo=0)	0.000	0.000	clk
W5	IBUF (Prop_ibuf_I_O)	1.458	1.458 r	clk_IBUF_inst/O
	net (fo=1, routed)	1.967	3.425	clk_IBUF
BUFGCTRL_X0Y0	BUFG (Prop_bufg_I_O)	0.096	3.521 r	clk_IBUF_BUFG_inst/O
	net (fo=29, routed)	1.634	5.155	convert2hz/clk_IBUF_BUFG
SLICE_X5Y8	FDRE		r	convert2hz/counter_reg[3]/C
SLICE_X5Y8	FDRE (Prop_fdre_C_Q)	0.456	5.611 f	convert2hz/counter_reg[3]/Q
	net (fo=2, routed)	0.857	6.468	convert2hz/counter_reg_n_0_[3]
SLICE_X4Y8	LUT4 (Prop_lut4_I2_O)	0.152	6.620 f	convert2hz/counter[27]_i_6/O
	net (fo=1, routed)	0.936	7.556	convert2hz/counter[27]_i_6_n_0
SLICE_X4Y13	LUT6 (Prop_lut6_I5_O)	0.326	7.882 f	convert2hz/counter[27]_i_2/O
	net (fo=2, routed)	0.963	8.845	convert2hz/counter[27]_i_2_n_0

```
    SLICE_X4Y10          LUT3 (Prop_lut3_I0_O)        0.124     8.969 r
convert2hz/counter[27]_i_1/O
                         net (fo=27, routed)          0.651     9.620    convert2hz/slowClk
    SLICE_X5Y10          FDRE                                       r  convert2hz/counter_reg[11]/R
  ----------------------------------------------------------------    -------------------

                         (clock sys_clk_pin rise edge)
                                              10.000    10.000 r
    W5                                         0.000    10.000 r  clk (IN)
                         net (fo=0)                    0.000    10.000    clk
    W5                     IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                         net (fo=1, routed)            1.862    13.250    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)          0.091    13.341 r
clk_IBUF_BUFG_inst/O
                         net (fo=29, routed)           1.515    14.856    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y10          FDRE                                       r  convert2hz/counter_reg[11]/C
                         clock pessimism               0.273    15.129
                         clock uncertainty            -0.035    15.094
    SLICE_X5Y10          FDRE (Setup_fdre_C_R)        -0.429    14.665
convert2hz/counter_reg[11]
  -------------------------------------------------------------------
                         required time                         14.665
                         arrival time                          -9.620
  -------------------------------------------------------------------
                         slack                                  5.045

Slack (MET) :             5.045ns  (required time - arrival time)
  Source:                 convert2hz/counter_reg[3]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[12]/R
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        4.465ns  (logic 1.058ns (23.697%)  route 3.407ns (76.303%))
  Logic Levels:           3  (LUT3=1 LUT4=1 LUT6=1)
  Clock Path Skew:        -0.026ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    4.856ns = ( 14.856 - 10.000 )
    Source Clock Delay      (SCD):    5.155ns
    Clock Pessimism Removal (CPR):    0.273ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
```

```
  Total System Jitter     (TSJ):    0.071ns
  Total Input Jitter      (TIJ):    0.000ns
  Discrete Jitter         (DJ):     0.000ns
  Phase Error             (PE):     0.000ns

  Location           Delay type              Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                     (clock sys_clk_pin rise edge)
                                             0.000     0.000 r
  W5                                         0.000     0.000 r  clk (IN)
                     net (fo=0)              0.000     0.000    clk
  W5                   IBUF (Prop_ibuf_I_O)        1.458     1.458 r  clk_IBUF_inst/O
                     net (fo=1, routed)          1.967     3.425    clk_IBUF
  BUFGCTRL_X0Y0      BUFG (Prop_bufg_I_O)        0.096     3.521 r
clk_IBUF_BUFG_inst/O
                     net (fo=29, routed)         1.634     5.155    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y8         FDRE                                  r  convert2hz/counter_reg[3]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y8         FDRE (Prop_fdre_C_Q)        0.456     5.611 f
convert2hz/counter_reg[3]/Q
                     net (fo=2, routed)          0.857     6.468    convert2hz/counter_reg_n_0_[3]
  SLICE_X4Y8         LUT4 (Prop_lut4_I2_O)       0.152     6.620 f
convert2hz/counter[27]_i_6/O
                     net (fo=1, routed)          0.936     7.556    convert2hz/counter[27]_i_6_n_0
  SLICE_X4Y13        LUT6 (Prop_lut6_I5_O)       0.326     7.882 f
convert2hz/counter[27]_i_2/O
                     net (fo=2, routed)          0.963     8.845    convert2hz/counter[27]_i_2_n_0
  SLICE_X4Y10        LUT3 (Prop_lut3_I0_O)       0.124     8.969 r
convert2hz/counter[27]_i_1/O
                     net (fo=27, routed)         0.651     9.620    convert2hz/slowClk
  SLICE_X5Y10        FDRE                                  r  convert2hz/counter_reg[12]/R
 -------------------------------------------------------------------    -------------------

                     (clock sys_clk_pin rise edge)
                                            10.000    10.000 r
  W5                                         0.000    10.000 r  clk (IN)
                     net (fo=0)              0.000    10.000    clk
  W5                   IBUF (Prop_ibuf_I_O)        1.388    11.388 r  clk_IBUF_inst/O
                     net (fo=1, routed)          1.862    13.250    clk_IBUF
  BUFGCTRL_X0Y0      BUFG (Prop_bufg_I_O)        0.091    13.341 r
clk_IBUF_BUFG_inst/O
                     net (fo=29, routed)         1.515    14.856    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y10        FDRE                                  r  convert2hz/counter_reg[12]/C
```

clock pessimism 0.273 15.129
clock uncertainty -0.035 15.094
SLICE_X5Y10 FDRE (Setup_fdre_C_R) -0.429 14.665 convert2hz/counter_reg[12]
---
required time 14.665
arrival time -9.620
---
slack 5.045

Min Delay Paths

Slack (MET) : 0.264ns (arrival time - required time)
Source: convert2hz/counter_reg[12]/C
(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Destination: convert2hz/counter_reg[12]/D
(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group: sys_clk_pin
Path Type: Hold (Min at Fast Process Corner)
Requirement: 0.000ns (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay: 0.369ns (logic 0.249ns (67.424%) route 0.120ns (32.576%))
Logic Levels: 1 (CARRY4=1)
Clock Path Skew: 0.000ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): 1.989ns
Source Clock Delay (SCD): 1.474ns
Clock Pessimism Removal (CPR): 0.515ns

Location Delay type Incr(ns) Path(ns) Netlist Resource(s)

(clock sys_clk_pin rise edge)
0.000 0.000 r
W5 0.000 0.000 r clk (IN)
net (fo=0) 0.000 0.000 clk
W5 IBUF (Prop_ibuf_I_O) 0.226 0.226 r clk_IBUF_inst/O
net (fo=1, routed) 0.631 0.858 clk_IBUF
BUFGCTRL_X0Y0 BUFG (Prop_bufg_I_O) 0.026 0.884 r clk_IBUF_BUFG_inst/O

```
                net (fo=29, routed)          0.591     1.474    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y10          FDRE                                         r  convert2hz/counter_reg[12]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y10          FDRE (Prop_fdre_C_Q)         0.141     1.615 r
convert2hz/counter_reg[12]/Q
                net (fo=2, routed)           0.120     1.735    convert2hz/counter_reg_n_0_[12]
  SLICE_X5Y10          CARRY4 (Prop_carry4_S[3]_O[3])
                                             0.108     1.843 r  convert2hz/counter0_carry__1/O[3]
                net (fo=1, routed)           0.000     1.843    convert2hz/data0[12]
  SLICE_X5Y10          FDRE                                         r  convert2hz/counter_reg[12]/D
 -------------------------------------------------------------------    -------------------

                (clock sys_clk_pin rise edge)
                                             0.000     0.000 r
  W5                                         0.000     0.000 r  clk (IN)
                net (fo=0)                   0.000     0.000    clk
  W5                 IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk_IBUF_inst/O
                net (fo=1, routed)           0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)         0.029     1.128 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          0.862     1.989    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y10          FDRE                                         r  convert2hz/counter_reg[12]/C
                clock pessimism             -0.515     1.474
  SLICE_X5Y10          FDRE (Hold_fdre_C_D)         0.105     1.579
convert2hz/counter_reg[12]
 -------------------------------------------------------------------
                required time                         -1.579
                arrival time                           1.843
 -------------------------------------------------------------------
                slack                                  0.264

Slack (MET) :             0.264ns  (arrival time - required time)
 Source:                 convert2hz/counter_reg[16]/C
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[16]/D
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Hold (Min at Fast Process Corner)
 Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:        0.369ns  (logic 0.249ns (67.424%)  route 0.120ns (32.576%))
 Logic Levels:           1  (CARRY4=1)
```

```
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.989ns
    Source Clock Delay      (SCD):    1.474ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location           Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.591     1.474    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y11          FDRE                                   r  convert2hz/counter_reg[16]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y11          FDRE (Prop_fdre_C_Q)        0.141     1.615 r
convert2hz/counter_reg[16]/Q
                       net (fo=2, routed)           0.120     1.735    convert2hz/counter_reg_n_0_[16]
    SLICE_X5Y11          CARRY4 (Prop_carry4_S[3]_O[3])
                                                  0.108     1.843 r  convert2hz/counter0_carry__2/O[3]
                       net (fo=1, routed)           0.000     1.843    convert2hz/data0[16]
    SLICE_X5Y11          FDRE                                   r  convert2hz/counter_reg[16]/D
  -------------------------------------------------------------------    -------------------

                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.414     0.414 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.685     1.099    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.029     1.128 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.862     1.989    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y11          FDRE                                   r  convert2hz/counter_reg[16]/C
                       clock pessimism             -0.515     1.474
    SLICE_X5Y11          FDRE (Hold_fdre_C_D)        0.105     1.579
convert2hz/counter_reg[16]
  -------------------------------------------------------------------
                       required time                         -1.579
                       arrival time                           1.843
```

```
  ----------------------------------------------------------------------
                    slack                                 0.264

Slack (MET) :             0.264ns  (arrival time - required time)
  Source:                 convert2hz/counter_reg[20]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[20]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.369ns  (logic 0.249ns (67.424%)  route 0.120ns (32.576%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.987ns
    Source Clock Delay      (SCD):    1.473ns
    Clock Pessimism Removal (CPR):    0.514ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                         0.000     0.000 r
    W5                                   0.000     0.000 r  clk (IN)
                    net (fo=0)           0.000     0.000    clk
    W5                 IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                    net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.590     1.473    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y12         FDRE                                   r  convert2hz/counter_reg[20]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y12         FDRE (Prop_fdre_C_Q)         0.141     1.614 r
convert2hz/counter_reg[20]/Q
                    net (fo=2, routed)           0.120     1.734    convert2hz/counter_reg_n_0_[20]
    SLICE_X5Y12         CARRY4 (Prop_carry4_S[3]_O[3])
                                         0.108     1.842 r  convert2hz/counter0_carry__3/O[3]
                    net (fo=1, routed)           0.000     1.842    convert2hz/data0[20]
    SLICE_X5Y12         FDRE                                   r  convert2hz/counter_reg[20]/D
  -------------------------------------------------------------------    -------------------

                    (clock sys_clk_pin rise edge)
```

```
                                    0.000     0.000 r
  W5                                0.000     0.000 r  clk (IN)
                    net (fo=0)      0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)      0.414     0.414 r  clk_IBUF_inst/O
                    net (fo=1, routed)        0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0     BUFG (Prop_bufg_I_O)      0.029     1.128 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)       0.860     1.987    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y12       FDRE                                r  convert2hz/counter_reg[20]/C
                    clock pessimism           -0.514     1.473
  SLICE_X5Y12       FDRE (Hold_fdre_C_D)      0.105     1.578
convert2hz/counter_reg[20]
 -------------------------------------------------------------------
                    required time                        -1.578
                    arrival time                          1.842
 -------------------------------------------------------------------
                    slack                                 0.264

Slack (MET) :             0.264ns  (arrival time - required time)
 Source:                  convert2hz/counter_reg[24]/C
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:             convert2hz/counter_reg[24]/D
                         (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:              sys_clk_pin
 Path Type:               Hold (Min at Fast Process Corner)
 Requirement:             0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:         0.369ns  (logic 0.249ns (67.424%)  route 0.120ns (32.576%))
 Logic Levels:            1  (CARRY4=1)
 Clock Path Skew:         0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD):    1.986ns
   Source Clock Delay      (SCD):    1.472ns
   Clock Pessimism Removal (CPR):    0.514ns

   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                    0.000     0.000 r
  W5                                0.000     0.000 r  clk (IN)
                    net (fo=0)      0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)      0.226     0.226 r  clk_IBUF_inst/O
                    net (fo=1, routed)        0.631     0.858    clk_IBUF
```

```
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.589     1.472    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y13         FDRE                                         r  convert2hz/counter_reg[24]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y13         FDRE (Prop_fdre_C_Q)         0.141     1.613 r
convert2hz/counter_reg[24]/Q
                    net (fo=2, routed)           0.120     1.733    convert2hz/counter_reg_n_0_[24]
  SLICE_X5Y13         CARRY4 (Prop_carry4_S[3]_O[3])
                                                   0.108     1.841 r  convert2hz/counter0_carry__4/O[3]
                    net (fo=1, routed)           0.000     1.841    convert2hz/data0[24]
  SLICE_X5Y13         FDRE                                         r  convert2hz/counter_reg[24]/D
 -------------------------------------------------------------------    -------------------

                    (clock sys_clk_pin rise edge)
                                                   0.000     0.000 r
  W5                                               0.000     0.000 r  clk (IN)
                    net (fo=0)                     0.000     0.000    clk
  W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk_IBUF_inst/O
                    net (fo=1, routed)           0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.859     1.986    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y13         FDRE                                         r  convert2hz/counter_reg[24]/C
                    clock pessimism             -0.514     1.472
  SLICE_X5Y13         FDRE (Hold_fdre_C_D)         0.105     1.577
convert2hz/counter_reg[24]
 -------------------------------------------------------------------
                    required time                         -1.577
                    arrival time                           1.841
 -------------------------------------------------------------------
                    slack                                  0.264

Slack (MET) :             0.264ns  (arrival time - required time)
 Source:                 convert2hz/counter_reg[4]/C
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[4]/D
                           (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Hold (Min at Fast Process Corner)
 Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
```

```
  Data Path Delay:        0.369ns  (logic 0.249ns (67.424%)  route 0.120ns (32.576%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.990ns
    Source Clock Delay      (SCD):    1.475ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.592     1.475    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y8           FDRE                                   r  convert2hz/counter_reg[4]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y8           FDRE (Prop_fdre_C_Q)        0.141     1.616 r
convert2hz/counter_reg[4]/Q
                       net (fo=2, routed)           0.120     1.736    convert2hz/counter_reg_n_0_[4]
    SLICE_X5Y8           CARRY4 (Prop_carry4_S[3]_O[3])
                                                  0.108     1.844 r  convert2hz/counter0_carry/O[3]
                       net (fo=1, routed)           0.000     1.844    convert2hz/data0[4]
    SLICE_X5Y8           FDRE                                   r  convert2hz/counter_reg[4]/D
  -------------------------------------------------------------------    -------------------

                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.414     0.414 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.685     1.099    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.029     1.128 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.863     1.990    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y8           FDRE                                   r  convert2hz/counter_reg[4]/C
                       clock pessimism             -0.515     1.475
    SLICE_X5Y8           FDRE (Hold_fdre_C_D)        0.105     1.580    convert2hz/counter_reg[4]
  -------------------------------------------------------------------
                       required time                         -1.580
```

```
                    arrival time                           1.844
  ----------------------------------------------------------------------
                    slack                                  0.264

Slack (MET) :             0.264ns  (arrival time - required time)
  Source:                 convert2hz/counter_reg[8]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[8]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.369ns  (logic 0.249ns (67.424%)  route 0.120ns (32.576%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.990ns
    Source Clock Delay      (SCD):    1.475ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                         0.000     0.000 r
    W5                                   0.000     0.000 r  clk (IN)
                    net (fo=0)           0.000     0.000    clk
    W5                IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                    net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.592     1.475    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y9          FDRE                                 r  convert2hz/counter_reg[8]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y9          FDRE (Prop_fdre_C_Q)        0.141     1.616 r
convert2hz/counter_reg[8]/Q
                    net (fo=2, routed)           0.120     1.736    convert2hz/counter_reg_n_0_[8]
    SLICE_X5Y9          CARRY4 (Prop_carry4_S[3]_O[3])
                                         0.108     1.844 r  convert2hz/counter0_carry__0/O[3]
                    net (fo=1, routed)           0.000     1.844    convert2hz/data0[8]
    SLICE_X5Y9          FDRE                                 r  convert2hz/counter_reg[8]/D
  -------------------------------------------------------------------    -------------------
```

```
                    (clock sys_clk_pin rise edge)
                                         0.000     0.000 r
  W5                                     0.000     0.000 r  clk (IN)
                    net (fo=0)           0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)        0.414     0.414 r  clk_IBUF_inst/O
                    net (fo=1, routed)          0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0     BUFG (Prop_bufg_I_O)        0.029     1.128 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)         0.863     1.990    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y9        FDRE                                  r  convert2hz/counter_reg[8]/C
                    clock pessimism             -0.515     1.475
  SLICE_X5Y9        FDRE (Hold_fdre_C_D)        0.105     1.580    convert2hz/counter_reg[8]
 -------------------------------------------------------------------
                    required time                         -1.580
                    arrival time                           1.844
 -------------------------------------------------------------------
                    slack                                  0.264

Slack (MET) :             0.267ns  (arrival time - required time)
 Source:                 convert2hz/counter_reg[13]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[13]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Hold (Min at Fast Process Corner)
 Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:        0.372ns  (logic 0.256ns (68.766%)  route 0.116ns (31.234%))
 Logic Levels:           1  (CARRY4=1)
 Clock Path Skew:        0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD):    1.989ns
   Source Clock Delay      (SCD):    1.474ns
   Clock Pessimism Removal (CPR):    0.515ns

   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                    (clock sys_clk_pin rise edge)
                                         0.000     0.000 r
  W5                                     0.000     0.000 r  clk (IN)
                    net (fo=0)           0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                    net (fo=1, routed)          0.631     0.858    clk_IBUF
```

```
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.591     1.474    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y11         FDRE                                         r  convert2hz/counter_reg[13]/C
  -------------------------------------------------------------------    -------------------
  SLICE_X5Y11         FDRE (Prop_fdre_C_Q)         0.141     1.615 r
convert2hz/counter_reg[13]/Q
                    net (fo=2, routed)           0.116     1.731    convert2hz/counter_reg_n_0_[13]
  SLICE_X5Y11         CARRY4 (Prop_carry4_S[0]_O[0])
                                                   0.115     1.846 r  convert2hz/counter0_carry__2/O[0]
                    net (fo=1, routed)           0.000     1.846    convert2hz/data0[13]
  SLICE_X5Y11         FDRE                                         r  convert2hz/counter_reg[13]/D
  -------------------------------------------------------------------    -------------------

                    (clock sys_clk_pin rise edge)
                                                   0.000     0.000 r
  W5                                               0.000     0.000 r  clk (IN)
                    net (fo=0)                     0.000     0.000    clk
  W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk_IBUF_inst/O
                    net (fo=1, routed)           0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r
clk_IBUF_BUFG_inst/O
                    net (fo=29, routed)          0.862     1.989    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y11         FDRE                                         r  convert2hz/counter_reg[13]/C
                    clock pessimism             -0.515     1.474
  SLICE_X5Y11         FDRE (Hold_fdre_C_D)         0.105     1.579
convert2hz/counter_reg[13]
  -------------------------------------------------------------------
                    required time                         -1.579
                    arrival time                           1.846
  -------------------------------------------------------------------
                    slack                                  0.267

Slack (MET) :             0.267ns  (arrival time - required time)
  Source:                 convert2hz/counter_reg[9]/C
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[9]/D
                            (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
```

```
  Data Path Delay:        0.372ns  (logic 0.256ns (68.766%)  route 0.116ns (31.234%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.989ns
    Source Clock Delay      (SCD):    1.474ns
    Clock Pessimism Removal (CPR):    0.515ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.026     0.884 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.591     1.474    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y10          FDRE                                   r  convert2hz/counter_reg[9]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y10          FDRE (Prop_fdre_C_Q)        0.141     1.615 r
convert2hz/counter_reg[9]/Q
                       net (fo=2, routed)           0.116     1.731    convert2hz/counter_reg_n_0_[9]
    SLICE_X5Y10          CARRY4 (Prop_carry4_S[0]_O[0])
                                                  0.115     1.846 r  convert2hz/counter0_carry__1/O[0]
                       net (fo=1, routed)           0.000     1.846    convert2hz/data0[9]
    SLICE_X5Y10          FDRE                                   r  convert2hz/counter_reg[9]/D
  -------------------------------------------------------------------    -------------------

                       (clock sys_clk_pin rise edge)
                                                  0.000     0.000 r
    W5                                              0.000     0.000 r  clk (IN)
                       net (fo=0)                   0.000     0.000    clk
    W5                   IBUF (Prop_ibuf_I_O)        0.414     0.414 r  clk_IBUF_inst/O
                       net (fo=1, routed)           0.685     1.099    clk_IBUF
    BUFGCTRL_X0Y0        BUFG (Prop_bufg_I_O)        0.029     1.128 r
clk_IBUF_BUFG_inst/O
                       net (fo=29, routed)          0.862     1.989    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y10          FDRE                                   r  convert2hz/counter_reg[9]/C
                       clock pessimism             -0.515     1.474
    SLICE_X5Y10          FDRE (Hold_fdre_C_D)        0.105     1.579    convert2hz/counter_reg[9]
  -------------------------------------------------------------------
                       required time                         -1.579
```

```
                  arrival time                           1.846
  ---------------------------------------------------------------------
                  slack                                  0.267


Slack (MET) :             0.267ns  (arrival time - required time)
  Source:                 convert2hz/counter_reg[17]/C
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Destination:            convert2hz/counter_reg[17]/D
                        (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
  Path Group:             sys_clk_pin
  Path Type:              Hold (Min at Fast Process Corner)
  Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
  Data Path Delay:        0.372ns  (logic 0.256ns (68.766%)  route 0.116ns (31.234%))
  Logic Levels:           1  (CARRY4=1)
  Clock Path Skew:        0.000ns (DCD - SCD - CPR)
    Destination Clock Delay (DCD):    1.987ns
    Source Clock Delay      (SCD):    1.473ns
    Clock Pessimism Removal (CPR):    0.514ns

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
                  (clock sys_clk_pin rise edge)
                                       0.000     0.000 r
    W5                                 0.000     0.000 r  clk (IN)
                  net (fo=0)           0.000     0.000    clk
    W5              IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
                  net (fo=1, routed)           0.631     0.858    clk_IBUF
    BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r
clk_IBUF_BUFG_inst/O
                  net (fo=29, routed)          0.590     1.473    convert2hz/clk_IBUF_BUFG
    SLICE_X5Y12         FDRE                                 r  convert2hz/counter_reg[17]/C
  -------------------------------------------------------------------    -------------------
    SLICE_X5Y12         FDRE (Prop_fdre_C_Q)         0.141     1.614 r
convert2hz/counter_reg[17]/Q
                  net (fo=2, routed)           0.116     1.730    convert2hz/counter_reg_n_0_[17]
    SLICE_X5Y12         CARRY4 (Prop_carry4_S[0]_O[0])
                                       0.115     1.845 r  convert2hz/counter0_carry__3/O[0]
                  net (fo=1, routed)           0.000     1.845    convert2hz/data0[17]
    SLICE_X5Y12         FDRE                                 r  convert2hz/counter_reg[17]/D
  -------------------------------------------------------------------    -------------------
```

```
                  (clock sys_clk_pin rise edge)
                                       0.000     0.000 r
  W5                                   0.000     0.000 r  clk (IN)
                  net (fo=0)           0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)        0.414     0.414 r  clk_IBUF_inst/O
                  net (fo=1, routed)           0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)        0.029     1.128 r
clk_IBUF_BUFG_inst/O
                  net (fo=29, routed)          0.860     1.987    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y12         FDRE                                 r  convert2hz/counter_reg[17]/C
                  clock pessimism             -0.514     1.473
  SLICE_X5Y12         FDRE (Hold_fdre_C_D)        0.105     1.578
convert2hz/counter_reg[17]
 -------------------------------------------------------------------
                  required time                         -1.578
                  arrival time                           1.845
 -------------------------------------------------------------------
                  slack                                  0.267

Slack (MET) :             0.267ns  (arrival time - required time)
 Source:                 convert2hz/counter_reg[5]/C
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Destination:            convert2hz/counter_reg[5]/D
                       (rising edge-triggered cell FDRE clocked by sys_clk_pin  {rise@0.000ns
fall@5.000ns period=10.000ns})
 Path Group:             sys_clk_pin
 Path Type:              Hold (Min at Fast Process Corner)
 Requirement:            0.000ns  (sys_clk_pin rise@0.000ns - sys_clk_pin rise@0.000ns)
 Data Path Delay:        0.372ns  (logic 0.256ns (68.766%)  route 0.116ns (31.234%))
 Logic Levels:           1  (CARRY4=1)
 Clock Path Skew:        0.000ns (DCD - SCD - CPR)
   Destination Clock Delay (DCD):    1.990ns
   Source Clock Delay      (SCD):    1.475ns
   Clock Pessimism Removal (CPR):    0.515ns

   Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
 -------------------------------------------------------------------    -------------------
                  (clock sys_clk_pin rise edge)
                                       0.000     0.000 r
  W5                                   0.000     0.000 r  clk (IN)
                  net (fo=0)           0.000     0.000    clk
  W5                IBUF (Prop_ibuf_I_O)        0.226     0.226 r  clk_IBUF_inst/O
```

```
                net (fo=1, routed)           0.631     0.858    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.026     0.884 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          0.592     1.475    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y9          FDRE                                 r  convert2hz/counter_reg[5]/C
 -------------------------------------------------------------------    -------------------
  SLICE_X5Y9          FDRE (Prop_fdre_C_Q)         0.141     1.616 r
convert2hz/counter_reg[5]/Q
                net (fo=2, routed)           0.116     1.732    convert2hz/counter_reg_n_0_[5]
  SLICE_X5Y9          CARRY4 (Prop_carry4_S[0]_O[0])
                                     0.115     1.847 r  convert2hz/counter0_carry__0/O[0]
                net (fo=1, routed)           0.000     1.847    convert2hz/data0[5]
  SLICE_X5Y9          FDRE                                 r  convert2hz/counter_reg[5]/D
 -------------------------------------------------------------------    -------------------

                (clock sys_clk_pin rise edge)
                                     0.000     0.000 r
  W5                                 0.000     0.000 r  clk (IN)
                net (fo=0)                   0.000     0.000    clk
  W5                  IBUF (Prop_ibuf_I_O)         0.414     0.414 r  clk_IBUF_inst/O
                net (fo=1, routed)           0.685     1.099    clk_IBUF
  BUFGCTRL_X0Y0       BUFG (Prop_bufg_I_O)         0.029     1.128 r
clk_IBUF_BUFG_inst/O
                net (fo=29, routed)          0.863     1.990    convert2hz/clk_IBUF_BUFG
  SLICE_X5Y9          FDRE                                 r  convert2hz/counter_reg[5]/C
                clock pessimism             -0.515     1.475
  SLICE_X5Y9          FDRE (Hold_fdre_C_D)         0.105     1.580    convert2hz/counter_reg[5]
 -------------------------------------------------------------------
                required time                         -1.580
                arrival time                           1.847
 -------------------------------------------------------------------
                slack                                  0.267
```

Pulse Width Checks

```
--------------------------------------------------------------------------------
Clock Name:         sys_clk_pin
Waveform(ns):       { 0.000 5.000 }
Period(ns):         10.000
Sources:            { clk }
```

Check Type	Corner	Lib Pin	Reference Pin	Required(ns)	Actual(ns)	Slack(ns)	Location	Pin
Min Period	n/a	BUFG/I	n/a	2.155	10.000	7.845	BUFGCTRL_X0Y0	clk_IBUF_BUFG_inst/I
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X4Y8	convert2hz/counter_reg[0]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y10	convert2hz/counter_reg[10]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y10	convert2hz/counter_reg[11]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y10	convert2hz/counter_reg[12]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y11	convert2hz/counter_reg[13]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y11	convert2hz/counter_reg[14]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y11	convert2hz/counter_reg[15]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y11	convert2hz/counter_reg[16]/C
Min Period	n/a	FDRE/C	n/a	1.000	10.000	9.000	SLICE_X5Y12	convert2hz/counter_reg[17]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X4Y8	convert2hz/counter_reg[0]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y10	convert2hz/counter_reg[10]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y10	convert2hz/counter_reg[11]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y10	convert2hz/counter_reg[12]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y11	convert2hz/counter_reg[13]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y11	convert2hz/counter_reg[14]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y11	convert2hz/counter_reg[15]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y11	convert2hz/counter_reg[16]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y12	convert2hz/counter_reg[17]/C
Low Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y12	convert2hz/counter_reg[18]/C

High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y13	convert2hz/counter_reg[21]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y13	convert2hz/counter_reg[22]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y13	convert2hz/counter_reg[23]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y13	convert2hz/counter_reg[24]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y14	convert2hz/counter_reg[25]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y14	convert2hz/counter_reg[26]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y14	convert2hz/counter_reg[27]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X4Y8	convert2hz/counter_reg[0]/C
High Pulse Width	Slow	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y10	convert2hz/counter_reg[10]/C
High Pulse Width	Fast	FDRE/C	n/a	0.500	5.000	4.500	SLICE_X5Y10	convert2hz/counter_reg[10]/C