```
#-----------------------------------------------------------
# Vivado v2016.2 (64-bit)
# SW Build 1577090 on Thu Jun  2 16:32:40 MDT 2016
# IP Build 1577682 on Fri Jun  3 12:00:54 MDT 2016
# Start of session at: Thu Feb 16 20:33:51 2017
# Process ID: 2704
# Current directory: C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.runs/synth_1
# Command line: vivado.exe -log lab3top.vds -mode batch -messageDb vivado.pb -notrace
-source lab3top.tcl
# Log file: C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.runs/synth_1/lab3top.vds
# Journal file: C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source lab3top.tcl -notrace
Command: synth_design -top lab3top -part xc7a35tcpg236-1
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35t'
INFO: Launching helper process for spawning children vivado processes
INFO: Helper process launched with PID 2880
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:05 ; elapsed = 00:00:07 . Memory (MB): peak =
272.941 ; gain = 66.633
---------------------------------------------------------------------------------
INFO: [Synth 8-638] synthesizing module 'lab3top' [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:1]
INFO: [Synth 8-638] synthesizing module 'clk_to_2hz' [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:12]
INFO: [Synth 8-256] done synthesizing module 'clk_to_2hz' (1#1) [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:12]
INFO: [Synth 8-638] synthesizing module 'clk_to_1hz' [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:35]
INFO: [Synth 8-256] done synthesizing module 'clk_to_1hz' (2#1) [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:35]
INFO: [Synth 8-638] synthesizing module 'traffic_light' [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/imports/examples/traffic_light.v:2]
CRITICAL WARNING: [Synth 8-5413] Mix of synchronous and asynchronous control for register
state_reg in module traffic_light. [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/imports/examples/traffic_light.v:193]
INFO: [Synth 8-256] done synthesizing module 'traffic_light' (3#1) [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/imports/examples/traffic_light.v:2]
INFO: [Synth 8-256] done synthesizing module 'lab3top' (4#1) [C:/Users/Akilan
Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/sources_1/new/lab3top.v:1]
---------------------------------------------------------------------------------
```

Finished RTL Elaboration : Time (s): cpu = 00:00:06 ; elapsed = 00:00:08 . Memory (MB): peak = 309.438 ; gain = 103.129

Report Check Netlist:
```
+------+-----------------+-------+---------+-------+-----------------+
|      |Item             |Errors |Warnings |Status |Description      |
+------+-----------------+-------+---------+-------+-----------------+
|1     |multi_driven_nets|      0|        0|Passed |Multi driven nets|
+------+-----------------+-------+---------+-------+-----------------+
```

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:06 ; elapsed = 00:00:08 . Memory (MB): peak = 309.438 ; gain = 103.129

INFO: [Device 21-403] Loading part xc7a35tcpg236-1
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/constrs_1/imports/Downloads/Basys3_Master.xdc]
Finished Parsing XDC File [C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/constrs_1/imports/Downloads/Basys3_Master.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/Akilan Pughazhendi/Desktop/EE460M/lab3/lab3.srcs/constrs_1/imports/Downloads/Basys3_Master.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/lab3top_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in [.Xil/lab3top_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.
Completed Processing XDC Constraints

INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.017 . Memory (MB): peak = 590.426 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:15 ; elapsed = 00:00:21 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Loading Part and Timing Information

Loading part: xc7a35tcpg236-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:15 ; elapsed = 00:00:21 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:21 . Memory (MB): peak = 590.426 ; gain = 384.117

INFO: [Synth 8-5545] ROM "slowClk" won't be mapped to RAM because address size (28) is larger than maximum supported(25)
INFO: [Synth 8-5544] ROM "slowClk" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
INFO: [Synth 8-802] inferred FSM for state register 'state_reg' in module 'traffic_light'
INFO: [Synth 8-5544] ROM "Gw" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "Yb" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "Gb" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "Ya" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "Ga" won't be mapped to Block RAM because address size (4) smaller than threshold (5)
INFO: [Synth 8-5544] ROM "nextstate" won't be mapped to Block RAM because address size (4) smaller than threshold (5)

State	New Encoding	Previous Encoding
iSTATE12	0000	1101
iSTATE	0001	0000
iSTATE0	0010	0001
iSTATE1	0011	0010
iSTATE2	0100	0011
iSTATE3	0101	0100
iSTATE4	0110	0101

```
              iSTATE5 |                0111 |                0110
              iSTATE6 |                1000 |                0111
              iSTATE7 |                1001 |                1000
              iSTATE8 |                1010 |                1001
              iSTATE9 |                1011 |                1010
             iSTATE10 |                1100 |                1011
             iSTATE11 |                1101 |                1100
---------------------------------------------------------------------------------------------
INFO: [Synth 8-3354] encoded FSM with state register 'state_reg' using encoding 'sequential' in
module 'traffic_light'
---------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory
(MB): peak = 590.426 ; gain = 384.117
---------------------------------------------------------------------------

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
---------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
            2 Input     28 Bit       Adders := 1
            2 Input      2 Bit       Adders := 1
+---Registers :
                       28 Bit    Registers := 1
                        2 Bit    Registers := 1
                        1 Bit    Registers := 3
+---Muxes :
            2 Input     28 Bit        Muxes := 1
           15 Input      4 Bit        Muxes := 1
            2 Input      2 Bit        Muxes := 1
            2 Input      1 Bit        Muxes := 2
           14 Input      1 Bit        Muxes := 8
---------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------
---------------------------------------------------------------------------
Start RTL Hierarchical Component Statistics
---------------------------------------------------------------------------
```

Hierarchical RTL Component report
Module clk_to_2hz
Detailed RTL Component Info :
+---Adders :
	2 Input 28 Bit Adders := 1
+---Registers :
	28 Bit Registers := 1
	1 Bit Registers := 1
+---Muxes :
	2 Input 28 Bit Muxes := 1
	2 Input 1 Bit Muxes := 1
Module clk_to_1hz
Detailed RTL Component Info :
+---Adders :
	2 Input 2 Bit Adders := 1
+---Registers :
	2 Bit Registers := 1
	1 Bit Registers := 1
+---Muxes :
	2 Input 2 Bit Muxes := 1
	2 Input 1 Bit Muxes := 1
Module traffic_light
Detailed RTL Component Info :
+---Registers :
	1 Bit Registers := 1
+---Muxes :
	15 Input 4 Bit Muxes := 1
	14 Input 1 Bit Muxes := 8

Finished RTL Hierarchical Component Statistics

Start Part Resource Summary

Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)

Finished Part Resource Summary

Start Parallel Synthesis Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Cross Boundary Optimization

INFO: [Synth 8-5545] ROM "convert2hz/slowClk" won't be mapped to RAM because address size (28) is larger than maximum supported(25)

Finished Cross Boundary Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 384.117

Finished Parallel Reinference : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 384.117

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start Area Optimization

Finished Area Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 384.117

Finished Parallel Area Optimization : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 384.117

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

Start Timing Optimization

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:27 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Finished Timing Optimization : Time (s): cpu = 00:00:27 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:27 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Finished Parallel Technology Mapping Optimization : Time (s): cpu = 00:00:27 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Report RTL Partitions:
+-+--------------+------------+----------+
| |RTL Partition |Replication |Instances |
+-+--------------+------------+----------+
+-+--------------+------------+----------+
Finished Parallel Synthesis Optimization : Time (s): cpu = 00:00:27 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Report Check Netlist:
+------+-----------------+-------+---------+-------+-----------------+
| |Item |Errors |Warnings |Status |Description |
+------+-----------------+-------+---------+-------+-----------------+
|1 |multi_driven_nets | 0| 0|Passed |Multi driven nets |
+------+-----------------+-------+---------+-------+-----------------+

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Report RTL Partitions:
+-+-------------+-----------+----------+
| |RTL Partition |Replication |Instances |
+-+-------------+-----------+----------+
+-+-------------+-----------+----------+

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:28 ; elapsed = 00:00:34 . Memory (MB): peak = 590.426 ; gain = 384.117

Start Writing Synthesis Report

Report BlackBoxes:

	BlackBox name	Instances

Report Cell Usage:

	Cell	Count
1	BUFG	1
2	CARRY4	7
3	LUT1	29
4	LUT2	2
5	LUT3	4
6	LUT4	8
7	LUT5	4
8	LUT6	6
9	FDCE	4
10	FDPE	1
11	FDRE	32
12	IBUF	2
13	OBUF	8

Report Instance Areas:

	Instance	Module	Cells
1	top		108
2	convert1hz	clk_to_1hz	6

```
|3     |  convert2hz |clk_to_2hz    |    73|
|4     |  light      |traffic_light |    18|
+------+-------------+--------------+------+
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:28 ; elapsed = 00:00:35 . Memory (MB): peak = 590.426 ; gain = 384.117

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:16 ; elapsed = 00:00:22 . Memory (MB): peak = 590.426 ; gain = 103.129
Synthesis Optimization Complete : Time (s): cpu = 00:00:28 ; elapsed = 00:00:35 . Memory (MB): peak = 590.426 ; gain = 384.117
INFO: [Project 1-571] Translating synthesized netlist
INFO: [Netlist 29-17] Analyzing 9 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
31 Infos, 0 Warnings, 1 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:27 ; elapsed = 00:00:33 . Memory (MB): peak = 590.426 ; gain = 384.117
report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.036 . Memory (MB): peak = 590.426 ; gain = 0.000
INFO: [Common 17-206] Exiting Vivado at Thu Feb 16 20:34:28 2017...