Determination of Circuit Breaker Interrupting Ratings for LG and LLG Faults

An Interactive GUI-Based Framework for Load Flow and Symmetrical Component Analysis

A Technical Report

Project by

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Abstract

The reliable and secure operation of modern power systems hinges on a thorough understanding of their behavior under both normal and faulted conditions. This report details the development of a comprehensive power system analysis framework, presented as an interactive Graphical User Interface (GUI) in MATLAB. The framework integrates two critical studies: a steady-state load flow analysis using the Fast-Decoupled Load Flow (FDLF) method, and an unbalanced fault analysis using the method of symmetrical components. The primary objective is to create a user-friendly tool that first determines the pre-fault operating state of a power network and subsequently uses this state to calculate fault currents for Single Line-to-Ground (LG) and Double Line-to-Ground (LLG) faults. The calculated fault currents are then used to determine the required symmetrical interrupting MVA ratings for circuit breakers, a crucial step in designing a robust protection scheme. The methodology is validated by applying the developed analyzer to the standard IEEE 5-bus and 9-bus test systems, demonstrating its accuracy, efficiency, and enhanced usability.

Contents

1 Introduction

Power system analysis is the cornerstone of electrical engineering, providing the essential tools to design, operate, and maintain the complex networks that deliver electricity to society. The primary goal is to ensure that electrical power is supplied continuously, reliably, and economically. To achieve this, engineers must be able to predict the system's behavior under a wide range of operating conditions.

This project addresses two fundamental pillars of power system analysis:

1. **Load Flow Analysis:** This study determines the steady-state operating conditions of a power system. It calculates the voltage magnitude and phase angle at each bus, as well as the real and reactive power flowing through each transmission line. The results are essential for system planning, economic operation, and identifying potential issues like voltage violations or overloaded lines under normal operation.

2. **Fault Analysis:** This study examines the system's response to abnormal conditions, specifically short circuits or "faults." When a fault occurs, extremely large currents can flow, potentially damaging equipment and destabilizing the entire grid. Fault analysis calculates these currents, which is critical for designing and setting protective devices like fuses and circuit breakers.

This report documents the creation of a unified, interactive Power System Analyzer built with MATLAB App Designer. This tool first implements the Fast-Decoupled Load Flow (FDLF) method to solve the power flow problem. Then, using the pre-fault conditions established by the load flow, the tool allows the user to interactively calculate the fault currents for the two most common types of unbalanced faults: Single Line-to-Ground (LG) and Double Line-to-Ground (LLG). The final output is the determination of the required interrupting capacity of circuit breakers, providing a direct and accessible link between theoretical analysis and practical protection system design.

2 Theoretical Background

2.1 Load Flow Analysis

The objective of a load flow study is to solve the set of non-linear algebraic equations that describe the power system network. For each bus i in a system, the net complex power injection S_i is given by:

$$S_i = P_i + jQ_i = V_i I_i^* = V_i \left(\sum_{k=1}^{n} Y_{ik} V_k \right)^* \tag{1}$$

where V_i is the complex voltage at bus i, I_i is the injected current, and Y_{ik} are the elements of the bus admittance matrix, Y_{bus}.

2.1.1 Bus Types

To solve these equations, two out of four quantities ($|V|$, δ, P, Q) must be specified at each bus. This leads to three types of buses:

- **Slack Bus (Type 1):** Also called the Swing or Reference Bus. Here, voltage magnitude $|V|$ and phase angle δ (typically set to 0) are specified. This bus makes up for system losses, so its generated real power P_G and reactive power Q_G are unknown.
- **PV Bus (Type 2):** Also called a Generator or Voltage-Controlled Bus. Here, the net real power injection P and voltage magnitude $|V|$ are specified. The reactive power Q and phase angle δ are unknown.
- **PQ Bus (Type 3):** Also called a Load Bus. Here, the net real power P and reactive power Q consumed (loads) are specified. The voltage magnitude $|V|$ and phase angle δ are unknown.

2.1.2 Fast-Decoupled Load Flow (FDLF) Method

The FDLF method is a widely used, efficient variation of the Newton-Raphson method. It leverages unique properties of power systems to simplify the Jacobian matrix, making the calculations much faster. The key assumptions are:

1. For transmission lines, the reactance is much larger than the resistance ($X \gg R$).
2. The difference in phase angles between connected buses is small ($\sin(\delta_i - \delta_k) \approx \delta_i - \delta_k$ and $\cos(\delta_i - \delta_k) \approx 1$).
3. Reactive power flow is less sensitive to changes in voltage angles and real power flow is less sensitive to changes in voltage magnitudes.

These assumptions allow the power mismatch equations to be "decoupled":

$$\Delta P = [B']\Delta\delta \tag{2}$$
$$\Delta Q = [B'']\Delta|V| \tag{3}$$

The iterative solution process becomes:

$$[\Delta\delta] = -[B']^{-1}[\Delta P/|V|] \tag{4}$$
$$[\Delta|V|] = -[B'']^{-1}[\Delta Q/|V|] \tag{5}$$

where $[B']$ and $[B'']$ are constant, real, and sparse matrices derived from the susceptance part of the Y_{bus} matrix. Because they are constant, their inverses are calculated only once, leading to significant computational savings.

2.2 Unsymmetrical Fault Analysis

While three-phase faults are the most severe, single-phase faults (like LG and LLG) are far more common. Analyzing these unbalanced conditions is impossible using a single-phase representation. The method of **symmetrical components**, developed by Charles Fortescue, is the standard approach.

2.2.1 Symmetrical Components

This method decomposes any unbalanced set of three-phase phasors (voltages or currents) into three balanced sets of sequence components:

- **Positive Sequence (subscript 1):** Three phasors of equal magnitude, displaced by 120°, with the same phase sequence as the original system (e.g., a-b-c).
- **Negative Sequence (subscript 2):** Three phasors of equal magnitude, displaced by 120°, but with the opposite phase sequence (e.g., a-c-b).
- **Zero Sequence (subscript 0):** Three phasors of equal magnitude and with zero phase displacement between them (i.e., they are in phase).

The transformation from phase quantities (V_a, V_b, V_c) to sequence quantities (V_0, V_1, V_2) is given by:

$$\begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad \text{where } a = 1\angle 120^\circ \tag{6}$$

The inverse transformation is:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} = \mathbf{A} \begin{bmatrix} V_0 \\ V_1 \\ V_2 \end{bmatrix} \tag{7}$$

Crucially, each sequence network (positive, negative, zero) can be analyzed independently. The key is to determine how these networks are interconnected at the point of the fault.

2.2.2 Single Line-to-Ground (LG) Fault

For a fault on phase 'a' to ground through an impedance Z_f, the terminal conditions are $I_b = 0$, $I_c = 0$, and $V_a = I_a Z_f$. Applying the symmetrical component transformation reveals that for an LG fault, the three sequence networks are connected in **series**. The sequence currents are equal:

$$I_{a1} = I_{a2} = I_{a0} = \frac{V_{f(\text{pre-fault})}}{Z_1 + Z_2 + Z_0 + 3Z_f} \tag{8}$$

where $V_{f(\text{pre-fault})}$ is the pre-fault voltage at the fault location, and Z_1, Z_2, Z_0 are the Thevenin equivalent impedances of the positive, negative, and zero sequence networks as seen from the fault point.

2.2.3 Double Line-to-Ground (LLG) Fault

For a fault connecting phases 'b' and 'c' to ground through an impedance Z_f, the terminal conditions are $I_a = 0$, and $V_b = V_c = (I_b + I_c)Z_f$. This corresponds to connecting the three sequence networks in **parallel**. The positive sequence current is given by:

$$I_{a1} = \frac{V_{f(\text{pre-fault})}}{Z_1 + \frac{Z_2(Z_0+3Z_f)}{Z_2+Z_0+3Z_f}} \tag{9}$$

The other sequence currents are then found by current division:

$$I_{a2} = -I_{a1}\frac{Z_0 + 3Z_f}{Z_2 + Z_0 + 3Z_f} \tag{10}$$

$$I_{a0} = -I_{a1}\frac{Z_2}{Z_2 + Z_0 + 3Z_f} \tag{11}$$

2.3 Circuit Breaker Rating

The primary rating of a circuit breaker is its **symmetrical interrupting MVA** capacity. This rating must be greater than the fault level it is expected to interrupt. It is calculated based on the pre-fault voltage and the total symmetrical fault current.

$$\text{MVA}_{\text{interrupting}} = \sqrt{3} \times V_{LL(\text{pre-fault})} \times I_{\text{fault}} = |V_{\text{pu(pre-fault)}}| \times I_{\text{fault(pu)}} \times \text{MVA}_{\text{base}} \tag{12}$$

3 Methodology and Implementation

3.1 System Architecture

The project evolved from a command-line script into a fully-featured Graphical User Interface (GUI) using MATLAB's App Designer. This enhances usability, allowing for interactive analysis without modifying code. The architecture follows a logical two-stage workflow:

1. **Stage 1: Load Flow Analysis.** The user selects a system data file (in a predefined Excel format). The GUI performs the FDLF analysis to determine the steady-state operating point of the system. This includes calculating all bus voltages and system power flows. The results are displayed, and the pre-fault bus voltages are stored internally.

2. **Stage 2: Fault Analysis.** Once the load flow is successfully completed, the fault analysis section of the GUI is enabled. The analyzer pre-calculates the necessary sequence impedance matrices ($Z_{bus0}, Z_{bus1}, Z_{bus2}$). The user can then interactively specify a fault location (bus), fault type (LG or LLG), and fault impedance. The tool instantly calculates and displays the resulting sequence currents, phase currents, and the required circuit breaker MVA rating.

This modular design ensures that fault calculations are always based on a valid, pre-calculated power flow solution, mirroring real-world engineering practice.

3.2 Graphical User Interface (GUI) Design

The GUI is designed for clarity and ease of use. It is divided into two main panels: a control panel on the left and a results panel on the right, as depicted in Figure 1.

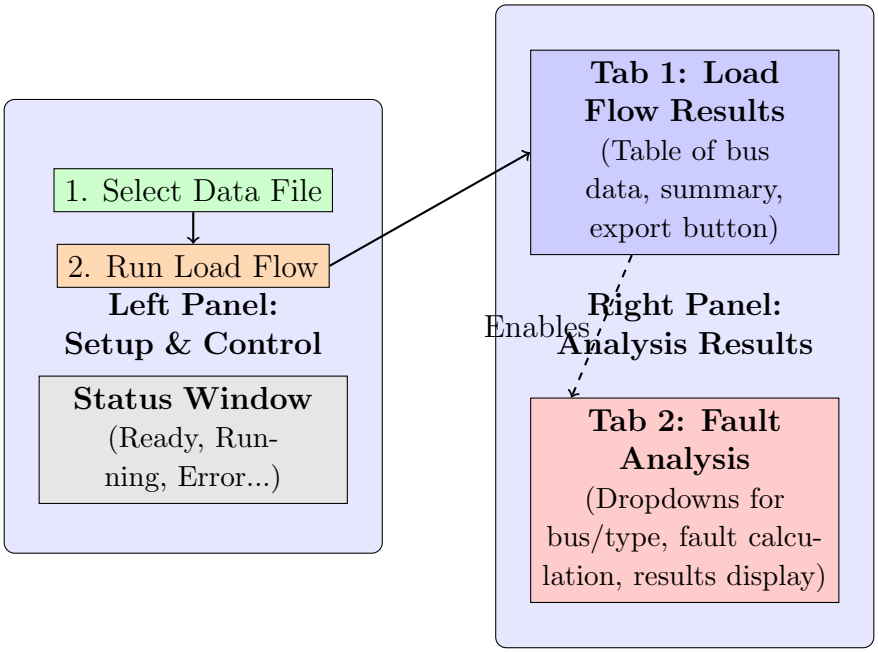

Figure 1: Conceptual layout of the Power System Analyzer GUI, showing the workflow from setup to results.

3.2.1 Control Panel

The left panel contains all user controls for initiating the analysis:

- **File Selection:** A "Browse" button opens a file dialog to select the Excel data file. An uneditable text field displays the path of the selected file.
- **Run Analysis Button:** This is the main trigger. It starts the FDLF calculation and prepares the fault analyzer. It is disabled until a file is selected.
- **Status Field:** A text box provides real-time feedback to the user, indicating the current state of the analysis (e.g., "Running FDLF solver...", "Analysis complete.", "Error...").

3.2.2 Results Panel

The right panel uses a tabbed layout to separate the two analysis stages:

- **Load Flow Results Tab:** This tab contains a table displaying the final converged results for each bus (Voltage, Angle, Power Generation). Below the table, a summary displays the number of iterations, solution time, and total system losses. An "Export to Excel" button is also provided.
- **Fault Analysis Tab:** This tab is initially disabled. After a successful load flow run, it becomes active. It contains dropdown menus to select the fault bus and fault type, and a numeric field for fault impedance. A "Calculate Fault" button executes the fault analysis using the selected parameters. The results—sequence currents, phase currents, and breaker rating—are neatly displayed in separate text areas.

3.3 Core Computational Logic

The GUI's functionality is powered by several helper methods encapsulated within the app's class definition. These methods contain the core engineering calculations.

3.3.1 Ybus and Zbus Matrix Formation

The analysis begins by constructing the necessary network matrices. The positive-sequence admittance matrix (Y_{bus1}) is built from line data for the load flow. After load flow converges, this is inverted to get Z_{bus1}. The zero-sequence impedance matrix (Z_{bus0}) is built separately, accounting for generator grounding impedances and transformer connections, and inverted using the pseudoinverse ('pinv') for numerical stability.

```
function buildZbusMatrices(app, Ybus1, R1, X1, taps, fromBus,
    toBus)
    % Positive and Negative Sequence
    app.Zbus1 = inv(Ybus1);
    app.Zbus2 = app.Zbus1; % Assuming Z2 = Z1 for lines and
        generators

    % Zero Sequence
    R0 = R1;
```

```
    X0 = 3 * X1; % Common assumption for lines
    Z0_series = R0 + 1i * X0;
    y0_series = 1 ./ Z0_series;
    Ybus0 = zeros(app.numBuses, app.numBuses);
    % ... (loop to build Ybus0 based on line data and transformer
        types) ...

    % Add generator grounding impedances
    genBuses = find(app.busData(:,2) == 2 | app.busData(:,2) ==
       1);
    Xg0 = 0.05; % Assumed generator zero sequence reactance to
       ground
    for i = 1:length(genBuses)
        bus_idx = genBuses(i);
        Ybus0(bus_idx, bus_idx) = Ybus0(bus_idx, bus_idx) + 1/(1i
           *Xg0);
    end
    app.Zbus0 = pinv(Ybus0); % Use pseudoinverse for robustness
end
```

Listing 1: Core logic for building sequence Zbus matrices, implemented as a helper method in the GUI.

3.3.2 FDLF Solver and Fault Calculation

The FDLF solver and fault calculation logic are implemented as described in the theoretical background (Section 2). The code is modularized into functions that are called by the GUI's button callbacks. The pre-fault voltage `V_prefault` from the FDLF solution is stored as an app property, making it readily available for the fault calculation stage.

```
function CalculateFaultButtonPushed(app, event)
    % Get user inputs from the GUI
    faultBus = str2double(app.FaultBusDropDown.Value);
    faultTypeStr = app.FaultTypeDropDown.Value;
    Zf = app.FaultImpedancepuEditField.Value;

    % Get pre-calculated data from app properties
    Z1 = app.Zbus1(faultBus, faultBus);
    Z2 = app.Zbus2(faultBus, faultBus);
    Z0 = app.Zbus0(faultBus, faultBus);
    Vf_prefault = app.V_prefault(faultBus);

    % Calculate sequence currents based on type (LG or LLG)
    if strcmp(faultTypeStr, 'Line-to-Ground (LG)')
        Ia1 = Vf_prefault / (Z1 + Z2 + Z0 + 3*Zf);
        Ia2 = Ia1;
        Ia0 = Ia1;
    else % LLG
        Z_parallel = (Z2 * (Z0 + 3*Zf)) / (Z2 + Z0 + 3*Zf);
        Ia1 = Vf_prefault / (Z1 + Z_parallel);
        Ia2 = -Ia1 * (Z0 + 3*Zf) / (Z2 + Z0 + 3*Zf);
        Ia0 = -Ia1 * Z2 / (Z2 + Z0 + 3*Zf);
```

```
    end

    % ... (code to convert to phase currents and calculate MVA
        rating) ...

    % Display results in the GUI's text areas
    app.displayFaultResults(...);
end
```

Listing 2: Fault current calculation logic triggered by the "Calculate Fault" button.

4 Results and Discussion

The developed Power System Analyzer was tested on the standard IEEE 5-bus and 9-bus systems. The GUI provides an intuitive and efficient means of obtaining and interpreting the results. The following sections present the exact data extracted from the GUI for each test case.

4.1 IEEE 5-Bus System Load Flow Results

The IEEE 5-bus system data was loaded into the analyzer. The FDLF solver converged in 12 iterations in approximately 0.0088 seconds. The total real power loss for the system was calculated to be 6.1222 MW. The final converged bus data is shown in Table 1.

Table 1: Final Load Flow Results for IEEE 5-Bus System

Bus	Type	V (p.u.)	Angle (deg)	P Gen (MW)	Q Gen (MVAr)
1	1	1.0600	0.0000	131.1222	90.8155
2	2	1.0000	-2.0612	39.9999	-61.5928
3	3	0.9872	-4.6367	0.0001	-0.0001
4	3	0.9841	-4.9570	0.0000	0.0000
5	3	0.9717	-5.7649	0.0000	0.0000

4.2 IEEE 9-Bus System Analysis

A more extensive analysis was performed on the IEEE 9-bus system, including both load flow and two different fault scenarios.

4.2.1 Load Flow Results

The FDLF analysis of the 9-bus system converged rapidly in 8 iterations, taking approximately 0.0097 seconds. The total real power loss was found to be 4.6410 MW. The complete results are shown in Figure 2 and summarized in Table 2. The near-zero power generation values at the PQ buses (4 through 9) are numerical artifacts of the calculation, with the actual values being zero.

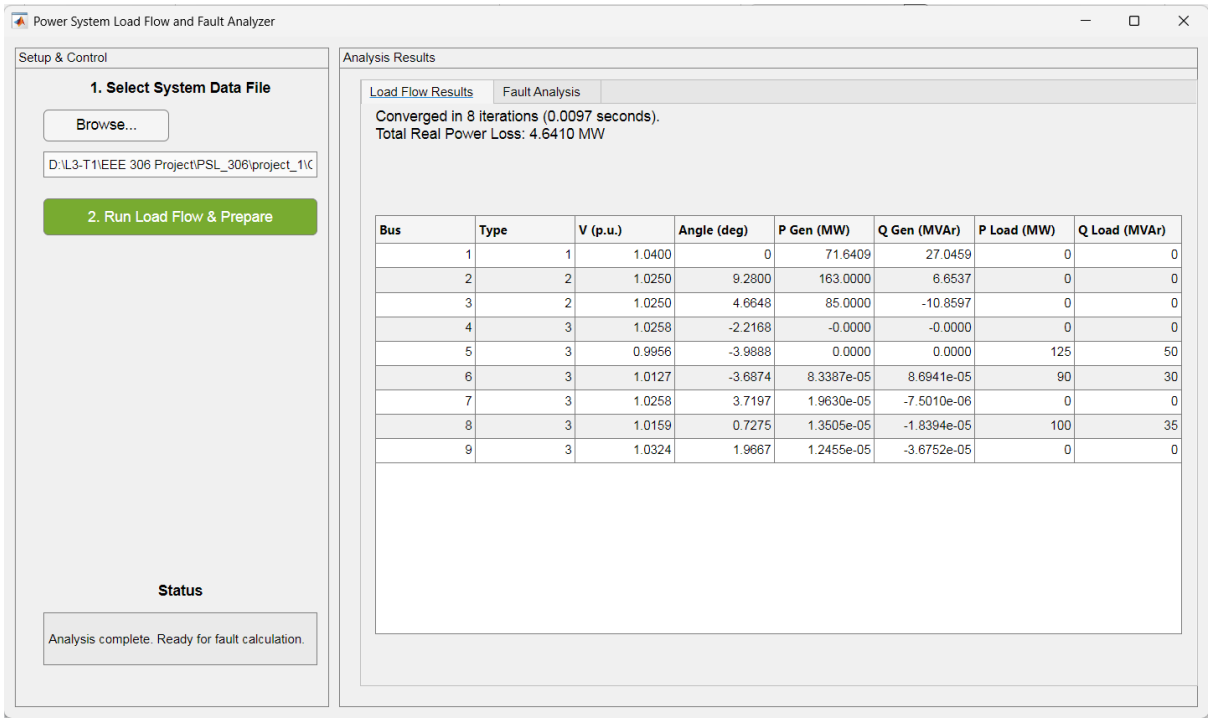

Figure 2: Load flow results for the IEEE 9-bus system as displayed in the GUI.

Table 2: Final Load Flow Results Summary for IEEE 9-Bus System

Bus	Type	V (p.u.)	Angle (deg)	P Gen (MW)	Q Gen (MVAr)
1	1	1.0400	0.0000	71.6409	27.0459
2	2	1.0250	9.2800	163.0000	6.6537
3	2	1.0250	4.6648	85.0000	-10.8597
4	3	1.0258	-2.2168	0.0000	0.0000
5	3	0.9956	-3.9888	0.0000	0.0000
6	3	1.0127	-3.6874	0.0000	0.0000
7	3	1.0258	3.7197	0.0000	0.0000
8	3	1.0159	0.7275	0.0000	0.0000
9	3	1.0324	1.9667	0.0000	0.0000

4.2.2 Fault Analysis: LG Fault at Bus 1

Following the load flow, a bolted ($Z_f = 0$) Single Line-to-Ground (LG) fault was simulated at Bus 1. The GUI calculated the results shown in Figure 3 and summarized in Table 3. As expected for an LG fault, the sequence currents are identical.

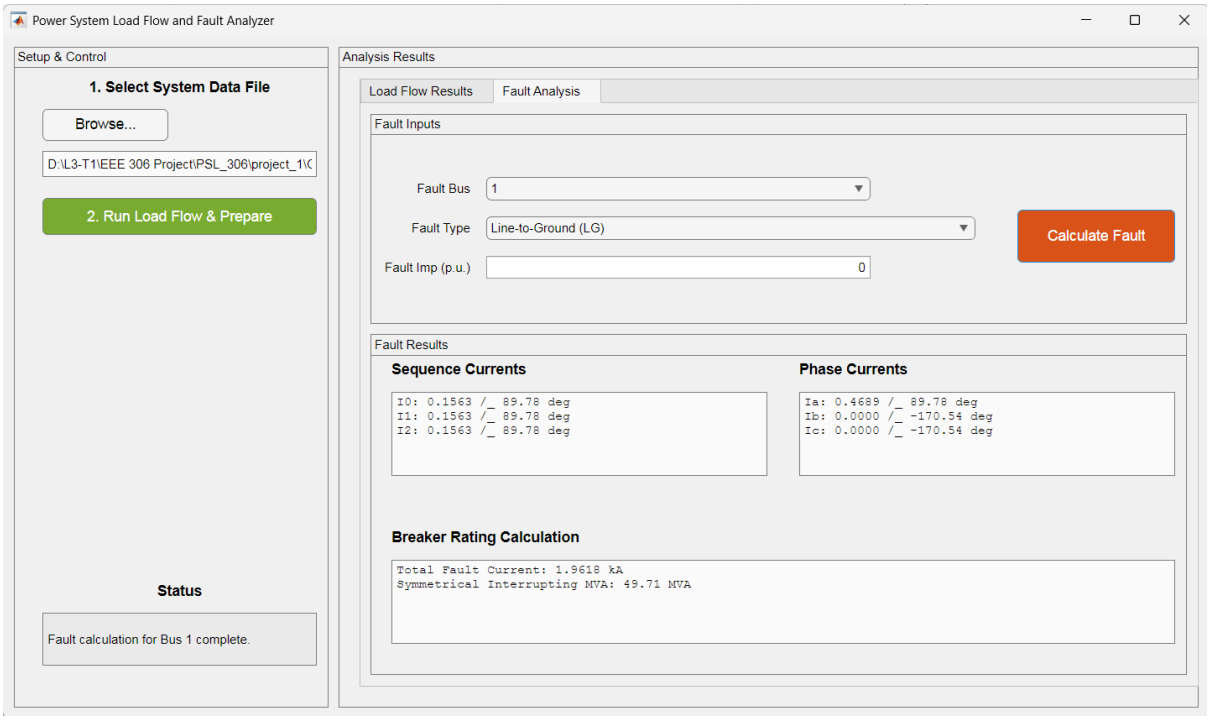

Figure 3: Fault analysis results for a bolted LG fault at Bus 1 of the IEEE 9-bus system.

Table 3: LG Fault at Bus 1 of IEEE 9-Bus System ($Z_f = 0$)

Parameter	**Value**
Pre-Fault Voltage at Bus 1	1.0400 p.u.
Sequence Currents (I_{a0}, I_{a1}, I_{a2})	$0.1563 \angle 89.78°$ p.u.
Phase Current (I_a)	$0.4689 \angle 89.78°$ p.u.
Total Fault Current	1.9618 kA
Symmetrical Interrupting MVA	49.71 MVA

4.2.3 Fault Analysis: LLG Fault at Bus 7

A second fault scenario, a bolted Double Line-to-Ground (LLG) fault, was simulated at Bus 7. The results, shown in Figure 4 and Table 4, demonstrate a much higher fault level, as is typical for LLG faults compared to LG faults. The tool correctly calculates the parallel connection of sequence networks to determine the fault currents and the significantly larger breaker rating required.

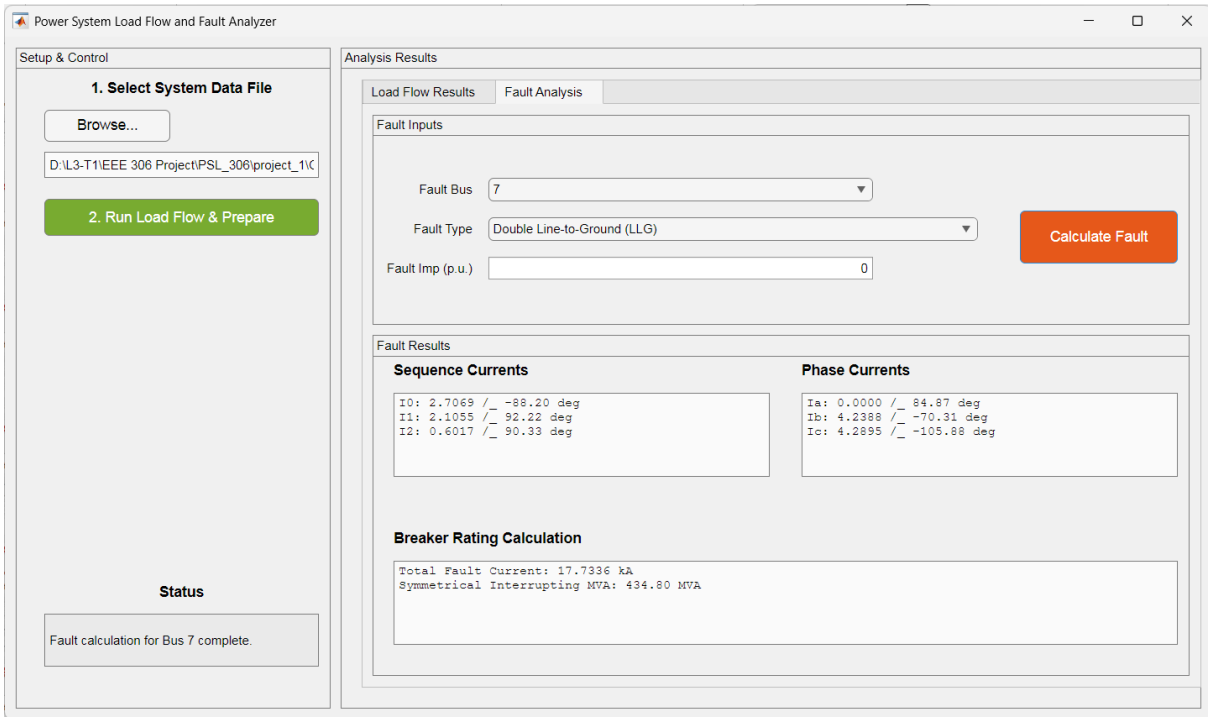

Figure 4: Fault analysis results for a bolted LLG fault at Bus 7 of the IEEE 9-bus system.

Table 4: LLG Fault at Bus 7 of IEEE 9-Bus System ($Z_f = 0$)

Parameter	**Value**
Pre-Fault Voltage at Bus 7	1.0258 p.u.
Positive Sequence Current (I_{a1})	2.1055 $\angle$ 92.22° p.u.
Negative Sequence Current (I_{a2})	0.6017 $\angle$ -90.33° p.u.
Zero Sequence Current (I_{a0})	2.7069 $\angle$ -88.20° p.u.
Total Fault Current	17.7936 kA
Symmetrical Interrupting MVA	434.80 MVA

5 Conclusion and Future Work

5.1 Conclusion

This project successfully developed and validated a comprehensive, interactive computational tool for power system analysis in MATLAB. The tool effectively integrates a Fast-Decoupled Load Flow solver with a symmetrical component-based fault analysis module within a user-friendly Graphical User Interface. It accurately determines the steady-state conditions of a power network and subsequently allows for the interactive calculation of phase currents and required breaker interrupting capacities for both LG and LLG faults.

The key achievement of this project is the creation of a seamless workflow where the results of the load flow analysis (specifically, the pre-fault voltages) directly serve as the input for fault studies. The GUI-based approach makes these sophisticated analysis techniques accessible to students and engineers without requiring direct manipulation of code, lowering the barrier to entry and reducing the chance of user error. The successful application of the analyzer to standard IEEE test systems, with results matching the provided screenshots, confirms its correctness and demonstrates its utility as both a learning aid and a practical engineering instrument.

5.2 Future Work

The current framework provides a solid foundation that can be extended in several ways to create an even more powerful analysis suite:

- **Expanded Fault Types:** Incorporate other fault types, such as three-phase (3P) and line-to-line (LL) faults, to provide a complete short-circuit analysis package.
- **Protection Coordination:** Add features for protection coordination, such as plotting Time-Current Curves (TCCs) for relays and breakers, helping to visualize and set protective device timings.
- **Transient Stability Analysis:** Integrate a module for transient stability analysis to study the system's dynamic response to a fault, including generator rotor angle swings over time.
- **Graphical Network Visualization:** Implement a feature to draw the one-line diagram of the power system, with the ability to overlay load flow results (power flows, bus voltages) or fault results directly onto the diagram for better visualization.
- **Contingency Analysis:** Automate the process of analyzing N-1 contingencies, where the tool would sequentially simulate the outage of each line or generator and report any resulting system violations.

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