ECE 586
COMPUTER ARCHITECTURE

MIPS-LITE 5-STAGE PIPELINE SIMULATOR

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1. Instruction types: Arithmetic, Logical, Memory Access, Control Transfer

   The breakdown of instruction frequencies for these instruction types is listed below:

Total Number of instructions	638
Number of Arithmetic instructions	333
Number of Logical instructions	50
Number of Memory Access instructions	103
Number of Control Transfer instructions	152

2. Final states of program counter and general-purpose registers are listed below:

   Final state of program counter = 100

   Final states of register files are listed below:

General Purpose Register	**Final State**
R1	1200
R2	1400
R3	100
R4	50
R5	50
R6	0
R7	25
R8	2550
R9	1275
R10	50
R11	50
R12	32

   From the above table it is shown that the states of all the register files are changed.

States of Final memory instructions:

Address: 1400, Contents: 25

Address: 1404, Contents: 2550

Address: 1408, Contents: 1275

3. Stall conditions in both the no forwarding & forwarding cases:

(i) Forwarding-Case:

(1). If the dependent instruction follows right after the producer instruction, then there won't be any stalls. Hence stall penalty is 0.

(2). If the dependent instruction follows right after the producer instruction and if the producer instruction is a LOAD instruction, then the stall penalty is 1.

(3). If the instruction is branch and is taken or if the instruction jump register is executed, then the stall penalty is 2.

(ii) Non-Forwarding Case:

(1). If the dependent instruction follows right after the producer instruction, then the stall penalty is 2 cycles.

(2) If the producer and dependent instructions are separated by an intermediate instruction, then the stall penalty is 1 cycle.

(3). If two instructions are present in between producer and dependent instruction and there is no dependency between those two instructions, then the stall penalty is 0.

(4). If the instruction is branch and is taken or if the instruction jump register is executed, then the stall penalty is 2.

4. No forwarding:

The total number of data hazards and the average stall penalty per hazard:

The total number of Data Hazards: 151

Single stalls: 1

Double stalls: 150

The total number of stalls: 301

Average stall penalty per hazard = Total number of stalls/Total number of data hazards

= 301/151 = 1.9933774834437086

5. Forwarding:

The number of data hazards which could not be fully eliminated by forwarding

The total number of stalls: 50

6. Execution time in terms of number of clock cycles for the **no forwarding** and the **forwarding** scenarios:

The number of clock cycles for no forwarding: 1095

The number of clock cycles for forwarding: 844

7. Speedup achieved by **forwarding** as compared to **no forwarding**:

Speedup achieved = (Execution time) no-forwarding / (Execution time) forwarding

Speedup = 1095/844 = 1. 29739336492891