Design and development of VDE-SAT compliant payloads for small satellite platforms

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***Abstract*— The VHF Data Exchange System (VDES) is an innovative system for two-way digital communication for maritime use, which foresees both terrestrial and satellite components, enabling ship-to-ship and ship-to-shore communication close to shore and in open water. This paper presents the performance results and the key features of a VDES half-duplex Radio Frequency (RF) Front-End (FE) subsystem for Low Earth Orbit (LEO) small satellite platforms (such as CubeSats or microsatellites) with dedicated transmitting (TX) and receiving (RX) stages, named VOCS Payload. The VOCS Payload has TX and RX capabilities, designed to manage the overall VDES frequency range, and allows the management of VDE-Satellite (VDE-SAT) Link IDs, as well as standard Automatic Identification System (AIS) and Application Specific Messages (ASM) messages, as defined by the last latest VDES technical recommendation by the International Telecommunication Union (ITU), [1].**

Keywords—VDES, VHF, LEO, CubeSat, Payload

I. INTRODUCTION

In recent years, a collaborative effort led by the International Association of Marine Aids to Navigation and Lighthouse Authorities (IALA), along with several players in the maritime industry, has played a crucial role in standardising the VDES standard [2]. This system encompasses the AIS, ASM and VDE systems. The primary aim is to alleviate congestion on the AIS datalink and enhance maritime navigation through the use of bidirectional terrestrial and satellite communication channels.

The baseline VDE-SAT scenario, as suggested by [1], foresees LEO polar orbit with an altitude of about 600 km, equipped with a deployable circularly polarised VHF antenna.

Within this context, an Italian consortium composed by M.B.I. s.r.l, DWave s.r.l. and Thales Alenia Space Italia S.p.A., in the framework of a ESA ARTES AT projects named VOCS [3], developed a prototype bidirectional VDES Payload (TRL-4), aka **VOCS Payload**, following the guidelines of the latest release of the VDES standard (ITU-R M.2092-1 02/2022) [1].

The VOCS Payload is compliant with standard 1U CubeSats, making it integrable with typical small satellite platforms.

The main subsystems of the VOCS Payload are:

- **Processing Platform**: based on the ZYNQ Z7035 System-on-Chip (SOC) [4], and the RF Transceiver AD9361 [5], it hosts the main Digital Signal Processing (DSP) modules related to the physical layer (L1) of a VDE-SAT payload, for both Uplink (UL) and Downlink (DL) channels. The board includes:
    - Processing Subsystem (PS) (Dual-core ARM Cortex-A9, [7])
    - Programmable Logic (PL) (Kintex-7 FPGA)
    - The communication logic/interface between the PL and PS is an essential component of ZYNQ Architecture for data transfer
- Prototype **RF FE**: the custom TX and RX boards for the transmission and reception of RF signals on VHF frequency range, related to VDES applications.

Figure 1 shows the rendering implementation of the VOCS Payload, which integrates as Processing Platform commercial-off-the-shelf (COTS) part numbers (PN) with flight heritage.

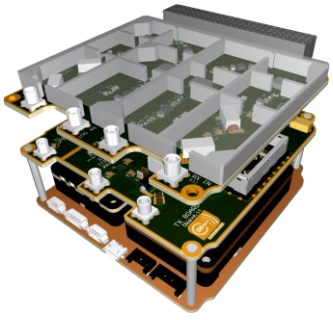


Figure 1: Rendering of the VOCS Payload

To make the VOCS payload operational for a VDE-SAT mission, it is necessary to integrate it with a deployable VHF antenna, circular polarized, tuned on VDES frequency range, and a GNSS receiving system, for time synchronization purposes.

Indeed, the VDES system uses the concept of a VDES frame, [1]: a frame equals one 1 minute and is divided into 2250 slots. Access to the data link for a terminal (ship) is, by default, given at the start of a slot. The VDES frame structure is synchronized in time to UTC (as in AIS). The VDES frame is subdivided into different Logical Channels (LC): a LC define functions for a set of continuous slots within a UL channel. The VDES frame, and corresponding association of LC, are specified in the VDE-SAT bulletin board, forwarded in the DL channels, as specified in [1]. For this reason, the GNSS system is necessary to allow the on-board modules to be aligned with universal UTC time.

The operational frequency ranges assigned to VDE-SAT, as by ITU-R M.1371-5, [6], are 157.1875-157.3375 and 161.7875-161.9375 MHz, named Lower Leg and Upper Leg, respectively. Lower Leg and Upper Leg are composed of 3 channels of 50 kHz, for an overall band of 150 kHz, each.

VOCS Payload uses the Lower Leg for the reception of the UL channels and the Upper Leg for the transmission of the DL channels. Furthermore, the RX stages were designed with *extended bandwidth* to receive also the Long-R AIS 3 / 4 and AIS1, AIS2, ASM1, ASM2 channels on Lower Leg and Upper Leg, respectively, allowing the possibility to process on-board all the modulation included in the VDES standard.

Figure 2: VHF data exchange system frequency usage in accordance with [6]

The VOCS payload was designed, breadboarded and verified using specific Verification Platform, whose main subsystems are:

- Traffic Generator (TGR): a Software Defined Radio (SDR) architecture able to emulate a population of active terminals (ships) scattered over the satellite footprint which are transmitting on the UL channels.
- DL Demodulator: SDR architecture able to decode and demodulate the RF signals on DL channels.

In the next sections, the system architecture of the VOCS Payload is described, focusing on the Software (SW) and Hardware (HW) elements and the corresponding breadboarding and testing phase.

II. SYSTEM ARCHITECTURE

A. Overview of the VOCS Payload

The next figure shows a scheme valid for VOCS payload (half-duplex) architecture

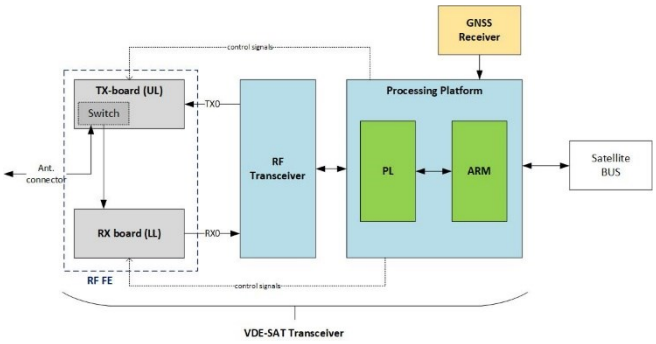


Figure 3: VOCS payload architecture

In particular, VOCS architecture is composed by the following key elements:

- **RF FE**, which integrates:
  - N.1 **TX-board:** able to transmit a single (N.1) channel of either 50 kHz or 100 kHz or 150 kHz on VDES Upper Leg bandwidth. Note that the (VHF) Switch needed to allow half-duplex operation is embedded into the TX-board
  - N.1 **RX-board:** able to receive up to N.3 physical channels at the same time on VDES Lower Leg bandwidth. This board also allows the reception of Long-Range AIS 3/4 channels and it is designed with extended bandwidth to also allow the reception of ASM1, AIS1, ASM2 and AIS2 channels when the satellite is not transmitting (i.e. DL is disabled)
- **Processing Platform**, which hosts all the DSP modules of the physical layer protocol (L-1), both for DL and UL channels; Link Layer (L-2) functionalities and external interfaces with upper layer or external modules. The board is also able to provide piloting or reference signal to the RF FE (such as piloting of VHF Switch technology)
- The **RF Transceiver** includes the ADCs and DACs required to perform digital to analogue conversion and vice versa as well as some RF stages such as analog up/down-conversions and amplifications
- A **GNSS receiver** able to generate reference signals (such as ppm or UTC time reference signal) for ARM and PL. Generally, a GNSS Receiver integrates a serial interface and a UART (Universal Asynchronous Receiver-Transmitter) interface
- A **VHF antenna**, such as Isoflux antenna (e.g. cross-dipole antenna), as suggested by [1]

B. Key components and main features

The Processing Platform, which integrates the VDE-SAT L1 DSP modules, combined with the RF FE prototype boards, composes the VOCS Payload.

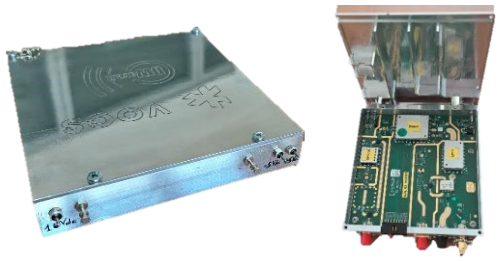


Figure 4: Picture of the TX-board

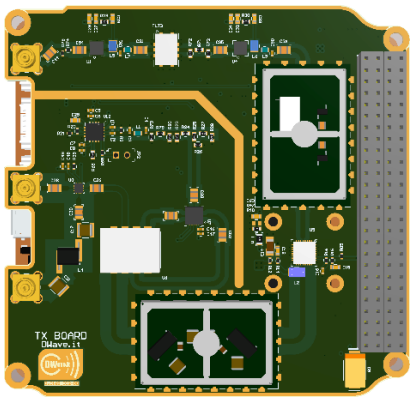


Figure 5: Tx-board rendering

The total dimensions of the VOCS Payload is 90x96x65mm and the total weight is about 0.750Kg.

The RF capabilities of the VOCS Payload are:

- Reception of 3 VDE-SAT uplink channels
- Reception of 2 ASM-SAT channels
- Reception of 4 AIS channels
- Transmission of up to 3 VDE-SAT downlink carriers

The operational frequency ranges are 157.1875-157.3375 and 161.7875-161.9375 MHz, (named Lower Leg and Upper Leg, respectively), for UL and DL, channels, respectively. In particular:

- **UL channels**: up to 150 kHz of bandwidth, the VDES standard [2] allows the allocation of N.3 channels at the same time, each 50 kHz. The UL Link IDs, as by [2], are five, and characterized by about 50 kHz of bandwidth and a Spreading Factor (SF) equal to 1, except for the Link ID20 which is SF equal to 16
- **DL channels**: up to 150 kHz of bandwidth, [2] allows the allocation of N.3 channels at the same time, each of 50 kHz. The DL Link IDs are characterized by about 50 kHz of bandwidth, except for the Link ID28 and Link ID29 which are characterized by 100 kHz and 150 kHz of bandwidth, respectively

The next table lists the main characteristics of the TX and RX boards, respectively:

TX-board specifications	RX-board specifications
Voltage Supply for HPA, RF Switch and control logic: • V1: 16-28V, 240-600mA • V2: +5V, 200mA Peak Power: 5W Signal Output Power: 28dBm MCX RF Connectors Weight: 0.350Kg Fits Standard PC104	Voltage Supply: +5V, 150mA - Gain: ~40/60dB MCX RF Connectors Weight: 0.2Kg Fits Standard PC104

Table 1: TX and RX boards characteristics

III. Design and Implementation

A. Processing Platform: Zynq Z7035 SoC

Processing Unit (ARM), combined with PL (FPGA), are the core of the Processing Platform, allowing to host all the DSP and SW modules necessary to make the VDE-SAT payload operable.

About the Processing Platform of the VOCS Payload the Evaluation Board selected is the low-power Analog Devices ADRV9361-Z7035 SDR 2x2 System-On-Module, mounted over the Carrier Board ADRV1CRR-BOB, [8], based on the low-cost EB produced by Analog Devices SDR 2x2 System On Module composed of the following main parts:

- Analog Devices AD9361 Integrated 2x2 RF Agile Transceiver
- Xilinx Zynq 7035 SoC for Digital Processing

The Processing Platform integrates:

- **VDE-SAT Demodulator**: able to demodulate up to N.3 physical adjacent UL channels, 50 kHz each, for an overall of 150 kHz; in particular the selected board is able to process: N.1 spread spectrum channel (aka *dem-sat#2*) + N.2 non-spread spectrum channels (aka dem-sat#1), or alternatively N.3 non-spread spectrum channels, running at the same time. In particular:
  - *dem-sat#1* (Linear Modulation, **LM-Demodulator**) for non-spread Link IDs (Link ID 21, 22, 23, 24)
  - *dem-sat#2* (Spread Spectrum, **SS-Demodulator**) for spread-waveform (Link ID 20, Spreading Factor = 16). It is to be noted that for SS-Demodulator, the Successive Interference Cancellation (**SIC**) module is employed. Indeed, to improve demodulation performance, SIC can be employed, as in the case of E-SSA protocol, [9]. Basically, each successfully demodulated burst is locally regenerated

and subtracted from the observation window, so that the interference (MAI) that it causes to the other bursts is removed, improving their signal-to-noise-plus-interference (SNIR). This is carried out for a certain number of SIC iterations. So, the blocks and logic required for the SIC (burst remodulation and subtraction, iterations of SIC) are only required for this Link ID. The number of SIC iterations implemented in the target EB is N.2

- **VDE-SAT Modulator:** able to transmit dynamically (based on the VDES bulletin board) up to N.3 physical adjacent DL channels, 50 kHz each, for an overall of 150 kHz, satisfying the VDES frame structure. The Link IDs managed by this module are: Link ID 25 (50 kHz), 26 (50 kHz), 27 (50 kHz), 28 (100 kHz), 29 (150 kHz), 32 (50 kHz), 33 (50 kHz), 34 (50 kHz)
- PL modules able to provide signalling or reference signal to pilot some elements of the RF FE (such as RF Switch, or Power Amplifier), and other SW modules necessary for the correct functionality of the board itself (such as external logical interfaces)

The next table shows the UL and DL Link IDs, aligned to the VDES standard, [1], manageable by the VOCS Payload:

		VDE-SAT UPLINK					VDE-SAT DOWNLINK							
Link ID		**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**32**	**33**	**34**
Payload Length	bits	80	704	3088	4512	7544	4776-32	38192-32	14326-32	21120-32	33312-32	312-32	4280-32	8320-32
CRC length	bits	16	32	32	32	32	32	32	32	32	32	32	32	32
FEC rate		1/4	2/3	2/3	2/3	5/6	1/2	1/4	1/2	1/4	1/4	1/4	1/3	1/3
Number of FEC blocks		1	1	1	1	2	1	7	19	4	6	1	1	2
FEC tail	bits	18	8	12	12	8	10	7*18	19*8	4*16	6*12	21	15	0
Padding	bits	0	0	4	3	0	0	7*3	0	0	0	0	0	0
Modulation		QPSK/CDMA	π/4-QPSK	π/4-QPSK	BPSK	16-QAM	BPSK/CDMA	π/4-QPSK	8-PSK	BPSK/CDMA	BPSK/CDMA	BPSK/CDMA	BPSK	π/4-QPSK
Bit Per Symbol	bits	2	2	2	3	4	1	2	3	1	1	1	1	2
Syncword length	symbols	48	27	27	27	27	48	27	27	48	48	48	48	27
Link ID length	symbols	0	16	16	16	16	0	0	0	0	0	0	0	0
Pilot Symbol Distance	symbols	17	0	0	33	33	N/A	27	27	N/A	N/A	8	N/A	27
Ramp Up/Down[1]	symbols	14	14	14	14	14	14	14	14	30	47	14	14	14
Codeword length	bits	402	1112	4696	6831	9108	9562	152915	229368	84544	133320	1269	12855	24960
N. of Data Symbols	symbols	201	556	2348	2277	2277	9562	76458	76458	84546	133325	1646	13171	13171
N. of Pilot Symbols	symbols	12	0	0	71	71	N/A	2940	2940	N/A	N/A	180	N/A	480
Burst Length	symbols	261	627	2419	2419	2419	10046	80371	80371	86112	134908	1646	13171	13171
Bandwidth	kHz	50	50	50	50	50	50	50	50	100	150	50	50	50
Roll-off		0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25	0,25
Symbol Rate	kbaud	2,1	33,6	33,6	33,6	33,6	4,2	33,6	33,6	36,0	56,4	4,2	33,6	33,6
Chip Rate	kchip/s	33,6	-	-	-	-	33,6	N/A	N/A	72,0	112,8	33,6	N/A	N/A
Spreading Factor	chip	16	-	-	-	-	8	N/A	N/A	2	2	8	N/A	N/A
Burst Duration	ms	125,12	18,66	71,99	71,99	71,99	2392,0	2392,0	2392,0	2392,0	2392,0	392,0	392,0	392,0
Slot Duration	ms	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67	26,67
Guard Interval	ms	8	8	8	8	8	8	8	8	8	8	8	8	8
Burst Duration	slot	5	1	3	3	3	90	90	90	90	90	15	15	15

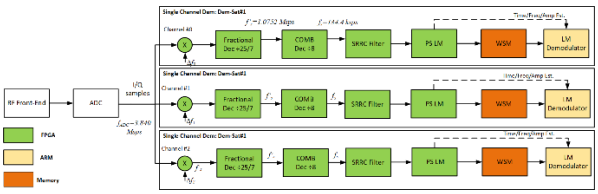
[1] Chips for Link ID 20, 25, 28, 29, 32

Table 2: VDE-SAT Link IDs manageable by the VOCS Payload

The EB Z7035 installed in the Verification Platform, was connected to N.2 GPS modules, for the injection of the 40 MHz reference signal (to stabilize in frequency the internal Local Oscillator) and PPM (pulse-per-minute) reference signal (to inject the universal UTC time-synchronization foreseen by the VDE slot frame).

1) VDE-SAT Demodulator

The overall receiver scheme is reported in Figure 6 (together with the division of tasks between FPGA and ARM).



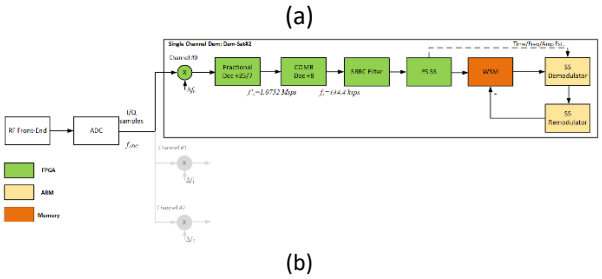


Figure 6: Uplink receiver architecture (a): LM Demodulator (dem-sat#1) and (b) SS Demodulator (dem-sat#2)

It is worth to recall that the three channels are adjacent, therefore, if the receiver sets its RF frequency f_{RX} equal to the center frequency of the central channel (the values of Δf_i, $i = 1,2,3$, used to extract each VDE-SAT channel are $\Delta f_i \in [-50,0,50]$ kHz.

As for what concerns the satellite modes architectures, to summarize:

- **Dem-Sat#1** is the demodulation architecture for VDE-SAT Link Id 21/24
- **Dem-Sat#2** is the demodulation architecture for VDE-SAT Link Id 20

The main reasons for the need of two different demodulation architectures are the following: the VDE Link Id 20 is based on a constant envelope spread spectrum (SS) signal and not on a linear modulation (LM) as the case of VDE-SAT Link Id 21/24. Therefore, the demodulator of the former requires some different blocks to handle this difference. Furthermore, the VDE-SAT Link Id 20 is used also for random-access channel meaning that more bursts are simultaneously received. In order to improve demodulation performance, SIC can be employed, as discussed above.

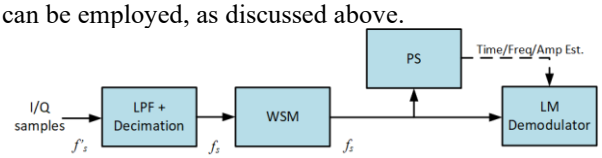


Figure 7: Dem-Sat#1 logical architecture

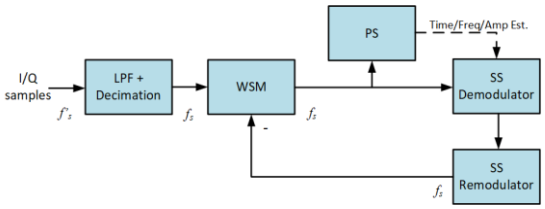


Figure 8: Dem-Sat#2 logical architecture

2) VDE-SAT Modulator

The technical specifications of the physical layer of the VDES downlink (DL) are defined in the recommendation [1], Annex 2 - section 1.2 and Annex 5 – section 2.

The VDES uplink and downlink share the architecture and the general structure of the physical layer specifications that is defined by the following items:

- frame structure
- burst properties
- modulation processing flow
- digital algorithms within the flow

- modulation scheme format

The recommendation defines several sets of properties of the items listed above. Those sets are the modulation schemes and are identified by the mean of a Link ID ([1], Annex 2 - section 1.2.7).
The above scheme shows the scheme of the VDES downlink modulator.

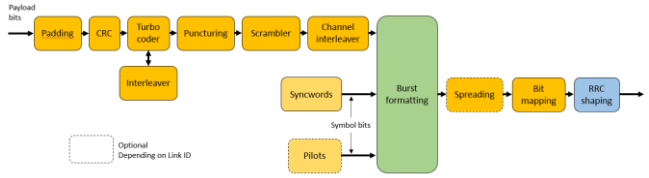


Figure 9: VDES downlink modulator block scheme

The data are coded via a forward error correction (FEC) code that is a Turbo code with mother code 1/5 defined in [1]. The coded bits are then punctured based on the puncturing patterns defined in [1], yielding coding rates in the set {1/2, 1/3, 1/4} depending on the Link Id. The resulting coding bits are then scrambled through a scrambling sequence for energy dispersal and interleaved to reduce the impact of short blockage on the channel.
Some bursts also transmit pilot symbols to aid parameters estimation at the receiver. These symbols are time interleaved with data symbols and, in particular, single pilot symbols are regularly distributed over the burst at a fixed distance. Data, syncwords and pilots are assembled to form the burst and the frame can be sent to the spreading block, depending on the Link ID.
Finally, these coded bits are mapped on the modulation symbols belonging to one of the following modulations: BPSK/CDMA, BPSK, $\pi/4$-QPSK and 8-PSK. Only the Link ID 27 defines two different modulations, one for the syncword and the other for the data stream. All the symbols which compose the burst are shaped by a root raised cosine (RRC) filter with a roll-off of 0.25 that includes a first interpolation stage with factor 4.
The next figure shows the architecture scheme of the on-board downlink transmitter in the VOCS scenario.

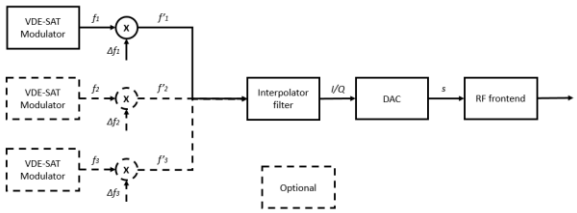


Figure 10: Downlink transmitter architecture

VOCS payload architecture allows to instantiate up to 3 modulators in the transmission path. Each modulator can have a channelization bandwidth of 50 kHz, 100 kHz or 150 kHz depending on the Link ID to be transmitted.
The up to 3 modulator outputs are mixed in the overall bandwidth by shifting each of them to base band. The frequency shift of the ith channel is Δf_i, where the latter corresponds to the frequency distance between the center of the bandwidth of the ith channel and the zero-frequency. The output *I/Q* samples are then passed to the filter and the interpolator. The digital-to-analog (DAC) block converts the interpolated *I/Q* symbols to the analog signal that is the input of the last block: the RF frontend. The latter is in charge to make the signal go on air.

B. RF Front-End: TX and RX boards

The VOCS RF architecture is shown in Figure 11:

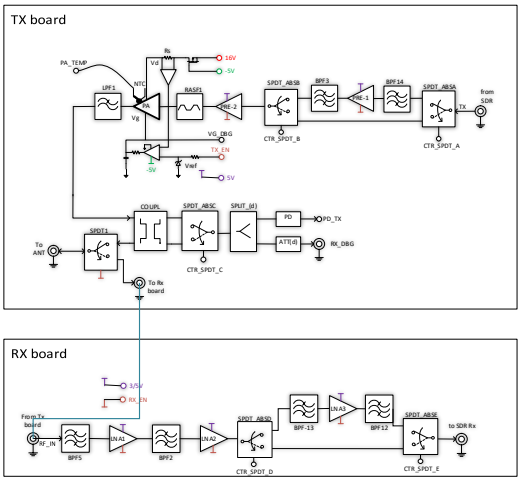


Figure 11: VOCS RF front end architecture

The RF FE is composed of the bidirectional (half-duplex) communication stages containing all the RF parts required to manage a VHF signal as required by VDES standard. It consists of N.1 TX-board (tuned on Upper Leg) and N.1 RX-board (tuned on Lower Leg).

1) TX-Board

The TX-board RF FE path is composed by following elements:

- Input passive band pass filter for 161.75-161.95 MHz band to reject out-of-band interference.
- Two LNA for first amplification gain stages.
- Passive RASF filter (custom design), to suppress noise in the 150-153MHz band which is the Radio-Astronomical band.
- High Efficiency Power Amplifier using GaN technology.
- Custom Low Pass Filter, to eliminate high order harmonics (starting from 5th).
- RF Directional Coupler for power detection measurements.
- RF SPDT Switch for half-duplex functionality.

Within the architecture, the device is able to provide 61dB of gain in the 159.4MHz – 163.15MHz with a noise figure of 4.9dB. The TX signal power budget is summarized in the following table:

Element TX (UL)	Min Gain [dB]	Nominal Gain [dB]	Max Gain [dB]	Signal PAPR [dB]	Signal at min. gain [dBm]	Nom Signal [dBm]	Signal at Max gain [dBm]	Peak Output Signal [dBm]	Signal at min. gain [W]	Nom Signal [W]	Signal at Max gain [W]	Peak Output Signal [W]
Transceiver TX	NA	NA	NA	5,0	-32,7	-33,7	-33,7	-28,7	5,4E-07	4,3E-07	4,3E-07	1,3E-06
Cable	-0,1	-0,1	-0,1	5,0	-32,8	-33,8	-33,8	-28,8	5,2E-07	4,2E-07	4,2E-07	1,3E-06
Input Switch + PreAmpli1	21,5	21,7	21,7	5,0	-11,3	-12,1	-12,1	-7,1	7,4E-05	6,2E-05	6,2E-05	1,9E-04
BPF3	-2,3	-2,0	-2,0	5,0	-13,6	-14,1	-14,1	-9,1	4,4E-05	3,9E-05	3,9E-05	1,2E-04
PreAmpli2	21,2	21,4	21,4	5,0	7,6	7,3	7,3	12,3	5,8E-03	5,4E-03	5,4E-03	1,7E-02
RASF1	-0,5	-0,4	-0,4	5,0	7,1	6,9	6,9	11,9	5,1E-03	4,9E-03	4,9E-03	1,5E-02
Power Amplifier	22,0	22,0	22,0	3,7	29,1	28,9	28,9	32,6	0,81	0,78	0,78	1,82
LPF1+Directional Coupler	-0,5	-0,4	-0,4	3,7	28,6	28,5	28,5	32,2	0,72	0,71	0,71	1,66
SPDT	-0,5	-0,4	-0,4	3,7	28,1	28,1	28,1	31,8	0,65	0,65	0,65	1,52
Cable	-0,1	-0,1	-0,1	3,7	28,0	28,0	28,0	31,7	0,63	0,63	0,63	1,48
Antenna load conducted power					28,0	**28,0**	28,0	31,7	0,63	0,63	0,63	1,48

Table 3: VOCS TX-board, signal power budget table

2) RX-Board

The RX-board RF FE path is composed by following elements:

- Custom designed Broadband filter for AIS3, AIS4 and VDES (lower leg); the overall band is 156.75MHz – 157.35MHz.
- Narrow filters for the AIS3, AIS4 and VDES (lower leg); the overall band is 156.75MHz – 157.35MHz.
- Up to three LNA gain stages.
- RF SPDT Switch to bypass third gain stage.

It is able to provide 61dB nominal gain in the 155.12MHz - 164.24MHz band with a noise figure of 0.87dB. The RX power budget is summarized in the following table at three level of input power (minimum is related to Link ID 20):

Element RX	*Min. Gain [dB]*	*Nominal Gain [dB]*	*Max Gain [dB]*	*Min Output Signal [dBm]*	*Nom Output Signal [dBm]*	*Max Output Signal [dBm]*	*Min Output Signal [W]*	*Nom Output Signal [W]*	*Max Output Signal [W]*
Antenna (RX) signal power	*NA*	*NA*	*NA*	*-139,0*	*-119,0*	*-99,0*	*1,3E-17*	*1,3E-15*	*1,3E-13*
Cable	*-0,1*	*-0,1*	*-0,1*	*-139,1*	*-119,1*	*-99,1*	*1,2E-17*	*1,2E-15*	*1,2E-13*
SPDT	*-0,5*	*-0,4*	*-0,4*	*-139,6*	*-119,5*	*-99,5*	*1,1E-17*	*1,1E-15*	*1,1E-13*
BPF5	*-0,4*	*-0,4*	*-0,4*	*-140,0*	*-119,9*	*-99,9*	*1,0E-17*	*1,0E-15*	*1,0E-13*
LNA1	*22,0*	*22,0*	*22,0*	*-118,0*	*-97,9*	*-77,9*	*1,6E-15*	*1,6E-13*	*1,6E-11*
BPF2	*-2,3*	*-2,0*	*-2,0*	*-120,3*	*-99,9*	*-79,9*	*9,3E-16*	*1,0E-13*	*1,0E-11*
LNA2	*21,5*	*21,7*	*21,7*	*-98,8*	*-78,2*	*-58,2*	*1,3E-13*	*1,5E-11*	*1,5E-09*
LNA3	*21,5*	*21,7*	*21,7*	*-77,3*	*-56,5*	*-36,5*	*1,9E-11*	*2,2E-09*	*2,2E-07*
Cable	*-0,1*	*-0,1*	*-0,1*	*-77,4*	*-56,6*	*-36,6*	*1,8E-11*	*2,2E-09*	*2,2E-07*
RX board Output (Transceiver RX input) conducted power				*-77,4*	***-56,6***	*-36,6*	*1,82E-11*	*2,19E-09*	*2,19E-07*

Table 4: VOCS RX path, signal power budget table

Figure 12 shows the RF FE of VOCS Payload installed on the Verification Platform:

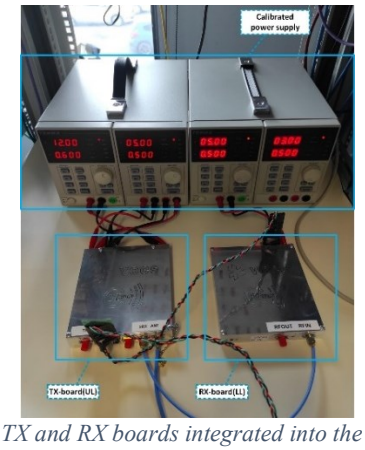


Figure 12: TX and RX boards integrated into the Verification Platform

IV. TESTING AND EVALUATION

A. Testbed setup and methodologies

Figure 14 shows the scheme of the Verification Platform, i.e. the **VOCS Testbed** used for the testing of VOCS Payload in a laboratory environment.

In particular:

- The modules related to the **VOCS Payload**, which integrates the *Processing Platform* (connected to the GPS modules) and the prototype RF FE, are highlighted in blue. The RF-FE includes the TX-board Lower Leg and the RX board Upper Leg, as evidenced in the next figure:

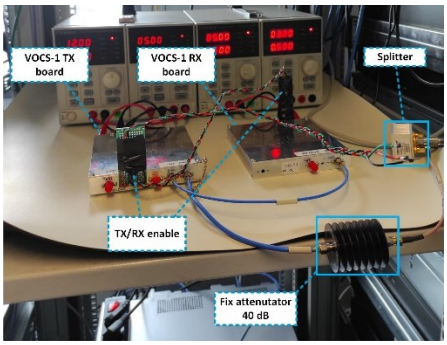


Figure 13: VOCS Testbed, Rx/Tx boards prototype

- The modules related to the "*ground components*" are highlighted in grey, i.e.:
  - The **Traffic Generator**, connected to a SDR device with integrated GPSDO, which integrates the modulator of UL Link IDs and is in charge of the emulation of the active VDES terminal on the UL channels over the satellite footprint
  - The **DL demodulator**, connected to a SDR device which is in charge of the demodulation of the incoming DL Link IDs on DL channels
  - A **Control PC**, to run the Testbed via WEB Graphic User Interface (GUI)
  - **Miscellaneous**, such as Radio Frequency (RF) cables, RF fixed attenuators, RF Splitter 4-way, Calibrated power supplies, Spectrum Analyzer, GBE Switch, ETH cables, electric cables, etc.

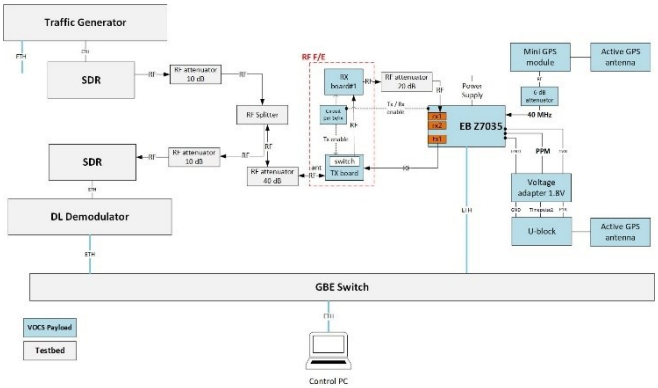


Figure 14: VOCS Verification Platform

The on-board SW, split among ARM and PL, is mainly responsible for the following tasks:

- Demodulation of VDE-SAT uplink bursts (spread and non-spread)
- Transmission of VDE-SAT downlink bursts (spread and not spread)
- Receiver and transmitter burst scheduling
- RF Transceiver Tx/Rx configuration
- VDES bulletin board emulator
- Timing and TDMA slot selection
- External interfaces to upper layer and control and general command and monitoring functions

The Verification Platform was used to validate the main Key Performance Indicators (KPIs) of the RF FE and to assess the performance of the on-board SW modules, focusing on VDE-SAT Demodulator and VDE-SAT Modulator.

B. Breadboarding and prototyping processes

The implementation losses of UL and DL Link IDs are always < 0.5 dB w.r.t. the indication of the VDES Standard, [1], this reflects the goodness of the implementation on the target Processing Platform.
The KPIs of the RF FE, such as operational frequency range, out-of-band emission, noise figure, etc. measured and analyzed during the breadboarding and testing phase through the Verification Platform, are aligned with the specifications suggested (or deduced) by the VDES standard, [1].
In particular:

- The HPA is capable of delivering 28 dBm conducted power.
- The ohmic losses of key elements sum up to 0.61 dB in TX-board and 0.54 dB in RX board.
- The RX noise figure is 0.87 dB with a margin of 2.43 dB from the recommended maximum value of 3.30 dB.
- The transmit carrier frequency error is -0.382 ppm, which is within the maximum allowed error of ±1 ppm (±160 Hz).
- The worst-case EIRP emission in the Radio-Astronomical band is -125.2 dBm/Hz, which is below the given requirement of -110 dBm/Hz with a 15.2 dB margin.

V. FOLLOW-UP AND ENHANCEMENTS

A. Potential improvements

The primary objective, from a technical point of view of a possible improvement, is to outline the path for advancing the VDE-SAT payload from TRL-4 to TRL-6 (or TRL-7), thereby enabling the commercialisation and integration of the implemented VOCS payloads into operational satellite systems (VHF communications) for VDES applications.

The steps for advancing the VDE-SAT payload from TRL-4 to TRL-6 can be summarised in the following points:

- **Prototype testing and validation**
    - **prototype breadboarding**: build and assemble an updated prototype of the VDE-SAT payload incorporating the upgraded hardware components (RF FE space-compliant). Ensure compatibility and interoperability with target small satellite platforms
    - **enhanced Software implementation**: implement in the candidate processing platform (with flight heritage) the refined DSP algorithms, the VDES Link Layer and the software add-on to implement fault tolerance mechanisms and error handling strategies, as expected for a VDE-SAT mission
    - **laboratory testing (TRL-5):** conduct laboratory testing of the VDE-SAT prototype to validate its performance, both HW and SW, under simulated space conditions. Evaluate key metrics such as signal-to-noise ratio, data throughput, and HW capabilities to achieve TRL-5 readiness
- **Environmental testing and demonstration**
    - **environmental simulation (TRL-6)**: subject the VDE-SAT prototype to environmental testing, including thermal cycling, vibration, and vacuum conditions, to assess its resilience and operational robustness in space-like environments
    - **Field Demonstration (TRL-7)**: conduct field demonstrations of the VDE-SAT prototype in real-world operational scenarios, e.g. embarking it on a CubeSat for an IOD, to validate its performance and functionality under actual operating conditions. Before this phase, it could be necessary to collaborate with industry partners and end-users to gather feedback and refine the payload design as needed

To summarize, potentially evolving the VOCS Payload, two steps are necessary:

- Performing VDE-SAT prototype environmental testing, including thermal cycling, vibration, and vacuum conditions, to assess its resilience and operational robustness in space-like environments
- Conducting on-field demonstrations of the VDE-SAT prototype in real-world operational scenarios, e.g. embarking it on a CubeSat for an in-orbit-demonstration, to validate its performance and functionality under actual operating conditions

B. Integration on CubeSat Platform

The **Processing Platform**, which integrated the VDE-SAT L1 modules, combined with the custom **RF FE** boards, composed the **VOCS Platform**, starting from which it is possible to make a VDES payload operational with the

following additional CubeSat COTS parts, as shown in Figure 1:

- VHF antenna, tuned on VDES frequency
- GNSS Receiver, necessary for the synchronization with universal UTC time
- as well as integration with all the on-board modules necessary to make the payload operable, such as the connection with the power supply modules (power bus) and the on-board computer (data bus)

The next figure shows a high-level scheme of a hypothetical satellite architecture, integrating the VOCS Payload:

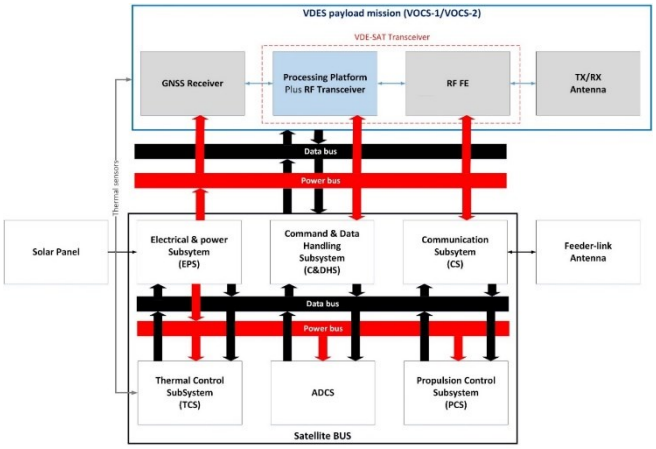


Figure 15: High-level on-board architecture

The table below summarizes the SWaP (Size, Weight and Power) constraints due to small satellite platforms for the integration of the VOCS payload

Platform	*Size*	*Weight*	*Power*
CubeSat	6U	12 kg	<20 Watt

Table 5: SWaP Constraints for CubeSat

To be noted that the philosophy of VOCS Payload, being based on CubeSat platform 6U, is to use COTS components where possible, in order to reduce the costs.
The target Processing Platform selected for VOCS payload is based on Z7035 integrated with RF Transceiver AD9361.
The target commercial solution could be based on the following COTS part numbers:

- RF Transceiver: SR2000, [10] for the VDE-SAT payload composed by Z7000,[11] and TR-600 [12]
- Processing Platform: NanoMind Processing Platform A3200, [13], in combination with NanoDock DMC3[14]

These part numbers are based on the same or very similar key modules (ADRV9361 and Z7020/Z7030/Z7035) of our target Processing Platform, and consequently, assure the same performances and most importantly the possibility of reusing the SW developed in the VOCS project.
The target deployable antenna, circular polarized is NanoCom ANT-6F, [15], (Max gain 0.8dBi) that fits on a 6U satellite.

VI. Conclusion

The paper showed the performance results and key features of an innovative bidirectional payload compatible with standard CubeSat units, developed for VDES applications, named VOCS Payload. The VOCS Payload is compliant with an half duplex operational mode, is able to manage the overall VDES frequency range and, furthermore, as assessed by the testing phase, it does not introduce any distortion or degradation on the RF signal and corresponding demodulation performances. Finally, the VOCS Payload could be enhanced by upgrading the RF FE to increase reliability and environmental resilience to guarantee it is space-compliant.

Acknowledgement

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