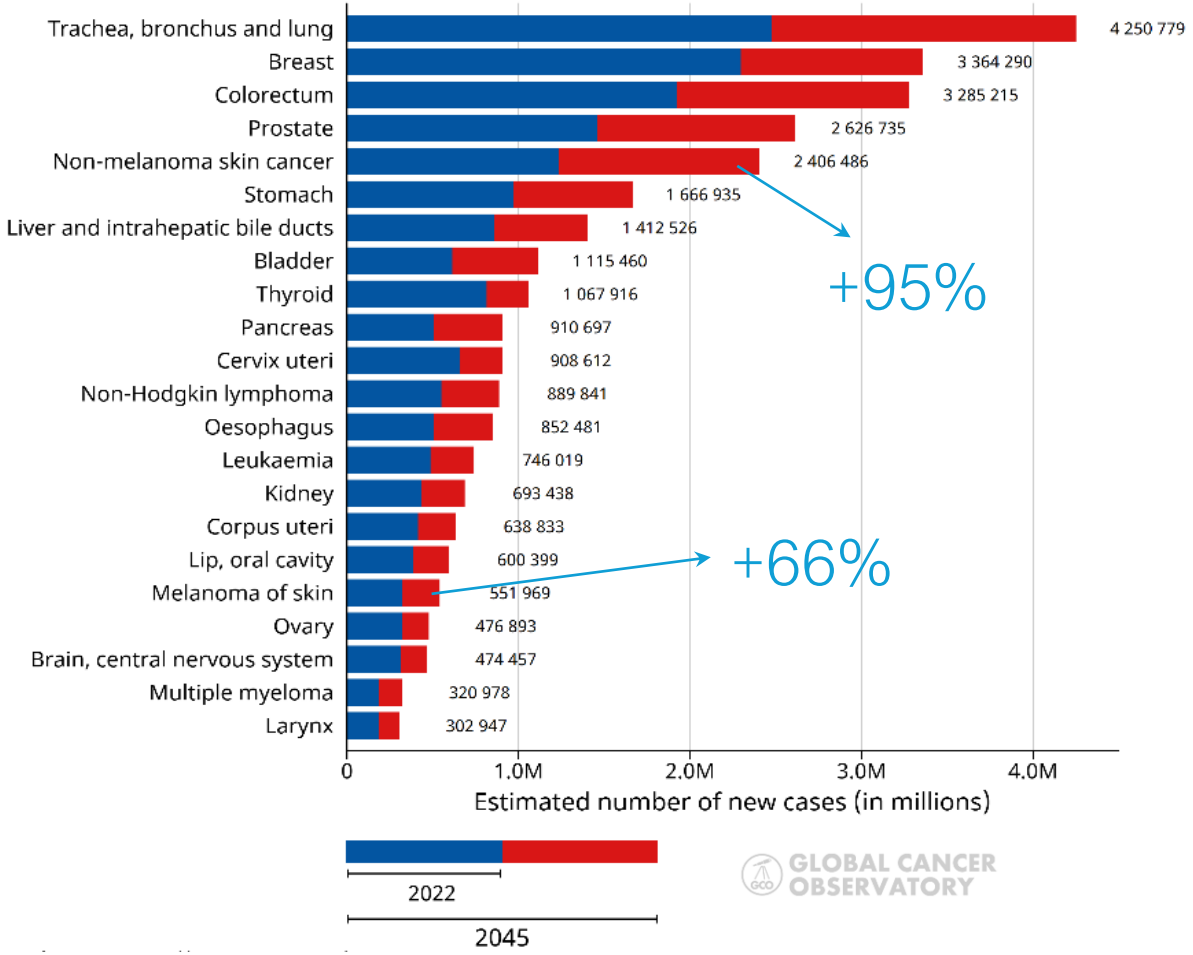
UNIC-CASS 3rd ed.

The BASIC Project

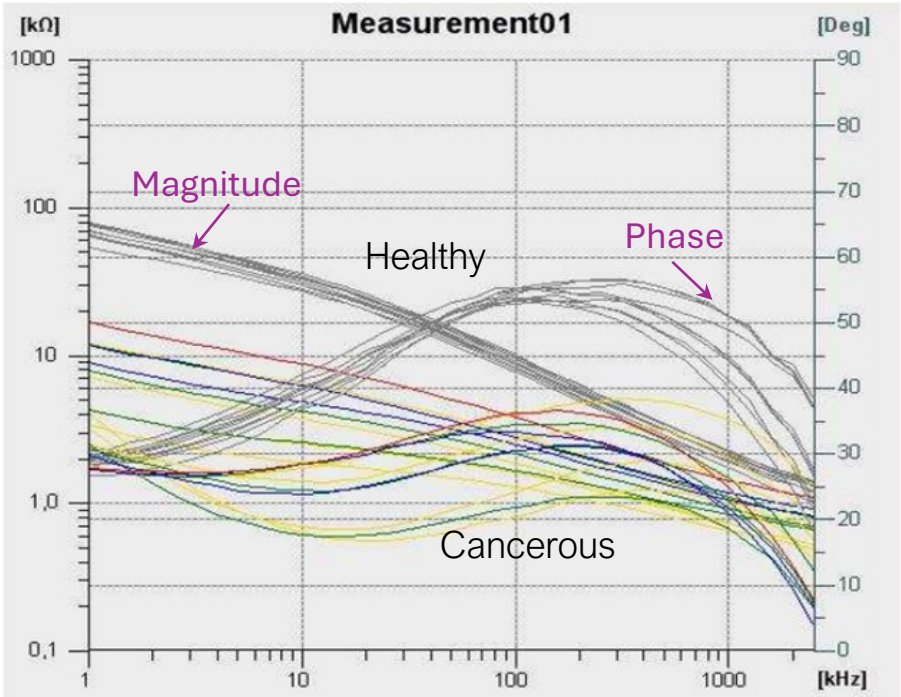
Florianópolis, December 8, 2025

A problem

Global cancer growth projections



One more way to help...

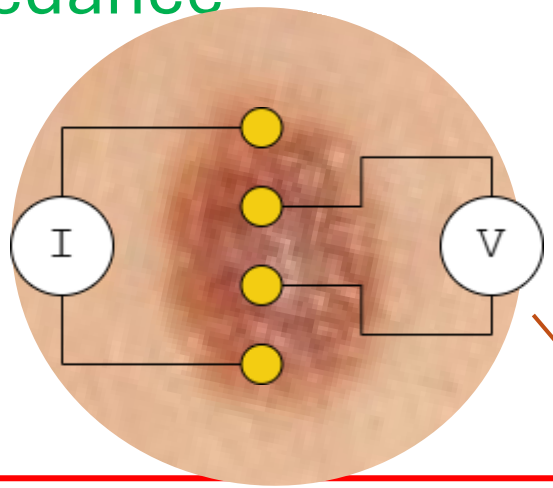


NEVISENSE™ by SCIBASE

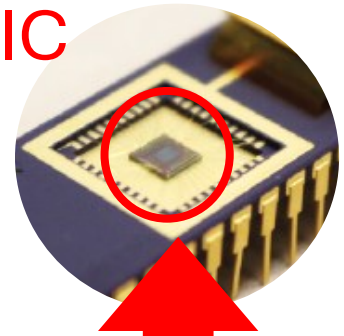
Bioimpedance

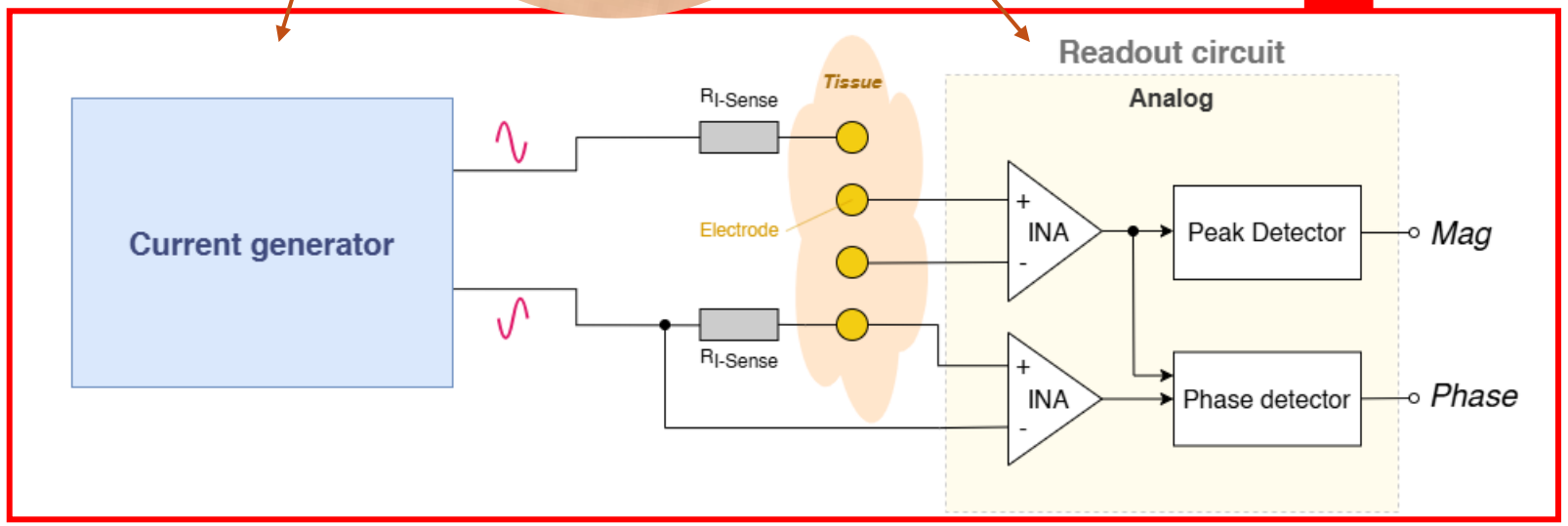
The BASIC Project

Bioimpedance



ASIC





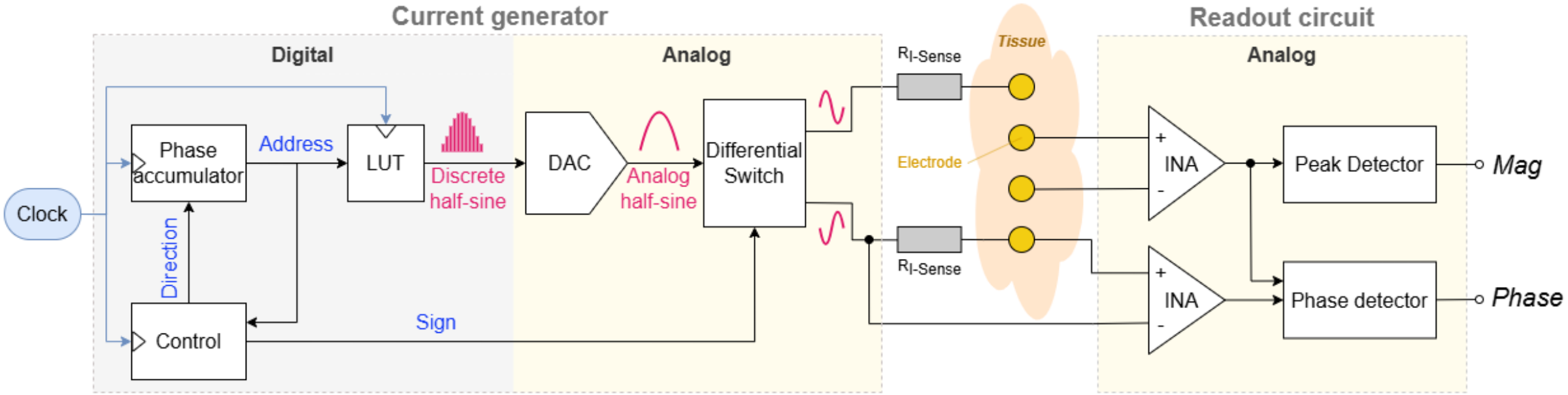
UNIC-CASS - 2023 (1st ed.)
Project: CAFEINA

- **FDDA circuit (for INA)**
  - **Analog**

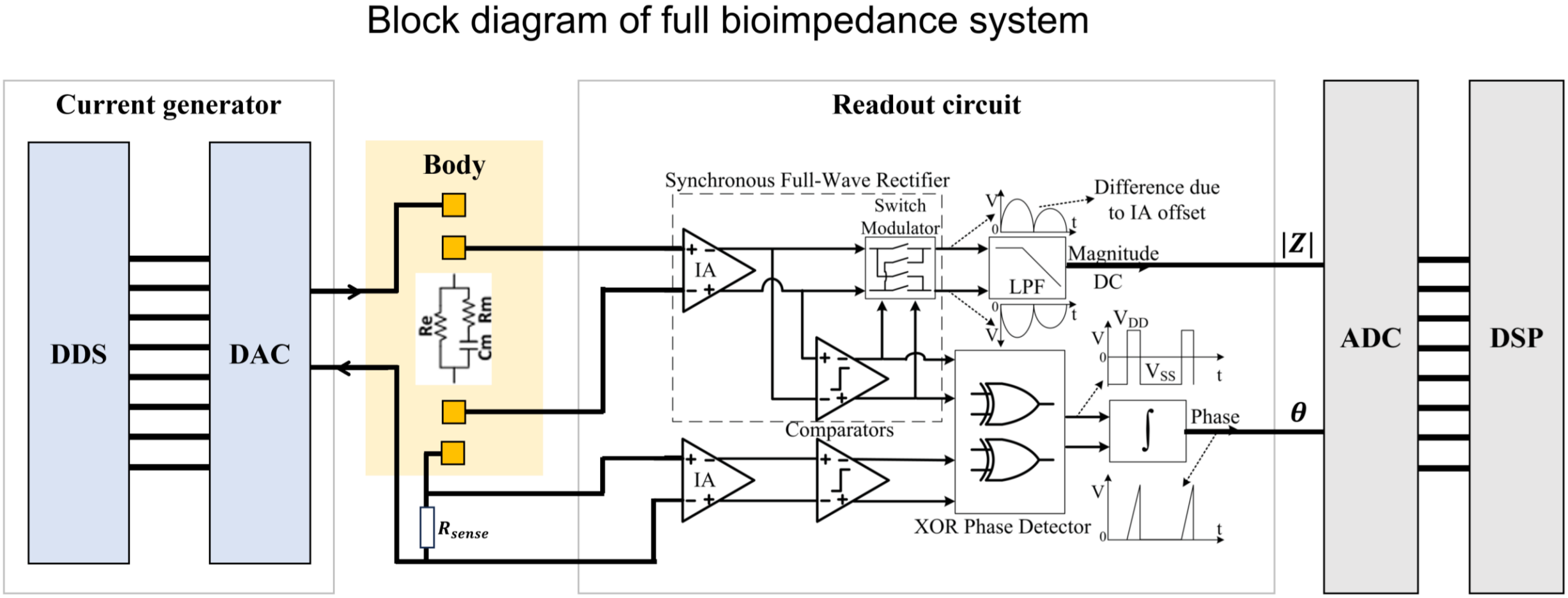
UNIC-CASS - 2024 (2nd ed.)
Project: CAFE

- **Current generator**
  - **Digital + analog**

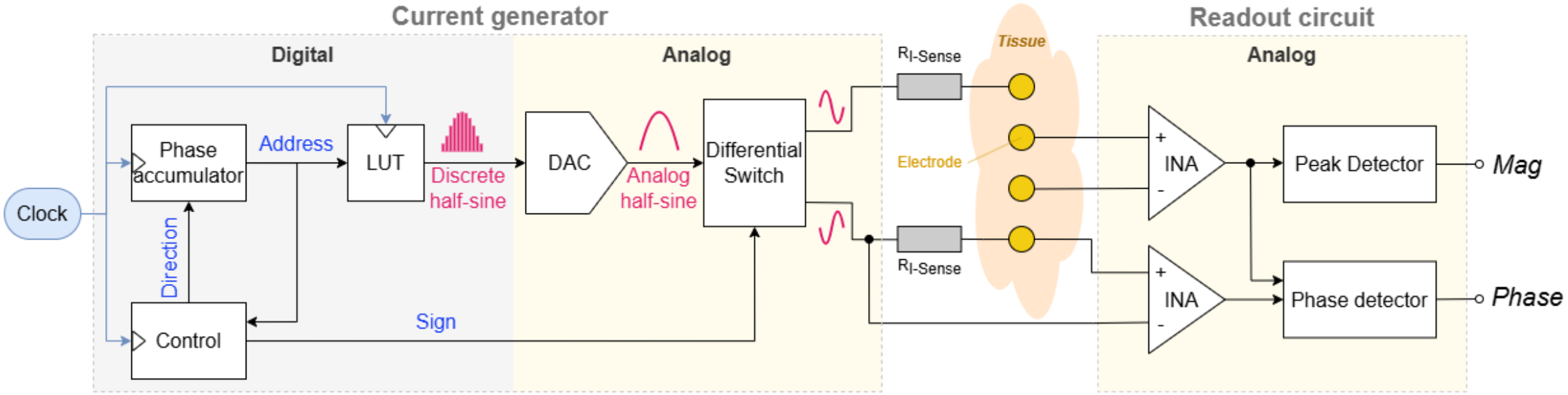
BASIC – detailed current gen



BASIC - detailed readout



UNIC-CASS 3rd ed. (2025)



→ *Plan A*

Current generator
- Digital: FSM+LUT
- Analog: DAC + Diff switch

Readout circuit
- Analog: INA + Peak detector + Phase detector

→ *Plan B*

Current generator
- Digital: FSM+LUT
- Analog: DAC + Diff switch

Readout circuit
- Analog: INA

→ *Plan C*

Current generator
- Digital: FSM+LUT
- Analog: DAC + Diff switch

Plan A

- 17 pins (min)
- W/out debug points
- W/out test mode selection

→ *Plan A*

Current generator
- Digital: FSM+LUT
- Analog: DAC + Diff switch

Readout circuit
- Analog:
  + INA
  + Peak detector
  + Phase detector

#	Pin name	Size	Direction	Domain	Description
1	AVDD	1	IO	Power	Supply for analog domain
2	VSS	1	IO	Ground	Ground
3	DVDD	1	IO	Power	Supply for digital domain
4	CC_P	1	IO	Analog	Positive CC
5	CC_N	1	IO	Analog	Negative CC
6	PU_P	1	IO	Analog	Positive PU
7	PU_N	1	IO	Analog	Negative PU
8	IREF_DAC	1	Input	Analog	DAC reference current
9	IREF_INA	1	Input	Analog	INA reference current
10	IGEN_SEL	1	Input	Digital	Current selector
11	GSEL<1:0>	2	Input	Digital	INA gain selector
12	CLK	1	Input	Digital	1MHz – 510 MHz
13	RST	1	Input	Digital	Rst for digital
14	VCM	1	Input	Analog	External CM voltage
15	EN_AN	1	Input	Digital	Enable for analog blocks
16	Magnitude	1	Output	Analog	Mag output
17	Phase	1	Output	Analog	Phase output

Plan B

- 15 pins (min)
- W/out debug points
- W/out test mode selection

→ Plan B

Current generator

- Digital: FSM+LUT
- Analog: DAC + Diff switch

Readout circuit

- Analog: INA

#	Pin name	Size	Direction	Domain	Description
1	AVDD	1	IO	Power	Supply for analog domain
2	VSS	1	IO	Ground	Ground
3	DVDD	1	IO	Power	Supply for digital domain
4	CC_P	1	IO	Analog	Positive CC
5	CC_N	1	IO	Analog	Negative CC
6	PU_P	1	IO	Analog	Positive PU
7	PU_N	1	IO	Analog	Negative PU
8	IREF_DAC	1	Input	Analog	DAC reference current
9	IREF_INA	1	Input	Analog	INA reference current
10	IGEN_SEL	1	Input	Digital	Current selector
11	GSEL<1:0>	2	Input	Digital	INA gain selector
12	CLK	1	Input	Digital	1MHz – 510 MHz
13	RST	1	Input	Digital	Rst for digital
14	VCM	1	Input	Analog	External CM voltage
15	EN_AN	1	Input	Digital	Enable for analog blocks
~~16~~	~~Magnitude~~	~~1~~	~~Output~~	~~Analog~~	~~Mag output~~
~~17~~	~~Phase~~	~~1~~	~~Output~~	~~Analog~~	~~Phase output~~

Plan C

- 10 pins (min)
- W/out debug points
- W/out test mode selection

→ *Plan C*

Current generator

- Digital: FSM+LUT
- Analog: DAC + Diff switch

#	Pin name	Size	Direction	Domain	Description
1	AVDD	1	IO	Power	Supply for analog domain
2	VSS	1	IO	Ground	Ground
3	DVDD	1	IO	Power	Supply for digital domain
4	CC_P	1	IO	Analog	Positive CC
5	CC_N	1	IO	Analog	Negative CC
~~6~~	~~PU_P~~	~~1~~	~~IO~~	~~Analog~~	~~Positive PU~~
~~7~~	~~PU_N~~	~~1~~	~~IO~~	~~Analog~~	~~Negative PU~~
6 ~~8~~	IREF_DAC	1	Input	Analog	DAC reference current
~~9~~	~~IREF_INA~~	~~1~~	~~Input~~	~~Analog~~	~~INA reference current~~
7 ~~10~~	IGEN_SEL	1	Input	Digital	Current selector
~~11~~	~~GSEL<1:0>~~	~~2~~	~~Input~~	~~Digital~~	~~INA gain selector~~
8 ~~12~~	CLK	1	Input	Digital	1MHz – 510 MHz
9 ~~13~~	RST	1	Input	Digital	Rst for digital
~~14~~	~~VCM~~	~~1~~	~~Input~~	~~Analog~~	~~External CM voltage~~
10 ~~15~~	EN_AN	1	Input	Digital	Enable for analog blocks
~~16~~	~~Magnitude~~	~~1~~	~~Output~~	~~Analog~~	~~Mag output~~
~~17~~	~~Phase~~	~~1~~	~~Output~~	~~Analog~~	~~Phase output~~

IGEN (Current Generator) - DDS

Block	Pin name	Size	Direction	Domain	Description
DDS	CLK	1	Input	Digital	1MHz – 510 MHz
	RST	1	Input	Digital	Rst for digital
	DVDD	1	IO	Power	Supply for digital domain
	SIGN	1	Output	Digital	Control sign of sine
	~~SIGNB~~	~~1~~	~~Output~~	~~Digital~~	~~Complementary control~~
	SINE_OUT<17:0>	18	Output	Digital	Control for 4T3B- DAC

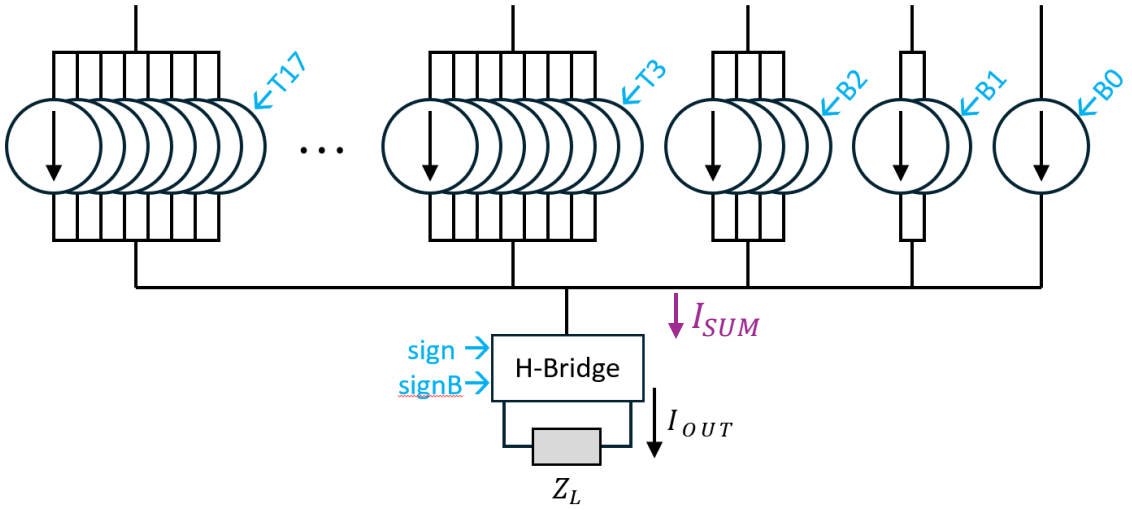
- Verilog: 6 pins
- DDS for layout: 6 pins + DVDD+DVSS = 8 pins
- W/out debug points

- Verilog for DDS done (no debug or sel mode included)
- If include inverter in DSW input SIGNB could be eliminated.
- If non-overlap circuit added, SIGNB could be eliminated.

IGEN (Current Generator) - DAC

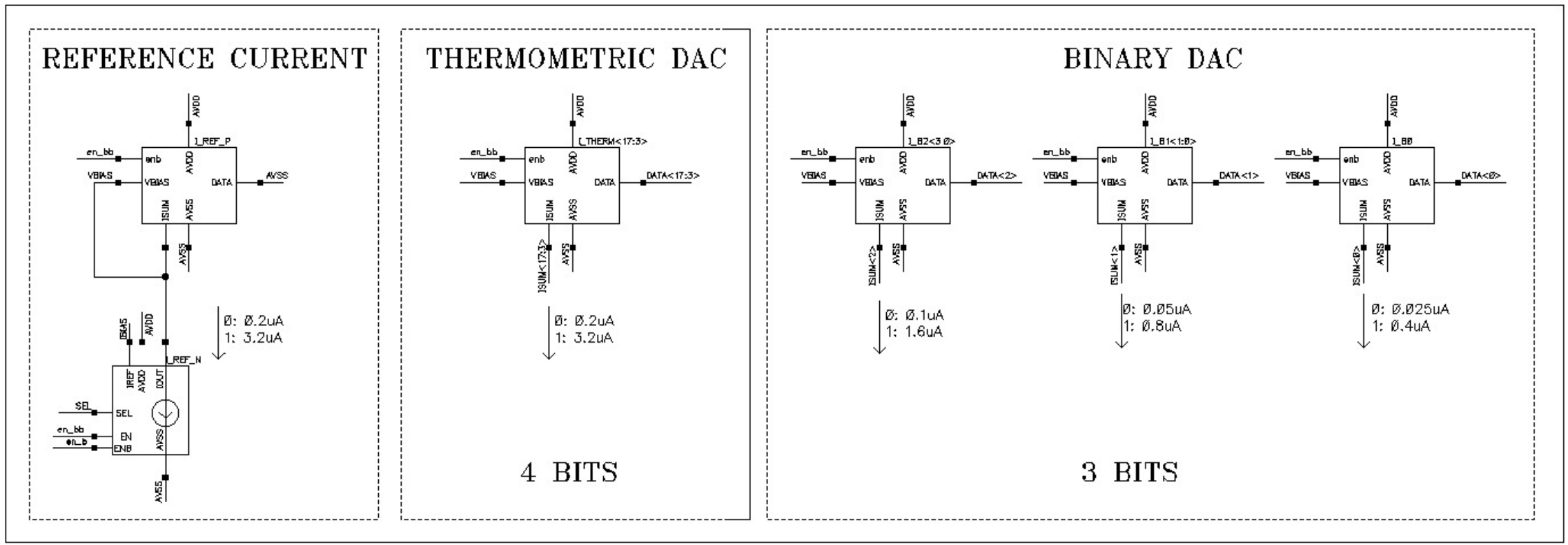
Block	Pin name	Size	Direction	Domain	Description
DAC	AVDD	1	IO	Analog	Supply for analog domain
	AVSS	1	IO	Analog	Ground for analog domain
	IREF	1	IO	Analog	Reference current
	DATA<17:0>	18	Input	Digital	15 thermometric current sources <17:3> 3 binary current sources <2:0>
	SEL_IGEN	1	Input	Digital	Current selector
	EN_AN	1	Input	Digital	Enable for analog blocks
	ISUM~~<17:0>~~	~~18~~ or 1	Output	Analog	Analog output

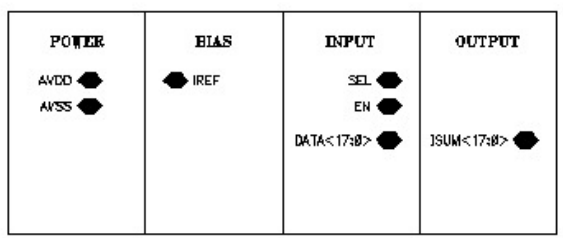
- 4T3B DAC: 15 thermometric current sources <17:3>
  3 binary current sources <2:0>
- ISUM could be short circuited, since output goes to 1 size input of DSW.
- Total: 24 pins (min) or 41 pins (ISUM<17:0>)

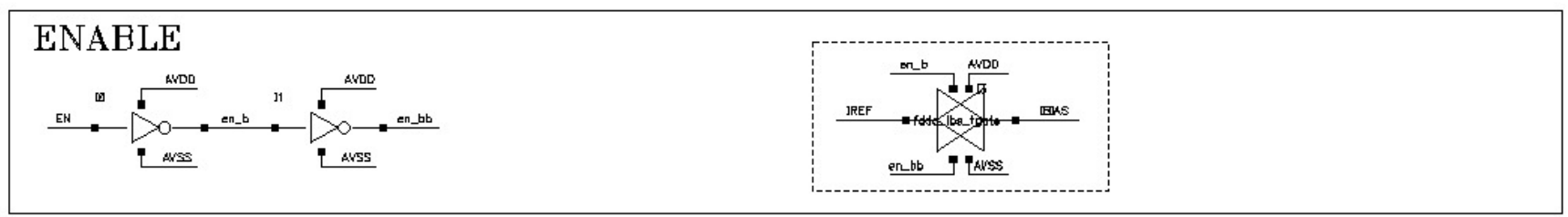


IGEN (Current Generator) - DAC

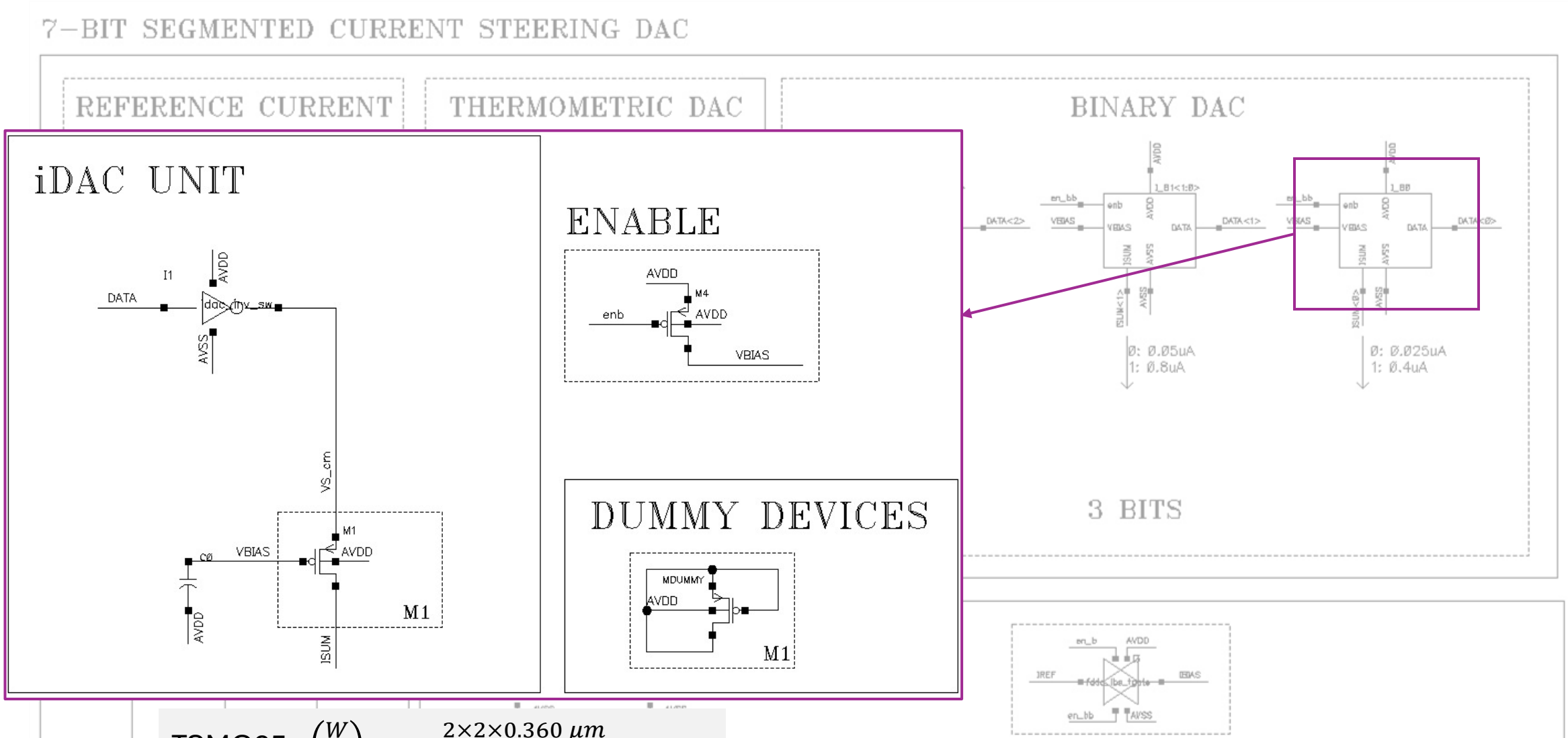
7−BIT SEGMENTED CURRENT STEERING DAC





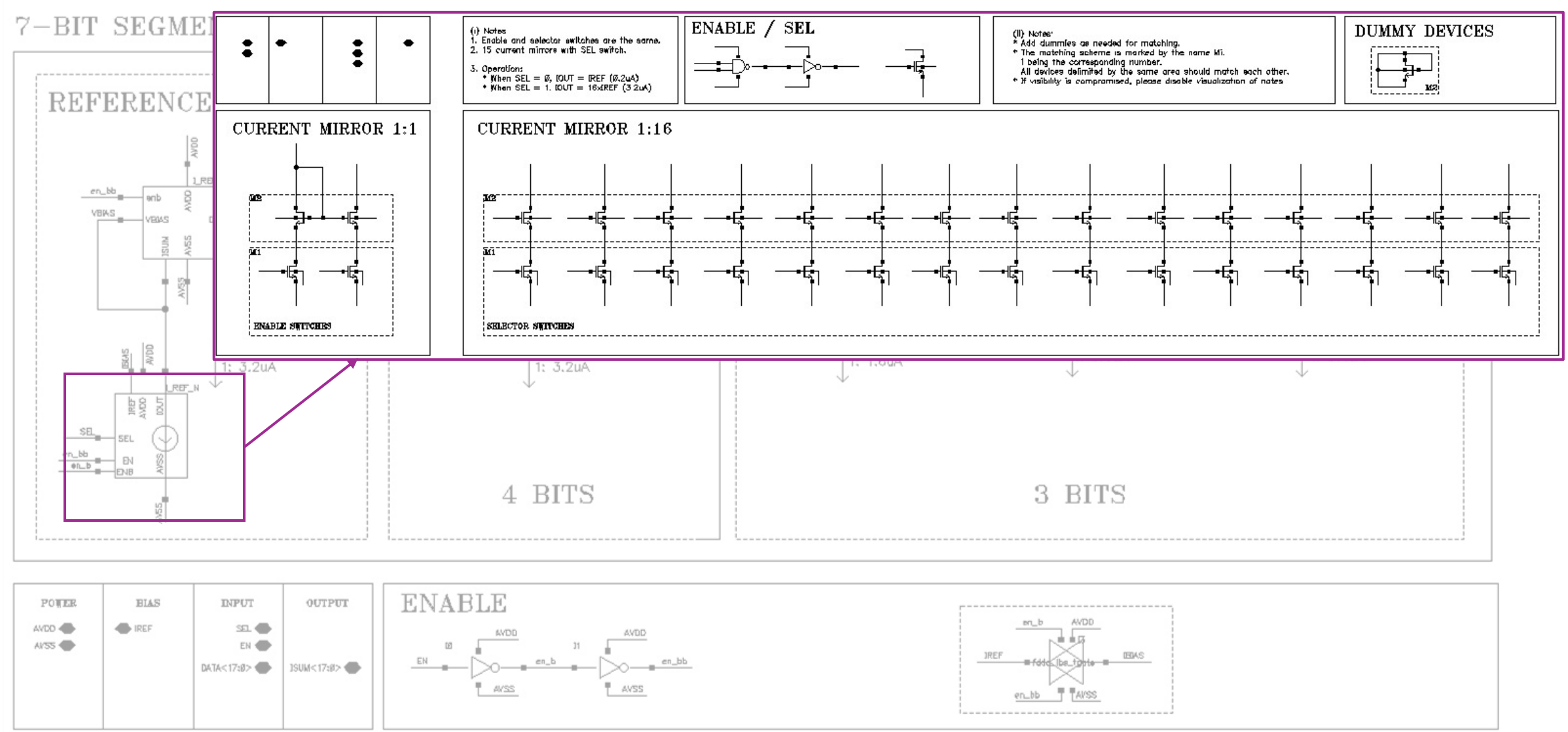


IGEN (Current Generator) - DAC



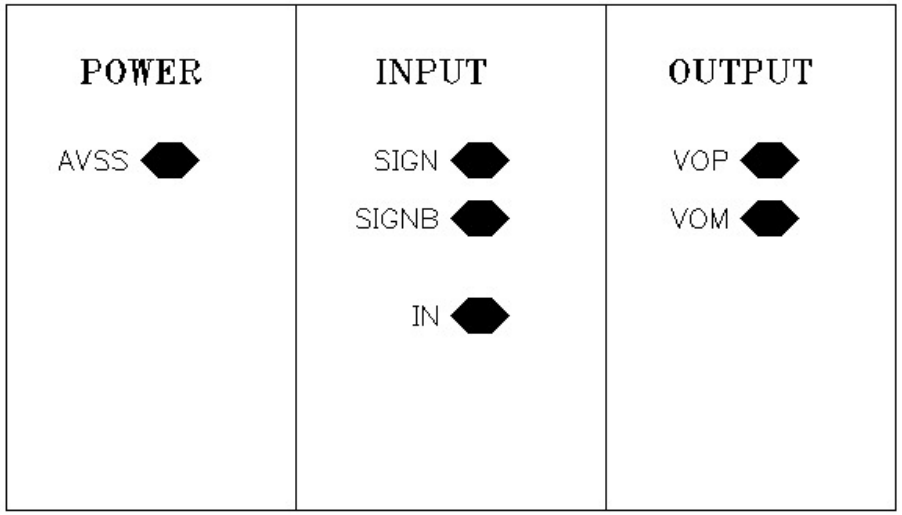
TSMC65 : $\left(\frac{W}{L}\right)_{M1} = \frac{2\times2\times0.360\ \mu m}{2\ \mu m}$

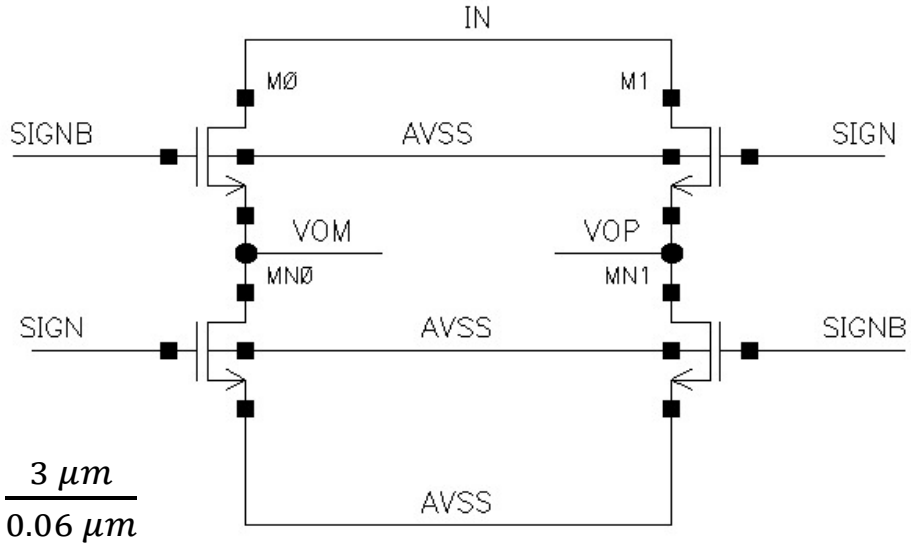
IGEN (Current Generator) - DAC



IGEN (Current Generator) - DSW

Block	Pin name	Size	Direction	Domain	Description
DSW	AVDD		IO	Power	Supply for analog domain
	AVSS		IO	Power	Ground for analog domain
	IN		Input	Analog	ISUM from DAC
	VOP		Output	Analog	Positive Output
	VOP		Output	Analog	Negative Output





TSMC65 : $\frac{W}{L} = \frac{3\ \mu m}{0.06\ \mu m}$

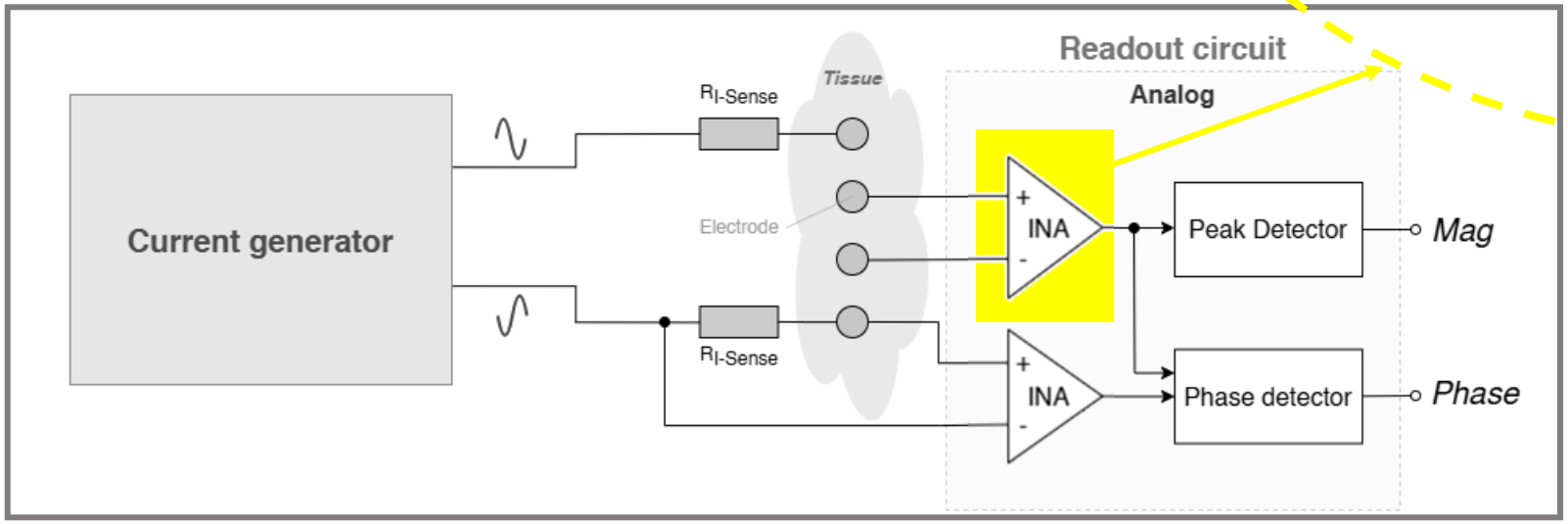
VREAD (Readout circuit) - INA

For Bioimpedance measurements:

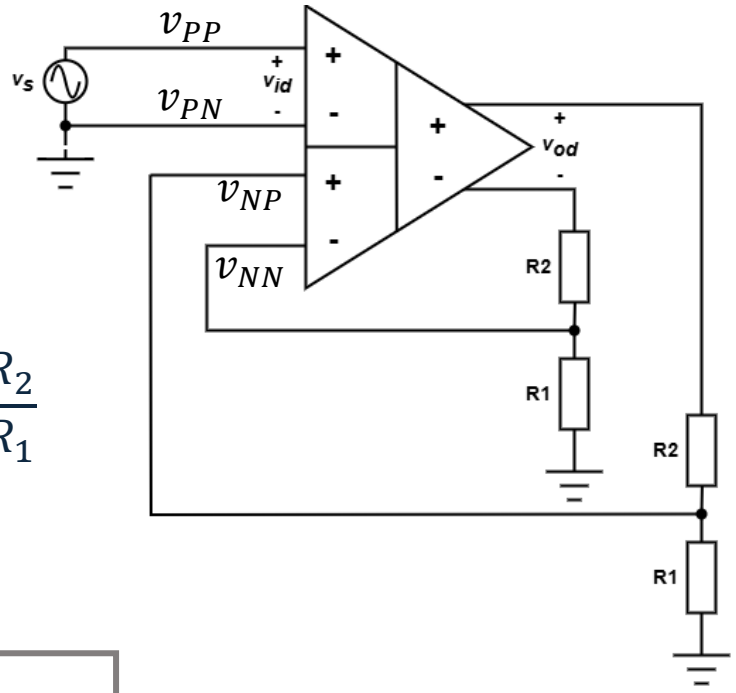
- ***Typical range 1 kHz – 1 MHz***

INA must have

- High GBW, CMRR, PSRR
- Adjustable gain: 1 (buffer), 5V/V, 25 V/V

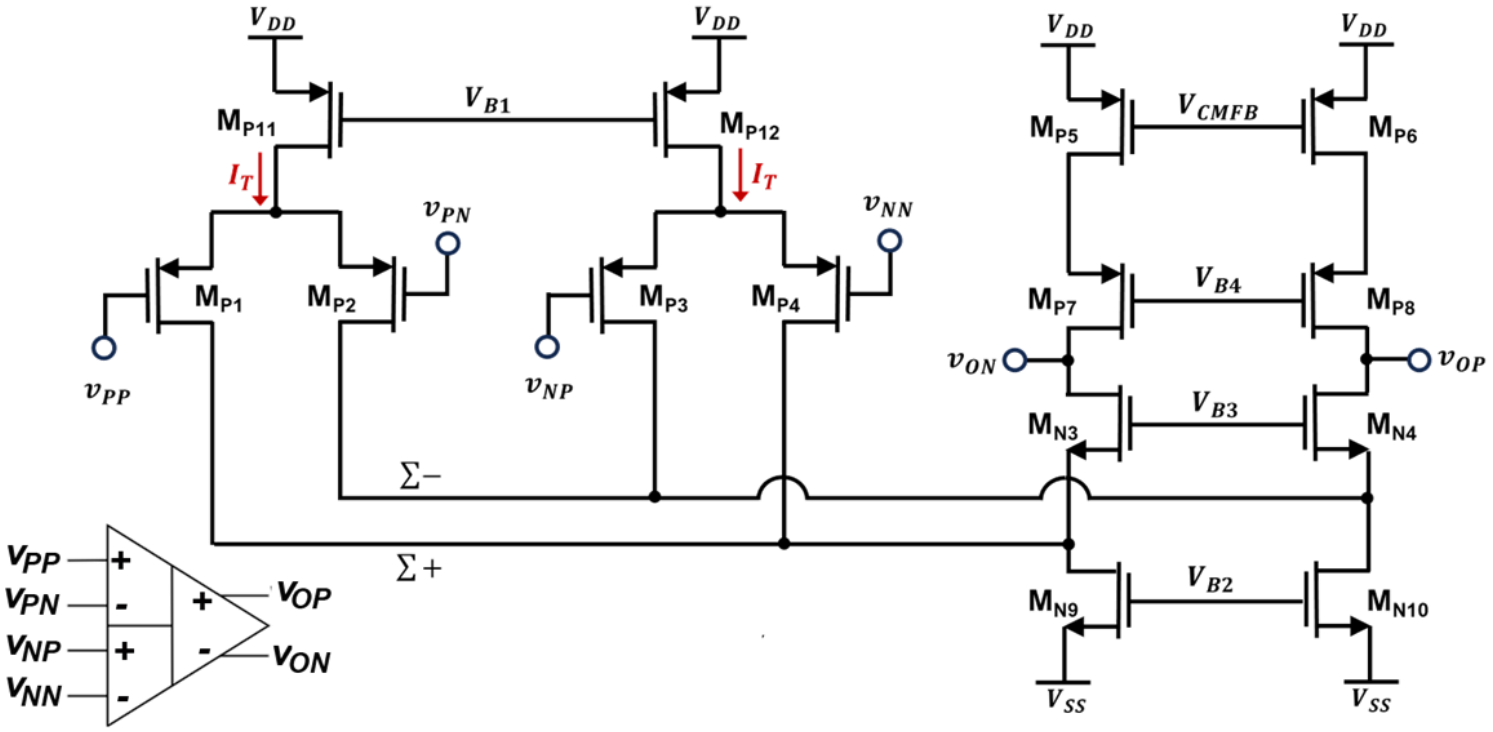


$$\frac{v_{od}}{v_{id}} = 1 + \frac{R_2}{R_1}$$



Fully Differential Difference Amplifier (FDDA)-based INA

VREAD (Readout circuit) – INA (FDDA)



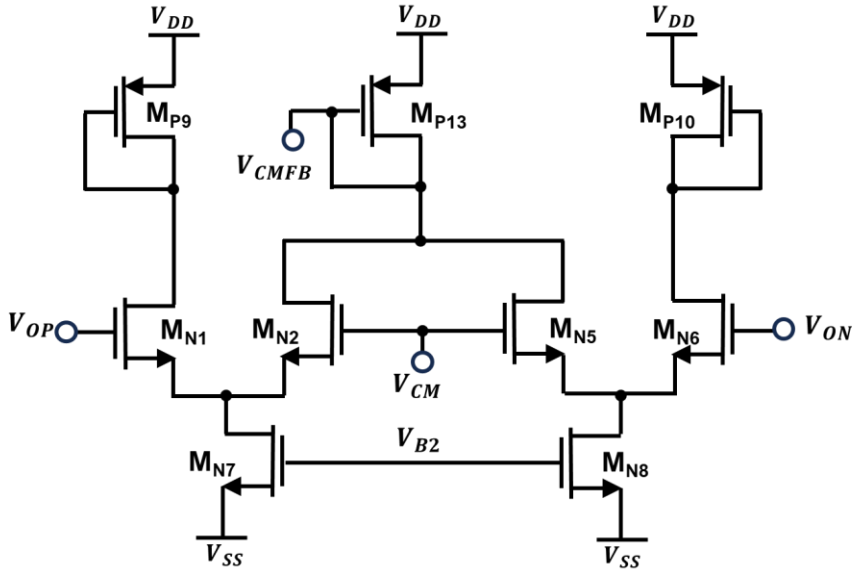
Desired:

- Vin & vout max diff swing: -0.4V – 0.4V

Depends on tech vdd

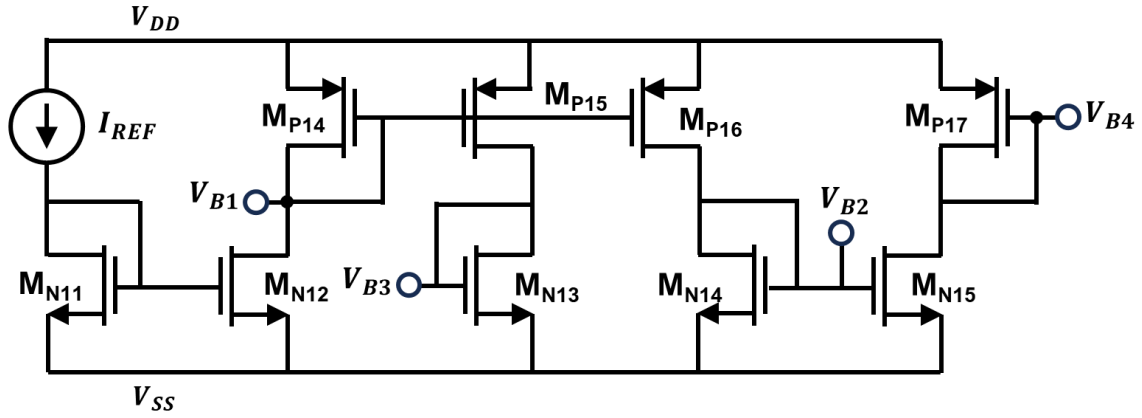
- *Vos < 2mV*
- *GBW > 30MHz (best if 50MHz)*

CMFB

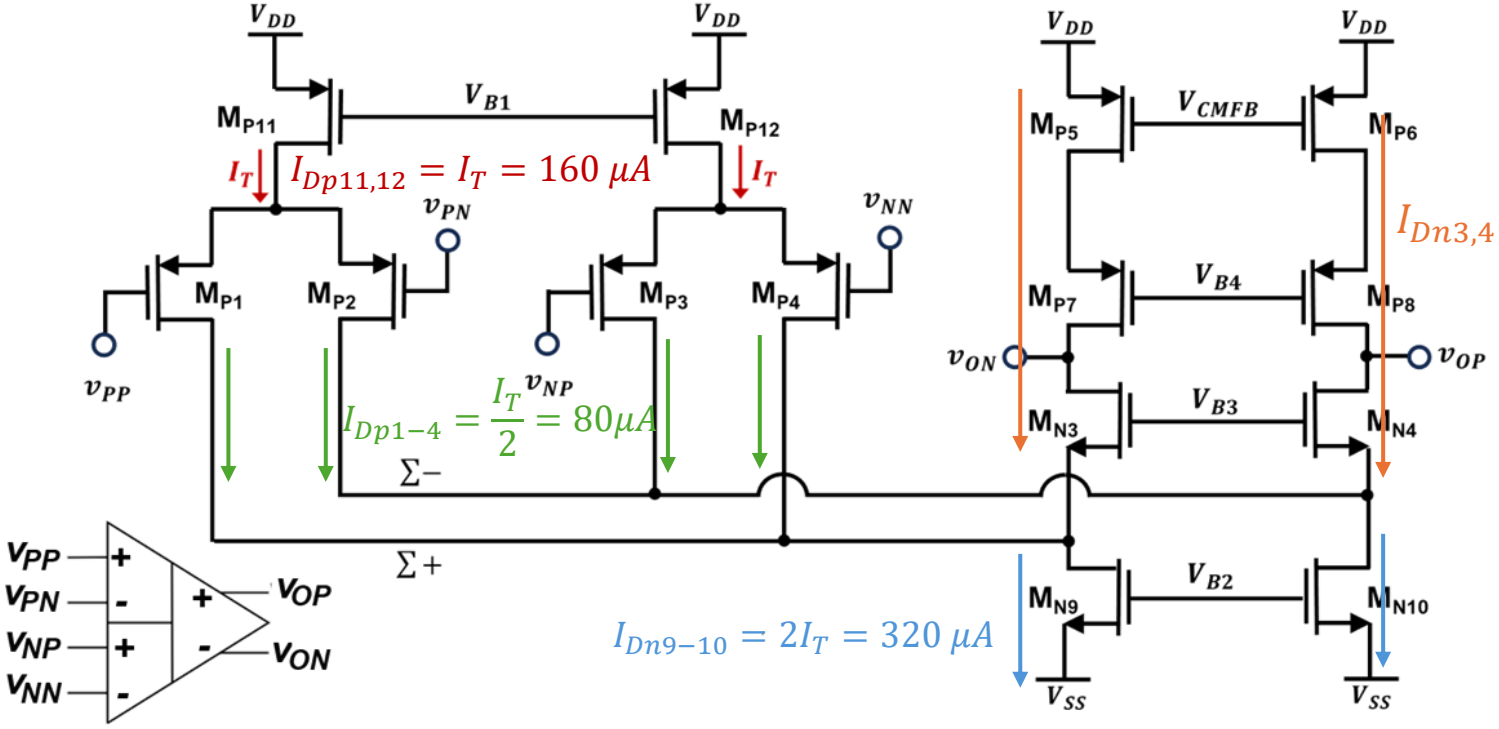


Bias circuit

$I_{REF} = 20\ \mu A$

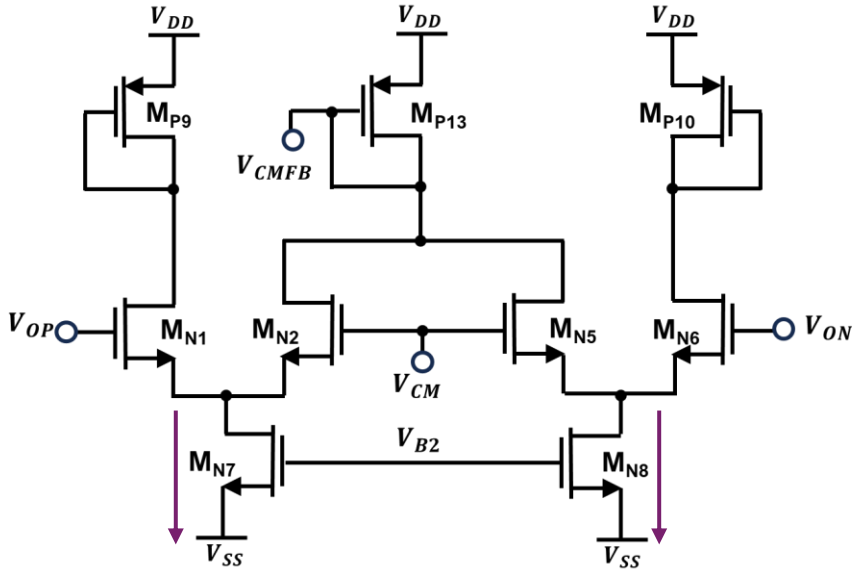


VREAD (Readout circuit) – INA (FDDA)



$I_{Dn3,4} = I_{Dp5-8} = I_T = 160\ \mu A$

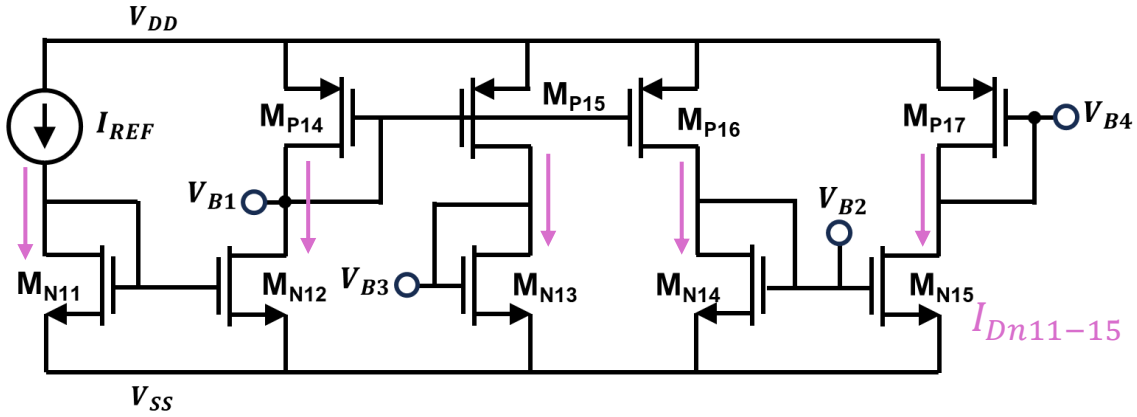
CMFB



$I_{Dn7-8} = 2I_{Dn14} \cong 40\ \mu A$

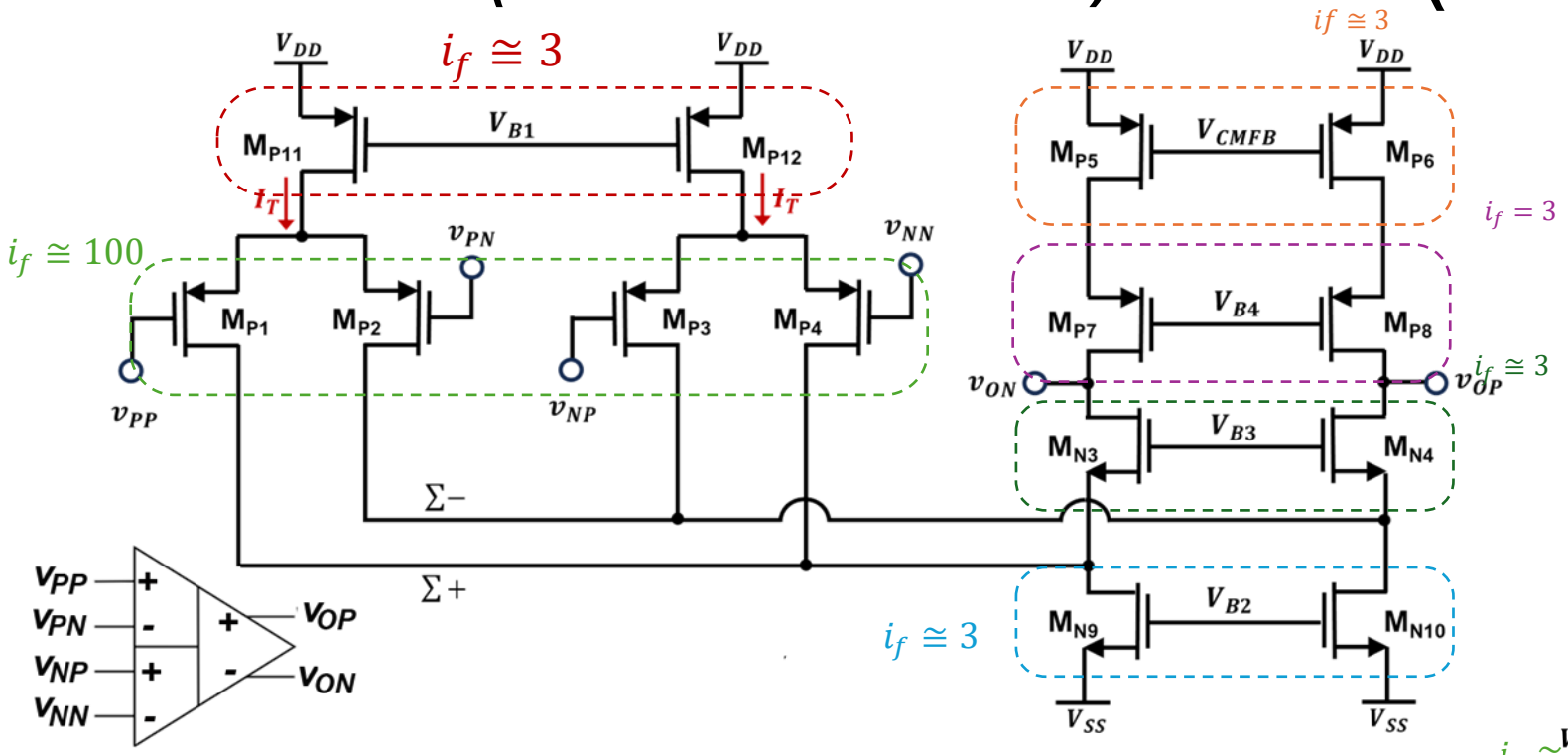
Bias circuit

$I_{REF} = 20\ \mu A$



$I_{Dn11-15} = I_{Dp14-17} = \frac{I_T}{8} \cong 20\ \mu A$

VREAD (Readout circuit) – INA (FDDA)



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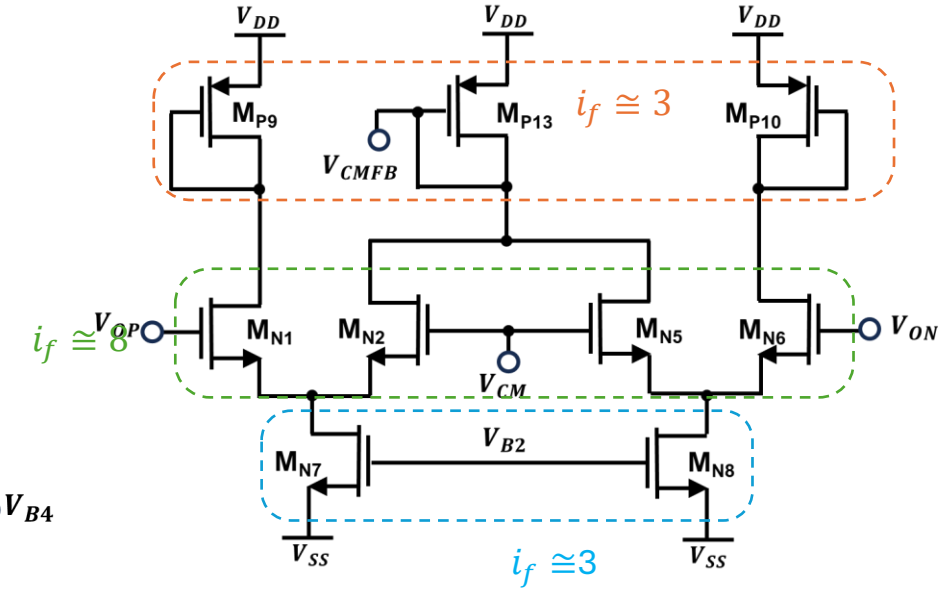
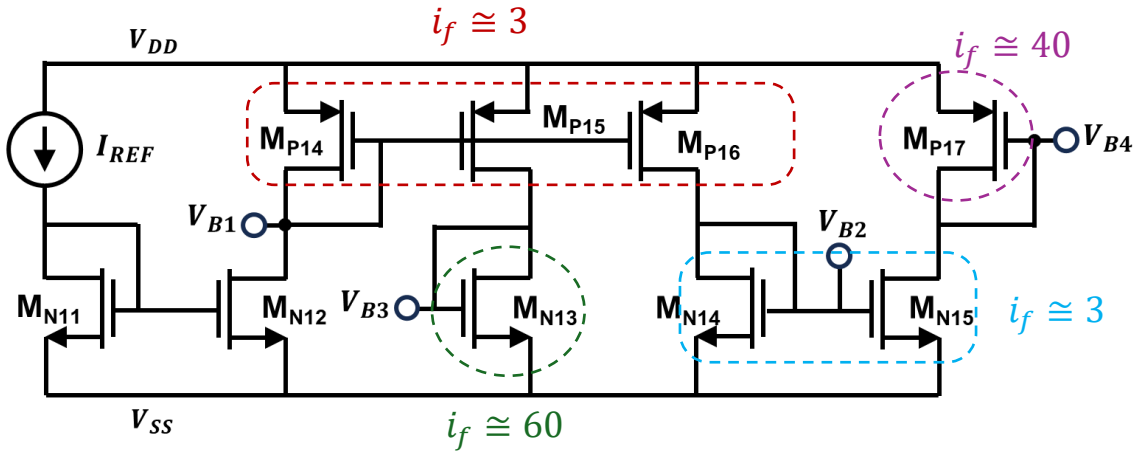


Bias circuit



VREAD (Readout circuit) – INA (FDDA)

	Device	Type	ID [uA] (ideal)	if (ideal)	W [um] (tot) m x nf x W	L [um] (tot) Series x L	S (calculated)
Input pair	MP1-4	P-lvt	80	100	24x2x0.5=24	2	12
Itail P	MP11-12	P-svt	160	3	128x4x3.5=1792	2	896
	MP5-6	P-svt	160	3	128x4x3.5=1792	2	896
	MP7-8	P-svt	160	3	64x4x3.5=896	1	896
Current source N	MN9-10	N-lvt	320	3	256x4x2	2	1024
Cascode N	MN3-4	N-lvt	160	3	80x4x1.6=512	2	512
Bias P	MP14-16	P-svt	20	3	16x4x3.5=224	2	112
Bias P	MP17	P-svt	20	40	9x4x3.5=126	8x2=16	7.88
Bias N	MN14-15	N-lvt	20	3	16x4x2=128	2	64
Bias N	MN16	N-lvt	20	60	8x4x1.6=51.2	8x2=16	3.2
CMFB pair	MN1-2,5-6	N-lvt	20	8	24x2x1.5=72	0.5	144
CMFB tail	MN7-8	P-svt	40	3	32x4x2=256	2	128
CMFB P	MP9-10	P-svt	20	3	16x4x3.5=224	2	112
CMFB P	MP13	P-svt	40	3	32x4x3.5=224	2	224

UNIC-CASS: Schedule

Date	Activity
Aug 4th, 2025	First Call for Participation
Aug 24th, 2025	Deadline for Proposal submission
Oct 28th, 2025	Result announcement
Dec 4th – March 2026	- Learn from specially curated educational materials - Design-to-Tapeout Mentoring sessions
End of March, 2026	Deadline for Layout submission (IHP)
Sept 2026	Chip test/bring-up

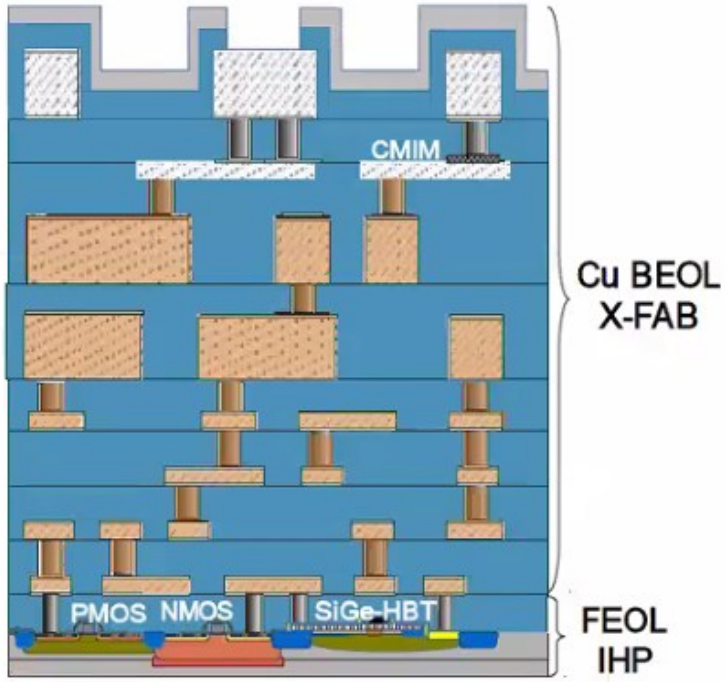
UNIC-CASS: Schedule

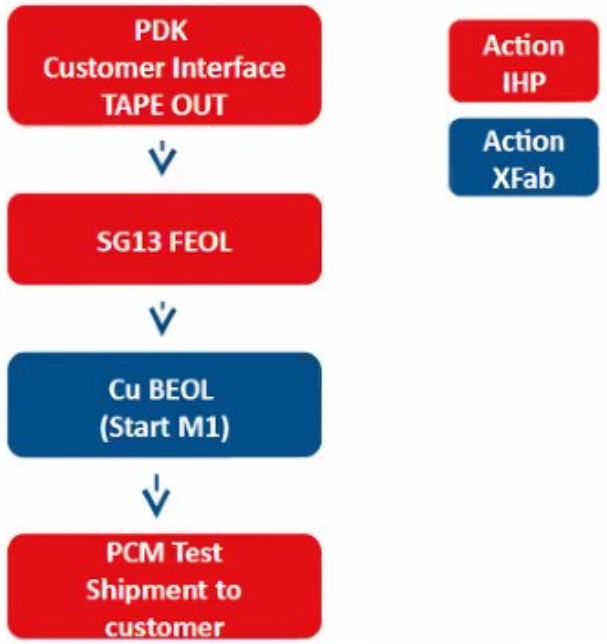
Main Design-to-tapeout milestones

- First design review (mock tapeout)
  - Purpose: Prepare the teams in advance for the final tape-out phase
    - **GO/NOGO milestone!**
  - Date: Jan 19
- Second design review (first DRC/LVS clean design delivery)
  - Purpose: Verify feasibility of designs and top integration
    - **GO/NOGO milestone!**
  - Date: Mar 9
- UNIC-CASS tapeout
  - Purpose: Final delivery of top designs (GDS+schematic+checks)
  - Date: Mar 27

UNIC-CASS: Tech

[New] IHP 130nm CMOS technology





Action IHP

Action XFab

- https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/sigec-bicmos-technologies
- https://github.com/IHP-GmbH/IHP-Open-PDK

UNIC-CASS: Tech

[New] IHP 130nm CMOS technology

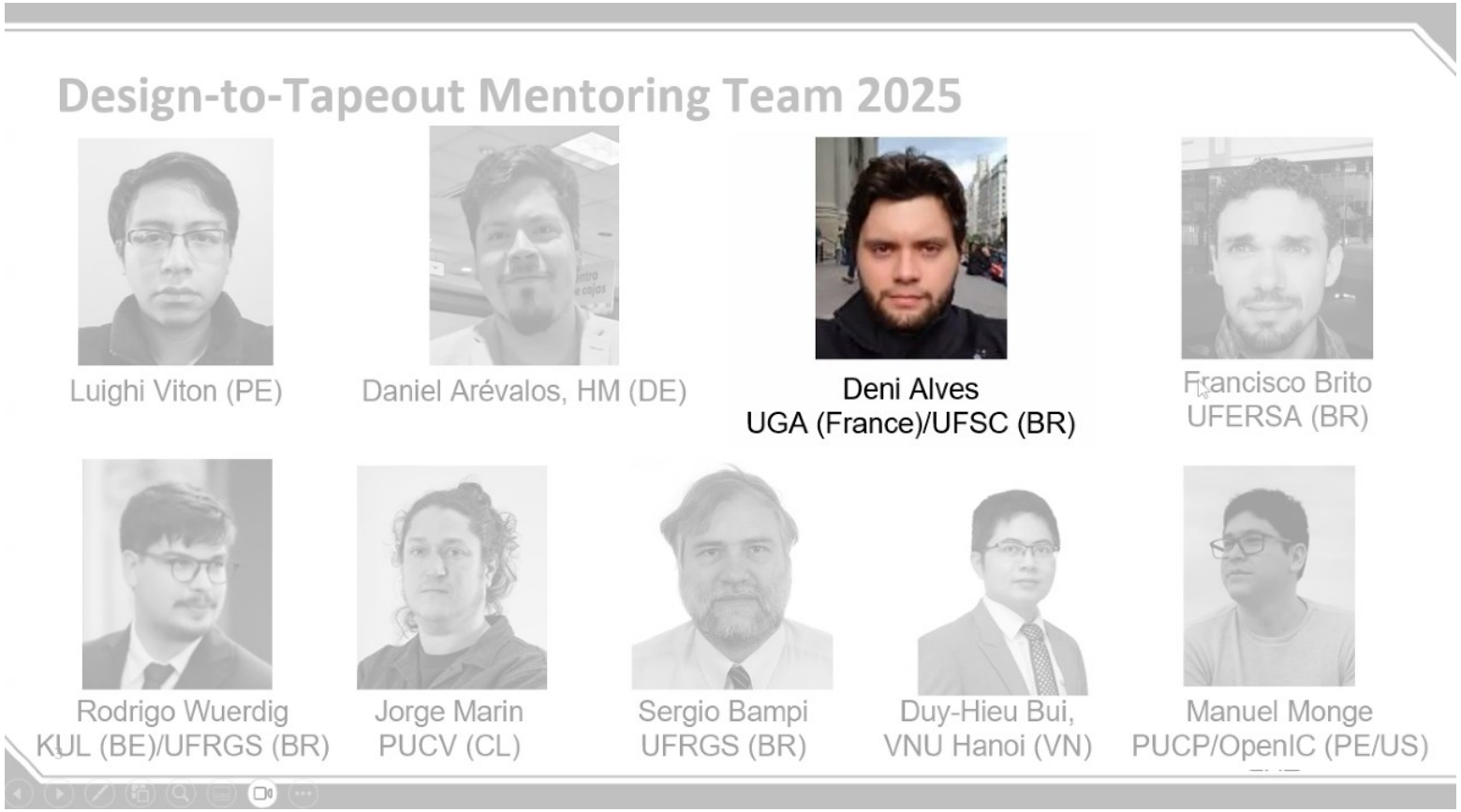
- SG13G2 is a high performance BiCMOS technology with a 0.13 µm CMOS process
- 2 gate oxides: A thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage
- PMOS and isolated NMOS transistors are offered
- Passive components like poly silicon resistors and MIM capacitors are available
- 5 thin metal layers, two thick metal layers (2 and 3 µm thick) and a MIM layer

UNIC-CASS: Mentoring

- IHP process
- Tool support
- Sim support
- Chip top

Exclusive mentor

Gabriel Maranhão
IMEC (Belgium)



UNIC-CASS: Mentoring

Weekly mentoring sessions (1)

Activities	Date/ Deadline	Purpose/ comments	Your Deliverables (provide info/links on your GitHub)	We will provide/handle
1st Meet-up	Dec 4, TBD UTC	Kick-off meeting	N/A	N/A
Biweekly meet-ups. 1st round	11/12,25/12,8/1, 22/1 **1 - 2 pm UTC (8am Eastern Time)**	Short presentations on topics such as IHP technology, UNIC-CASS Docker, best practices and pitfalls to avoid for both analog and digital. Mentoring and Design groups to present progress.	N/A	Slides and videos will be posted on the UNI-CASS website
1st Design submission [Mock tape-out]	Jan 19	Prepare the teams in advance for the final tape-out phase	Passing mock tapeout report	1. Detailed instructions for mock tapeout 2. Example files
1st Design Review & Feedback	Jan 22	Provide feedback and advice for the next stages	N/A	Feedback on the mock tapeout work
Bieekly meet-ups, 2nd round	6/2, 20/2, 6/3, 20/3 **1 - 2 pm UTC (8am Eastern Time)**	Focused mentoring + preparation for final tape-out + evaluate status of potential drop-outs	N/A	Slides and videos will be posted on the UNI-CASS website

UNIC-CASS: Mentoring

Weekly mentoring sessions (2)

Activities	Date/ Deadline	Purpose/ comments	Your Deliverables (provide info/links on your GitHub)	We will provide/handle
2nd Design submission	Mar 2	Verify feasibility of designs and top integration	Detailed circuit description (pinout, area and functionality) + DRC/LVS reports of top design	Check reports to confirm all blocks are LVS and DRC clean.
2nd Design Review & Feedback from mentors	Mar 6	Provide feedback and advice for the final stages	N/A	Feedback on the individual designs + advice for top merge
IHP pre-check + tapeout	Mar 27	Complete tape-out work on IHP platform	Deliver COMPLETE multiproject chip drop-ins to IHP final check	Provide assitance to tape-out leaders within the teams
Tape-out	Mar 30	See: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/low-cost-open-source-mpw-access-1	N/A	List of winner teams included in this tapeout List of unfinished designs to candidate for 2026 UNIC-CASS program
Chip delivery date	October 2026	TBD	N/A	Chip shipping and testing logistics

UNIC-CASS: Mentoring

Specific mentoring sessions

- IHP PDK + environment → Krzysztof Herman (IHP)
- Educational material → Duy-hieu Biu (VNU Hanoi, Vietnam)
- Digital Flow → Rodrigo Wuerdig + Daniel Arévalos
- Analog Flow → Deni Alves + Jorge Marin
- Tapeout pitfalls and best practices in IC design → Manuel Monge
- Other sessions? We are open to proposals!