UNIC-CASS 2025 Design-to-Tapeout Mentoring Kick-off session

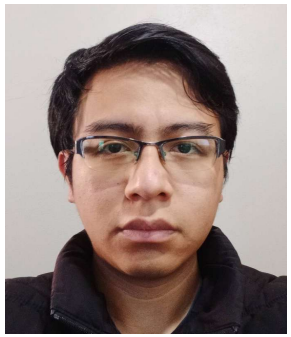
Dec 4, 2025

UNIC-CASS
Universalization of IC Design from IEEE CASS

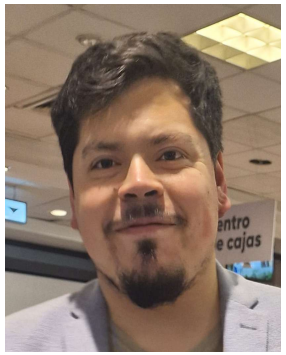
Topics

- Design-to-tapeout mentoring info and team
- Mentoring sessions and milestones schedule
- Top integration example

Design-to-Tapeout Mentoring Team 2025

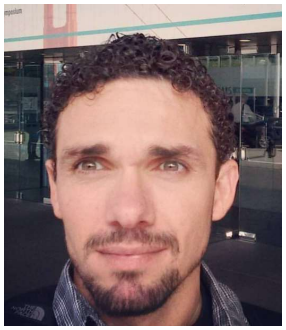


Luighi Viton (PE)



Daniel Arévalos, HM (DE)

Deni Alves
UGA (France)/UFSC (BR)



Francisco Brito
UFERSA (BR)

Rodrigo Wuerdig
KUL (BE)/UFRGS (BR)

Jorge Marin
PUCV (CL)

Sergio Bampi
UFRGS (BR)

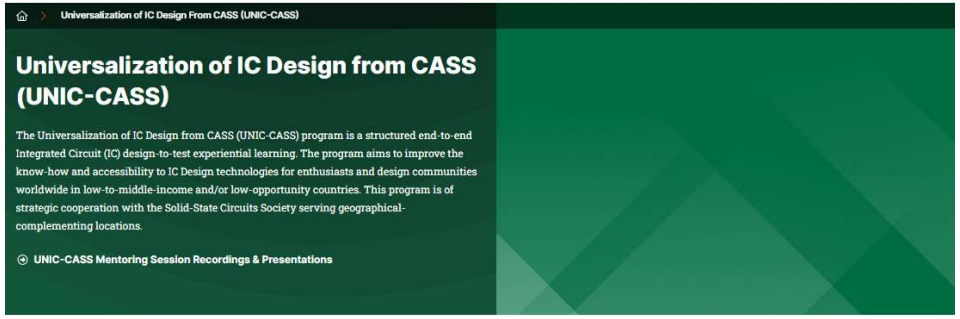
Duy-Hieu Bui,
VNU Hanoi (VN)

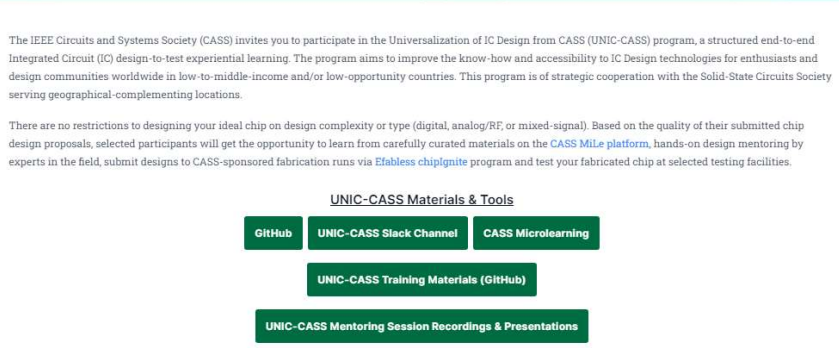
Manuel Monge
PUCP/OpenIC (PE/US)

Design-to-Tapeout Mentoring

Communication and organization

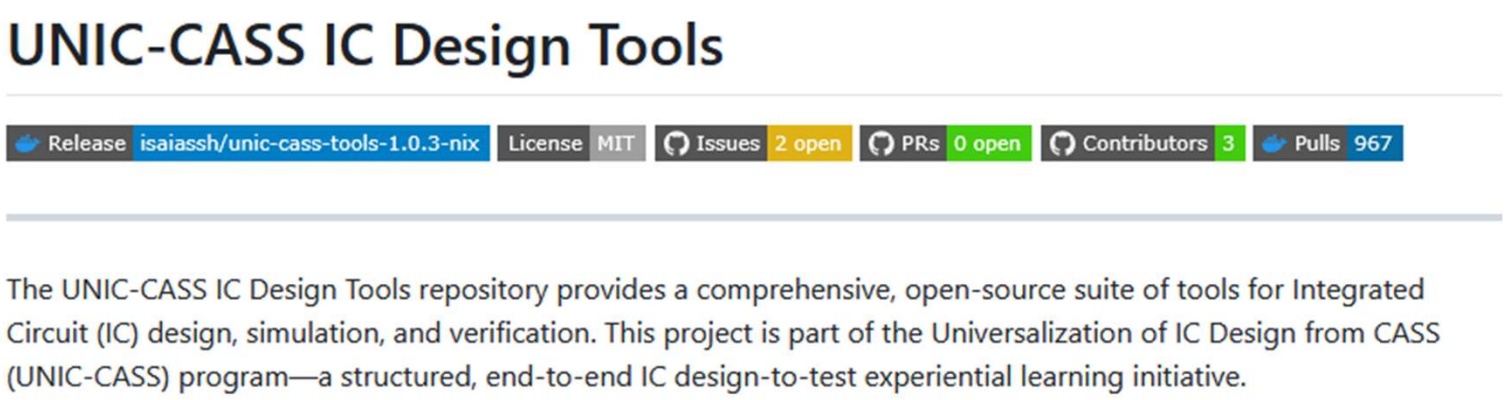
- Bi-weekly mentoring sessions
  - Separate meetings close to tapeout
- Element Channel
  - http://fossi-chat.org/
  - #unic-cass-2025 channel
  - Direct link: https://matrix.to/#/#unic-cass-2025:fossi-chat.org
- UNIC-CASS website





Recordings and presentations: https://ieee-cas.org/unic-cass-mentoring-session-recordings-presentations

[New] UNIC-CASS IC design tools Docker



- https://github.com/unic-cass/uniccass-icdesign-tools
- Includes main design tools for analog + digital OS design flows
- Lightweight + tapeout-verified

Main Design-to-tapeout milestones

- First design review (mock tapeout)
  - Purpose: Prepare the teams in advance for the final tape-out phase
    - **GO/NOGO milestone!**
  - Date: Jan 19
- Second design review (first DRC/LVS clean design delivery)
  - Purpose: Verify feasibility of designs and top integration
    - **GO/NOGO milestone!**
  - Date: Mar 9
- UNIC-CASS tapeout
  - Purpose: Final delivery of top designs (GDS+schematic+checks)
  - Date: Mar 27

Design-to-Tapeout Mentoring

Weekly mentoring sessions (1)

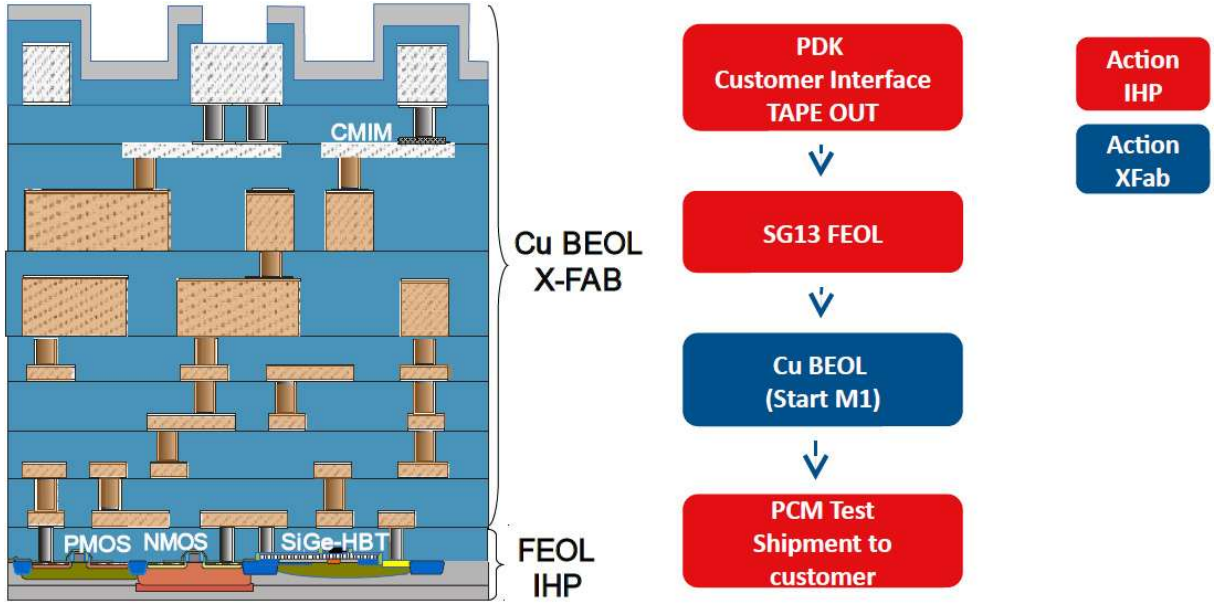
Activities	Date/ Deadline	Purpose/ comments	Your Deliverables (provide info/links on your GitHub)	We will provide/handle
1st Meet-up	Dec 4, TBD UTC	Kick-off meeting	N/A	N/A
Biweekly meet-ups. 1st round	11/12,25/12,8/1, 22/1 **1 - 2 pm UTC (8am Eastern Time)**	Short presentations on topics such as IHP technology, UNIC-CASS Docker, best practices and pitfalls to avoid for both analog and digital. Mentoring and Design groups to present progress.	N/A	Slides and videos will be posted on the UNI-CASS website
1st Design submission [Mock tape-out]	Jan 19	Prepare the teams in advance for the final tape-out phase	Passing mock tapeout report	1. Detailed instructions for mock tapeout 2. Example files
1st Design Review & Feedback	Jan 22	Provide feedback and advice for the next stages	N/A	Feedback on the mock tapeout work
Bieekly meet-ups, 2nd round	6/2, 20/2, 6/3, 20/3 **1 - 2 pm UTC (8am Eastern Time)**	Focused mentoring + preparation for final tape-out + evaluate status of potential drop-outs	N/A	Slides and videos will be posted on the UNI-CASS website

Design-to-Tapeout Mentoring [UPDATE]

Weekly mentoring sessions (2)

Activities	Date/ Deadline	Purpose/ comments	Your Deliverables (provide info/links on your GitHub)	We will provide/handle
2nd Design submission	Mar 2	Verify feasibility of designs and top integration	Detailed circuit description (pinout, area and functionality) + DRC/LVS reports of top design	Check reports to confirm all blocks are LVS and DRC clean.
2nd Design Review & Feedback from mentors	Mar 6	Provide feedback and advice for the final stages	N/A	Feedback on the individual designs + advice for top merge
IHP pre-check + tapeout	Mar 27	Complete tape-out work on IHP platform	Deliver COMPLETE multiproject chip drop-ins to IHP final check	Provide assitance to tape-out leaders within the teams
Tape-out	Mar 30	See: https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/low-cost-open-source-mpw-access-1	N/A	List of winner teams included in this tapeout List of unfinished designs to candidate for 2026 UNIC-CASS program
Chip delivery date	October 2026	TBD	N/A	Chip shipping and testing logistics

[New] IHP 130nm CMOS technology



- https://www.ihp-microelectronics.com/services/research-and-prototyping-service/mpw-prototyping-service/sigec-bicmos-technologies
- https://github.com/IHP-GmbH/IHP-Open-PDK

[New] IHP 130nm CMOS technology

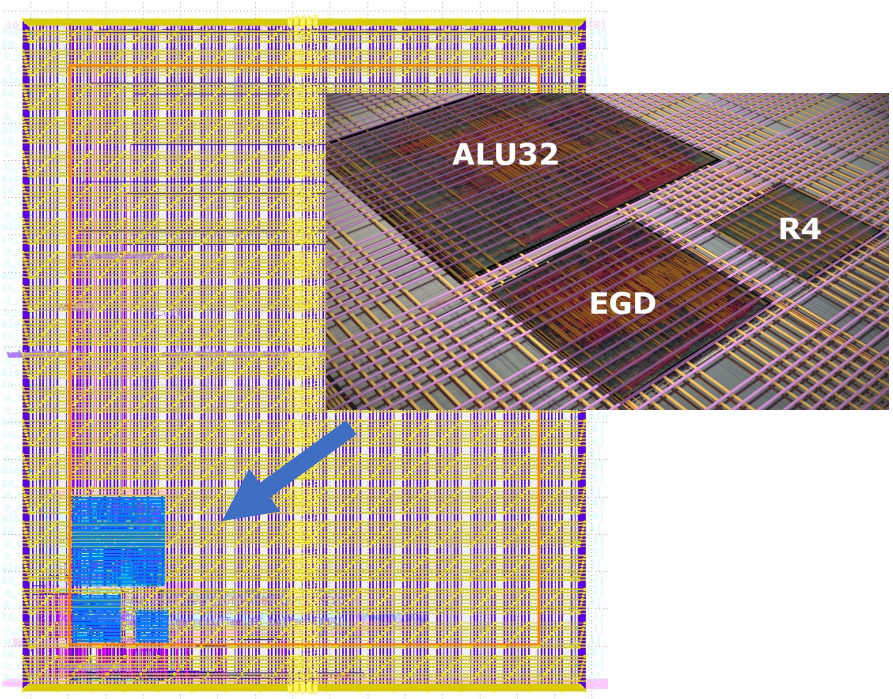
- SG13G2 is a high performance BiCMOS technology with a 0.13 µm CMOS process
- 2 gate oxides: A thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage
- PMOS and isolated NMOS transistors are offered
- Passive components like poly silicon resistors and MIM capacitors are available
- 5 thin metal layers, two thick metal layers (2 and 3 µm thick) and a MIM layer

Specific mentoring sessions

- IHP PDK + environment → Krzysztof Herman (IHP)
- Educational material → Duy-hieu Biu (VNU Hanoi, Vietnam)
- Digital Flow → Rodrigo Wuerdig + Daniel Arévalos
- Analog Flow → Deni Alves + Jorge Marin
- Tapeout pitfalls and best practices in IC design → Manuel Monge
- Other sessions? We are open to proposals!

Top-level integration

Example: IC4 – CASS @UNIC-CASS2023



- Decide on teams per chip (normally analog/digital division)
  - Area + pin count protocol/discussion
- Pad ring team
- Decide on top level leaders (from teams and from mentoring team)