PROJECT - I

EE 619A: VLSI SYSTEM DESIGN

BACKEND DESIGN FOR MIXED-SIGNAL IC

GROUP NAME: Backbench Designers

GROUP MEMBERS:

- Akshay Mehta - 190095 - akshaym@iitk.ac.in
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DESIGN RESPONSIBILITY:

- Frequency estimation module and Testbench modification: N Bhuvan
- Serial data implementation in Backend module: Akshay Mehta
- Backend module and Testbench modification: Bibek Lakra

SUMMARY:

- Designed a Backend for initializing analog modules correctly. Backend also consists of frequency estimator, which can find the frequency of an unknown clock.
- Integrated all these functionalities into a single module (Backend).
- Backend module (1.1 + 1.2) consists of serial data communication logic (1.3) and Frequency estimation logic (1.4).
- The frequency estimator has a precision upto 0.001 MHz.