Data Management Plan

The outcomes and results of the proposed research will be disseminated broadly, at all stages of the project.

I Types of data

The PIs expect that this research will result in several conference and journal papers, and possibly specialized thematic tutorials. The research work on the project will also result in simulator source code, measurement data, calibration data, and possibly demos.

II Standards for data

The publications will be in the Adobe Acrobat document format. All numerical results presented in the papers (either as plots or tables) will be in either Excel or Origin format, and instructions on how to use these files will be detailed in an accompanying readme.txt file.

The source code for software (simulators, microbenchmarks, snippet construction, computing weights, etc.) for will be in C/C++, MATLAB, Perl, Java, Python, and possibly other well-known and widely available programming languages, and will be in source code format with appropriate file names and extensions (.c, .cpp, .m, .pl, etc.). Assembler (ARM and RISC-V) source code is also likely to be used in microbenchmarks for obtaining empirically-derived per-event snippets and for computing/adjusting weights for snippets generated from circuit-level simulation. Such assembler source code will use ARM, RISC-V, x86, and possibly other well-known and well-documented instruction

The results of simulations and measurements will be in text format, spreadsheet (Excel or comma-separated .csv), JSON, or in the (text-based) formats used by each simulator. Measurement and calibration data will be in JSON format for metadata, while recorded (digitized) signals and signal samples with the MATLAB.m format and the GNU Radio stream-of-samples format, which are the formats used by measurement instruments and Software-Defined Radios to save such data.

The source code for hardware description, e.g. RTL for processors used in evaluation and calibration (Task 4) and building blocks for circuit-level simulation in Task 2 will be in Verilog and VHDL hardware description languages.

III Policies for access and sharing

The PIs plan to use their websites for rapid and broad dissemination of the ideas and results of this project. All publications will be available on the web site with the appropriate copyright notices regarding where these papers are published. All numerical results presented in the papers will be available on-line after the paper is published. The source code and result files will be made publicly available after the corresponding papers have been accepted for publication.

IV Policies and provisions for re-use and re-distribution

The material available on the PIs' websites can be used, with appropriate citations of the corresponding web site or journal/conference article. The materials from this project will be maintained for at least 5 years after the completion of the project.