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Effects of deposition temperature on the electrical properties of Ti/SiC Schottky barrier diodes

Tom N. Oder; Krishna C. Kundeti; Nicholas Borucki; Sundar B. Isukapati

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Effects of deposition temperature on the electrical properties of Ti/SiC Schottky barrier diodes

Tom N. Oder,[a] Krishna C. Kundeti, Nicholas Borucki, and Sundar B. Isukapati
Department of Physics and Astronomy, Youngstown State University, Youngstown, OH 44555, U.S.A.

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Ti Schottky contacts were deposited on n-type 4H-SiC at different temperatures ranging from 28 °C to 900 °C using a magnetron sputtering deposition system to fabricate Schottky barrier diodes. Post deposition annealing at 500 °C for up to 60 hours in vacuum was carried to further improve the contact properties. Optimum barrier height of 1.13 eV and ideality factor of 1.04 was obtained in contacts deposited at 200 °C and annealed for 60 hours. Under a reverse voltage bias of 400 V, the average leakage current on these set of diodes was 6.6 x 10^{-8} A. Based on the x-ray diffraction analysis, TiC, Ti_5Si_3 and Ti_3SiC_2 were formed at the Ti/SiC interface. These results could be beneficial to improving the performance of 4H-SiC Schottky diodes for high power and high temperature applications. https://doi.org/10.1063/1.4985841

I. INTRODUCTION

A large number of electronics essential to our everyday life such as remote actuators, distributed high power control systems, avionics, automotive and geophysical electronic systems require functionality at high temperatures. Electronics fabricated with traditional semiconductors such as silicon (Si) if operated at temperatures above 125 °C require elaborate cooling systems that introduce serious drawbacks including addition of a substantial amount of weight, which lowers their efficiency and reliability. It is now widely accepted that the development of electronic systems capable of high temperature operations above 300°C without the need for cooling is a critical necessity for current and future technology.[1] Devices, such as Schottky barrier diodes (SBD), made from wide band gap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) are being developed for high temperature and high power applications. Schottky barrier diodes are widely used in power supply circuits, mixers, detectors, sensors and other high frequency applications on account of their low conduction loss and close to zero reverse recovery time when compared with p-n junction diodes. These benefits are easily extensible to the metal semiconductor field effect transistors (MESFETs) which employ Schottky contacts and which are attractive for microwave circuits, power amplifiers, and wireless communications.[2]

The electrical properties of Schottky diodes can be extracted from the thermionic emission theory where the applied forward voltage V_F and the forward current density J_F (forward current per unit surface area of the diode) are related by the expression:

$$V_F = \frac{nkT}{q}\ln\left(\frac{J_F}{A^{**}T^2}\right) + n\phi_B + RJ_F \tag{1}$$

where n is the ideality factor, k is the Boltzmann constant, T is the temperature, A^{**} is the effective Richardson constant (= 146 $Acm^{-2}K^{-2}$ for 4H-SiC), Φ_b is the Schottky barrier height (SBH) and R is the resistance of the drift region.[3,4] The value of n and Φ_b are obtained from the linear fit of the graph of $\ln(J_F)$ versus V_F. An ideal Schottky barrier diode (with $n \approx 1$) should also have a small

[a]E-MAIL: tnoder@ysu.edu, PHONE (330) 941-7111, FAX (330) 941-3121

forward voltage to minimize conduction loss, enhance switching speed and generally improve the efficiency of the system during the "on" state. This implies that a low value of V_F is achieved by a combination of low barrier height and small on-resistance. Furthermore, an ideal Schottky diode should have a small value of leakage current density J_{sat} under reverse bias ("off" state) which is given by the relation

$$J_{sat} = A^{**}T^2 \exp\left(\frac{-\Phi_B}{\kappa T}\right) \tag{2}$$

Therefore, a high value of Schottky barrier height relates to reduction of the reverse leakage current density, hence results in a high reverse breakdown voltage. A diode of high or low barrier height is thus selected based on whether the forward or reverse characteristics are of higher importance.

The Schottky-Mott theory is used to predict the energy barrier (Φ_b) to the flow of electrons across the metal/semiconductor interface. For n-type semiconductors, this is obtained by the relation:

$$\Phi_b = \varphi_m - \chi_S \tag{3}$$

where φ_m is the work function of the metal and χ_S is the electron affinity of the semiconductor.[5,6] Titanium (Ti) is the metal commonly used as Schottky contact in n-type 4H-SiC because of its low barrier height, resulting in low forward voltage.[7–9] With a work function of 4.33 eV for Ti and an electron affinity of 3.24 eV for 4H-SiC, the barrier height of Ti/4H-SiC contact is expected to be 1.09 eV.[10,11] However, further improvements are still desired to address the many factors arising that affect the quality of the Ti/SiC interface and lead to increase in reverse leakage current and low forward current. Some of the factors that cause non-uniform or inhomogeneous characteristics include undesired contaminations and reaction products at the interface, variation in doping concentration and structural defects of the semiconductor.[12] Post deposition annealing is one of the methods that have been studied to improve the electrical characteristics of Ti/SiC SBDs. This is believed to flatten double barriers and improve the ideality of the diodes.[13] Han *et al.* characterized Ti/SiC Schottky contacts annealed at different temperatures and found those annealed at 500 ^oC for 5 min in N_2 exhibited the least amount of inhomogeneity.[7] Kyoung *et al.* and Kim *et al.* similarly reported improvement of Ti/SiC contacts using post deposition thermal treatment.[9,14] Roccaforte *et al.* performed ion irradiation of Ni/Ti bilayer on SiC contacts and observed a significant improvement in its electrical properties which was linked to deactivation of dopants in the SiC material at the interface.[8] Our group previously reported improvement of SiC Schottky diodes by depositing various metal contacts at elevated temperatures.[15–17] Improvements in the contacts were explained in terms of removal of unwanted oxides at the interface and the formation of silicides with higher work functions. In this paper, we investigated the effect of Ti Schottky contact deposition temperature on the Ti/SiC Schottky barrier diodes, which, as far as we know, has not yet been conducted. The Ti films were deposited on *n*-type 4H-SiC substrates held at different temperatures from 25 ^oC to 900 ^oC. The results showed that diodes with the contacts deposited at 200 ^oC yield optimum *I-V* characteristics consisting of larger barrier height of 1.13 eV, ideality factor of 1.04 and a leakage current of 6.60 x 10^{-8} A measured at -400 V. Furthermore, the diode with the contact deposited at 200 ^oC maintains its rectifying ability at higher temperatures. The interface region was found to consist of TiC, Ti_6Si_3 and Ti_3SiC_2.

II. EXPERIMENT

The *n*-type 4H-SiC wafer used in this study comprised two epitaxial layers grown 4^o off the basal (0001) plane; one was 0.5 μm thick, with $N_d \sim 1.0 \times 10^{18}$ cm^{-3} and the second one was 11.7 μm thick with $N_d \sim 5.1 \times 10^{15}$ cm^{-3}. These were grown on a 400 μm-thick *n*-type SiC substrate of resistivity 0.019 Ω-cm. This material was supplied by Cree, Inc. and a full description of the wafer surface preparation and back-side ohmic contact preparation carried can be found in Ref. 15. On the front (epilayer) side of the samples, about 200 nm-thick Ti film was deposited at different temperatures (28 ^oC, 200 ^oC, 400 ^oC, 500 ^oC, 700 ^oC and 900 ^oC) from a 99.995% purity 2-inch target through a stainless steel shadow mask consisting of circular holes of 600 μm in diameter. Post-deposition annealing was performed on these samples in vacuum at 500 ^oC under a pressure of 2 x 10^{-7} Torr for a total of 60 hours. The samples were periodically removed for current-voltage

(I-V) and capacitance-voltage (C-V) measurements. Each sample was then diced into 2 pieces, one for current-voltage-temperature (I-V-T) measurements and the other for microstructural characterization. A Keithley 2400 sourcemeter was used to collect the I-V data, while the Agilent LCR precision meter was used for the C-V measurements. For the I-V-T measurements, the samples were held at different temperatures from 25 °C to 500 °C in steps of 25 °C while the I-V data were collected. The film microstructures were investigated by x-ray diffraction (XRD) measurements using the Bruker-Prospector diffractometer (Bruker AXS, Inc., Madison, Wisconsin, USA) with a high brightness Cu Incoatec microsource.

III. RESULTS AND DISCUSSIONS

Figure 1 shows the cross section scanning electron microscope (SEM) image of the as-deposited Ti contact, deposited at 400 °C on SiC. The measured Ti film thickness was 184 nm, which is about the same value found for all the samples studied and is close to the desired value of 200 nm. Figure 2 shows J_F-V_F plots of diodes with as-deposited Ti contact deposited at different substrate temperatures from 28 °C to 900 °C. It can be seen that the linear portion of the diodes with the contacts deposited at 28 °C - 500 °C cover 6 decades of current range, a sign of good quality diodes.

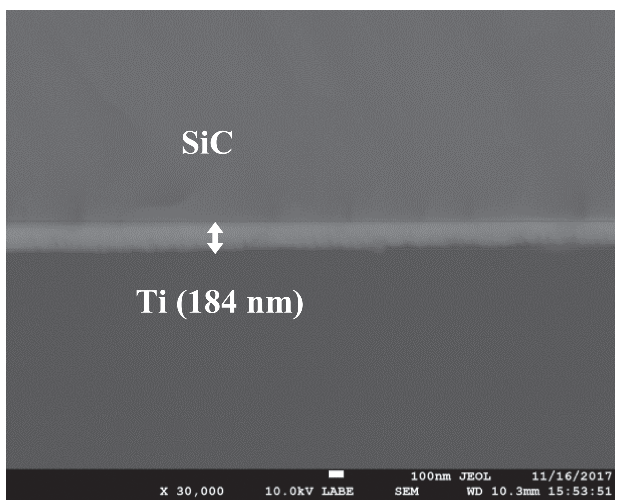

FIG. 1. SEM image of Ti/SiC cross-section.

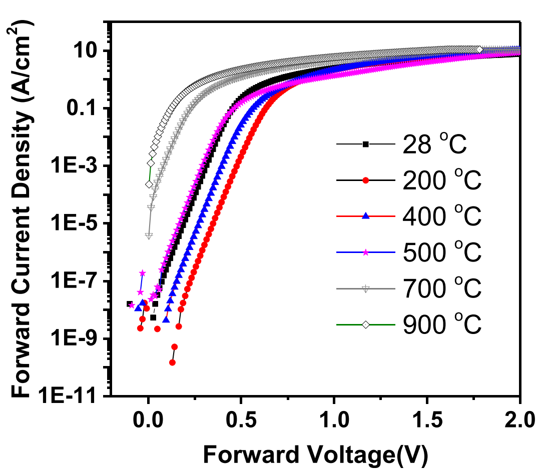

FIG. 2. J_F-V_F plot of diodes with as-deposited Ti contact deposited at different substrate temperatures from 28 °C to 900 °C.

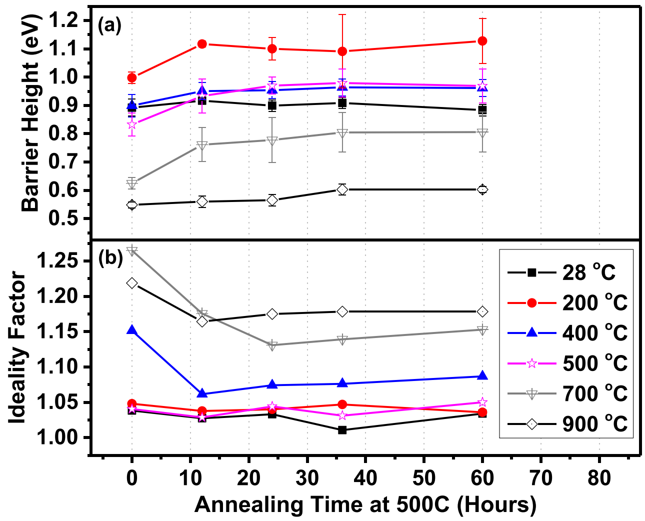

FIG. 3. Plots showing variation of (a) barrier height and (b) ideality factor with post deposition annealing time from diodes with Ti contacts deposited at different substrate temperatures from 28 °C to 900 °C.

Figure 3 shows the plots of (a) barrier height and (b) ideality factor with post deposition annealing time from the diodes with Ti contacts deposited at different substrate temperatures from 28 °C to 900 °C. Each data point represents an average value obtained from measurements taken on five diodes, with 1- 10% deviation from the mean values. The first observation that can be made from these plots is that substrate temperatures of 28 °C - 500 °C produce diodes with low ideality factors (1.01 – 1.15) and higher barrier heights (0.83 – 1.13 eV). Diodes with contacts deposited at 700 °C and 900 °C show higher ideality factors and lower barrier heights, indicative of poorer rectifying qualities. Secondly, the optimum post deposition annealing time is achieved within the first 12 hours. Thirdly, the diode with the Ti contact deposited at 200 °C has the best overall forward *I-V* qualities with an average barrier height of 1.13 eV and ideality factor of 1.04.

The specific on-resistance R_{on} of the diodes were extracted by differentiating equation (1) with respect to the forward current I_F and rearranging to get

$$\frac{dV_F}{d\ln(I_F)} = I_F R + \frac{nkT}{q} \tag{4}$$

The series resistance is the slope of the graph of $dV/d\ln(I_F)$ plotted against I_F. The specific on-resistance (R_{on}) is determined by taking the product of the series resistance and the area of the Schottky contact. Values of R_{on}, determined from the *I-V* data taken at room temperature of the as-deposited samples are shown in figure 4. Note here that R_{on} for contacts deposited at temperatures ≤ 500 °C have lower values within 8 – 10 mΩ-cm^2. The inset in figure 4 shows a representative plot of $dV/d\ln(I_F)$ versus I_F of a diode with the Ti contacts deposited at 200 °C, yielding a series resistance of 3.05 Ω and R_{on} of 8.60 mΩ-cm^2. The R^2 correlation coefficient of the linear fitting in this plot has a value of 0.9995, indicating an excellent linear fit. This figure also shows the results of the reverse biased characteristics, determined by measuring the saturation current (I_{sat}) at -400 V. These results indicate that the diode with the Ti contact deposited at 200 °C has the smallest leakage current of 6.6 x 10^{-8} A. The leakage current for diodes with the contact deposited at 28 °C and 900 °C are not shown in the plot because they exhibited reverse break down at values less than 350 V.

The data of the capacitance (C) obtained from applied negative DC voltage (V) were analyzed using the relation

$$\left(\frac{A}{C}\right)^2 = \frac{2(V_{bi} - kT/q)}{q\varepsilon_S N_D} + \frac{2\,|V|}{q\varepsilon_S N_D} \tag{5}$$

where A is the area of the Schottky contact, V_{bi} is the built-in potential, ε_{S} is the semiconductor dielectric constant (9.66 for 4H-SiC), N_{D} is the doping concentration of the semiconductor and

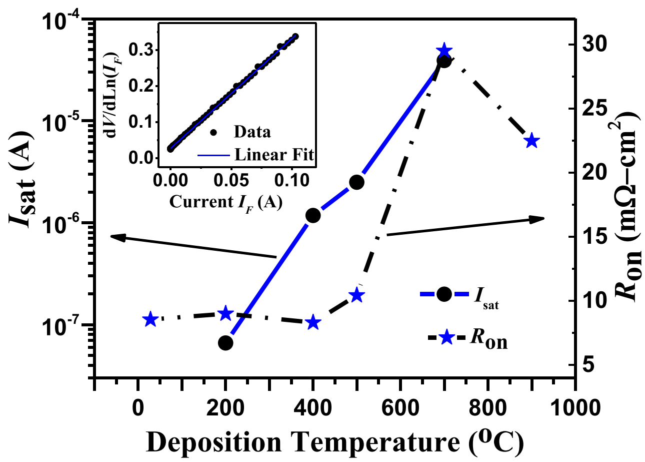

FIG. 4. A plot showing the variation of the specific on-resistance (R_{on}) and saturation current density (I_{sat}) with deposition temperature. The inset shows a plot of $dV/d[\ln(I_F)]$ versus current used to obtain R_{on}.

kT is the thermal energy.[3,5,18,19] Details of the measurements and data analysis are described in Refs. 15 and 16. Figure 5 shows a plot of $(A/C)^2$ versus V for one of the Ti/SiC diode with the contact deposited at 200 °C and annealed for 12 hours at 500 °C in vacuum. The correlation coefficient (R^2 value) obtained from this plot was 0.9999, indicating an excellent linear fit. Analysis of the C-V data yields a barrier height of 1.26 eV, which is larger than the value obtained from the I-V data as the latter is reduced by image force phenomena and inhomogeneities at the metal/SiC interface. The average value of the donor density (N_D) was found to be 8.8 x 10^{15} cm^{-3}, which compares well with the value 5.1 x 10^{15} cm^{-3} specified by Cree, Inc.

Figure 6 shows the J_F-V-T plot of the diode with the Schottky contact deposited at 200 °C and annealed at 500 °C for 60 hours in vacuum. The measurements were taken at different temperatures from 25 °C to 500 °C in steps of 25 °C. As can be seen in the highlighted plot, the graph of the data taken while the sample was held at 300 °C shows good rectifying characteristics, with 2 decades of linearity in the $\ln(J_F)$ range, indicating high thermal stability.

From equation (1), the saturation current (I_{sat}) calculated from the linear intercept of the $\ln(I_F)$ versus V at $V = 0$ can be expressed as

$$I_{sat} = AA^*T^2 \exp\left(-\frac{\Phi_b}{kT}\right) \quad \text{or} \quad Ln\left(\frac{I_{sat}}{T^2}\right) = Ln(AA^*) - \frac{\Phi_b}{kT} \tag{6}$$

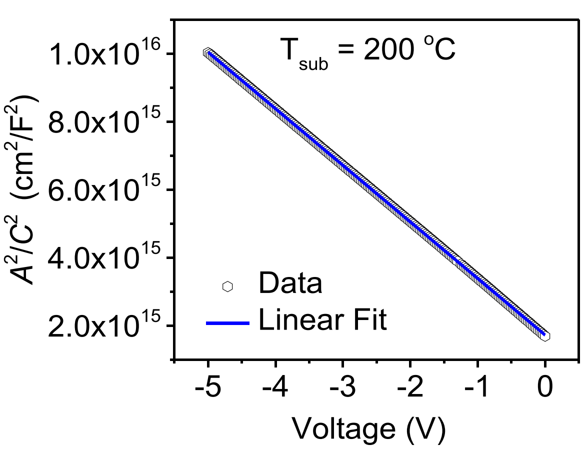

FIG. 5. A plot of $(A/C)^2$ versus Voltage for a diode with Ti contact deposited at 200 °C and annealed for 12 hours at 500 °C in vacuum.

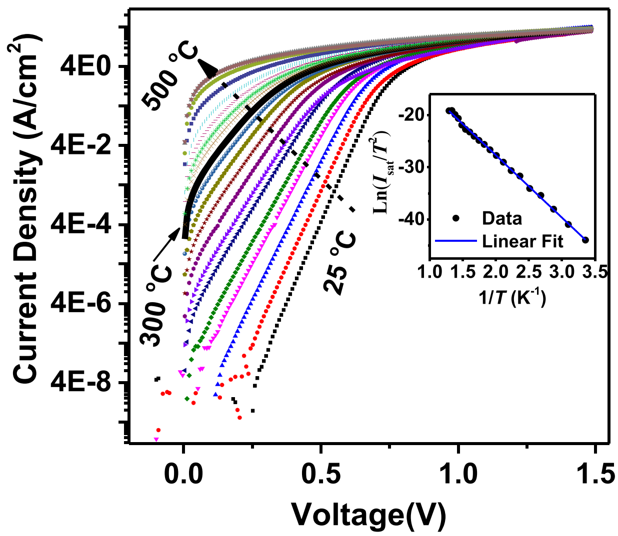

FIG. 6. Plot of J_F-V characteristics taken at different temperatures from 25 °C to 500 °C in steps of 25 °C of diodes with Ti contacts deposited at 200 °C. The inset shows the Richardson plot of $\ln(I_{sat}/T^2)$ versus $1/T$ for this contact.

From this expression, the Richardson's plot of $\ln(I_{sat}/T^2)$ versus $1/kT$ is linear, out of which the barrier height and Richardson's constant can be obtained. The inset in figure 6 shows the Richardson's plot of a diode with the contact deposited at 200 °C and annealed at 500 °C for 60 hours. The R^2 value of the linear fit of this plot is 0.9983, also indicating the data fits very close to a linear trend. The "effective" or "zero bias" barrier height extracted from this plot is 1.03 eV, which is close to the theoretically predicted value of 1.09 eV, but less than the value of 1.13 eV obtained from the *I-V* measurements plotted in Figure 3. The value of Richardson's constant extracted is 8.53 Acm^{-2}K^{-2}, which is much smaller than the theoretical value of 146 Acm^{-2}K^{-2}. The small value of the extracted Richardson's constant is interpreted as an indication that the actual area of the contact is much smaller than the device area.[4,7,20]

The structural composition of the interface between the Ti and SiC was investigated by *x*-ray diffraction (XRD) measurements, performed on each of the six Ti Schottky metal contacts deposited at 28 °C to 900 °C. The XRD scans were performed on four Schottky contacts on each sample and it was verified that the scans from each sample were consistent. Figure 7 shows the 2θ scans obtained from these samples. The main phases identified were TiC (111) with peaks at 35.4°, SiC (004) with peaks at 35.6°, Ti_5Si_3 (210) with peaks at 38°, Ti_3SiC_2 (008) with peaks at ~ 40° and Ti_5Si_3 (002) with peaks at 42°.[14,21–24] Previous studies of Ti/SiC carried by La Via *et al.* and by Porter *et al.* indicated that Ti reacts with SiC to form TiC layer at the interface and the freed Si atoms interact with Ti to form titanium silicide(s).[24,25] From these analyses, it is believed that heat treatment at

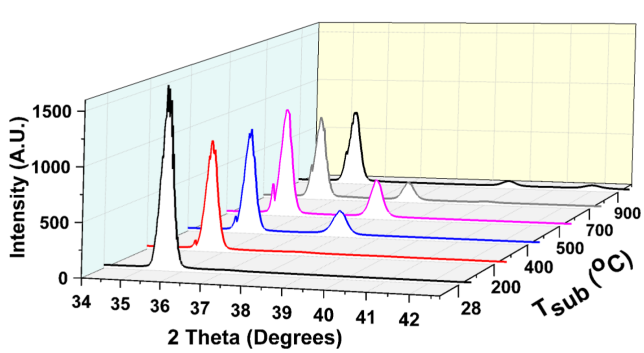

FIG. 7. XRD intensity scans of diodes with Ti contacts deposited at different substrate temperatures from 28 °C to 900 °C.

750°C leads to formation of TiC (111) at the interface and Ti_5Si_3 (210) is generated between TiC (111) and Ti. The work functions of TiC (4.6 eV) is higher than that of Ti (4.33 eV) and Ti_5Si_3 (4.2 eV).[26,27] Kim et al., reported that the work function of TiC depends on the deposition temperature and decreases from 5.2 eV at $T_{sub} = 250\ ^{o}C$ to about 4.5 eV at $T_{sub} = 550\ ^{o}C$.[27] Based on these results, it can be concluded that a substrate temperature of 200 ^{o}C would promote formation of TiC phase with a higher work function. The higher barrier height, as well as better reverse biased characteristics noted in the Schottky diodes formed with Ti contacts deposited at 200 ^{o}C could therefore arise from reaction products with larger work functions formed during deposition. In contrast, diodes with Ti contacts deposited at 700 ^{o}C and 900 ^{o}C have poorer forward and reverse characteristics due to the formation of carbides and silicides with lower work functions.

IV. CONCLUSION

In conclusion, Ti Schottky contacts were deposited on *n*-type SiC at temperatures from 28 ^{o}C – 900 ^{o}C. The contacts deposited at 200 ^{o}C produced diodes with optimum properties comprising an average barrier height as high as 1.13 eV and ideality factor of 1.04. In addition, these diodes exhibited very low leakage current and high temperature tolerance. These characteristics are attributed to the formation of TiC with a higher work function. As Ti is a common metal contact used in SiC Schottky diodes, the results from this investigation could provide further improvement in the performance of 4H-SiC Schottky diodes for high power and high temperature applications.

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[1] P. G. Neudeck, R. S. Okojie, and L. Y. Chen, Proceedings of the IEEE **90**(6), 1065 (2002).
[2] Y. Yang, B. Duan, and X. Zhang, *Physics and Technology of Silicon Carbide Devices*, Edited by Y. Hijikata (InTech, DOI: 10.5772/51085, 2012), pp. 291–311. Available from: https://www.intechopen.com/books/physics-and-technology-of-silicon-carbide-devices/silicon-carbide-power-mesfet.
[3] A. Itoh, T. Kimoto, and H. Matsunami, IEEE Electron. Dev. Lett. **16**, 280 (1995).
[4] F. Roccaforte, F. La Via, V. Raineri, R. Pierobon, and E. Zanoni, J. Appl. Phys. **93**, 9137 (2003).
[5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd Edition (John Wiley and Sons, New York, 1981), pp. 254–258.
[6] E. H. Rhoderick and R. H. Williams, *Metal-Semiconductor Contacts*, 2nd Edition (Oxford, Clarendon, 1988), p. 35.
[7] L. C. Han, H. J. Shen, K. A. Liu, Y. Y. Wang, Y. D. Tang, Y. Bai, H. Y. Xu, Y. D. Wu, and X. Y. Liu, Chin. Phys. B **23**(12), 127302 (2014).
[8] F. Roccaforte, C. Bongiorno, F. La Via, and V. Raineri, Appl. Phys. Lett. **85**, 6152 (2004).
[9] S. Kyoung, E. S. Jung, and M. Y. Sung, Microelectronic Engineering **154**, 69 (2016).
[10] S.Yu. Davydov, Semiconductors **41**(6), 696 (2007).
[11] *Tables of Physical & Chemical Constants*, 16th Edition 1995 (Kaye & Laby Online Version 1.0, 2005), 4.3 Work function. Available at www.kayelaby.npl.co.uk.
[12] R. Pérez, N. Mestres, J. Montserrat, D. Tournier, and P. Godignon, Phys. Stat. Sol. (A) **202**(4), 692 (2005).
[13] S. U. Omar, T. S. Sudarshan, T. A. Rana, H. Song, and M. V. S. Chandrashekhar, J. Phys. D. Appl. Phys. **47**, 295102 (2014).
[14] D. H. Kim, J. H. Lee, J. H. Moon, M. S. Oh, H. K. Song, J. H. Yim, J. B. Lee, and H. J. Kim, Solid State Phenomena **124-126**, 105 (2007).
[15] T. N. Oder, T. L. Sung, M. Barlow, J. R. Williams, A. C. Ahyi, and T. Isaacs-Smith, J. Electron. Mater. **38**(6), 772 (2009).
[16] T. N. Oder, P. Martin, A. V. Adedeji, T. Isaacs-Smith, and J. R. Williams, J. Electron. Mater. **36**(7), 805 (2007).
[17] T. N. Oder, P. Martin, J. Y. Lin, H. X. Jiang, J. R. Williams, and T. Isaacs-Smith, Appl. Phys. Lett. **88**, 183505 (2006).
[18] D. K. Schroder, *Semiconductor Material and Device Characterization* (Wiley, New York, 1990).
[19] Y. A. Goldberg, M. Levinshtein, and S. L. Rumyantsev, *Properties of advanced semiconductor materials: GaN, AlN, InN, BN, SiC, SiGe*, Edited by M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur (John Wiley & Sons, Inc., New York-Chichester-Weinheim-Brisbane-Singapore-Toronto, 2001), Chapters 5, Silicon Carbide.
[20] A. F. Hamida, Z. Ouennoughi, A. Sellai, R. Weiss, and H. Ryssel, Semicond. Sci. Technol. **23**(4), 045005 (2008).
[21] H. Chao, Z. Y. Ming, S. Q. Wen, T. X. Yan, Z. Y. Men, G. Hui, and W. Y. Hu, Chinese Physics B **24**(11), 117304 (2015).
[22] X. Pang, X. Liu, and B. Jin, Journal of Nanomaterials **2014**, 286484.
[23] I. P. Nikitina, K. V. Vassilevski, A. B. Horsfall, N. G. Wright, A. G. O'Neill, C. M. Johnson, T. Yamamoto, and R. K. Malhan, Semiconductor Science and Technology **21**(7), 898 (2006).
[24] F. La Via, F. Roccaforte, A. Makhtari, V. Raineri, P. Musumeci, and L. Calcagno, Microelectronic Engineering **60**(1), 269 (2002).

[25] L. M. Porter, R. F. Davis, J. S. Bow, M. J. Kim, R. W. Carpenter, and R. C. Glass, Journal of Materials Research **10**(3), 668 (1995).
[26] H. Zhu, M. Aindow, and R. Ramprasad, Phys. Rev. B **80**, 201406(R) (2009).
[27] C. K. Kim, H. J. Ahn, J. M. Moon, S. Lee, D. H. Moon, J. S. Park, B. J. Cho, Y. K. Choi, and S. H. Lee, Solid State Electr. **114**, 90 (2015).