IMSAI 8080 Configuration Switch Settings

This is a draft document, please report errors, typos etc. on the forum (doc ver V4.1)

	15	14	13	12		11	10	9	8	l	7	6	5	4	l	3	2	1	0	l					
_	Reserved	Reserved	Reserved	Reserved		NVS_BANK_ROM	NVS_BOOT_ROM	NVS_BOOT_ROM	NVS_BOOT_ROM		NVS_UNLIMITED	NVS_4MHZ	NVS_NO_UNDOC	NVS_Z80		NVS_IF_STA	NVS_LOG_LEVEL	NVS_LOG_LEVEL	NVS_POST						
↑ dn	N/A	N/A	N/A	N/A	←d∩	ROM @ ADDR 0000H	ROM#	ROM#	ROM#	← d∩	Unlimited CPU speed	4MHz	No undoc op. codes	Z-80 CPU	← d∩	Station Mode (STA)	Boot Messages	Boot Messages	Enabled	←dn					
→ Down	N/A	N/A	N/A	N/A	← Down	ROM at START ADDR	ROM#	ROM#	ROM#	← Down	CPU speed from bit 6	2MHz	Allow undoc op. codes	8080 CPU	← Down	Access Point (AP)	Boot Messages	Boot Messages	Disabled	← Down					
																	$ \leftarrow \leftarrow \rightarrow \rightarrow $	↑ ↓ ↑			Informational Boot Messages Warning Boot Messages Error Boot Messages No Boot Messages				
ROM 7 @ 00	000H					\uparrow	\uparrow	\uparrow	\uparrow		\uparrow	1	\uparrow	\uparrow							Z-80 + Unlimited CPU Speed + Undoc OpCodes				
ROM 6 @ 00	ROM 6 @ 0000H					\uparrow	\uparrow	\uparrow	\downarrow		\uparrow	\downarrow	\uparrow	\uparrow							Z-80 + Unlimited CPU Speed + Undoc OpCodes				
ROM 5 @ 00	000H					\uparrow	\uparrow	\rightarrow	\uparrow		\downarrow	\uparrow	\uparrow	\uparrow							Z-80 + 4MHz CPU Speed + Undoc OpCodes				
ROM 4 @ 00	000H					\uparrow	\uparrow	\rightarrow	\rightarrow		\downarrow	\downarrow	\uparrow	\uparrow							Z-80 + 2MHz CPU Speed + Undoc OpCodes				
ROM 3 @ 00	ROM 3 @ 0000H							\uparrow	\uparrow		\uparrow	\uparrow	\uparrow	\downarrow							8080 + Unlimited CPU Speed + Undoc OpCodes				
ROM 2 @ 00					\uparrow	\downarrow	\uparrow	\rightarrow		\uparrow	\downarrow	\uparrow	\rightarrow							8080 + Unlimited CPU Speed + Undoc OpCodes					
ROM 1 @ 00	ROM 1 @ 0000H						\downarrow	\rightarrow	\uparrow		\rightarrow	\uparrow	\uparrow	\downarrow						8080 + 4MHz CPU Speed + Undoc OpCodes					
No ROM Mar	No ROM Mapped					\uparrow	\downarrow	\rightarrow	\rightarrow		\rightarrow	\downarrow	\uparrow	\downarrow						8080 + 2MHz CPU Speed + Undoc OpCodes					
ROM 7 @ ROM A	ROM 7 @ ROM ADDR						\uparrow		\uparrow		\uparrow	\uparrow	\downarrow	\uparrow						Z-80 + Unlimited CPU Speed + No Undoc OpCodes					
ROM 6 @ ROM A	ROM 6 @ ROM ADDR						\uparrow	←	\rightarrow	ĺ		\downarrow	\downarrow	\uparrow						Z-80 + Unlimited CPU Speed + No Undoc OpCodes					
ROM 5 @ ROM A	ROM 5 @ ROM ADDR			\downarrow			\uparrow	\rightarrow	\uparrow	l	\rightarrow	\uparrow	\downarrow	\uparrow						Z-80 + 4MHz CPU Speed + No Undoc OpCodes					
ROM 4 @ ROM A	ROM 4 @ ROM ADDR						\uparrow	\rightarrow	\rightarrow	l	\rightarrow	\downarrow	\downarrow	\uparrow						Z-80 + 2MHz CPU Speed + No Undoc OpCodes					
ROM 3 @ ROM A	ROM 3 @ ROM ADDR						\downarrow		\uparrow		\uparrow	\uparrow	\downarrow	\downarrow							8080 + Unlimited CPU Speed + No Undoc OpCodes				
ROM 2 @ ROM A	ROM 2 @ ROM ADDR					\downarrow	\downarrow		\rightarrow	Ī	\uparrow	\downarrow	\downarrow	\downarrow							8080 + Unlimited CPU Speed + No Undoc OpCodes				
ROM 1 @ ROM A	ROM 1 @ ROM ADDR					\rightarrow	\downarrow	\rightarrow	\uparrow	l	\rightarrow	\uparrow	\downarrow	\downarrow		8080 +					8080 + 4MHz CPU Speed + No Undoc OpCodes				
No ROM Map				\downarrow \downarrow \downarrow \downarrow					\downarrow	\downarrow	\downarrow	\downarrow							8080 + 2MHz CPU Speed + No Undoc OpCodes						

IMSAI 8080 Configuration Switch Example Settings

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15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N/A	W/N	W/N	W/N	ROM @ ADDR 0000H	ROM #	ROM #	ROM #	Unlimited CPU speed	zHW4	No undoc op. codes	N40 08-Z	Station Mode (STA)	Boot Messages	Boot Messages	POST Enabled
N/A	W/N	W/N	N/A	ROM at START ADDR	ROM #	ROM #	ROM #	CPU speed from bit 6	2MHz	Allow undoc op. codes	8080 CPU	Access Point (AP)	Boot Messages	Boot Messages	POST Disabled

Factory Default	The state of the s
-	V V V V V V V V V V V V V V V V V V V
CP/M 2.2 ROM	↑ ↑ ↑ ↑ ROM 1 @ Address 0000H/D800H + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ROM1=mpu-a-rom.hex
CP/M vio ROM	ROM 2 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
	V V V V V V V V V ROM2=mpu-a-vio-rom.hex
XYBASIC	ROM 5 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
	V V V V V A ROM5=xybasic.hex
8K MBASIC 1.4	ROM 4 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
	VVVVVVVVV AVVVV AVVVV ROM4=basic8k.hex
4K BASIC	ROM 3 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
	↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ROM3=basic4k.hex
No ROM Z-80	No ROM + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
No ROM 8080	No ROM + 2MHz + No Undocumented Opcodes + 8080 + STA Mode + No Error + No POST
DOM 7	DOM 7 @ DOM Address AMIII Undequenented Operator 790 CTA Mode No Fires No DOCT
ROM 7	ROM 7 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
ROM 6	ROM 6 @ ROM Address + 4MHz + Undocumented Opcodes + Z80 + STA Mode + No Error + No POST
KUIVI 6	ROW 0 @ ROW Address + 4MHZ + Undocumented Opcodes + 280 + STA Mode + No Error + No POST