LaCASA NVM Research Infrastructure

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Introduction

- What is this document about?
  - Contains a brief description of research infrastructure developed in the LaCASA Laboratory to enable ongoing and future research in non-volatile memories
- Who developed it?
  - Prawar Poudel, pp0030@uah.edu

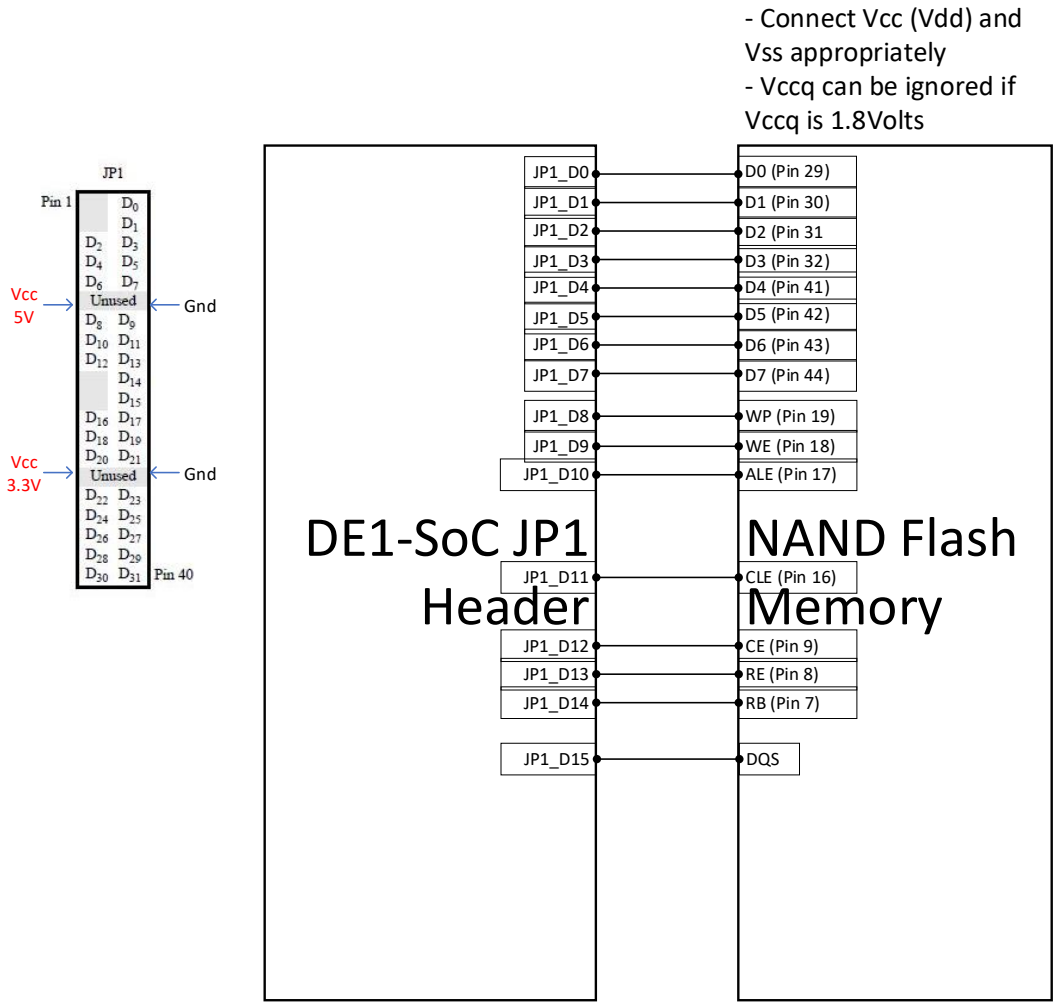
List of Tools/Environments

- 1. Software-emulated ONFI Interface on DE1-SoC platform
- 2. Software-emulated ONFI Interface on DE1-SoC platform (TLC implementation requiring all 3 pages, interlacing, Micron chip)
- 3. FTDI/Python ONFI Interface
- 4. Software-emulated parallel memory MRAM/SRAM interface on DE1-SoC platform
- 5. Software-emulated parallel NOR flash memory interface on DE1-SoC
- 6. RPi/SPI Non-Volatile Memory Interface
- 7. IP hardware module for programming MRAM memory with configurable clock shapes

1. Software-Emulated ONFI Interface

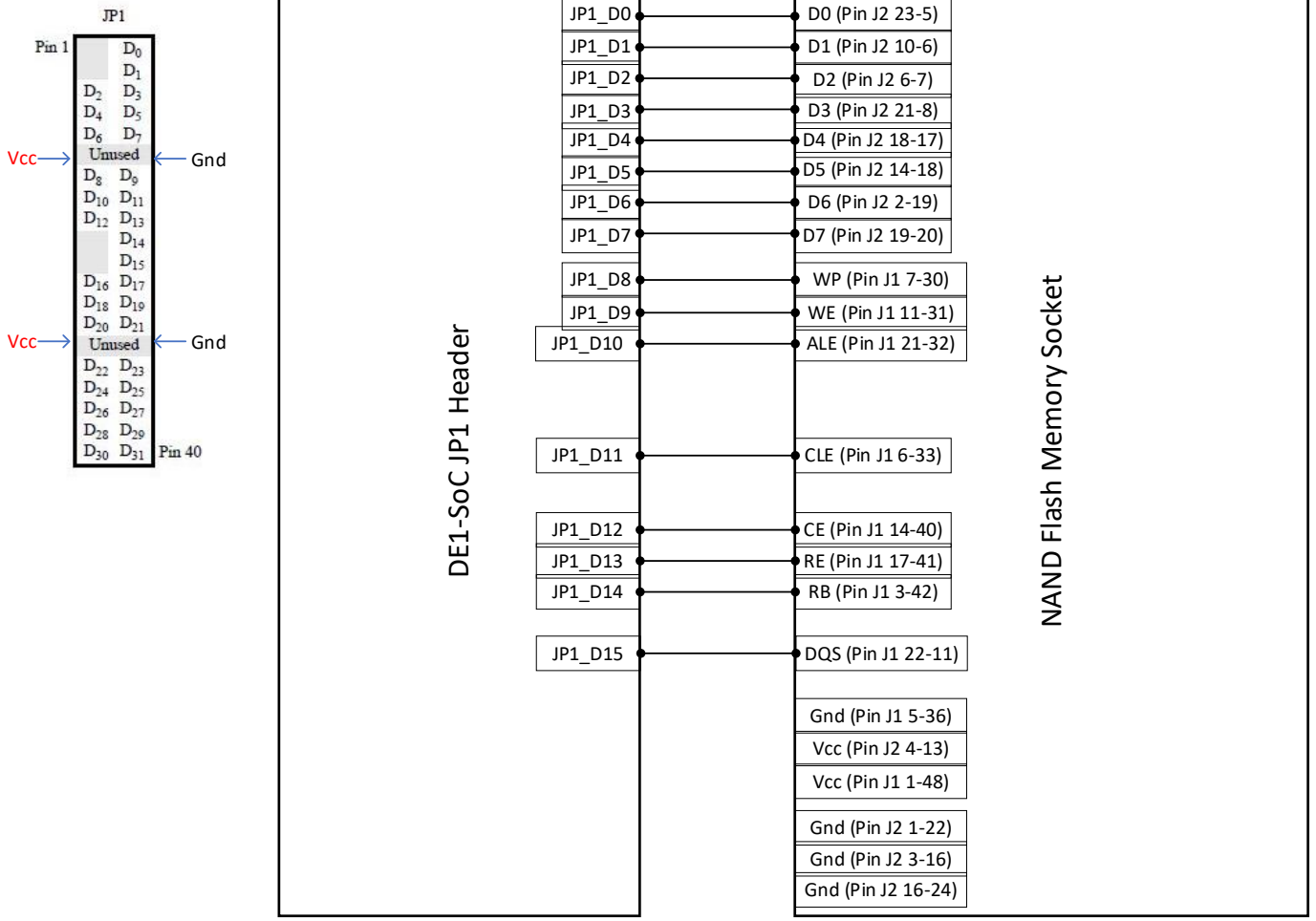
- What: Interfaces NAND flash memories (asynchronous interface)
- Synopsys: DE1-SoC ARM processor is running a program that emulates asynchronous ONFI interface through a parallel port
- Platform: DE1-SoC board
- Hardware implementation: ARM-based DE1-SoC computer (with peripherals in the FPGA fabric)
- OS: Intel (Altera) version of Linux
- Software: Written by Prawar, compiled by gcc
- Link: https://github.com/sickRanchez-c137/onfi_plus
- Flash memory sockets: TSOP48, BGA132
- Flash memory chips tested: Micron SLC, Micron MLC

1. Software-Emulated ONFI Interface



TSOP Connection

1. Software-Emulated ONFI Interface

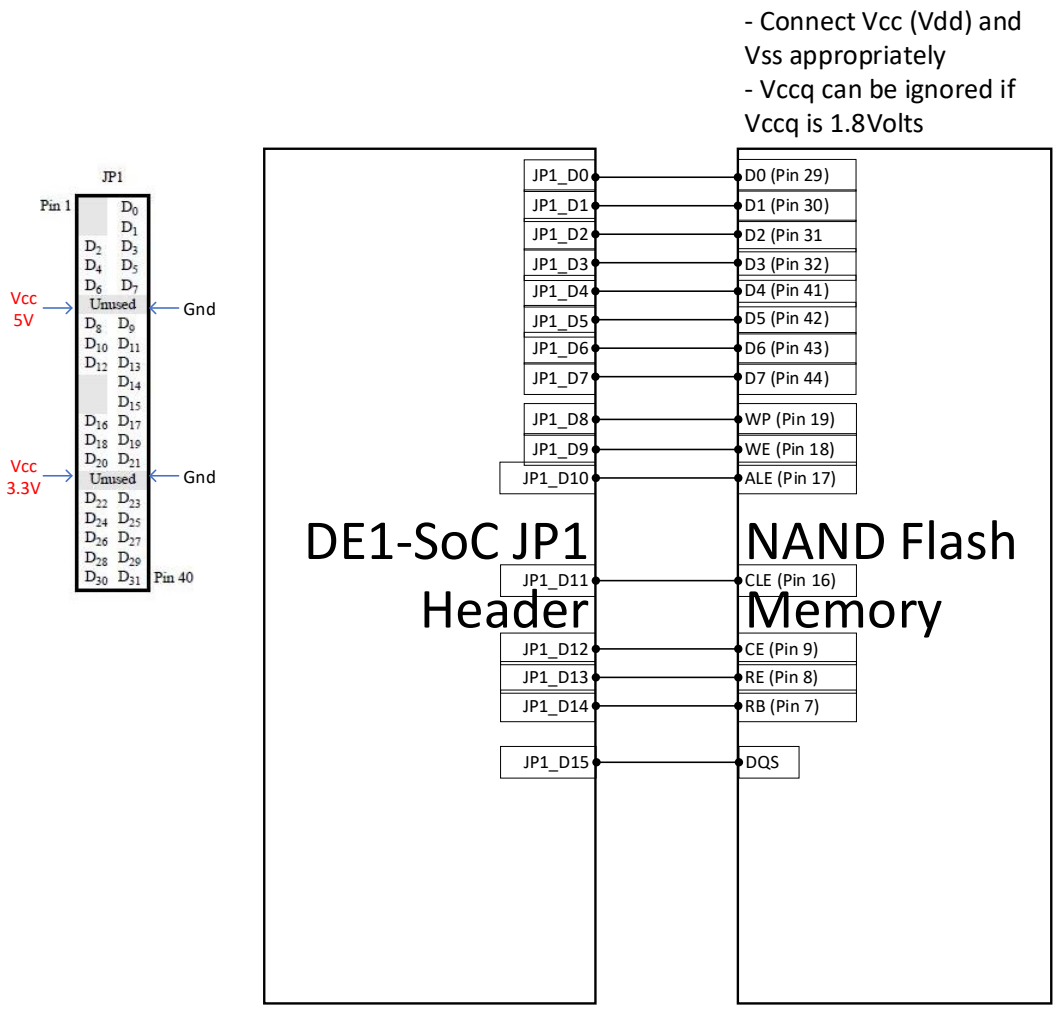


BGA

2. Software-Emulated ONFI Interface (TLC)

- What: Interfaces TLC NAND flash memories (asynchronous interface)
- Synopsys: DE1-SoC ARM processor is running a program that emulates asynchronous ONFI interface through a parallel port
- Platform: DE1-SoC board
- Hardware implementation: ARM-based DE1-SoC computer (peripherals are in the FPGA fabric)
- OS: Intel (Altera) version of Linux
- Software: Written by Prawar, compiled by gcc
- Link: N/A
- Flash memory sockets: TSOP48
- Flash memory chips tested: Micron TLC (requires special approach to programming)

2. Software-Emulated ONFI Interface (TLC)



TSOP Connection

3. FTDI/Python Flash Interface

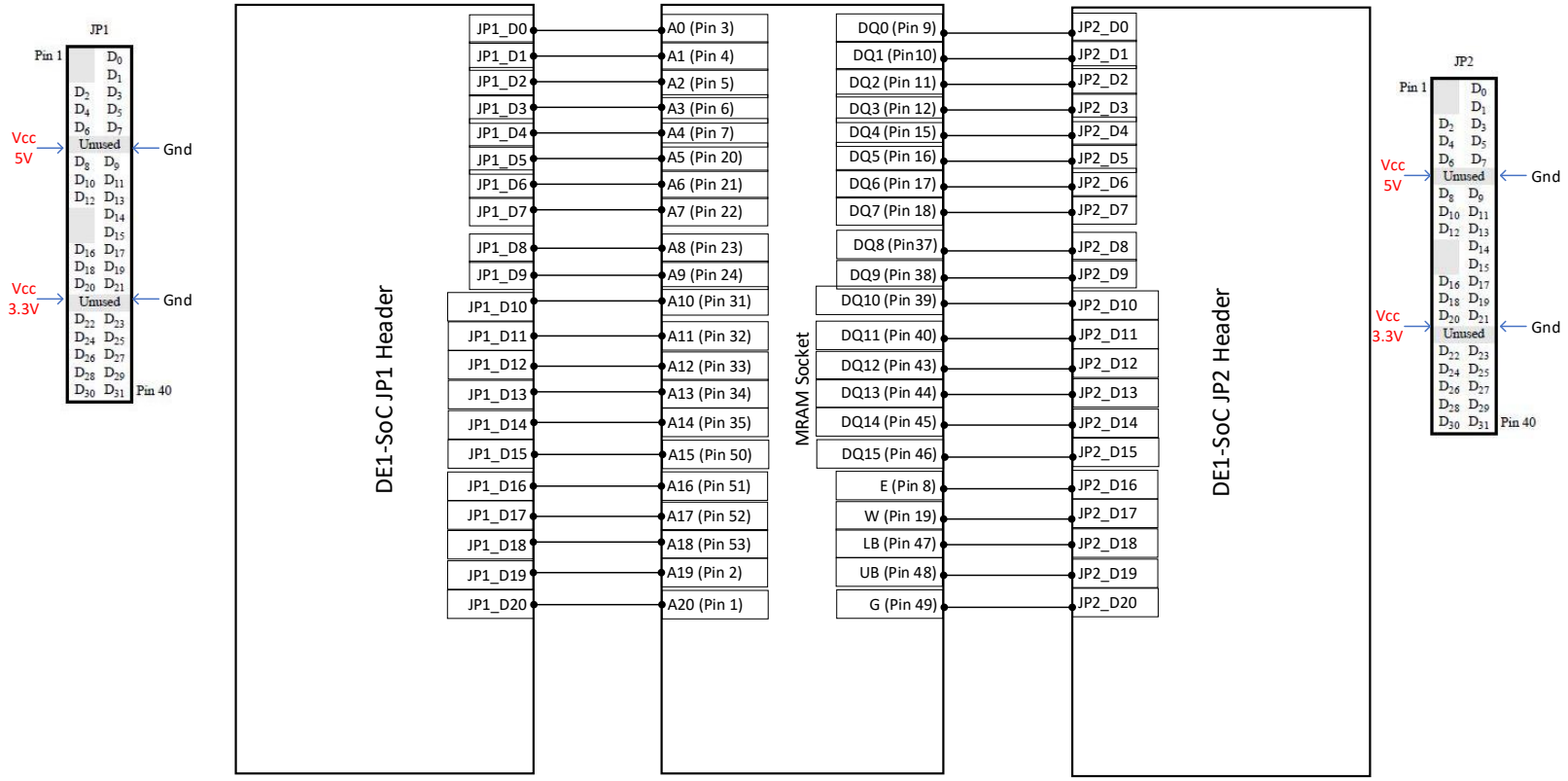
- What: Interfaces NAND flash memories (asynchronous interface)
- Synopsys: Python code written by Matt Oh that allows a low-level interfacing of flash memory chips through an FTDI223H connected through to USB (https://github.com/ohjeongwook/dumpflash)
- Platform: Any PC running Windows with corresponding FTDI driver
- Software: Modified by Prawar and Ethan
- Link: https://github.com/uah-lacasa/ONFI-Interface-LL
- Flash memory sockets: TSOP48, BGA132
- Flash memory chips tested: Micron SLC, Micron MLC

4. Software-emulated parallel memory interface

- What: Implements standard parallel memory (RAM/ROM) interface
- Synopsys: DE1-SoC ARM processor is running a program that emulates the standard parallel memory interface through two parallel ports
- Platform: DE1-SoC board
- Hardware implementation: ARM-based DE1-SoC computer (peripherals are in the FPGA fabric)
  - Interface: 21 address lines, 16 data lines, CE, WE, OE, UB (upper byte), LB (lower byte)
- OS: Intel (Altera) version of Linux
- Software: written by Prawar, compiled by gcc
- Link: https://github.com/sickRanchez-c137/parallel-mram-interface
- Memory sockets: TSOP54
- Memory chips tested: Everspin MRAM MR5A16A

4. Software-emulated parallel memory interface

- Pin1(A20), Pin2(A19), Pin3(A0) are on the upper face of the socket on left
- Pin54(NC), Pin53(A18), Pin52(A17) are on the upper face of the socket on right



TSOP-II 54 For MRAM

5. Software-emulated NOR flash memory interface

- What: Interfaces parallel memories (asynchronous interface)
- Synopsys: DE1-SoC ARM processor is running programs that emulate NOR flash memory parallel memory interface through two parallel ports
- Platform: DE1-SoC board
- Hardware implementation: ARM-based DE1-SoC computer (peripherals are in the FPGA fabric)
  - Interface: 21 address lines, 16 data lines, CE, WE, OE, UB (upper byte), LB (lower byte)
- OS: Intel (Altera) version of Linux
- Software: written by Prawar, compiled by gcc
- Link: https://github.com/sickRanchez-c137/TSOP48_JEDEC_NORInterface
- Memory sockets: TSOP48
- Memory chips tested: Cypress NOR (Mirror BIT NOR flash memory)

6. RPI/SPI Memory interface

- What: Interfaces SPI NVM memories (FeRAM, Flash, MRAM)
- Synopsys: SPI interface is utilized to carry out memory operations
- Platform: RPI
- Hardware implementation: -
- OS: Raspbian with SPI driver
- Software: Written by Prawar, compiled by gcc
- Link: https://github.com/sickRanchez-c137/Raspberry-Pi-SPI-Memory
- Memory sockets: SOIC8, SOIC16
- Memory chips tested: Fujitsu FRAM, Everspin MRAM

7. IP Core with a PLL for Writing

- What: Runs custom write on parallel MRAM chip
- Synopsys: IP core with PLL that programs the parallel Everspin MRAM in a sweeping way (with clock shape control through PLL duty cycle)
- Platform: DE1-SoC (just FPGA portion, expansion port JP1)
- Hardware implementation: see above
- OS: none (IP core in hardware)
- Software: none (Verilog HDL)
- Link: N/A
- Memory sockets: Protoboard
- Memory chips tested: MRAM Everspin XX
- Status: not successful yet