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# ONFI Compliant NAND Flash Controller

## Reference & Specs. Rev. 17

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A brief and simplified user reference for the ONFI Compliant NAND Flash Controller.

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## NAND Flash

"***NAND flash*** memory is a type of non-volatile storage technology that does not require power to retain data. An important goal of ***NAND flash*** development has been to reduce the cost per bit and increase maximum chip capacity so that flash memory can compete with magnetic storage devices like hard disks." WhatIs.com

## ONFI

"The Open NAND Flash Interface (ONFI) is an industry Workgroup made up of more than 100 companies that build, design-in, or enable NAND Flash memory. We're dedicated to simplifying NAND Flash integration into consumer electronic products, computing platforms, and any other application that requires solid state mass storage. We define standardized component-level interface specifications as well as connector and module form factor specifications for NAND Flash." Onfi.org

## Controller Interface

### Avalon MM ports

| Port name | Bit width | Direction | Purpose |
|---|---|---|---|
| CLK | 1 | IN | System clock |
| $\overline{\text{RESET}}$ | 1 | IN | Reset input. Active low |
| READDATA | 32 | OUT | Data output port |
| WRITEDATA | 32 | IN | Data/command input port |
| ADDRESS | 2 | IN | Address index |
| $\overline{\text{PREAD}}$ | 1 | IN | Read strobe |
| $\overline{\text{PWRITE}}$ | 1 | IN | Write strobe |

### NAND interface ports

| Port name | Bit width | Direction | Purpose |
|---|---|---|---|
| NAND_CLE | 1 | IN | Command latch enable |
| NAND_ALE | 1 | IN | Address latch enable |
| $\overline{\text{NAND\_WE}}$ | 1 | IN | Write enable. Active low |
| $\overline{\text{NAND\_WP}}$ | 1 | IN | Write protect. Active low |
| $\overline{\text{NAND\_CE}}$ | 1 | IN | Chip enable. Active low |
| $\overline{\text{NAND\_RE}}$ | 1 | IN | Read enable |
| NAND_$\overline{\text{RB}}$ | 1 | OUT | Ready/busy. Is low when busy |
| NAND_DATA | 16 | INOUT | Data/command bus. Upper 8 bits are ignored for x8 NAND flash chips. |

## Instruction set

| Instruction | Code | Operation |
|---|---|---|
| NAND_RESET | 1 | Instructs the controller to reset NAND flash. |
| NAND_READ_PARAMETER_PAGE | 2 | Reads ONFI parameter page |
| NAND_READ_ID | 3 | Reads NAND Flash ID code |
| NAND_BLOCK_ERASE | 4 | Instructs the controller to perform block erase operation on the chip |
| NAND_READ_STATUS | 5 | Read the content of the NAND Flash's status register |
| NAND_READ_PAGE | 6 | Instructs the controller to read one page from NAND Flash |
| NAND_PAGE_PROGRAM | 7 | Instructs the controller to program one page to NAND Flash |
| CTRL_GET_STATUS | 8 | Retrieves the status of the controller |
| CTRL_CHIP_ENABLE | 9 | Enables the underlying NAND Flash chip |
| CTRL_CHIP_DISABLE | 10 | Disables the underlying NAND Flash chip |
| CTRL_WRITE_PROTECT | 11 | Turns on write protection on the underlying NAND Flash chip |
| CTRL_WRITE_ENABLE | 12 | Turns off write protection on the underlying NAND Flash chip |
| CTRL_RESET_INDEX | 13 | Resets index register to 0 |
| CTRL_GET_ID_BYTE | 14 | Retrieves the ID byte currently pointed by the index register[1] |
| CTRL_GET_PARAMETER_PAGE_BYTE | 15 | Retrieves the byte currently pointed by the index register from the parameter page buffer[1] |
| CTRL_GET_DATA_PAGE_BYTE | 16 | Retrieves the byte currently pointed by the index register from the data page buffer[1] |
| CTRL_SET_DATA_PAGE_BYTE | 17 | Sets the byte currently pointed by the index register in the data page buffer to the value on WRITEDATA port[1] |
| CTRL_GET_CURRENT_ADDRESS_BYTE | 18 | Retrieves the byte currently pointed by the index register from the address register[1] |
| CTRL_SET_CURRENT_ADDRESS_BYTE | 19 | Sets the byte currently pointed by the index register in the address register to the value on WRITEDATA port[1] |
| NAND_BYPASS_ADDRESS | 20 | Send single address byte directly to NAND chip[2] |
| NAND_BYPASS_COMMAND | 21 | Send single command byte directly to NAND chip[2] |
| NAND_BYPASS_DATA_WR | 22 | Send single byte of data directly to NAND chip[3] |
| NAND_BYPASS_DATA_RD | 23 | Read single byte of data directly from NAND chip[3] |

1. **Operation increments the index register or resets it to 0 if the register points out of the bounds of the related register/buffer.**
2. **This is useful when sending vendor specific commands (e.g. accessing OTP area on different chips) or commands that are not yet supported by this controller.**
3. **Data is written/read to/from the NAND chip without modifying the page_data buffer.**

## Addresses

+0000: 32 bit data port

+0004: 8 bit command port

+0008: 8 bit status port

## Status byte

| Bit position | Meaning |
|---|---|
| 0 | 1-is ONFI compliant; 0-is not ONFI compliant |
| 1 | Bus width (0 – x8/ 1 – x16) |
| 2 | 1 when chip is enabled |
| 3 | 1 when chip is write protected |
| 4 | 1 when array pointer (index register) points out of bouds |
| 5-7 | reserved |