

CLASS A POWER AMPLIFIER DESIGN

Niki Galagedara (8728488) + Nick Cardamone (300060019)

ELG 4115 DESIGN PROJECT April 12th, 2023

Abstract

This report outlines the design and implementation of a Class A power amplifier for broad bandwidth applications instead of narrowband. The project involved three stages: initial design, fabrication, and full two port S parameter measurements. Two revisions were made to the printed circuit board design, and the project involved the use of alternate design methodologies such as scripting and optimization. The report compares the Class A power amplifier to commercially available low noise amplifiers, Class C amplifiers, and commercial bias tees. The discussion section explores system gain, bandwidth, input matching, and transistor selection. The report concludes with an overview of the project's successes and setbacks, highlighting the importance of modern design methodologies and a thorough understanding of circuit components for successful RF electronics design.

Table of Contents

Abstract	1
Introduction	5
Benchmarking	5
Low Noise Amplifier	5
Class C Power Amplifier	6
Bias Tee	7
Initial Design.....	8
Bias Circuit.....	8
Bias Tee	8
Scripting and Matching Network	9
Revision One	15
Simulation	15
PCB	17
Problems	17
Revision Two	17
Design.....	17
RF Amplifier.....	17
Bias Circuitry	19
RF Simulation	20
PCB	23
Fabrication	25
Testing Results.....	28
Discussion.....	30
System Gain and Bandwidth	30
Transistor Selection.....	30
Design Methodologies, Scripting and Optimization	31
Group Teamwork.....	31
Conclusion.....	32
References.....	32

Figure 1: Wideband Low Noise Amplifier Benchmark	6
Figure 2: Wideband LNA Frequency Response	6
Figure 3: Class C Amplifier Benchmark	7
Figure 4: Class C Amplifier Frequency Response	7
Figure 5: Commercial Bias Tee [3]	7
Figure 6: Ideal Bias Tee [3]	9
Figure 7: Bias Tee Prototype	9
Figure 8: Bias Tee Prototype Frequency Response	9
Figure 9: K stability parameter over frequency.....	10
Figure 10: Input Stability Circles, over frequency and with no approximations.....	10
Figure 11: Output Stability Circles, over frequency and with no approximations.....	11
Figure 12: Input and Output Stability Circles, Unilateral Approximation.....	12
Figure 13: Input Matching Network Schematic (AWR)	12
Figure 14: Output Matching Network (AWR).....	13
Figure 15: Matching Network Input Impedances from MATLAB	13
Figure 16: Optimizer Goals, with Input Matching Network Enabled	14
Figure 17: Input Matching Network Dimensions	14
Figure 18: Output Matching Network Dimensions	14
Figure 19: Full Schematic Rev 1 (AWR)	15
Figure 20: Rev 1 Power Amplifier Gain	15
Figure 21: Output Matching Network Impedances with Optimizer Goals.....	16
Figure 22: Rev 1 Power Amplifier S_{11} and S_{22}	16
Figure 23: Rev 1 PCB	17
Figure 24: Rev 2 Input Matching Network Schematic (AWR).	18
Figure 25: Rev 2 Output Matching Network Schematic (AWR).....	18
Figure 26: Rev 2 Full Schematic (AWR)	18
Figure 27: Rev 2 Optimizer Goals	19
Figure 28: Rev 2 Optimizer Results	19
Figure 29: Rev 2 RF Layout	19
Figure 30: Rev 2 bias circuit	20
Figure 31: Rev 2 Power Amplifier Gain	21
Figure 32: Rev 2 Power Amplifier Return Loss	21
Figure 33: Rev 2 Power Amplifier S_{11} Smith Chart	22
Figure 34: Rev 2 Power Amplifier S_{22}	22
Figure 35: RF Altium Schematic	23
Figure 36: Rev 2 RF Layout	24
Figure 37: Rev 2 RF Layout, 3D View	24
Figure 38: Bonding the RF PCB to an FR4 substrate for mechanical rigidity.....	25
Figure 39: Thermal image of the boards baking on the hotplate	25
Figure 40: RF PCB with FR4 board bonded to the bottom, with SMA connectors soldered on	26
Figure 41: Rev 2 RF Board	26
Figure 42: Bias Circuit Board	27
Figure 43: Rev 2 Fully Assembled Power Amplifier.....	27
Figure 44: Rev 2 Power Amplifier with Cables	28

Figure 45: Low Frequency Power Amplifier Response.....	28
Figure 46: Full 2 Port S Parameter Measurements of the Rev 2 Power Amplifier Design	29
Figure 47: In Lab VNA Measurement Setup (1)	29
Figure 48: In Lab VNA Measurement Setup (2)	30

Introduction

Power amplifiers are essential components in the field of radio frequency electronics, used to amplify signals to higher power levels for transmission. While there are several classes of power amplifiers, Class A amplifiers are known for their high linearity and low distortion, making them a popular choice for applications that require high-quality signal amplification.

In this microwave circuits class project, a class A power amplifier has been designed and fabricated to maximize gain over the broadest bandwidth possible. Unlike class C amplifiers, which are known for their high efficiency but produce high levels of distortion, class A amplifiers offer high linearity and low distortion, making them suitable for our project's goal of maximizing gain while maintaining a clean signal.

The first revision of the amplifier was designed using a scripting and optimizer tool in AWR software. The second revision used a readily available transistor and was designed entirely through parameter optimization. In the second revision, An emphasis was put on achieving a broader bandwidth over high gain.

Throughout this report, the design and performance of this class A power amplifier will be discussed, with a particular focus on the realization and the measured S parameters. The target center frequency was 3.3 GHz, however that has been rounded to 3 GHz throughout this report.

The MATLAB code mentioned in this report is available at MATLAB code for this is available at
<https://github.com/ncardamone10/ELG4115>

Benchmarking

Low Noise Amplifier

As a comparison, this class A power amplifier design was evaluated against a commercially bought low noise amplifier that was powered from USB. The low noise amplifier utilized class A biasing and lumped elements, which can work for designs at 3 GHz. A current source and self-bias configuration were utilized to reduce temperature variation and improve performance. The amplifier's signal was transmitted via coplanar waveguide with via stitching instead of microstrip. The amplifier was powered via USB with a linear regulator to regulate voltage down to the bias point and attenuate switching noise from the battery bank. As part of this benchmarking, the amplifier gain over frequency was characterized with a spectrum analyzer.



Figure 1: Wideband Low Noise Amplifier Benchmark

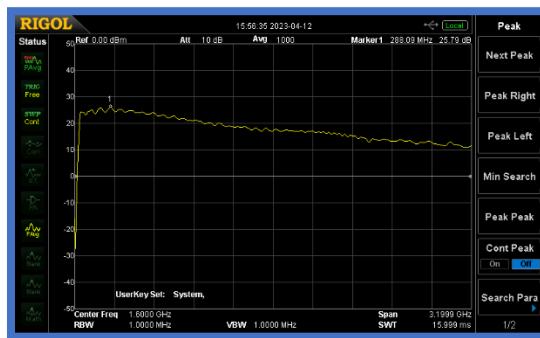


Figure 2: Wideband LNA Frequency Response

Class C Power Amplifier

The comparison of the class A power amplifier design also included a class C amplifier powered from 12V. Class C amplifiers are known for their high efficiency but are characterized by high levels of distortion due to their nonlinear operation [2]. Resonant input matching networks can improve linearity, but the class C amplifier that was benchmarked had a poorly designed matching network, resulting in poor linearity and high distortion. When a 20 MHz tone was injected into the amplifier, the resulting total harmonic distortion was less than 10 dB. Similar to the previous benchmark, the gain of this amplifier was also characterized.

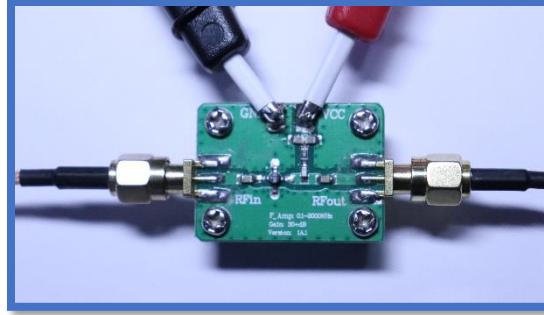


Figure 3: Class C Amplifier Benchmark

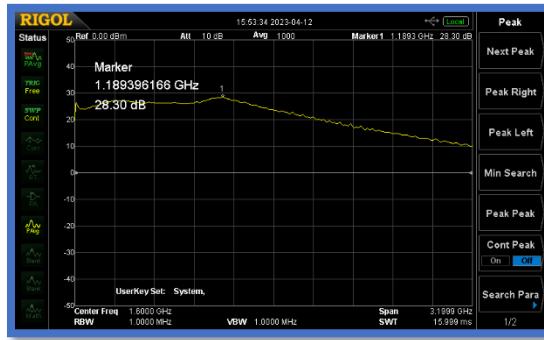


Figure 4: Class C Amplifier Frequency Response

Bias Tee

The RF choke part of the class A power amplifier design was also compared to a commercial bias tee that is commonly used to combine a DC bias signal with an RF signal. The bias tee utilized multiple inductors in series to achieve improved high-frequency performance and bandwidth. SMD components were preferred due to their lower equivalent series inductance, but larger inductors were still wire-wound and can cause interwinding capacitance issues that can impact high-frequency performance.

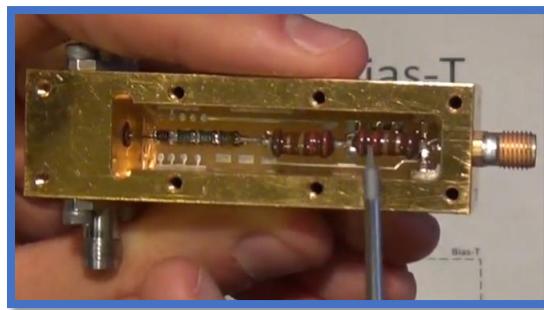


Figure 5: Commercial Bias Tee [3]

Initial Design

Bias Circuit

In the bias circuit design, 0603 resistors were used to provide bias for a collector current of 25 mA and a collector voltage of 8V. A DC current gain of 150 was assumed for the transistor. To bias the transistor, a base resistor of 47 kΩ and a collector resistor with a self-biasing configuration were utilized. The collector resistor had a value of 220 Ω and a bias voltage of 12 V was applied. The self-biasing configuration ensured that a stable bias point was maintained regardless of temperature or transistor parameters. Overall, the bias circuit was designed to provide stable and reliable biasing for the Class A power amplifier. The following were used to calculate the resistor values:

$$R_{base} = \frac{V_{collector} - V_{base}}{\frac{I_{collector}}{DC\ Current\ Gain}} = \frac{8 - 0.7}{\frac{25m}{150}} \approx 47\ k\Omega$$
$$R_{collector} = \frac{V_{bias} - V_{collector}}{I_{collector}} = \frac{12 - 8}{25m} \approx 220\ \Omega$$

Bias Tee

The bias tee design was optimized to provide higher bandwidth and high frequency response. The components used in the design were selected based on their availability only. If other component values were available, there would have been more inductors in series with nano henry values being used. Multiple inductors were used in series to improve high-frequency performance and bandwidth, while surface mount components with less equivalent series inductance were utilized to minimize parasitics. However, the 1000 μH inductor is still wire-wound inductors caused excess interwinding capacitance and impacted performance. The resulting isolation at 3 GHz is about 20 dB. This could have been better if different values could have been used for the inductor.

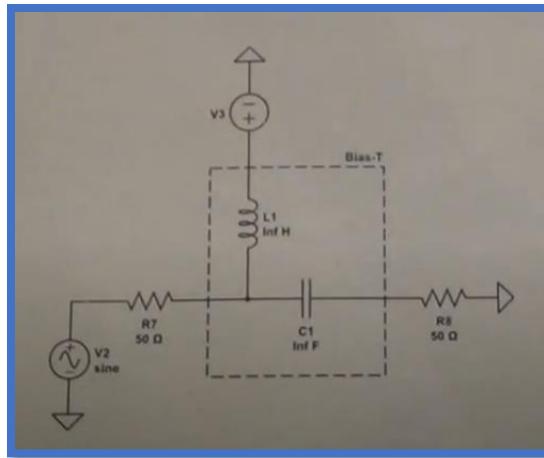


Figure 6: Ideal Bias Tee [3]

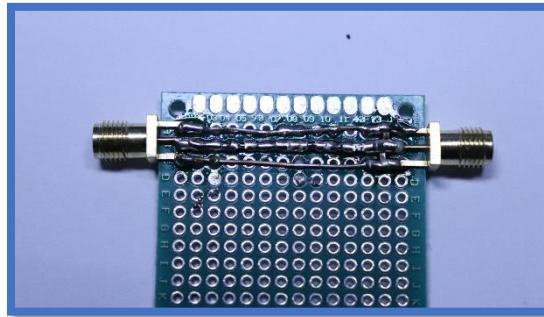


Figure 7: Bias Tee Prototype

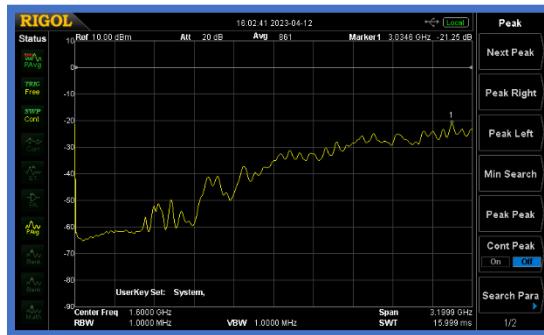


Figure 8: Bias Tee Prototype Frequency Response

Scripting and Matching Network

To design the input and output matching networks, a script in MATLAB has been written and the optimizer has been used in AWR as opposed to using paper, pencil and a smith chart, as this is the more professional solution. From these scripts, it was determined that when the S parameters are used with

no approximations, the transistor can be potentially unstable. The following is the K stability parameter plotted over frequency.

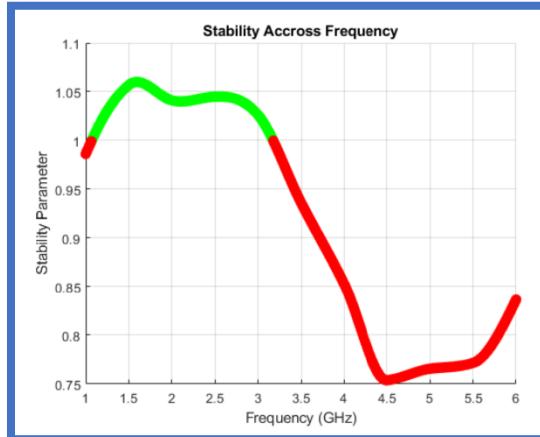


Figure 9: K stability parameter over frequency

When looking at the mu stability parameter, the transistor is most likely to oscillate around 4 GHz. When the unilateral approximation is made, the system becomes unconditionally stable and a design for the maximum possible power gain can be achieved. Before moving on to that, the stability circles should be checked just in case, as the system is technically potentially unstable. Below are the stability circles for the input and output matching network.

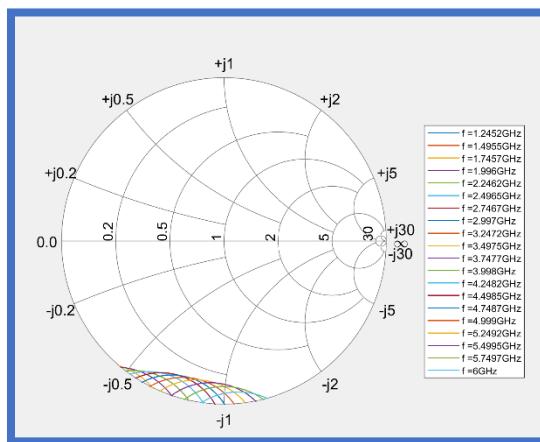


Figure 10: Input Stability Circles, over frequency and with no approximations

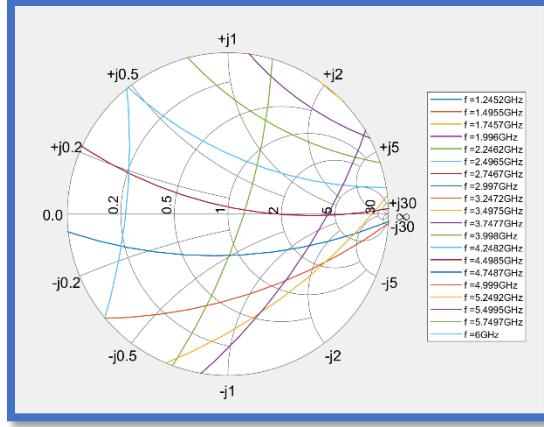


Figure 11: Output Stability Circles, over frequency and with no approximations

As seen from the input stability circles, the input matching network should not cause any problems. However, the output matching network could lead to some parasitic oscillations as the stability circles rotate through the plane when sweeping over frequency. When this code is run live, the various stability circles are animated and one can tell which frequencies could cause problems.

After verifying stability and looking at the stability circles, the reflection coefficients looking towards the load and generator respectively from the transistor were chosen as the following.

$$\Gamma_{\text{towards gen}} = S_{11}^* = 0.68 \angle -124^\circ, \Gamma_{\text{towards load}} = S_{22}^* = 0.37 \angle 54^\circ$$

With these reflection coefficients chosen, stability must be assessed. The following plots make use of the unilateral approximation and show the system is unconditionally stable.

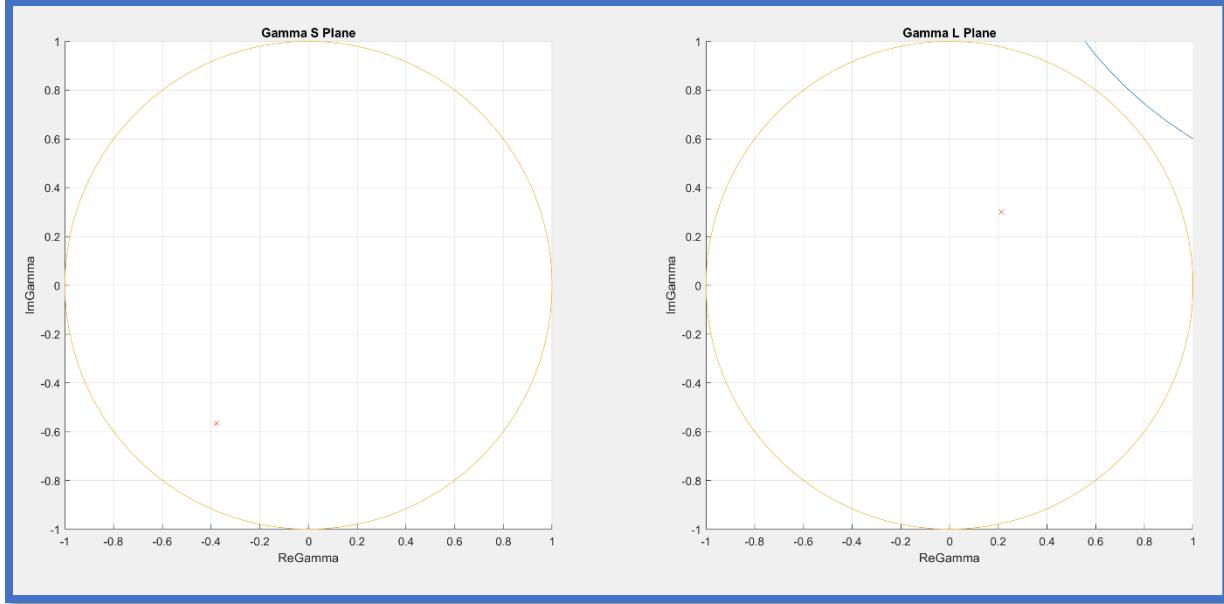


Figure 12: Input and Output Stability Circles, Unilateral Approximation

Once the stability was verified, a topology for the input and output matching networks were chosen. They are as follows.

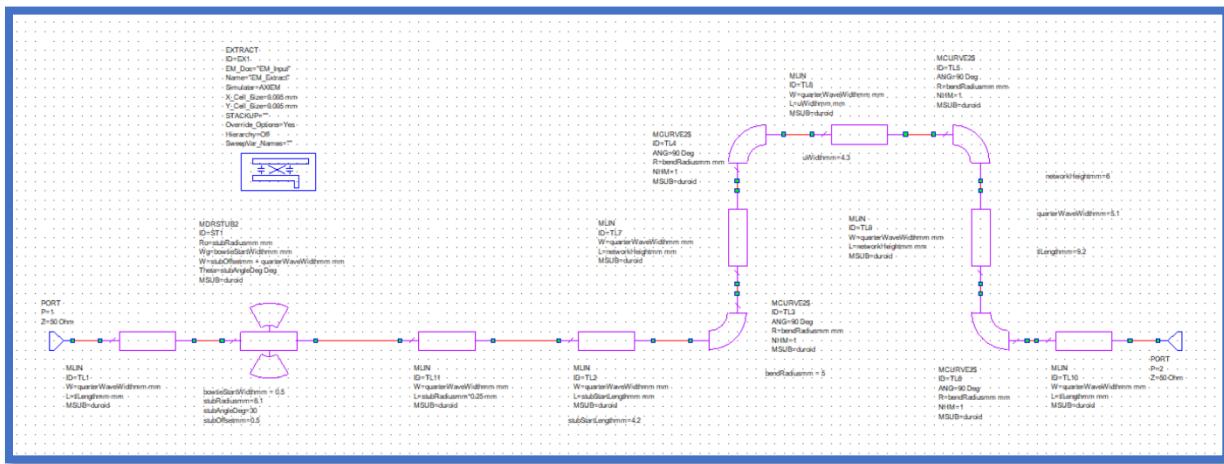


Figure 13: Input Matching Network Schematic (AWR)

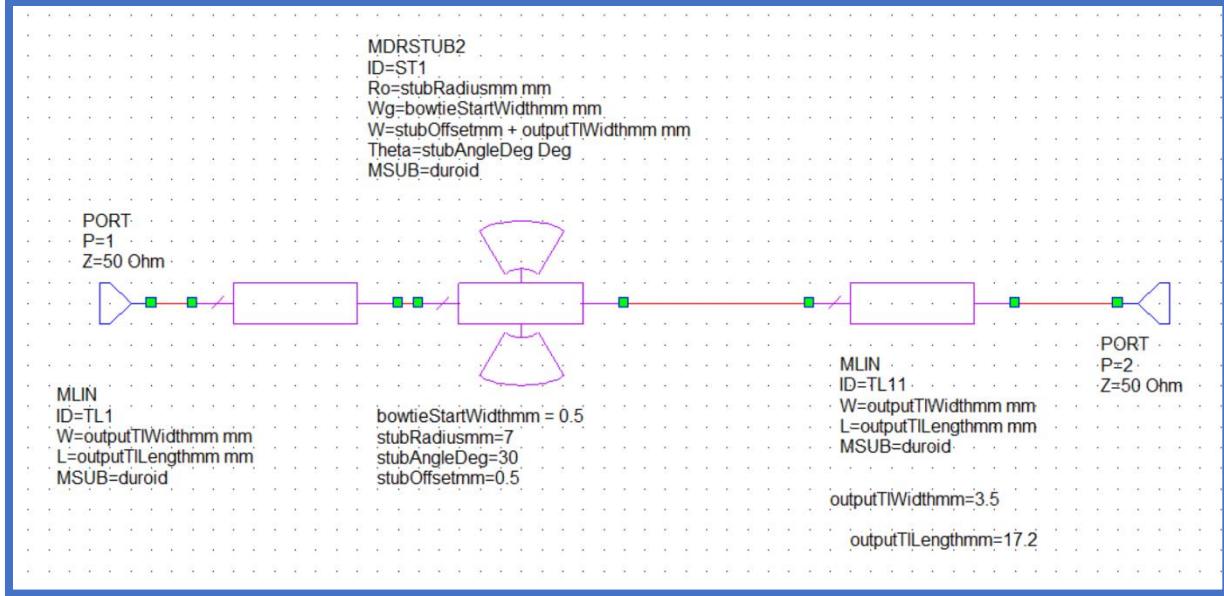


Figure 14: Output Matching Network (AWR)

To find the dimensions that satisfy the required reflection coefficients, the optimizer in AWR was used. To do that, the reflection coefficients were first transformed into impedances with 50Ω as the system impedance. Then the optimizer goals were set as follows.

For the input matching network:
Gamma looking towards gen from transistor: $0.68027 \angle -123.7179^\circ$
Corrisponding Z: $12.1108 - 25.511i\Omega$

For the output matching network:
Gamma looking towards load from transistor: $0.368 \angle 54.7055^\circ$
Corrisponding Z: $60.8703 + 42.2935i\Omega$

Gain Info
Expected gain @3.3GHz: 10.5485dB
Gain error bounds [0.80549, 1.0535] dB

Figure 15: Matching Network Input Impedances from MATLAB



Figure 16: Optimizer Goals, with Input Matching Network Enabled

Document input	Element	ID	Parameter	Value	<input checked="" type="checkbox"/> Tune	<input checked="" type="checkbox"/> Optimize	<input checked="" type="checkbox"/> Constrain	Lower	Upper	Step Size	Tag
Input	MCURVE2\$	TL6	NHM	1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Input	EQN		networkHeightmm	6	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	1	15	0.1	
Input	EQN		quarterWaveWidthmm	5.1	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0.5	15	0.1	
Input	EQN		bowtieStartWidthmm	0.5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Input	EQN		stubRadiusmm	8.1	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0.5	20	0.1	
Input	EQN		bendRadiusmm	5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Input	EQN		tILengthmm	9.2	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	2	20	0.1	
Input	EQN		stubStartLengthmm	4.2	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	0	10	0.1	
Input	EQN		uWidthmm	4.3	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	2	30	0.1	
Input	EQN		stubOffsetmm	0.5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Input	EQN		stubAngleDeg	30	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				

Figure 17: Input Matching Network Dimensions

Document output	Element	ID	Parameter	Value	<input checked="" type="checkbox"/> Tune	<input checked="" type="checkbox"/> Optimize	<input checked="" type="checkbox"/> Constrain	Lower	Upper	Step Size	Tag
Output	PORT	P1	Z	50	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Output	PORT	P2	Z	50	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Output	EQN		stubRadiusmm	7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	0.5	20	0.1	
Output	EQN		outputTILengthmm	17.2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	1	20	0.1	
Output	EQN		outputTIWidthmm	3.5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	0.5	10	0.1	
Output	EQN		stubOffsetmm	0.5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Output	EQN		stubAngleDeg	30	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				
Output	EQN		bowtieStartWidthmm	0.5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				

Figure 18: Output Matching Network Dimensions

Revision One

Simulation

After the parameters have been found via numerical optimization. The circuit can be simulated. The following are the simulation results of the first revision with the AT41486 transistor.

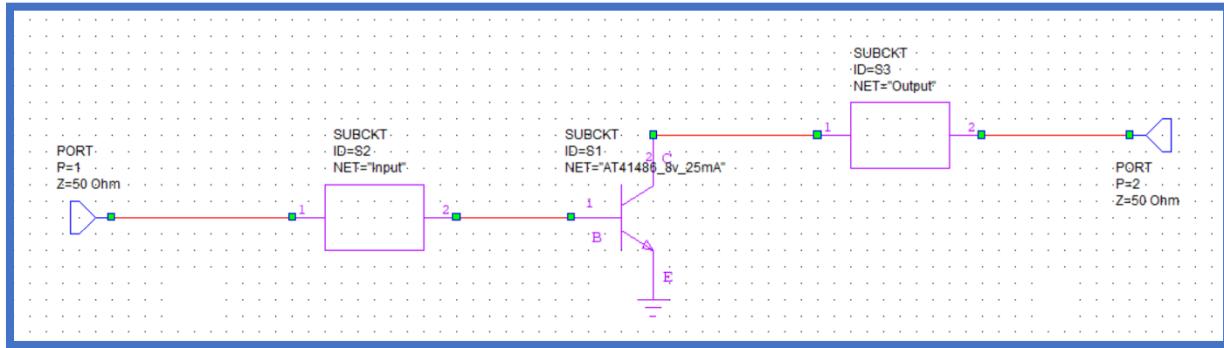


Figure 19: Full Schematic Rev 1 (AWR)

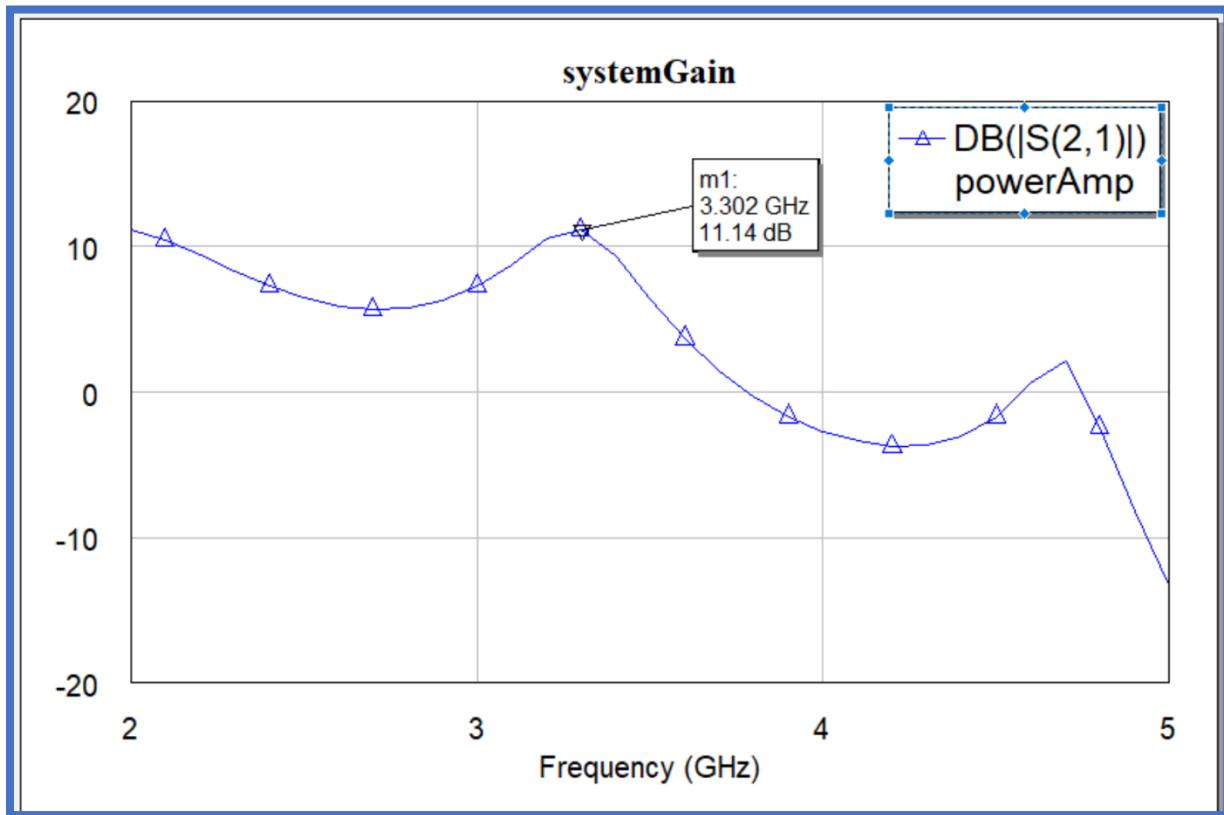


Figure 20: Rev 1 Power Amplifier Gain

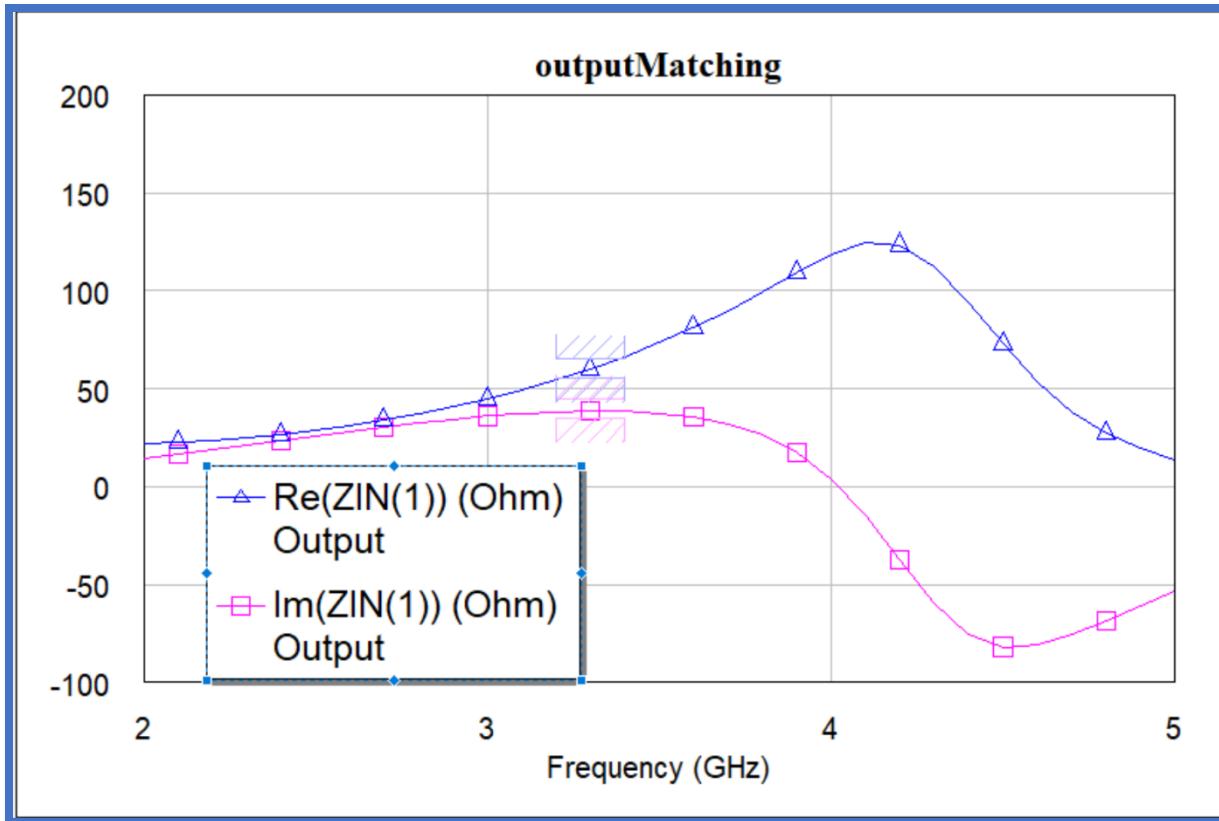


Figure 21: Output Matching Network Impedances with Optimizer Goals

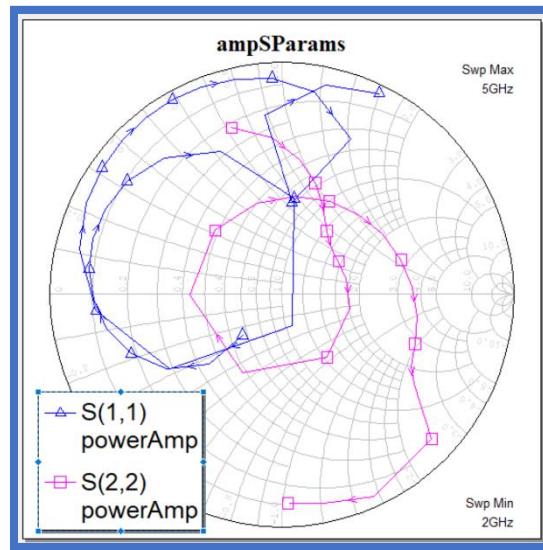


Figure 22: Rev 1 Power Amplifier S_{11} and S_{22}

PCB

The following was the fabricated PCB.

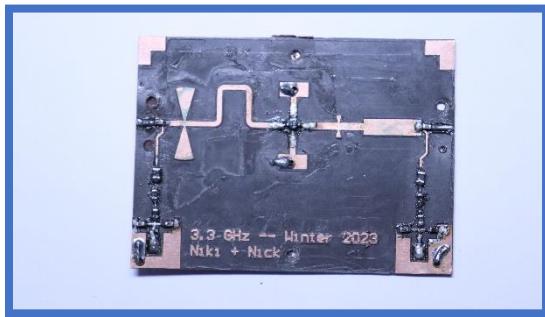


Figure 23: Rev 1 PCB

Problems

During the first revision of the PCB design, significant problems were encountered. No gain could be obtained from the amplifier due to the incorrect application of bias and the swapping of resistor values, resulting in an unstable amplifier. These issues were identified too late in the design process, rendering the first revision of the PCB unusable. Additionally, due to the limited supply of AT41486 transistors, a new design was necessary, which could be fabricated using more readily available components. In addition to that, tired engineers make mistakes.

Revision Two

Design

RF Amplifier

The second revision of the PCB design was undertaken after the failure of the first revision. A new transistor was needed, and the BFP620H7764XTSA1 RF TRANS NPN 2.8V 65GHZ SOT343-4 [1] was selected through parametric search on Digikey based on cost, availability, and ease of simulation. The transistor was added to an order for another capstone project, and the design was carried out using AWR simulation software only. The SPICE model for the new transistor was already loaded into the software, making the design process easier. The optimizer was used to prioritize a wideband design as well as 20 dB of gain, resulting in a high-performing Class A power amplifier.

The following are the AWR schematics used.

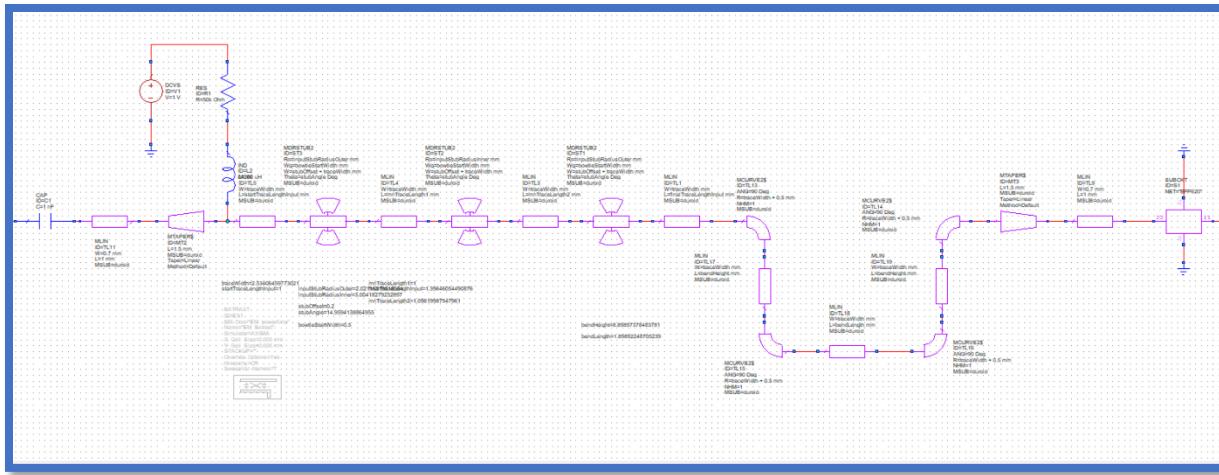


Figure 24: Rev 2 Input Matching Network Schematic (AWR)

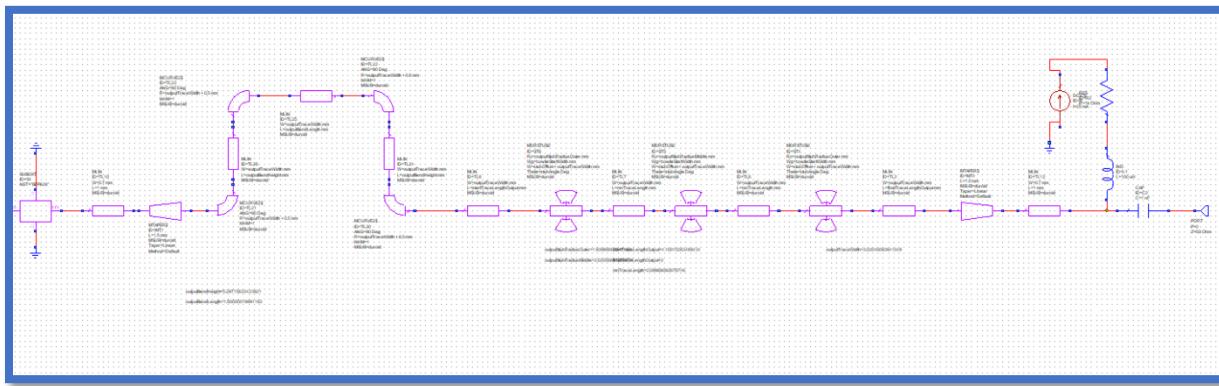


Figure 25: Rev 2 Output Matching Network Schematic (AWR)

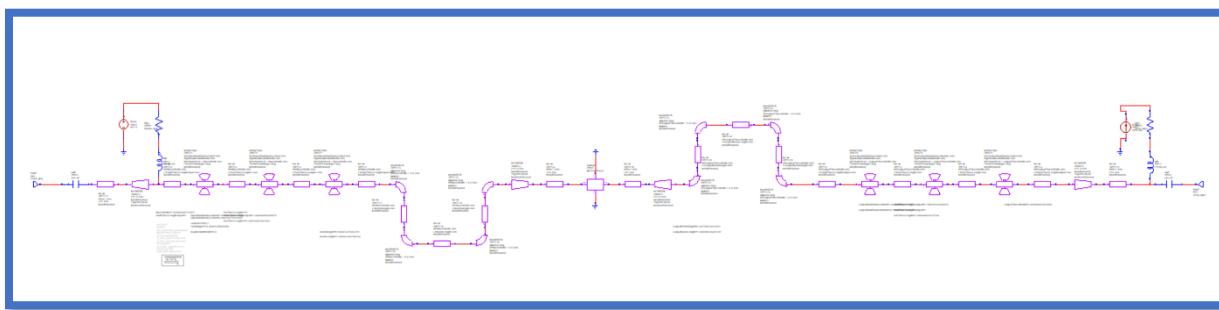


Figure 26: Rev 2 Full Schematic (AWR)

The following are the optimizer goals and parameter results.

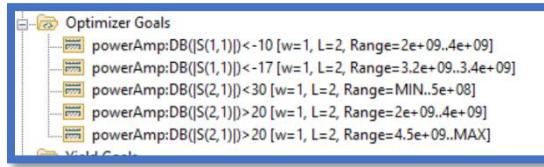


Figure 27: Rev 2 Optimizer Goals

Document	Bernier	ID	Parameter	Value	Tune	Optimize	Constraint	Lower	Upper	Step Size	Tag
powerAmp	MCURVE2s	TL20	NHM	1							
powerAmp	MCURVE2s	TL14	ANG	90							
powerAmp	EQN		outputTraceWidth	3.02046093941048							
powerAmp	EQN		inputStubRadiusOuter	0.0011613864655							
powerAmp	EQN		traceWidth	0.00111613918554							
powerAmp	EQN		mnTraceLength1	1							
powerAmp	EQN		outputStubRadiusMiddle	2.0056887059771							
powerAmp	EQN		statTraceLengthInput	1							
powerAmp	EQN		bowlStartWidth	0.5							
powerAmp	EQN		bowlEndLength	1.00000019991182							
powerAmp	EQN		bendLength	1.8993240705239							
powerAmp	EQN		stabOffset	0.2							
powerAmp	EQN		lnalTraceLengthInput	1.39646054490976							
powerAmp	EQN		mnTraceLength2	1.05615987947361							
powerAmp	EQN		inputStubRadiusInner	3.00418279323987							
powerAmp	EQN		outputStubRadiusOuter	4.0010263489434							
powerAmp	EQN		stabBendHeight	5.2998533400007							
powerAmp	EQN		mnTraceLength	2.0998505787748							
powerAmp	EQN		outputStubRadiusOuter	1.93905005311198							
powerAmp	EQN		lnalTraceLengthOutput	2							
powerAmp	EQN		bendHeight	8.89897378403781							
powerAmp	IND	1.5	b	400							

Figure 28: Rev 2 Optimizer Results

The following is the layout generated by AWR

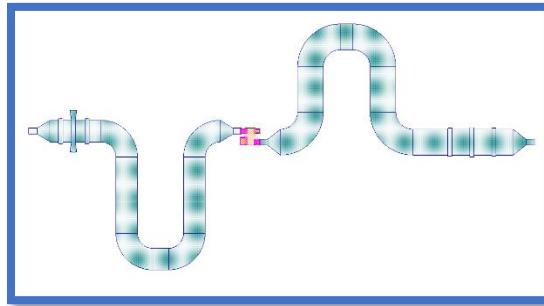


Figure 29: Rev 2 RF Layout

Bias Circuitry

To do the bias circuit, a second PCB has been designed to mate with the RF duroid PCB. The following is the schematic for the bias circuit

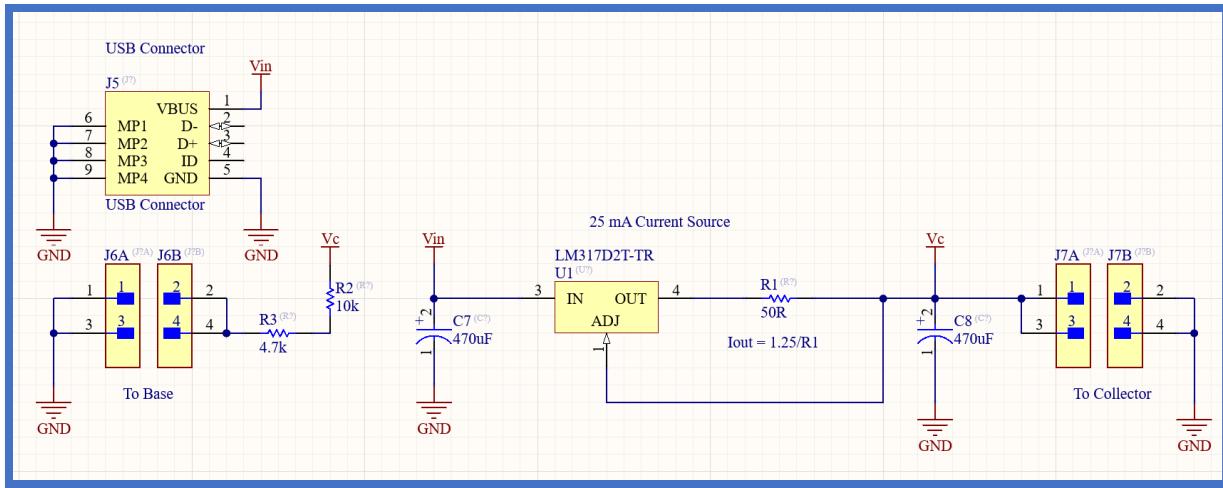


Figure 30: Rev 2 bias circuit

Unlike in the first revision, the bias is supplied by a USB power bank. That USB power bank supplies 5V. After this, a LM317 linear regulator is used as a current source to provide 25 mA to the collector. The bias calculations are as follows.

$$I_{collector} = \frac{V_{reference}}{R1} = \frac{1.25V}{50\Omega} = 25 \text{ mA}$$

To bias the base, a self bias/ diode connected transistor architecture was selected based on simplicity of design. The collector should be kept around 2V and the base should be at 0.7V based on the datasheet. In addition to that, the DC current gain should be around 180 mA/mA. The following is the formula used to calculate base resistor.

$$R_{base} = \frac{V_{collector} - V_{base}}{\frac{I_{collector}}{h_{fe}}} = \frac{2V - 0.7V}{\frac{25 \text{ mA}}{180}} \approx 10 \text{ k}\Omega + 4.7 \text{ k}\Omega$$

To provide a stable input and output voltage, two 470 μF electrolytic capacitors were added into the circuit. All components selected have been used based on availability.

RF Simulation

The following are the results of the AWR simulations.

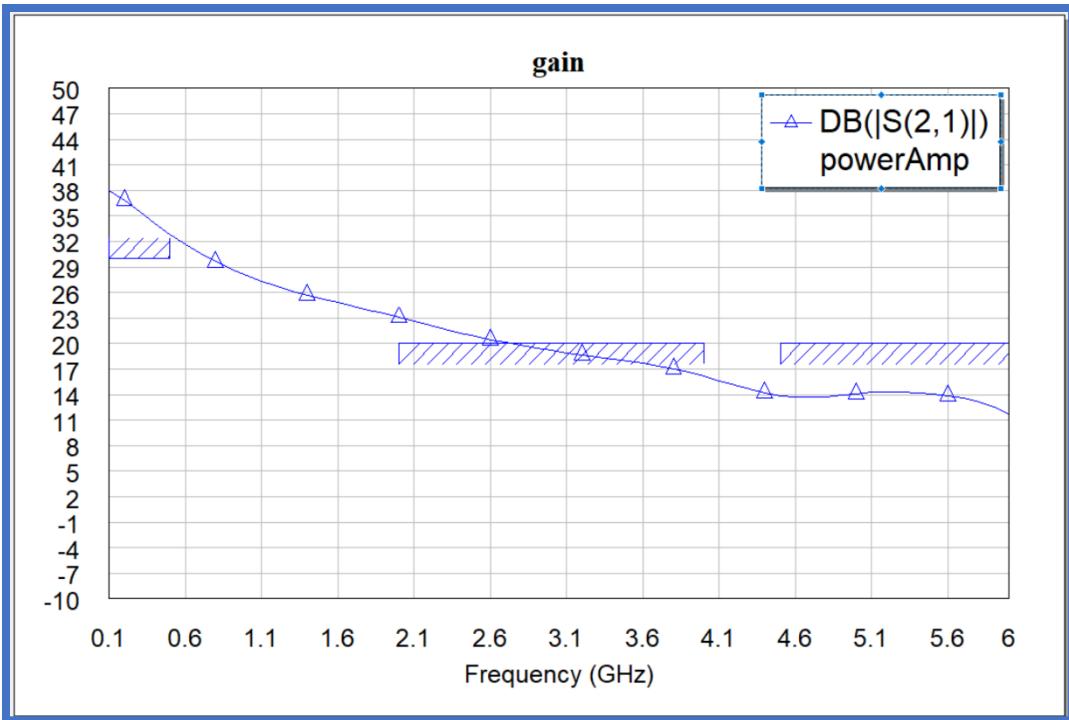


Figure 31: Rev 2 Power Amplifier Gain

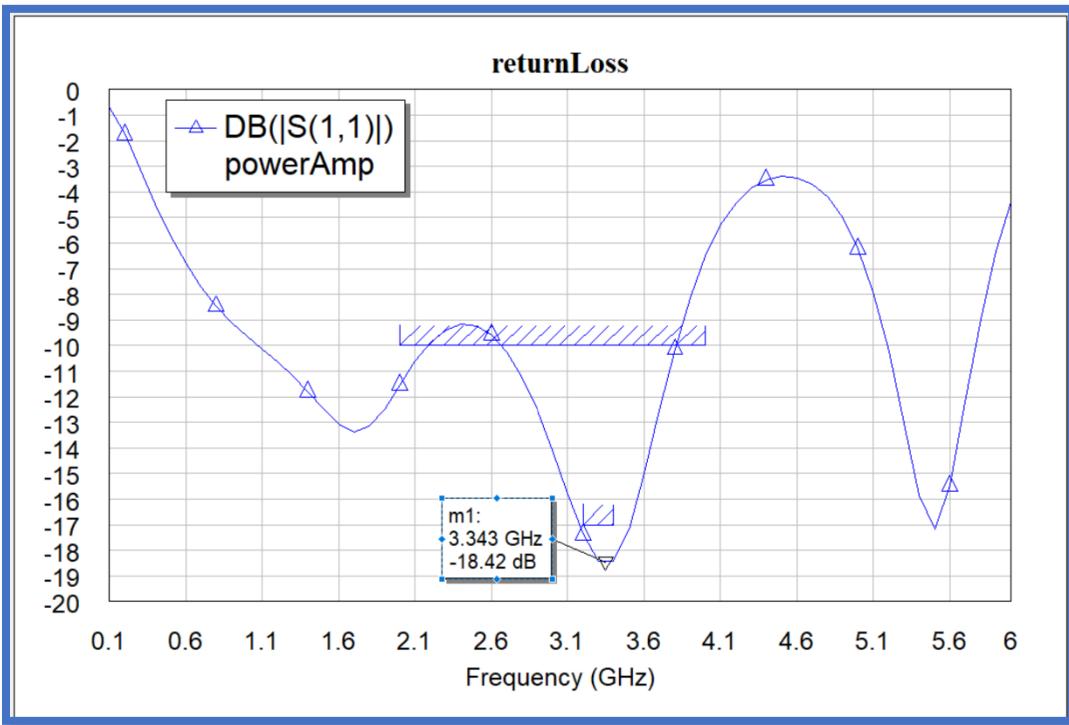


Figure 32: Rev 2 Power Amplifier Return Loss

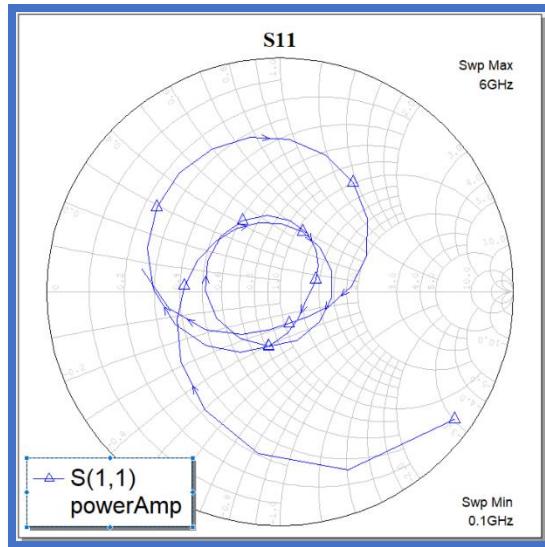


Figure 33: Rev 2 Power Amplifier S_{11} Smith Chart

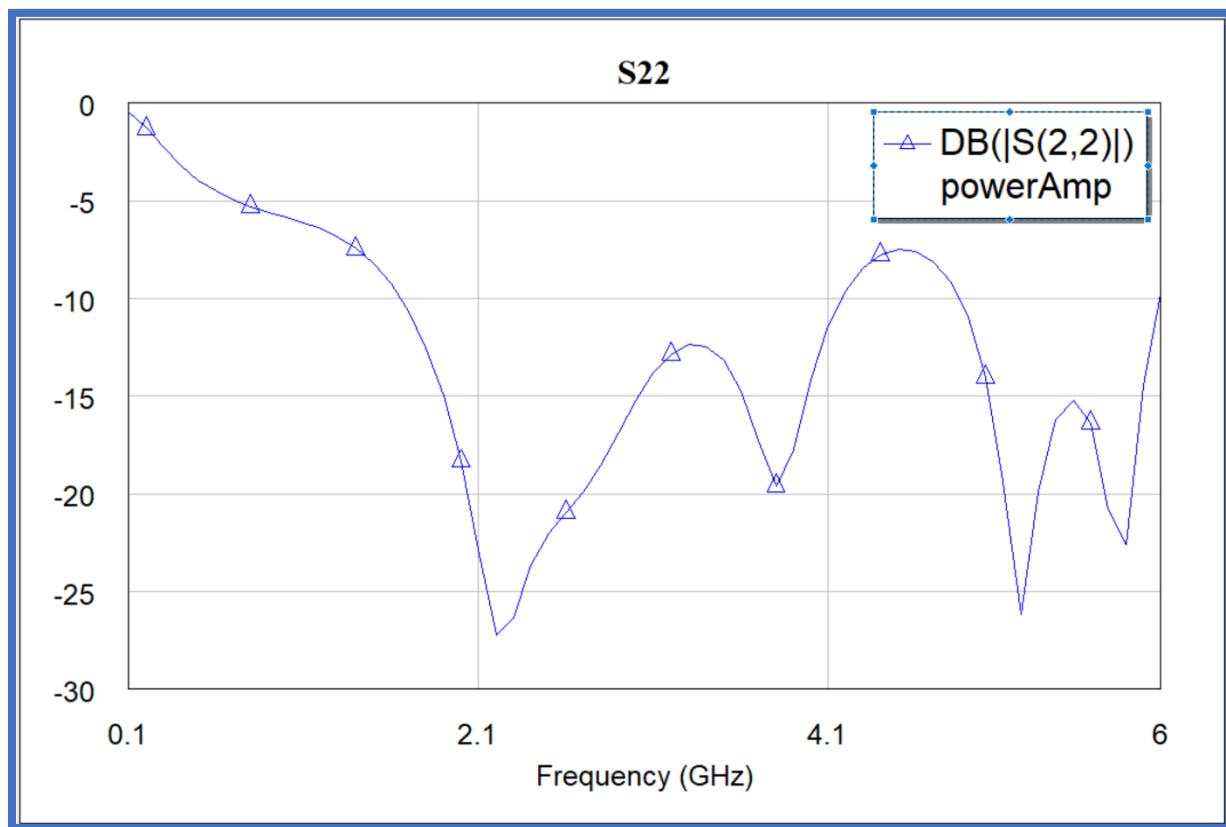


Figure 34: Rev 2 Power Amplifier S_{22}

PCB

To create both revisions of the PCB, Altium designer was used in conjunction with AWR. The workflow basically was both input and output matching networks were isolated and exported as separate DXF files. That was then imported into Altium to do the PCB layout. As part of that layout, a new Altium schematic was generated as follows.

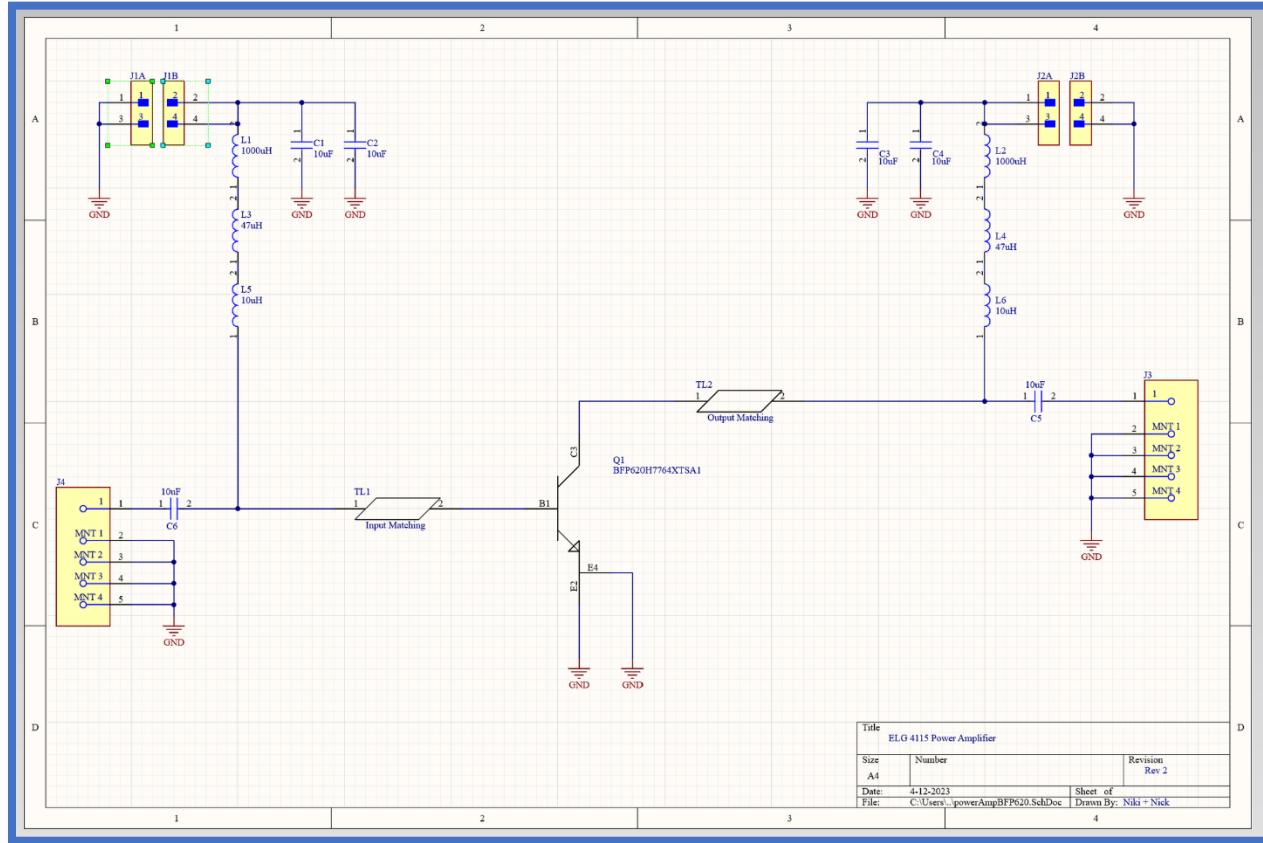


Figure 35: RF Altium Schematic

As previously mentioned, the second revision used a multiboard design. The main RF PCB handles the class A amplifier/ transistor and the bias tee's. A second board handles the bias circuit as well as the USB interface. The following is the layout of the RF board.

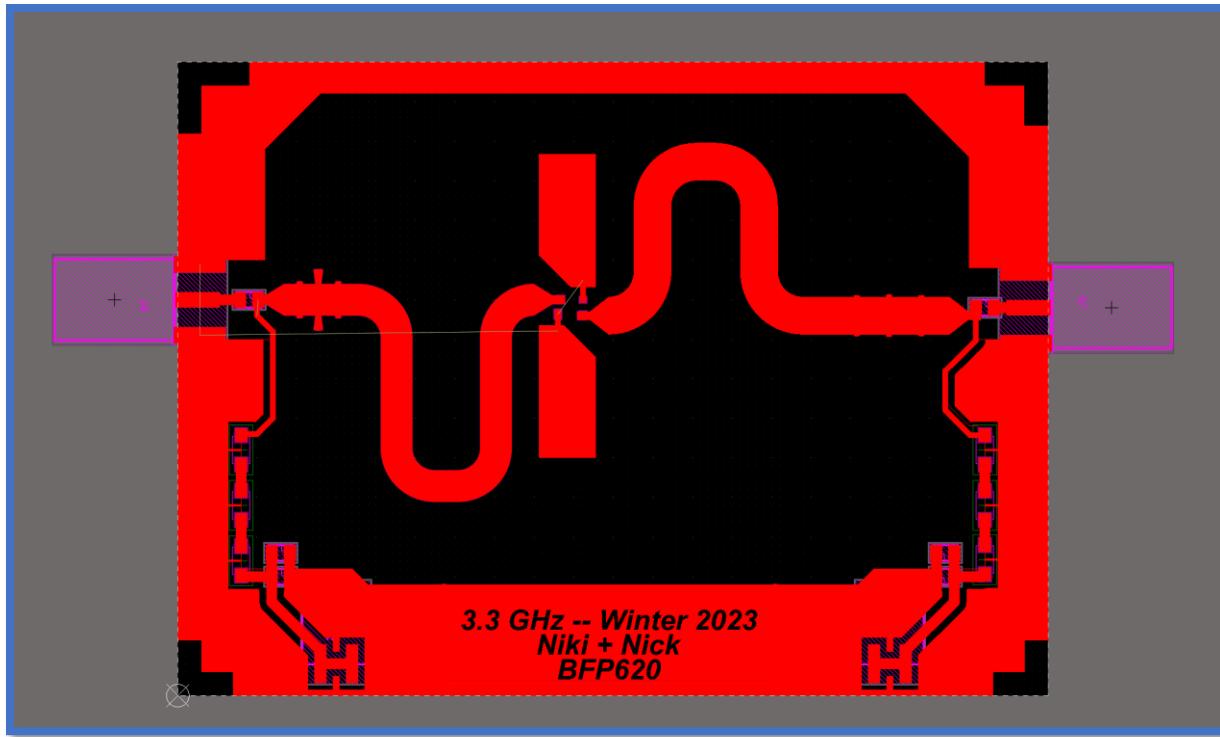


Figure 36: Rev 2 RF Layout

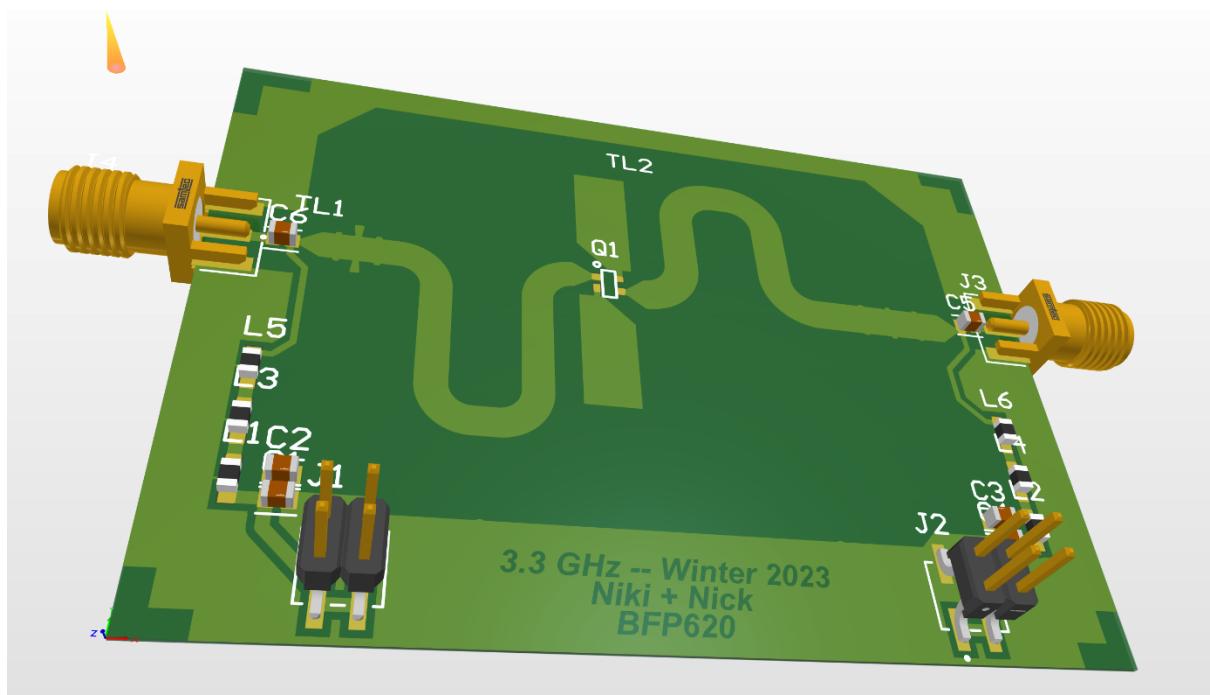


Figure 37: Rev 2 RF Layout, 3D View

Fabrication

The two boards for this design were fabricated with two different methodologies. For the RF board, that was milled and cut out of the duroid 5880 PCB material as supplied by the microwave lab. After that was done, holes were drilled in this PCB to create blind vias. After those holes were drilled, a regular FR4 PCB was bonded to the bottom ground plane of the duroid RF PCB to increase the mechanical rigidity. To do this, ample solder paste and flux were applied to the junction of the PCBs and that was then baked on a hot plate for around 30 minutes slowly increasing the temperature to 200C and waiting until the smoking stopped. It is important to note that the solder paste melts at around 140C so the interface needs to be heated well above that melting point. In addition to that, the baking process has a tendency of warping the duroid board. To solve this, a heatsink was placed on the board to flatten it out as it baked. The following is what this process looked like both in colour and a thermal image showing the soldering process. After that the final board is shown from the bottom.



Figure 38: Bonding the RF PCB to an FR4 substrate for mechanical rigidity

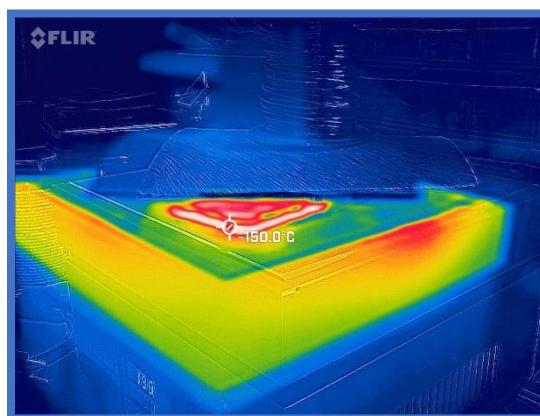


Figure 39: Thermal image of the boards baking on the hotplate

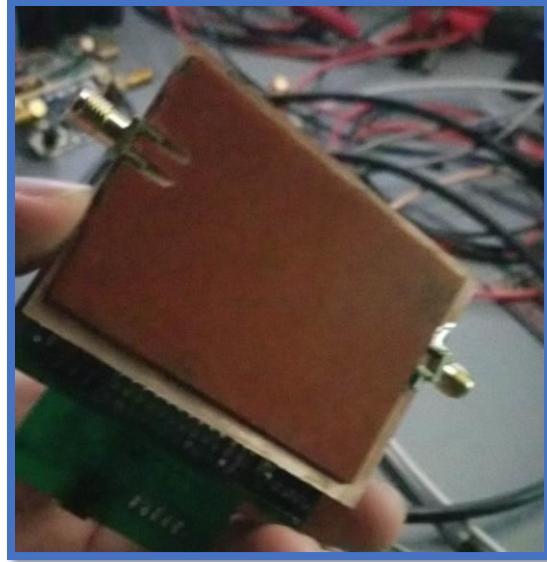


Figure 40: RF PCB with FR4 board bonded to the bottom, with SMA connectors soldered on

To create the bias circuitry board, some regular protoboard was used and a soldering iron was used to solder the components in place. To solder the SMD components onto the RF board, a heat gun and more solder paste was used while being careful not to short anything.

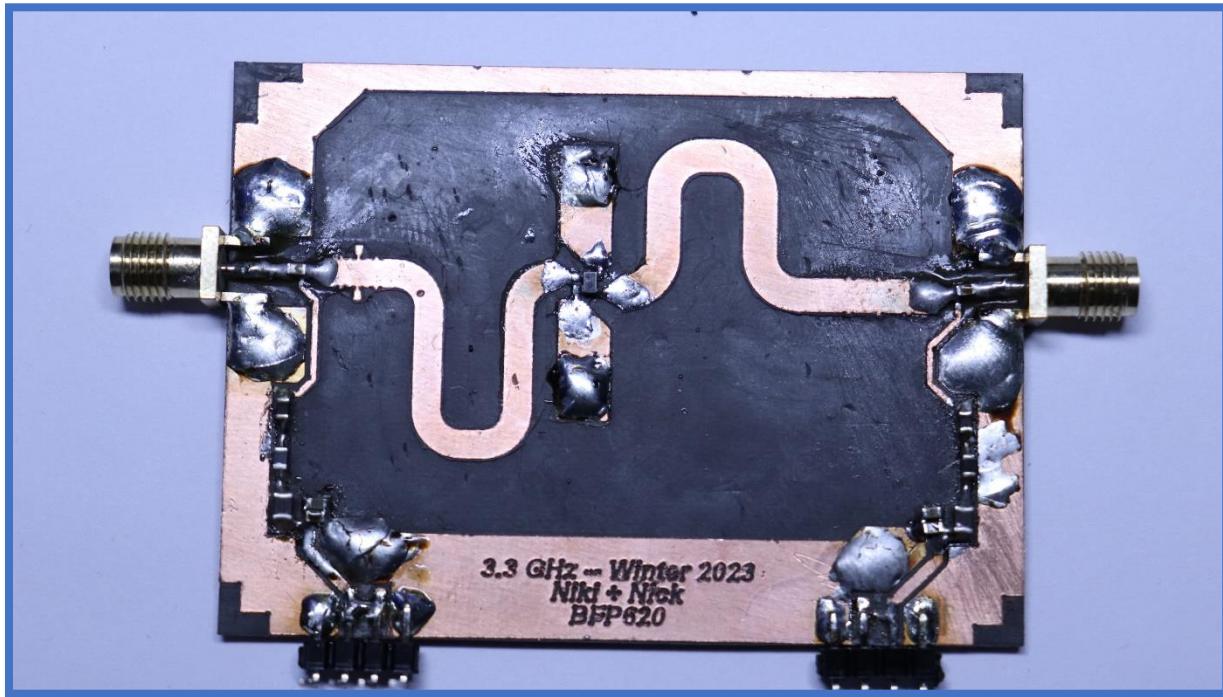


Figure 41: Rev 2 RF Board

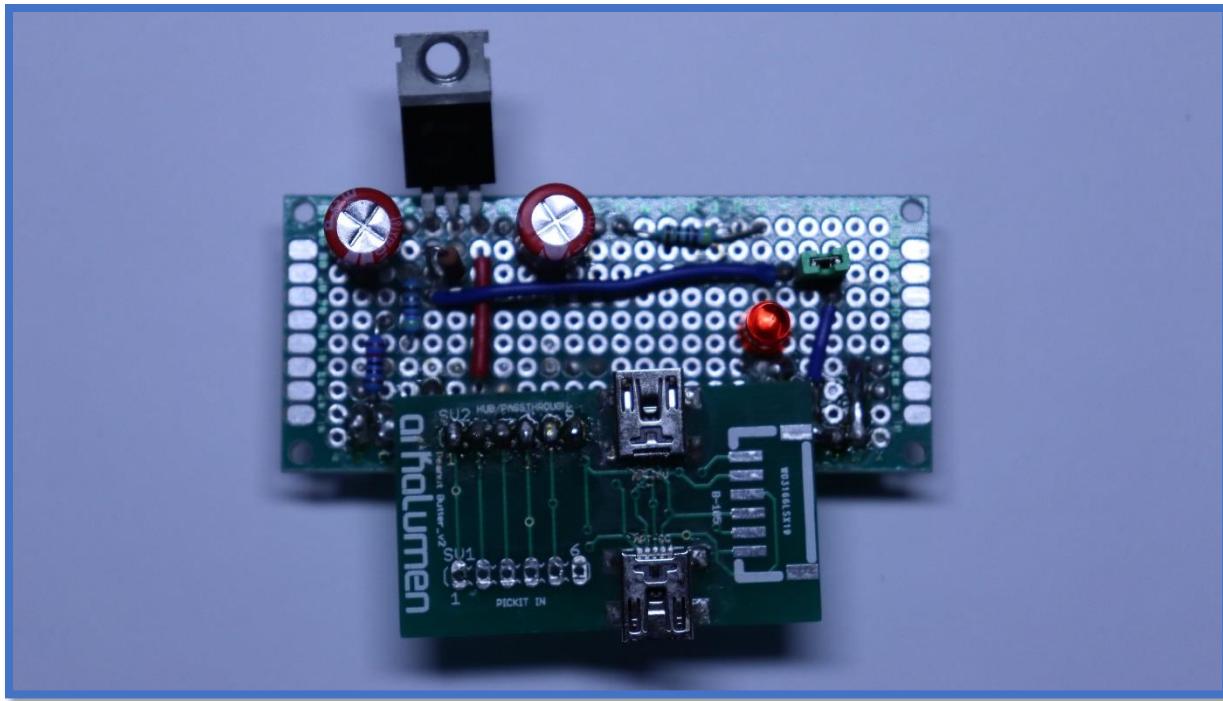


Figure 42: Bias Circuit Board

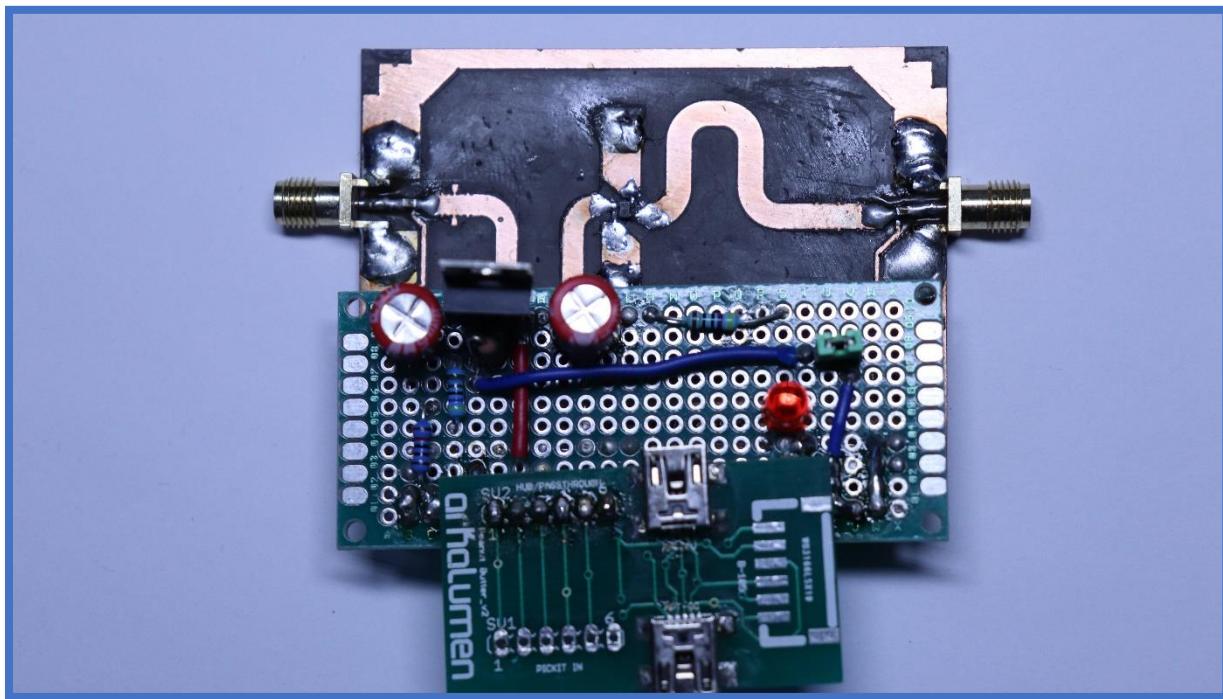


Figure 43: Rev 2 Fully Assembled Power Amplifier

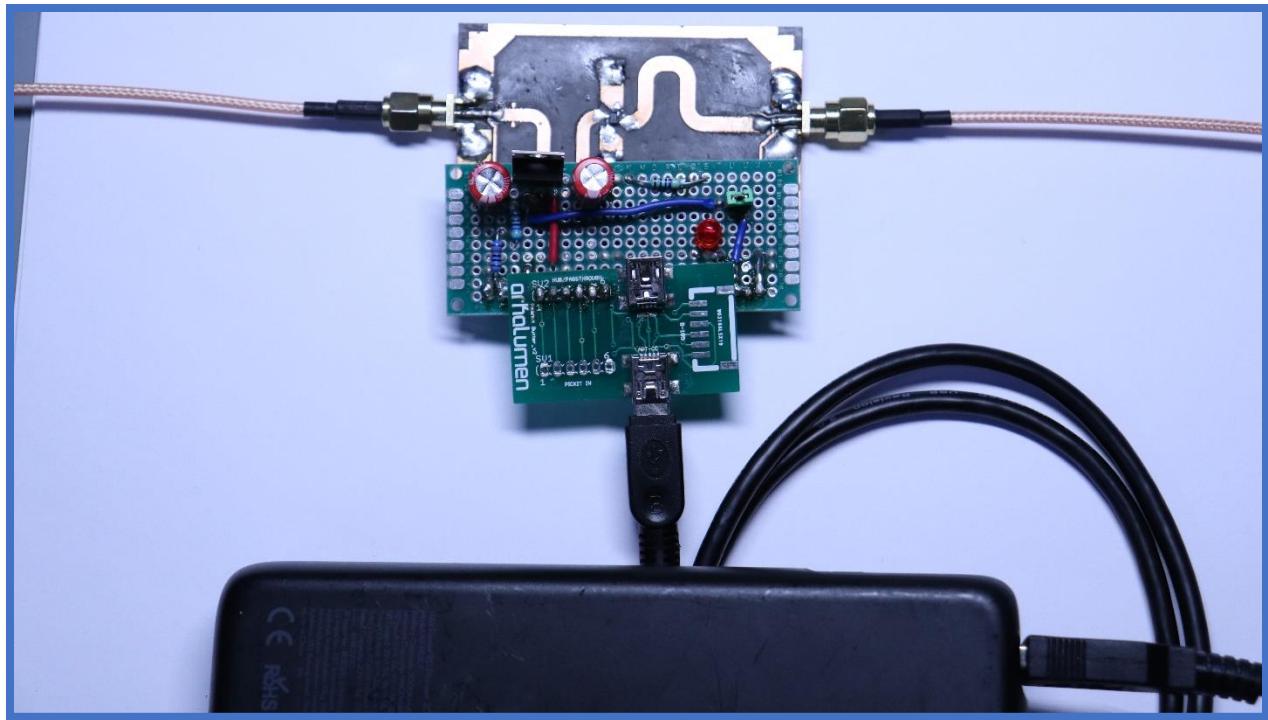


Figure 44: Rev 2 Power Amplifier with Cables

Testing Results

The following are the results from the second revision of the power amplifier.

Table 1: Measured Bias Conditions of BFP620 Transistor

Collector Current (I_C) (mA)	19.6
Base Voltage (V_B) (mV)	684
Collector Voltage (V_C) (V)	1.92

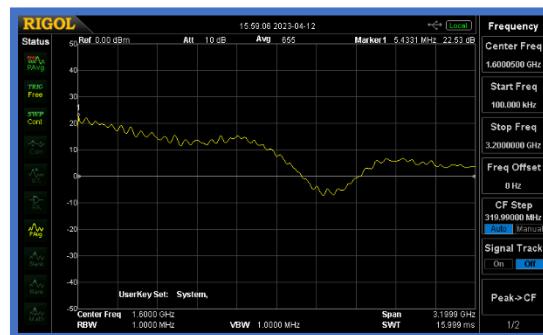


Figure 45: Low Frequency Power Amplifier Response

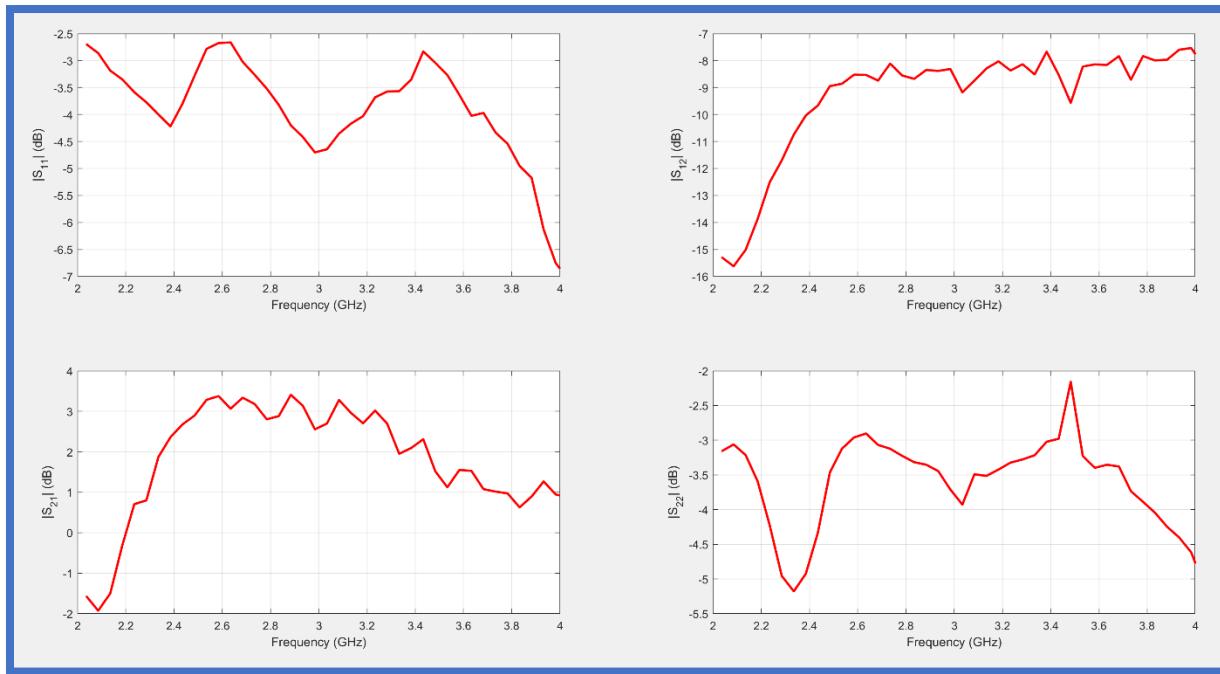


Figure 46: Full 2 Port S Parameter Measurements of the Rev 2 Power Amplifier Design

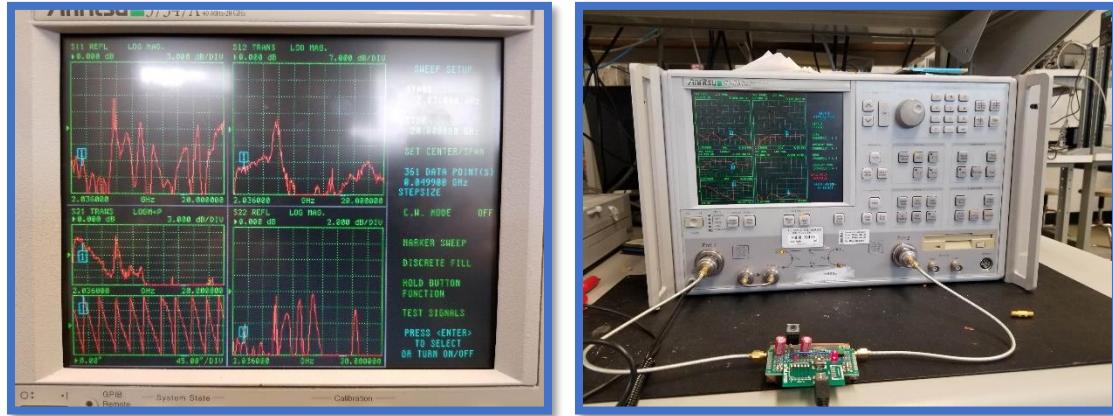


Figure 47: In Lab VNA Measurement Setup (1)

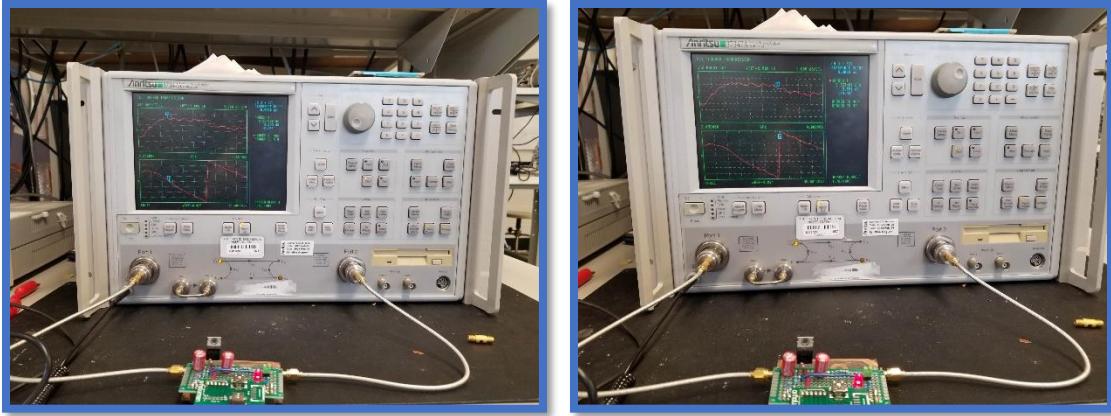


Figure 48: In Lab VNA Measurement Setup (2)

Discussion

System Gain and Bandwidth

The measurement of this second revision of the power amplifier design revealed some interesting findings. Specifically, the realized gain of the amplifier was significantly lower (3 dB) than the simulated gain (17 dB), which could be attributed to the large ground pads on the emitters that were not included in the simulation. Additionally, the wideband design could have contributed to the reduced gain as amplifiers generally need to maintain a constant gain bandwidth product. The input matching of the amplifier was also found to be poor, with a 4 dB return loss, which could be improved in future designs with different topology, lumped element matching networks or better optimization. Finally, the center frequency in return loss shifted from 3.3 GHz to 3 GHz, likely due to simulation inaccuracies and approximations.

Transistor Selection

The selection of the appropriate transistor for this amplifier design required careful consideration of several factors. One consideration was the quantity of components available, as a transistor that was readily available in large quantities was preferred. Companies often buy extra stock in the thousands or tens of thousands due to the current market volatility and semiconductor shortage. Additionally, the selected transistor was already in the AWR simulation environment, making it a better choice for this project. Another important consideration was the use of conflict materials. Many companies declare that their products are conflict material-free, meaning they do not get materials from exploited workers,

particularly in some African nations. This is an ethical consideration that must be taken into account when selecting components for projects such as this amplifier design.

Design Methodologies, Scripting and Optimization

This design project employed advanced design methodologies such as scripting and optimization, which are the norm in industry today. Unlike traditional paper designs, generating a script to calculate basic parameters and then using an optimizer is becoming increasingly common in industry. This approach is similar to the shape synthesis being researched in the antennas group and offers several advantages over traditional design methods such as a reduced iteration time, greater understanding of the larger system as well as the underlying principals without being bogged down by endless equations and circles. The use of MATLAB-generated Smith charts in this project allowed for a better understanding of stability, as other groups had experienced problems with parasitic oscillations. This amplifier design project thus highlights the importance of leveraging modern design methodologies and tools to achieve optimal results in today's rapidly evolving electronics landscape.

Group Teamwork

Throughout this design project there were many twists, turns, struggles, heart aches and conflicts. As part of being on an engineering team, the actual soft skills like team work are critical for success. More specifically, good communication really matters and can mean the difference between meeting a deadline or not. The point of an engineering team is no one person can solve the problem alone, no matter how much they think they can. When issues arise, it is important to talk to team members to come up with risk mitigation strategies just in case something comes up, which usually happens in industry. In addition to that, team members need to be able to trust each other and be able to be open about if they might not make a deadline and what is blocking the progress. Only then can actions be taken to say divert resources towards achieving the deadline or goal.

This kind of thinking could have made this project more successful as there were a lot of difficulties encountered, which happens in industry all the time. In addition to that, tired engineers make mistakes. That is something that just needs to be accepted for what it is and should be dealt with in terms of a risk management and planning perspective.

Overall, this project was fairly successful even though the gain was nowhere near optimal. However, the second revision was rather rushed and better planning/ communication could have improved things.

Conclusion

In conclusion, the Class A power amplifier design project involved the design and implementation of a power amplifier for broad bandwidth applications. The project encompassed several stages, including the initial design and two revisions of the printed circuit board. The benchmarking phase compared the Class A power amplifier to commercially available low noise amplifiers, Class C amplifiers, and commercial bias tees. The results highlighted the importance of input matching networks and inductor selection for bias tees. The discussion section delved into the system gain, bandwidth, input matching, and transistor selection. The project also demonstrated the importance of modern design methodologies, including scripting and optimization, for achieving optimal results.

Despite some setbacks in the initial design phase, the project ultimately yielded a somewhat successful Class A power amplifier design that achieved a wide bandwidth at the cost of a sufficient gain. Overall, this power amplifier design project highlights the importance of effective design methodologies and thorough understanding of circuit components for successful RF electronics design.

References

- [1] Infineon Technologies AG. (2019). BFP620H7764XTSA1 RF TRANS NPN 2.8V 65GHZ SOT343-4. Retrieved from https://www.mouser.ca/datasheet/2/196/Infineon_BFP620_DS_v02_00_EN-2309386.pdf
- [2] Razavi, B. (2012). RF Microelectronics Second Edition. Upper Saddle River, NJ: Prentice Hall.
- [3] The Signal Path. (2017, September 20). TSP #26 - Tutorial on Microwave and mm-Wave Components and Modules [Video file]. Retrieved from <https://www.youtube.com/watch?v=6kwamCh1QkE>.