ELG 4115 Microwave Circuits

Project Information and Design Guidelines

Professor: Dr. P. Berini

The laboratory components of ELG 4115 are to be done in the form of a practical term project. Students are expected to go through a full real-world engineering design cycle for developing a working microwave circuit. This cycle includes:

- preliminary pencil and paper design work,
- simulation and optimization of the **realistic** implementation of the circuit using an industry standard CAD tool,
- preparation of the layout (artwork) necessary for the fabrication of the circuit,
- assembly and mounting of the circuit on the ELG 4115 microwave test jig,
- full experimental characterization of the circuit using industry standard instrumentation such as an HP, Agilent or Anritsu microwave network analyzer,
- hardware debugging and optimization if necessary,
- production of a **high-quality** full engineering technical report.

Due to time, space and budget limitations students must work in groups.

Project Substrate

The circuits will be fabricated using the robust Microwave Integrated Circuit (MIC) technology and all distributed elements will be **microstrip** transmission lines. The substrate used to fabricate your circuits is a high-quality low-loss microwave substrate that has the following characteristics:

- Type: Rogers RT/Duroid 5880
- Thickness: 0.031 inch or 787.41 μm.
- Dielectric constant: $\varepsilon_r = 2.20 \pm 0.04$.
- Dielectric losses: $\tan \delta = 0.0009$ at 10 GHz.
- Copper thickness: 1 ounce (avoirdupoid weight) per square foot or 34 μm.

ELG 4115 Project Specifications

A microwave amplifier will be designed, simulated, built and tested at your assigned frequency in a 50 Ω system. You will be assigned an npn type BJT from those that are currently available for the course. They are the AT-41486 (modified) low-noise devices fabricated by Hewlett-Packard - the relevant specification sheets are attached (legacy devices: AT-42035, AT-42085, AT-41485, AT-60585). The Duroid boards will be fabricated using our in-house etching process. You will then mount all external components and test your amplifier. The following design specifications must be met:

- Gain: $G_{T,max}$ at the design frequency.
- Stability: stable over the entire useful bandwidth of the device.
- $S_{11}|_{amp}$: minimize.
- $S_{22}|_{amp}$: minimize.
- Bandwidth: maximize, based on a narrowband design.

The matching networks are to be designed and constructed using distributed elements (T.L.'s). Only open-circuited shunt stubs should be used since they can easily be fabricated and they allow some tuning. A number of matching networks should be designed and combinations that comfortably fit in the given space (limited by the perimeter of our test fixtures) should be simulated and optimised. The pair of networks that are to be used in the end should be selected such that the bandwidth of the amplifier is maximized. Recall that there exists a number of $\lambda/4$ and non $\lambda/4$ type matching networks and that all shunt stubs can be balanced or unbalanced. Each type of network has a different frequency response and the frequency response of the amp will depend on the combination of matching networks and on the device. You may do the paper design assuming lossless lines but should account for losses in the simulation.

The transistors will be biased using two independent dc power supplies; you must design bias tee's (rf choke and dc block) and incorporate them at the input and output of your amplifier. Your amplifier must be dc isolated. A variety of chip capacitors are available and specifications are attached along with their physical dimensions. 50 Ω chip resistors are also available.

It is important that the physical dimensions of all external elements (Xtor, C, R) be taken into account in your design so that they can be soldered adequately in the final circuit. The last two digits in the product number of HP devices correspond to the package used. The physical description of the package is given in the specification sheets provided. You may assume that the common emitter S parameters provided by the manufacturer have been de-embedded such that the reference planes should be taken at the body of the device on the input (base) and output (collector) leads. The transistor must be positioned over the rectangular area (the hole) in the test jig in order to accommodate for the emitter legs that must be soldered on the backplane of your substrate (you must drill through the substrate to solder the emitter leads of the transistor).

Simulation Work

The design of all circuits must be done on paper first and then simulated, refined and optimized using a commercial industry-standard computer-aided-design package, comprising a circuit simulator that can be used as a design aid to obtain the theoretical performance of a realistic microwave circuit before fabrication. **Simulation tutorials are scheduled as described below - attendance to these tutorials is mandatory for all students.** Instructions on how to access the software package will be provided during our first simulation tutorial. Don't leave your simulation work to the last minute!

Microwave Test Jig and Circuit Layout

Your circuit is to be mounted in a special microwave test jig for which a drawing is attached. Make sure that your final circuit layout fits the dimensions: 2.000 × 2.750 inches. **Also, it is critical that all access lines on your circuit line up with the microwave launchers (coax to microstrip transitions).**

The layout of the circuit to be fabricated can be produced using a computer drawing tool of your choice (*e.g.*, AWR, ADS, Autocad, Illustrator,…), but the layout file to be submitted must be of high resolution and in the format of a Gerber (.gbr) file - no other formats will be accepted. Please prepare the layout on a single layer (defined as the "top layer" in CAD software). The layout must be prepared such that **everything that is to be copper will be black** and **everything to be etched will be white** - grayscale should not be used so save in black and white only. The scale for the layout must be 1:1. The electronic file of your layout must be submitted to Mr. Jean-Noël Nugu by email at jnugu@uottawa.ca; the email subject line must state ELG 4115 and your group number. A printed version (on standard white paper) of the layout **must** also be submitted to Mr. Nugu at room CBY B518; you can slide it under the door if required (put it in an envelope).

Obviously, circuit layout is critical at microwave frequencies so make sure that you measure accurately and sketch straight. **Include cutting guides at all four corners** of your layout; your substrate will be trimmed along the **outside** edge of your cutting guides. All mounting holes required in your substrate must be located away from any circuit feature and should also be included on your layout, marked via a small filled circle. Identify your layout by your group number (or a unique symbol) somewhere in a non-critical region of the circuit.

Check your layout printed copy so that:

- Its scale is exact (*i.e.* 2.0 × 2.750 inches) along the outside edges of the cutting guides
- Your cutting guides are only in the corners and are fairly wide (min. 1/8 in)
- You have space between the launchers and the blocking capacitors
- You have lined up the access microstrip lines to the launchers on the jig
- Your group number is visible and cannot be reversed (*i.e.* 6)
- Your printed copy should be made with a high quality laser printer
- If you see ragged edges then your electronic copy is of too low a resolution
- The mounting holes are drilled through the board away from your circuit features

Laboratory Work

The practical portion of the work will be held in the Electromagnetics Laboratories: room CBY B520 for the hardware mounting work and CBY B519 for the circuit testing and measurements. The lab can accommodate only four groups at a time as there are a limited number of assembly and measurement benches. A laboratory schedule prepared on a group basis will be provided shortly; extra lab time with the TA can be negotiated with the TA, the laboratory technician **must be present** whenever the students are in the lab. A fabrication and measurement kit will be necessary; you may borrow one for the duration of your lab session in exchange for a student card. The kit contains useful tools and coaxial elements that are required for the calibration of the analyzers and for the measurements. **An anti-static wrist band must be used whenever handling a device that is sensitive to electrostatic discharge such as transistors or chip capacitors, or whenever you are manipulating the vector network analyzers or other microwave test instruments.** During your first scheduled lab session, the TA will give a short presentation on the operation of the microwave network analyzers.

The Electromagnetics Lab room CBY-B518 and the Fabrication Lab room CBY-B520 are under the responsibility of **Mr. Jean-Noël Nugu**, room CBY-B518, email: jnugu@uottawa.ca

Soldering

Soldering work will be required to make good electrical connections between your access lines and the launchers and to mount any external device to your circuit. To create a proper hot joint you must:

- use an iron at about 700 F or 371 ^{o}C,
- clean the tip of the iron using the wet sponge,
- tin the tip,
- quickly heat the work then apply the solder to the work, not the iron.

Engineering Report Guidelines

Your final report must be prepared according to the standard format generally used for the preparation of an engineering technical report. It must contain the following parts in order:

- **Title Page**. It gives the title of the report and identifies its authors. It is clear that if an author's name appears on the title page then she/he has participated actively in the work and agrees with the contents of the report.

- **Abstract**. One paragraph that summarizes the topic, methodology and main results presented in the report.

- **Introduction**. The introduction addresses the objectives of the project, describes the circuits to be designed, discusses the applications of the circuits, and describes the design cycle or methodology that was followed.

- **Body**. The body is the main part of a technical report. It must contain the following:
  - Preliminary paper design work.
  - Complete set of simulation results for the designed circuits (including simulation results for the parameters of importance related to the individual circuits).
  - Pertinent measurement results for the fabricated circuit (including measurements of the specific parameters of importance related to the circuit) **signed by the T.A**.
  - Insightful and intelligent discussion of the results.
  - Suggestions for improvements for the next design cycle.

- **Conclusion**

- **Presentation guidelines**:
  - concise writing style
  - typed report
  - a 12pt font double-spaced
  - 0.75 inch margins all around
  - Bound

Marking Scheme:

- 90% of the mark goes to the body of the report:
  - 20% for the paper design,
  - 20% for the simulation and optimization work (enough to justify the chosen design, also include the simulation results for the complete amplifier including bias tees and DC blocks),
  - 30% for the lab measurements signed by the T.A. (magnitude of S_{11}, S_{22}, S_{21}, S_{12} and the phase of S_{21} over the bandwidth of the amplifier),
  - 20% for the discussion and suggestions for improvements (if any are needed).
- 10% of the mark goes to the rest of the report.

ELG 4115 Project Scheduling Information: Winter 2023

The T.A. for the course is:

- Mohammed Nassor, mnass091@uottawa.ca

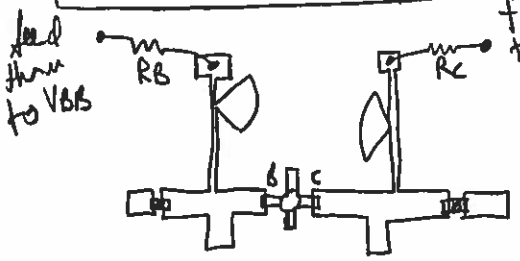
A project design tutorial given by Prof. Berini is scheduled for Thursday February 16th, 10:00 am - 11:00 am (our regular lab slot) but in ARC 233. Two simulation and design tutorials given by the T.A. are scheduled for March 6th and March 13th, 8:30 am - 10:00 am, in CBY B202 (our regular DGD slots). Bring a laptop with you on which you have downloaded the AWR RF/Microwave Design & Analysis package (please obtain a free student license or trial version on your own https://www.ema-eda.com/products/cadence/systems-analysis/awr-overview2#awr-trial). **Attendance to these three tutorials is mandatory for all students**.

The due date for the layout is **Tuesday March 14th at 10 am. THIS DEADLINE IS ABSOLUTELY FIRM**. The circuits will be ready in time for the first laboratory session, starting on March 16th. The final report is due on April 12th, uploaded to our Brightspace website.

Each group will be assigned lab slots and each group must be present during their lab slot to receive their circuit and a microwave test jig, and to hear the presentation on the use of the network analyzers given by the T.A. The lab schedule will be posted shortly on our Brightspace course page - consult this schedule to find out when your group should come to the lab. You may schedule extra lab time with the T.A. if you require help. The lab is accessible outside of our lab times, as long as the technician is present, and as long as you have been trained on the use of our network analyzers. **All experimental results incorporated in your report must be signed by the T.A.**

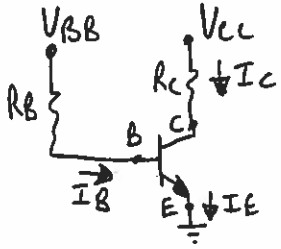
Feed-thru:  LPF.

Biasing the BJT



- the resistors R_B & R_C increase the resistance of r.f. feed back paths through the D.C. supplies.
- Increases low-f stability

D.C. Analysis:



KVL (BE): $-V_{BB} + I_B R_B + V_{BE} = 0$

$$V_{BB} = I_B R_B + V_{BE} \quad (1)$$

KVL (CE): $-V_{CC} + I_C R_C + V_{CE} = 0$

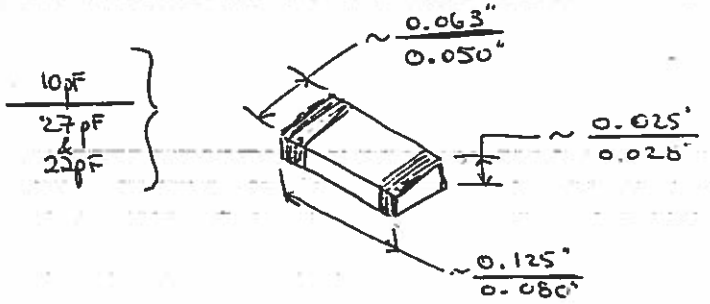
$$V_{CC} = I_C R_C + V_{CE} \quad (2)$$

Active mode operation: $\Rightarrow I_C = \beta I_B = \alpha I_E$

& $\beta \cong 150$ for 605, 420 & 414

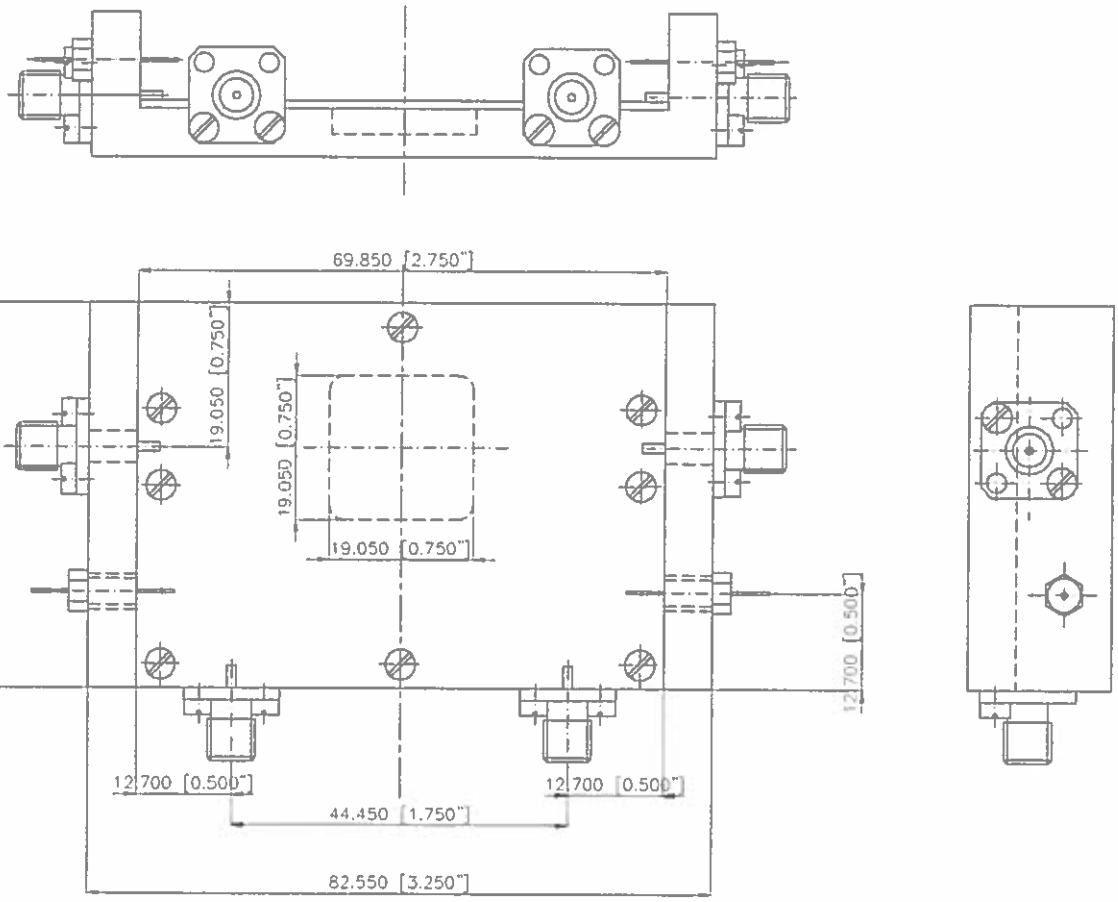
- Power supplies have $V_{max} = 25$ V
- All standard R's are available
- to bias device apply Vcc first then VBB

chip Capacitors



Use the 27 pF capacitors.

All dimensions are in inches.


69.850 [2.750"]
19.050 [0.750"]
19.050 [0.750"]
19.050 [0.750"]
50.800 [2.000"]
12.700 [0.500"]
12.700 [0.500"]
12.700 [0.500"]
44.450 [1.750"]
82.550 [3.250"]