Efficient CAD Tool for RF/Microwave Transistor Modeling

Mustapha C.E. Yagoub [1], F.A. Mohammadi [2]

[1] SITE, University of Ottawa, 800 King Edward, Ottawa, ON, Canada, K1N 6N5
[2] Dept of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada, M5B 2K3

Abstract **— As microelectronic technology continues to progress, there is an ever-increasing demand for higher levels of system integration and circuit miniaturization. This trend leads to highly repetitive computational tasks during simulation, optimization and statistical analyses, requiring fast and accurate modeling tools. This paper presents a robust technique for extracting the most suitable small-signal equivalent model of a given transistor. The proposed approach is demonstrated through examples of field effect and heterojunction bipolar transistor characterization.**

Index Terms **— Extraction, FET, fuzzy logic, HBT, modeling, neural networks.**

I. Introduction

With ever-higher integration and smaller layout size, RF/microwave circuit design needs highly repetitive computational tasks. This trend requires a permanent upgrading of existing modeling tools so that the design can be achieved reliably [1]. At the circuit level, the efficiency of such tools relies heavily upon the speed and accuracy of the existing component models. In the recent years, a computer-aided design (CAD) approach based on neural (NN) and fuzzy-neural networks (FNN) has been introduced for RF/microwave device modeling, simulation and optimization [2]-[4]. Fast and accurate neural models can be utilized in place of computationally intensive physics/EM models to speed-up the overall design process.

In this paper, the authors used NN and FNN techniques to model field effect (FETs) and heterojunction bipolar transistors (HBTs) [2]. The efficiency of the proposed tool is demonstrated through examples of FET and HBT modeling.

II. Transistor Modeling

Since FETs and HBTs are widely used in RF/microwave, a large number of modeling approaches are being proposed [5]-[7]. Detailed physics-based transistor models are accurate but slow. Table look-up models can be fast, but suffer from the disadvantages of large memory requirements and limitations on number of parameters. Nevertheless they are difficult to develop, equivalent circuit models remain the most used modeling approach, where the element values can be determined either by direct extraction [5] or by optimization-based extraction [6]. Fast and simple to implement, direct-extraction techniques provide adequate values for the more dominant circuit model elements but they cannot determine all the extrinsic elements uniquely [7]. On the other side, optimization-based extraction techniques are more accurate but computationally intensive and relatively sensitive to the choice of starting values. Furthermore, in order to make them attractive to non-experienced users, such extraction techniques often assume a *prior universal* circuit topology referred as the *FET standard topology* or FET circuit #1 (Fig. 10) [8] and the *HBT standard topology* or HBT circuit #1 (Fig. 2) [9]. Determining the most suitable small-signal equivalent circuit topology and accurately extracting its element parameters was the aim of the proposed approach.

Based on a large literature review, the authors created a library with different circuit topologies displayed in Fig. 3 to 6 [10]-[13] and in Fig. 7 to 10 [9], [14]-[16] for FETs and HBTs, respectively. For a given transistor, a standard topology extraction [5] was then performed and the obtained S-parameters ($S_{ij}^{\mathbf{s}}$, $i, j = 1, 2$) from the standard topology were compared to the measured S-parameters (denoted as $S_{ij}^{\mathbf{m}}$, $i, j = 1, 2$). If the difference is greater than the user-defined error, a new circuit topology should be selected from the library. By combining the Fuzzy c-means (FCM) method [17] and the small-signal representation of the device behavior, the aim was to select the most suitable transistor topology.

In this work, for any circuit *#k* from the library, the related $\mathbf{S}^{\mathbf{k}}$ matrix was compared to the given input $\mathbf{S}^{\mathbf{m}}$ matrix and each element of the 2x2 error matrices $\mathbf{E}^{\mathbf{k,\,Re}}$ and $\mathbf{E}^{\mathbf{k,\,Im}}$,

$$E_{ij}^{\mathbf{k,Re}} = \mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right) \quad i,j = 1, 2 \qquad (1)$$

$$E_{ij}^{\mathbf{k,Im}} = \mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right) \quad i,j = 1, 2 \qquad (2)$$

will receive a score depending on its value (based on the FCM technique). Thus, topology *#k* with smallest $\mathbf{E}^{\mathbf{k,\,m}}$,

$$E^{\mathbf{k,m}} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left\{\left[\mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{m}}\right)\right]^2\right\} \qquad (3)$$

i.e., smallest score, will be selected as the most suitable equivalent model. Here, Re(*) and Im(*) denote real part and imaginary part respectively. Finally, a simple extraction will be performed to determine final element values of the selected topology. However, since there is *no prior* knowledge on the input S-parameters, it is impossible to compute numerically (3).

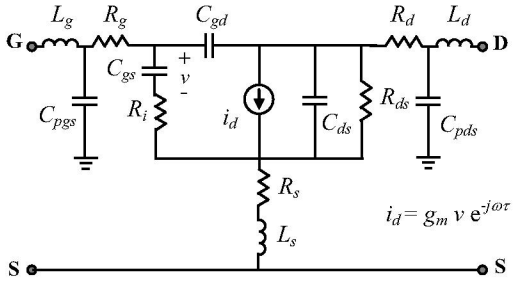

Fig. 1. FET standard circuit topology (# 1) [8].

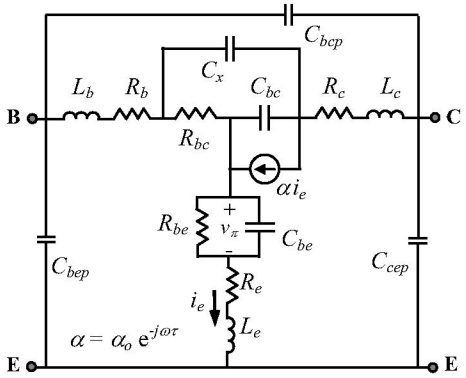

Fig. 2. HBT standard circuit topology (#1) [9].

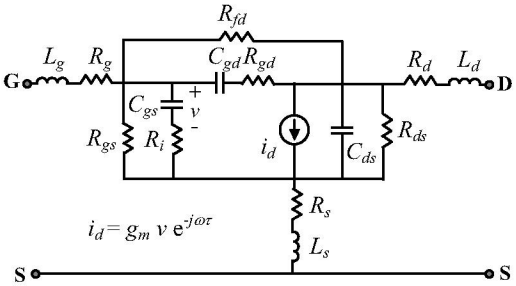

Fig. 3. FET circuit topology #2 as reported in [10].

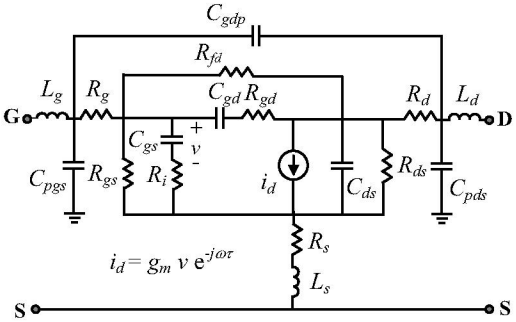

Fig. 4. FET circuit topology #3 as reported in [11].

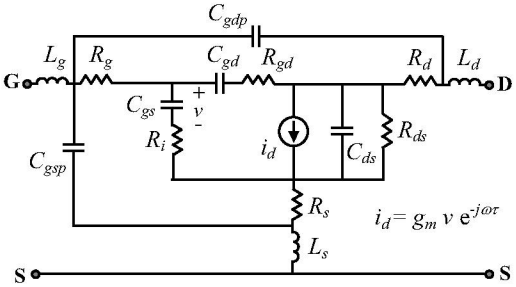

Fig. 5. FET circuit topology #4 as reported in [12].

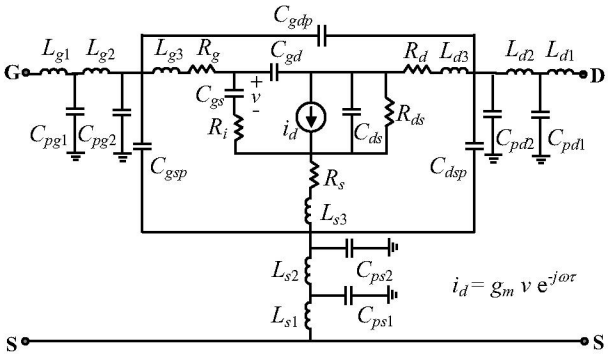

Fig. 6. FET circuit topology #5 as reported in [13].

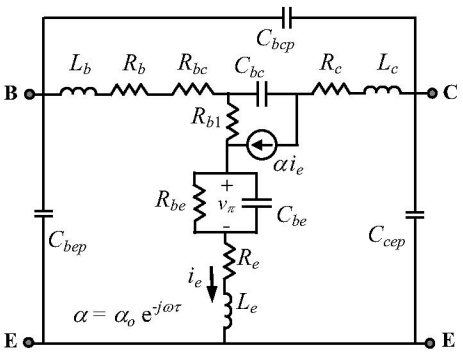

Fig. 7. HBT circuit topology #2 as reported in [9].

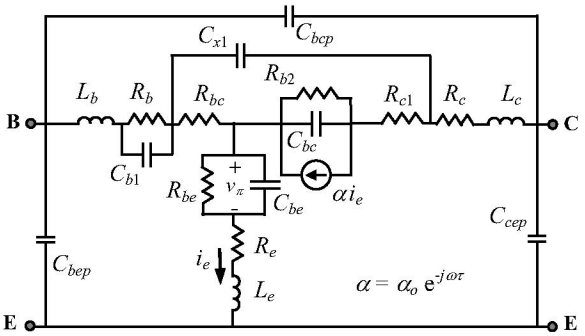

Fig. 8. HBT circuit topology #3 as reported in [14].

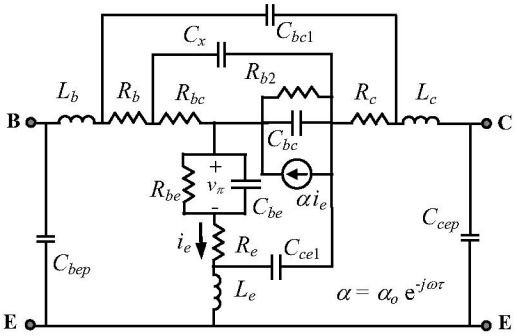

Fig. 9. HBT circuit topology #4 as reported in [15].

Let $\{\Omega^{\mathbf{s}}\}$ be the set of P_s elements $\Omega^{\mathbf{s}}_p$ ($p = 1, \ldots, P_s$) in the standard topology. A symbolic code was developed using [18] to analytically derive the following nonlinear functions

$$S^{\mathbf{k}}_{ij} = f^{\mathbf{k}}_{ij}\left(S^{\mathbf{s}}_{ij}, \{\Omega^{\mathbf{k}}\}\right) \quad i,j = 1, 2 \quad k = 1, \ldots, 5 \qquad (4)$$

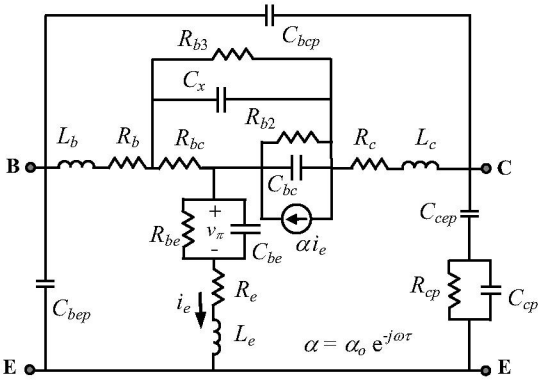

Fig. 10. HBT circuit topology #5 as reported in [16].

where $\{\Omega^{\mathbf{k}}\}$ is the set of the P_k elements added in circuit #k versus the standard topology, e.g.,

$$\{\Omega^2\}_{FET} = \{R_{fd}, R_{gd}, R_{gs}\}\big|_{C_{pgs}=C_{pds}=0}$$

$$\{\Omega^3\}_{FET} = \{R_{fd}, R_{gd}, R_{gs}, C_{gdp}\}$$

$$\{\Omega^4\}_{FET} = \{R_{gd}, C_{gdp}, C_{gsp}\}\big|_{C_{pgs}=C_{pds}=0}$$

$$\{\Omega^5\}_{FET} = \left\{\begin{array}{l} C_{gdp}, C_{gsp}, C_{dsp}, C_{pg1}, C_{pg2}, \\ C_{ps1}, C_{ps2}, C_{pd1}, C_{pd2}, L_{g1}, \\ L_{g2}, L_{s1}, L_{s2}, L_{d1}, L_{d2} \end{array}\right\}\Bigg|_{C_{pgs}=C_{pds}=0}$$

for the FET, and

$$\{\Omega^2\}_{HBT} = \{R_{b1}\}\big|_{C_x=0}$$

$$\{\Omega^3\}_{HBT} = \{C_{b1}, C_{x1}, R_{b2}, R_{c1}\}\big|_{C_x=0}$$

$$\{\Omega^4\}_{HBT} = \{C_{bc1}, R_{b2}, C_{ce1}\}\big|_{C_{bcp}=0}$$

$$\{\Omega^5\}_{HBT} = \{R_{b3}, R_{b2}, R_{cp}, C_{cp}\}$$

for the HBT. Therefore, the following alternative fuzzy criteria can be defined for each topology #k

$$E^{\mathbf{k},\mathbf{s}} = \sum_{i=1}^{2}\sum_{j=1}^{2}\left\{\left[\mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right)\right]^2 + \left[\mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right)\right]^2\right\} \qquad (5)$$

Since these equations are strongly interdependent and highly nonlinear, we used NNs to learn them. By varying the values of the elements Ω^{k}_p (p = 1, …, P_k) of set $\{\Omega^{\mathrm{k}}\}$, we can compute the $\mathbf{S}^{\mathbf{k}}$ scattering matrix and therefore, the difference $\{\mathbf{S}^{\mathbf{k}} - \mathbf{S}^{\mathbf{s}}\}$. The resulting data in the form of

$$Tr^{\mathbf{k}} = \left[\underbrace{\mathrm{Re}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right), \mathrm{Im}\left(S_{ij}^{\mathbf{k}} - S_{ij}^{\mathbf{s}}\right)}_{8\ \text{inputs}\ \ (i,j=1,2)}, \underbrace{\Omega_1^{\mathbf{k}}, \ldots, \Omega_{p_{\mathbf{k}}}^{\mathbf{k}}}_{p_{\mathbf{k}}\ \text{outputs}}\right] \qquad (6)$$

was submitted to a three-layer (MLP3) neural network structure for training using [19]. The input layer has 9 neurons (the 4 real and 4 imaginary parts in (6) and the operating frequency f) while the output layer contains P_k neurons. The hidden layer is composed of 22 to 45 neurons depending on the circuit data file under training. A final extraction is then performed with vector

$$\Omega = \left[\Omega_1^{\mathbf{k}}, \ldots, \Omega_{P_{\mathbf{k}}}^{\mathbf{k}}, \Omega_1^{\mathbf{s}}, \ldots, \Omega_{P_{\mathbf{s}}}^{\mathbf{s}}\right] \qquad (7)$$

as starting vector for the final optimization round. Since this vector is close to the final solution, this procedure assures a very fast convergence. In fact, the maximum number of iterations for 100 different sets of S-parameters did not exceed ten iterations with a maximum computing time of 11s and a user predefined error of 1%.

III. Examples

The first device to be characterized is the FET reported in [4] using topology #4. Since in this paper all circuit element values are given as well as the final error between measured and simulated S-parameters, a reliable comparison can be performed for a full validation. In fact, by comparing the S-parameters (Fig. 11) and the extracted values given in [4] with those obtained in 2.3 seconds using our technique, topology #4 achieved the closest agreement with a smaller final error (2.9% vs. the 8.4% in [4]) defined for a set of N_f selected frequency values fq (q = 1, …,, N_f) as [4]

$$E^{\mathbf{k},\mathbf{m}} = \sum_{q=1}^{N_f}\sum_{i=1}^{2}\sum_{j=1}^{2}\left|1 - \frac{S_{ij}^{\mathbf{k}}(f_q)}{S_{ij}^{\mathbf{m}}(f_q)}\right|^2 \qquad (8)$$

The second device to be modeled is an InP/GaInAs HBT proposed in [15] using topology #4. A similar close agreement is shown with published results (Fig. 12).

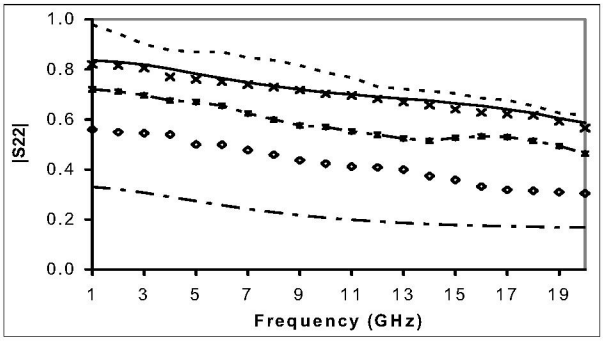

Fig. 11. FET: Comparison of input S_{22} (x) with those extracted using standard topology (– – – –), topology #2 (- - -), topology #3 (◊), topology #4 (—) [4], and topology #5 (– – –).

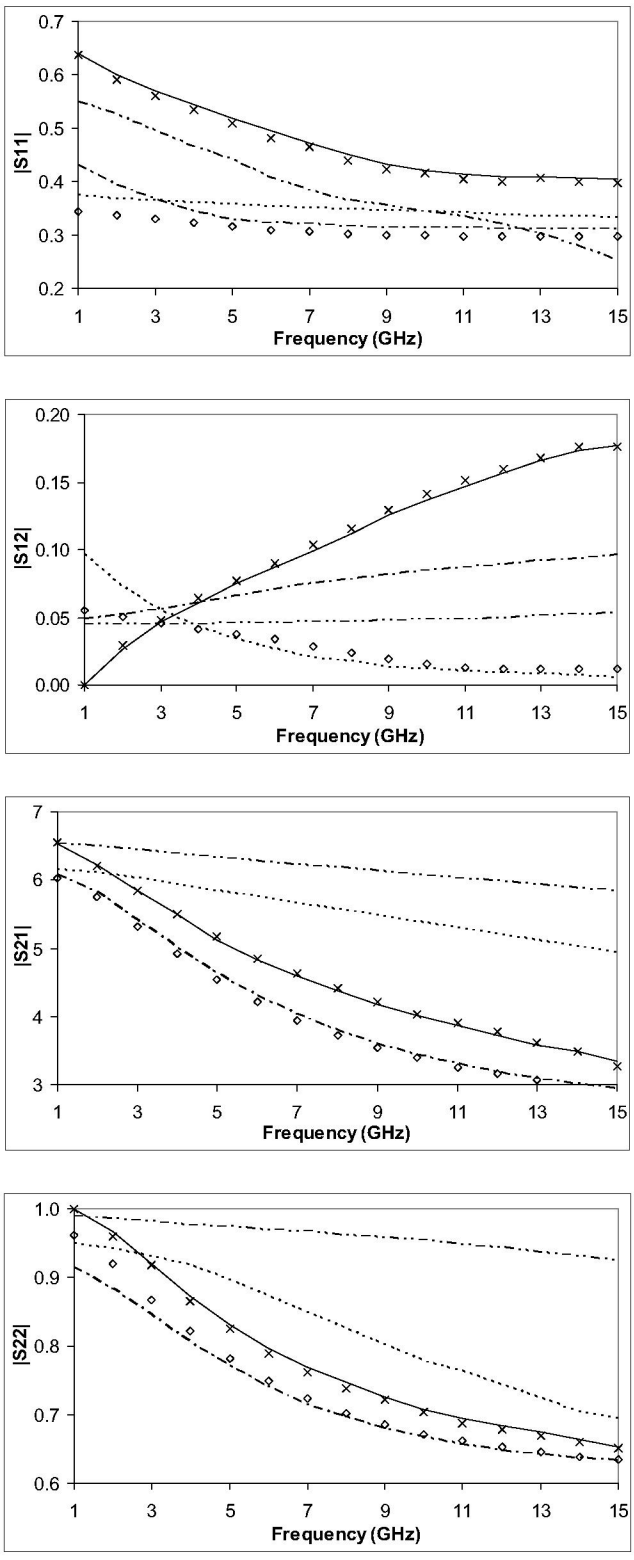

Fig. 12. HBT: Comparison of input S-parameters (x) with those extracted using standard topology (— - - —), topology #2 (- - -), topology #3 (◊), topology #4 (—) [15], and topology #5 (— — —).

IV. Conclusion

In this paper, an efficient CAD tool was presented that combines fuzzy and neural techniques to predict the most suitable small-signal circuit of a given transistor. It will be shortly extended to include the nonlinear transistor behaviors.

Acknowledgement

This work is supported in part by Natural Science and Engineering Research Council of Canada.

References

[1] T. Edwards, "Countdown to the microwave millenium", *Microwave J.*, Vol. 41, pp. 70-81, 1998.

[2] Q.J. Zhang, K.C. Gupta, *Neural Networks for RF and Microwave Design*, Norwood: Artech House, 2000.

[3] M.C.E. Yagoub, "Optimisation des performances de modules multi-puces. Modélisation par réseaux de neurones," *Annales des Télécomm.*, Vol. 59, pp. 941-966, Sept.-Oct. 2004.

[4] M.K. Ahmed, S.M.M. Ibrahem, "Small signal GaAs MESFET model parameters extracted from measured S-parameters," *Nat. Radio Science Conf.*, Cairo, Egypt, pp. 507-515, 1996.

[5] J.M. Golio, *Microwave MESFETs and HEMTs*, Boston: Artech House, 1991.

[6] L. Fujiang, G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search-a new concept," *IEEE Trans. Microwave Theory Tech.*, Vol. 42, pp. 1114-1121, 1994.

[7] C. Van Niekerk *et al.*,"A robust integrated multibias parameter-extraction method for MESFET and HEMT models," *IEEE Trans. Microwave Theory Tech.*, Vol. 48, pp. 777-786, 2000.

[8] G. Dambrine *et al.*, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, Vol. 36, pp. 1151-1159, 1988.

[9] P.J. Tasker, M. Fernandez-Barciela, "HBT small signal T and Π model extraction using a simple, robust and fully analytical procedure", *IEEE MTT-S Int. Symp.*, pp. 2129–2132, 2002.

[10] R. Menozzi *et al.*, "Small-signal modeling for microwave FET linear circuits based on a genetic algorithm," *IEEE Trans. Circuits and Systems*, Vol. 43, pp. 839-847, 1996.

[11] M. Fernandez-Barciela *et al.*, "A simplified broad-band large-signal nonquasi-static table-based FET model," *IEEE Trans. Microwave Theory Tech.*, Vol. 48, pp. 395-405, 2000.

[12] R. Anholt, S. Swirhun, "Equivalent-circuit parameter extraction for cold GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, Vol. 39, pp. 1243-1247, 1991.

[13] *ADS* 2004, *Agilent Technologies*, Palo Alto, CA, USA.

[14] J.M.M. Rios *et al.*, "A self-consistent method for complete small-signal parameter extraction of InP-based heterojunction bipolar transistors", *IEEE Trans. Microwave Theory Tech.*, Vol. 45, pp. 39-45, 1997.

[15] B. Sheinman *et al.*, "A peeling algorithm for extraction of the HBT small-signal equivalent circuit", *IEEE Trans. Microwave Theory Tech.*, Vol. 50, pp. 2804-2810, 2002.

[16] T. H. Teo *et al.*, "Systematic direct parameter extraction with substrate network of SiGe HBT", *Radio Frequency Integrated Circuits Symp.*, pp. 603-606, 2004.

[17] C. Fager *et al.*, "Optimal parameter extraction and uncertainty estimation in intrinsic FET small-signal models," *IEEE Trans. Microwave Theory Tech.*, Vol. 50, pp. 2797-2803, 2002.

[18] Maple 8, *Maplesoft*, Waterloo, ON, Canada.

[19] *NeuroModeler* 1.2, Carleton U., Ottawa, Canada.