A High-Power, Low-Loss W-band SPDT Switch Using SiGe PIN Diodes

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***Abstract* — This paper presents a W-band SPDT switch implemented using PIN diodes in a new 90 nm SiGe BiCMOS technology. The SPDT switch achieves a minimum insertion loss of 1.4 dB and an isolation of 22 dB at 95 GHz, with less than 2 dB insertion loss from 77-134 GHz, and greater than 20 dB isolation from 79-129 GHz. The input and output return losses are greater than 10 dB from 73-133 GHz. By reverse biasing the off-state PIN diodes, the P_{1dB} is larger than +24 dBm. To the authors' best knowledge, these results demonstrate the lowest loss and highest power handling capability achieved by a W-band SPDT switch in any silicon-based technology reported to date.**

***Index Terms* — millimeter wave integrated circuits, single-pole double-throw, SPDT switch, PIN diode, SiGe, W-band.**

I. Introduction

Recent developments in sub-100 nm SiGe BiCMOS technology include optimized PIN diodes, creating attractive platforms for implementing fully integrated millimeter-wave front-ends. For either pulsed radar or communications front-ends, a single-pole double-throw (SPDT) switch is an essential component. The loss of the SPDT is critical as it both reduces the transmitter's output power as well as contributes to the receiver's noise figure. Therefore, reducing loss and improving power handling of the SPDT switch are important factors for increasing the limited dynamic range of typical integrated mm-wave systems. This paper demonstrates a state-of-the-art W-band SPDT switch implemented utilizing PIN diodes in a newly-developed 90 nm SiGe BiCMOS technology, achieving insertion loss and power handling performance comparable to W-band PIN SPDT switches in competing III-V compound semiconductor technologies.

II. Technology Overview

The switch is fabricated in IBM's 90 nm SiGe BiCMOS technology (IBM 9HP). The process features high-speed SiGe HBTs with $f_T/f_{MAX}/BV_{CEO}$ of 300 GHz/350 GHz/1.5 V. The back-end-of-line (BEOL) consists of four Cu digital metals, four Cu intermediate metals, one thick Cu metal, and an Al thick RF metal, as shown in Fig. 1. Low-loss, 50 Ω microstrip transmission lines are designed using a 21 µm-wide LD metal layer over the lower digital metal layers, which are connected together in a cross-hatch pattern to form the ground-plane.

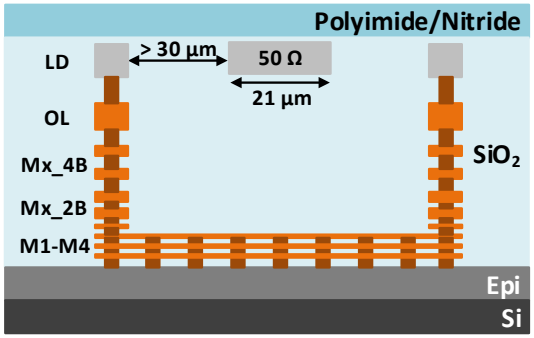

Fig. 1. Cross-section of IBM's 90 nm, 10 metal-layer BEOL.

The PIN diodes in this process are targeted for operation at 60 and 77 GHz, as described in [1]-[2]. The p+ anode is formed by the extrinsic SiGe HBT base epitaxial film, the intrinsic region is formed by silicon epitaxial growth, and the cathode is formed by a deep n+ implant with an n+ reach-through to contact the cathode, as shown in Fig. 2 [1]. Typically, the HBT sub-collector is used as the n+ cathode to reduce cost; however, due to the shrinking distance between the base epitaxial film and sub-collector of state-of-art HBTs, this results in high anode-cathode capacitance [2]. Thus, in the present case, the formation of the PIN diode's deep n+ implant is decoupled from the HBT's sub-collector to reduce the intrinsic capacitance and improve the performance at mm-wave frequencies.

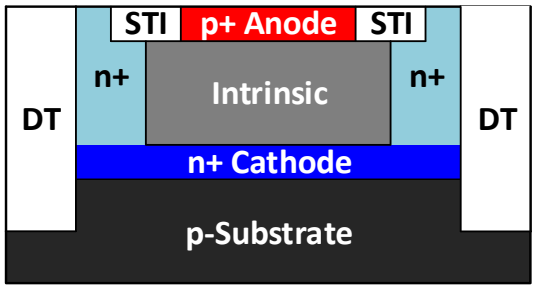

Fig. 2. Cross-section of a vertical SiGe PIN diode.

III. Circuit Design

The schematic and chip micrograph of the SPDT switch are shown in Fig. 3. The IC occupies an area of 580 x 240 μm^2 without RF pads.

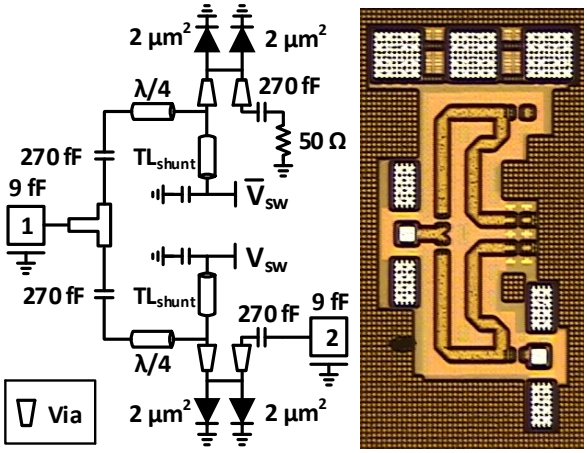

Fig. 3. Schematic and chip micrograph of the SPDT switch.

Due to non-negligible device parasitics at mm-wave frequencies, there are a limited number of topologies to be considered for a SPDT switch. A series-shunt switch topology can eliminate the need for a quarter-wave (λ/4) transformer; however, receiver and transmitter circuits often need the spacing created from the quarter-wave transformer, eliminating the benefit of a small SPDT switch. Series-shunt topologies also have increased series resistance in the thru-state with proper sizing for the off-state, and increased biasing complexity as compared to the λ/4 shunt topology. For these reasons, the λ/4 shunt SPDT switch topology is popular at mm-wave frequencies. However, in this topology it is a critical design criteria to maintain high isolation.

For λ/4 shunt SPDT switch operation, the PIN diodes in one arm are turned on, such that they present a short circuit that is transformed to an open at the common port after the 50 Ω λ/4-transmission line. The PIN diodes in the opposite path are turned off such that Z_{IN} seen from the common port is 50 Ω.

Reducing the on-state resistance and increasing the off-state resistance while minimizing the off-state shunt capacitance of the PIN diodes is essential in order to both maximize the reflection of the isolation path and to minimize the insertion loss over a wide bandwidth. Small devices have high on-state resistance, which leads to a deviation from a perfect short, resulting in poor isolation and increased insertion loss. Larger devices, on the other hand, have a low off-state resistance and an increased off-state capacitance, which increases the insertion loss and reduces the bandwidth of the SPDT switch. The device sizing trade-offs are illustrated in Fig. 4.

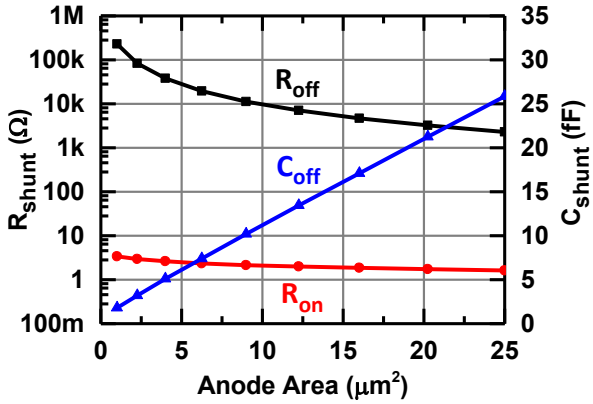

Fig. 4. Ideal on- and off-state shunt resistance and off-state shunt capacitance over PIN diode anode area at 94 GHz.

The high ratio between $R_{Shunt-off}$ and $R_{Shunt-on}$ of the PIN diodes, as compared to CMOS and SiGe HBTs for a reasonable anode area, allows for attaining unprecedented performances; however, careful attention needs to be paid to the layout of the devices such that the isolation is not compromised. In order to maximize the isolation using only a single shunt section per arm of the SPDT, the via and interconnect parasitics were incorporated into the transmission line in a similar fashion as [3], such that the isolation does not degrade as significantly over frequency due to the imaginary impedance presented by the via interconnects of the PIN diodes. This approach is shown in Fig. 5 (b) and compared with the conventional approach in Fig. 5 (a).

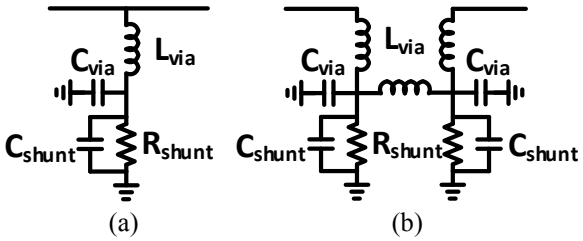

Fig. 5. Via parasitics with PIN diode equivalent model for the (a) conventional approach and the (b) distributed approach.

The off-state shunt capacitance of the PIN diodes is resonated out by a shorted shunt-stub (TL_{Shunt} in Fig. 3). The RF short is provided by MIM capacitors, with the DC bias for the PIN diodes applied at this point. The input and output of each switch arm are DC-blocked using MIM capacitors sized to be series resonant at 94 GHz.

One of the ports of the SPDT switch is terminated on-chip with a 50 Ω TaN resistor to facilitate on-chip measurement. Finally, to allow the use of negative biasing for high power handling in the off-state, TaN resistors were used instead of n-well connections in order to provide discharge paths for some of the MIM capacitors to prevent dielectric breakdown during fabrication.

IV. Measurements

The S-parameters were measured from 0.05-110 GHz using an Anritsu ME7808C VNA with mm-wave extenders and 1-mm coax probes, and also measured from 110-170 GHz using an Agilent E8364B VNA with OML D-band extenders and WR-6 probes. Both measurements utilized a probe-tip LRRM calibration.

The simulated and measured S-parameters of the SPDT switch are shown in Figs. 6 and 7. The RF pads were not de-embedded from the S-parameter measurements, but given a typical BeCu probe tip to Aluminum pad contact resistance of 1-2 Ω as shown in [4], this results in a total insertion loss contribution of 0.17 – 0.34 dB.

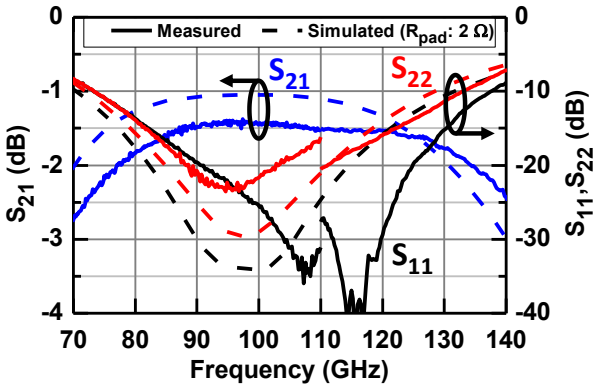

Fig. 6. Measured vs. simulated S-parameters (insertion loss).

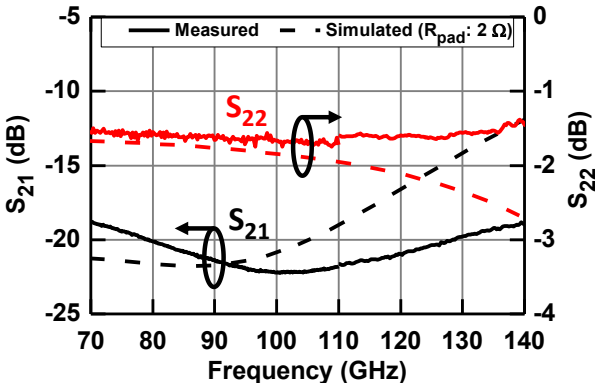

Fig. 7. Measured vs. simulated S-parameters (isolation).

The bias voltages for the insertion loss state were $V_{sw} = -4\,V$ and $\overline{V}_{sw} = 1.2\,V$, and vice versa for the isolation state. The DC power consumption of the SPDT switch with one arm in the on-state is 10.2 mW at 1.2 V.

The SPDT achieves a minimum insertion loss of 1.4 dB at 95 GHz with less than 2 dB insertion loss from 73-133 GHz. A maximum isolation of 22.2 dB is achieved at 100 GHz with greater than 20 dB isolation from 79-129 GHz. Input return loss is greater than 10 dB from 73-137 GHz, and output return loss is greater than 10 dB from 73-133 GHz.

After considering the aluminum pad contact resistances, the simulated insertion loss lines up more closely with the measured result. The remaining differences may be attributed to inaccuracies in the initial PIN diode device model and reduced Q-factor of device interconnects as compared to EM simulations.

The large-signal measurement setup consisted of a Millitech 6x multiplier and mechanical step attenuator, a Quinstar 90-96 GHz power amplifier, Maury WR-10 tuners, a fixed 10 dB attenuator, a HP WR-10 power sensor, and WR-10 probes.

The large-signal behavior was measured with the tuners set to present 50 Ω to the DUT at 92 GHz, where the instrumentation PA produced a peak output power of +24 dBm at the probe tip. The input power was fed to port 2, and the output power was measured at port 1 of Fig. 3. This bypasses the loss of the quarter-wave section to report P_{1dB} in a more accurate form for front-end modules. The measured large-signal results are shown in Fig. 8.

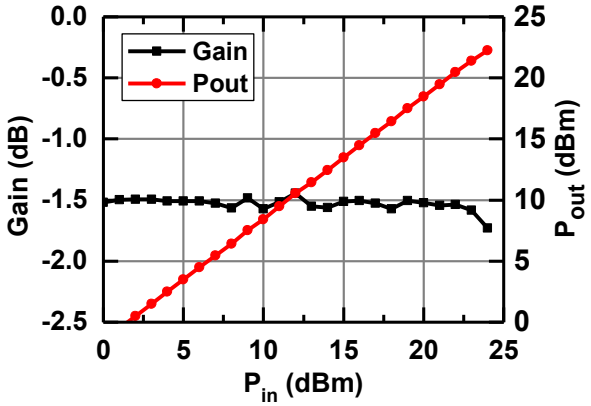

Fig. 8. Measured P_{out} and Gain across P_{in} at 92 GHz.

Due to the lack of a reverse breakdown in the preliminary PIN diode model, the power handling of the thru state was initially estimated through hand calculations. The negative RF voltage swing is limited to the design manual's specified reverse breakdown of -8.2 V. The positive swing is limited by the turn-on voltage of the diode of about 0.6

V. The DC bias point of V_{sw} is set at the midpoint at -4 V to allow for maximum RF voltage swing. Given a 50 Ω load and a RF voltage swing with a $V_{Peak-Peak}$ of 8.8 V, this results in a maximum linear region of operation up to +23 dBm, which agrees well with the measured results given that the PIN diodes are not fully conducting at the given voltage extremities. In Fig. 8, the thru state started to show signs of compression at +24 dBm, but did not reach P_{1dB} due to the limited available source power from the measurement setup.

TABLE I
COMPARISON OF STATE-OF-THE-ART W-BAND SPDT SWITCHES

Reference	[5]	[6]	[7]	[8]	**This Work**
Technology	GaAs	130nm SiGe	130nm SiGe	90nm SiGe	**90nm SiGe**
Device	PIN	nMOS	PIN	HBT	**PIN**
Topology	λ/4 shunt	λ/4 shunt	Series-shunt	λ/4 shunt	**λ/4 shunt**
Freq. (GHz)	75-110	85-105	50-78	77-110	**73-133**
Insertion Loss (dB)	1.1-1.6	2.3-3.0	2.0-2.7	1.4-2.0	**1.4-2.0***
Isolation (dB)	21-22	20-21	25-35	17.5-19	**19-22**
P_{1dB} (dBm)	-	-	-	+19	**> +24****
Area (mm^2)	0.94	0.05	0.11	0.14	**0.14**

* Aluminum pads have not been de-embedded.
** Limited by available source power.

V. CONCLUSION

A state-of-the-art W-band SPDT switch implemented using PIN diodes in a 90 nm SiGe BiCMOS technology was presented. A comparison of this switch to other state-of-the-art W-band SPDT switches is shown in Table I. In comparison, to [6]-[8], the present work did not de-embed the aluminum RF pads, which would result in an insertion loss reduction of approximately 0.17-0.34 dB. To our best knowledge, this is the lowest insertion loss and highest power handling W-band SPDT switch in any silicon-based technology reported to date.

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