Chapter 2

Nonlinear modeling of active microwave devices

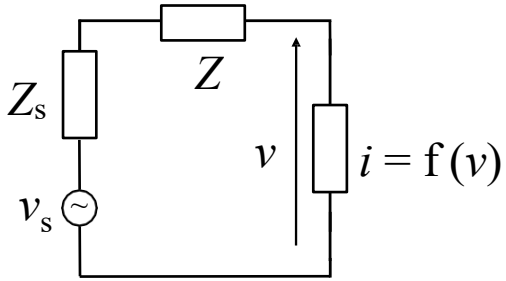
NONLINEAR COMPONENTS

Two-terminal and transfer components

In nonlinear CAD, two nonlinear concepts are used, namely:

two-terminal nonlinearities and **transfer** nonlinearities.

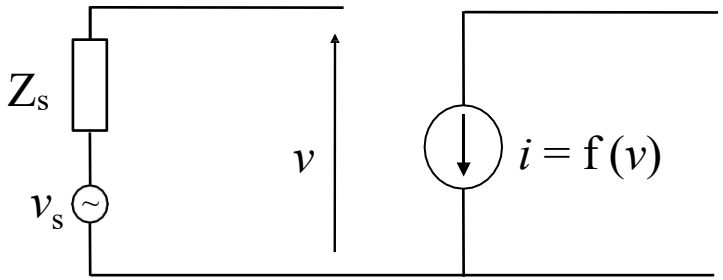
A **two-terminal** is a simple nonlinear component, usually **passive** (i.e., R, L, or C), which value is function of one independent variable, the voltage *v* across *its terminals* or the current *i* flowing from one of *its terminals* to the other one.



An example of **transfer** nonlinearity is the nonlinear controlled current source

$$I_{ds} = f(v_{gs}, v_{ds}) \quad \text{or} \quad I_c = f(I_b)$$

in the equivalent circuit of a **transistor**.



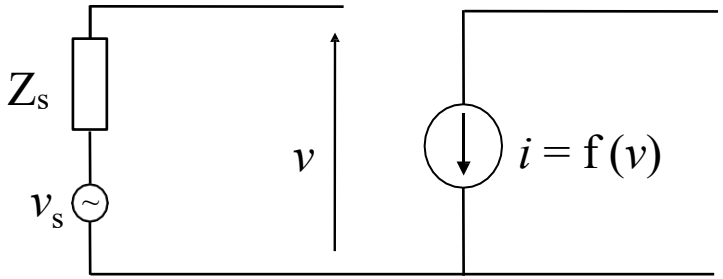
NONLINEAR COMPONENTS

Two-terminal and transfer components

In transfer nonlinearity, the control voltage or current is somewhere in the circuit *other than at the element's terminals*. Thus, it is possible for a circuit element to have more than one control variable (i.e., the current I_{ds} is function of both V_{gs} and V_{ds} in a FET).

Practical circuits and circuit elements often include both types of nonlinearities (e.g., the gate-source capacitance and the drain current of a FET).

The difference between the two types of nonlinearities can be illustrated by an example.



Let us assume the nonlinear two-terminal is a nonlinear resistor and the transfer nonlinearity is a nonlinear ideal transconductance amplifier. Both are excited by a voltage source having some internal impedance.

- The amplifier output current is a function of the excitation voltage and the nonlinear transfer function; it can be found by **simply substituting the voltage waveform** into the **transfer function**, regardless of the nature of the input or output circuits.
- In the two-terminal element, however, the excitation voltage generates current components in the resistance (**harmonics**). These components circulate in the rest of the circuit, generating voltages at those frequencies across the nonlinear resistance. These new voltage components will generate new current components, and the process continues until current and voltage components at all possible frequencies are generated.

$\Rightarrow$ The two-terminal nonlinearity is clearly more complicated analytically than the transfer nonlinearity.

That is ***why*** the transfer nonlinearities are more popular to nonlinear circuit designers.

NONLINEAR COMPONENTS

Quasi-static assumption

Inherent in the nonlinear time- or frequency-domain analyses of nonlinear circuits is the **quasi-static** assumption:

All parameters of nonlinear elements (transconductance, capacitance, etc.) change instantaneously with a change in one or more control voltages or currents.

Because they are based on a fundamental assumption of ***linearity***, impedance concepts and multi-port circuit theory cannot be used as the sole means of describing a nonlinear circuit.

NONLINEAR COMPONENTS

Quasi-static assumption

Accordingly, the most popular means for characterising diodes and transistors (*S*- *Y*- or *Z*-parameters) **cannot** be used to model nonlinear solid-state devices.

Instead, the most successful method of characterising such devices is to use **a lumped circuit model** that includes a **mix** of linear and nonlinear resistances, capacitances, inductors, and controlled sources.

- ***The nonlinear elements are assumed to be quasi-static to frequencies up to 100 GHz.***
- ***Under the quasi-static assumption, all nonlinear elements are assumed to change instantaneously with changes in their control voltages.***

NONLINEAR COMPONENTS

Quasi-static assumption

One advantage is that small-signal models can be converted easily to large-signal models.

- Small-signal devices are described by lumped-element models as an alternative to multi-port parameters.

The advantage of using such models is that they require less characterisation data than a large table of two-port parameters or a full electromagnetic characterisation.

Such models can be converted to large-signal models simply by including the voltage dependence of the circuit's elements or/and by making minor changes in the topologies of the models while linear-based elements can **share** the same circuit.

NONLINEAR COMPONENTS

Requirements for nonlinear device models

- Assure high accuracy. This situation is possible only with the use of complex circuit topologies, which requires large CPU time usage for their simulation.
- Use a simple but adequate model. A simpler topology/model would not assure high accuracy.

Concern for computational difficulty is crucial because many nonlinear analyses require a huge number of evaluations of the circuit equations (during optimization and/or statistical analysis).

Another requirement is that it must be possible to determine the model's parameters without undue difficulty.

NONLINEAR LUMPED COMPONENTS

Nonlinear device models consist usually of nonlinear passives and controlled sources. The circuit elements can be described by one of two kinds of characteristics:

- Large signal global characteristic, which describes the overall *I/V* or *Q/V* relationships and used for modelling large-signal circuits.
- Incremental small-signal characteristic, which describes the deviation of voltage and current or charge in the vicinity of a bias point, and used for modelling small-signal and quasi-linear circuits.

Note: As solid-state devices are not lumped circuits, the responses of such lumped equivalent circuit models should be then seen as an **approximation** of their real behaviour.

NONLINEAR LUMPED COMPONENTS

Two critical concepts in the modelling of nonlinear devices are **voltage and current control**, and **incremental quantities**.

Many elements are either current- or voltage-controlled, and the value of a voltage-controlled element is dependent upon a voltage that may be applied to its terminals or may be elsewhere in the circuit.

For example, we know from the technical literature of circuit theory that the small signal junction conductance of a nonlinear diode can be expressed as a nonlinear exponential function of voltage or as a linear function of current.

But, in the case of nonlinear elements, we should *precise* at this point what we mean exactly by *small signal resistance of nonlinear elements*.

Question:

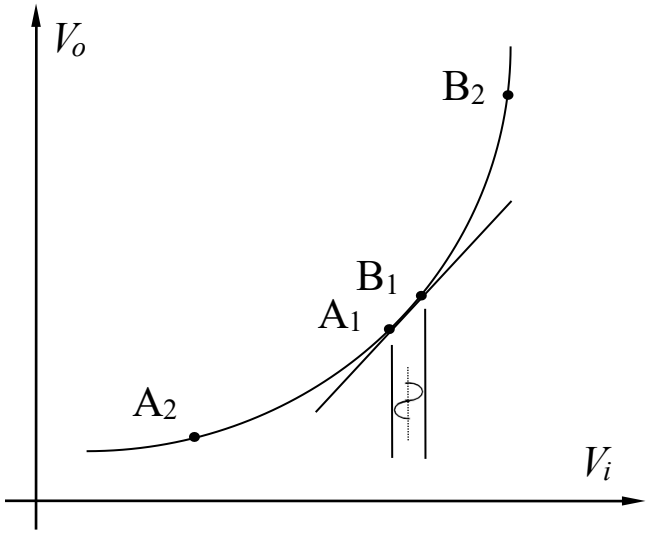
What is the difference between **small-signal resistance** and **nonlinear resistance**?

LINEARITY AND NONLINEARITY IN CIRCUIT THEORY

Recall from Chapter 1 :

If an input signal V_i imposes a small excursion around the DC point (Q point), the curve A_1B_1 is almost linear

$$V_o = G\,V_i$$



The input-output relationship for the nonlinear case will be

$$V_o = AV_i + B\,V_i^2 + C\,V_i^3 + \ldots$$

Each mth term " $(V_i)^m$ " generates the harmonic mf_i of the fundamental input frequency f_i.

SUBSTITUTION THEOREM

The I-V characteristic of a linear resistance is given by $V = RI$.

Now, suppose a current controlled nonlinear resistance r is used in an application where a small signal ac current is applied and a dc control current I_o exists.

The ac component of the resistance voltage should be given by

$$v(t) = r(I_o)\, i(t)$$

where $v(t)$ and $i(t)$ are the **small-signal** voltage and current, respectively.

It is clear that

$$r(I_o) = \left.\frac{dv}{di}\right|_{i=I_o}$$

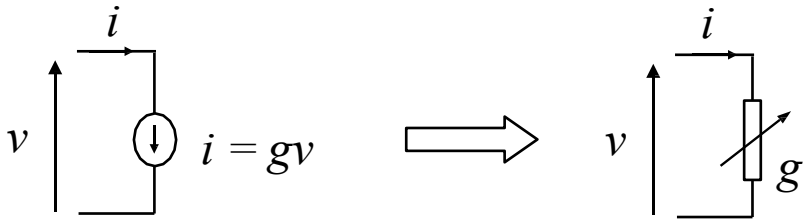
This is the *incremental resistance,* valid in **small-signal quasi-linear** analysis.

In the case of a voltage-controlled conductance, the small-signal current i can be expended in a Taylor series around the DC bias voltage V_0 as

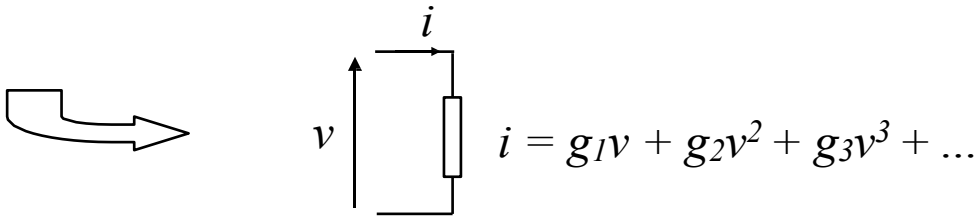
$$i(v) = f(V_o + v) - f(V_o) = v\left.\frac{df(v)}{dv}\right|_{v=V_o} + \frac{1}{2}v^2\left.\frac{d^2 f(v)}{dv^2}\right|_{v=V_o} + \frac{1}{6}v^3\left.\frac{d^3 f(v)}{dv^3}\right|_{v=V_o} + \ldots$$

SUBSTITUTION THEOREM APPLIED TO NONLINEAR COMPONENT MODELING

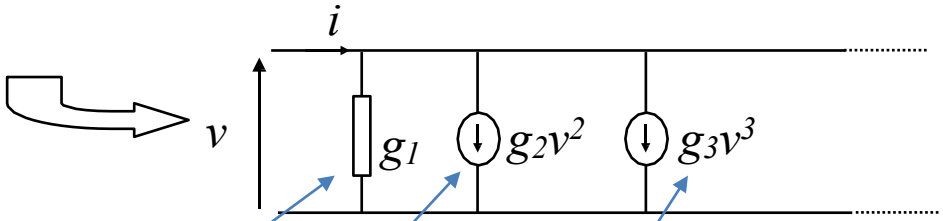
With the help of the substitution theorem, the nonlinear element can be modelled as



$$i(v) = g_1 v + g_2 v^2 + g_3 v^3 + \ldots$$

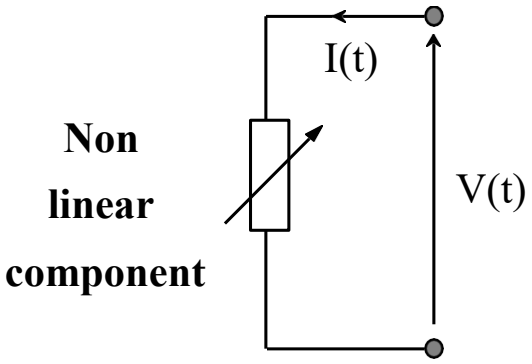


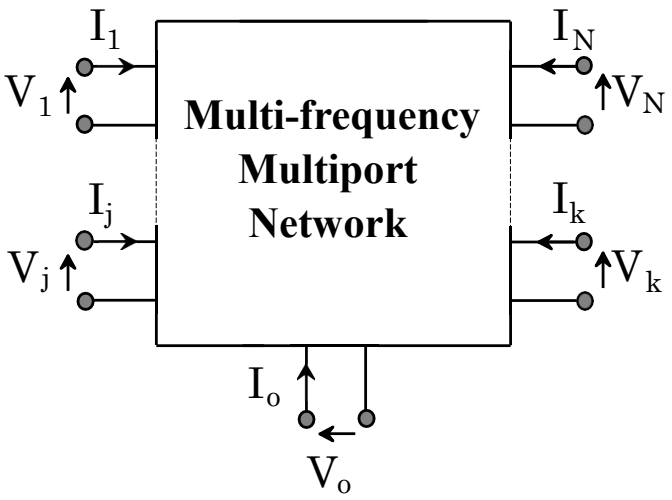
A nonlinear component can be modeled as a set of linear elements !!



$$i(v) = f(V_o + v) - f(V_o) = v\left.\frac{df(v)}{dv}\right|_{v=V_o} + \frac{1}{2}v^2\left.\frac{d^2 f(v)}{dv^2}\right|_{v=V_o} + \frac{1}{6}v^3\left.\frac{d^3 f(v)}{dv^3}\right|_{v=V_o} + \ldots$$

CHAPTER 1: MULTI-FREQUENCY NETWORK





NONLINEAR ACTIVE DEVICES

A nonlinear active device modelling can be based on physics equations or equivalent electrical circuit. We have retained this approach, which is more efficient for circuit theory purposes.

A large variety of diodes are available for various purposes: detection, amplification, mixing, oscillation, multiplication, etc.

Usually, we should distinguish between *Transit Time Devices* or *Transferred Electron Devices* like Gunn and IMPATT diodes where the **quasi-static assumption is not valid**, and those where the assumption applies like Schottky, varactor and Tunnel diodes.

NONLINEAR ACTIVE DEVICES

DIODES

Gunn Diodes

Gunn diodes are not usual diodes because there is **no junction**. The diode operation is based on the volume effect or **Gunn effect** (transfer of electrons when an electrical field is applied).

Several large-signal diode models have been proposed but the recurrent problem is to establish a general and efficient *I/V* relationship due to the fact there is many operating modes namely, the **transit-time mode,** the **delay-domain mode,** the **quenched-domain mode,** the **accumulation-layer mode** and the **stable domain mode**.

Moreover, the voltage variation has a field-dependent behaviour.

NONLINEAR ACTIVE DEVICES

Gunn Diodes

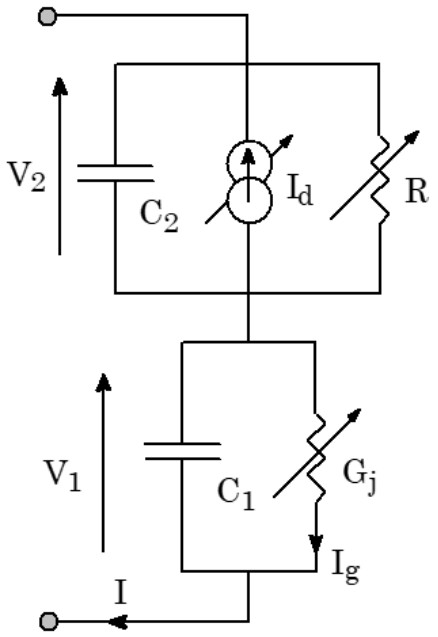
One of the most used large-signal Gunn diode models is the one proposed by Chua where the elements are defined as:

$$I_g = A\,q\,n_o\,f\left(\frac{V_1}{L}\right) = A\,q\,n_o\,f\,(E_o)$$

$$I_d = C_2\,n_o\left\{\int_{E_o}^{E_M}\left[\frac{f(E_o)-f(E)}{n_a-n_o}+\frac{f(E_o)-f(E)}{n_o-n_d}\right]dE\right\}-I$$

$$C_1 = \frac{\varepsilon A}{L}$$

$$C_2 = \frac{\varepsilon A}{W}$$



IMPATT Diodes

IMPact ionization Avalanche Transit Time diodes (IMPATT, also known as Read diodes) are P^+-N-N^+ diodes with a large breakdown region. These diodes are used in parametric amplification, frequency multiplication and as millimetre power sources for radars (high power impulsion).

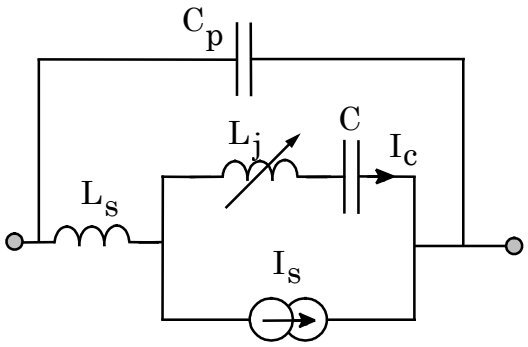
They allow high-order frequency multiplication and up-conversion with high conversion rates. However, they are unstable (oscillations) and exhibit a relatively high noise figure.

Their equivalent circuit presents a current source

$$I_s(t) = \frac{1}{\tau_d}\int_{t-\tau_d}^{t} I_c(t')\,dt' - I_c(t)$$

and a nonlinear inductance L_j which is function of current I_c, bias current I_{dc}, and breakdown inductance L_a

$$L_j(I_c) = \left(\frac{I_{dc}}{I_c}\right) L_a$$



However, Gunn and IMPATT Diodes are **rarely** present in a CAD process while they are very efficient and cost-effective!!

Why?

- Quasi-static assumption is **not** valid

  ➞ How to use a model in which linear and nonlinear elements **cannot** cohabit?

- Their voltage is dependent of the electrical field.

  ➞ How to set their I-V relationship, required to set the linear system of equations?

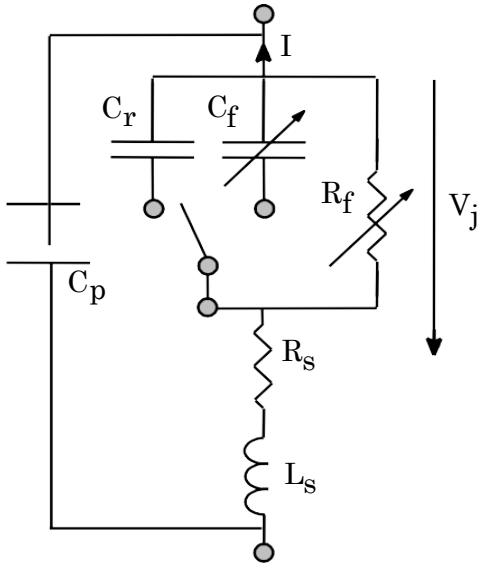
- Their voltage-current relationship is an **integro-differential equation** function of input signal amplitude and frequency.

  ➞ How to establish the **linear** system of I-V equations simulators need to solve?

SRD Diodes

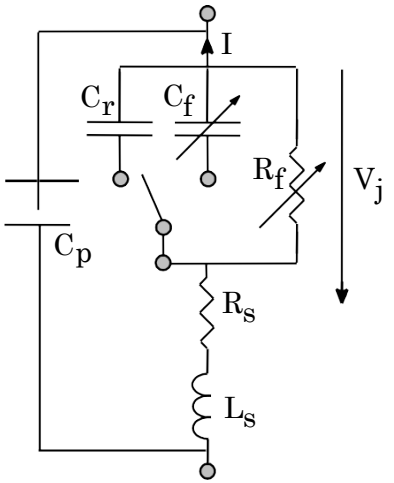
SRD diodes ("Step Recovery Diodes") are used for high-order frequency multiplication or generation of high frequency signals from low frequency harmonic oscillators.

For illustration, harmonic generators with fundamental frequency of 10 MHz have generated output frequencies around 100 GHz.

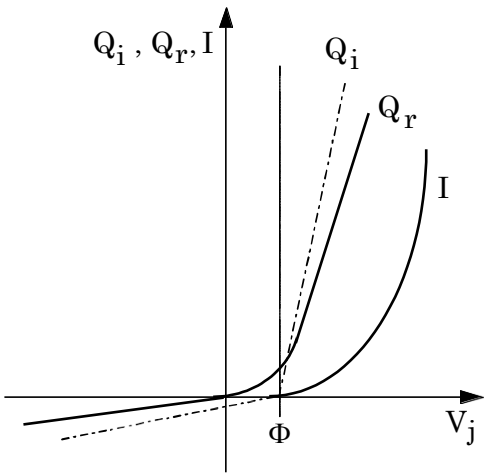


SRD Diodes

However, the real diode exhibits a transit time, a series resistance and parasitic elements C_p and L_s. Relationship between the charge Q and the junction voltage V_j can be established in function of barrier voltage Φ, forward capacitance C_f, and inverse capacitance C_r:



$$Q = \begin{cases} C_r V_j & V_j \le 0 \\ \dfrac{C_f - C_r}{2\Phi}\left(V_j + \dfrac{C_r \Phi}{C_f - C_r}\right)^2 - \dfrac{C_r^2}{2\left(C_f - C_r\right)}\Phi & 0 < V_j < \Phi \\ C_f V_j - \dfrac{C_f - C_r}{2}\Phi & \Phi \le V_j \end{cases}$$



(Q_i: ideal curve; Q_r : real curve)

PIN Diodes

PIN diodes are used as power attenuators and limitors. First, the diodes exhibit a higher breakdown voltage. Second, their impedance presents the particularity to switch from a very low value in direct bias to a very high value in inverse.

Such aspect is very important in microwaves because the diode is working as a reflector (a reflector is able to handle high powers, as it does not have to absorb them).

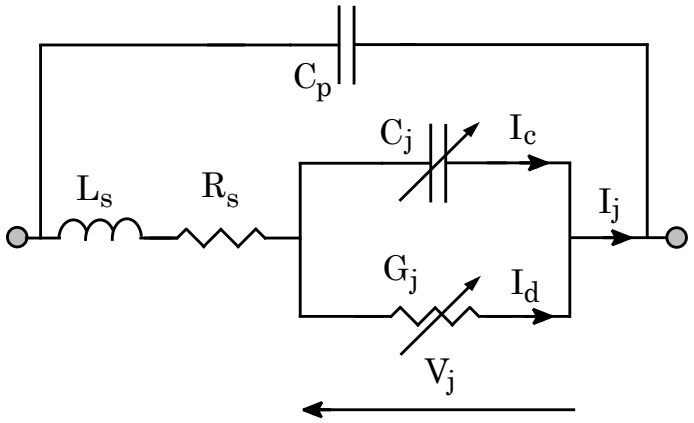
Moreover, in inverse polarisation, as the junctions P-I and I-N are biased in inverse, the intrinsic region is fully depleted and then acts as a perfect isolation. So, when the diode reaches the breakdown region, it can generate a high-order frequency multiplication.

Schottky Diodes

Schottky diodes are widely used in detection, mixing and frequency multiplication. They consist of a metal contact deposited on a semiconductor; such contacts do not have the recombination time limitations of PN junctions (low junction capacitance). Moreover, they exhibit a low noise figure and works usually at zero bias.

If the early diodes had the default to be not reliable, it is not the case today with the new technologies. Schottky diodes are electrically equivalent to a junction capacitance C_j in parallel with a junction conductance G_j. When they are exited by a large signal, G_j and C_j act as nonlinear elements function of the voltage V_j.

If the diode is forward-biased, the nonlinear effect of the conductance $G_j(V_j)$ is predominant. In inverse, the nonlinear effect is mainly due to the capacitance $C_j(V_j)$.



Schottky Diodes

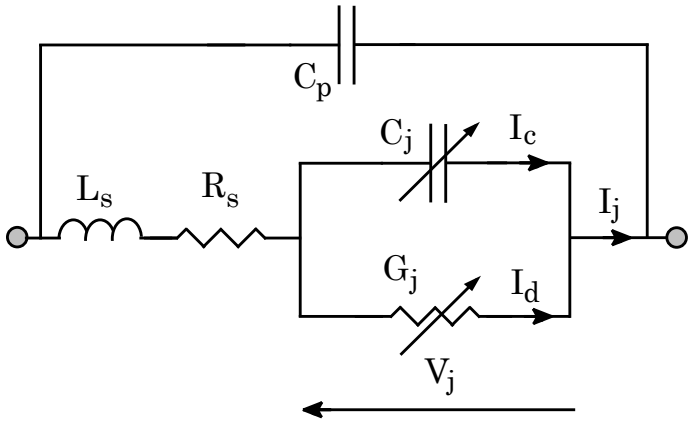
The total junction current I_j is the sum of the current I_c due to the capacitance C_j and the current I_d due to the conductance G_j, i.e.

$$I_d(V_j) = I_s\left(e^{\frac{q}{\eta kT}V_j} - 1\right)$$

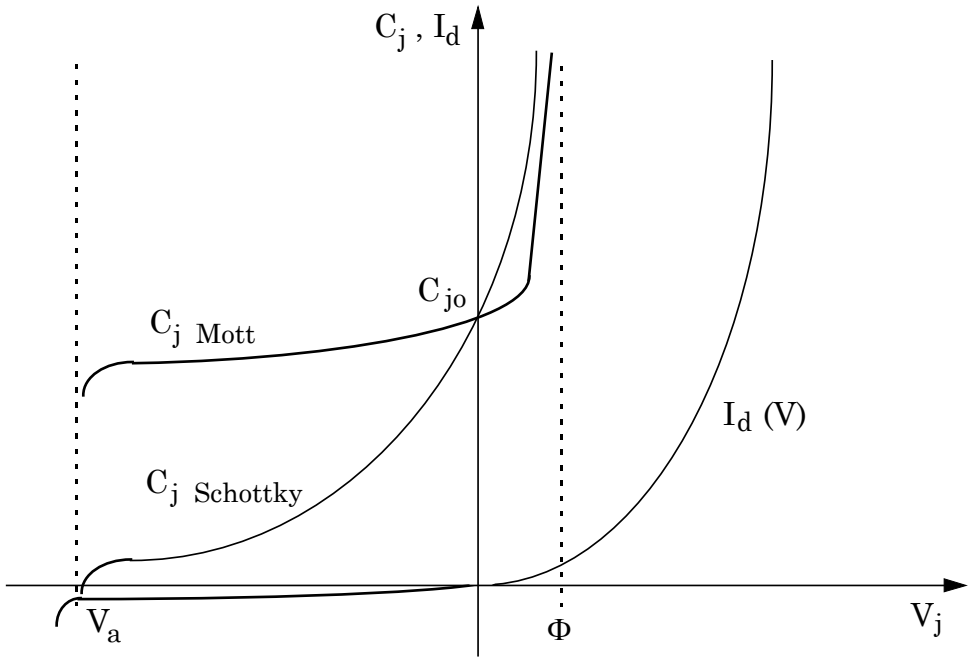
$$I_c(V_j) = C_j(V_j)\frac{dV_j(t)}{dt} + V_j\frac{dC_j(V_j)}{dV_j}\frac{dV_j}{dt}$$

$\gamma = 2$ for uniform doping. For non-uniform doping, the exponent γ value changes.

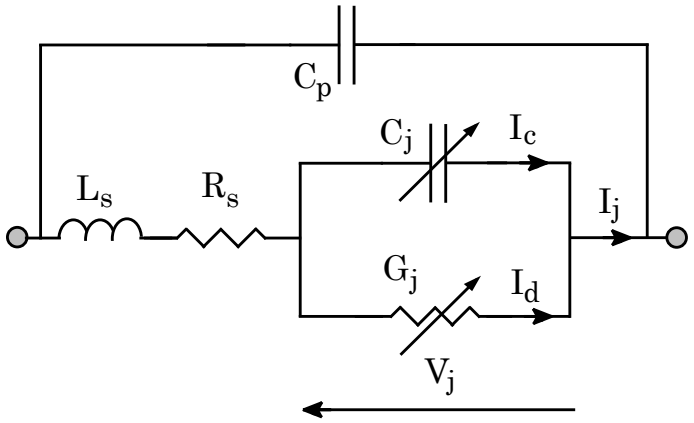
$$C_j(V_j) = C_{jo}\left\{1 - \frac{V_j(t)}{\Phi}\right\}^{-\gamma}$$



Schottky Diodes vs. Mott Diodes



$$C_j(V_j) = C_{jo}\left\{1 - \frac{V_j(t)}{\Phi}\right\}^{-\gamma}$$



Varactor Diodes

Varactor diodes use exclusively their C-V characteristic (inverse bias).

We must distinguish between PN varactors and Schottky varactor diodes:

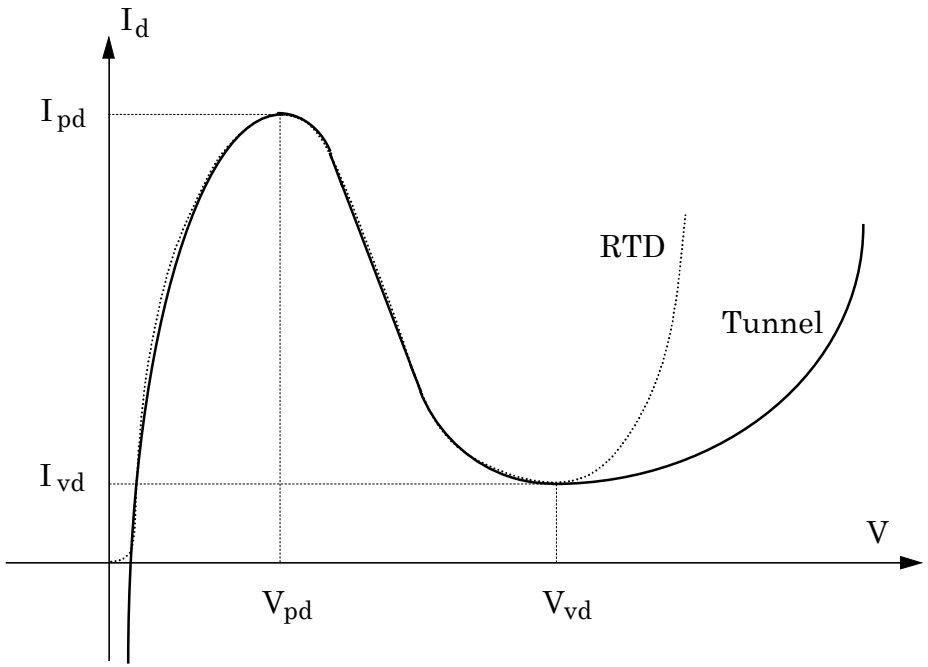
- The PN varactor has a capacitance-voltage characteristic similar to PN rectifier diodes and then has a higher capacitance value (better efficiency in frequency multiplication).

- The Schottky varactor diode has an equivalent electrical circuit similar to the one of the Schottky diode. As its capacitance-voltage characteristic nonlinearity is more accentuated, it is used mainly in frequency multiplication and as voltage controlled tuning element.

Tunnel Diodes

Esaki or tunnel diode I-V characteristic has the particularity to exhibit negative resistance, which is useful for oscillation. However, due to its poor performance, the tunnel effect has been neglected in oscillation until its use in millimetre range was underlined by the **RTD** ("Resonant Tunnelling Diodes") devices, which have emerged in the mm range because of their lower capacitance value and control of the peak-valley current-voltage values.

Moreover, they are mainly used for odd-order frequency multiplication (the I-V characteristic is symmetric). They are also used for detection/mixing and can operate without power absorption (the negative resistance compensates the real positive part of the diode impedance and then let the component purely reactive).



TRANSISTORS

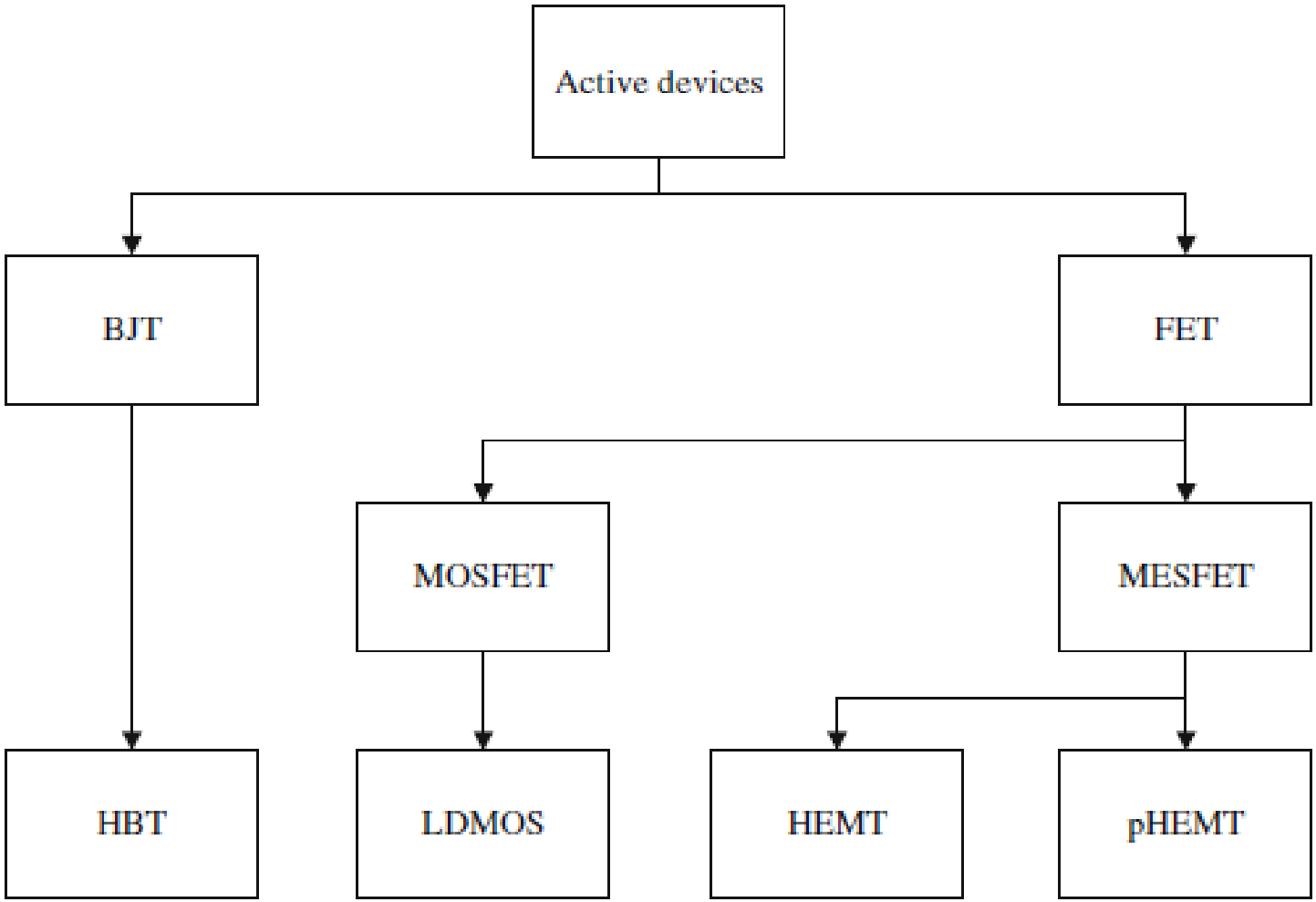
Hybrid or monolithic transistor circuits and systems are widely used for fixed and mobile communications. Thus, a circuit designer should have access to a large range of reliable models to use in any CAD process.

To be reliable and efficient, a model has to meet two opposite goals: speed and accuracy.

A complete transistor model is very precise but very slow, as it can **include more than 80 parameters** and use complex equations to fit the measured data over a large range of frequency and Q points.

On the other side, a simpler model can be faster, but it will present lower accuracy and performance. The designer has then to deal between these two extreme cases.

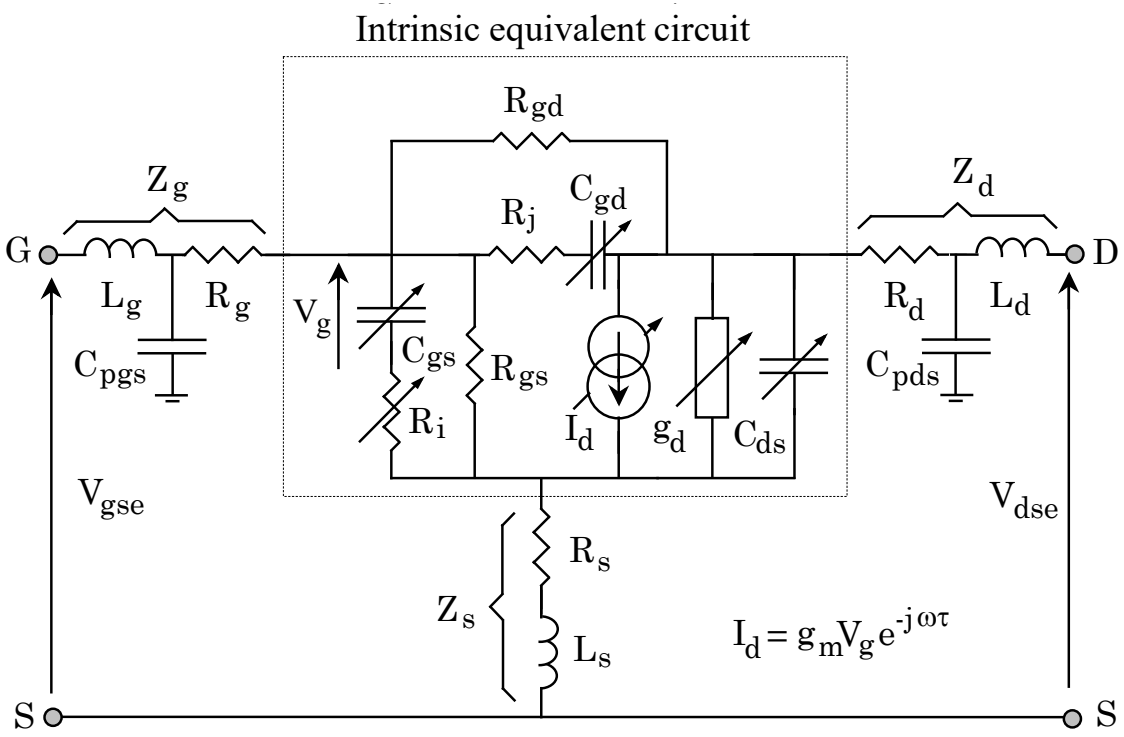
TRANSISTORS



MESFETs

MESFET ("Metal Semiconductor Field Effect Transistor") is one of the most widely used transistors in the upper part of the centimeter range and the lower part of the millimeter range.

The drain current source I_d is the most predominant nonlinear element in the circuit and then the most complex one to model.



The following list is therefore given just as illustration and is, obviously, not exhaustive:

Shockley (1952): $I_d = \beta (V_{gs} - V_{po})^n$

Shichman-Hodges (1968):

Ohmic region: $I_d = \beta V_{ds} \left(2\left(V_{gs} - V_{po}\right) - V_{ds}\right)\left(1 + \lambda V_{ds}\right)$

Saturation region: $I_d = \beta \left(V_{gs} - V_{po}\right)\left(1 + \lambda V_{ds}\right)$

Taki (1978): $I_d = I_{dss}\left(1 - \dfrac{V_{gs}}{V_p - \sigma V_{ds}}\right)^2 \tanh\left(\alpha \left| \dfrac{V_{ds}}{V_p - \sigma V_{ds} - V_{gs}} \right|\right)$

Curtice (1980): $I_d = \beta \left(V_{gs} - V_{po}\right)^2 \left(1 + \lambda V_{ds}\right) \tanh\left(\alpha V_{ds}\right)$

Tajima 1 (1981): $I_d = I_{d1}.I_{d2}$

$$I_{d1} = 1 + \frac{V_{gs} - V_{bi}}{V_{po} + pV_{ds} + V_{bi}} - \frac{1}{m} + \frac{1}{m}\exp\left\{-m\left(\frac{V_{gs} - V_{bi}}{V_{po} + pV_{ds} + V_{bi}}\right)\right\}$$

$$I_{d2} = \frac{I_{dsp} m}{m - \left[1 - \exp\left(-m\right)\right]}\left\{1 - \exp\left[-\frac{V_{ds}}{V_{dss}} - a\left(\frac{V_{ds}}{V_{dss}}\right)^2 - b\left(\frac{V_{ds}}{V_{dss}}\right)^3\right]\right\}$$

Materka 1 (1983):

$$I_d = I_{dss}\left(1-\frac{V_{gs}}{V_{po}+\gamma V_{ds}}\right)^2 \tanh\left(\frac{\alpha V_{ds}}{V_{gs}-V_p}\right)$$

Tajima 2 (1984):

$$I_d = I_{dss}.F_g F_d + G_{d0}.V_{ds}$$

$$F_g = \frac{1}{k}\left[1+\frac{V_{gs}}{V_p}-\frac{1}{m}\left\{1-\exp\left(-m\left(1+\frac{V_{gs}}{V_p}\right)\right)\right\}\right]$$

$$F_d = 1-\exp\left(-V_{dsn}-aV_{dsn}^2-bV_{dsn}^3\right)$$

$$V_{dsn} = \frac{V_{ds}}{V_{dsp}\left(1+W\frac{V_{gs}}{V_p}\right)} \qquad G_{d0} = g_d\big|_{v_{ds}=0}$$

Materka 2 (1985):

$$I_d = I_{dss}\left(1-\frac{V_{gs}}{V_{po}+\gamma V_{ds}}\right)^2\left(1+\frac{\eta V_{ds}}{I_{dss}}\right)\tanh\left(\frac{\alpha V_{ds}}{I_{dss}\left(1-\lambda V_{gs}\right)}\right)$$

Curtice-Ettenberg (1985):

$$I_d = \left(a_o+a_1V+a_2V^2+a_3V^3\right)\tanh\left(\alpha V_{ds}\right)$$

$$V = V_{gs}\left(1+\beta\left(V_{dso}-V_{ds}\right)\right)$$

Statz-Pucel "Raytheon model " (1987):

$$I_d = \begin{cases} \dfrac{\beta\left(V_{gs}-V_{po}\right)^2}{1+b\left(V_{gs}-V_{po}\right)}\left(1+\lambda V_{ds}\right)\left[1-\left(1-\alpha\dfrac{V_{ds}}{3}\right)^3\right] & 0 < V_{ds} < 3/a \\ \dfrac{\beta\left(V_{gs}-V_{po}\right)^2}{1+b\left(V_{gs}-V_{po}\right)}\left(1+\lambda V_{ds}\right). & V_{ds} \geq 3/a \end{cases}$$

Hwang (1987):

$$I_d = \begin{cases} I_d = I_{dss}\left(1-\dfrac{V_{gs}}{V_p}\right)^2 \tanh\left(\dfrac{\alpha V_{ds}}{V_{gs}-V_p}\right) & V_{ds} < V_{sat} \\ I_d = I_{dss}\left(1-\dfrac{V_{gs}}{V_p}\right)^2 \tanh\left(\dfrac{\alpha V_{ds}}{V_{gs}-V_p}\right) - \dfrac{g_o V_{ds}}{\left(A-V_{gs}\right)^q} & V_{ds} \geq V_{sat} \end{cases}$$

Vincent (1987):

$$I_d = I_{dss}\left(1-\frac{V_{gs}}{V_p}\right)^2 \tanh\left(\frac{\alpha V_{ds}}{V_{gs}-V_p}\right) + F\left(V_{gs},V_{ds}\right)$$

$$F(V_{gs},V_{ds}) = \begin{cases} 0 & V_{ds} < V_{sat} \\ -V_{ds}.g_o\left[V_s-V_{gs}\right]^{-q} + I_{sr}\, exp\left\{\beta\left[V_{ds}-V_{gs}\right]\right\} & V_{ds} \geq V_{sat} \end{cases}$$

Plessey (1990):

$$I_d = I_{dss} \cdot \frac{\left(V_{gs} - V_{po}\right)^2}{1 + b\left(V_{gs} - V_p\right)}\left(1 + \lambda V_{ds}\right)\tanh\left(\alpha V_{ds}\right)$$

$$+\left(1 + \frac{V_{ds}}{V_p\left(1 - \beta V_{ds}\right)}\right) g_{dp} . V_{ds} . \tanh\left(\alpha V_{ds}\right)$$

Hu (1990):

$$I_d = \frac{\beta\left(V_{gs} - V_{po}\right)^2}{1 + b\left(V_{gs} - V_{po}\right)}\left(1 + \mu V_{gs} \exp\left\{\sigma V_{gs} V_{ds}\right\} + \lambda V_{gs} V_{ds}\right)\tanh\left(\alpha V_{ds}\right)$$

TOM "TriQuint's Own Model" (1990):

$$I_d = \begin{cases} \dfrac{\beta\left(V_{gs} - V_p\right)^Q}{1 + \delta\,\beta V_{ds}\left(V_{gs} - V_p\right)^Q}\left[1 - \left(1 - \alpha\dfrac{V_{ds}}{3}\right)^3\right] & 0 < V_{ds} < 3/a \\ \dfrac{\beta\left(V_{gs} - V_p\right)^Q}{1 + \delta\,\beta V_{ds}\left(V_{gs} - V_p\right)^Q} & V_{ds} \geq 3/a \end{cases}$$

Brazil (1991):

$$I_d = I_{dss}\left[1 + \tanh\left\{1 - \exp\left(\mu - \frac{\alpha\left(V_{gs} - V_{bi}\right)}{V_{ds}^2 + V_{bi}}\right)\right\}\right]\tanh\left[\sigma . V_{ds}\right]$$

Angelov (1992):

$$I_d = I_p\left(1 + \tanh\left[\sum \alpha_i \left(V_{gs} - V_{po} - \gamma V_{ds}\right)^i\right]\right)\left[1 + \lambda V_{ds}\right]\tanh\left[\sigma . V_{ds}\right]$$

Rodriguez (1992):

$$I_d = \beta \left(V_{gs} - V_{po} + \gamma V_{ds}\right)^2 \left(1 + \lambda V_{ds}\right) \tanh\left(\alpha V_{ds}\right)$$

Teyssier (1994):

$$I_d = I_{dss}.a \left\{1 + \beta \left(V_{ds} - V_{dm}\right)\left(1 + \tanh\left\{\alpha \left(V_{gs} - V_{gm}\right)\right\}\right)\right\}$$

Fernández (1996):

$$I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_{po} + \gamma V_{ds}}\right)^{\left(\mu + \beta V_{gs}\right)} . \left(1 + \eta V_{ds}\right) \tanh\left(\frac{\alpha V_{ds}}{I_{dss}}\right)$$

Ooi (2002):

$$I_d = b_1 V_{ds} V_{eff}^3 + \frac{b_4 V_{ds}\left(b_2 + b_3 V_{ds}\right)V_{eff}^2}{\sqrt{\left(1 + g V_{gst}\right)^2 + V_{ds}^2}\left(b_2 + b_3 V_{ds}\right)^2} + \frac{b_5 V_{ds}\left(b_2 + b_3 V_{ds}\right)V_{eff}}{\sqrt{\left(1 + g V_{gst}\right)^2 + V_{ds}^2}\left(b_2 + b_3 V_{ds}\right)^2}$$

$$V_{gst} = V_{gs} - V_{bi} + \gamma V_{ds} \qquad V_{eff3} = 0.5\left(V_{gst}\left(1 + c\right) + \sqrt{V_{gst}^2 + V_M^2}\left(1 - c\right)\right)$$

$$V_{eff} = V_M \left(1 + M V_{ds}\right) \ln\left(1 + \exp\left(\frac{V_{eff3}}{V_M\left(1 + M V_{ds}\right)}\right)\right)$$

Angelov (2005):

$$I_d = 0.5\left(I_{dsp} - I_{dsn}\right) \qquad \psi_n = \sum_{i=1}^{3} P_{im}\left(V_{gd} - V_{pk}\right)^i \qquad \psi_p = \sum_{i=1}^{3} P_{im}\left(V_{gs} - V_{pk}\right)^i$$

$$I_{dsp} = I_{pk0}\left[1 + \left[\tanh\left(\psi_p\right)\right] * \left[1 + \tanh\left(\alpha_p V_{ds}\right)\right] * \left[1 + \lambda_p V_{ds} + L_{SB0} \exp\left(V_{dg} - V_{tr}\right)\right]\right]$$

$$I_{dsn} = I_{pk0}\left[1 + \left[\tanh\left(\psi_n\right)\right] * \left[1 - \tanh\left(\alpha_n V_{ds}\right)\right] * \left[1 + \lambda_n V_{ds}\right]\right]$$

Question:

From this huge number of models, how a designer can choose the correct model?

The choice is based not only on the desired circuit performance, but also on the model complexity, the transistor size, the Q point variations, the temperature behaviour, the gain, the input/output power range ….

For example, Materka's model is very efficient in the linear region of the I-V curves. On the other hand, Curtice and Statz models are preferred for small transistors and Rodriguez's model presents many advantages in the knee region.

Some other researchers have concentrated their efforts to generate more general expressions in the form of analytical or semi analytical relations like Madjar (1988):

$$I_d = \alpha\left(1+mV_{ds}\right)\tanh\left(\frac{V_{ds}}{V_a\left(V_{gs}\right)}\right)+G_1\left(V_{gs}\right)\left(\frac{dV_{gs}\left(t-\tau\right)}{dt}\right)+G_2\left(V_{ds}\right)\left(\frac{dV_{ds}}{dt}\right)$$

These relations are more accurate and general than the empirical ones, but they use physical transistor parameters, which are not available to all designers. In practice, the most used models in circuit simulators like Cadence®, Spice®, Libra®, Compact®, Touchstone®, Serenade®, ADS® ... are Materka, TOM, Angelov, Statz-Pucel, and Curtice models.

Similarly, several nonlinear equations have been published by different authors to model the C_{gs} and C_{gd} behaviours. For example, Statz and Pucel (1987) proposed the following relations:

$$C_{gs} = \frac{C_{gso}\left(1+K_1\right)\left(1+K_2\right)}{4}\left(1-\frac{V_1}{V_{bi}}\right)^{-\frac{1}{2}} + \frac{C_{gdo}\left(1-K_2\right)}{2}$$

$$V_e = \frac{1}{2}\left(V_{gs}+V_{gd}+\sqrt{\left(V_{gs}-V_{gd}\right)^2+\delta^2}\right)$$

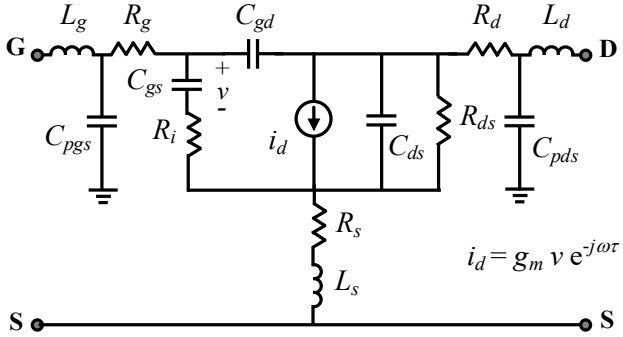
$$C_{gd} = \frac{C_{gdo}\left(1+K_1\right)\left(1-K_2\right)}{4}\left(1-\frac{V_1}{V_{bi}}\right)^{-\frac{1}{2}} + \frac{C_{gso}\left(1+K_2\right)}{2}$$

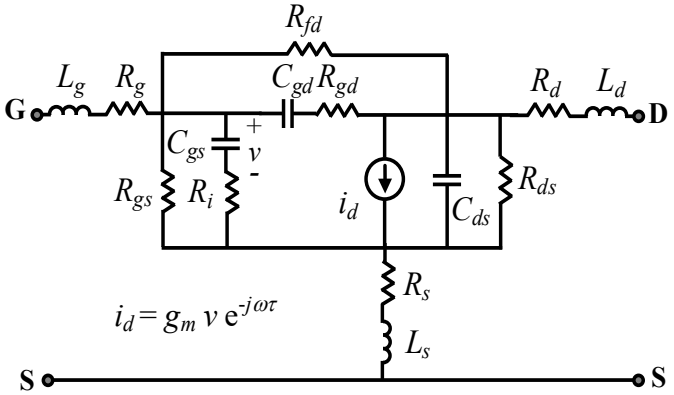
$$V_n = \frac{1}{2}\left(V_e+V_t+\sqrt{\left(V_e-V_t\right)^2+\delta^2}\right)$$

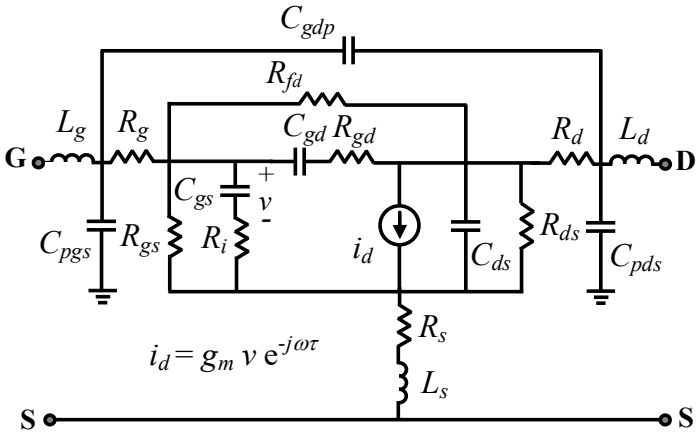
$$K_1 = \frac{V_e-V_t}{\sqrt{\left(V_e-V_t\right)^2+\delta^2}}$$

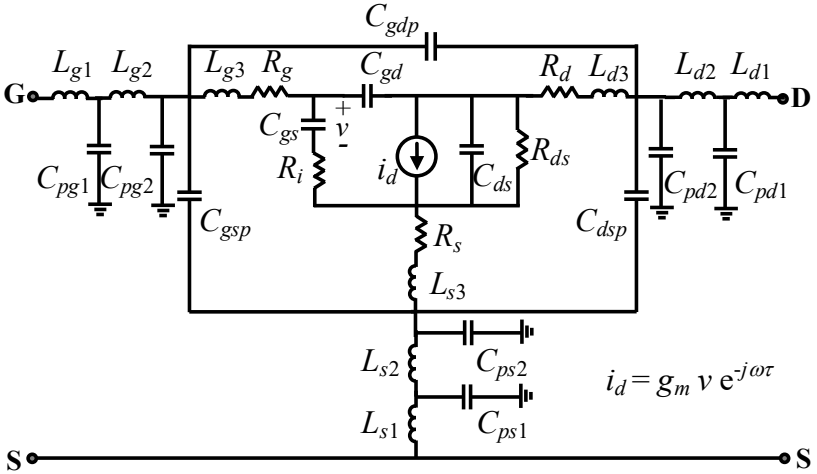
$$K_2 = \frac{V_{gs}-V_{gd}}{\sqrt{\left(V_{gs}-V_{gd}\right)^2+\left(\frac{1}{\alpha}\right)^2}}$$

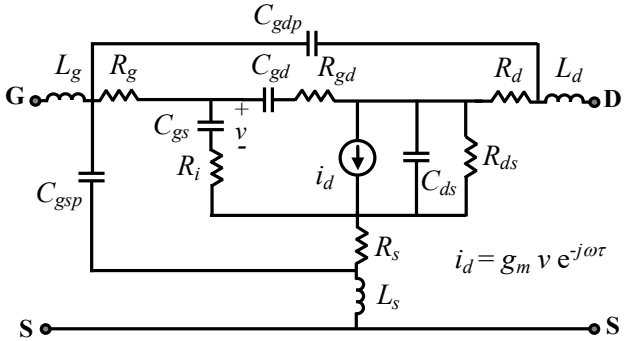
WHAT ABOUT THE EQUIVALENT CIRCUIT?





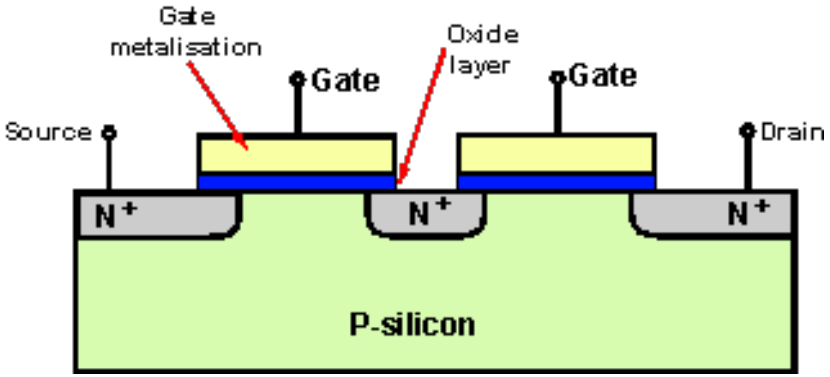


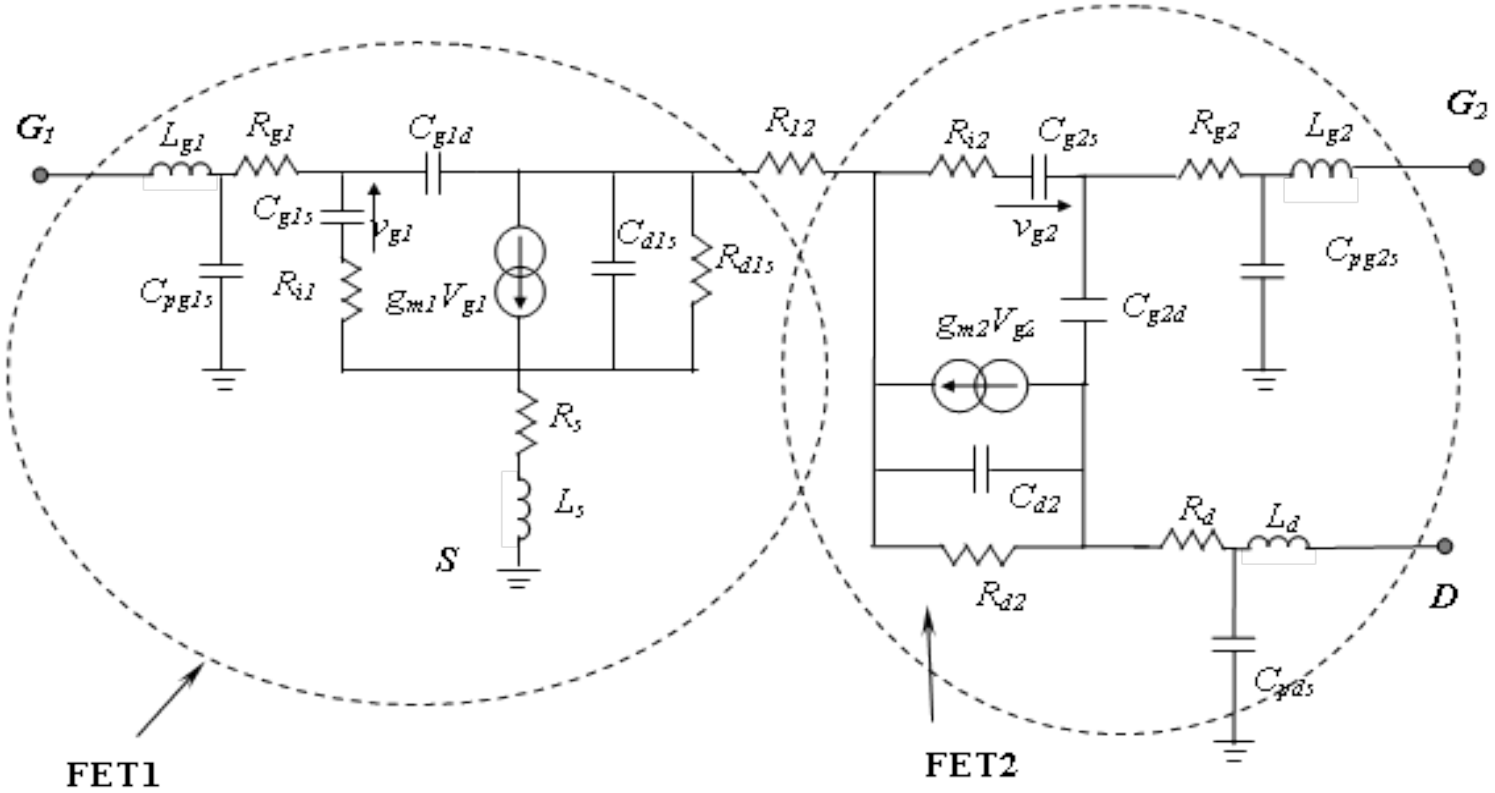




DUAL-GATE MESFETS

Introduced by Turner, dual-gate FET transistors have two parallel gates that are electrically independent. For common use, the configuration is common-source with the excitation signal applied to the first gate while the second one is grounded. If the second gate is positively biased, the gain will significantly increase *without* changing the *gain*Bandwidth* product; the circuit is equivalent to a cascode circuit common source + common gate.




G1
Lg1
Rg1
Cg1d
Cg1s
vg1
Cpg1s
Ri1
gm1Vg1
Cd1s
Rd1s
Rs
Ls
S
R12
Ri2
Cg2s
vg2
Rg2
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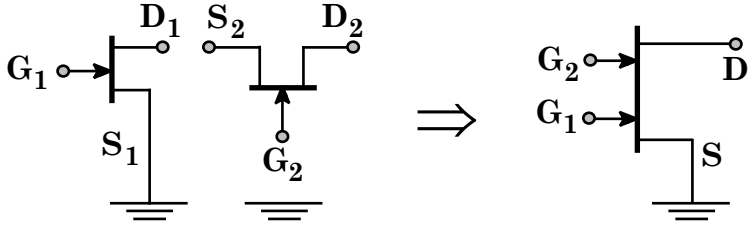
Cg2d
Cd2
Rd2
Rd
Ld
D
Cpd2s
FET1
FET2


D1
S2
D2
G1
S1
G2
G2
G1
D
S

GaAs MESFET

Advantages	Disadvantages
• Mature technology • Optical gates (usually) means low cost • Great microwave substrate (ε_r of 12.9, low loss tangent, high bulk resistivity) • Six inch wafers available • Photonic properties • 16-20 volt breakdown possible • Relatively cheap to produce (but always more than silicon) • Channel temperatures up to 150C possible	• Limited to Ku-band or lower • Noise figure and power performance not as good as GaAs PHEMT • Positive and negative voltage typically needed (V_{GS} and V_{DS}).

HEMTS

The High Electron Mobility Transistor (HEMT) is a transistor with smaller noise figure and higher cut-off frequency than MESFET. Moreover, it exhibits a better mobility, which implies higher transconductance and less effect of parasitic capacitances. The drain current modeling has also been the subject of many papers such as:

Mahon "Core model" (1992):

$$I_d = \begin{cases} 0 & V_{ds} < 0 \\ \left(1 - \left(1 - \dfrac{V_{ds}}{V_{dss}}\right)^2\right).I_{dss} & 0 \le V_{ds} \le V_{dss} \\ I_{dss} & V_{dss} < V_{ds} \end{cases}$$

Chen (1995):

$$I_d = I_{dss} \tanh\left[\left(10^{\sum_{k=0}^{4} a_k V_{gs}^k} - 1\right)V_{ds} - \left(10^{\sum_{k=0}^{4} b_k V_{gs}^k} - 1\right)V_{ds}^2 \left(10^{\sum_{k=0}^{4} c_k V_{gs}^k} - 1\right)V_{ds}^3\right]$$

HEMTS

Shirakawa (1996):

$$I_d = V_o e^{V_g}\left(\delta\left(1+\alpha\tan^{-1}\beta\left(V_{gs}-V_{go}\right)-V_{g1}\right)V_{ds}+\tanh\left(\lambda V_{ds}\right)\right)$$

Tanimoto (1996):

$$I_d = \left(\frac{a_o e^{a_1 V_{gs}}}{1+a_o a_2 e^{a_1 V_{gs}}}\right)+\left(\beta\left[1+\lambda V_{ds}\right]\tanh\left[\alpha V_{ds}\right]\right)$$

$$\beta = \frac{\beta_1 V_{gs}^2}{1+\beta_2 V_{gs}+\beta_3 V_{gs}^2+\beta_4 V_{gs}^3+\beta_5 V_{gs}^4} \qquad \alpha = \alpha_o + \alpha_1 exp\left(-\left(\frac{V_{gs}-\alpha_2}{\alpha_3}\right)^2\right)$$

Other variants of these transistors are MODFET ("MOdulation-Doped Field Effect Transistor"), SDHT ("Selectively Doped Heterostructure Transistor"), TEGFET ("Two-dimensional Electron Gas FET"), PHFET ("Pseudomorphic Heterostructure FET") or non-doped transistors like SISFET, MISFET, HIGFET, ...

Moreover, the same remarks for MESFET capacitances can apply to HEMT capacitances.

pHEMT TRANSISTORS

- Molecular Beam Epitaxial Growth for high electron mobility layers in AlGaAs and InP
- Low knee voltage (600 mV) and high breakdown voltage giving high efficiency
- High transconductance close to pinch-off yielding excellent gains in Class B and Class F
- Both Depletion Mode (normally "on") / Enhancement Mode (normally "off") available
- Excellent Reliability -- MTTF > 10^7 hours at 150^{o}C

GaAs PHEMT

Advantages	Disadvantages
• Useful through Q-band, especially if thinned to 2 mils and individual source vias are used • Excellent power and efficiency (greater than 60% PAE) • Breakdown 12 volts at best, typical operate at 5-6 volts • Channel temperatures up to 150C possible.	• E-beam gates (increases cost) • Positive and negative voltage typically needed (V_{GS} and V_{DS})

GaAs MHEMT

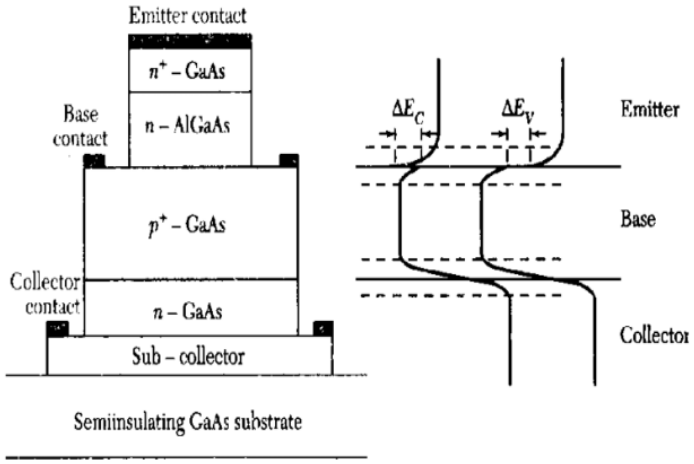
Advantages	Disadvantages
• Extremely low noise figure • Incredibly high f_{max} (more than 100 GHz) • Extremely low on-resistance, makes great switches, but not as good as PIN diodes. • Channel temperatures up to 150C possible.	• Breakdown voltage much lower than pHEMT • Low operating voltage (1 to 2 volts) • Positive and negative voltage typically needed (V_{GS} and V_{DS})

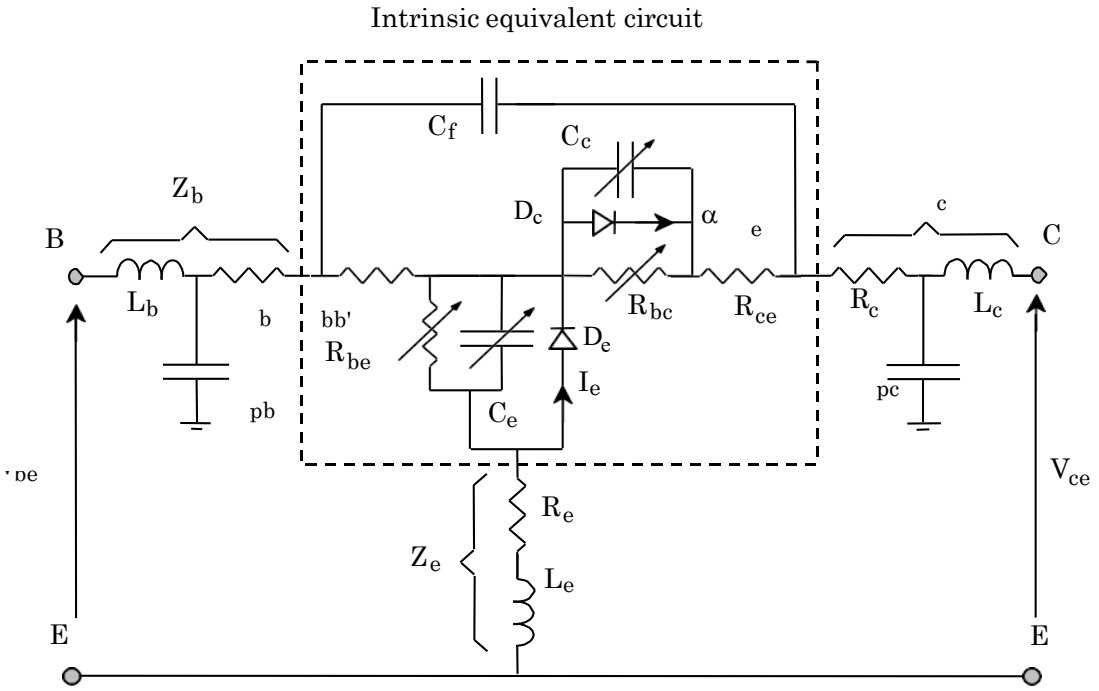
INDIUM PHOSPHIDE (InP) HEMT

Advantages	Disadvantages
• Extremely low noise figure • Useful through W-band and beyond	• More expensive than GaAs due to starting material costs, small size of wafers. • Extremely fragile. • Low breakdown voltage (power is low)

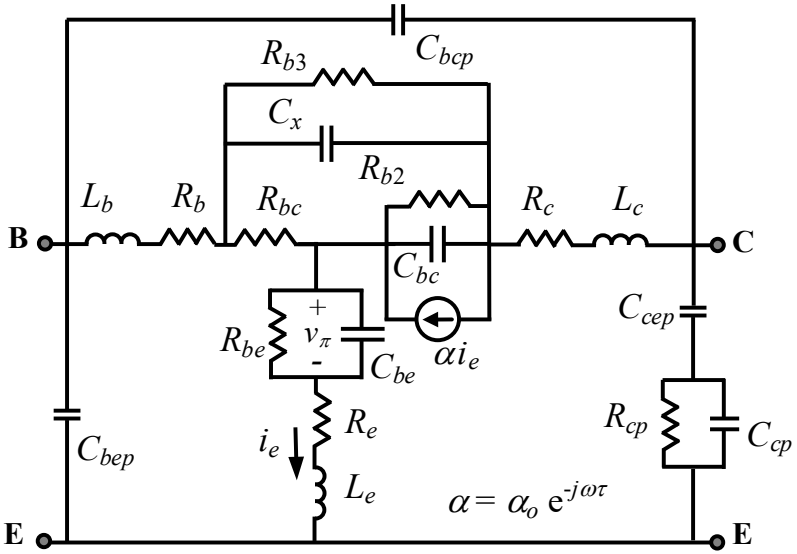
HBT TRANSISTORS

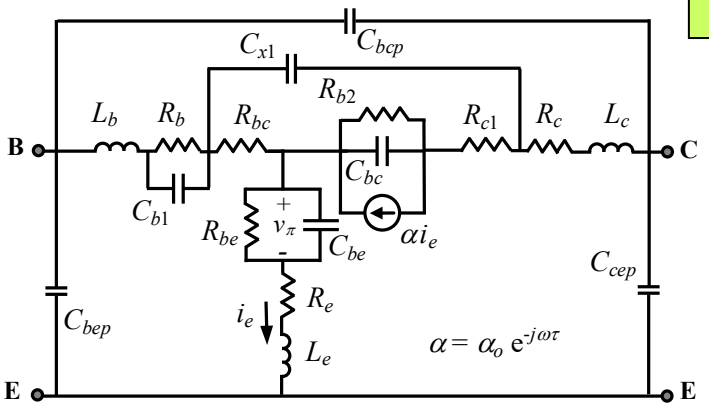
Due to the junction capacitance limitations (commutation time), BJTs are replaced by HBTs (Heterojunction Bipolar Transistors) in the high microwave frequency range due to their low doping of emitter and collector that can reduce the transit capacitances, and their high doping of base that can increase significantly the power gain.

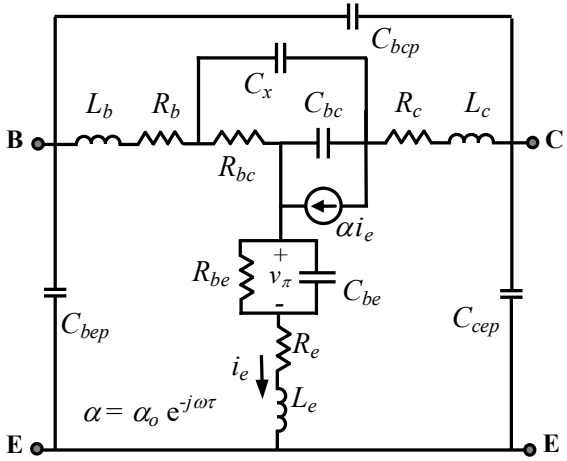


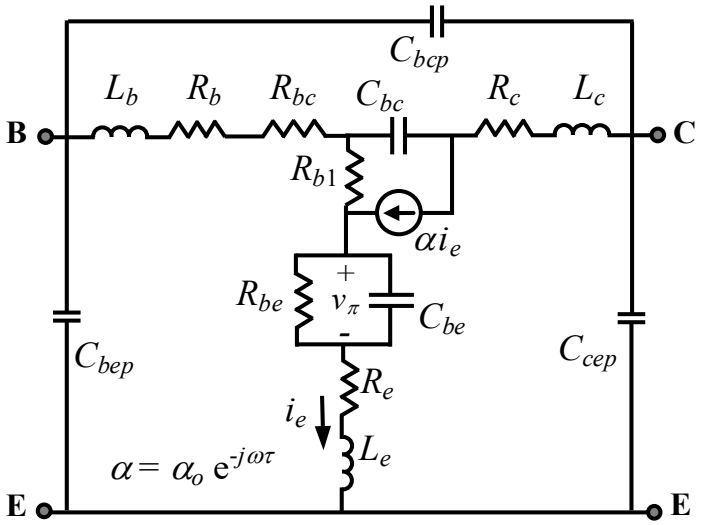


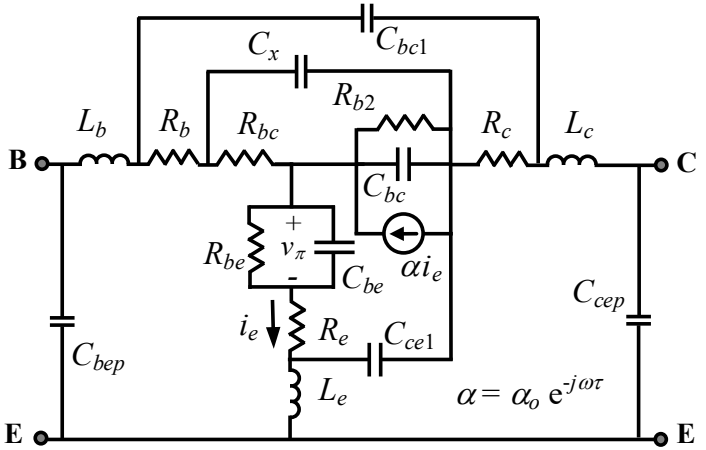
WHAT ABOUT THE EQUIVALENT CIRCUIT?











HBT TRANSISTORS

For its modeling, the "T" scheme is one of the most popular one. Suitable models are

Ebers-Moll model: I_e is coupled to I_c

$$I_c = -\alpha_f \, I_{es}\left(\exp\left(\frac{V_{eb}}{V_t}\right)-1\right)+ I_{cs}\left(\exp\left(\frac{V_{cb}}{V_t}\right)-1\right)$$

$$I_e = I_{es}\left(\exp\left(\frac{V_{eb}}{V_t}\right)-1\right)-\alpha_r \, I_{cs}\left(\exp\left(\frac{V_{cb}}{V_t}\right)-1\right)$$

Gummel-Poon model: I_e is function of the base-emitter I_{ee} and the base–collector current I_{cc}

$$I_e = \beta_f \, I_{ee} - \beta_r \, I_{cc}$$

HBT TRANSISTORS

- AlGaAs and InGaP MBE and MOCVD Layer Growth
  - InGaP is more reliable and allows higher power densities (MTTF > 10^6 hours at 150^{o}C)
- SiGe HBTs also becoming available
- Convenient Operation from positive voltage only
- Low knee voltage (< 1 volt) but high V_{BE} voltage (approx. 1.3 volts) makes efficient operation below 2 volts a problem
- High power density compared to pHEMT (by a factor of 2)
  - need to beware of higher operating junction temperatures
- Employed in many handsets today - Connexant (Rockwell) and RFMD have high penetration of HBT MMIC Amplifiers

SILICON GERMANIUM (SiGe) HBT

Advantages	Disadvantages
• Eight inch silicon wafers mean low production cost in high volume • All-optical process (also low cost) • Possible to add scads of logic onto RF chip (BiCMOS logic)	• Low V_{br}, as bad as 1.5 volts for IBM "9HP" • Electrically, Si is not a great insulator • Thermal runaway? • 110C max junction temperature • Not radiation hard • No equivalent of a switch FET, so phase shifters and attenuators are a problem • Not many foundries do SiGe • High setup charges due to expensive mask set

GaAs HBT

Advantages	Disadvantages
• Single power supply polarity • All-optical process	• Heat dissipation can be problem at small emitter size • Typically, reverse isolation is not as high as with PHEMT amplifiers, leading to poor amplifier directivity. • Collector resistors are required to stabilize amplifiers. These cut into your power efficiency.

HETERO STRUCTURE TRANSISTORS: COMPARISON

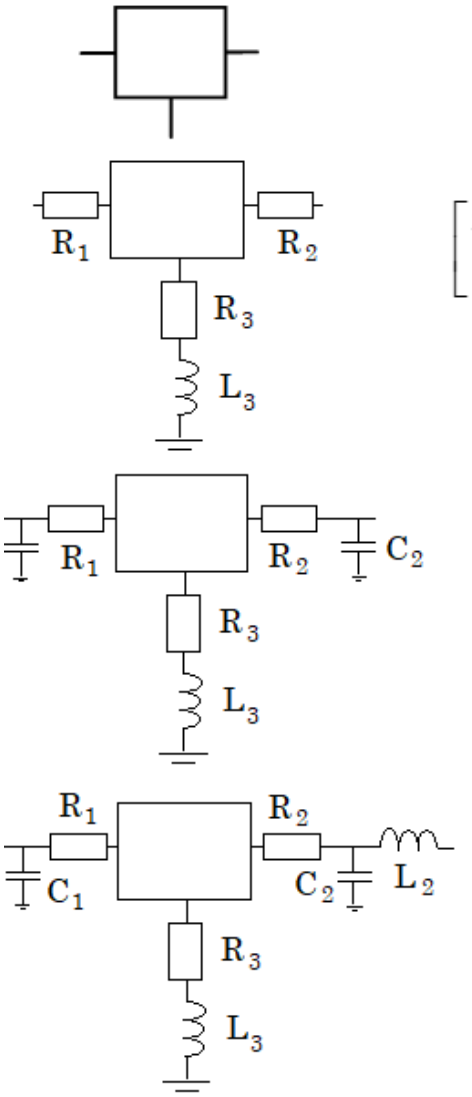
Heterostructures

- are semiconductor structures consisting of at least two different semiconductors
- are uncommon in mainstream electronics
- are frequently used in RF transistors
  - FETs: HEMTs
  - Bipolars: HBTs
- The RF transistors showing
  - the highest f_T and f_{max}
  - the highest output power densities
  - the lowest noise

  are heterostructure transistors.

Therefore it is useful to discuss some aspects of heterostructures in the following.

DETERMINATION OF THE OVERALL [S] MATRIX



$[Y_{int}] \rightarrow [Z]$

$$\begin{bmatrix} z_{11} + R_1 + R_3 + j\omega L_3 & z_{12} + R_3 + j\omega L_3 \\ z_{21} + R_3 + j\omega L_3 & z_{22} + R_2 + R_3 + j\omega L_3 \end{bmatrix}$$

$[Z] \rightarrow [Y]$

$$\begin{bmatrix} y_{11} + j\omega C_1 & y_{12} \\ y_{21} & y_{22} + j\omega C_2 \end{bmatrix}$$

$[Y] \rightarrow [Z]$

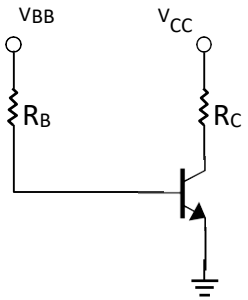
$$\begin{bmatrix} z_{11} + j\omega L_1 & z_{12} \\ z_{21} & z_{22} + j\omega L_2 \end{bmatrix} \rightarrow [Z] \rightarrow [S]$$

To determine the overall S-matrix of HBTs and FETs (and extracting their parameters), some manipulations are required.

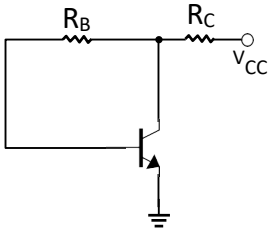
These transformations arevery useful if one wants to extract or characterize these transistors.

Here, $[Y_{int}]$ is the intrinsic admittance matrix.

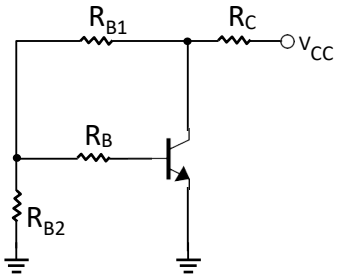
BIASING HBT TRANSISTORS



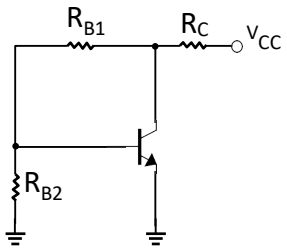
Non-stabilized
HBT Bias Network



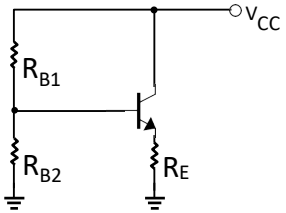
Voltage Feedback
HBT Bias Network



Voltage Feedback
with Current Source
HBT Bias Network

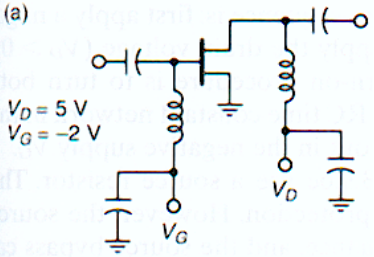
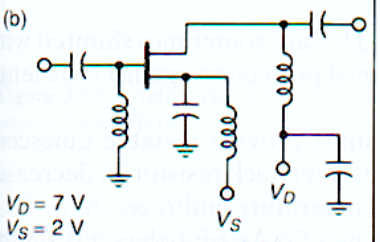
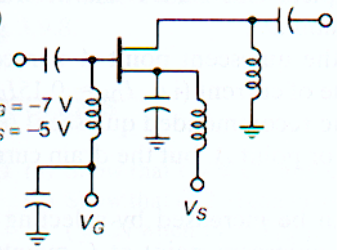
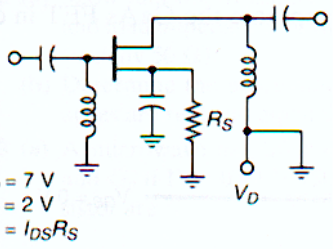
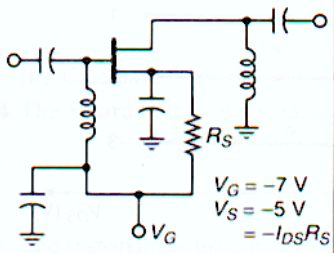


Voltage Feedback
with Voltage Source
HBT Bias Network

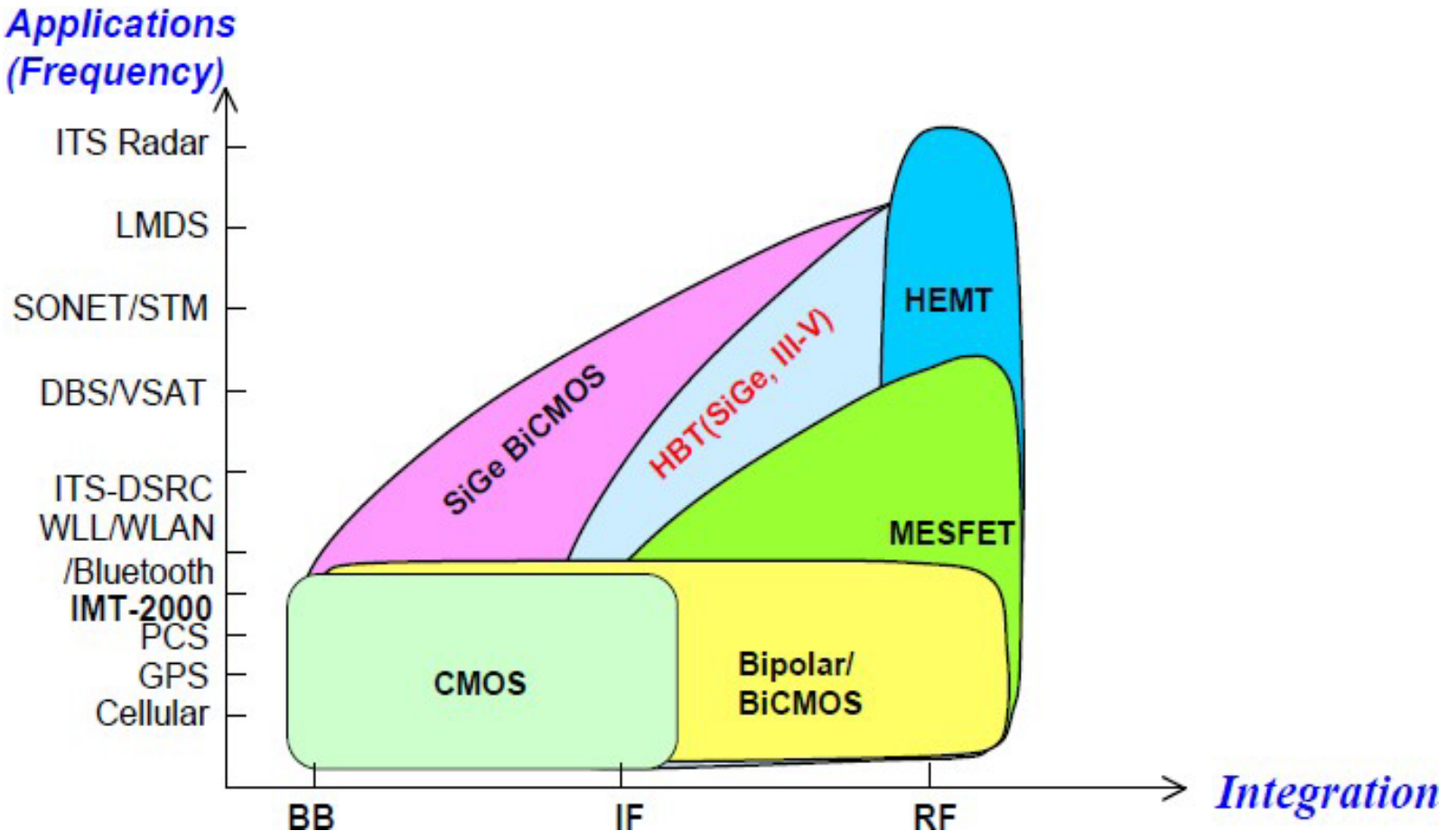


Emitter Feedback
HBT Bias Network

BIASING FET/HEMT TRANSISTORS

Figure	How	Amplifier characteristics	Power supply used
(a) 	Apply V_G, then V_D	Low noise High gain High power High efficiency	Bipolar, Minimum source inductance
(b) 	Apply V_S, then V_D	[same as (a)]	Positive supply
(c) 	Apply V_S, then V_G	[same as (a)]	Negative supply
(d) 	Apply V_D	Low noise High gain High power Lower efficiency Gain easily adjusted by varying R_S	Unipolar, incorporating R_S automatic transient protection
(e) 	Apply V_G	[same as (d)]	Negative unipolar, incorporating R_S

Technology review



Technology review

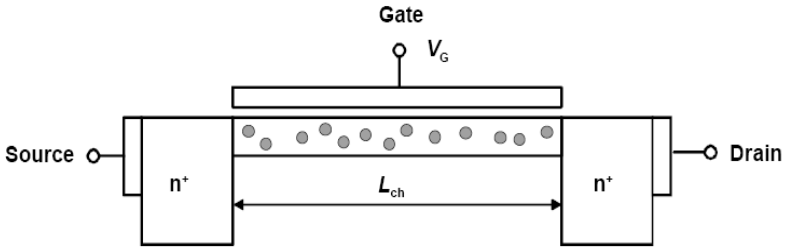
Some major issues have to be taken into account to make a transistor suitable for RF/microwave applications (i.e., reacts as fast as possible to the excitation):

- the physical parameters,
- the material used to fabricate the transistor,
- the cutoff and maximum frequencies, etc.

Question:

How to make a transistor fast?

Technology review



Design:
- short channel (small L_{ch})
- fast carriers (n-channel)

Material:
- fast carriers (high mobility, high velocity)

An RF transistor has to react as fast as possible on a variation of the input signal

FET – gate voltage V_G Bipolar Transistor – base voltage V_B (base current I_B)

➢ The charge distribution in the active region of the transistor has to be changed.

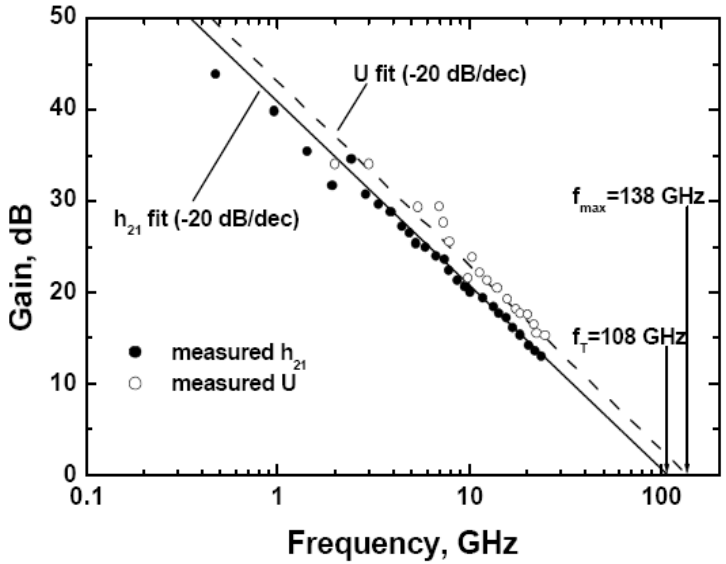
➢ To achieve this we have to consider
- Transistor Design
  Small active region of the transistor.
  Critical dimension – FET: gate length L
  – Bipolar: base thickness (width) w_B
- Material Issues
  Most important: Fast carriers

Technology review

Key parameters to consider in terms of FOM (**Factor of Merit**) are

- the transition frequency f_T (where current gain falls to unity)
- the maximum oscillation frequency f_{max} (at which the power gain drops to unity).

Technology review



Measured h_{21} and U of a GaAs MESFET
After K. Onodera et al., IEEE Trans. ED 38, p. 429.

h_{21} and U roll off at higher frequencies at a slope of –20 dB/dec.

Cutoff Frequency f_T
Frequency, at which the magnitude of the short circuit current gain h_{21} rolls off to 1 (0 dB).

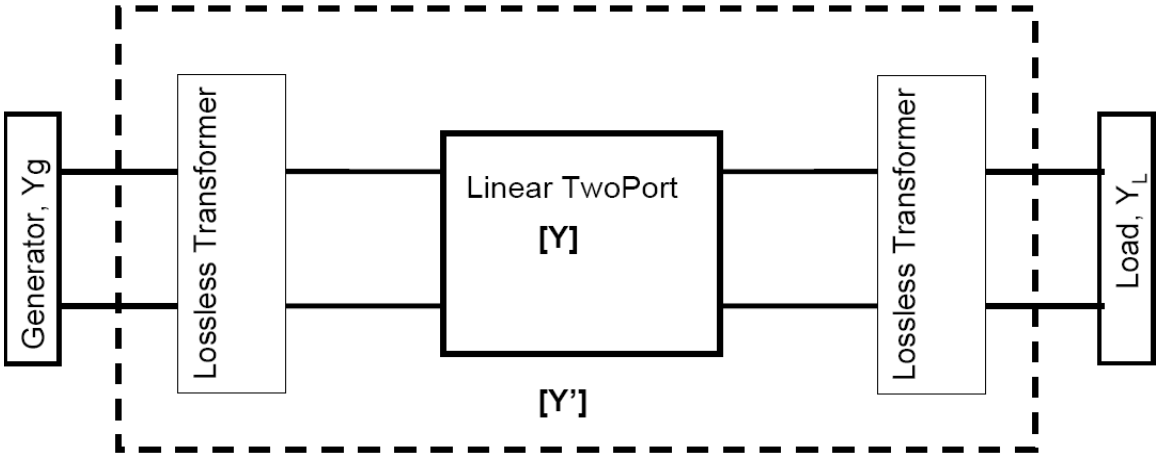
Maximum Frequency of Oscillation f_{max}
Frequency, at which the unilateral power gain U rolls off to 1 (0 dB).

Attention: Frequently f_{max} is NOT extrapolated from measured U, but from measured *MAG* or *MSG* !

Check before working with published f_{max} values !

Cutoff (transit) frequencies f_t, f_{max}

Maximum Available (or power) Gain (MAG), Mason's Gain, f_{max}

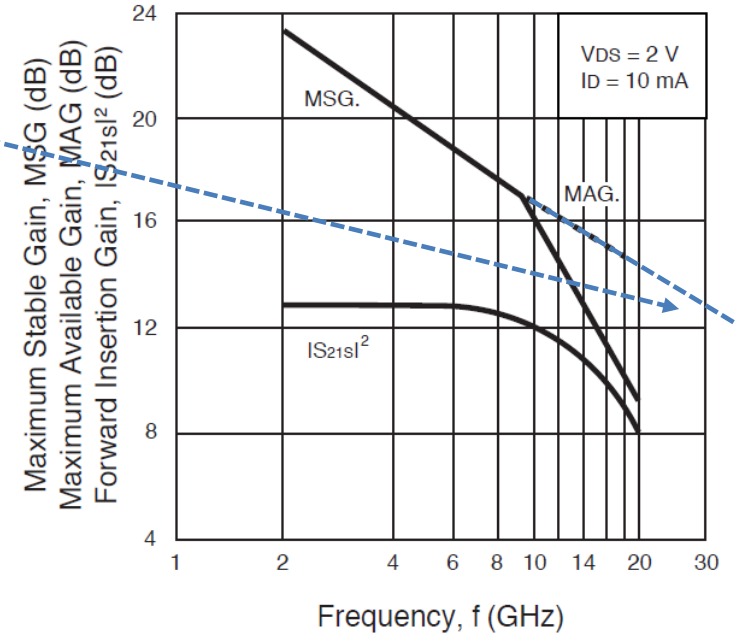


If $Y_{11}' = Y_g^*$ and $Y_{22}' = Y_L^*$

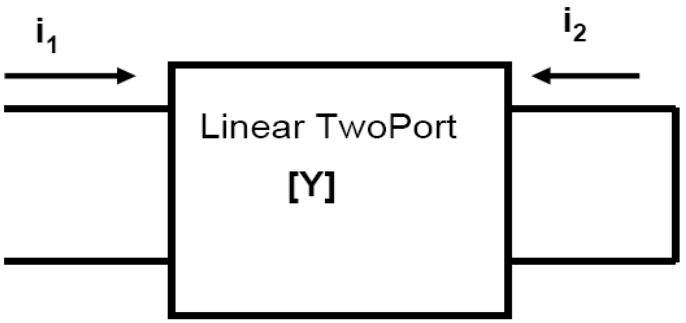
$$MAG = \left|\frac{Y_{21}}{Y_{12}}\right|(k - \sqrt{k^2 - 1}) \quad avec \quad k = \frac{2\,Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}$$

The transit frequency corresponding to MAG (dB) = 0 dB is called f_{max}

MAXIMUM AVAILABLE GAIN, FORWARD INSERTION GAIN vs. FREQUENCY



Current Gain, f_t



$$|H_{21}|^2(dB) = 10\log_{10}\left(\left|\frac{Y_{21}}{Y_{11}}\right|^2\right)$$

The transit frequency corresponding to $|H_{21}|^2$ (dB) = 0 dB is called f_t

FOMs – f_T and f_{max} vs f_{op}

Rule of thumb

$$f_T \sim n \times f_{op},\ f_T \sim f_{max}$$

- Low-noise transistors: $n \sim 10$ (conservative) , i.e., f_T should be around $10 \times$ the operating frequency f_{op} of the RF system in which the transistor is to be used.
- Power transistors: $n \sim 5$.

What does this mean?

If $n = 10$ and $f_T = f_{max}$, we have 20 dB unilateral power gain U at f_{op}. Note that U is the upper limit for the power gain a transistor can achieve. The actual gain in a realistic circuit environment, e.g. G_a for minimum noise, will be several dB lower.

Examples:

GaAs MESFET:	f_{max} = 70 GHz	U @ 12 GHz = 15.3 dB, G_a @ 12 GHz = 11 dB
AlGaAs/GaAs HEMT:	f_{max} = 50 GHz	U @ 12 GHz = 12.4 dB, G_a @ 12 GHz = 9 dB
AlGaAs/GaAs HEMT:	f_{max} = 120 GHz	U @ 18 GHz = 16.5 dB, G_a @ 18 GHz = 11.6 dB

TRANSISTORS: COMPARISON

Si technology

(www.target-org.net)

Silicon for RF (applications)

Microwave applications:

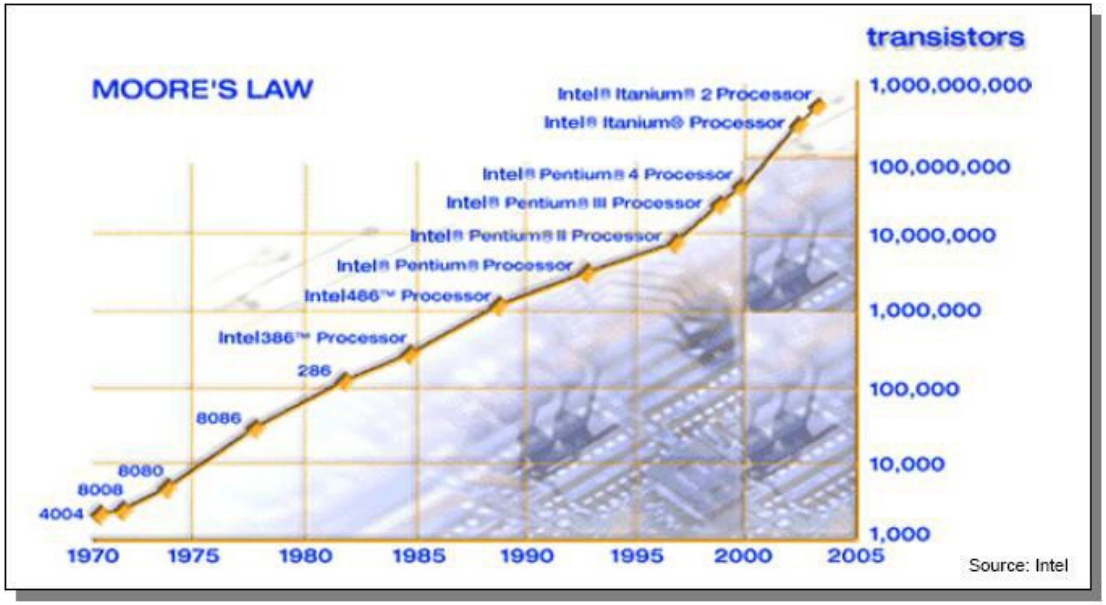
- Cell phones (0.85-2.6 GHz)
- GPS (1.8 GHz)
- WLAN (2.4 GHz)
- Bluetooth (2.4 GHz)
- WLAN (5 GHz)
- DBS (12 GHz)
- HiperLink (17 GHz)
- LMDS (27-35 GHz)
- MVDS (44 GHz)
- CAR (77 GHz)
- Radio astronomy (>100 GHz)

Silicon dominates up to around 3-5 GHz.

This is also the field for the real mass markets.

Note: Microprocessors today operates above 3 GHz!

Enormous development of silicon technology



TRANSISTORS: COMPARISON

Capability	D-Mode FET	D-Mode HEMT	E-Mode FET	E-Mode HEMT	GaAs HBT	SiGe HBT	Si BJT	Si MOSFET
Linearity	+	+	0	0	++	0	–	–
Noise figure	+	++	+	++	–	0	–	–
Power	++	++	+	+	++	++	++	++
PAE	++	++	0	0	+	+	+	+
Control circuits Mixers/oscillators	++	++	+	+	0	+	–	–
Passive components	+	+	+	+	+	–	–	–
Integration on a single chip	++	+	–	–	0	0	0	0
Single polarity supply	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Turn-on voltage control	0	0	0	0	++	++	++	+
Multiple thresholds	++	–	+	–	N/A	N/A	N/A	++
Low-voltage operation	++	++	+	+	+	0	0	–
Maximum operating temperature	++	++	++	++	+	0	0	0
Tj (max) (°C)	150	150	150	150	125	125	125	125
Wafer size (mm)	100	100	100	100	100	200	200	200
Technology maturity	+	0	+	0	+	–	++	++
Cost	Moderate	High	Moderate	High	Moderate-High	Low	Low	Low
Maximum frequency of operation	+	++	+	++	+	+	0	0

++, Excellent; +, Good; 0, Fair; –, Poor

Table 40a High-Performance Logic Technology Requirements—Near-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
DRAM ½ Pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	*90*	*78*	*68*	*59*	*52*	*45*	*40*	*36*	*32*
MPU Physical Gate Length (nm)	*32*	*28*	*25*	*22*	*20*	*18*	*16*	*14*	*13*
L_g: Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
EOT: Equivalent Oxide Thickness [2]									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
Gate Poly Depletion and Inversion-Layer Thickness [3]									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
$J_{g.limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm^2)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm^2)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm^2)							6.25E+02	7.86E+02	8.46E+02
V_{dd}: Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185

Manufacturable solutions exist, and are being optimized

Manufacturable solutions are known

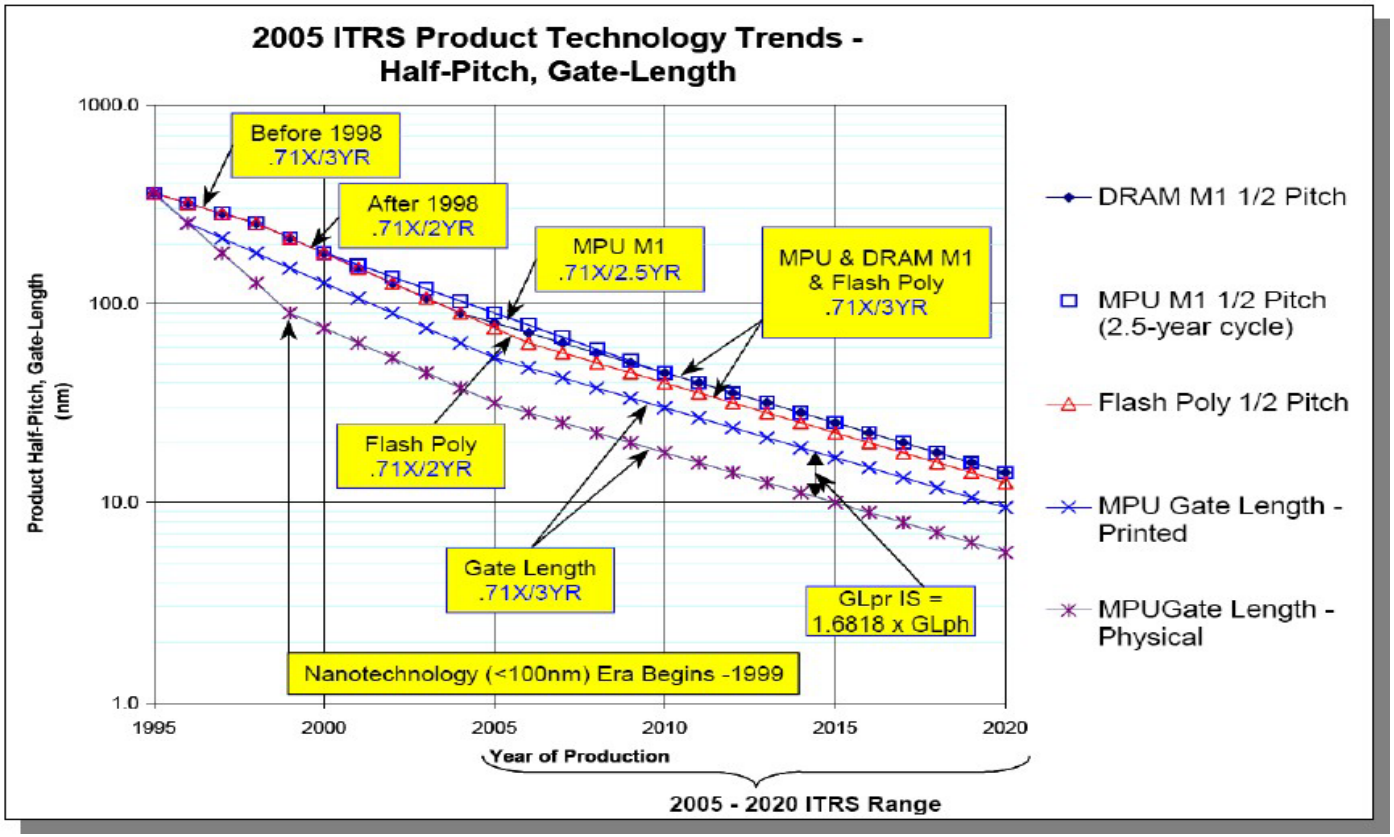
Interim solutions are known

Manufacturable solutions are NOT known

Source: ITRS 2005

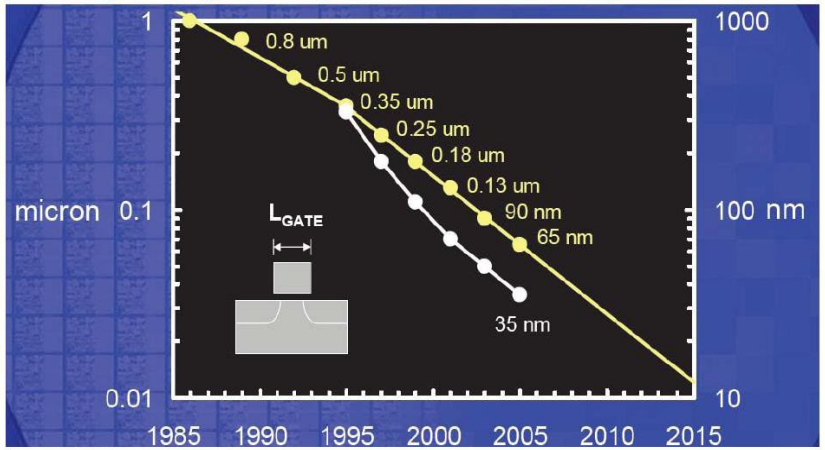
ITRS (International Roadmap for Semiconductors) describes the necessary and expected development

Example: scaling trend of gate length Lg



Aggressive scaling of L_G

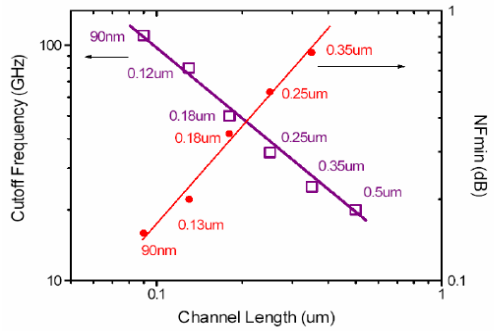
Faster gate length scaling to maintain transistor performance

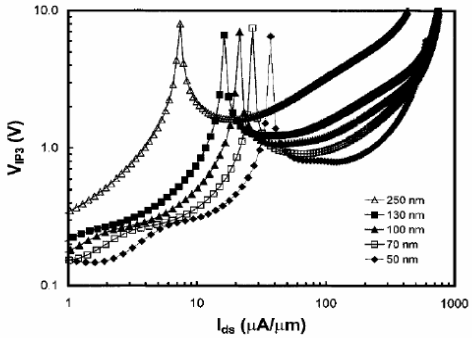


Source: Intel

RF performance vs. scaling

- In general RF-CMOS performance increases strongly with transistor scaling
- Linearity performance may be a problem – alternative scaling methodology can reduce the problem





SUMMARY

Uses and characteristics of solid-state devices described in this chapter (the frequency range is as of date 2001. So given here just as illustration. These ranges change yearly).

Device	Frequency Range	Uses and Characteristics
Schottky-barrier Diode	From RF to sub- millimeter range	Mixers, modulators, and detectors. Occasionally used for frequency multipliers and switches.
PN-Junction Varactor	Up to 60GHz	Frequency multipliers, voltage controlled oscillators.
Schottky Varactor	To several hundred GHz	Frequency multipliers, voltage controlled oscillators.
SRD	Up to 30GHz	Frequency multipliers with fast pulses and high-order frequency multiplication.
BJT	Usually X-band and below. Mm-wave BJTs have been made	Small-signal amplifiers with moderate noise. Fast digital circuits. Good power devices. Low 1/f noise makes them ideal for low-noise oscillators.

Device	Frequency Range	Uses and Characteristics
HBT	Although some HBTs may have gain at 80GHz, practical limits are around 60GHz.	Power amplifiers, low-noise oscillators. Fast analog circuits. Lower 1/f noise than MESFETs and HEMTs. Preferred for oscillators.
JFET	Up to the VHF/UHF range	Low-cost. Moderately low-noise applications in amplifiers, mixers, oscillators, and switches.
MESFET	Up to 40GHz. Can go higher, but HEMTs are usually preferred.	Amplifiers, oscillators, mixers, modulators, frequency multipliers, control components, etc. Much better noise figure than HBTs but higher 1/f noise.
HEMT	Highest frequency device available. Over 200GHz	Much the same as MESFETs. Best syuited for small-signal, low-noise uses, but power devices are possible. Much better noise figure than HBTs but higher 1/f noise.
MOSFET	Up to 6 GHz for advanced technologies. 2-3 GHZ more common.	Analog, digital, and RF Si IC applications. MESFETs and HEMTs have much lower noise figures at microwave frequencies.

Comparison between technologies

GaAs MESFET

Advantages	Disadvantages
Mature technology	Limited to KU-band
Low cost	GaAs PHEMT has better noise figure and power performance
Great microwave substrate	Positive and negative voltage are needed
Six inch waveform	
16-20 volt breakdown possible	
Cheap to produce but more than silicon	
Temperature up to 150C	

GaAs PHEMT

Advantages	Disadvantages
Excellent power and efficiency	Positive and negative voltage are needed
Breakdown voltage 12 v at best, operate typically at 5 and 6 volt	Increase cost
Temperature up to 150C possible	

GaAs MHEMT

Advantages	Disadvantages
Extremely low Nosie figure	Breakdown voltage lower than PHEMT
Higher fmax more than 100 GHz	Low operating voltage
Chanel temperature up to 150 C	Positive and negative voltage are needed

Comparison between technologies

Silicon CMOS

Advantages	Disadvantages
Low cost	12 inch big wafer
Can operate up to 110 C	Not good for Microstrip (lossy)
Very good amplifier above x band	Pretty good heat dissipater

Idium phosphide (InP) HEMT

Advantages	Disadvantages
Low noise figure	More expensive than GaAs due to material cost
Useful through W band	Fragile
	Low breakdown voltage

Gallium nitride (GaN)

Advantages	Disadvantages
Up to 10X the power density of GaAs PHEMT	Very expensive
Higher operating voltage, less current	Deal with a huge heat flux
Excellent efficiency possible	
Can operate hotter than GaAs,Si or SiGe	

GaAs HBT

Advantages	Disadvantages
All optical process	Heat dissipation can be problem
Single power supply polarity	Reverse isolation is not as high as PHEMT amplifier ,poor amplifier directivity
	Collector resistors are need for stability amplifier

GALLIUM NITRIDE (GaN)

GaN transistors behave very similarly to Si Power MOSFETs. A positive bias on the gate relative to the source causes a field effect which attracts electrons that complete a bidirectional channel between the drain and the source.

Since the electrons are pooled, as opposed to being loosely trapped in a lattice, the resistance of this channel is quite low. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region, and once again, giving it the capability to block voltage.

To obtain a higher voltage device, the distance between the Drain and Gate is increased. As the resistivity of our GaN pool is very low, the impact on resistance by increasing blocking voltage capability is much lower when compared with Silicon. EPC's first generation of devices is shown as well.

Silicon MOSFET has approached its theoretical limits. Progress in silicon has slowed to the point where small gains have significant development cost. GaN is young in its life cycle and will see significant improvement in the years to come.

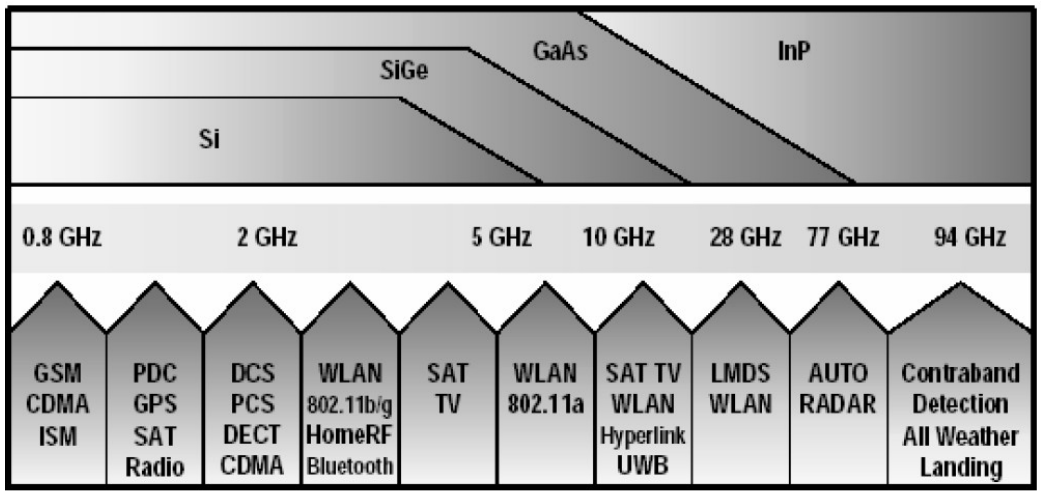
GALLIUM NITRIDE (GaN)

Advantages	Disadvantages
• Up to 10X the power density of GaAs PHEMT has been demonstrated. • Higher operating voltage, less current. • Excellent efficiency possible. • SiC substrates are great heat spreaders. • Can operate hotter than GaAs, Si or SiGe.	• Expensive! • Reliability not established yet • Huge heat flux.

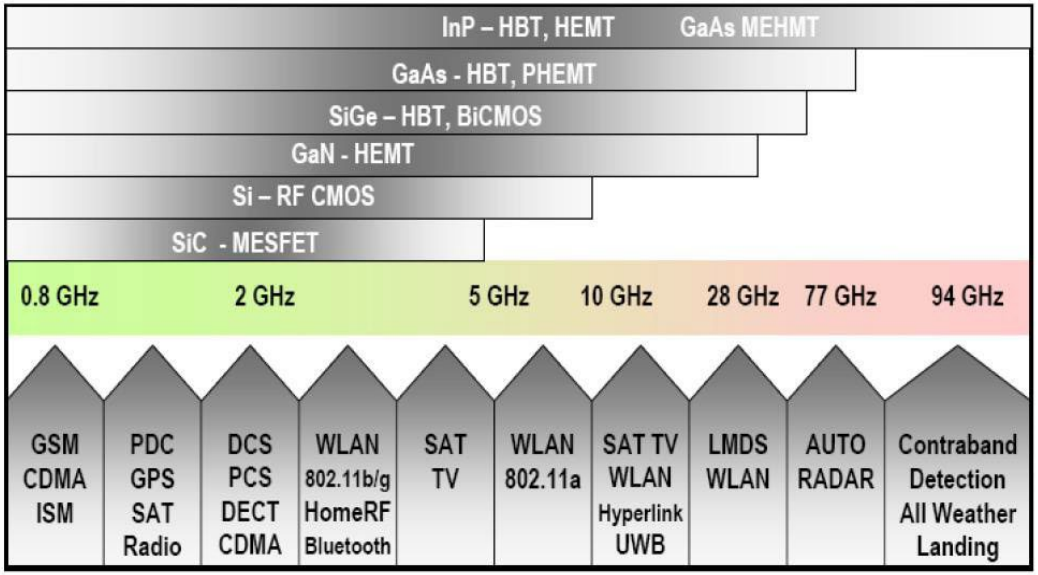
COMPARISON

Property	Units	Silicon	GaAs	4H-SiC	GaN
Bandgap	eV	1.11	1.43	3.2	3.4
Breakdown field	V/cm	$7*10^5$	$7*10^5$	$35*10^5$	$35*10^5$
Saturation velocity	Cm/sec	$1*10^7$	$1*10^7$	$2*10^7$	$1.5*10^7$
Saturation field	V/cm	$8*10^3$	$3*10^3$	$25*10^3$	$15*10^3$
Thermal conductivity	W/cm-K	1.5	0.46	4.9	1.7/substrate
Electron mobility	$Cm^2/V\text{-}s$	1350	6000	800	1000
Hole mobility	$Cm^2/V\text{-}s$	450	330	120	300

TRANSISTORS: APPLICATIONS



Taken from: ITRS 2003 Edition.
Chapter *Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications*



TRANSISTORS: APPLICATIONS

Depending on applications, the following features are required:

* maximum power gain bandwidth,
* minimum noise figure and/or low 1/f noise,
* maximum power-added efficiency,
* low thermal resistance,
* high temperature of operation and reliability,
* low leakage current under cut-off operation,
* low leakage current under cut-off operation,
* semi-insulating substrate,
* Cost effective,
* maximum conversion gain,
* low intermodulation products,
* low on-resistance/high-off resistance,
* high linearity or nonlinearity,
* low power dissipation,
* multi-functionality,
* low/multiple single power supply,
* mature technology,

etc.

TRANSISTORS: APPLICATIONS BELOW 6 GHz

Frequency /Technology	Cellular 900MHz	Sat. 1.6GHz	PCS/3G 1.8-2.2GHz	ISM/Sat. 2.4GHz	WLL 3.4 GHz	HyperLan/NII 5.8 GHz
Si Bipolar	X		X			
LDMOS	X	X	X	X	X	X
MESFET	X	X	X	X		
pHEMT			X			
HBT	X		X	X		X
SiGe HBT	X		X			
SiC FET	X					X
GaN FET						

Thank you !

End of Chapter 2