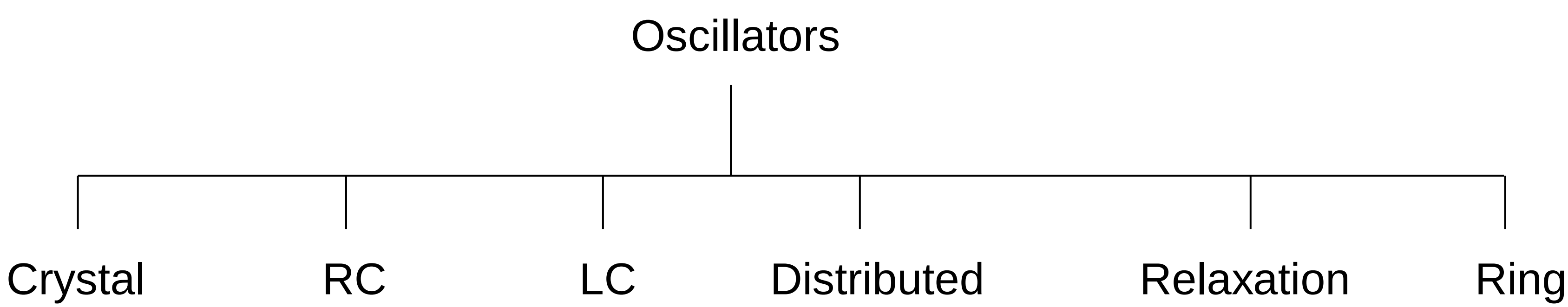
Chapter 6

Microwave Oscillators

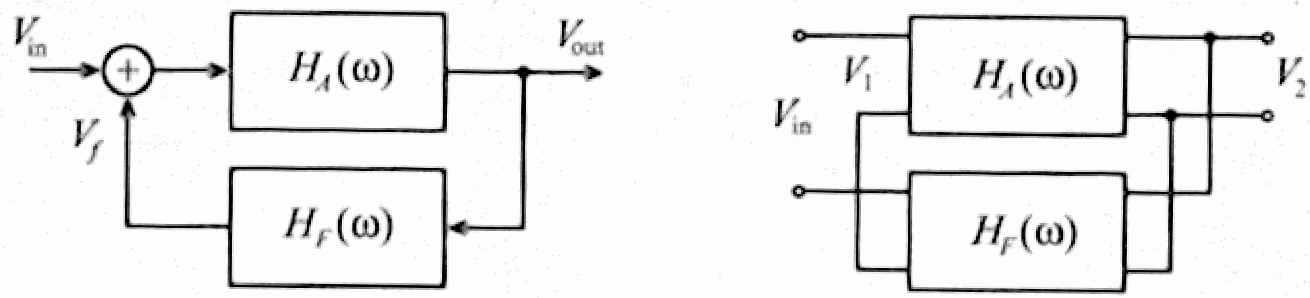
SOME THEORY

DEFINITION AND CLASSIFICATION

An oscillator is a network that is able to generate an output periodic signal without using a periodic input excitation. In other words, it can be viewed as a dc-to-ac converter and can be explained in terms of feedback circuit. Oscillators can be classified as crystal, RC, LC, relaxation, ring, and distributed oscillators.



An oscillator can be viewed as a loop that causes a positive feedback.



(a) Closed-loop circuit model (b) Network representation

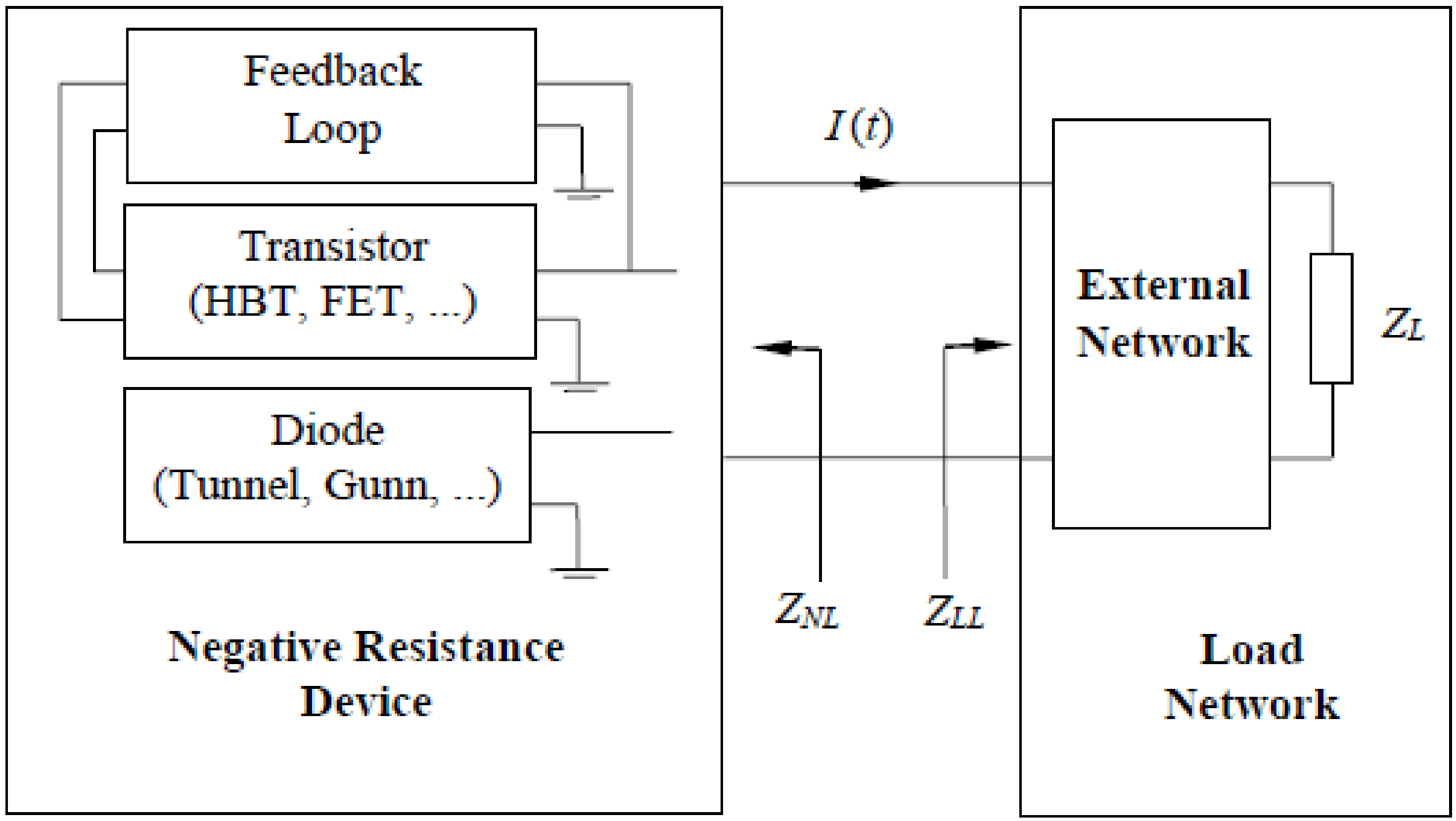
For steady oscillation, two conditions must be simultaneously met for the closed-loop gain

$$H(\omega_o) = \frac{V_{out}}{V_{in}} = \frac{H_A(\omega_o)}{1 - H_F(\omega_o)H_A(\omega_o)}$$

- The loop gain, $|H(j\omega_o)|$ must be equal to unity (condition of oscillation) at the frequency ω_o,
- The total phase shift around the loop, /_ $H(j\omega_o)$_ must be equal to zero or 180^o at the frequency ω_o if the dc feedback is negative (condition of stability).

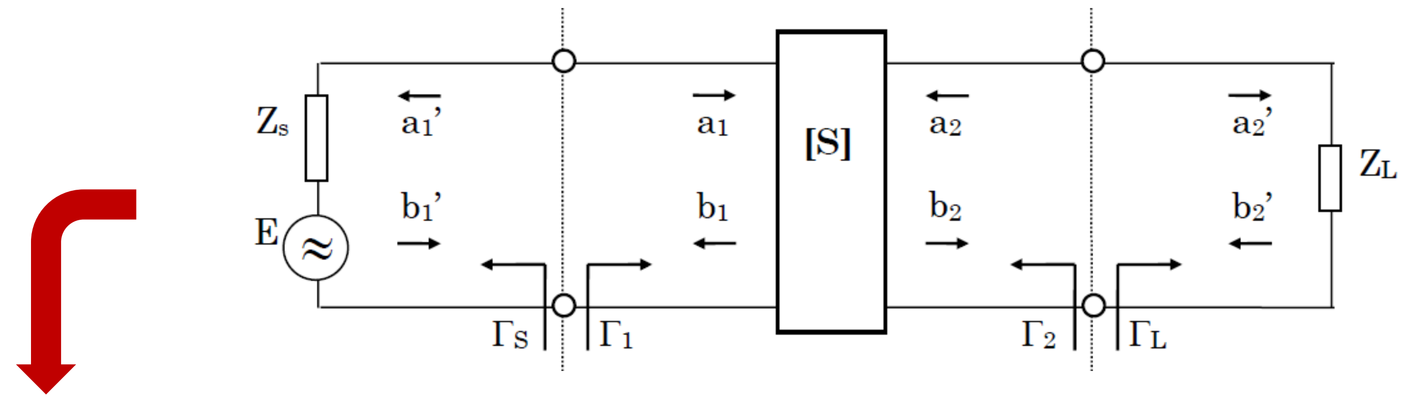
These oscillation criteria can be expressed in terms of negative resistance provided by a diode (e.g., Tunnel diode) or an unstable transistor.

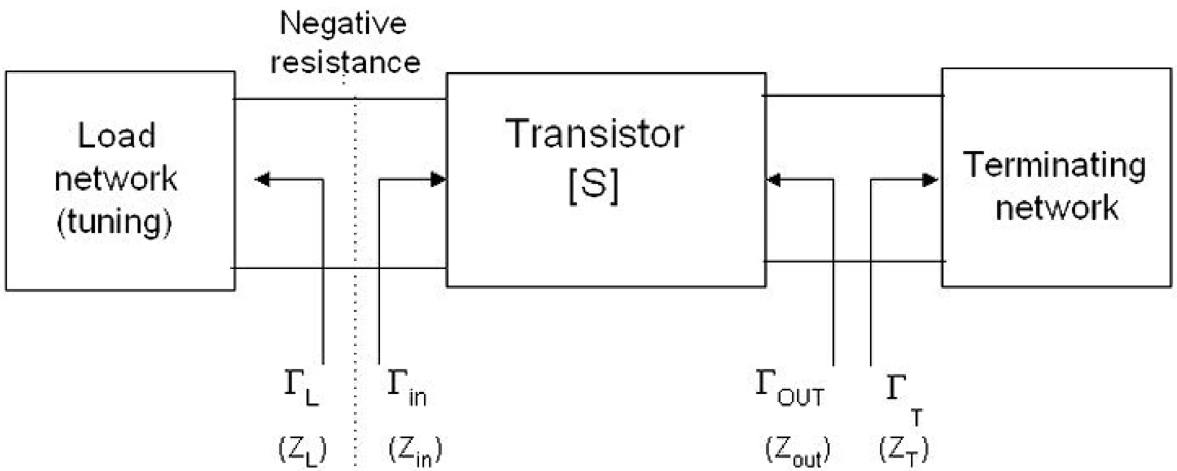
$$R_{NL} = -R_{LL} \qquad \text{and} \qquad j(X_{NL} + X_{LL}) = 0 \qquad \Rightarrow \quad \Gamma_{NL}.\Gamma_{LL} = 1$$



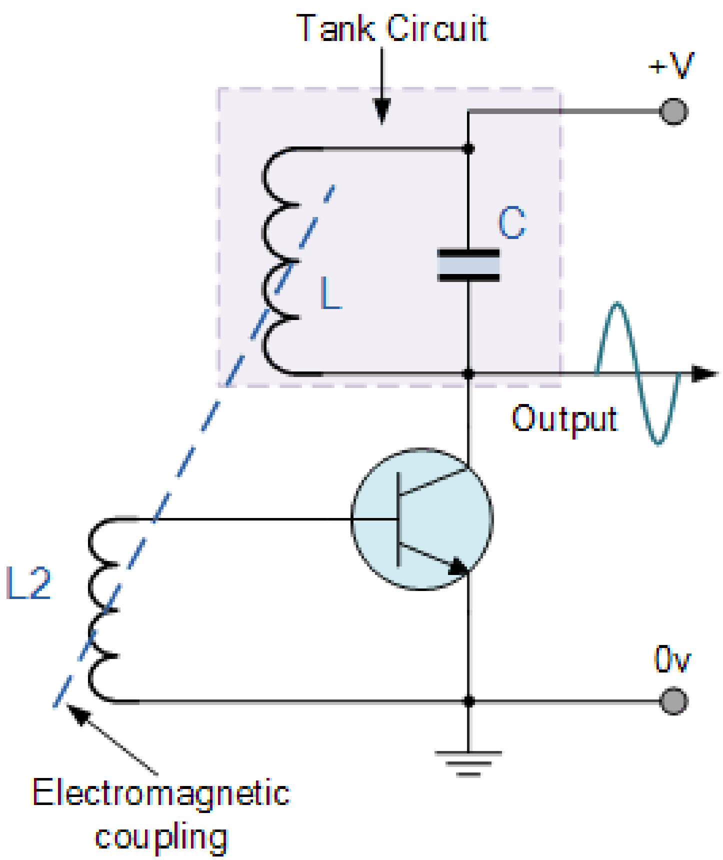
ANALYSIS BY THE TRANSISTOR S-PARAMETERS

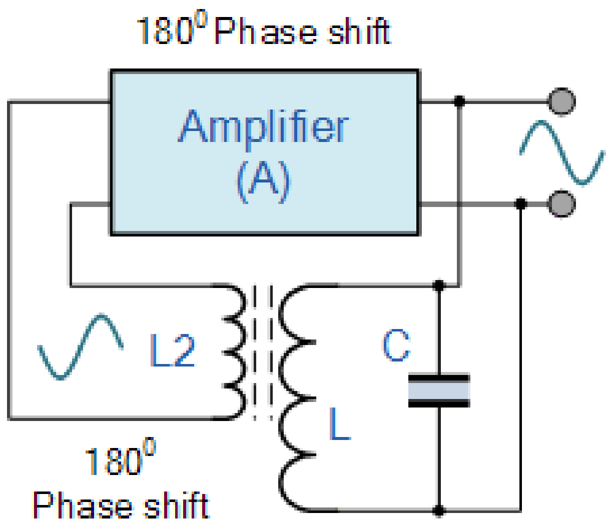
(FROM AMPLIFIER TO OSCILLATOR)





WORKING PRINCIPLE OF TRANSISTOR BASED OSCILLATORS





ANALYSIS BY THE TRANSISTOR S-PARAMETERS

(FROM AMPLIFIER TO OSCILLATOR)

The unknown incident power a_2 must be minimized to assure an optimum efficiency.

Let A be the gain defined as

$$A = \frac{b_2}{a_1} \qquad \Rightarrow \qquad a_2 = \frac{A - S_{21}}{S_{22}} a_1$$

$$A_{opt} = \frac{1}{|S_{22}|^2 + |S_{12}|^2 - 1}\left(|S_{12}|^2 S_{21} - S_{21} - S_{22} S_{11} S_{12}^*\right)$$

ANALYSIS BY THE TRANSISTOR S-PARAMETERS

(FROM AMPLIFIER TO OSCILLATOR)

The following steps can summarize this process (mainly experimental):

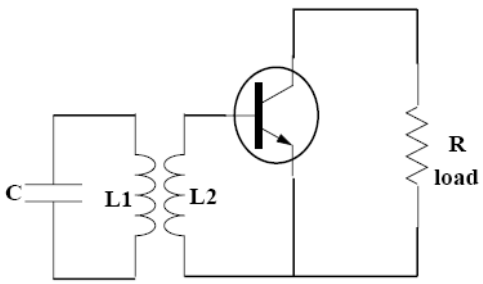
- Choose a convenient range for a_1.
- Fix a value for a_1 and measure S_{11} and S_{21}. Then, estimate a_2 to obtain S_{12} and S_{22}.
- Determine A_{opt}, deduce the ratio a_2/a_1, then a_2 (these two quantities are independent of the reference planes). Therefore, the output parameters S_{12} and S_{22} can be obtained as well as the optimum output power.
- Vary a_1. A curve of the optimum output power versus the incident power can be plotted.
- Select a_1 that gives the highest output power. Note the corresponding a_2.

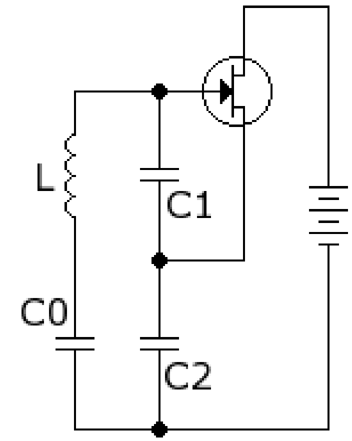
The main limitation is in the assumption that **S_{11} and S_{21} depend only of the incident power a_1** (and similarly for S_{22} and S_{12} versus a_2). This could lead to significant errors for some power devices.

ANALYSIS BY Z OR Y PARAMETERS

Main types of LC Oscillators Circuits

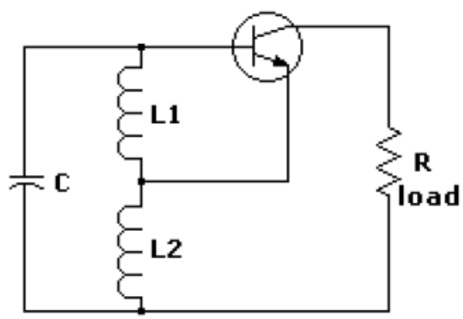
Armstrong



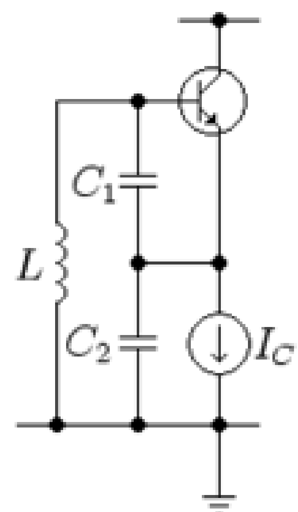


Clapp

Hartley



Colpitts



ANALYSIS BY Z OR Y PARAMETERS

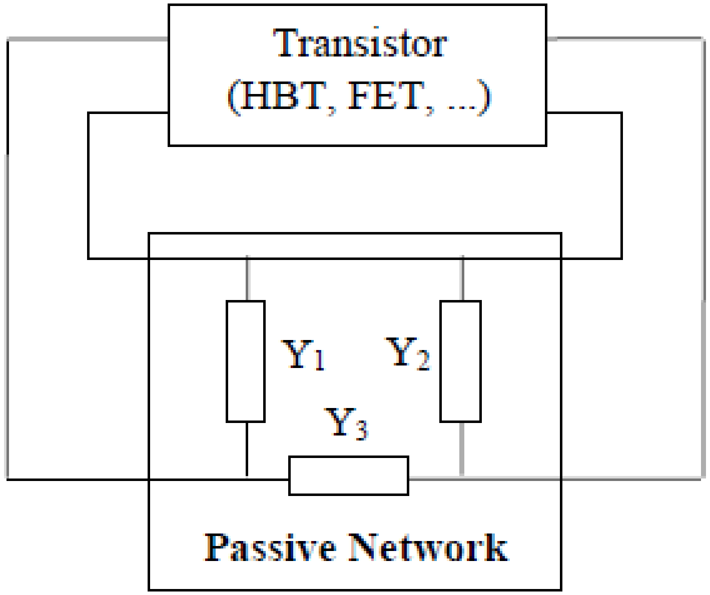
Usually, the oscillator configuration highlights unknown impedances or admittances

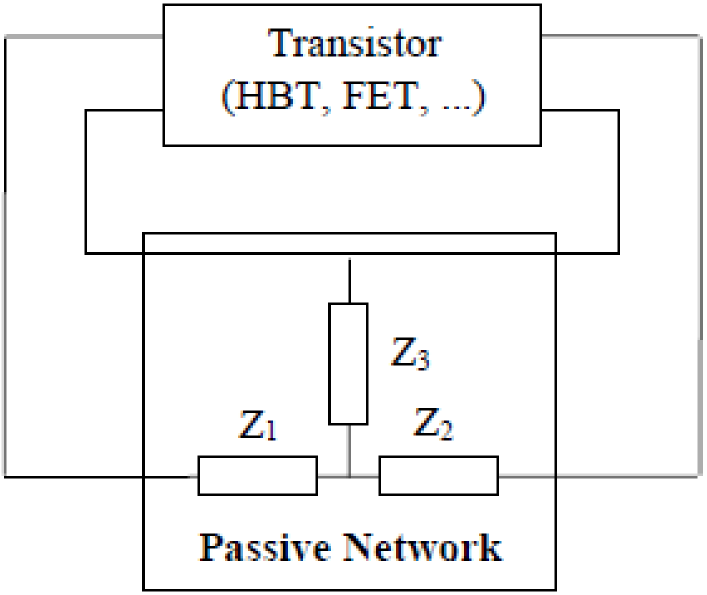
$$\{ Z_1, Z_2, Z_3 \} \quad \text{or} \quad \{Y_1, Y_2, Y_3\}$$

with

$$Z_i = R_i + j\,X_i \quad \text{and} \quad Y_i = G_i + j\,B_i$$

Why considering T or π networks ?





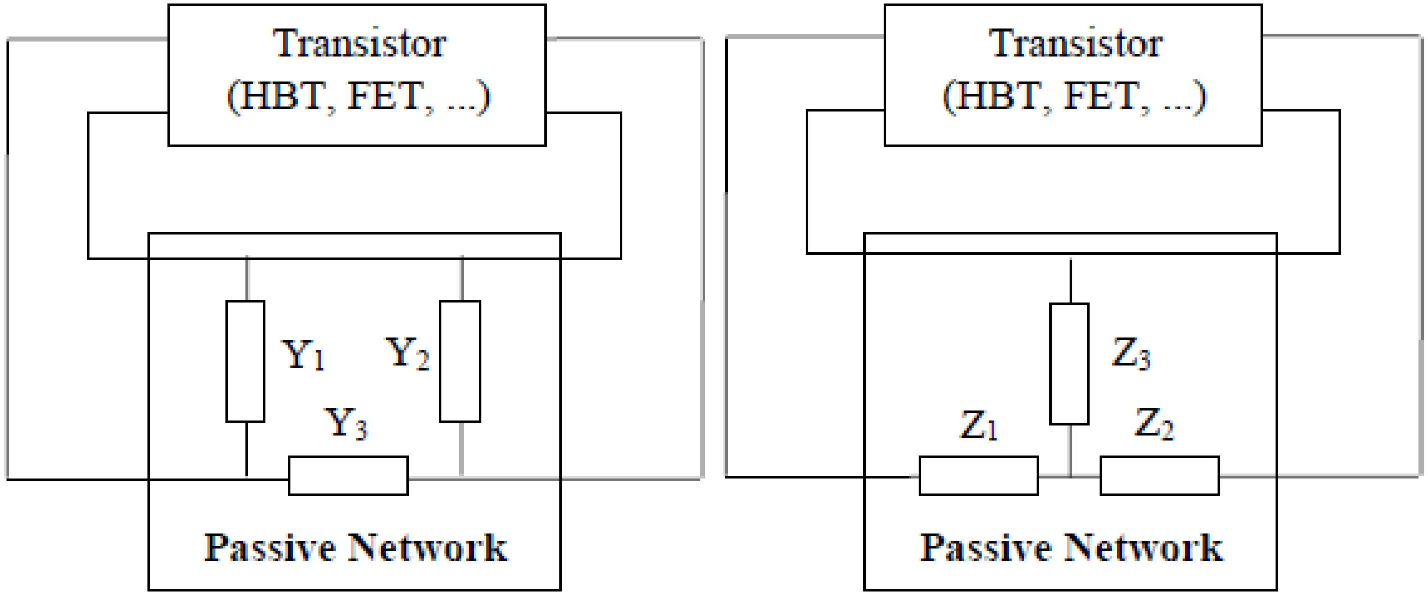
ANALYSIS BY Z OR Y PARAMETERS

We have in total 6 unknown variables: $\{Z_1, Z_2, Z_3\}$ or $\{Y_1, Y_2, Y_3\}$

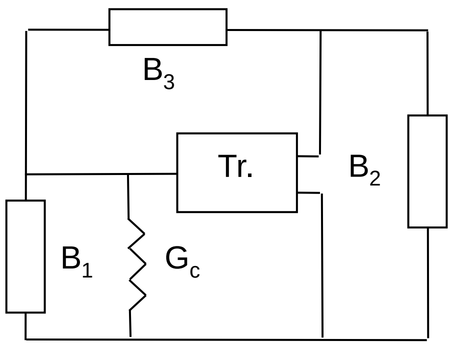
However, we have 2 ports so 2 equations.

Therefore:

- we set two of the impedances/admittances as purely reactive and
- the real part of the third impedance/admittance is set as the oscillator load R_c or G_c.



ANALYSIS BY Z OR Y PARAMETERS – π NETWORKS

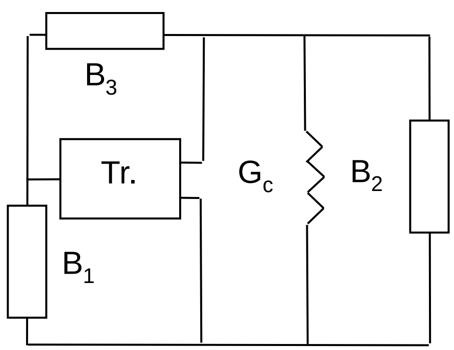


$$G_c = C_1 + A_r C_3 + A_i C_4$$

$$B_1 = C_2 + (1 - A_r)(C_4 + C_3 A_r / A_i)$$

$$B_2 = C_3 (A_r - 1)/A_i + C_4$$

$$B_3 = -C_3 A_r / A_i - C_4$$

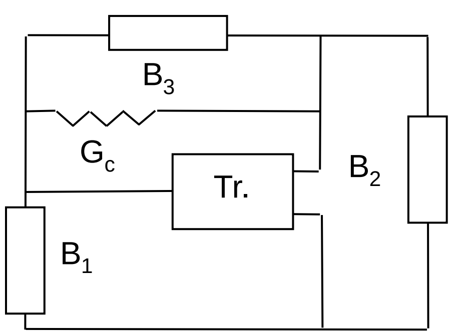


$$G_c = (C_1 + A_r C_3 + A_i C_4)/|A|^2$$

$$B_1 = C_1 (A_r - 1)/A_i + C_2$$

$$B_2 = (C_1 (A_r - |A|^2)/A_i + A_r C_4 - A_i C_3)/|A|^2$$

$$B_3 = C_1 / A_i$$



$$G_c = (C_1 + A_r C_3 + A_i C_4)/|A - 1|^2$$

$$B_1 = (C_1 + C_3) A_r / A_i + C_2 + C_4$$

$$B_2 = -(C_1 + C_3)/A_i$$

$$B_3 = (C_1 - (1 - A_r) G_c)/A_i$$

$$C_1 = -\mathrm{Re}\ (Y_{11} + A Y_{12})$$

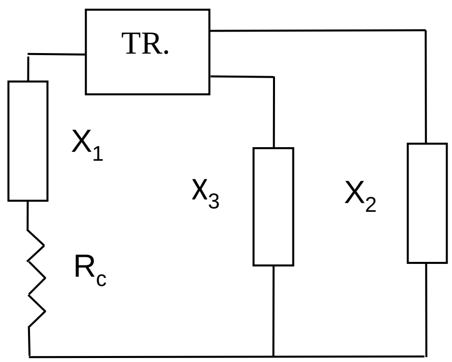
$$C_2 = -\mathrm{Im}\ (Y_{11} + A Y_{12})$$

$$C_3 = -\mathrm{Re}\ (Y_{21} + A Y_{22})$$

$$C_4 = -\mathrm{Im}\ (Y_{21} + A Y_{22})$$

$$A = A_r + j A_i = -(Y_{21} + Y_{12}^*)/2\,\mathrm{Re}(Y_{22})$$

ANALYSIS BY Z OR Y PARAMETERS – T NETWORKS

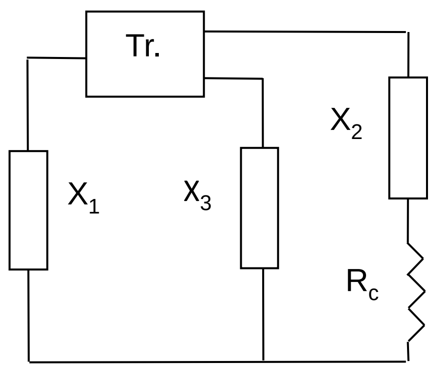


$$R_c = D_1 + F_r D_3 + F_i D_4$$

$$X_1 = D_2 - (1 + F_r)(D_4 + D_3 F_r / F_i)$$

$$X_2 = -D_3(1 + F_r)/F_i - D_4$$

$$X_3 = D_3 F_r / F_i + D_4$$

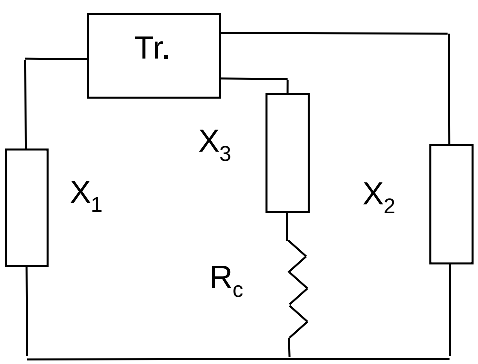


$$R_c = (D_1 + F_r D_3 + F_i D_4)/|F|^2$$

$$X_1 = D_1(1 + F_r)/F_i + D_2$$

$$X_2 = (D_1(F_r + |F|^2)/F_i + F_r D_4 - F_i D_3)/|F|^2$$

$$X_3 = -D_1/F_i$$



$$R_c = (D_1 + F_r D_3 + F_i D_4)/|1 + F|^2$$

$$X_1 = (D_1 - D_3)F_r/F_i + D_2 - D_4$$

$$X_2 = (D_1 - D_3)/F_i$$

$$X_3 = \frac{\left((1 + F_r)(D_4 - (D_1 - D_3)F_r/F_i) - F_i D_1\right)}{|1 + F|^2}$$

$$D_1 = -\mathrm{Re}\ (Z_{11} + F Z_{12})$$

$$D_2 = -\mathrm{Im}\ (Z_{11} + F Z_{12})$$

$$D_3 = -\mathrm{Re}\ (Z_{21} + F Z_{22})$$

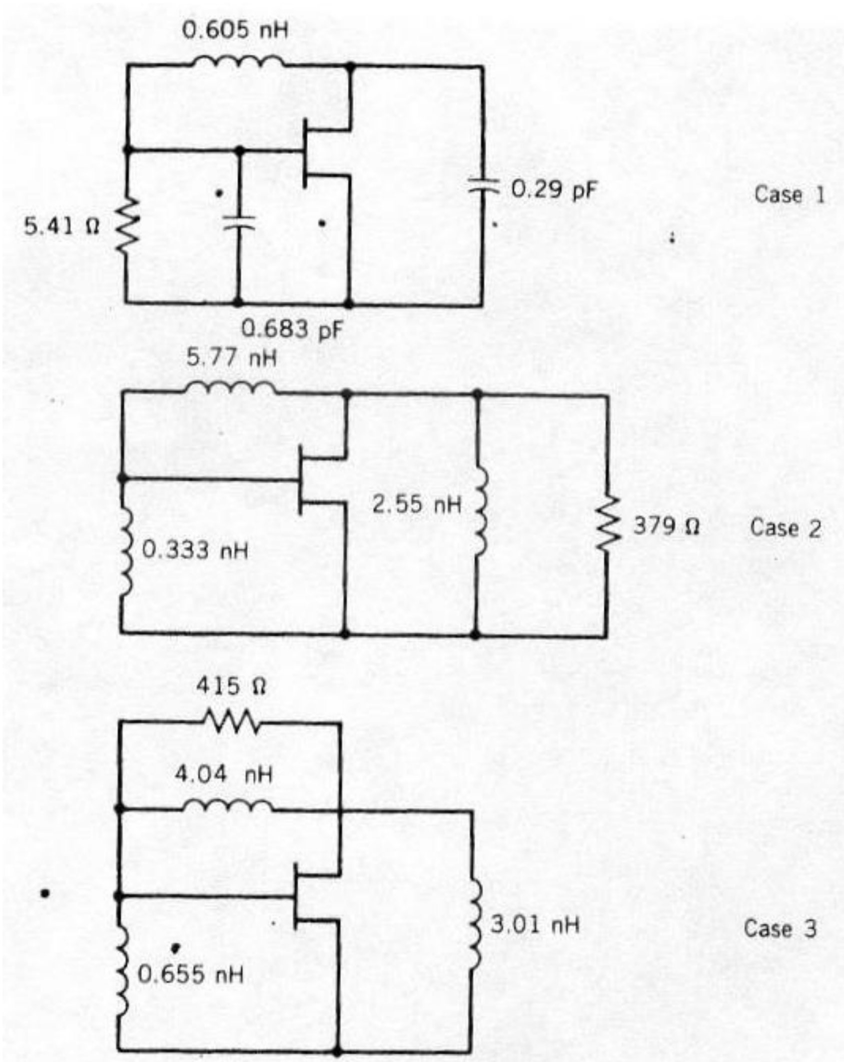
$$D_4 = -\mathrm{Im}\ (Z_{21} + F Z_{22})$$

$$F = F_r + jF_i = (Z_{21} - A Z_{11})/(A Z_{12} - Z_{22})$$

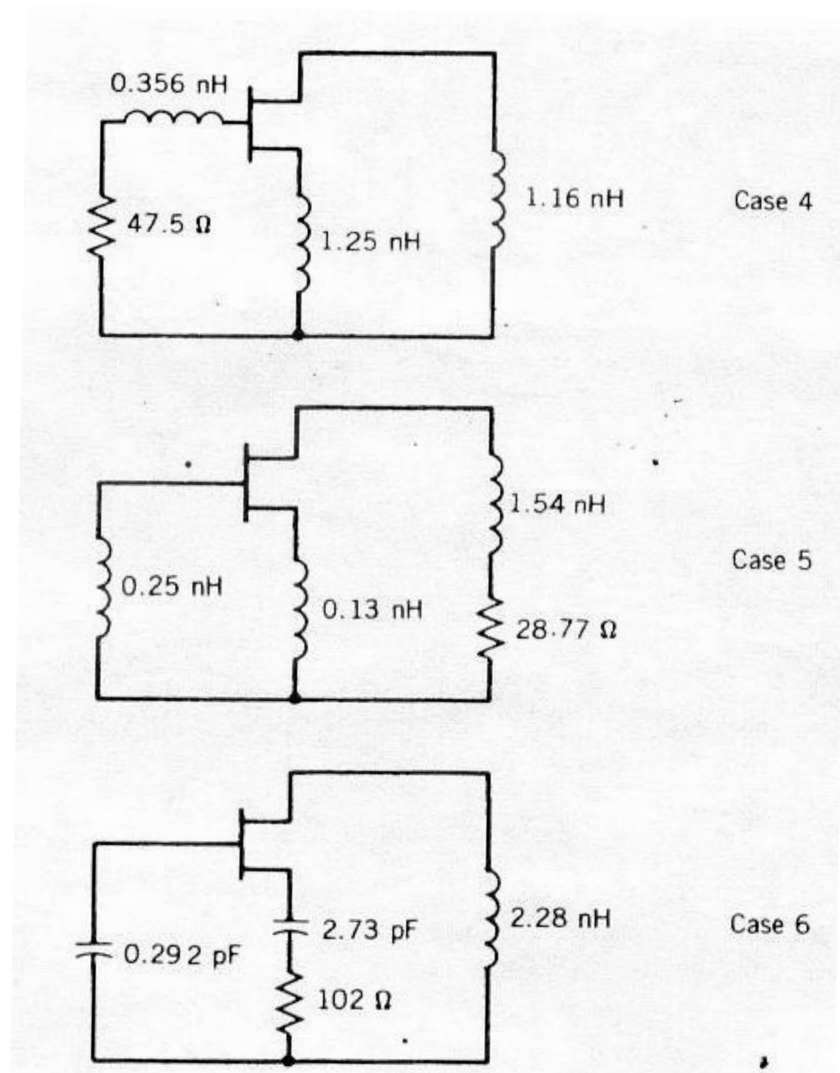
An example of this calculation for a 500 µm DXL-3501A GaAs MESFET is given at 10 GHz

$S_{11} = 0.66\ \angle -143^{o}$ $S_{21} = 1.26\ \angle +46^{o}$

$S_{12} = 0.071\ \angle +117^{o}$ $S_{22} = 0.74\ \angle -59^{o}$



(a)



(b)

Which one is the most suitable ?

HARMONIC OSCILLATORS

HARMONIC OSCILLATORS

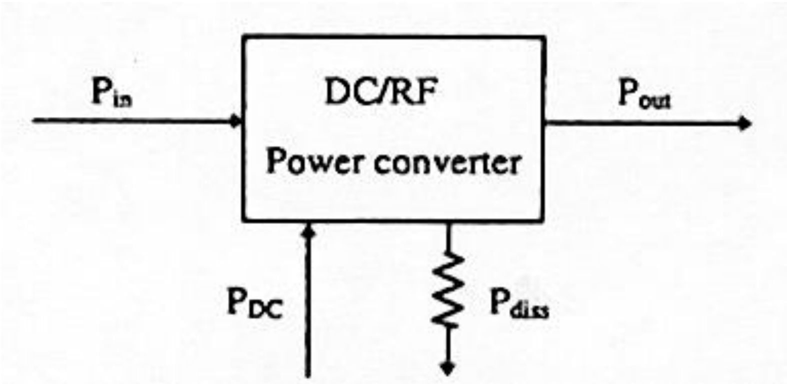
Harmonic oscillators function both as a fundamental frequency oscillator and as a harmonic generator. These components deserve special attention due to their capability of generating RF power above the frequencies usually obtained from fundamental frequency oscillators.

One can start by considering the dynamic balance of power in a microwave amplifier (with *G* the gain and P_{ad} the RF power added by the amplifier) :

$$P_{in} + P_{dc} = P_{out} + P_{diss}$$

$$P_{diss} = P_{dc} - (P_{out} - P_{in}) = P_{dc} - (G-1)P_{in}$$

$$P_{ad} = P_{out} - P_{in}$$



HARMONIC OSCILLATORS

The power balance for the oscillator is also similar to the amplifier case: Conventional oscillator theory states that the maximum available power P_{osc} from an oscillator is equal to the added power from an amplifier at the point of maximum efficiency (i.e., when the difference between P_{out} and P_{in} is maximum).

For a harmonic oscillator, the output power comprises the fundamental frequency power, P_{of}, plus the harmonic power P_{oh}.

$$P_{osc} = P_{out} - P_{in} = P_{dc} - P_{diss}$$

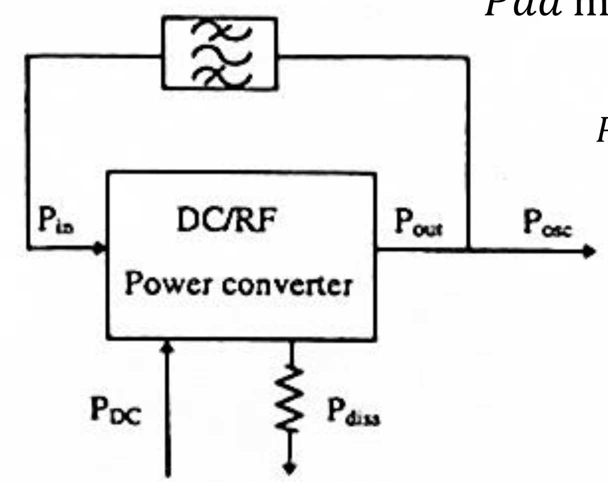
$$P_{in} + P_{dc} = P_{out} + P_{diss}$$

$$P_{hosc} = \left(P_{of} - P_{in}\right) + P_{oh} = (P_{oh} - P_{in}) + P_{of}$$

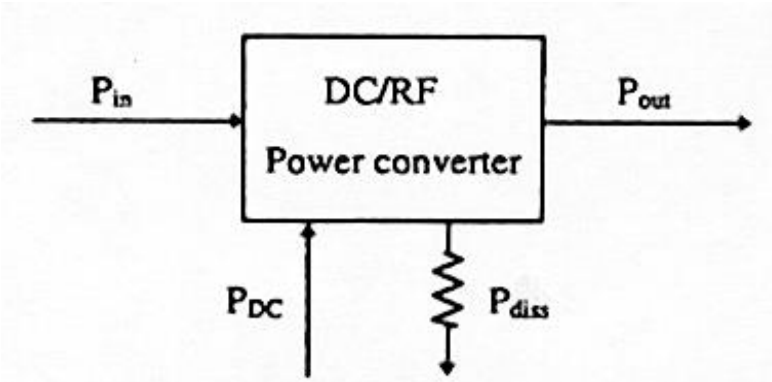
$$P_{diss} = P_{dc} - (P_{out} - P_{in}) = P_{dc} - (G-1)P_{in}$$

$$Pad \max(P_{out} - P_{in})_{osc\max}$$

$$P_{ad} = P_{out} - P_{in}$$



$$P \max(P_{oh} - P_{in})_{of\,hosc\max}$$



HARMONIC OSCILLATORS - DESIGN APPROACH

The design of harmonic oscillators starts with the design of a frequency multiplier

" The harmonic amplifier "

The objectives of a frequency multiplier are a maximum output power at the desired harmonic, a matched input for maximum efficiency, and a reasonable frequency bandwidth.

For harmonic oscillation operation, the multiplier's saturation characteristics are also required:

$$P_{oh}(P_{in}, n\omega_o) - P_{in}(\omega_o) = f[P_{in}(\omega_o)]$$

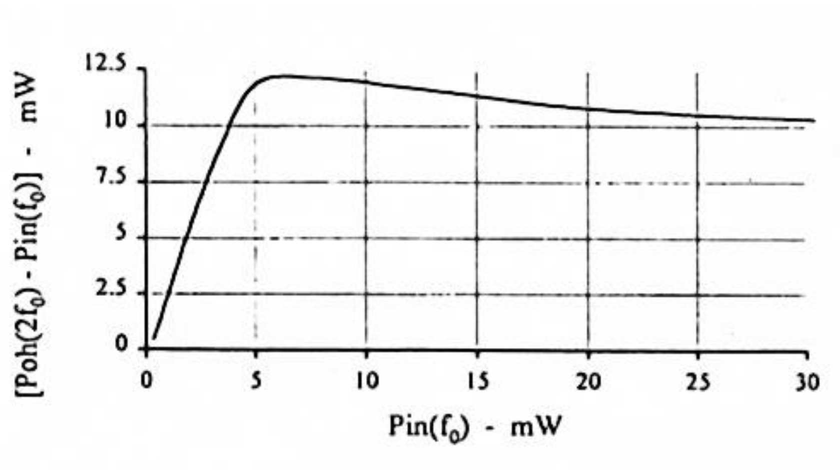
HARMONIC OSCILLATORS - DESIGN APPROACH

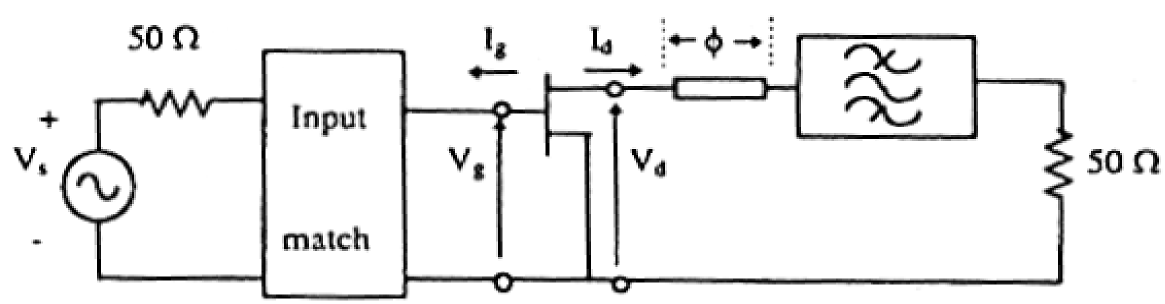
As illustration of such characteristics, let us consider a 5-10 GHz frequency doubler.

One can observe a nonlinear relation between input and output powers at low levels, and a saturation of the second harmonic output power after a certain input drive level.

The added power is maximized at the peak of the curve obtained for

- A matched input that maximize the gate voltage swing, a shorted load,
- A shorted load for the fundamental frequency maximizing the drain current,
- A matched second harmonic drain impedance.





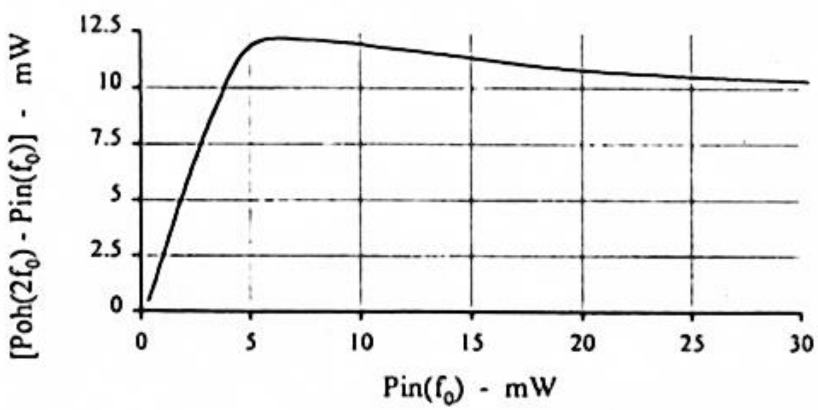
HARMONIC OSCILLATORS - DESIGN APPROACH : 5-10 GHz frequency doubler

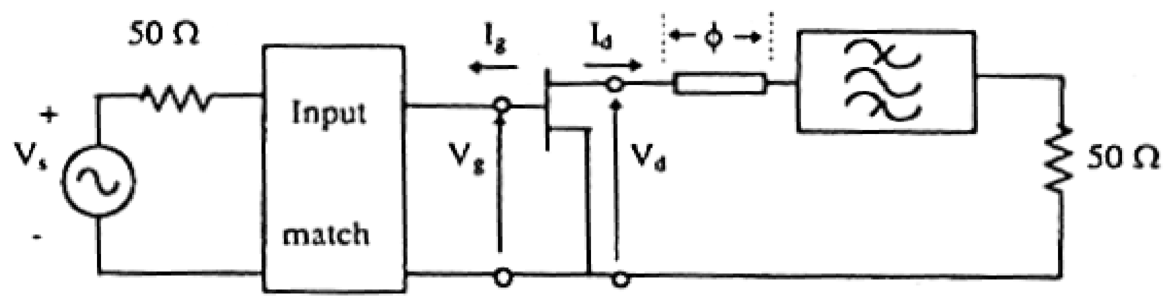
Network elements for the T topology:

Fundamental Frequency Impedances	Output Harmonic Frequency Impedances
$Z_D(\omega_o) = R_{D1} + jX_{D1}$	$Z_D(n\omega_o) = R_{Dn} + jX_{Dn}$
$Z_S(\omega_o) = jX_{S1}$	$Z_S(n\omega_o) = 0$
$Z_G(\omega_o) = jX_{G1}$	$Z_G(n\omega_o) = R_{Gn} + jX_{Gn}$

Case	Z_G	Z_S	Z_D
$Re\{Z_G\} = Re\{Z_S\} = 0$	$\frac{jRe\{V_G(I_G^* + I_D^*)\}}{Im\{I_G^* I_D\}}$	$\frac{jRe\{V_G I_G^*\}}{Im\{I_G I_D^*\}}$	$\frac{V_D}{I_D} - Z_s\left[1 + \frac{I_G}{I_D}\right]$
$Re\{Z_G\} = Re\{Z_D\} = 0$	$\frac{jRe\{I_D(V_D^* - V_G^*)\}}{Im\{I_G I_D^*\}}$	$\frac{V_G - Z_G I_G}{I_G + I_D}$	$\frac{jRe\{I_G(V_G^* - V_D^*)\}}{Im\{I_G I_D^*\}}$
$Re\{Z_D\} = Re\{Z_S\} = 0$	$\frac{V_G}{I_G} - Z_s\left[1 + \frac{I_D}{I_G}\right]$	$\frac{jRe\{V_D I_D^*\}}{Im\{I_G^* I_D\}}$	$\frac{jRe\{V_D(I_D^* + I_G^*)\}}{Im\{I_G I_D^*\}}$

T configuration: Network elements as a function of terminal current-voltage at the fundamental frequency.





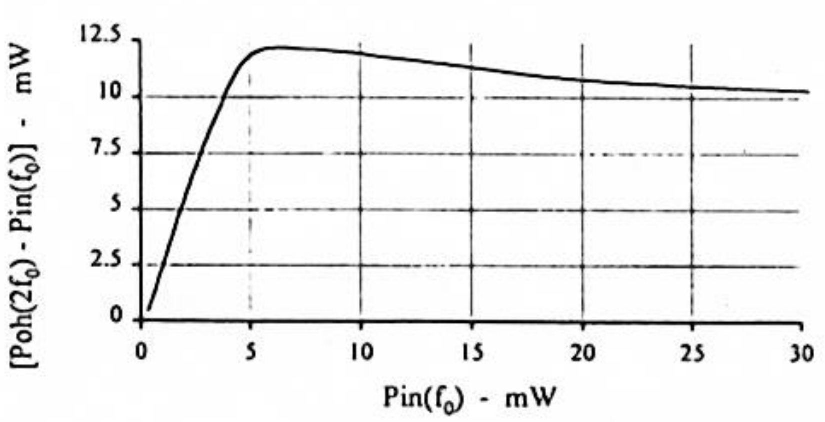
HARMONIC OSCILLATORS - DESIGN APPROACH : 5-10 GHz frequency doubler

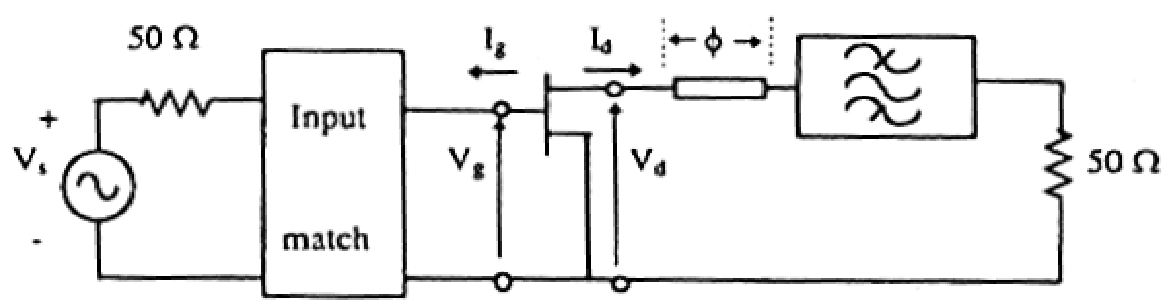
Network elements for the π topology:

Fundamental Frequency Admittance	Output Harmonic Frequency Admittance
$Y_{DS}(\omega_0) = G_{DS1} + jB_{DS1}$	$Y_{DS}(n\omega_0) = G_{DSn} + jB_{DSn}$
$Y_{GS}(\omega_0) = jB_{GS1}$	$Y_{GS}(n\omega_0) = G_{GSn} + jB_{GSn}$
$Y_{DG}(\omega_0) = jB_{DG1}$	$Y_{DG}(n\omega_0) = 0$

Case	Y_{GS}	Y_{GD}	Y_{DS}
$Re\{Y_{GS}\} = Re\{Y_{GD}\} = 0$	$\frac{jRe\{I_G(V_D^* - V_G^*)\}}{Im\{V_D V_G^*\}}$	$\frac{jRe\{V_G^* I_G\}}{Im\{V_G^* V_D\}}$	$\frac{I_D}{V_D} + Y_{GD}\left[\frac{V_G}{V_D - 1}\right]$
$Re\{Y_{GS}\} = Re\{Y_{DS}\} = 0$	$\frac{jRe\{V_D(I_D^* + I_G^*)\}}{Im\{V_D V_G^*\}}$	$\frac{Y_{GS}V_G - I_G}{V_D - V_G}$	$\frac{jRe\{V_G(I_G^* + I_D^*)\}}{Im\{V_D^* V_G\}}$
$Re\{Y_{GS}\} = Re\{Y_{DS}\} = 0$	$\frac{I_G}{V_G} - Y_{GD}\left[\frac{V_D}{V_G} - 1\right]$	$\frac{jRe\{V_D^* I_D\}}{Im\{V_D^* V_G\}}$	$\frac{jRe\{I_D(V_G^* - V_D^*)\}}{Im\{V_D^* V_G\}}$

π configuration: Network elements as a function of terminal current-voltage at the fundamental frequency.





Fundamental Frequency Admittance	Output Harmonic Frequency Admittance
$Y_{DS}(\omega_0) = G_{DS1} + jB_{DS1}$	$Y_{DS}(n\omega_0) = G_{DSn} + jB_{DSn}$
$Y_{GS}(\omega_0) = jB_{GS1}$	$Y_{GS}(n\omega_0) = G_{GSn} + jB_{GSn}$
$Y_{DG}(\omega_0) = jB_{DG1}$	$Y_{DG}(n\omega_0) = 0$

Note: Although both topologies are possible**, the T configuration is more adequate to harmonic oscillators**, due to the difficulty of building a circuit where the feedback element Y_{DG}, is an open circuit at the output harmonic.

Fundamental Frequency Impedances	Output Harmonic Frequency Impedances
$Z_D(\omega_o) = R_{D1} + jX_{D1}$	$Z_D(n\omega_o) = R_{Dn} + jX_{Dn}$
$Z_S(\omega_o) = jX_{S1}$	$Z_S(n\omega_o) = 0$
$Z_G(\omega_o) = jX_{G1}$	$Z_G(n\omega_o) = R_{Gn} + jX_{Gn}$

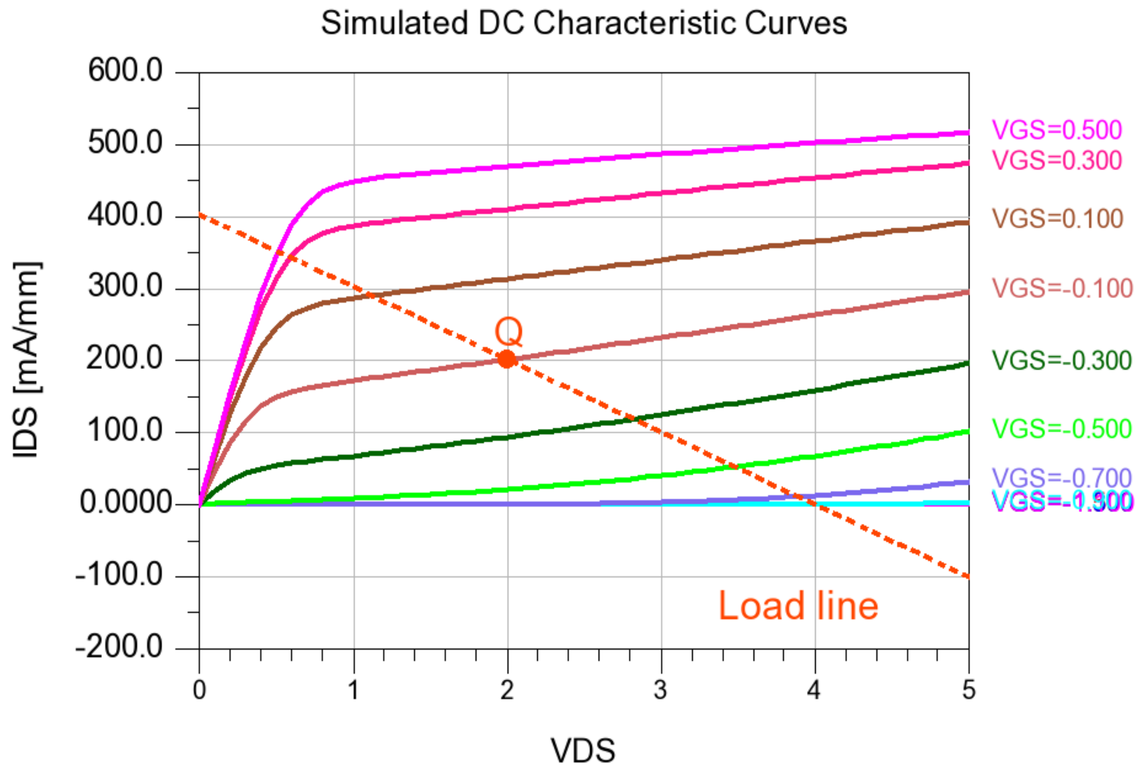
FIRST DESIGN: SINGLE FREQUENCY OSCILLATOR

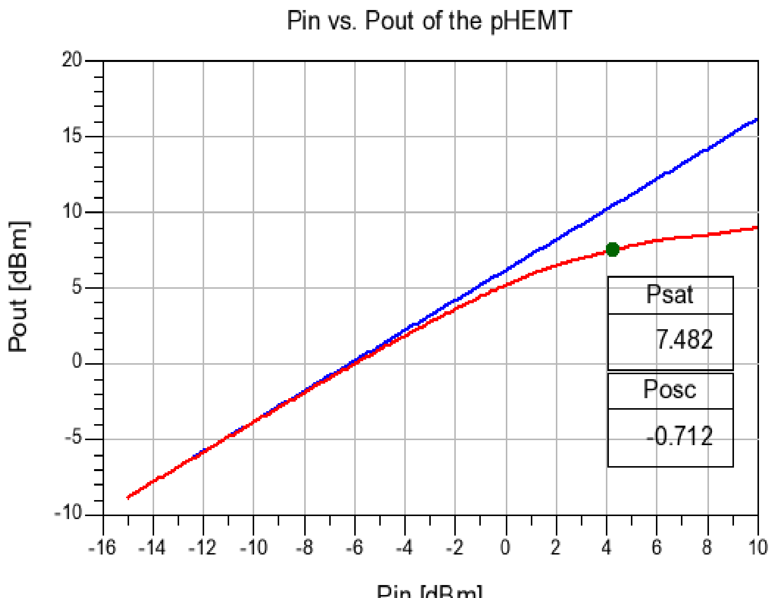
(35 GHz oscillator for radiolocation applications)

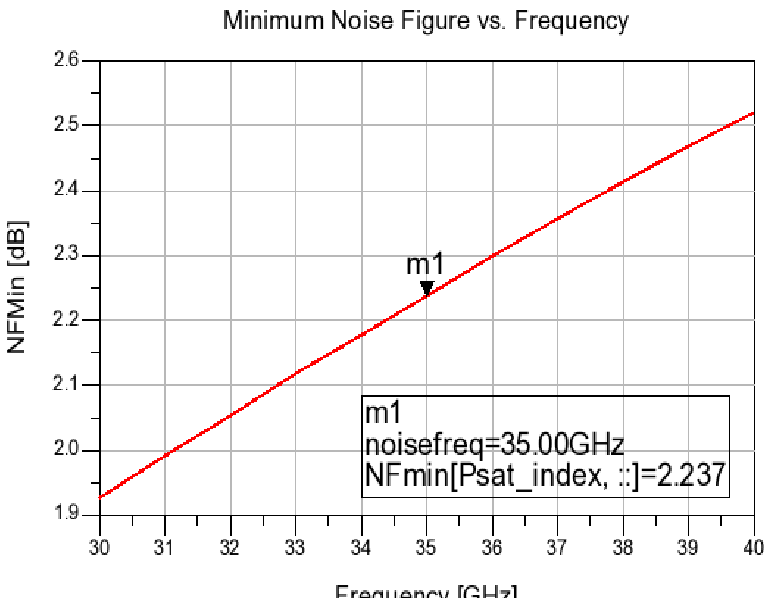
Design Requirements

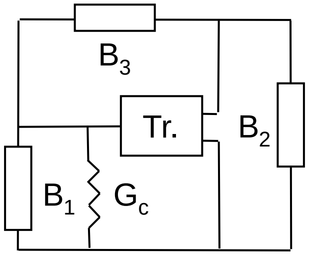
Parameter	Units	Specs
Frequency	GHz	35
Output Power	dBm	> 6.0
Phase Noise	dBc/Hz (@1MHz offset)	> 110
DC Power Consumption	W	< 50 mW
DC-to-RF Efficiency	%	> 10

0.15μm pHEMT device



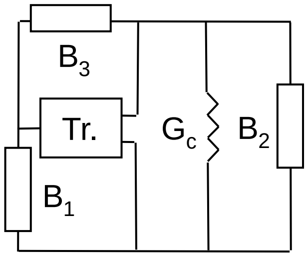






Component values to implement a shunt oscillator

Y_{11} [mΩ]	Y_{12} [mΩ]	Y_{21} [mΩ]	Y_{22} [mΩ]
1.09 + j 28.55	0.225 – j 5.05	41.8 – j 23.2	6.67 + j 21.9

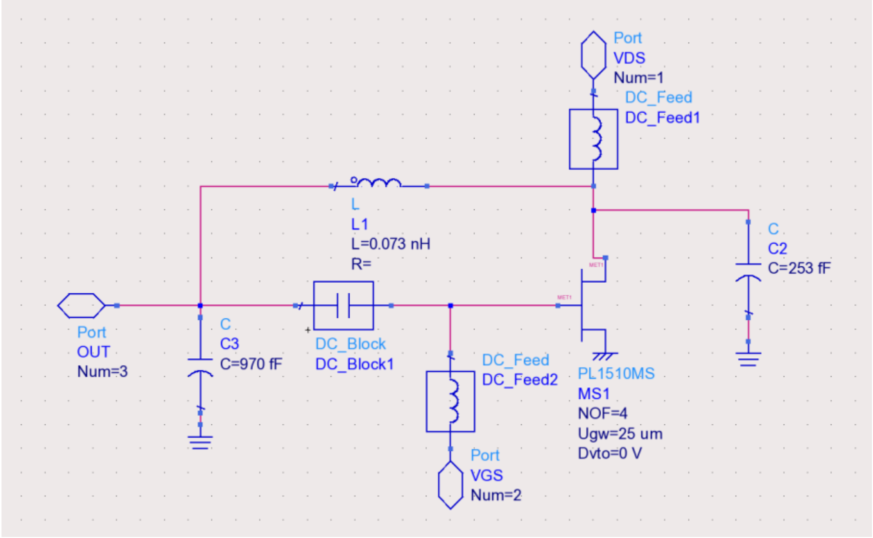


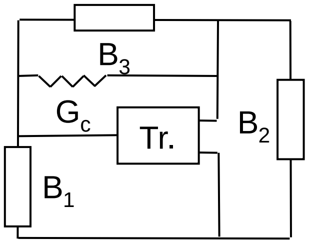
We selected the first :

Why?

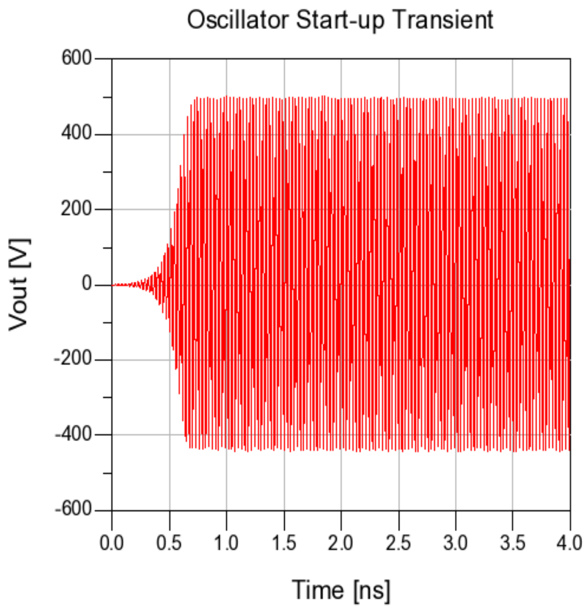
Extracted large-signal

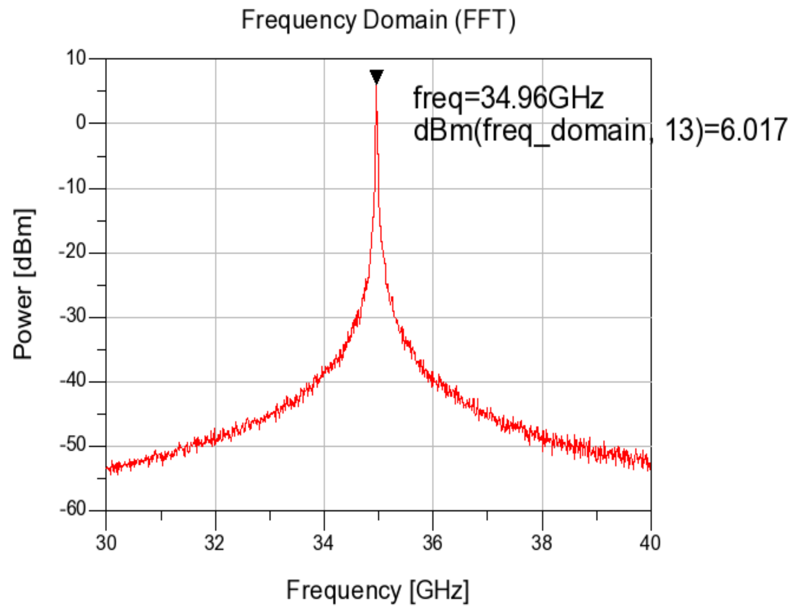
Y-parameters

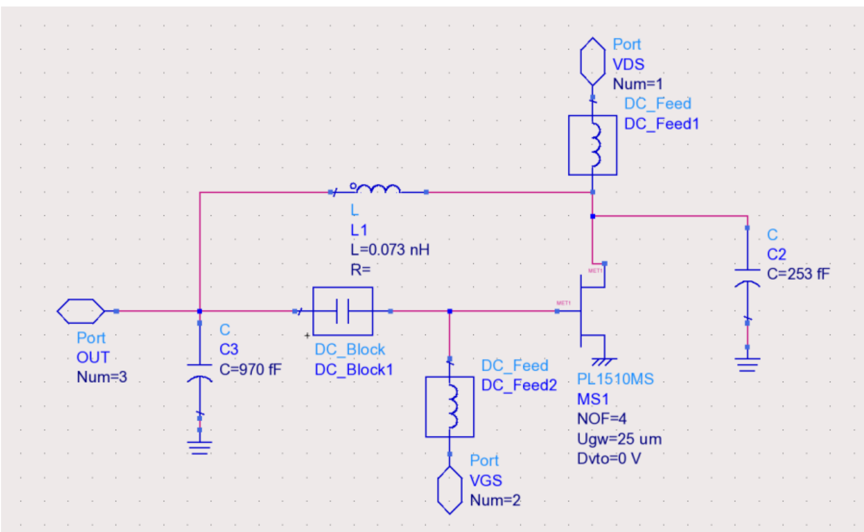


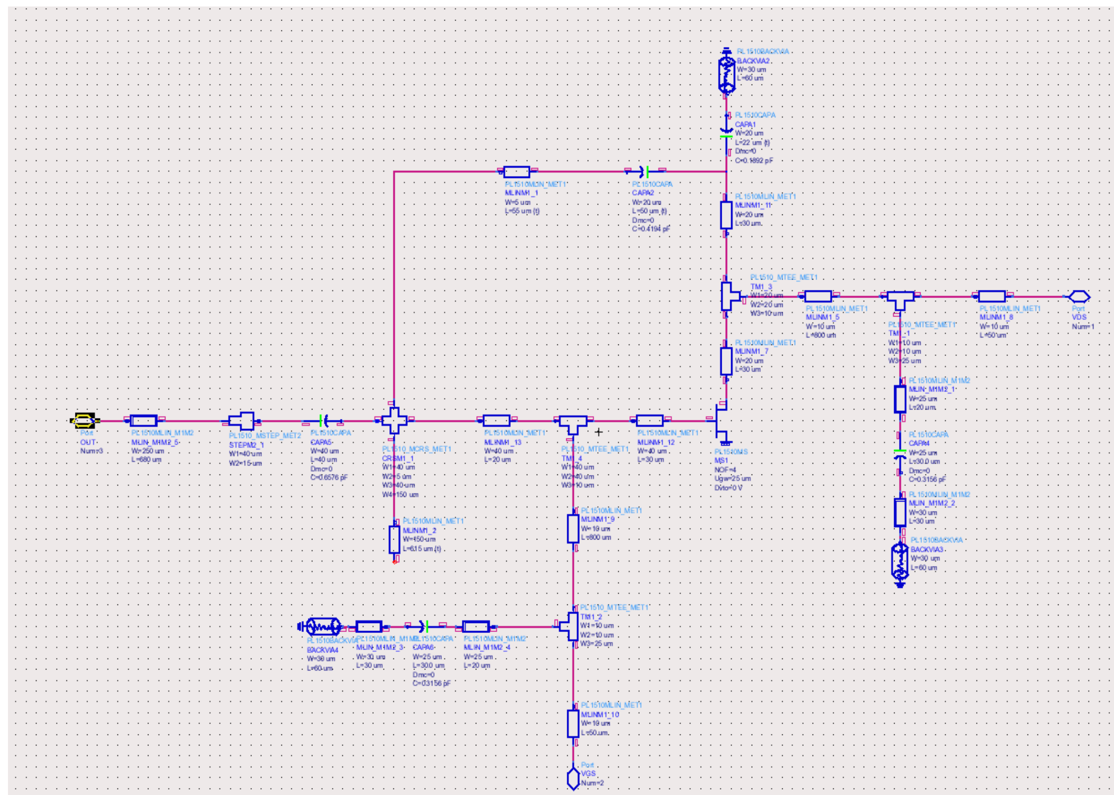


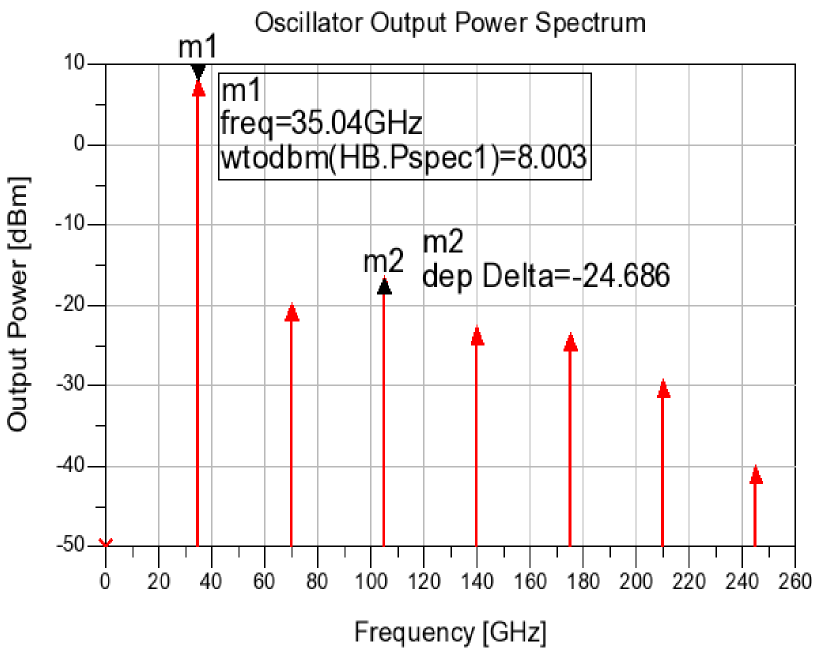
G_L connected between:	B_1		B_2		B_3		G_L
	C [fF]	L [µH]	C [fF]	L [µH]	C [fF]	L [pH]	
Gate & Source	971		253			73	12.9
Drain & Source		200		275		852	152
Gate & Drain	156			3480		256	246

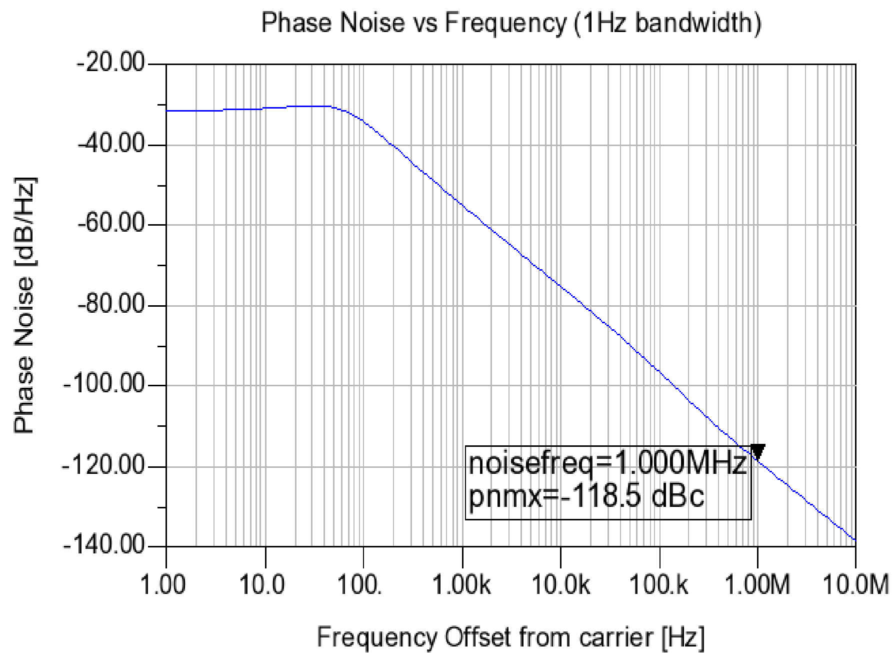

Oscillator Start-up Transient
600
400
200
0
-200
-400
-600
Vout [V]
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0
Time [ns]


Frequency Domain (FFT)
freq=34.96GHz
dBm(freq_domain, 13)=6.017
10
0
-10
-20
-30
-40
-50
-60
Power [dBm]
30 32 34 36 38 40
Frequency [GHz]


Port
VDS
Num=1
DC_Feed
DC_Feed1
L
L1
L=0.073 nH
R=
C
C2
C=253 fF
Port
OUT
Num=3
C
C3
C=970 fF
DC_Block
DC_Block1
DC_Feed
DC_Feed2
PL1510MS
MS1
NOF=4
Ugw=25 um
Dvto=0 V
Port
VGS
Num=2







DC Power Consumption

P_DC	efficiency	P_RF
0.040	0.158	0.006

Note : phase noise is in dBc/Hz = phase noise density with a BW of 1Hz

- dBc : decibels relative to carrier, a common measurement in RF engineering to specify the power of a sideband in a modulated signal relative to the carrier.
- Since noise has infinite BW, wider the application bandwidth, higher the noise. Therefore, the industry has settled on a bandwidth of 1Hz as a standard – this is considered as the normalized bandwidth

Comparison of simulated and specified values for the designed oscillator

Parameter	Units	Specs	Simulated
Frequency	GHz	35	35.04
Output Power	dBm	> 6.0	8.0
Phase Noise	dBc/Hz (@1MHz offset)	> 110	-118
DC Power Consumption	W	< 50 mW	40mW
DC-to-RF Efficiency	%	> 10	15.8

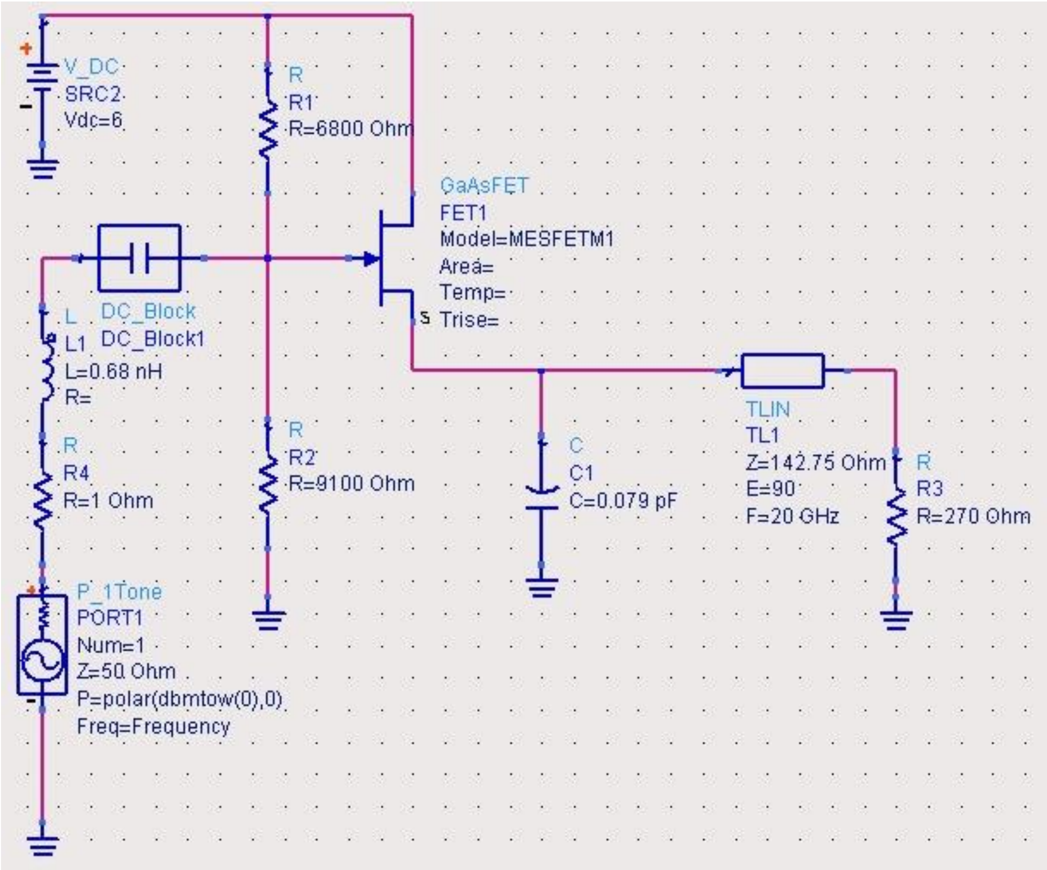
SECOND DESIGN: SINGLE FREQUENCY OSCILLATOR

(20 GHz OSCILLATOR FOR TEST & MEASUREMENT EQUIPMENT)

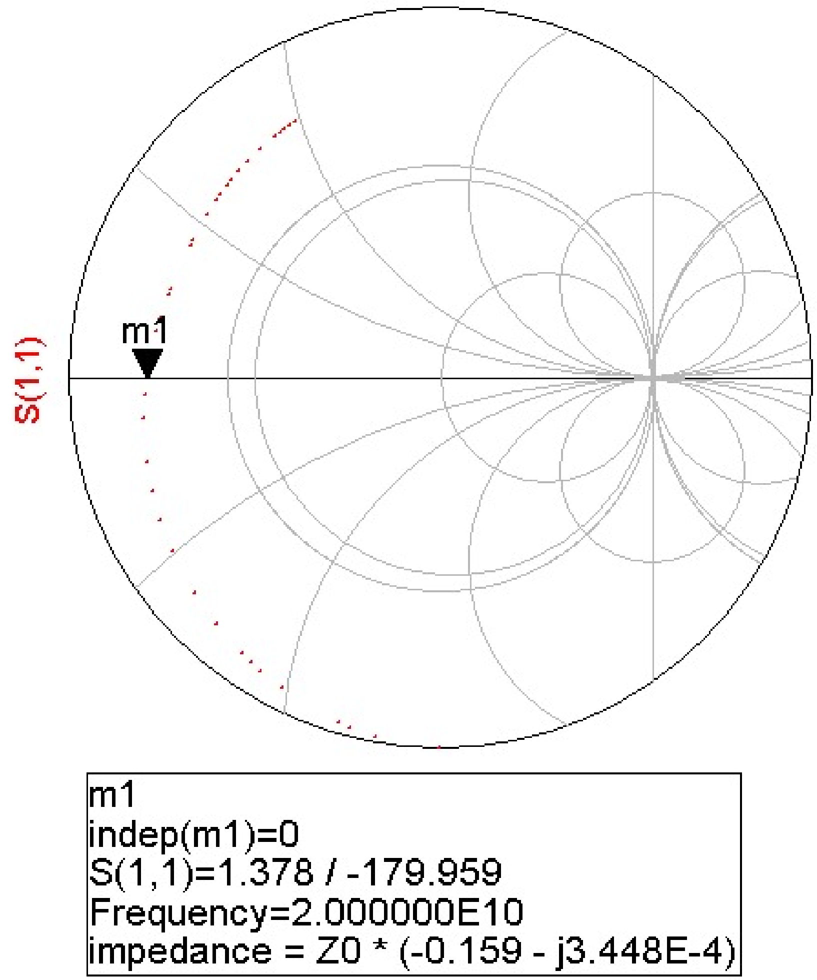
Design Requirements

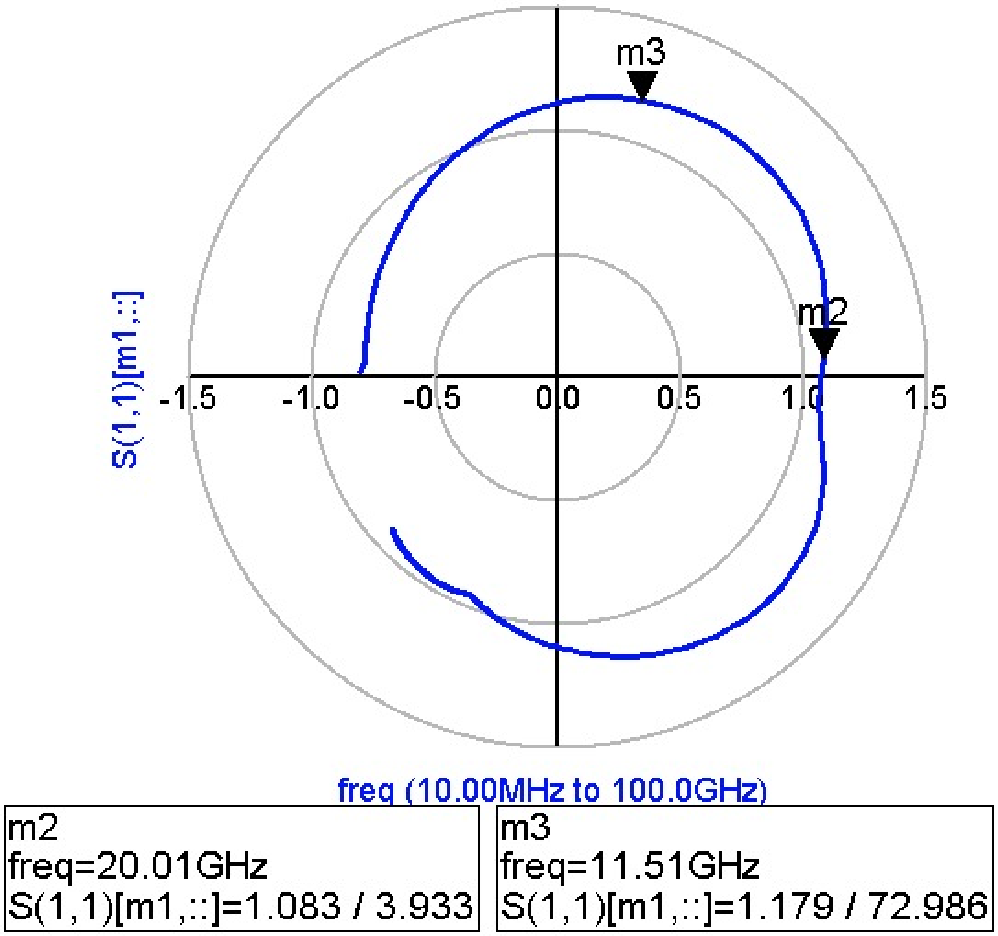
Output Frequency	**20 GHz**
Output Power	**> 10 dB**
Phase Noise	**> 150 dBc/Hz**

- Selected the common drain configuration since it was more likely to be unstable than common source.
- Also simpler to design



- After canceling the device capacitive impedance with an inductor and capacitor in the resonator, we should have oscillations.

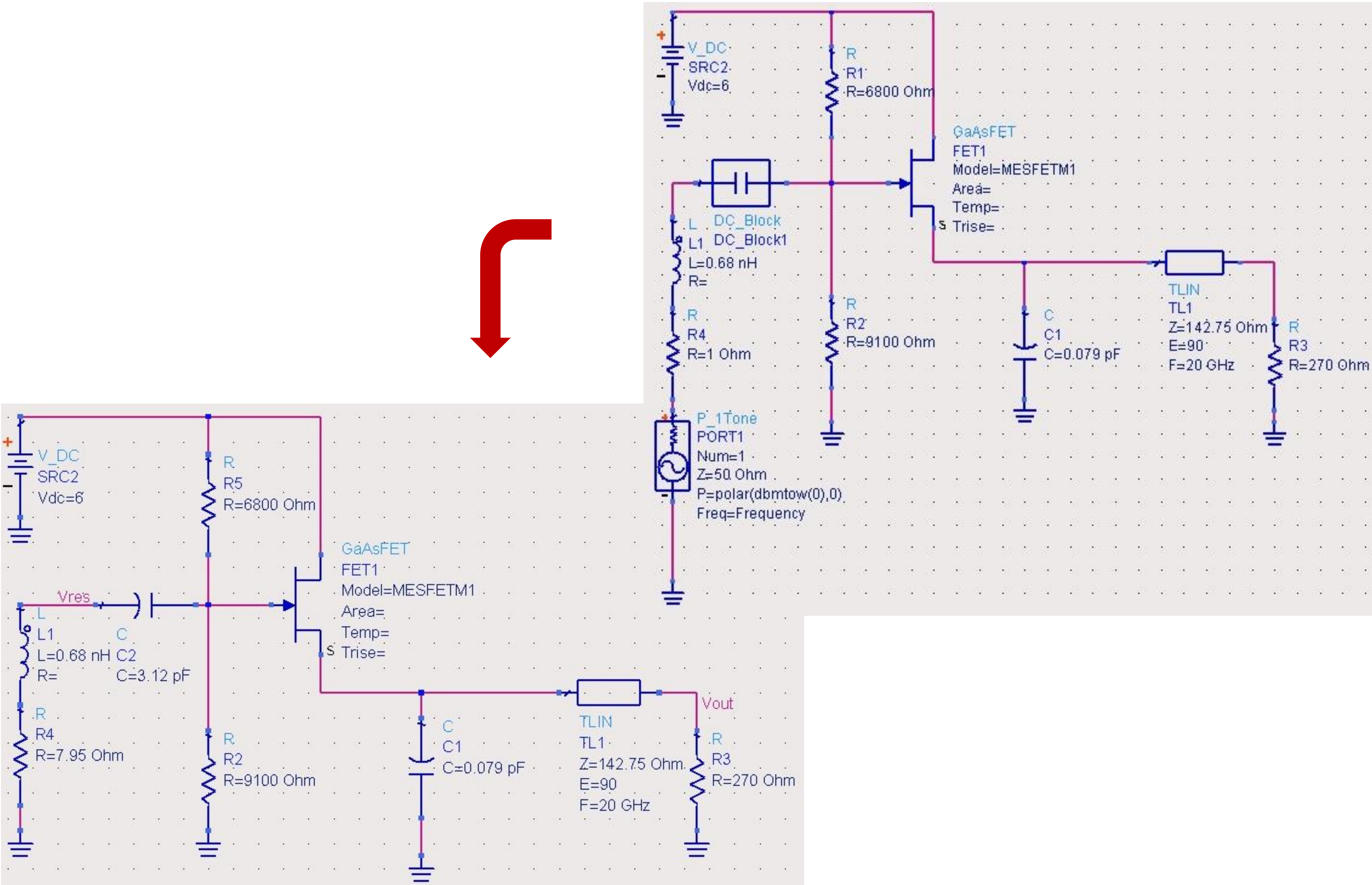




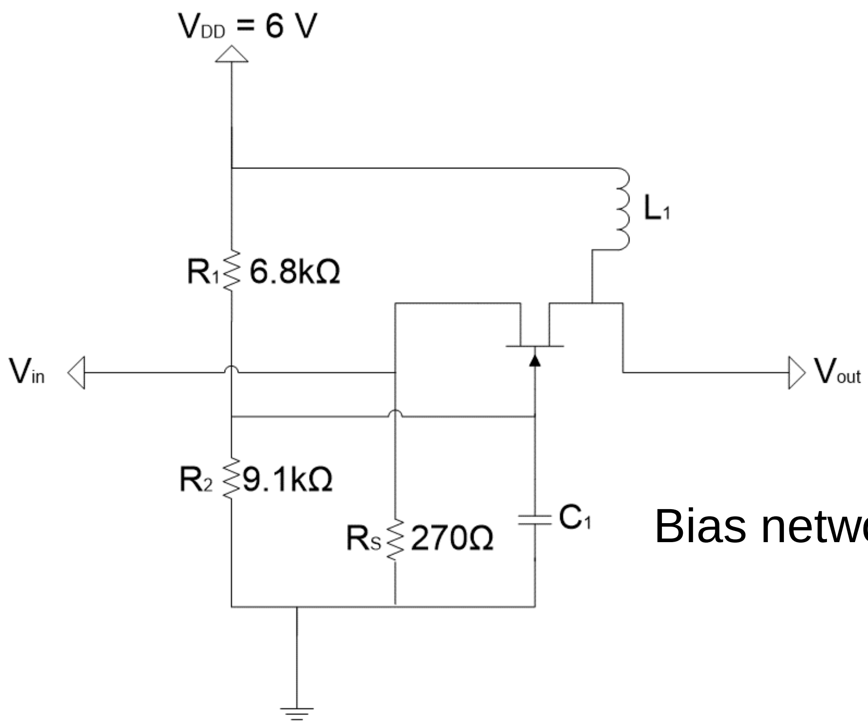
Nyquist Plot

ANALYSIS BY THE TRANSISTOR S-PARAMETERS

(FROM AMPLIFIER TO OSCILLATOR)



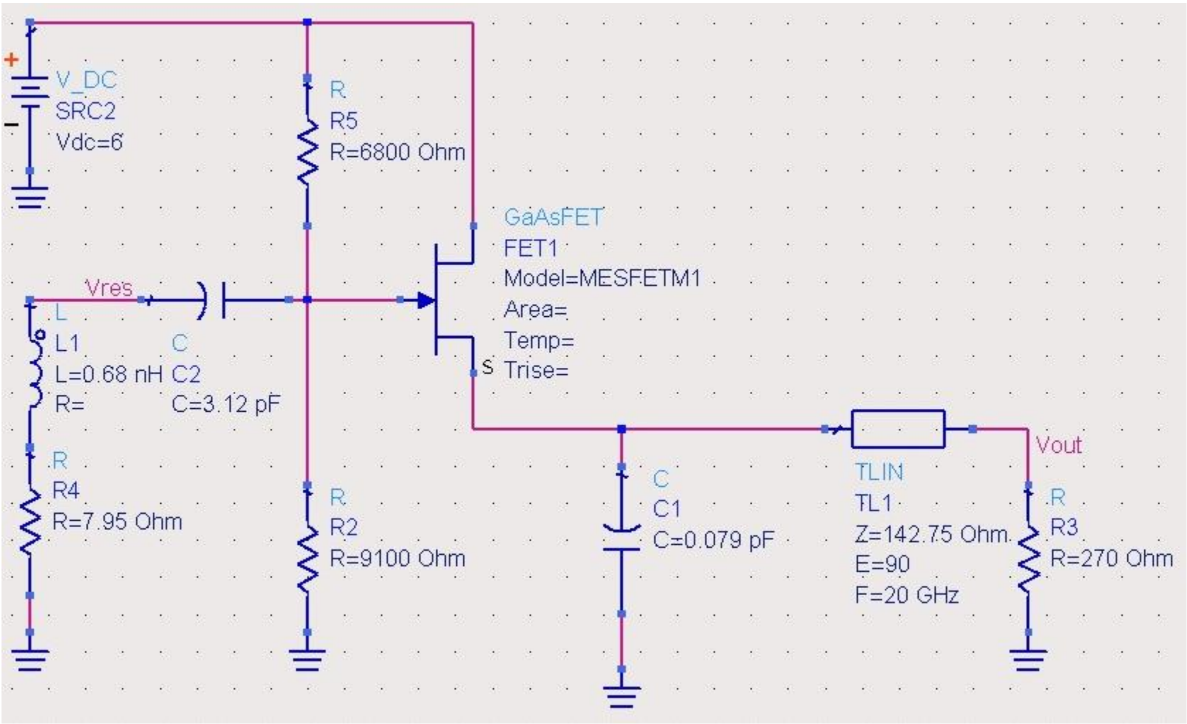
Found the maximized negative input resistance by altering values of L_G and C_D (1 nH, 0.05 pF)



Bias network

PROBLEM 1:

The gate inductor L_G effectively shorts out the DC bias at the gate!!



Attempted various solutions:

$\lambda/4$ transformer

$\lambda/4$ transformer with single stub matching

Inductive shorted transmission line coupled with capacitor

Both solutions proved unreliable as they were prone to drive the oscillator into stability.

(influenced both gain and phase)

→ Reverted to LC planar elements instead.

PROBLEM 2:

The negative resistance values are too close, thereby increasing the likely hood of stability later on !

Power Level	Normalized Impedance
-20 dBm	-1.599 – j2.240
+20 dBm	-1.601 – j2.216

Solution:

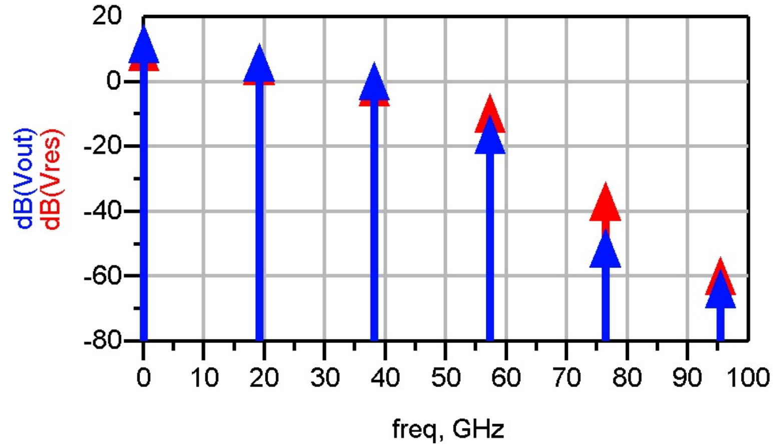
Drive the transistor into mild saturation ≈ 5 dBm

But this will increase phase noise and distort the output !

PROBLEM 2:

The negative resistance values are too close, thereby increasing the likely hood of stability later on !

Power Level	Normalized Impedance
-20 dBm	-1.599 – j2.240
+20 dBm	-1.601 – j2.216



Solution:

Add a filter

THIRD DESIGN: VOLTAGE CONTROLLED OSCILLATOR (VCO)

Design Requirements

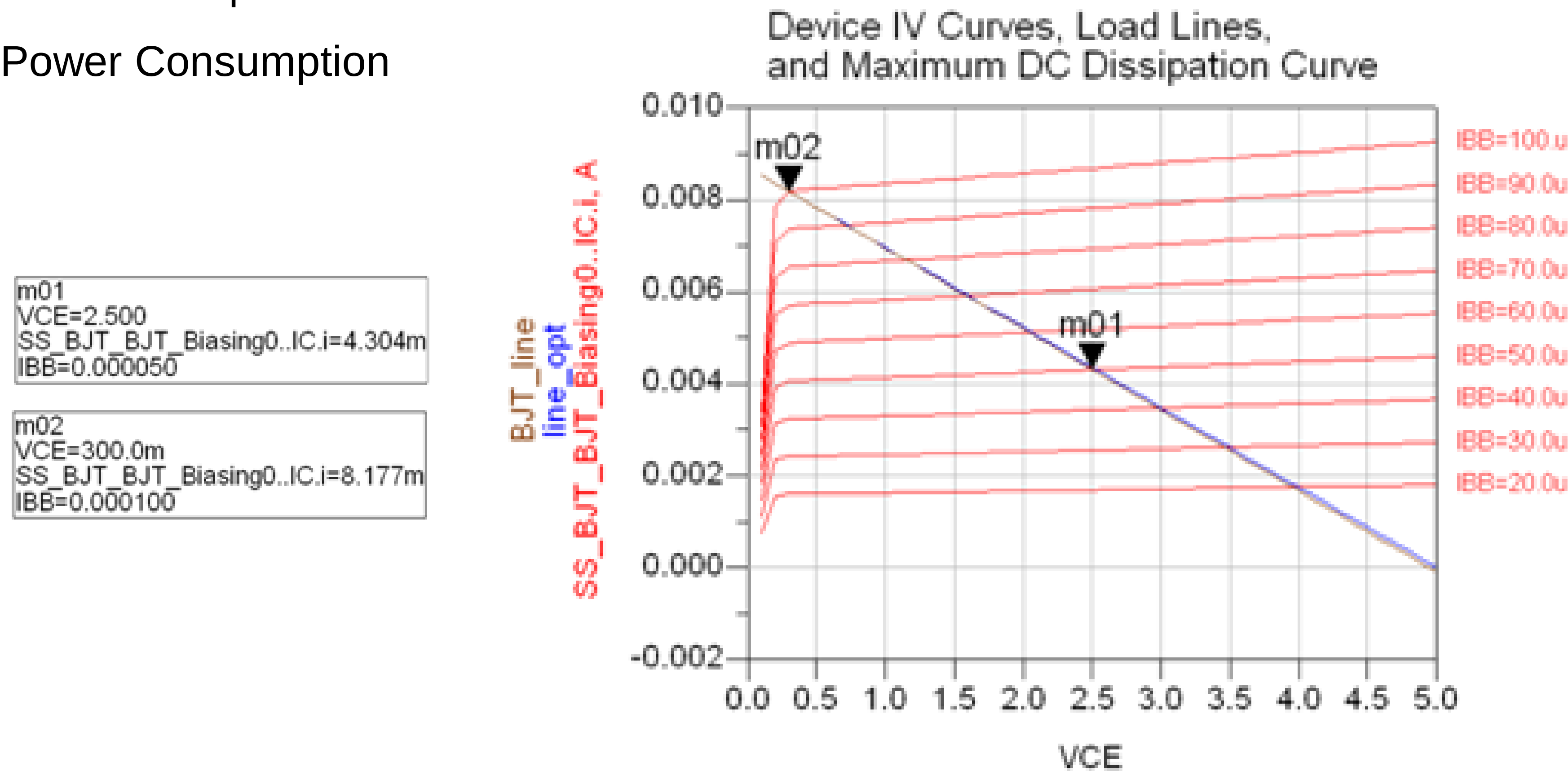
Output Frequency	**0.92 GHz**
Output Power	**- 6 dB**
Phase Noise	**- 60 dBc/10 Hz**

Voltage controlled oscillator (VCO)

A voltage controlled oscillator or VCO is a circuit element that adjusts its oscillation frequency in response to an input DC voltage (it usually uses a varactor to tune a capacitor value which, in turn, will tune the resonant frequency).

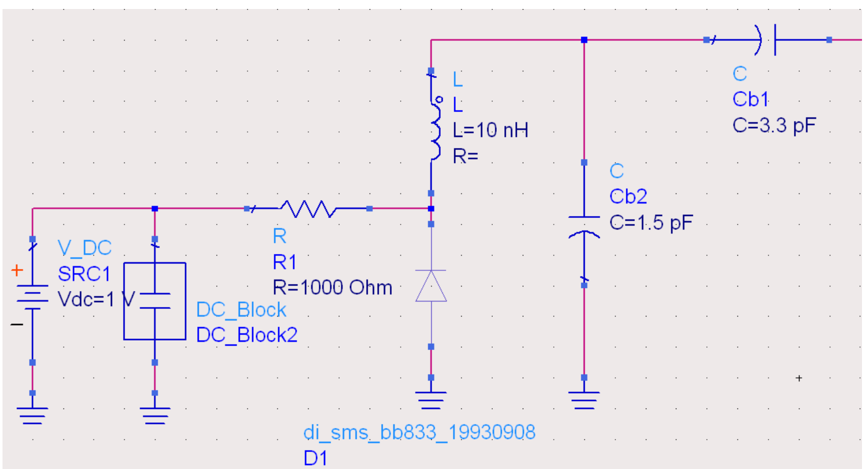
Transistor must operate within power specifications

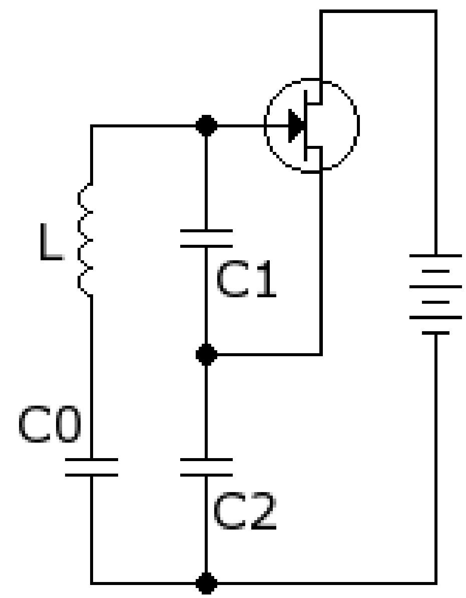
- Low Power Dissipation
- Low Power Consumption



Clapp circuit retained :

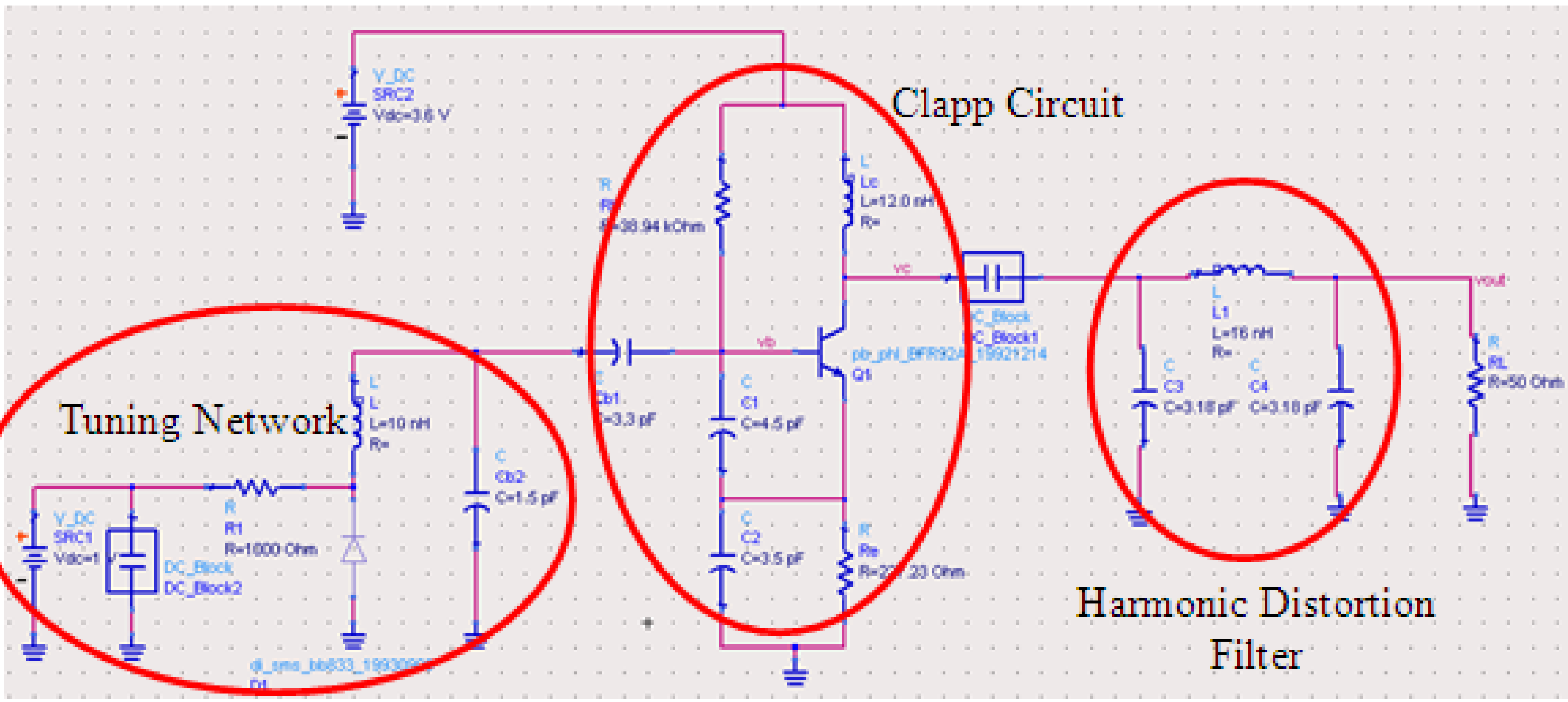
- A resonant circuit allows achieving the required frequency.
  - Here C_0 encompasses Cb1, Cb2, and the varactor diode capacitance
  - Cb2 is used to tune the resonant frequency and helps limit the junction capacitance of the diode.
  - The varactor diode capacitance changes as the voltage is changed. Increased voltage leads to increase in frequency.

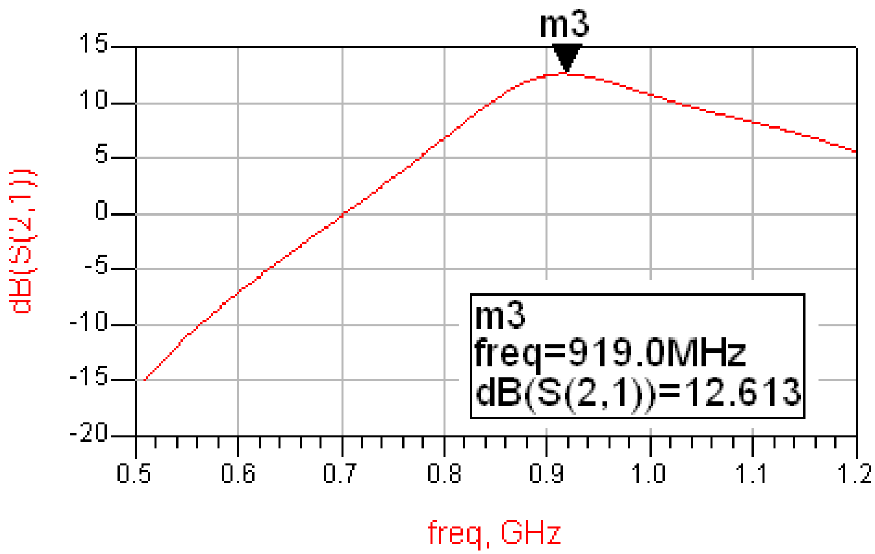




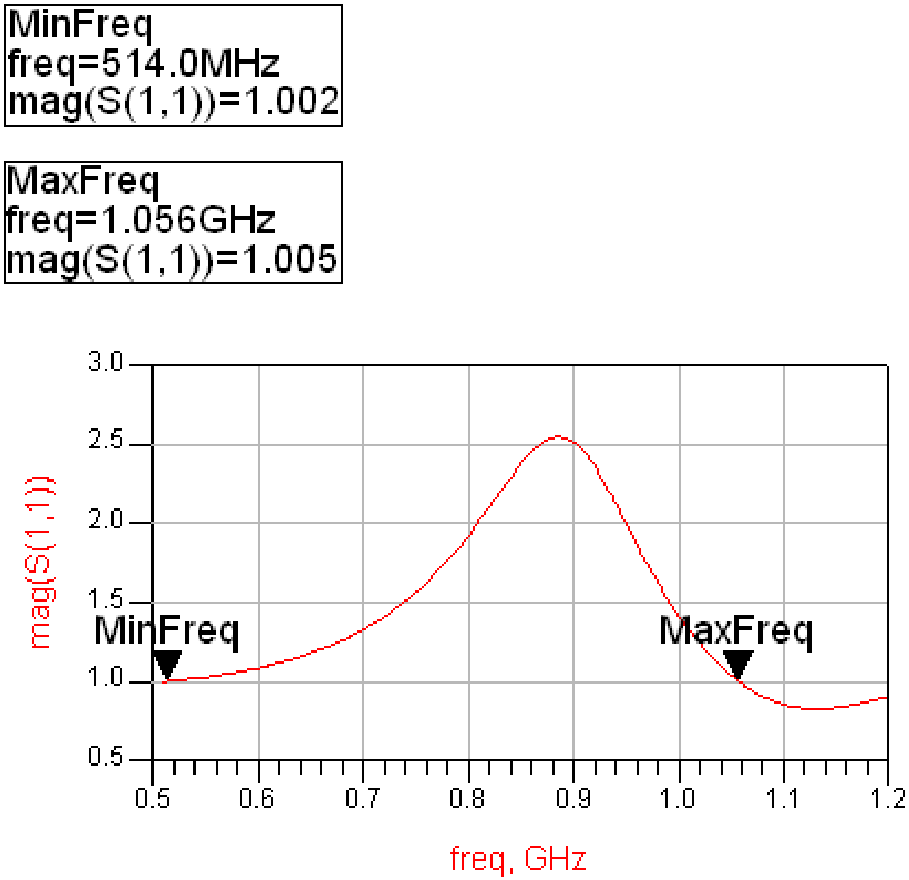
This schematic was used to find the frequency of operation and was used to show the range of frequency values for which this VCO operates. This was achieved by adjusting the voltage across the varactor diode.

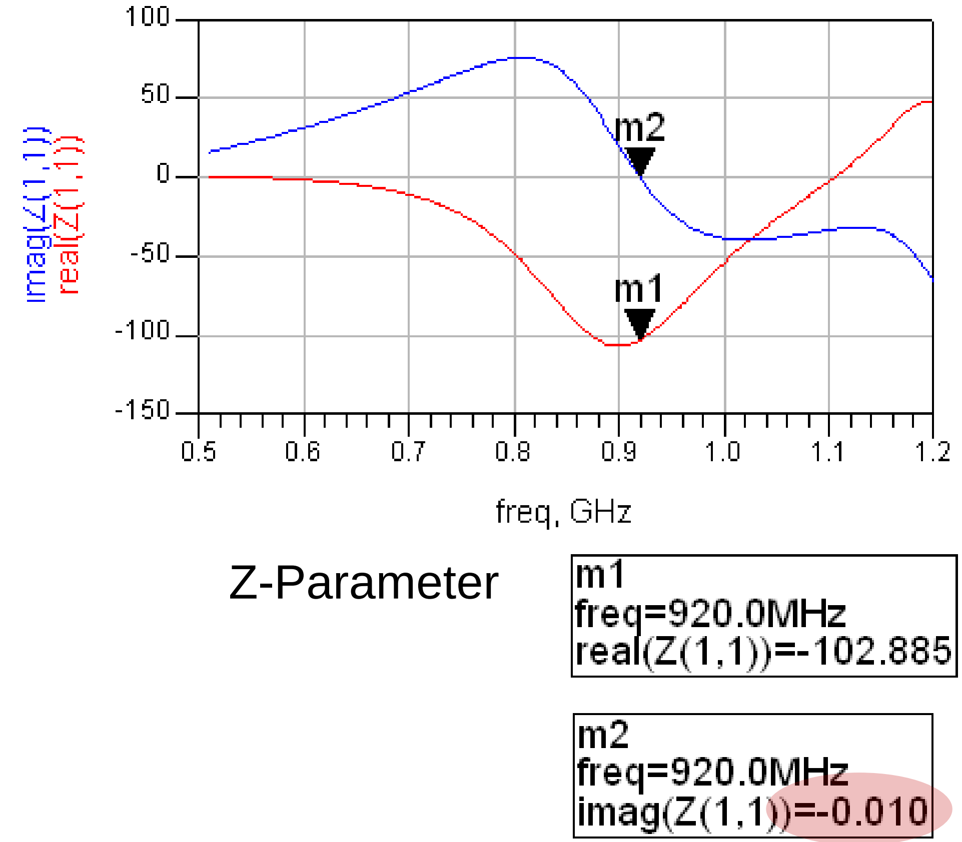
Input is taken at the beginning of the Clapp circuit, not the resonant circuit.





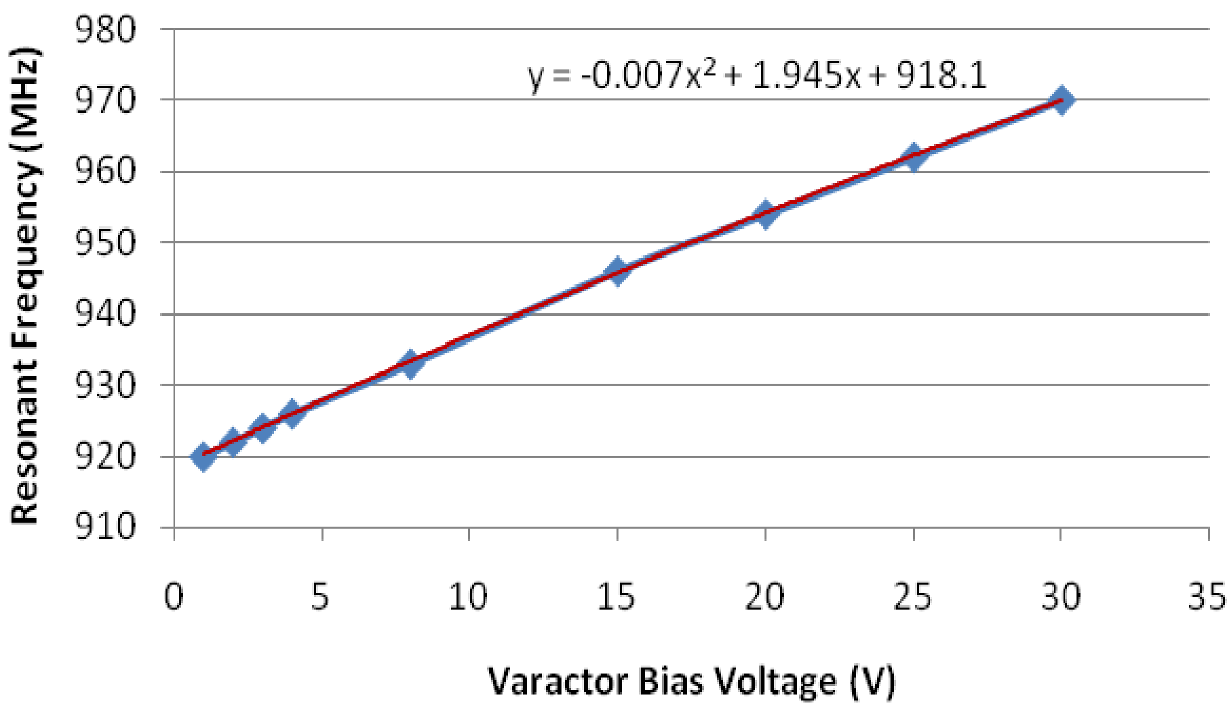
- S_{21} shows the resonant frequency where gain is the highest
- S_{11} shows the "maximum" range of frequency the oscillator could cover (with $S_{11} > 1$)
- Z_{11} shows the resonant frequency (with phase equals to 0)





Z-Parameter

Resonant frequency vs. Varactor bias voltage



$$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{L}\left(\frac{1}{C_0}+\frac{1}{C_1}+\frac{1}{C_2}\right)^{-1}}$$

We added a harmonic filter.

Why?

Harmonic distortion is due to the high alternating voltage in the tuning circuit due to:

- The nonlinearity of the capacitance that may produce harmonics
  - In order to reduce the effects of this, the voltage across the diode should be kept small. A resistor can be placed in series to reduce the voltage.
- The diode nonlinearities
- The varactor diode which does not follow the sine law. Thus, the resonator frequency may change when a sinusoidal voltage is applied to it.
  - Under certain conditions they may even lead to **squegging**, which can cause an oscillator to start and stop at frequencies much lower than the desired frequency

Squegging is a radio engineering term. It is a contraction of **self-quenching**. A squegging or *self-blocking* oscillator produces an intermittent or changing output signal.

Wildlife tags for birds and little mammals use squegging oscillators.

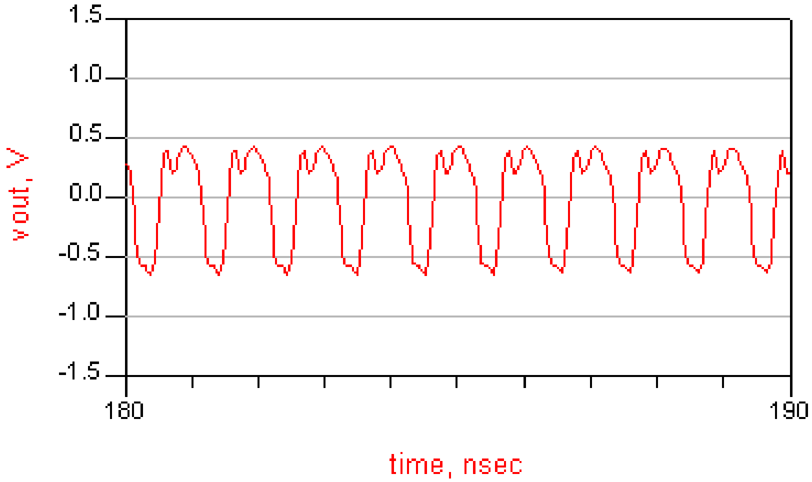
The receiver sensitivity rises while the oscillation builds up. The oscillation stops when the operation point no longer fulfills the Barkhausen stability criterion. The blocking oscillator recovers to the initial state and the cycle starts again.

Squegging is an oscillation that builds up and dies down with a much longer time constant than the fundamental frequency of the oscillation.

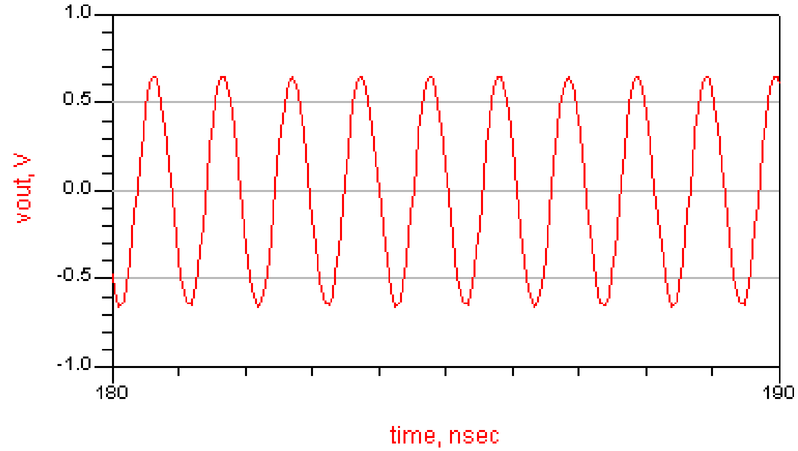
A self-quenching oscillator circuit oscillates at two or more frequencies at the same time.

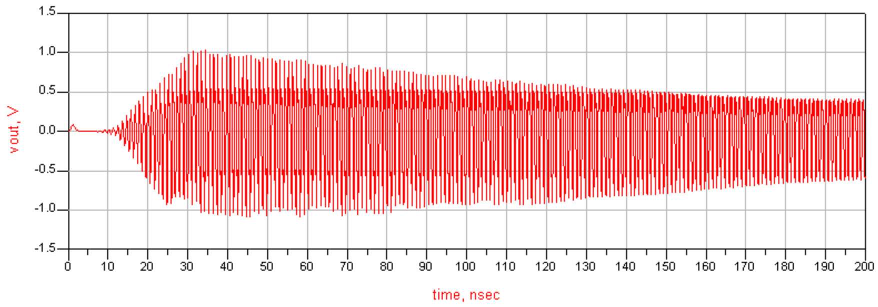
https://en.wikipedia.org/wiki/Squegging

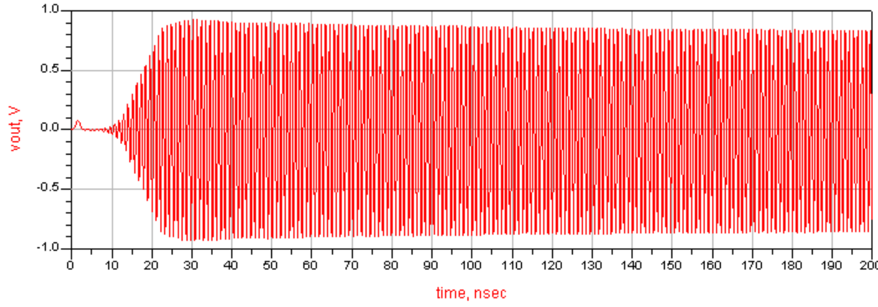
Without Filter



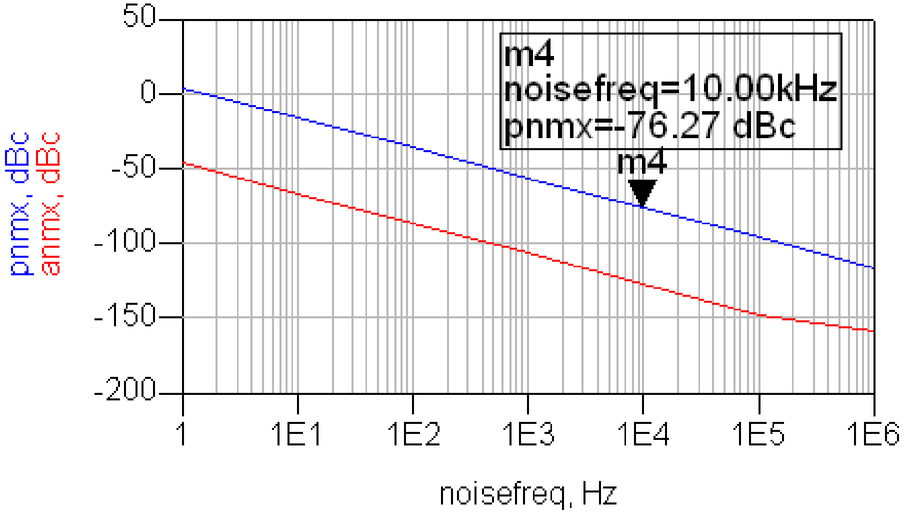
With Filter



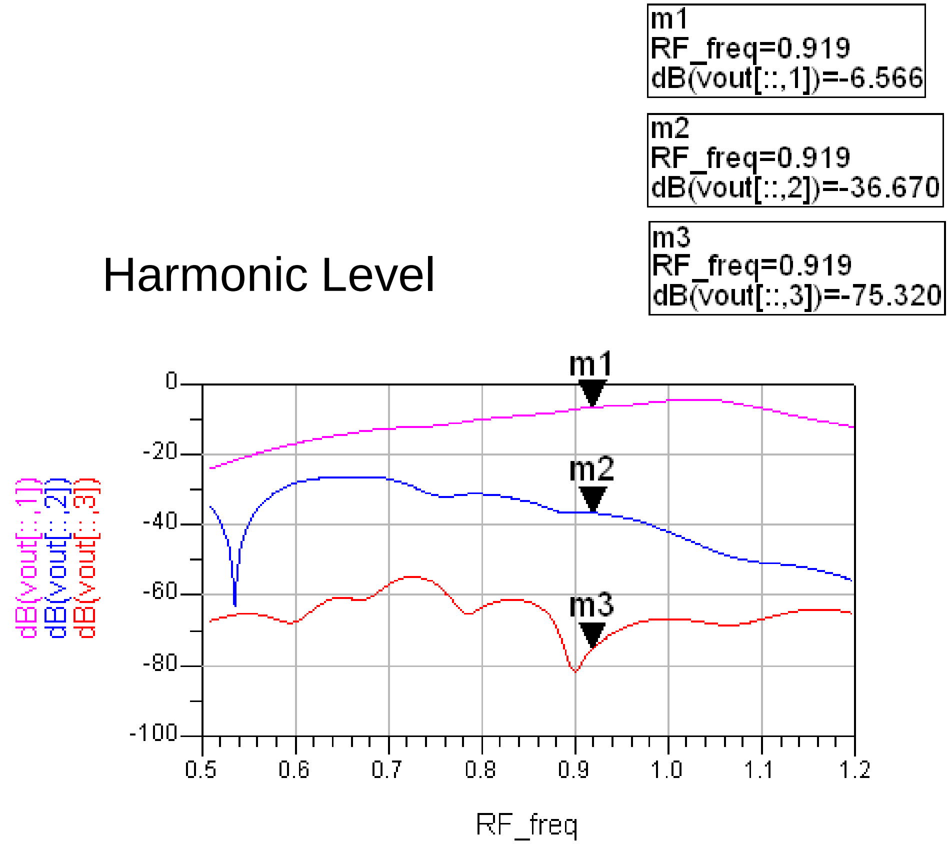




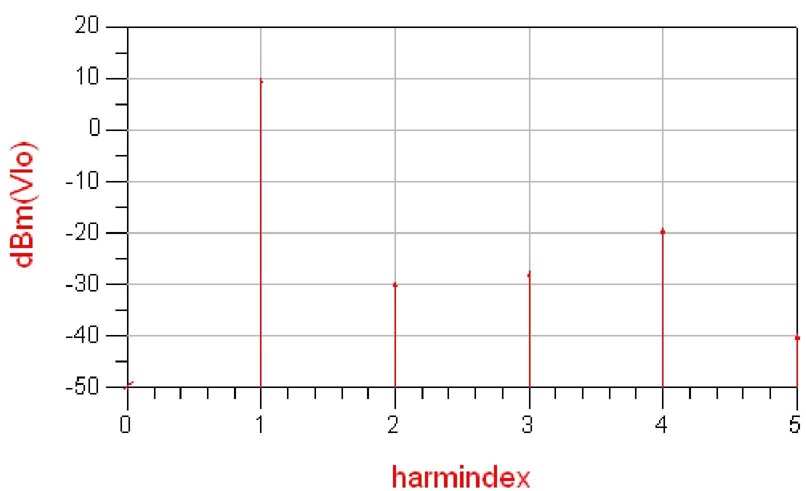
Phase Noise



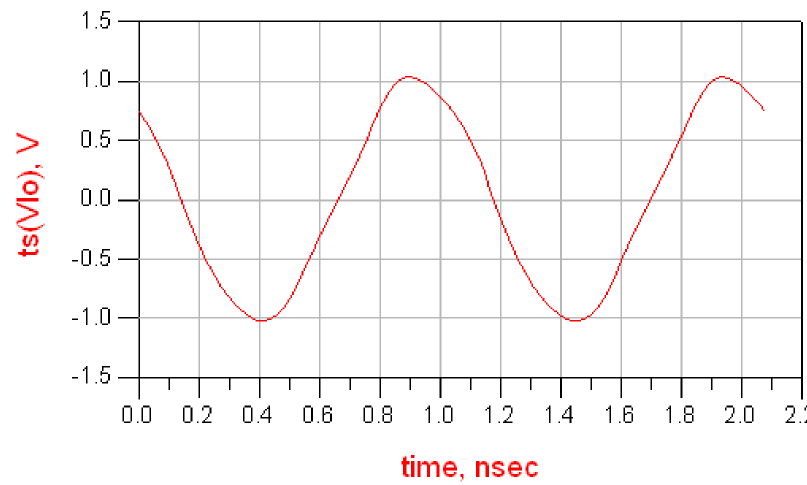
Harmonic Level



Harmonic Spectrum



Time Signal Output



Thank you !

End of Chapter 6