# Optimization of High Voltage SiC PiN Diode for Operation in Opening Switch Mode


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***Abstract*—A high-voltage silicon carbide (SiC) PiN diode that was primarily designed to operate as a rectifier in energy conversion systems was evaluated in an opening switch mode by testing it in inductive storage circuit. Based on obtained experimental data, a mixed-mode simulation model which includes the circuit topology and the device structure, was created and validated. Numerical simulations of a diode structure optimized for operation in an opening switch mode was performed.**



***Keywords—semiconductor opening switch, PiN diode, numerical simulation, Silicon Carbide, High Voltage.***


## I. Introduction

Pulse power generators with inductive storage and fast current interrupters are of great interest for pulsed power electronics. A silicon device called drift step recovery diode (DSRD) was proposed and realized in 1983 by Grekhov, at al. to be used as a solid-state current interrupter [1]. The diode structure consisted of $p^+/n/n^+$ layers and was capable of interrupting current densities up to 160 A/cm$^2$ with current interruption times of about 2 ns and voltages on the order of 1 kV.

In 1991, Mesyats, et al. from the Institute of Electro-physics (Russia) discovered another semiconductor opening switch (SOS) effect in silicon PiN-diode like structures. The $p^+/p/n/n^+$ silicon diodes could interrupt current densities of ~60kA/cm$^2$. This effect was used to develop high-power semiconductor opening switches in intermediate inductive storage circuits [2]. The breaking power of the opening switch was as high as 5 GW with interrupted currents up to 45kA, reverse voltages up to 450kV, and current interruption times between 10 ns and 60 ns.

Fig. 1 (left scale) illustrates the comparison of the DSRD and SOS devices among other solid-state current switchers, where $t_c$ is the characteristic time either of the current build-up through a device (FT-Fast Thyristor) or its cut-off (CSD-Charge Storage Diode, DSRD, SOS), while Figure 1 (right scale) shows the maximum working voltages achieved in the above-mentioned semiconductor switches. The current interrupters developed on the basis of DSRDs have a maximum operating voltage of 20-30 kV [3].

Compared with other state of the art devices that are capable of switching multi-kW to multi-MW electrical pulses in less than 10 ns, these Si based diode switches are the best choice when high pulse repetition rate, high average power, and long lifetime are required.

Fundamental limitations of these devices, which primarily result from material properties (electric field breakdown strength, maximum junction temperature, carrier saturation velocity, and dielectric constant) can potentially be extended to realize a smaller, faster, higher voltage device made of Silicon Carbide.

Basic physical properties of SiC open up a unique opportunity to fabricate switches with 20 times faster switching speed than corresponding Silicon devices with the same operating voltage. Moreover, the average pulse repetition frequency for SiC devices can be more than ten times higher than that of Si devices under the same conditions of heat power dissipation.

Ivanov, et al. reported a mesa-epitaxial 4H-SiC p+/p/n/n+-diode operating in pulse regimes similar to DSRD and SOS modes [4]. It has been demonstrated that after short pumping the diodes by a forward current pulse (5 ns duration, 200A/cm2

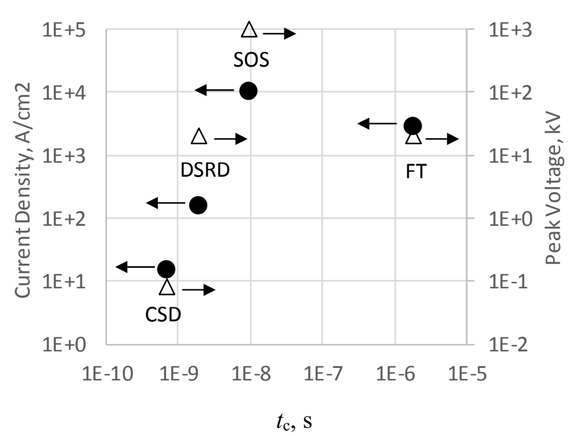


Fig.1. (left scale) Characteristic current density switching time $t_c$, and (right scale) working voltage, U, of semiconductor devices with different mechanisms of current switching: CSD - Charge Storage Diode; DSRD - Drift Step Recovery Diode; FT - Fast Thyristor; SOS - semiconductor opening switch.


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peak current density) followed by applying a reverse voltage pulse (rise time of 2 ns), the diodes were able to interrupt a reverse current density of 3.5 - 25 kA/cm2 in a time less than 0.3 ns.

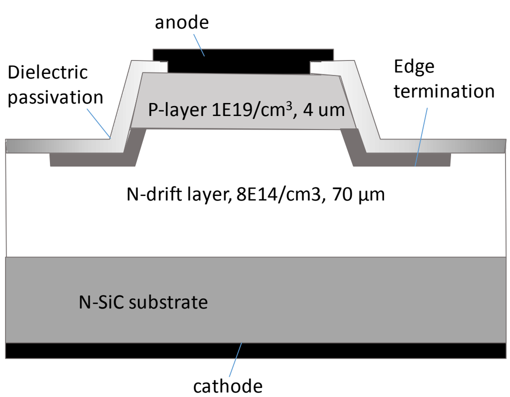
However, despite SiC DSRD and SOS devices showing encouraging results that may qualify them as ultrafast switches in high power pulse systems, many more design and processing issues need to be addressed. Specifically, a premature surface breakdown at SiC DSRD (SOS) chip edges is still a major hurdle to clear as it has been reported in Refs. [4,5]. Moreover, relatively short lifetimes of charge carriers in SiC could be another limiting factor to implement SiC SOS devices.

Although, the premature breakdown issue in SiC power devices has been resolved to date by using specially designed edge termination that enabled to achieve a breakdown voltage close to the theoretical limit [6], charge carrier lifetimes are subject for improvement in SiC technology.

The objectives of this work are to test a GE 6.5kV SiC PiN diode with robust edge termination in a fast switching mode, develop and validate numerical models based on obtained empirical data and perform optimization of opening switch diode.

## II. EXPERIMENT

SiC PiN diodes used in this work were designed to operate in energy conversion systems up to 6.5kV with fast recovery switching waveforms and low reverse recovery losses [6]. Fig. 2a shows a schematic cross-section of the device. The diodes were fabricated on a 4H-SiC N-type substrate with a 70-µm drift layer and $8 \times 10^{14}$ $cm^{-3}$ doping. The anode area of the diodes was formed using reactive ion etching of the p-type layer (4 µm, $1 \times 10^{19}$ $cm^{-3}$) grown on top of the lightly doped n-type drift layer. An aluminum-implanted junction termination extension was used to achieve a high blocking voltage. Implant activation was carried out at 1675◦C. Al/Ni/Al ohmic contacts were patterned and annealed at 1050◦C. The chips were designed to operate at a current density of 200 A/$cm^2$.

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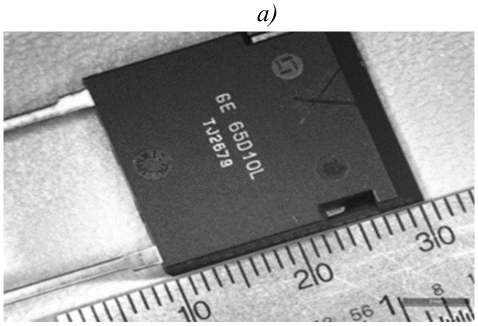



*b)*

Fig.2. (a) Cross-section of GE SiC PiN diode and (b) Photograph of packaged SiC 6.5kV PiN diode.

The SiC diodes were packaged in ISOPLUS™ discrete package (one 6x6 $mm^2$ chip per package) as shown in

The switching characteristic of this diode was tested using a resonant circuit with a single pole admittance. The circuit, shown in Fig.3, was realized using a SiC MOSFET, a 20 nF array of Class 2 ceramic capacitors, and a 250 nH aircore inductor. The current through the diode was measured using a current transformer with a 2 ns usable risetime (Pearson 6585 which is not shown in SPICE model diagram) and the voltage switched by the diode was measured using a high voltage 20 dB pad with 50 Ω input impedance with a 500 ps usable risetime (TPS). The waveforms were measured using a Tektronix MSO4034B (350 MHz front-end bandwidth, 2.5 GSa/sec). The measured results are shown Fig.4.

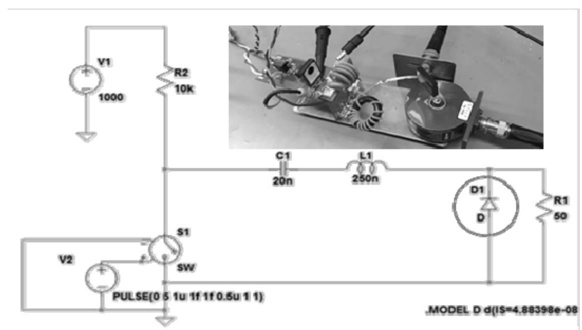



Fig.3. Testing circuit diagram used for SPICE modeling and a picture of the testing board set-up

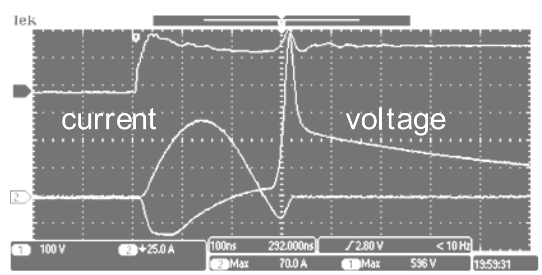



Fig.4. Load resistor voltage and current waveforms

## III. MODELING AND DEVICE OPTIMIZATION

Mixed-mode simulation was employed in order to model the switching characteristics of the PiN diode shown in Fig. 4. The mixed-mode simulation includes a circuit model with a device structure model of the diode. The PiN device structure shown in Fig. 2a was simulated together with the circuit shown in Fig. 3. The results of the simulation are shown in Fig. 5, where experimental voltage waveforms across the load resistor are added for comparison purposes. A good fit between model and experimental curves for rise and fall times of the voltage pulse was achieved, although some inconsistencies in the waveforms at turn-on were observed, which we believe, are associated with parasitic noise of the measurement tools. Carrier lifetimes used in the model were 500 ns and 11 ns for electrons and holes, respectively.

The tested PiN diode was designed to be used as a rectifier with fast recovery, thus to have an SOS like diode, the device structure must be modified in order to increase the speed of the current interruption process during the second half part of the reverse recovery process. Two structures are proposed for sharp current interruption in SiC diodes: (a) p+-p-n+-substrate and (b) p++-p-n$^-$-n+-substrate [4]. The first structure requires a deep dry etch process which is challenging in SiC technology, thus, the second structure is more promising at this point and it is modeled in this work.

Following recommendations made in Ref [7] that a thickness of p-plasma storage layer, $W_p$, should be around ~0.1$W_n$, where $W_n$ is the thickness of the n-drift layer, a numerical design of experiment was performed. Figure 6 shows calculated current and voltage waveforms for an optimized structure of a SiC opening switch. Note, that the parameters of the circuit elements and pumping pulse characteristics used are the same as in the validation model of the PiN diode. Current and voltage waveforms of the SiC PiN diode are shown in Fig. 6 for comparison purposes. A peak value of 2600V during reverse recovery was achieved in the opening switch due to the sharp current interruption, while in the PiN diode, the peak voltage was only on the order of 600V at a maximum voltage of 500V across the discharge capacitor.

Fig. 7 shows the electric field distribution in the PiN diode (Fig.7a) and opening switch diode (Fig.7b) at characteristic transient times $t_1$, $t_2$, and $t_3$, as marked in Fig.6. Note, that the waveforms in Fig. 6 were synchronized with a pumping pulse. Time $t_1$ corresponds to the peak value of the reverse current in the PiN diode. Electron-hole plasma in the PiN diode at this instant has started to disassociate and a space charge region with a peak electric filed at the p-n junction started to fill the drift region, while a reverse current in the opening switch has not reach its maximum value and an electric field has not formed yet. When a reverse current in the opening switch diode reaches its maximum value (time $t_2$), the electric field distribution in the SOS diode is similar to the field distribution in the PiN diode at $t_1$, however, in the PiN diode, the space charge region expanded deeper into the drift layer and the peak of electric field has increased. At time $t_3$, an electron-hole plasma in the opening switch diode is completely disassociated, the space-charge region (SCR) is extended through the entire drift layer. The latter causes a sharp current interruption and a voltage increase across the load resistor. Transient currents in the PiN diode at the corresponding time $t_3$ are gradually decreasing since non-equilibrium charge carriers have not completely recombined and the SCR has not reached the n$^+$ layer (Fig.7a).

## IV. CONCLUSIONS

Mixed-mode simulations of an optimized diode structure with an additional p-layer has demonstrated the feasibility of making a SiC diode with a semiconductor opening switch effect even with charge carrier lifetime values typical for modern SiC technology. The model suggested that, e.g., with a 500V charged capacitor, a 7ns pulse of 2600V could be achieved across the load.

Further tuning of the SOS diode structure and optimization of the circuit topology should improve both the risetime and the voltage peak.

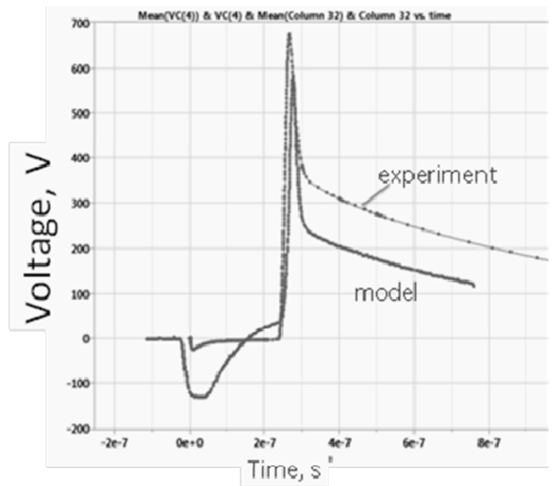



Fig. 5 Experimental and simulated voltage waveforms of SiC diode on load resistor per circuit of Figure 3.

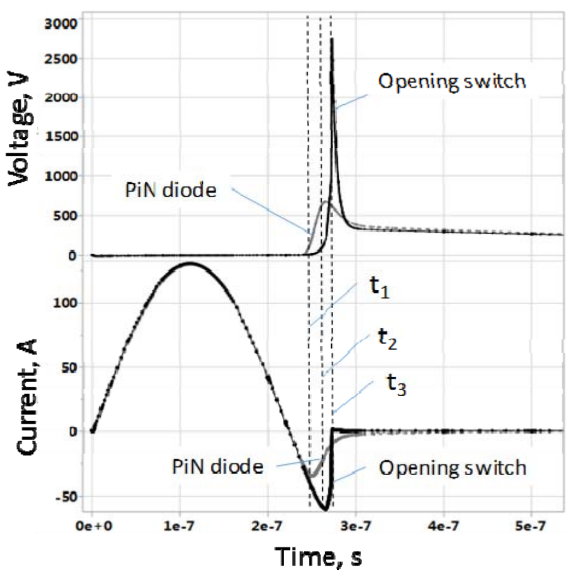
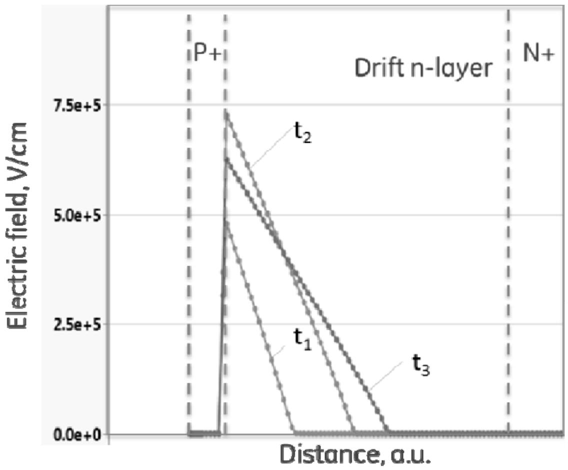



Fig.6. Simulated voltage and current waveforms of PiN diode and opening switch diode..

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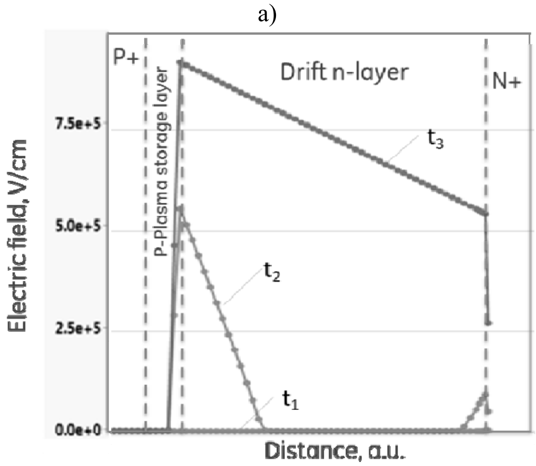


b)

Fig.7. Electric field distributions at different transient times in (a) PiN diode and (b) open switch diode.

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