SiC Power Schottky and PiN Diodes

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***Abstract*—The present state of SiC power Schottky and PiN diodes are presented in this paper. The design, fabrication, and characterization of a 130 A Schottky diode, 4.9 kV Schottky diode, and an 8.6 kV 4H-SiC PiN diode, which are considered to be significant milestones in the development of high power SiC diodes, are described in detail. Design guidelines and practical issues for the realization of high-power SiC Schottky and PiN diodes are also presented. Experimental results on edge termination techniques applied to newly developed, extremely thick (e.g., 85 and 100 μm) 4H-SiC epitaxial layers show promising results. Switching and high-temperature measurements prove that SiC power diodes offer extremely low loss alternatives to conventional technologies and show the promise of demonstrating efficient power circuits. At sufficiently high on-state current densities, the on-state voltage drop of Schottky and PiN diodes have been shown to be comparable to those offered by conventional technologies.**

***Index Terms*—Diode, leakage, on-resistance, PiN, rectifiers, reverse recovery, Schottky, SiC.**

I. Introduction

POWER diodes made with silicon carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because SiC has an order of magnitude higher breakdown electric field ($2-4\times10^6$ V/cm) than conventional materials, and an electron mobility only ~20% lower than silicon. A high breakdown electric field allows the design of SiC power diodes with 10× thinner and higher doped (100×) voltage blocking layers. The 4H polytype of SiC is particularly suited for vertical power devices because of its higher vertical (a-axis) mobility. Its larger bandgap is also expected to result in a much higher operating temperature and higher radiation hardness. The thermal conductivity of n^+ SiC is approximately >3.3 W/°C-cm at room temperature, which is 2–3× higher than Si. High voltage (>3 kV) Si PiN diodes made using conventional semiconductor materials are restricted to <50 kHz and <120 °C, thereby severely limiting the availability of advanced electronic hardware used for utility applications, energy storage, pulsed power, intelligent machinery and solid state power conditioning. The main features of 4H-SiC PiN high voltage diodes are: 1) a voltage drop in the on-state comparable to stacked Si diodes at sufficiently high current densities; 2) switching speeds that are at least 30× faster than any of their Si counterparts because of the use of thinner epitaxial layers; and 3) good high-temperature operating characteristics.

A two orders of magnitude advantage in resistance is expected for Schottky-based diodes in SiC over those in Si, thereby making them attractive in the commercially lucrative 600–1500 V range, where Si PiN diodes are used. For the voltage range of 1500–3000 V, SiC Schottky-PiN hybrid rectifiers like the JBS and MPS diodes are expected to replace Si PiN diodes used in this voltage range due to their superior on-state and switching characteristics. Beyond 3kV, SiC PiN diodes offer performance advantages over Si PiN diodes because of their exceptionally fast switching and excellent high-temperature stability. At frequencies above 100–150 kHz, SiC Schottky diodes also become competitive with SiC PiN diodes at any blocking voltage.

II. 4H-SiC Schottky Diodes

The biggest challenge in realizing the full potential of high-power 4H-SiC Schottky diodes is the achievement of lowest possible on-state voltage drop and a high breakdown voltage for a given voltage blocking epitaxial layer, over a sufficiently large area. A typical Schottky diode consists of an ideal rectifying metal contact deposited on an optimally designed epitaxial layer, an appropriate edge termination design, a highly doped substrate, and a backside ohmic contact. The doping and thickness of the epitaxial layer determine its resistance and the ideal blocking voltage capability. There exists a trade-off between these competing performance parameters as explained in [1]. Usually, the targeted blocking voltage rating and the effectiveness of the edge termination employed determines the minimum thickness and the maximum doping used for the design of epitaxial layer properties. The specific on-resistance of the epitaxial layer used in the fabrication of a Schottky diode made using n-type SiC is given by

$$R_{epi} = \frac{W_D(N_D)}{q \cdot \mu_n \cdot N_D} \tag{1}$$

where $W_D(N_D)$ is the epitaxial (drift) layer thickness, N_D is the doping of the epitaxial layer, q is the electronic charge, and μ_n is the doping dependent bulk electron mobility, as given by [2]. A nonpunchthrough drift region design corresponds to the case where drift region thickness is equal to or larger than the parallel plane avalanche breakdown width [1]. In the case of a punchthrough drift layer design, the epitaxial layer thickness is smaller than the parallel plane breakdown avalanche breakdown

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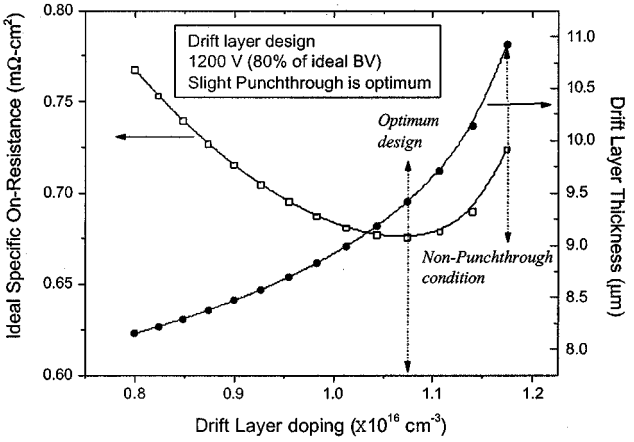

Fig. 1. Lowest resistance epitaxial layer design for a majority carrier device (like Schottky barrier diode) corresponds to a slightly punchthrough condition.

width. For such a case, the drift region thickness can be derived from basic depletion equations to be

$$W_D = \frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D} - \sqrt{\left[\frac{\varepsilon \cdot E_C(N_D)}{q \cdot N_D}\right]^2 - \left[\frac{2\varepsilon \cdot V_B}{q \cdot N_D}\right]} \quad (2)$$

where V_B is the designed breakdown voltage of the diode, ε is the dielectric constant of SiC, and $E_C(N_D)$ is the critical electric field as a function of the drift region doping. One of the empirically derived relationships showing the dependence of critical electric field with drift region doping in 4H-SiC is given by [3]

$$E_C = \frac{2.49 \times 10^6}{1 - \frac{1}{4}\log\left(\frac{N_D}{10^{16}}\right)}. \quad (3)$$

Using these formulae, the design of drift region doping and thickness can be performed to determine the lowest possible specific on-resistance for a given designed breakdown voltage of any majority carrier device, such as a Schottky barrier diode. Fig. 1 shows such a design performed for a breakdown voltage of 1200 V assuming 80% ideal breakdown is achieved. This plot shows that the lowest specific on-resistance corresponds to a drift region doping and thickness corresponding to a slightly punchthrough design.

The on-state voltage drop is primarily determined by the metal–semiconductor barrier height of the Schottky metal used (which determines the knee voltage), and the on-resistance of the diode. It is essential to minimize the parasitic on-resistance components such as substrate and cathode contact resistance and the anode metallization resistance. Schottky diodes are very vulnerable to the leakage current, which may also determine its breakdown voltage.

Over the past ten years, the tradeoff between on-state and blocking voltage results reported have improved with the improvement of material quality and refinement of device edge termination techniques. Probably the first demonstration of a high-voltage SiC Schottky diode was done by Bhatnagar *et al.* [4] in 1992. In this paper, 400 V Schottky diodes were demonstrated using 10 μm, 3.6E16 cm^{-3} doped epitaxial layers. No edge termination was used in the fabrication of these diodes. After the commercial availability of better quality SiC substrates and refinement of edge termination techniques, improved results were obtained. A highly resistive implanted edge termination ring around the Schottky contact provided a relatively high leakage current, but near-ideal Schottky diodes [5] in 1996. This demonstration shows a 1.1 kV Schottky diode made using a Boron dose of 1E15 cm^{-2} in a 100 μm band around the Schottky metal. The development of hot wall CVD technique dramatically improved the quality of epitaxial layers used for the fabrication of SiC devices. This was particularly significant because the control of leakage current was a major limitation in the demonstration of high voltage Schottky diodes, which is partially dependent on the integrity of the voltage blocking epitaxial layers used to fabricate them. In 1999, [6] demonstrated a 300 μm diameter, 3.85 kV Schottky diode made using 43 μm epitaxial layers grown using hot wall CVD technique with an on-state voltage drop of 3.9 V at 100 A/cm^2.

With the advent of junction termination extension (JTE) using a controlled activation of Boron ion-implanted species, the tradeoff between on-state and blocking voltage of Schottky diodes improved significantly. This technique propelled such Schottky diodes into a commercially attractive range. The achievement of a good tradeoff between on-state and reverse characteristics was assumed, and performance and reliability of these diodes was evaluated in order to be commercially competitive. Reference [7] showed avalanche capable Schottky diodes with stable forward and reverse characteristics for 1000 h in 1999. Further, these 600 V, 2.25 mm^2 Schottky diodes have a low $R_{on,\,sp}$ of 2.1 mΩ-cm^2 and carry a rated current of 6 A.

The design, fabrication, and experimental results that amplify issues and challenges faced in the implementation of high voltage Schottky diodes are presented below.

A. 1700 V Schottky Diodes

In this experiment, two types of Schottky metals: nickel and titanium, were used on Schottky diodes made with a 13 μm epitaxial layer with a 3.3×10^{15} cm^{-3} doping [8]. A 100 μm band of Boron ion implantation with a total dose of 10^{15} cm^{-3} was implanted at 30 keV as an edge termination design. This implant was annealed at 1050 °C for 90 min. The backside contact was unannealed aluminum onto unpolished heavily doped substrate. No passivation was used on top of the edge terminated areas.

Both Ni and Ti Schottky diodes show good Schottky on-state characteristics with eight decades of linearity on a semi-logarithmic plot at 20 °C, and eventually rolling off because of epitaxial layer resistance. The specific on-resistance was measured at 5.6 mΩ-cm^2, which was influenced by backside contact and substrate region resistance. The on-resistance increases with an increase in temperature up to 255 °C. The measured ideality factors for Ti and Ni Schottky diodes were 1.15 and 1.21, respectively. The metal–semiconductor barrier height measured from the on-state characteristics shows a 0.8 eV for Ti and 1.3 eV for Ni. The highest blocking voltage of 1720 V was obtained from a Ni Schottky diode. The reverse leakage current was found to increase linearly with voltage up to 500 V in the case of Ni Schottky diodes, which changes to a conventional exponential behavior at higher blocking voltages. The Boron implanted edge termination regions form a resistive leakage path which results

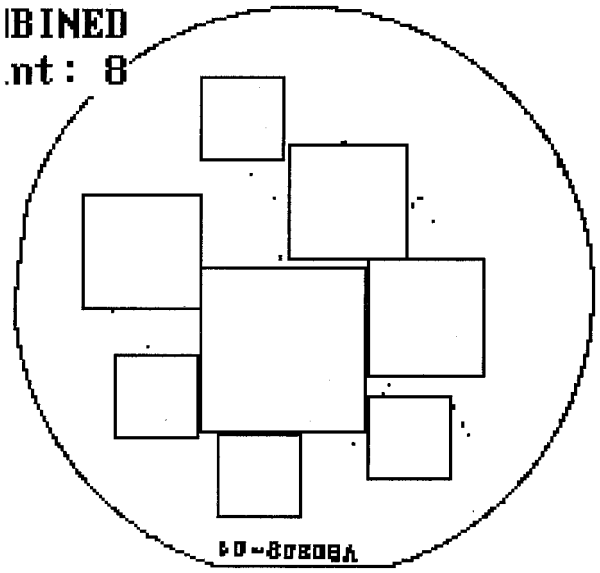

Fig. 2. Micropipe map of a 1.375″ 4H-SiC wafer with 1 cm × 1 cm, 0.7 cm × 0.7 cm, and 0.5 cm × 0.5 cm areas identified with no micropipes. The 0.5 cm × 0.5 cm MFAs were ignored.

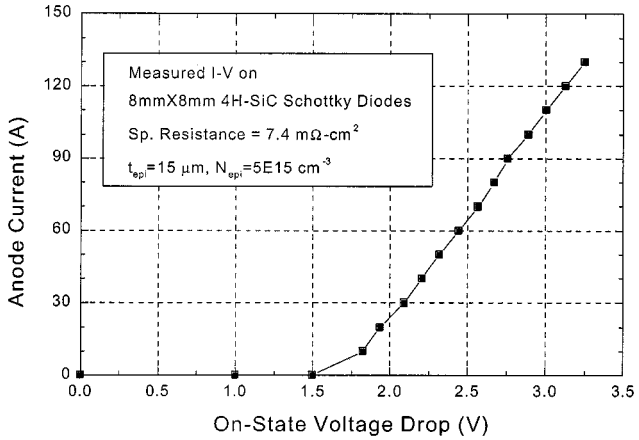

Fig. 3. High current of 130 A was achieved on a 0.8 cm × 0.8 cm Pt Schottky diode with a 300 V blocking capability. The measured specific on-resistance was only 7.4 mΩ-cm^2.

in the linear reverse current–voltage (I–V) characteristics. This leakage was not found to be evident in the case of Ti Schottky diodes because of the lower Schottky barrier height of Ti, which results in a three orders of magnitude higher leakage current, which overshadows the resistive leakage current due to Boron implanted edge terminations.

B. 130 Ampere Schottky Diodes

Presently, large area high-voltage Schottky diodes in 4H-SiC suffer from a low yield due to the presence of micropipes. However, micropipes tend to cluster together leaving some randomly distributed, relatively large, micropipe free areas (MFA). On some 4H-SiC wafers, 1 cm × 1 cm and 0.7 cm × 0.7 cm areas were identified, as shown in Fig. 2, for the fabrication of 0.8 cm × 0.8 cm and 0.6 cm × 0.6 cm Schottky diodes, respectively. On these wafers, 15 μm of 5 × 10^{15} cm^{-3} n- epitaxial layer was grown. Using standard optical tools, photolithography on such randomly located areas was particularly challenging. This implant was annealed at 1500 °C, to activate the Boron and mitigate the implant damage. A Boron edge termination with a total dose of 7 × 10^{12} cm^{-2} was implanted up to a depth of 0.7 μm in the entire wafer, except for the Schottky contact area. A passivating oxide of 1.5 μm was deposited on top of this implant. A backside annealed Ni contact was used to achieve a low contact resistance. The biggest challenge facing the achievement of a high blocking voltage was the leakage current generated on such large Schottky contacts. Platinum was used as a Schottky metal because of its relatively large barrier height to 4H-SiC, which suppresses the leakage current generated across the Schottky interface. A 2 μm gold layer was deposited on top of this Schottky metal in order to minimize anode current spreading resistance.

A high current of 130 A was passed through a 0.8 cm × 0.8 cm Schottky diode with an on-state voltage drop of 3.25 V, as shown in Fig. 3. This current corresponds to over 200 A/cm^2, and represents the highest current single chip, Schottky diode demonstrated yet in SiC. This measurement was conducted on unpackaged diodes which were clamped between two metal slugs which were attached to the two terminals of a high current power supply. A high current pulse was applied and an on-state voltage drop was measured for these diodes. A relatively low specific on-resistance of 7.4 mΩ-cm^2 was achieved on this large area Schottky diode. However, a relatively high leakage current of 120 mA was observed at 300 V, as measured on a diced, bare chip using a standard curve tracer. On smaller 0.6 cm × 0.6 cm Schottky diodes made on the same wafer, a blocking voltage of 600 V was observed at a leakage current of less than 10 mA.

C. Comparison of 1200 V SiC Schottky Diode With Si Diodes

For 1200 V SiC Schottky diodes to have a comparable on-state voltage drop as fast Si PiN diodes, the total on-resistance must be below 4 mΩ-cm^2. Using 10 μm, 2.7 × 10^{15} cm^{-3} epitaxial layers, Schottky diodes with 1250 V blocking capability and total on-resistance of 2.2 mΩ-cm^2 were demonstrated [9]. Boron was implanted at a total dose of 10^{15} cm^{-2} at 30 keV in a 100 μm band around the Schottky contact to provide a edge termination region, and no passivation was used on top of these terminated regions. The wafers were annealed at 1050 °C for 90 min to activate part of the implanted Boron. The 0.1 μm Ni Schottky contact used for these diodes was capped with 1 μm of gold in order to minimize the anode spreading resistance. The backside Ni contact was annealed at 950 °C for 3 min in order to get a good backside ohmic contact. The measured barrier height for Ni was 1.4 eV, and a forward voltage drop of 2.0 V was measured at a current density of 300 A/cm^2.

The reverse recovery measurements conducted on these diodes at a di/dt of 1000 A/μs and 150 °C show a 7× reduction in peak reverse current and a 5× reduction in reverse recovery time as compared to ultrafast Si PiN diode (Harris RHR660). These diodes were evaluated at high temperatures in a clamped inductive load test [9]. The energy loss in Si PiN diodes increases dramatically with temperature, due to the well known increase in peak reverse current. However, the transient current in these SiC Schottky diodes was found to be independent of temperature. Therefore, the turn-on energy

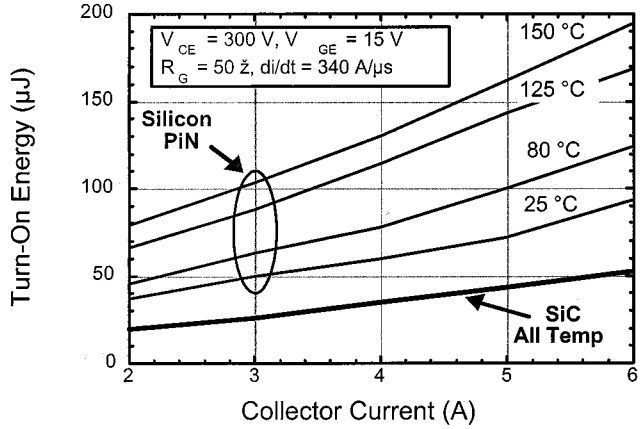

Fig. 4. IGBT turn-on energy comparison of inductively clamped circuit with SiC Schottky diodes and Si PiN diodes in the 25 °C to 150 °C range. While Si PiN diodes increase the turn-on energy in the IGBT by 2× for a Si PiN diode case, it remains unchanged in the case of SiC Schottky diodes in this temperature range.

loss in the SiC Schottky diode was constant over 25 °C to 150 °C temperature range, as shown in Fig. 4. Between room temperature and 150 °C, the Si PiN diode tested showed a 2× increase in energy loss, while the SiC Schottky diode showed no significant increase over the same range.

D. 5 kV 4H-SiC Schottky Diodes

The highest voltage 4H-SiC Schottky diode demonstrated yet is the 5 kV SiC Schottky diode [10], whose I–V characteristics are shown in Fig. 5. A 50 μm epitaxial layer doped at 7×10^{14} cm^{-3} and a 100 μm Boron implanted edge termination region was used for the fabrication of this device. 0.1 μm Ni was used as a Schottky contact while the backside Ni contact was annealed at 975 °C for 3 min. No passivation was used on top of the edge terminated areas. The extracted Schottky barrier was 1.41 eV, with an ideality factor of 1.1, and the specific on-resistance of 17 mΩ-cm^2. This value of resistance is close to the theoretical resistance of the epitaxial layer used in the fabrication of this diode. At 25 A/cm^2, this 425 μm diameter device showed an on-state voltage drop of approximately 2.4 V. Such extremely high voltage 4H-SiC Schottky diode may be useful in high voltage military hardware where switching speeds significantly determine the circuit efficiency.

III. 4H-SiC PiN Rectifiers

As mentioned previously, >3 kV 4H-SiC PiN rectifiers offer extremely high switching speeds and a comparable on-state voltage drop at sufficiently high current densities. The biggest challenges facing the realization of such high voltage rectifiers is the design of the edge termination and the growth of pure, low defect density epitaxial layers with sufficiently high minority carrier lifetimes. The advent of hot wall epitaxial reactors have enabled the growth of >40 μm 4H-SiC epitaxial layers which are capable of blocking >4 kV. In the recent past, minority carrier lifetimes have been improved to a level that enables the realization of high voltage SiC diodes with <4.5 V on-state drop at 100 A/cm^2. From a device design standpoint,

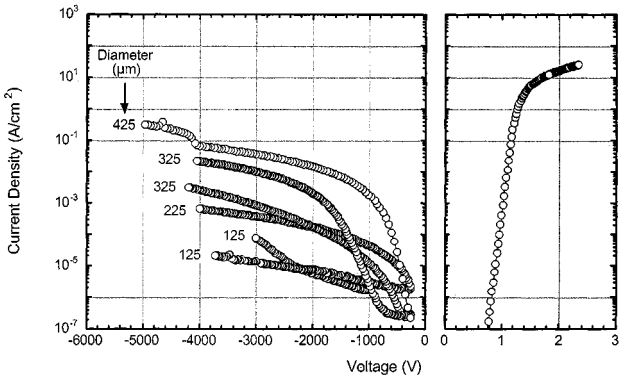

Fig. 5. Forward and reverse (I–V) characteristics of several nominally 5 kV Schottky barrier diodes.

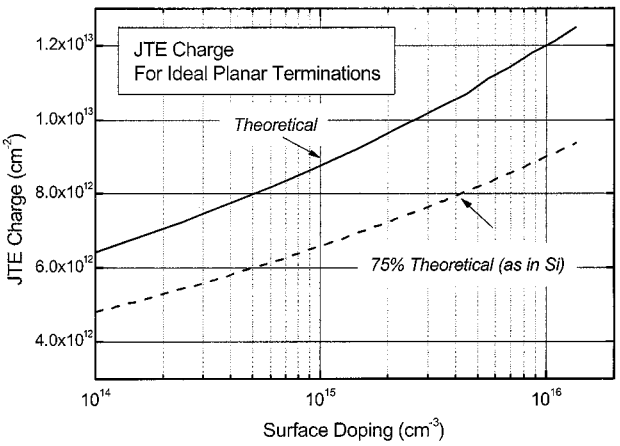

Fig. 6. JTE charge versus surface doping of the voltage blocking layer for a SiC device.

the biggest challenge is the design and implementation of an effective edge termination.

An effective edge termination technique makes the electric field distribution uniform at the edge of the device, in order to approach the ideal breakdown voltage capability of the epitaxial layer used. Traditionally, many techniques like guard rings, floating field rings, and trench guard rings [11] have been used to achieve this. Another promising edge termination design involves implanting the device edge with an optimum p-type charge (for the typically used n-type epitaxial layer) in order to gradually reduce the electric field from the edge of the Schottky diode to the outer periphery of the device structure. This technique is called junction termination extension (JTE). The optimally implanted JTE charge that corresponds to the ideal breakdown voltage depends upon the background doping concentration of the low doped n-type region. A plot showing the ideal total charge per unit area along a vertical cross-section of the implanted JTE region is shown in Fig. 6. In silicon, when planar terminations are made using JTE, it has been found that it is safe to implement a JTE charge with about 75% of that predicted by theoretical analysis. This is because JTE charge in excess of the ideal value results in a sharp reduction in the obtained breakdown voltage, while a charge smaller than the optimum does not severely affect the breakdown voltage of the device. The JTE charge corresponding to 75% is also plotted in

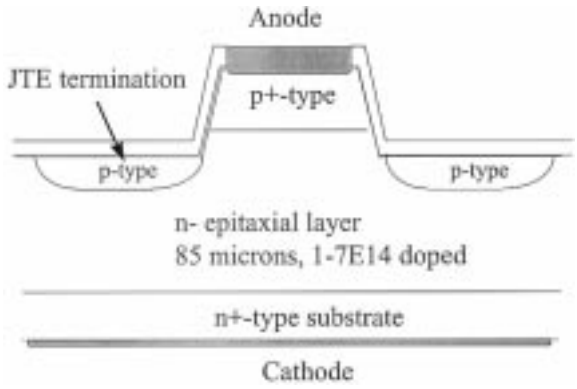

Fig. 7. Structure of the planar PiN diode using JTE termination.

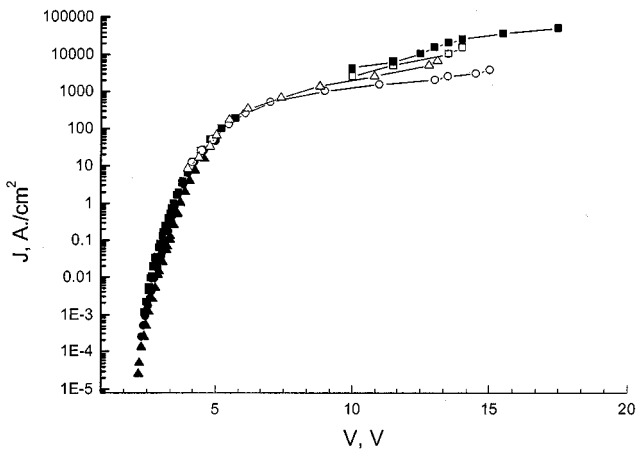

Fig. 8. Forward I–V at ultrahigh current densities of 50 kA/cm^2 on many 5.5 kV PiN diodes show a modest forward voltage drop of 17–18 V.

this graph for silicon carbide. Most promising results on PiN diodes [12] were obtained with the ion implantation of Boron as the dopant in the JTE region.

Overall, the market for $>$2 kV 4H-SiC PiN rectifiers is relatively small as compared to 4H-SiC Schottky diodes, especially in the relatively low current range that are commercially feasible at the present state of material technology. Hence, there are relatively few groups working in this field. Mitlehner [12] demonstrated extremely fast switching characteristics of 3.3 kV 4H-SiC PiN rectifiers. Lendenmann *et al.* [13] demonstrated a commercially attractive marriage of Si IGBT with SiC Schottky diodes in a 2.5 kV, 150 A motor control module. This demonstration showed that Si-IGBTs do not have to be severely de-rated when used in conjunction with a SiC rectifier as compared to when it is used with a similarly rated Si rectifier. This is because the turn-on energy loss in the IGBT is reduced substantially when the rectifier is undergoing reverse recovery. This study also demonstrated important guidelines for the optimization of modules that utilize SiC rectifiers and devices. Below, some salient results on high voltage SiC rectifiers developed by the authors over the past five years are presented.

A. The 5.5 kV PiN Rectifier

The first successful attempt in the demonstration of a $>$5 kV 4H-SiC rectifier was done using a 4H-SiC n$^-$ epitaxial layer with a thickness of 85 μm and a doping in the range of 1 to 7E14 cm^{-3} [14]. This epitaxial layer grown by chemical vapor deposition (CVD) in a hot-wall SiC CVD reactor. To achieve a high activated p$^+$ concentration, the anode region was epitaxially grown to enable a high concentration of injected holes into the low doped drift layer during the on-state operation of the diode. To prevent premature breakdown of the device, the voltage-blocking layer was exposed and junction termination extension (JTE) was used as the planar edge termination method as shown in Fig. 7. The 500 μm JTE terminated zone was passivated using a 1.5 μm SiO_2 layer. Although the device did not fail while blocking 5.5 kV, a high leakage current of 250 μA (3 A/cm^2), was observed using an on-wafer measurement conducted using a high voltage (20 kV) power supply. The leakage current at a reverse bias of 4500 V was approximately 80 μA. The forward voltage drop at 100 A/cm^2 was 5.4 V. The contacts have a resistivity of 10 mΩ-cm^2 which contributes 1 V drop at a current density of 100 A/cm^2. The differential resistance (dV/dI) beyond the built-in voltage in this device was measured to be less than 12 mΩ-cm^2, which shows that the drift region is conductivity modulated. From this on-state voltage drop the carrier lifetime of the diodes was estimated to be greater than 1 μs.

On diodes fabricated with a similar epitaxial layer and a slightly different JTE design and better contact resistance, switching measurements were conducted. The measured rise time for an on-state current density of 1000 A/cm^2 was approximately 1.5 μs. The reverse recovery tail shows an ambipolar lifetime of $>$1.5 μs. Measurements at extremely high current densities of $>$20 kA/cm^2 show the differential on-resistance closely approaching the contact resistance value of 1–2 mΩ-cm^2, thereby showing extremely good conductivity modulation in the drift region [15]. Since the on-state voltage drop of this diode at a high current density of 50 kA/cm^2 is only 17–18 V (as shown in Fig. 8), 4H-SiC PiN diodes are expected to be promising candidates for pulsed power applications. These measurements were conducted on experimentally fabricated packaging environment in order to measure the characteristics of the diode.

B. Design and Fabrication of 8.6 kV 4H-SiC Diode

The basic structure of the diode blocking 8.6 kV is similar to that used for the 5.5 kV diode described earlier. However, the voltage-blocking layer for this diode was 100 μm with a doping of 1 to 3 $\times$ 10^{14} cm^{-3}, and the JTE length was increased to 700 μm. The voltage blocking layer was capped with a 2.5 μm, highly doped ($>$3 $\times$ 10^{18} cm^{-3}) p-type epitaxial layer, which forms the anode contact of the diode. The topside ohmic contact is made using Pt, because it has a low hole barrier height to p-type 4H-SiC. The cathode ohmic contact is made using Ni, which has been shown to result in a very low contact resistance to n-type SiC. The edge termination of this diode is implemented using the mesa-JTE termination developed at Cree, Inc. [16].

The reverse bias I–V characteristics of a 200 μm diameter diode blocking 8.6 kV using the above epitaxial structure is shown in Fig. 9. From this figure, it can be seen that the measured leakage current was below the detection limit of the instrument used (about 0.1 μA) up to 8.6 kV. Beyond this reverse

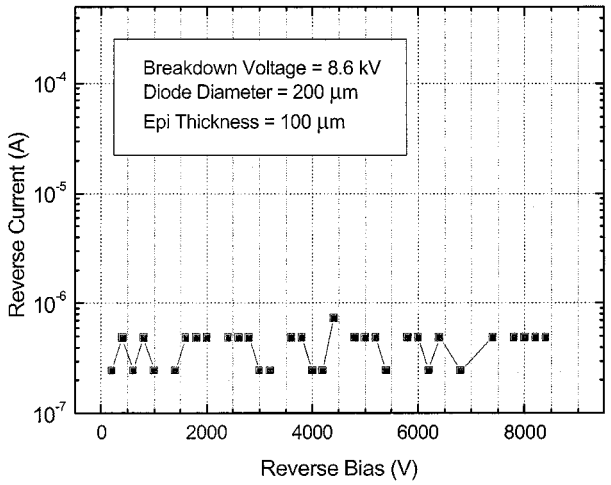

Fig. 9. Reverse characteristics show extremely low leakage up to the catastrophic breakdown of diode.

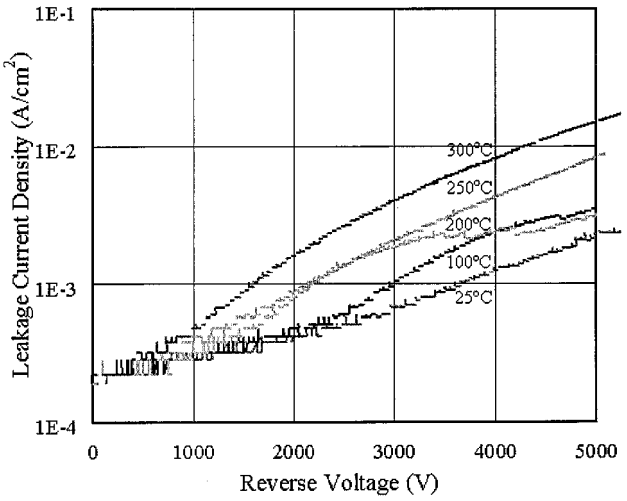

Fig. 10. Reverse bias measurements up to 5 kV show that leakage current increases by only an order of magnitude from room temperature to 300 °C.

voltage, a catastrophic breakdown was observed. This measurement was taken on wafer using a high voltage (20 kV) power supply. It was possible to find diodes with breakdown voltage $>$7 kV uniformly across the entire wafer. The yield for these devices with a breakdown voltage $>$7 kV was about 9.5% [16]. One of these diced and high voltage packaged diodes with a $>$7 kV blocking capability was measured up to 300 °C. This measurement was conducted up to 5 kV in a pure SF_6 ambient. At room temperature, the measured leakage current density was only 2×10^{-3} A/cm^2, which increased to about 2×10^{-2} A/cm^2 at 300 °C and 5 kV, as shown in Fig. 10. The edge termination design used in the fabrication of these devices is robust since it results in a leakage current increase of only an order to magnitude at 300 °C at 5 kV.

The forward voltage drop at 100 A/cm^2 for the diode blocking 8.6 kV was 7.1 V, as measured on-wafer using a probe station. The forward I–V shows the characteristic exponential increase in anode current with forward bias. Using TLM structures, the anode p-type contacts were measured to have a resistivity of 10 mΩ-cm^2, which contributes 1 V

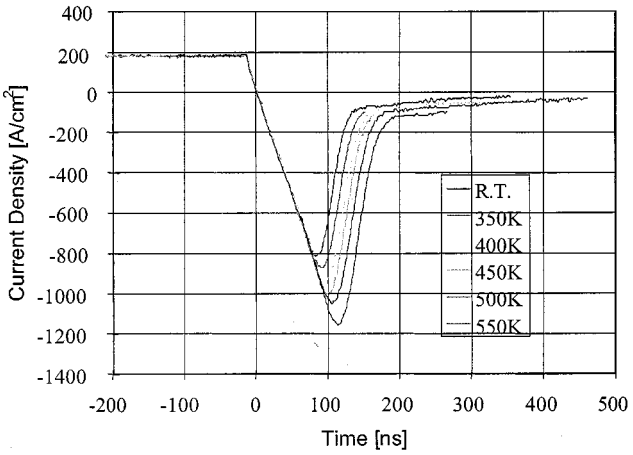

Fig. 11. Reverse recovery measurements shows only $\sim$2$\times$ increase in reverse recovery charge between room temperature and 275 °C.

drop at a current density of 100 A/cm^2. The differential resistance (dV/dI) on many diodes made on the same wafer was measured to be in the range of 18–25 mΩ-cm^2. Such low differential on-resistance can be obtained only if strong conductivity modulation is achieved in these high resistivity (625 mΩ-cm^2) drift regions during the forward conduction of the diode. The uniform differential on-resistance measured on this wafer indicates that the epitaxial layer properties are uniform across the entire wafer. The carrier lifetime of the diodes is estimated to be more than 2 μs from this differential on-resistance measurement. This value of carrier lifetime is quite high considering the very large (100 μm) epitaxial layer thickness.

Reverse recovery measurements on these diodes show extremely fast switching as compared with similarly rated Si power diodes, as shown in Fig. 11. These measurements were conducted at an extremely high reverse dJ/dt of 10^4 A/cm^2/μs because a very small reverse recovery current was observed on these diodes at lower switching rates. These measurements show about 2$\times$ increase in reverse recovery charge between room temperature and 275 °C. This is insignificant as compared to typical Si diodes, where 4$\times$ increase is observed from room temperature to 120 °C.

IV. Summary

The 4H-SiC Schottky and PiN diodes are expected to play an enabling and vital role in the design of future commercial and military hardware. The system level benefits include a large reduction in the size, weight, and cost of the power conditioning system. These devices will help in the realization of solid state power conditioning and circuit protection systems used for motors, actuators, energy storage, and pulse power systems. Results on devices presented in this paper show the capabilities of high power SiC Schottky and PiN diodes. Design, fabrication and characterization of the highest current (130 A) and highest voltage (5 kV) SiC Schottky diodes show their applicability to a large variety of ultrafast circuits. The application of 1200 V Schottky diodes to a practical circuit presented in this paper addresses the promise these devices hold for this commercially important market. The measured results from the operation of

5.5 kV 4H-SiC PiN diodes at ultrahigh current densities prove that this component will be essential for pulsed power applications. The growth of very pure, high carrier lifetime, thick 4H-SiC epitaxial layers used in the fabrication of 8.6 kV diodes is a critical technology for use in utility and military applications. Such PiN diodes have been shown to work at a high temperature of 300 °C. Characterization results presented here show that these diodes show remarkable stability at extreme operating conditions.

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