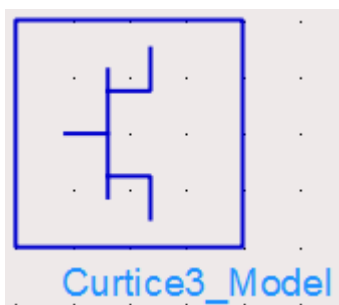


Curtice3 Model (Curtice-Cubic GaAsFET Model)

Curtice3_Model (Curtice-Cubic GaAsFET Model)

Symbol



Parameters

Model parameters must be specified in SI units.

Name	Description	Units	Default
NFET	N-channel model type: yes or no	None	yes
PFET	P-channel model type: yes or no	None	no
Idsmod	Ids model: 1=CQ 2=CC 3=Statz 4=Materka 5=Tajima 6=symbolic 7=TOM 8=Modified Materka	None	2
Beta2	Coefficient for pinch-off change with respect to Vds	1/V	0.0
Rds0 ^{†††}	DC D-S resistance at Vgs=0	Ohm	0
Vout0	output voltage (Vds) at which A0, A1, A2, A3 were evaluated	V	0
Vdsdc	Vds at Rds0 measured bias	V	0
Tau	transit time under gate	sec	0.0
Gamma	current saturation	1/V	2.0
Tnom	nominal ambient temperature at which these model parameters were derived	°C	25
Idstc	Ids temperature coefficient	None	0
A0 ^{†, ††}	cubic polynomial Ids equation coefficient 1	A	0

A1 ^{†, ††}	cubic polynomial Ids equation coefficient 2	A/V	0
A2 ^{†, ††}	cubic polynomial Ids equation coefficient 3	A/V ²	0
A3 ^{†, ††}	cubic polynomial Ids equation coefficient 4	A/V ³	0
Vtotc	VTO temperature coefficient	V/°C	0.0
Betatce	BETA Exponential Temperature Coefficient	%/°C	0.0
Rin ^{†††}	channel resistance	Ohm	0.0
Rf ^{†††}	gate-source effective forward-bias resistance	Ohm	infinity [†]
Fc	forward-bias depletion capacitance coefficient (diode model)	None	0.5
Gscap	0=none, 1=linear, 2=junction, 3=Statz charge, 5=Statz cap	None	linear
Cgs ^{††}	zero-bias gate-source capacitance	F	0.0
Cgd ^{††}	zero-bias gate-drain capacitance	F	0.0
Rgd ^{†††}	gate drain resistance	Ohm	0.0
Gdcap	0=none, 1=linear, 2=junction, 3=Statz charge, 5=Statz cap	None	linear
Rd ^{††}	drain ohmic resistance	Ohm	fixed at 0
Rg	gate resistance	Ohm	fixed at 0
Rs ^{†††}	source ohmic resistance	Ohm	fixed at 0
Ld	drain inductance	H	fixed at 0.0
Lg	gate inductance	H	fixed at 0.0
Ls	source inductance	H	fixed at 0.0
Cds ^{††}	drain-source capacitance	F	0.0
Crf ^{††}	with Rds, models frequency dependent output conductance	F	0.0
Rds ^{†††}	additional output resistance for RF operation	Ohm	0.0
Gsfwd	0=none, 1=linear, 2=diode	None	linear
Gsrev	0=none, 1=linear, 2=diode	None	None
Gdfwd	0=none, 1=linear, 2=diode	None	None
Gdrev	0=none, 1=linear, 2=diode	None	linear
R1 ^{†††}	approximate breakdown resistance	Ohm	infinity [†]
R2 ^{†††}	resistance relating breakdown voltage to channel current	Ohm	fixed at infinity [†]

Vbi [†]	built-in gate potential	V	0.85
Vbr	gate-drain junction reverse bias breakdown voltage (gate- source junction reverse bias breakdown voltage with Vds < 0)	V	1e100
Vjr	breakdown junction potential		0.025
Is ^{† †}	gate junction saturation current (diode model)	A	1.0e-14
Ir	gate reverse saturation current	A	1.0e-14
Xti	Saturation Current Temperature Exponent	None	3.0
Eg	energy gap for temperature effect on Is	None	1.11
N	gate junction emission coefficient (diode model)	None	1
A5	time delay proportionality constant for Vds	None	fixed at 0.0
I _{max}	explosion current	A	1.6
I _{melt}	explosion current similar to I _{max} ; defaults to I _{max} (refer to Note 3)	A	defaults to I _{max}
Taumdl	Use 2nd order Bessel polynomial to model tau effect in transient: yes or no	None	no
Fnc	flicker noise corner frequency	Hz	0.0
R	gate noise coefficient	None	0.5
P	drain noise coefficient	None	1.0
C	gate-drain noise correlation coefficient	None	0.9
Vto	(not used in this model)	None	None
wVgfw	gate junction forward bias (warning)	V	None
wBvgs	gate-source reverse breakdown voltage (warning)	V	None
wBvgd	gate-drain reverse breakdown voltage (warning)	V	None
wBvds	drain-source breakdown voltage (warning)	V	None
wldsmax	maximum drain-source current (warning)	A	None
wPmax	maximum power dissipation (warning)	W	None
Kf	flicker noise coefficient	None	0.0
Af	flicker noise exponent	None	1.0
Ffe	flicker noise frequency exponent	None	1.0
AllParams	DataAccessComponent for file-based model parameter values	None	None
[†] Parameter value varies with temperature based on model Tnom and device Temp. ^{††} Parameter value scales with Area. ^{†††} Parameter value scales inversely with Area. [‡] A value of 0.0 is interpreted as infinity.			

- The Curtice cubic model is based on the work of Curtice and Ettenberg. Curtice3_Model contains most of the features described in Curtice's original paper plus some additional features that may be turned off. The following subsections review the highlights of the model. Refer to Curtice's paper [1] for more information.
- I_{max} and I_{melt} Parameters
I_{max} and I_{melt} specify the P-N junction explosion current. I_{max} and I_{melt} can be specified in the device model or in the Options component; the device model value takes precedence over the Options value.
If the I_{melt} value is less than the I_{max} value, the I_{melt} value is increased to the I_{max} value.
If I_{melt} is specified (in the model or in Options) junction explosion current = I_{melt}; otherwise, if I_{max} is specified (in the model or in Options) junction explosion current = I_{max}; otherwise, junction explosion current = model I_{melt} default value (which is the same as the model I_{max} default value).
- Use AllParams with a DataAccessComponent to specify file-based parameters (refer to "DataAccessComponent" in *Introduction to Circuit Components*). A nonlinear device model parameter value that is explicitly specified will override the value set by an AllParams association.

Equations/Discussion

Drain-Source Current

Drain current in Curtice3_Model is calculated with the following expression:

$$I_{ds} = I_{dso} \times \tanh(\text{Gamma} \times V_{ds}), \quad \text{Tau}_{NEW} = \text{Tau} + A5 \times V_{ds}$$

where:

$$I_{dso} = [A0 + A1 \times V_1 + A2 \times V_1^2 + A3 \times V_1^3] + (V_{ds} - V_{dsdc})/R_{ds0}$$

$$V_1 = V_{gs}(t - \text{Tau}_{NEW}) \times (1 + \text{Beta2} \times (V_{out0} - V_{ds})), \text{ when } V_{ds} \geq 0.0 \text{ V}$$

$$V_1 = V_{gd}(t - \text{Tau}_{NEW}) \times (1 + \text{Beta2} \times (V_{out0} + V_{ds})), \text{ when } V_{ds} < 0.0 \text{ V}$$

The latter results in a symmetrical drain-source current that is continuous at $V_{ds}=0.0 \text{ V}$. For values of V_1 below the internal calculated maximum pinchoff voltage V_{pmax} , which is the voltage at the local minimum of the function:

$$A0 + A1 \times n + A2 \times n^2 + A3 \times n^3$$

I_{dso} is replaced with the following expression:

$$I_{dso} = [A0 + A1 \times V_{pmax} + A2 \times V_{pmax}^2 + A3 \times V_{pmax}^3] + (V_{ds} - V_{dsdc})/R_{ds0}$$

If the I_{dso} value is negative (for $V_{ds} > 0.0\text{V}$), current is set to 0.

This implementation models the delay as an ideal time delay.

NOTE

When R_{ds0} is defaulted to 0, the term $(V_{ds} - V_{dsdc})/R_{ds0}$ is simply ignored and there is no divide by zero.

Junction Charge (Capacitance)

Two options are provided for modeling the junction capacitance of a device: to model the junction as a linear component (a constant capacitance); to model the junction using a diode depletion capacitance model. If a non-zero value of C_{gs} is specified and G_{scap} is set to 1 (linear), the gate-source junction will be modeled as a linear component. Similarly, specifying a non-zero value for C_{gd} and $G_{dcap}=1$ result in a linear gate-drain model. A non-zero value for either C_{gs} or C_{gd} together with $G_{scap}=2$ (junction) or $G_{dcap}=2$ will force the use of the diode depletion capacitance model for that particular junction. Note that each junction is modeled independent of the other; therefore, it is possible to model one junction as a linear component while the other is treated nonlinearly. The junction depletion charge and capacitance equations are summarized next.

Gate-Source Junction

For $V_{gc} < F_c \times V_{bi}$

$$Q_{gs} = 2 \times V_{bi} \times C_{gs} \times \left[1 - \sqrt{1 - \frac{V_{gc}}{V_{bi}}} \right]$$

$$Capacitance_{gs} = \frac{\partial Q_{gs}}{\partial V_{gc}} = \frac{C_{gs}}{\sqrt{1 - \frac{V_{gc}}{V_{bi}}}}$$

For $V_{gc} \geq F_c \times V_{bi}$

$$Q_{gs} = 2 \times V_{bi} \times C_{gs} \times [1 - \sqrt{1 - F_c}] + \frac{C_{gs}}{(1 - F_c)^{3/2}}$$

$$\times \left[\left(1 - \frac{3 \times F_c}{2} \right) \times (V_{gc} - F_c \times V_{bi}) \left(\frac{V_{gc}^2 - (F_c \times V_{bi})^2}{4 \times V_{bi}} \right) \right]$$

$$Capacitance_{gs} = \frac{\partial Q_{gs}}{\partial V_{gc}} = \frac{C_{gs}}{(1 - F_c)^{3/2}} \times \left[1 - \frac{3 \times F_c}{2} + \frac{V_{gc}}{2 \times V_{bi}} \right]$$

Gate-Drain Junction

For $V_{gd} < Fc \times V_{bi}$

$$Q_{gd} = 2 \times V_{bi} \times Cgd \times \left[1 - \sqrt{1 - \frac{V_{gd}}{V_{bi}}} \right]$$

$$Capacitance_{gd} = \frac{\partial Q_{gd}}{\partial V_{gd}} = \frac{Cgd}{\sqrt{1 - \frac{V_{gd}}{V_{bi}}}}$$

For $V_{gd} \geq Fc \times V_{bi}$

$$Q_{gd} = 2 \times V_{bi} \times Cgd \times \left([1 - \sqrt{1 - Fc}] + \frac{Cgd}{(1 - Fc)^{3/2}} \right)$$

$$\times \left(1 - \frac{3 \times Fc}{2} \right) \times \left(V_{gd} - F(c \times V_{bi}) + \frac{V_{gd}^2 - (Fbi)^2}{4 \times V_{bi}} \right)$$

$$Capacitance_{gd} = \frac{\partial Q_{gd}}{\partial V_{gd}} = \frac{Cgd}{(1 - Fc)^{3/2}} \times \left[1 - \frac{3 \times Fc}{2} + \frac{V_{gd}}{2 \times V_{bi}} \right]$$

Gate Forward Conduction and Breakdown

Keysight's implementation of the Curtice quadratic model provides a few options for modeling gate conduction current between the gate-source and gate-drain junctions. The simplest model is that proposed by Curtice for his cubic polynomial model (see Curtice3). This model assumes an *effective value* of forward bias resistance R_f and an approximate breakdown resistance R_1 . With model parameters $Gsfwd = 1$ (linear) and R_f reset to non-zero, gate-source forward conduction current is given by:

$$I_{gs} = (V_{gs} - V_{bi})/R_f \text{ when } V_{gs} > V_{bi}$$

$$= 0 \text{ when } V_{gs} \leq V_{bi}.$$

If $Gsfwd = 2$ (diode), the preceding expression for I_{gs} is replaced with the following diode expression:

$$I_{gs} = I_s \times \left[\exp\left(\frac{V_{gs}}{N \times v_t}\right) - 1 \right]$$

Similarly, with parameter $Gdfwd = 1$ (linear) and R_f set to non-zero, gate-drain forward conduction current is given by:

$$I_{gd} = (V_{gd} - V_{bi})/R_f \text{ when } V_{gd} > V_{bi}$$

$I_{gd} = 0$ when $V_{gd} \leq V_{bi}$.

If Gdfwd is set to 2 (diode), the preceding expression for I_{gd} is replaced with a diode expression:

$$I_{gd} = I_s \times \left[\exp\left(\frac{V_{gd}}{N \times v_t}\right) - 1 \right]$$

The reverse breakdown current (I_{dg}) is given by the following expression if R1 is set non-zero and Gdrev = 1 (linear):

$$I_{dg} = (V_{dg} - V_b)/R1 \text{ when } V_{dg} \geq V_b \text{ and } V_b > 0$$

$I_{dg} = 0$ when $V_{dg} < V_b$ or $V_b \leq 0$

$$V_b = V_{br} + R2 \times I_{ds}$$

If Gdrev is set to 2, the preceding I_{dg} expression is replaced with a diode expression:

$$I_{dg} = -I_r \times \left[\exp\left(\frac{V_{dg} - V_b}{V_{jr}}\right) - 1 \right]$$

With Gsrev = 1 (linear) and R1 set to non-zero, the gate-source reverse breakdown current I_{gs} is given by the following expression:

$$I_{gs} = (V_{sg} - V_b)/R1 \text{ when } V_{sg} \geq V_{bi} \text{ and } V_b > 0$$

$I_{gs} = 0$ when $V_{sg} \leq V_{bi}$ or $V_b \leq 0$

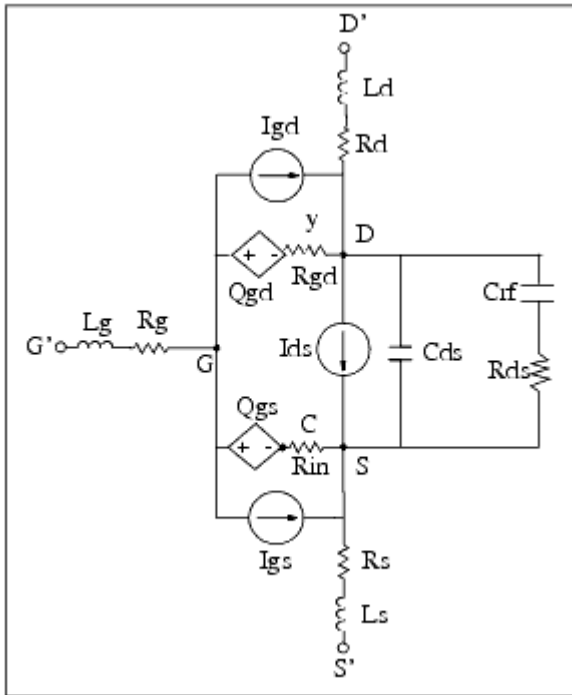
If Gsrev is set to 2, the preceding I_{gs} expression is replaced with a diode expression.

$$I_{gs} = -I_r \times \left[\exp\left(\frac{V_{sg} - V_b}{V_{jr}}\right) - 1 \right]$$

When the diode equations are both enabled, the DC model is symmetric with respect to the drain and source terminals. The AC model will also be symmetric if, in addition to the latter, $C_{gs}=C_{gd}$.

High-Frequency Output Conductance

Curtice3_Model provides the user with two methods of modeling the high frequency output conductance. The series-RC network dispersion model (**Curtice Cubic Model**) is comprised of the parameters Crf and Rds and is included to provide a correction to the AC output conductance at a specific bias condition. At a frequency high enough such that Crf is an effective short, the output conductance of the device can be increased by the factor $1/R_{ds}$. (Also see [2]).



Curtice Cubic Model

Temperature Scaling

The model specifies T_{nom} , the nominal temperature at which the model parameters were calculated or extracted. To simulate the device at temperatures other than T_{nom} , several model parameters must be scaled with temperature. The temperature at which the device is simulated is specified by the device item $Temp$ parameter. (Temperatures in the following equations are in Kelvin.)

The saturation current I_s scales as:

$$I_s^{NEW} = I_s \times \exp \left[\left(\frac{Temp}{T_{nom}} - 1 \right) \frac{q \times E_g}{k \times N \times Temp} + \frac{X_{ti}}{N} \times \ln \left(\frac{Temp}{T_{nom}} \right) \right]$$

The gate depletion capacitances C_{gs} and C_{gd} vary as:

$$C_{gs}^{NEW} = C_{gs} \left[\frac{1 + 0.5[4 \times 10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + 0.5[4 \times 10^{-4}(T_{nom} - T_{REF}) - \gamma^{T_{nom}}]} \right]$$

$$C_{gd}^{NEW} = C_{gd} \left[\frac{1 + 0.5[4 \times 10^{-4}(Temp - T_{REF}) - \gamma^{Temp}]}{1 + 0.5[4 \times 10^{-4}(T_{nom} - T_{REF}) - \gamma^{T_{nom}}]} \right]$$

where y is a function of junction potential and energy gap variation with temperature.
The gate junction potential V_{bi} varies as:

$$V_{bi}^{NEW} = \frac{Temp}{T_{nom}} \times V_{bi} + \frac{2k \times Temp}{q} \ln \left(\frac{n_i^{T_{nom}}}{n_i^{Temp}} \right)$$

where n_i is the intrinsic carrier concentration for silicon, calculated at the appropriate temperature.
The cubic polynomial coefficients A_0 , A_1 , A_2 , and A_3 vary as:

$$\Delta = V_{totc}(Temp - T_{nom})$$

$$A_0^{NEW} = (A_0 - \Delta \times A_1 + \Delta^2 \times A_2 - \Delta^3 \times A_3) \times 1.01^{Betatce(Temp - T_{nom})}$$

$$A_1^{NEW} = (A_1 - 2\Delta \times A_2 + 3\Delta^2 \times A_3 - \Delta^3 \times A_3) \times 1.01^{Betatce(Temp - T_{nom})}$$

$$A_2^{NEW} = (A_2 - 3\Delta \times A_3) \times 1.01^{Betatce(Temp - T_{nom})}$$

$$A_3^{NEW} = (A_3) \times 1.01^{Betatce(Temp - T_{nom})}$$

If $Betatc = 0$ and $Idstc \neq 0$

$$I_{ds}^{NEW} = I_{ds} \times (1 + Idstc \times (Temp - T_{nom}))$$

Noise Model

Thermal noise generated by resistors R_g , R_s and R_d is characterized by the spectral density:

$$\frac{\langle i^2 \rangle}{\Delta f} = \frac{4kT}{R}$$

Parameters P , R , and C model drain and gate noise sources.

$$\frac{\langle i_d^2 \rangle}{\Delta f} = 4kTg_m P + 4kTg_m PFnc / f + Kf I_{ds}^{Af} / f^{Ffe}$$

$$\frac{\langle i_g^2 \rangle}{\Delta f} = 4kT C_{gs}^2 \omega^2 R / g_m$$

$$\frac{\langle i_g, i_d^* \rangle}{\Delta f} = 4kTj C_{gs} \omega \sqrt{PR} C$$

For Series IV compatibility, set $P=2/3$, $R=0$, $C=0$, and $Fnc=0$; copy Kf , Af , and Ffe from the Series IV model.

Calculation of V_{to} Parameter

The V_{to} parameter is not used in this model. Instead, it is calculated internally to avoid the discontinuous or non-physical characteristic in i_{ds} versus v_{gs} if A_0 , A_1 , A_2 , A_3 are not properly extracted.

For a given set of A_s , ADS will try to find the maximum cutoff voltage (V_{pmax}), which satisfies the following conditions:

$$f(V_{pmax}) = A_0 + A_1 \times V_{pmax} + A_2 \times V_{pmax}^2 \times 2 + A_3 \times V_{pmax}^3 \times 3 \leq 0$$

first derivative of $f(V_{pmax}) = 0$ (inflection point)

second derivative of $f(V_{pmax}) > 0$ (this is a minimum)

If V_{pmax} cannot be found, a warning message is given *cubic model does not pinch off*.

During analysis, the following are calculated:

$$v_c = v_{gs} \times (1 + \text{Beta2} \times (V_{out0} - v_{ds}))$$

$$i_{ds} = ((A_0 + A_1 \times v_c + A_2 \times v_c^2 + A_3 \times v_c^3) + (v_{ds} - V_{dsdc}) / R_{ds0}) \times \tanh(\text{Gamma} \times v_{ds})$$

If $i_{ds} < 0$ then sets $i_{ds} = 0$.

If $i_{ds} > 0$ and $V_c \leq V_{pmax}$ then calculates i_{vc} as follows:

$$i_{vc} = (f(V_{pmax}) + (v_{ds} - V_{dsdc}) / R_{ds0}) \times \tanh(\text{Gamma} \times v_{ds})$$

If $i_{vc} > 0$ then sets $i_{ds} = i_{vc}$ and gives a warning message *Curtice cubic model does not pinch off, I_{ds} truncated at minimum*.

$$\text{else set } i_{ds} = 0$$

To ensure the model is physical and continuous, it is important to obtain a meaningful set of A_s that V_{pmax} can be found.

Additional Information

References

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