A Novel SiGe PIN Diode SPST Switch for Broadband T/R Module

Pinping Sun, *Student Member, IEEE*, Parag Upadhyaya, *Student Member, IEEE*, Dong-Ho Jeong, *Member, IEEE*, Deukhyoun Heo, *Member, IEEE*, and George S. La Rue, *Member, IEEE*

***Abstract*—A novel octagonal SiGe p-type intrinsic n-type (PIN) diode single pole single throw (SPST) switch is first implemented in a standard 0.18-μm SiGe BiCMOS technology. Distinctive radio frequency performance of monolithic silicon PIN diode switch is achieved for broadband applications with improvement of its geometry. Over the 2–16 GHz frequency band, the PIN diode SPST switch exhibits an insertion loss of less than 1 dB and isolation between 42 dB to 19 dB. An accurate small signal model of series PIN diode is also presented.**

***Index Terms*—Diode, phased array communication systems, PIN diode, SiGe BiCMOS system-on-chip (SOC), transmit/receive (T/R) module.**

I. Introduction

THE rapid growth of satellite communications systems such as satellite radio, TV, broadband internet, and GPS service have driven the proliferation of low cost, light-weight, and reconfigurable phased array communication systems. A high level of integration with a reduced number of off-chip components is the key for low cost satellite and other mobile platforms to transmit and receive real time information. In the past, the high performance transmit/receive (T/R) modules in phased array communication systems were commonly implemented in III–V compound semiconductor technology, such as GaAs or InP [1]. However, the high cost of these materials is prohibitive to the commercialization of an integrated T/R module. Silicon CMOS technology is a low cost and low power alternative, but its performance in X band is limited [3]. Low cost and high performance SiGe BiCMOS technology is more radiation tolerant than CMOS counterpart [2], [3] and is better suited for satellite applications. Therefore, SiGe BiCMOS is the most suitable technology for the implementation of high performance system-on-chip (SoC) T/R modules for phased array communication systems.

For the next generation T/R module in the phased array communication systems, high isolation and low insertion loss switch is an essential building block. A robust PIN diode can be used to achieve high isolation backend radio frequency (RF) switches, variable attenuators and phase shifters. Previously, a square SiGe PIN diode was implemented in a 0.5-μm standard BiCMOS process [4]. An improved SiGe PIN diode structure is presented in this letter to cover applications in X and Ku frequency bands. Insertion loss is improved by employing an octagonal geometry and a larger subcollector contact area to lower resistances. The PIN diode was fabricated using the standard 0.18-μm IBM 7 HP SiGe BiCMOS process, which allows for high levels of integration.

The design of the octagonal PIN diode is discussed in Section II. Measurement results showing state-of-the-art performance are presented in Section III along with a fitted small signal lumped-element model.

Manuscript received October 31, 2006; revised February 23, 2007. This work was supported by the Air Force Research Laboratory.

P. Sun, P. Upadhyaya, D. Heo, and G. S. La Rue are with the School of Electrical Engineering, Washington State University, Pullman, WA 99164-2752 USA (e-mail: dheo@eecs.wsu.edu).

D.-H. Jeong is with The School of Electronic Engineering, Dongyang University, Yeongju 750-711, Korea (e-mail: dhjeong@dyu.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LMWC.2007.895706

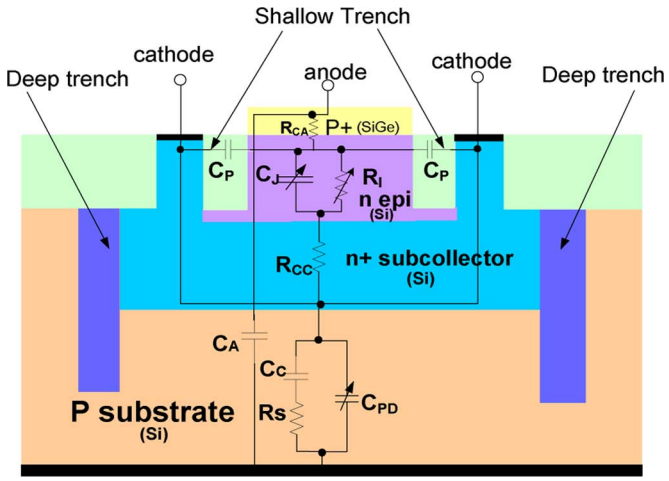

Fig. 1. PIN diode cross section structure.

II. PIN Diode Design

A PIN diode switch is formed by highly doped $P+$ (anode) and $N+$ junction (cathode) with lightly doped intrinsic (I) region. In a standard 0.18-μm SiGe BiCMOS process, the PIN diode is realized with HBT material layers: the $P+$ base layer, the n-collector layer and the buried $n+$ subcollector layer as shown in Fig. 1. The relationships of the equivalent-circuit model to the physical parameters of the PIN diode are also described. C_A and C_C are anode and cathode to substrate capacitance, respectively. C_P is the parasitic capacitance between the anode and cathode port. R_C is the contact resistance which consists of anode contact resistance $R_{\rm CA}$ and cathode contact resistance $R_{\rm CC}$. R_I is the current based resistance, C_J is the junction capacitance in the intrinsic region and R_S is the parasitic resistance in the p-substrate. $C_{\rm PD}$ is the capacitance of the parasitic Nwell-Psub diode that varies with bias voltage.

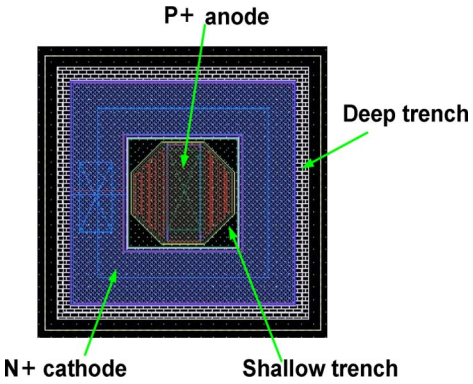

Fig. 2. Octagonal PIN diode.

In a low power satellite phased array communication system, low insertion loss devices are extremely desirable. A minimized forward-bias resistance can help to achieve low insertion loss in the PIN diode. The total forward bias resistance R_F consists of the contact resistance R_C and current dependent resistance R_I [4]. The R_I is given by

$$R_I = \frac{l_i^2}{2\mu\tau I_{\rm dc}} \tag{1}$$

where l_i, the thickness of intrinsic region, μ, the average electron and hole mobility, are predefined by the process. In this design, by optimizing the geometry of PIN diode, the effective minority carrier lifetime τ, is improved to achieve reduced current based resistance, and thus, a low insertion loss at low dc current level. The optimization method is based on the reverse proportional relationship between the τ and PIN diode's periphery-to-area ratio (P/A). As (2)–(4) describes, the minority carrier recombination from the $P+/I$ interface and the periphery is the main factor affecting τ because there are more dislocations located at the interface and the periphery than in the bulk region [5]

$$R_{\rm eff} = R_{\rm bulk} + R_{\rm perim} + R_{\rm interface} \tag{2}$$

$$\frac{p-p_0}{\tau}A \approx \frac{p-p_0}{\tau_{\rm interface}}A + \nu_{\rm perim}(p-p_0)P \tag{3}$$

$$\frac{1}{\tau} \approx \frac{1}{\tau_{\rm interface}} + \nu_{\rm perim}\left(\frac{P}{A}\right) \tag{4}$$

where $R_{\rm eff}$ is the effective recombination rate of the device, $R_{\rm bulk}$ is the bulk minority carrier recombination rate, $R_{\rm perim}$ is the periphery normalized minority carrier recombination rate, $R_{\rm interface}$ is the recombination rate at the SiGe/Si interface, $p-p_0$ is the excess minority carrier concentration on the n-side of the junction, $\tau_{\rm interface}$ is the $P+/I$ interface minority carrier lifetime and $\nu_{\rm perim}$ is the effective hole surface recombination velocity. The interface recombination is determined by the process, but the PIN diode geometry is custom-tailored in this design to achieve a small periphery-to-area ratio, and longer minority carrier lifetime.

Compared with the rectangular anode region (1.25 μm $\times$ 5 μm with $P/A = 2 \times 10^4$ cm^{-1}) and the square anode region (2.5 μm $\times$ 2.5 μm with $P/A = 1.62 \times 10^4$ cm^{-1}) PIN diodes [2], the octagonal PIN diode anode region, shown in Fig. 2, (6.25 μm^2 with $P/A = 1.48 \times 10^4$ cm^{-1}), became our considerate selection due to its smallest P/A for a given cross-sectional area of 6.25 μm^2 [6]. The octagonal PIN diode was implemented in a SiGe process due to process limitation, though a circular one has the smallest P/A. The octagonal PIN diode improves the PIN diode's minority carrier lifetime, which helps to reduce the forward bias resistance and lower the insertion loss. For the 6.25 μm^2 PIN diode, with an average $v_{\rm perim}$ of 8000 cm/s and $\tau_{\rm interface}$ of 10 ns [7], the reduced P/A increases $\tau_{\rm eff}$ by 19% and 6% compared to the rectangular and square layout, respectively. Additionally, in the proposed octagonal PIN diode layout, the total subcollector contact area is increased resulting in reduced contact resistance and forward bias resistance, and therefore, lower insertion loss.

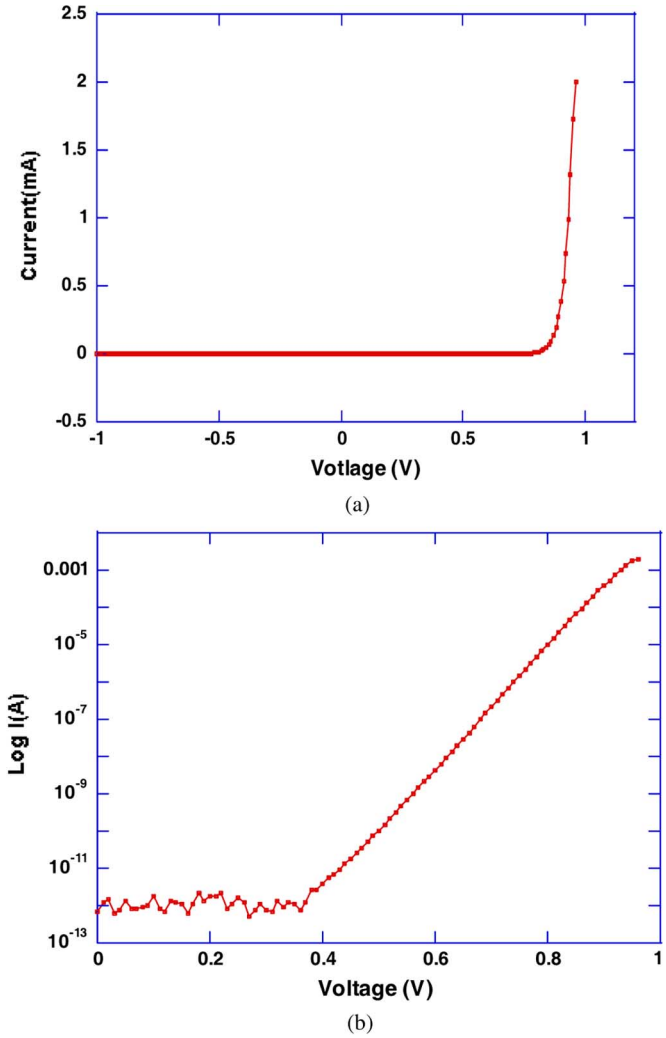

Fig. 3. (a) dc I–V characteristic and (b) log current versus voltage of 6.25-μm^2 shunt PIN diode.

III. Measurement Results

Fig. 3 shows the dc measurement performance of a 6.25 μm^2 shunt PIN diode. The measured saturation current I_s is 2.1×10^{-21} A and the junction reverse breakdown voltage V_b is -11 V at $T = 300$ K, respectively. The reverse saturation current is only around 10^{-12} A; this parameter is significantly smaller than 10^{-8} A reported in [4] and gives an ideality factor of 1.008.

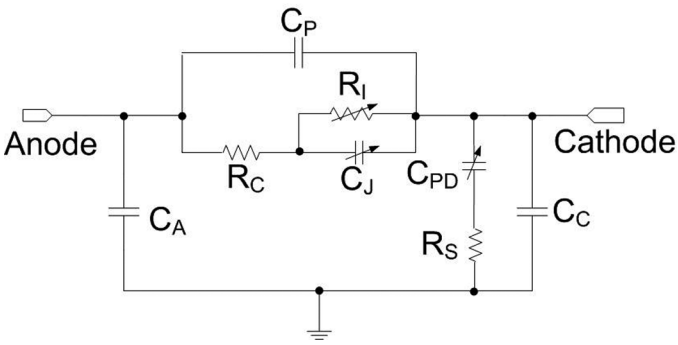

Fig. 4. Equivalent circuit model of the PIN diode.

TABLE I
SERIES SWITCH MODEL PARAMETERS OF 6.25 μM^2 PIN DIODE

	ON (I_{FB} = 2 mA)	OFF(V_{RB}=1.5 V)
R_C	1.035 Ω	1.035 Ω
R_I	2.001 Ω	100 MΩ
C_J	2.005 pF	0.007 pF
C_P	0.001 pF	0.001 pF
C_A	0.0001 pF	0.0001 pF
C_{PD}	0.021 pF	0.012 pF
R_S	1203 Ω	1203 Ω
C_C	0.061 pF	0.061 pF

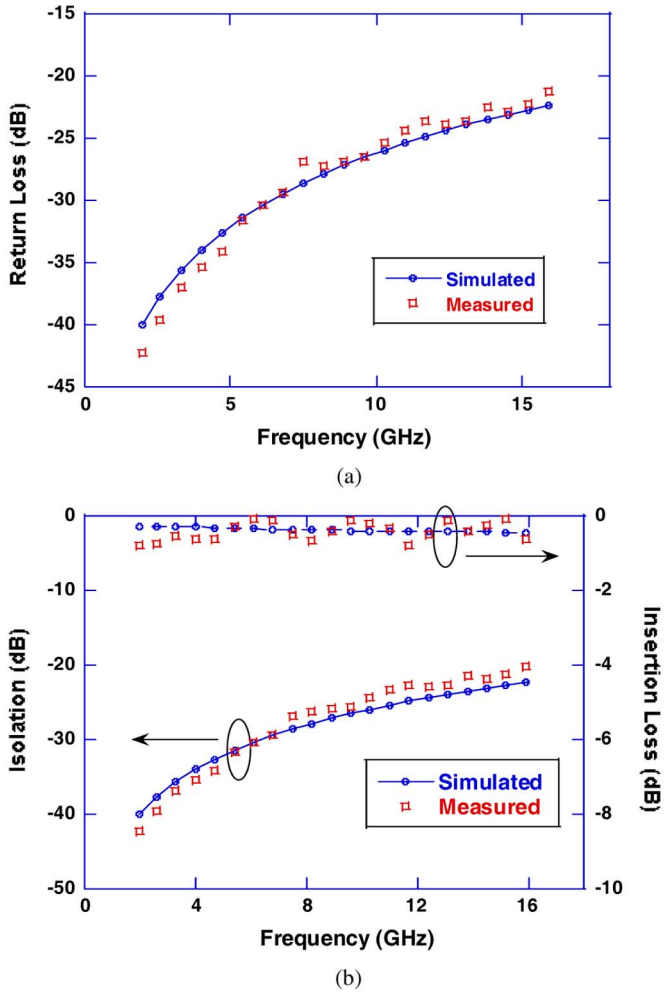

Fig. 5. Simulated and measured results of series PIN diode switch (a) return loss and (b) insertion loss and isolation.

A PIN diode model was derived from small signal S-parameters measured using on-wafer RF probes. The forward bias model was derived for $I_{\rm FB} = 2$ mA. The reverse bias model was obtained at the reverse bias voltage of 1.5 V. Fig. 4 shows the lumped element model and Table I shows the model component values for the 6.25 μm^2 octagonal PIN diode.

Fig. 5 shows the RF measurements of the return loss, insertion loss and isolation for a series switch using a 6.25-μm^2 PIN diode. At 16 GHz, the input return loss is -22 dB, which is excellent. The single pole single throw (SPST) switch achieves insertion loss lower than 1 dB and isolation between 42 dB and 19 dB over a frequency band from 2 to 16 GHz. The proposed PIN diode model correlates well with measured data as shown in Fig. 5. The measured output $P_{1\rm dB}$ is 5.4 dBm for a 6.25-μm^2 PIN diode at $I_{\rm FB} = 2$ mA.

IV. CONCLUSION

A high performance novel octagonal PIN diode SPST switch for broadband T/R module is demonstrated in a standard 0.18-μm SiGe BiCMOS process. With the proposed geometry, an improvement of PIN diode's reverse saturation current, insertion loss, and isolation is achieved. Over 2–16 GHz, the PIN SPST RF switch can achieve an insertion loss of less than 1 dB and isolation between 42 dB to 19 dB. To the author's knowledge, this is the best monolithic PIN diode switch on a 0.18-μm SiGe BiCMOS tchnology reported to date. Integration of the PIN diode SPST switch with other RF components is a feasible option for achieving fully integrated low cost system-on-chip T/R module for phased array communication systems in satellite and other mobile applications.

REFERENCES

[1] J. A. Torres and J. C. Freire, "Monolithic transistors SPST switch for L-band," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 51–56, Jan. 2002.
[2] J. D. Cressler, "SiGe HBT reliability issues associated with operation in extreme environments," in *IEEE SIRF Tech. Dig.*, Jan. 2006, pp. 3–7.
[3] Z. Li and K. K. O. , "15-GHz Fully Integrated NMOS switches in a 0.13-μm CMOS process," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2323–2328, Nov. 2005.
[4] R. Tayrani, M. A. Teshiba, G. M. Sakamoto, Q. Chaudhry, R. Alidio, Y. Kang, I. S. Ahmad, T. C. Cisco, and M. Hauhe, "Broad-band SiGe MMICs for phased-array radar applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 9, pp. 1462–1471, Sep. 2003.
[5] P. G. Neudeck, "Perimeter governed minority carrier lifetimes in 4H-SiC p + n diodes measured by reverse recovery switching transient analysis," *J. Electron. Mater.*, vol. 27, pp. 17–323, 1998.
[6] P. Sun, L. Wang, P. Upadhyaya, and D. Heo, "High isolation 10 GHz to 20 GHz SPDT switch design using novel octagonal PIN diode structure," in *Proc. IEEE Workshop Microelectron. Electron Devices*, Apr. 2005, pp. 38–41.
[7] F. Hirose, K. Kurita, Y. Takahashi, and M. Mukaida, "Operation mechanism on SiGe/Si/Si PIN diodes explained using numerical simulation," *Electrochem. Solid State Lett.*, vol. 8, no. 7, pp. G160–G163, 2005.