Impact of Surface Effects on RF Switching PIN Diodes

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***Abstract*— This paper presents a study of the impact of surface conditions on PIN diode resistance and carrier lifetime. The discussion shows that large radius PIN diodes exhibit less impact from surface conditions than do smaller radius devices. Knowledge of this feature is important for microwave and RF design engineers working in both high and low power applications. PIN diodes used in high power applications often need to be of wider radius to handle the larger current densities associated with the high-power operation, and so see a reduction of influence from the surface. PIN diodes in receive applications, where small cross section devices are often used, will see an associated greater influence of the surface on their operation. The advantage of the smaller radius device is that the capacitance of the device will be lower, impacting the upper frequency limit that these devices may be used. The discussion is verified with a series of measurements on carrier lifetime and resistance of PIN diodes of various geometries.**

Keywords—PIN diode, switching, resistance, surface effects

I. INTRODUCTION

PIN diodes are used in a large variety of RF control applications, spanning the range of antenna transmit/receive switching to component switching in automated impedance matchers to receiver protectors. For the RF circuit designer, the two most important parameters for the PIN diode are its on-state resistance and its off-state capacitance, both of which are contributors to the broadband switch cutoff frequency figure of merit. For the on-state resistance, a combination of I-region width (W), carrier lifetime (τ) and DC forward current (I_{DC}) play a role in determining the resistance value, with smaller W and larger τ and I_{DC} yielding lower resistance values. For the off-state, the capacitance is the primary metric of interest with W and the diode radius R (and hence area) governing the capacitance value. Smaller R and wider W devices yield lower capacitance values. Parameters such as W and R often play counteracting roles, where the increase of one dimension for lower resistance, for example, comes at the expense of higher capacitance. In addition to these diode geometry factors, the role of the diode's semiconductor surface also needs to be considered as it impacts the overall charge concentration in the I-region. Surface states, and their attendant surface recombination velocity, can be passivated with various surface coatings, with each type of surface passivation impacting the surface in different ways. Studies have shown [1, 2] that surface effects can have a role in reducing the carrier lifetime from its bulk value τ_{bulk} to a lower effective value τ_{eff}, which will ultimately impact resistance. In addition, the diode geometry factors radius R_0 and I-region thickness W can also play a role in the surface's impact on τ, with larger radius diodes having lower impact on the lifetime τ_{eff}, since the surface is farther from the PIN diode core. These surface effects impact traditional discrete mesa-style PIN diodes which can be modeled assuming they are cylindrical in shape, as well as fully integrated PIN diodes which may exhibit asymmetric surface impacts due to surface and substrate interactions simultaneously, as discussed in a previous work [3].

II. THEORY AND SIMULATION

A. Time-Domain PIN Diode Model

PIN diode resistance is strongly related to the charge stored in the I-region. The traditional PIN diode resistance expression shows this relationship in (1); increases in I-region stored charge Q yield a lower diode resistance for a given I-region thickness W:

$$R_S = \frac{W^2}{2\mu_a I_{dc}\tau} = \frac{W^2}{2\mu_a Q} \tag{1}$$

where μ_a is the ambipolar mobility. From (1), it is seen that any factor associated with the PIN diode that reduces the overall stored charge Q in the I-region will tend to increase the on-state resistance. For switching applications, this unanticipated increase in resistance will lead to additional loss. Therefore, the PIN diode charge density needs to be studied carefully.

The traditional method of computing the carrier density is based on the carrier transport equation as shown in (2):

$$\nabla^2 n(r,z) + \frac{n(r,z)}{L^2} = 0 \tag{2}$$

where L is the bulk recombination length computed as $L^2 = D_a\tau_{bulk}$, D_a is the ambipolar diffusivity and τ_{bulk} is the bulk carrier lifetime. Closed form solutions of the carrier density *n(r,z)* in cylindrically shaped PIN diodes (the most common form of discrete device) yield a Bessel function of the first kind solution for the radial component (r) and a complex function along the I-region axis (z). The first boundary condition assumes full recombination of carriers at the surface [$n(R_0,z)=0$] (infinite surface recombination velocity) and provides a worst-case solution to (2) in the radial direction. The second boundary condition relates the gradient of the charge density in the z-direction to the DC injected current I:

$$I_{dc} = -qAD_a\left(\frac{dn}{dz}\right)_{z=0} = qAD_a\left(\frac{dn}{dz}\right)_{z=W} \tag{3}$$

and by using the definition of hyperbolic functions, the carrier density can be written as:

$$n(r,z) = J_0\left(\frac{2.408}{R_0}r\right)\left(\frac{\cosh(\alpha z)+\cosh(\alpha z-\alpha W)}{\sinh(\alpha W)}\right) \quad (4)$$

where $\alpha^2=(1/L^2+k^2)$ and $k = 2.408/R_0$.

This result was compared with numerical simulations for identical conditions in the PIN diode [2, 3]. Fig. 1 shows a comparison of the carrier density at the P-I boundary as a function of position away from the diode core (R=0) for identical PIN diodes of I_{DC} = 10 mA, R_0= 2,250 µm, and W= 75 µm (R/W=30). These results show that the theoretical calculations overestimate the carrier density in the core of the device, whereas the numerical simulations show a relatively constant I-region carrier density except within a few recombination lengths L of the surface.

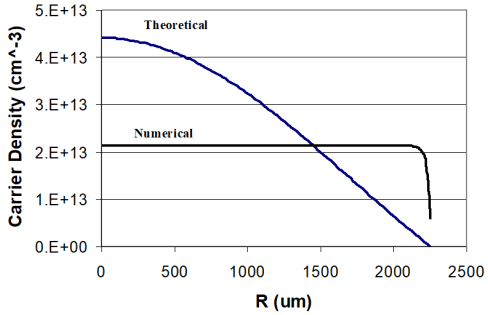

Fig. 1. Carrier density at PI boundary as a function of distance from diode core.

This large difference between the two approaches shows that the overall stored charge in the I-region will be overestimated by the theory, leading to a lower resistance and higher carrier lifetime than is actually the case. In general, the carrier density is complex as shown by numerical modeling in Fig. 2, with small variations in the carrier density between the P-I and I-N junctions, but with significant changes in the carrier density as one approaches the surface.

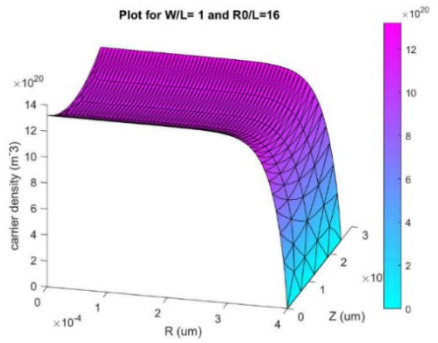

Fig. 2. Carrier density as a function of distance from the junctions and surface of a PIN diode [2].

The impact of geometry on the carrier lifetime as a function of geometry was explored by numerical simulations of the stored charge at fixed DC current with infinite surface recombination. Fig. 3 shows the ratio of the effective carrier lifetime to the bulk carrier lifetime ratio τ_{eff}/τ_{bulk} as a function of the normalized radius with respect to intrinsic region thickness R/W for various normalized I-region widths (normalized to the recombination length L). Fig. 3 shows that for large I-region width and large radius devices as might be used in high power control applications (on the transmit side of a system for example), the effective carrier lifetime approaches the bulk carrier lifetime. Conversely, smaller radius PIN diodes will exhibit lower capacitance values and are useful in receiving applications will suffer the largest impact on carrier lifetime, with a subsequent reduction in carrier lifetime and I-region stored charge, with a resulting increase in the device resistance.

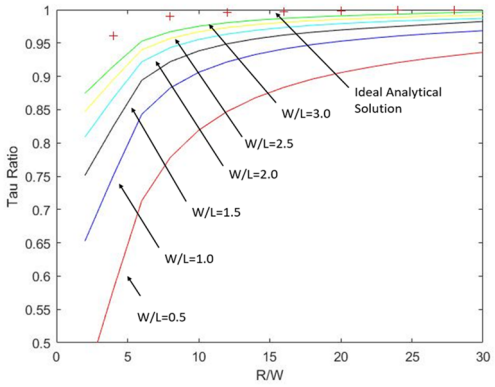

Fig.3. Carrier lifetime ratio τ_{eff}/τ_{bulk} versus normalized PIN diode radius (normalized to the PIN diode radius W) using W/L as a parameter. The plus signs (+) are from the theoretical solution in (4) [2]

The effect of surface conditions can also be seen in the resistance as shown in Fig. 4. This figure shows the resistance of an ideal PIN diode with infinite surface recombination velocity as a function of normalized diode radius and I-region width (R/W and W/L, respectively) at 10 mA DC forward current. As shown in the figure, PIN diode resistance can vary by more than 10% over a wide range of radii.

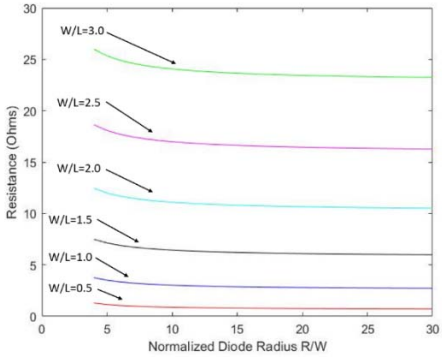

Fig. 4. PIN diode resistance as a function of normalized geometrical parameters at 10 mA DC forward current [2]

III. Measurements and Discussion

The theoretical and simulation results show that PIN diodes will exhibit variations because of the surface. These studies indicate that wider devices, such as used in high power applications, will see lower impact from the surface.

Measurements of PIN diodes with different radii (R) and I-region widths (W) the observations from the simulations. These results are shown in Fig. 5 and indicate that larger radius PIN diodes (larger R/W) exhibit longer carrier lifetimes than smaller R/W devices, with resulting lower resistances (solid curves - lifetime, dotted lines - resistance. Same color curves correspond to the same device). Larger radius diodes have higher effective carrier lifetime as the effects of the surface diminish. Thinner devices, such as used in receiver applications, show more impact from the surface.

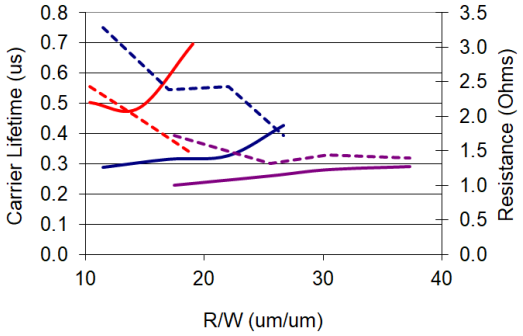

Fig. 5. Measured PIN diode carrier lifetime and resistance as a function of normalized geometrical parameters at 10 mA DC forward current [from 3]

Measurements were also performed on gallium arsenide (GaAs) PIN diodes. These devices exhibit relatively small carrier lifetimes which as previous work has shown [4, 5] provides a higher frequency minimum (f_{min}) in their reactive component (neglecting the device/package inductance). Fig. 6 and 7 show resistance and reactance measurements of a GaAs PIN diode at 1 and 10 mA DC forward current. Indicated in the curves is the reactance minimum, where the carrier lifetime can be computed using the expression from [4]:

$$\tau_{bulk} = \frac{1}{2\pi f_{min}} \quad . \qquad (4)$$

The effective carrier lifetime shown in Figs. 6 and 7 decreases with increasing DC bias and needs further investigation.

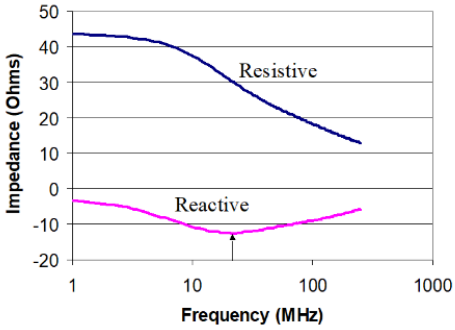

Fig. 6. Measured PIN diode resistance at reactance at 1 mA DC forward current. The reactance minimum occurs at approximately 22 MHz, indicating an effective carrier lifetime of 7.2 ns.

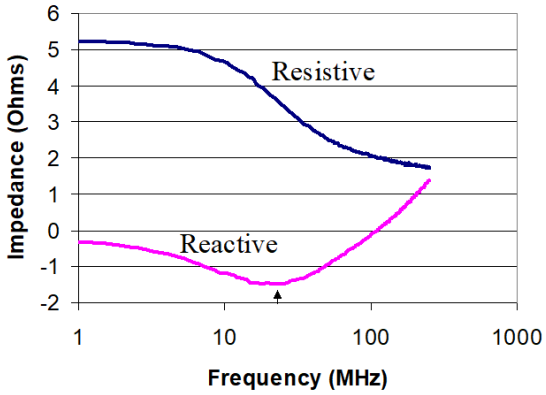

Fig. 7. Measured PIN diode resistance at reactance at 1 mA DC forward current. The reactance minimum occurs at approximately 24 MHz, indicating an effective carrier lifetime of 6.6 ns.

IV. Conclusion

This paper presented the results of a study on the impact of surface conditions on PIN diode resistance. The analysis showed that large radius PIN diodes show less impact from surface conditions than do smaller radius devices. This phenomenon is important for both high and low power applications since PIN diodes in high power applications often need to be of wider radius to handle the larger current densities associated with the high-power operation. This would indicate that these applications will see much less influence of surface conditions than smaller radius devices. Receive applications, where small cross section devices can be used, will see an associated greater influence of the surface on their operation. The advantage of the smaller radius device is that the capacitance of the device will be lower, potentially impacting the upper frequency limit that these devices may be used. The simulation results were verified with a series of measurements. Further work needs to be done looking at the impact of higher current densities in the devices as measurements also show a reduction in carrier lifetime as DC current increases.

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