# Vertical p–i–n Polysilicon Diode With Antifuse for Stackable Field-Programmable ROM

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***Abstract*—A field-programmable, stackable memory cell using 0.15-$\mu$m technology is demonstrated. Vertical polycrystalline silicon diodes are stacked on top of one another, with tungsten (with TiN adhesion film) interconnect wires. An $SiO_2$ antifuse film separates the top of each diode from the TiN–W films. The cell is programmed when sufficient biasing voltage is applied to break down the antifuse, connecting the diode to tungsten. The cell is unprogrammed when the antifuse is intact. Cell fabrication and performance are described.**

***Index Terms*—Antifuse, breakdown, p–i–n diode, polysilicon, read-only memories (ROMs).**

## I. Introduction

A STACKABLE, field-programmable, read-only memory (ROM) cell using 0.15-$\mu$m technology is described. The cell can be manufactured entirely with existing silicon-based complementary metal–oxide–semiconductor (CMOS) fabrication tools and materials. With a single cell size of $4F^2$, where $F$ is the minimum feature size, and read/write transistors located *underneath* arrays of memory cells, an effective density for eight layers of memory bits is $4F^2/8$ or $0.5F^2$, enabling a very large density of bits per mm$^2$ of silicon wafer. The cells have an additional advantage over mask ROM technology by enabling the programming of die in the field instead of the fabrication facility.

The cell described in this letter is an improvement on similar, previously described cells. By stacking the cells on top of one another, we achieve higher density than single-plane devices [1]. By achieving a larger current difference between programmed and unprogrammed states, we have a larger tolerance for manufacturing variance. By separating the etch and insulating oxide gap fill of the wiring interconnects from the etch and insulating oxide gap fill of the silicon-based cells, the aspect ratio for gap fill is minimized, enabling scaling of the technology to smaller dimension with minimal change in tool sets [2]–[4]. The cells are shown in schematic in Fig. 1. Vertical polycrystalline silicon (polysilicon) diodes are stacked on top of one another, with tungsten (on a TiN adhesion film) interconnect wires in between. The diodes "point" in the opposite direction for each layer, allowing for a simpler read/write circuit architecture, allowing the cells to share wiring lines and minimizing the possibility of disturb events during programming. An $SiO_2$ antifuse film separates the top of each diode from the tungsten interconnect. The cell is unprogrammed when the antifuse is intact. The cell is programmed when sufficient biasing voltage is applied to break down the antifuse, connecting the diode to tungsten. We describe the fabrication and performance of the cells in this letter.

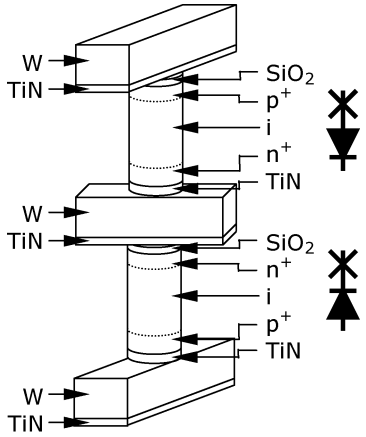


Fig. 1. Schematic of two memory cells with diodes "pointing" in opposite directions.

## II. Device Processing

Cells were fabricated on 200–mm silicon wafers. Read/write transistors were fabricated by CMOS processing and insulated from the memory cells above by planarized $SiO_2$. The main topic of this letter is the memory cell, and the transistors are fabricated from standard processing, thus, we will not discuss transistor fabrication. The transistors applied 10 V to the memory cells for programming and the cells were "read" at 2 V. After transistor fabrication, two layers of etched tungsten films (with TiN adhesion layers) were used to make horizontal and vertical interconnects from the transistors to the memory arrays.

Memory cell fabrication and wiring interconnects between the memory cells proceeded after interconnect fabrication from the transistor devices. Wiring layers between memory cells were made by etching 1500-Å–thick tungsten lines (with a 200-Å-thick TiN adhesion layer underneath) and depositing $SiO_2$ by high-density plasma-enhanced chemical vapor deposition (HDPCVD) as an insulator between and on top of the etched tungsten lines. Chemical–mechanical polishing (CMP) then removed the oxide from the top of the tungsten lines and planarized the surface. The high removal rate of $SiO_2$ and low

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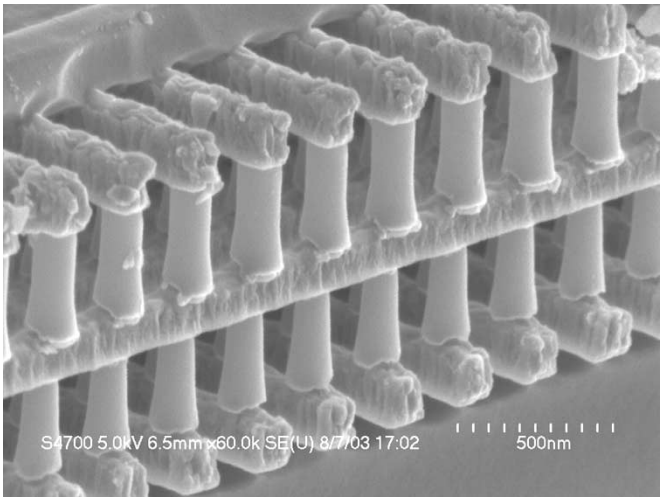


Fig. 2. SEM micrograph of two layers of memory cells with tungsten interconnects. Insulating $SiO_2$ has been etched to reveal structure. The die has been fractured in an array of cells.

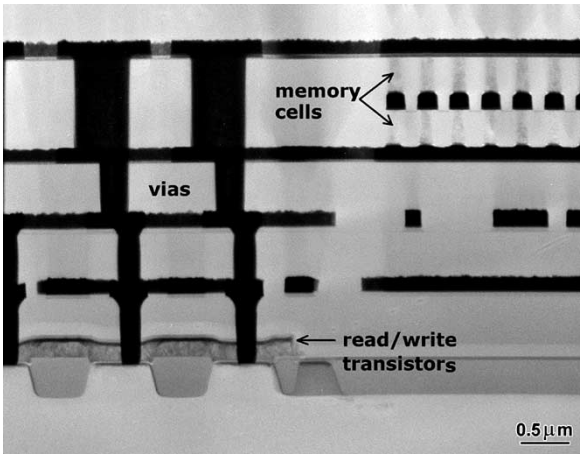


Fig. 3. Cross-sectional transmission electron microscope micrograph showing the major components of the memory die.

removal rate of tungsten resulted in minimal tungsten thickness loss during the CMP step. A 200-Å–thick TiN diffusion barrier was then deposited on top of the exposed tungsten lines, followed by 4300-Å-thick low-pressure CVD silicon doped *in situ*. The silicon was doped with boron during initial deposition. The boron source gas was discontinued to deposit undoped silicon, forming an $p^+$/undoped stacked film. The Si–TiN was then etched into individual cylindrical vertical diodes. The gaps in between the diodes were filled with HDPCVD $SiO_2$ and CMP until the tops of the diodes were exposed. CMP was carefully controlled so as to remove a maximum of 800 Å of silicon across the wafer, while completely exposing all diodes across the wafer. An $n^+$-doped ohmic contact to the undoped region at the top of the film was formed by phosphorus ion implantation forming a p–i–n "upward" pointing diode. The silicon was amorphous *as deposited*, except for the *in situ* $p^+$-doped portion. Using $BCl_3$ as a doping source gas induced polycrystalline deposition, even at 540 °C [5]. After all memory layers have been formed, a rapid thermal anneal at 750 °C fully crystallized the deposited silicon.

The $SiO_2$ antifuse, 2–3–nm-thick, was grown on top of the doped silicon diodes by rapid thermal oxidation. A second film of tungsten (with TiN adhesion film) was deposited on top of the diodes and then etched into lines, with the lines orthogonal to the first set underneath the diode. Insulating $SiO_2$ film was again deposited on the wires and CMP is performed to remove $SiO_2$ from the top of the wires and planarize the wafer. This completed fabrication of the "upward" pointing memory cell with wiring on both terminals of the diode. A similar process was repeated to form the "downward" pointing memory cell. For the "downward" pointing memory cell, the silicon was doped $n^+$ at the bottom (to make an ohmic contact to the interconnect) and was undoped above that. A boron ion implant formed n-i-p diodes. A scanning electron microscope (SEM) micrograph of two layers of cells is shown in Fig. 2. Vias were formed by oxide etch at every other memory cell layer. The vias were filled first with CVD TiN and then CVD tungsten to form vertical interconnects between memory cell layers and to the read/write transistors in the single crystal substrate. Tungsten deposition into the vias simultaneously deposited the metal for wiring layers, conserving steps. The cross section in Fig. 3 shows the major components of the memory.

## III. Results and Discussion

The cells are programmed by high-voltage transistors with current routed through two levels of tungsten interconnects in between the transistors in the substrate and memory arrays above. The selected cell has a high voltage applied to the word-line (connected to the $p^+$ cell diode terminal) while the bitline (connected to the $n^+$ cell diode terminal) is held at ground. Probability plots of the unprogrammed and programmed forward currents of the lower cells (called L0) are shown in Fig. 4(a), and those of the upper cells (called L1) are shown in Fig. 4(b). The cells were programmed with a 10-V pulse. The cells were distributed in 1024 × 1024 array of cells. The L1 cells consistently showed a higher and more uniform forward current after programming. The cause of this difference is unknown and is under active investigation. The antifuses all broke down in the range 4.5–6 V. During programming, the unselected bit and word lines on the layer containing the target cell, and on the layers immediately above and below it (if any), are held at constant voltages. Typically, these voltages are $V\mathrm{prog}$ −0.7 V for the bit lines and 0.7 V for the word lines [3]. Thus, the fully unselected diodes are biased in reverse (at $V\mathrm{prog}$ −1.4 V). At these biases, the leakage current through the antifuse is large enough so that most of this voltage drops across the diode junction, thus protecting the antifuse from program disturb. The median reverse current at −2 V during read is $1.6 \times 10^{-11}$ A ($1\sigma = 1.1 \times 10^{-11}$ A) for L0, and $5.5 \times 10^{-12}$ A ($1\sigma = 3.6 \times 10^{-12}$ A) for L1.

Transient cell characteristics of a typical cell programmed by voltage pulse are shown in Fig. 5. A 2-V pulse is first applied to the unprogrammed cell, followed by a 10-V programming pulse, and finally a second 2-V read pulse. The output waveform remains low while reading the unprogrammed cell, but is high when reading the programmed cell. A large difference between the unprogrammed and programmed cell currents is desirable for robustness of fabrication, but a short programming

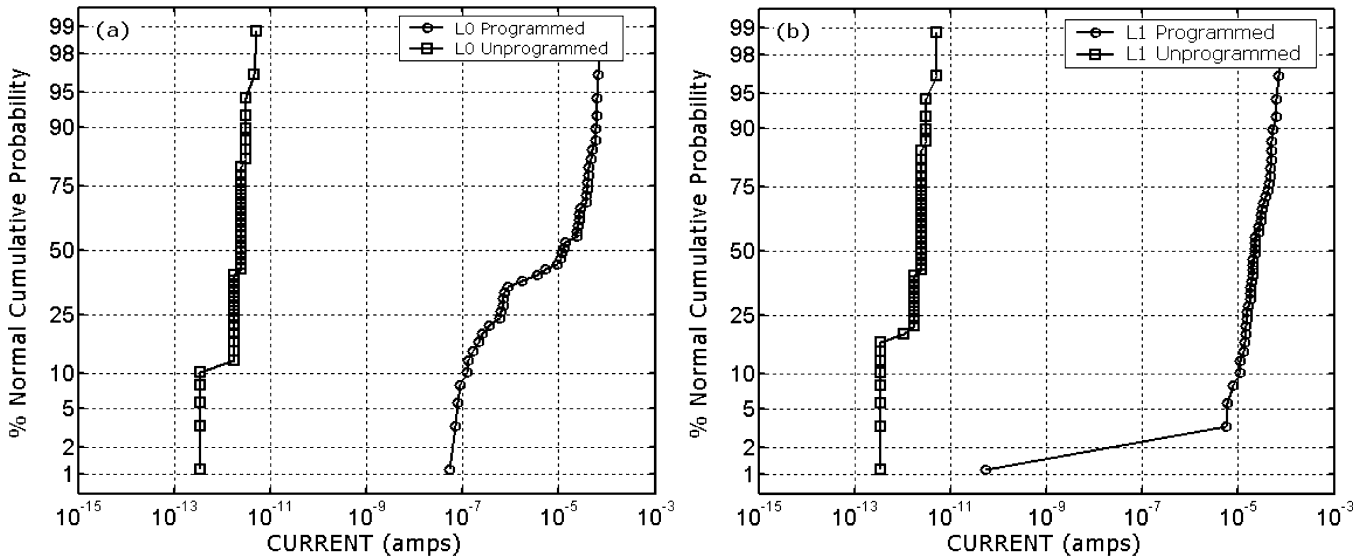


Fig. 4. Probability plots of the unprogrammed and programmed currents for (a) the lower cells with "upward" pointing diodes and (b) the upper cells with "downward" pointing diodes.

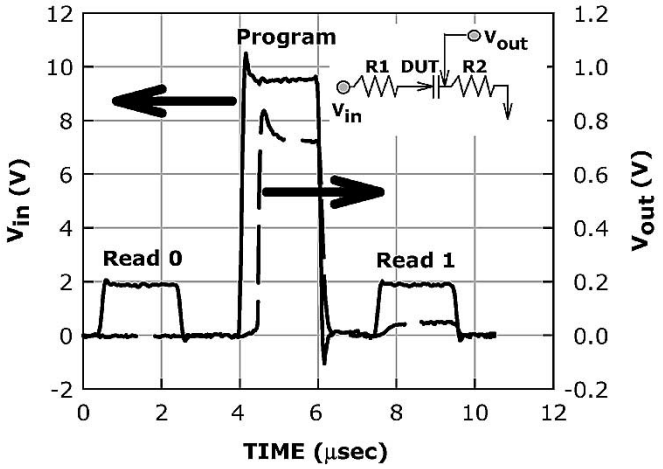


Fig. 5. Transient cell characteristics, measured on a upper L1 cell with a "downward" diode, before, during, and after cell programming. In this measurement, $R1 = 15.7\ \mathrm{k}\Omega$ and $R2 = 2.9\ k\Omega$.

time is desired for fast write times. The unprogrammed forward current, or forward leakage, is decreased by growing a thicker antifuse oxide, but this increases the programming time. The programmed forward current is not measurably affected by the antifuse oxide thickness prior to break down. The output waveform in Fig. 5 also indicates the current through the cell during programming. This current is typically 200–400 $\mu$A, depending on the resistances in series with the cell.

## IV. Conclusion

In conclusion, we describe a field-programmable, ROM cell based on vertical polysilicon diodes with an antifuse. The cell is unprogrammed when the antifuse is intact. The cell is programmed when sufficient biasing voltage is applied to break down the antifuse, connecting the diode to the metal interconnect. By changing the thickness of the antifuse oxide film, the unprogrammed forward leakage of the cell and time to program can be modulated. The cells can be stacked above read/write transistors and above one another, enabling very high packing density.

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