

ELG 6369

NONLINEAR MICROWAVE DEVICES AND EFFECTS

CHAPTER V

MICROWAVE FREQUENCY MULTIPLIERS

A- FREQUENCY MULTIPLIERS: OVERVIEW

I – Introduction

The waveforms used in communication systems in the millimeter and sub-millimeter ranges are often obtained from a relatively low frequency source. This is the principle of frequency multiplication, which shifts the signal from an input frequency f_i to an output frequency $n f_i$.

The schematic of a frequency multiplier is shown in Figure V-1. The blocks F_1 and F_n are two pass-band filters centered respectively on f_i and $n f_i$

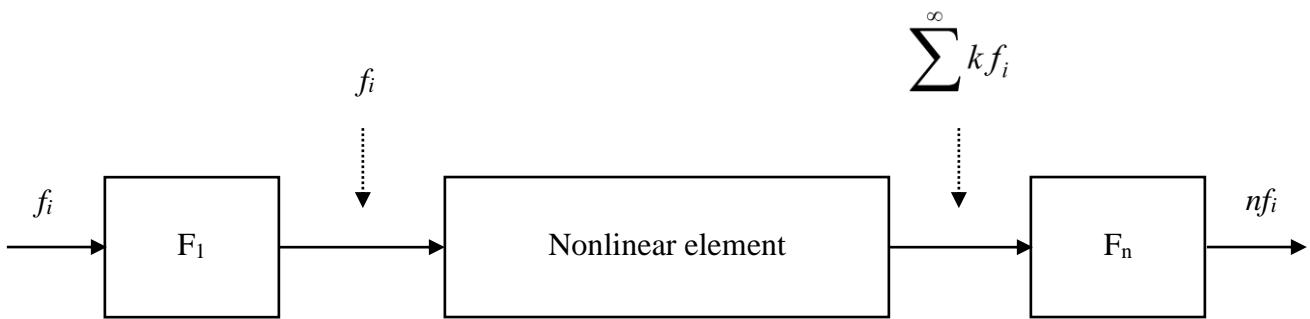


Fig. V-1: Frequency multiplier schematic.

II – Design philosophy

In the past, frequency multipliers were used to generate high levels of microwave RF power. High power multipliers are very important microwave circuits because solid-state amplifiers did not yet exist; at microwave frequencies, power amplification could be provided only by tubes which were expensive and required high DC power. Accordingly, a high-power multiplier block

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consisted of a power amplifier that delivered high power to a cascade of diodes (usually, varactors or SRDs).

Today, solid-state power amplification at microwave frequencies is possible, so high power multipliers are used significantly less because the functions of power amplification and signal generation are separated. Keeping these functions separate has many advantages.

First, the required frequencies are now generated at relatively low powers. Second, it minimizes the dc power consumption that dissipates the most heat from those that may be temperature sensitive. Operating the frequency multiplier circuit at low power reduces the levels of spurious signals and harmonics.

Most frequency multiplier circuits are now used in mixer local oscillators, in test instruments or frequency synthesizers or as low-power drivers for transmitters.

B - DIODES VERSUS TRANSISTORS

When used as frequency multipliers, FETs can usually achieve gain conversion over broad bandwidths while maintaining good dc-RF efficiency at these low power levels. In contrast diode multipliers always exhibit loss. Varactor multipliers are lossy narrow-band components that operate best at moderate to high power levels.

Resistive diode multipliers (using Schottky diodes) are more broadband but have even greater loss and a limited power handling ability. Thus, the medium- to high-power driver amplifiers required by such multipliers, generate RF power that is eventually wasted in the diodes and matching networks. It is not unusual for a driver amplifier and a diode multiplier chain to require several watts of dc power to generate a few milliwatts of RF power.

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Note 1: The Schottky diode I - V curve is presented on Figure V-2. As we can see, if the dc point (Q point) is beyond the barrier voltage Φ , the diode frequency multiplier is called "resistive multiplier" because it exploits the conductance characteristic of the diode.

On the other hand, for a dc point between the breakdown voltage (avalanche voltage) V_a and the barrier voltage Φ , the circuit uses the capacitance variations to generate frequency multiplication.

In this last case, we must distinguish between two different cases. If the Q point dynamic excursion is from V_a to Φ without reaching this maximal value, the diode presents a pure reactance and such frequency multipliers are called "reactive circuits" or "parametric circuits". As for amplifiers, they exhibit a very low noise figure.

However, if the barrier voltage value is slightly exceeded, a high accumulation of charges in the nonlinear capacity during the positive cycle of the exciting signal will create a phenomenon called "snap off effect". This phenomenon favors high-order multiplication. In fact, the discharge of a high accumulation of charges in a nonlinear capacity during the negative cycle of the signal will generate a very large number of harmonics.

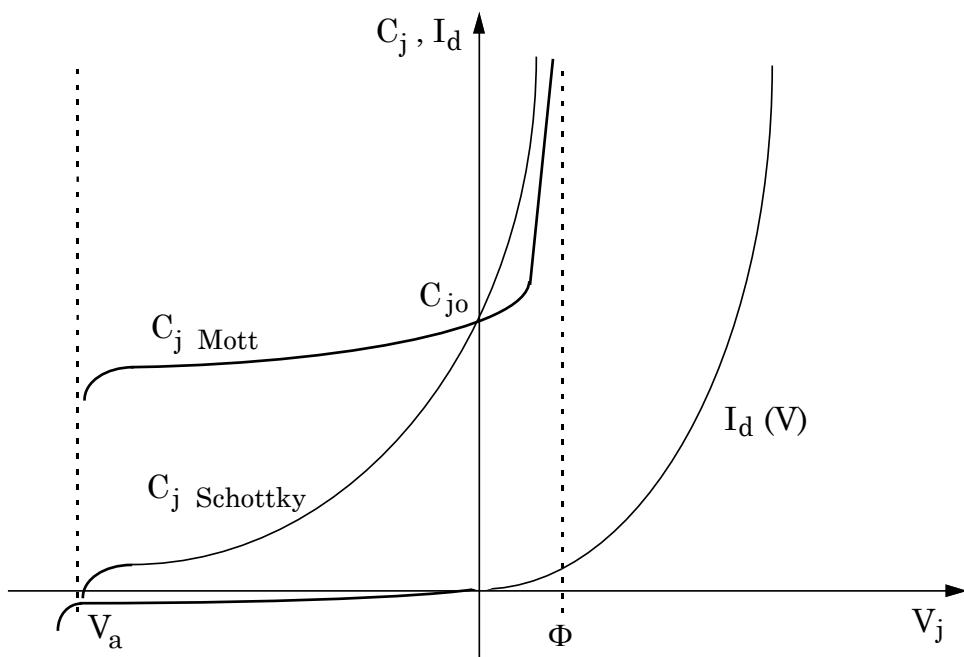


Fig. V-2: I-V characteristic of a Schottky diode.

C – DIODE MULTIPLIERS

I – Parametric diode multipliers

The parametric effect is governed by the Manley-Rowe relations (see chapter IV). As for a frequency multiplier, only one signal is present at the input, these relations can be simplified to

$$\sum_{m=0}^{\infty} P_m = 0 \quad (\text{V-1})$$

where P_m is the power at frequency $m f_e$. This needs to include an “idler” circuit to reject and dissipate the undesirable powers other than the output power.

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II – Resistive diode multipliers

A direct bias of a diode gives a low-order multiplication. Using the nonlinearity of the conductance characteristic, resistive diode frequency multipliers exhibit a lower efficiency but a larger bandwidth than parametric diode frequency multipliers. Moreover, it is easier to design a resistive circuit than a parametric circuit because the latter is very sensitive to mismatching and very difficult to optimize.

D – TRANSISTOR MULTIPLIERS

As mentioned above, FETs can usually achieve unity (or greater) gain conversion over broad bandwidths while maintaining good dc-RF efficiency at these low power levels. In contrast diode multipliers always exhibit loss. If the MESFET was widely used for frequency multiplication in the RF/microwave range, HEMTs are now more present in frequency multiplier circuits.

The basic scheme of an n-order transistor multiplier is similar to the amplifier one except that the output we have a resonant circuit between the output and the load. This resonant circuit is centered on the n^{th} harmonic of the fundamental input frequency. The excitation is usually applied to the gate (Figure V-3).

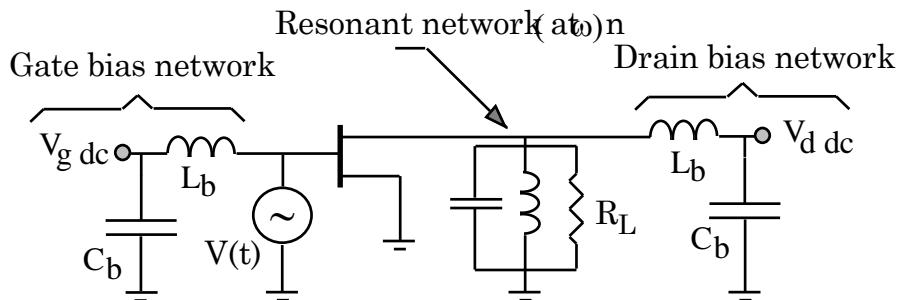


Fig. V-3. Circuit of an ideal FET frequency multiplier.

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I – Theory of transistor multiplier design

For an M finite number of harmonics the nonlinear input-output voltage-current parameters can be written as

$$V_i(t) = \sum_{k=-M}^M V_{ik} e^{jk\omega t} \quad (\text{V-2-a})$$

$$I_i(t) = \sum_{k=-M}^M I_{ik} e^{jk\omega t} \quad (\text{V-2-b})$$

and

$$V_o(t) = \sum_{k=-M}^M V_{ok} e^{jk\omega t} \quad (\text{V-3-a})$$

$$I_o(t) = \sum_{k=-M}^M I_{ok} e^{jk\omega t} \quad (\text{V-3-b})$$

Since the field-effect transistor frequency multiplier is widely used in multiplication, the following figure can be utilized for the design (Figure V-4).

The parasitic elements of gate (R_e, L_e and C_e) and drain (R_s, L_s and C_s) are assumed to be linear and added respectively to the external input-output impedances of the matching networks. These source and load impedances are noted respectively $Z_{RLe}(k\omega)$ and $Z_{RLs}(k\omega)$.

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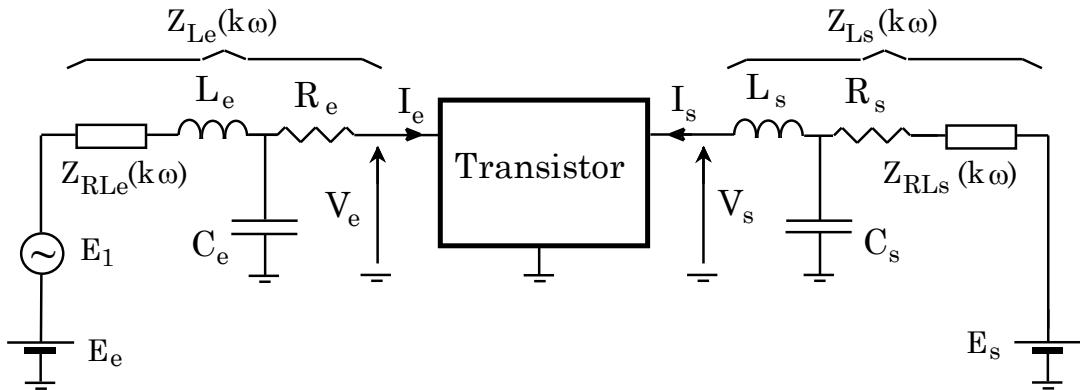


Fig. V-4: FET Transistor multiplier.

Let E_e and E_s be the bias voltages of gate and drain, respectively, and let E_1 be the input voltage. The network equations can be written on the form of the following system

$$\left. \begin{array}{l} V_{e0} = E_e - I_{e0} Z_{Le}(0) \\ V_{s0} = E_s - I_{s0} Z_{Ls}(0) \end{array} \right\} \text{for } k=0$$

$$\left. \begin{array}{l} V_{e\pm 1} = E_1 - I_{e\pm 1} Z_{Le}(\pm \omega) \\ V_{s\pm 1} = -I_{s\pm 1} Z_{Ls}(\pm \omega) \end{array} \right\} \text{for } k=1$$

$$\left. \begin{array}{l} V_{e\pm k} = -I_{ek} Z_{Le}(\pm k\omega) \\ V_{s\pm k} = -I_{sk} Z_{Ls}(\pm k\omega) \end{array} \right\} \text{for } k=2, 3, \dots$$

The resolution of this system leads to the optimum input output voltages for the multiplier.

Note 1: The system can be highly nonlinear, and therefore its resolution is not straightforward. We will discuss in the next section some approximate design of FET frequency multipliers.

Note 2: Because the multiplier is based on the combination of a FET device and input-output filters, a chapter will be devoted to introducing these passive circuits and discussing their design.

Compared to diode frequency multipliers, FET frequency multipliers can achieve broad bandwidths and conversion gains (greater than unity). Furthermore, because small-signal FETs can be used to realize efficient multipliers (particularly for low-order multiplication devices such as doublers), high-frequency FET multiplier chain usually consumes little dc power and dissipates little heat; this is an important advantage in space-based systems.

II – Class-B multiplier

The most widely used circuit is the low-power “Class-B” multiplier, which operates in a manner analogous to that of a Class-B amplifier. Such multipliers are very stable and have good gain, efficiency, and output power. Other modes of operation can provide higher gain than the Class-B multiplier. However, this high gain is often the result of feedback effects, which may make the multiplier unstable. Consequently, the Class-B multiplier is usually the more practical form of FET frequency multiplier for most applications. So, this configuration will be used for the design discussed in the next section.

E – PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

I – Introduction

In this part, we will examine the design of a low power Class-B multiplier that generate low-level RF output power (normally below 8-10 dBm) at low harmonics, have at least unity gain, and may have high output frequencies, sometimes in the millimeter range. The design approach we will develop is applicable to power FET multipliers operating at lower frequencies; it will require only a larger FET with higher power.

As the multiplier is operating in Class-B, the gate is biased near the turn-on voltage V_t , the channel conducts in pulses having a duty cycle near 50% and the gate and drain are short-circuited at all unwanted harmonics of the excitation frequency.

II – Approximate design

The design we will use is an initial design which can be optimized using CAD tool such as the harmonic balance.

The process starts by examining the properties of a large-signal multiplier circuit that uses an ideal FET, then modify the circuit to include a FET having a minimal set of parasitic elements. Figure V-5 shows a modified version of the circuit of the FET frequency multiplier presented in Figure V-3.

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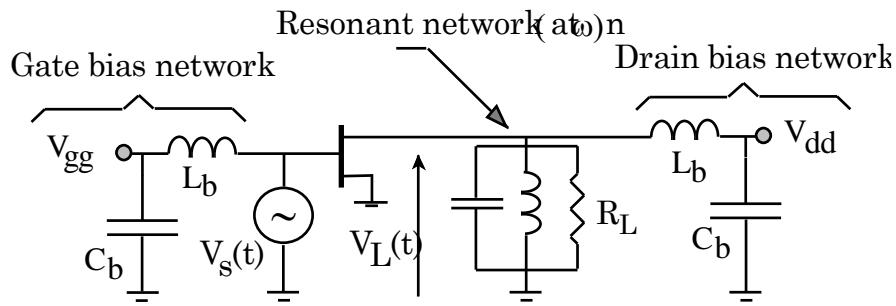


Fig. V-5. Circuit of an ideal FET frequency multiplier.

The gate-bias voltage in an efficient FET multiplier must be equal to or less than (more negative than) the turn on voltage V_t . Thus, the FET's channel conducts only during the positive half of the excitation cycle, and the drain conducts in pulses (the shape of the pulses is approximately a rectified cosine or half cosine). The drain-current waveform can be then modeled as a train of half-cosine pulses. The duty cycle of the pulses varies with V_{gg} : if $V_{gg} = V_t$, the duty cycle is 50%, but if $V_{gg} < V_t$ (the ideal situation), the FET is turned off over most of the excitation cycle, so the duty is less than 50%.

Figure V-6 shows the voltage and current waveforms of the ideal FET used as a frequency doubler. Because the output resonator eliminates all voltage components except the one at the n^{th} harmonic, the drain voltage $V_d(t)$ is a sinusoid having frequency $n\omega_p$. For best efficiency, and output power, the drain voltage must vary between V_{dmax} and V_{dmin} (in Figures V-6 and V-7). V_{dmin} is the value of drain voltage at the knee of the drain I - V curve when the gate voltage has its maximum value V_{gmax} .

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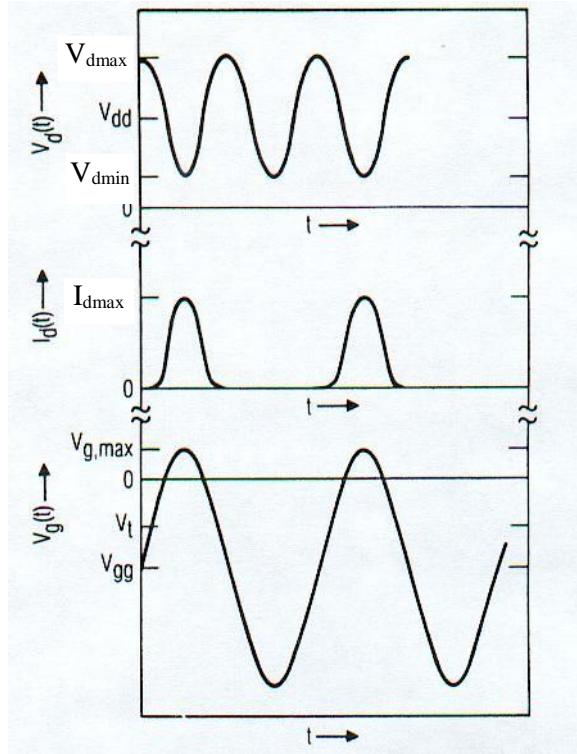


Fig. V-6. Voltage and current waveforms in the ideal FET frequency multiplier.

As the maximum negative excursion of V_g is $2V_t$, then

$$V_{d\max} = V_a - 2 |V_t| \quad (\text{V-4})$$

where V_a is the drain-gate avalanche breakdown voltage. V_{dd} , the dc drain voltage, is halfway between $V_{d\min}$ and $V_{d\max}$. The load conductance is equal to the slope of the load line

$$G_L = \frac{V_{d\max} - V_{d\min}}{I_{d\max} - I_{d\min}} \quad (\text{V-5})$$

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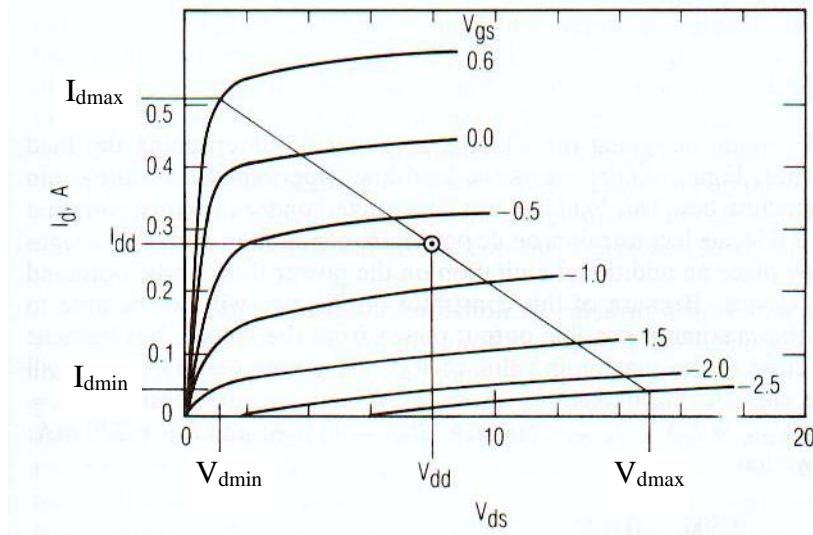


Fig. V-7. Example of FET's I-V characteristics including the load line.

The gate voltage varies between V_{gmax} , the peak gate voltage (limited to 0.5V in MESFETs by rectification in the gate-channel Schottky junction) and $\{ 2V_{gg} - V_{gmax} \}$, a relatively high reverse voltage.

The drain current peaks at the value I_{dmax} , and the current pulses have the time duration t_o ; $t_o \leq T/2$ where T is the period of the excitation. If we make $t = 0$ equal to the point where the current is maximum, the Fourier-series representation of the current has only cosine components

$$I_d(t) = I_o + I_1 \cos(\omega_p t) + I_2 \cos(2\omega_p t) + I_3 \cos(3\omega_p t) + \dots \quad (\text{V-3})$$

When $n \geq 1$, the coefficients are

$$I_n = I_{d\max} \frac{4t_o}{\pi T} \left| \frac{\cos(n\pi t_o/T)}{1 - (2nt_o/T)^2} \right| \quad (\text{V-4})$$

and when $n = 0$,

$$I_o = I_{d\max} \frac{2t_o}{\pi T} \quad (\text{V-5})$$

When $\{ t_o/T = 1/2n \}$, $n \neq 0$, the equation (V-4) is indeterminate. Then

$$I_n = I_{d\max} \frac{t_o}{T} \quad (\text{V-6})$$

As the current I_n circulates in the load R_L and contributes to output power, we must maximize I_n . Moreover, (V-4) shows that we have only one degree of freedom for doing so: varying t_o/T . Figure V-4 shows a plot of $I_n/I_{d\max}$ as a function of t_o/T when $n = 2$ through $n = 4$; each of these curves has a clear maximum below $t_o/T = 0.5$. It would appear that, in order to achieve the optimum value of I_n , we need only to adjust V_{gg} so that $I_d(t)$ has the desired period of conduction t_o .

Unfortunately, to achieve a short conduction period we should take into account two aspects:

- $\{ V_{gg} \ll V_t \}$ but this large bias voltage would make the magnitude of the peak reverse voltage (which is $2V_{gg}$) very large. As in practical design, the peak drain-gate voltage can be nearly $\{ V_{max} - 2V_{gg} \}$, if V_{gg} is adjusted to make t_o/T very small, the peak drain-gate voltage may be much greater than the avalanche voltage.

- In order to achieve an acceptable output power level, the input power should be high (especially for a multiplier having an output harmonic greater than the second). The selected t_o/T should be then greater than the optimum value to achieve an acceptable trade-off between gain and output power.

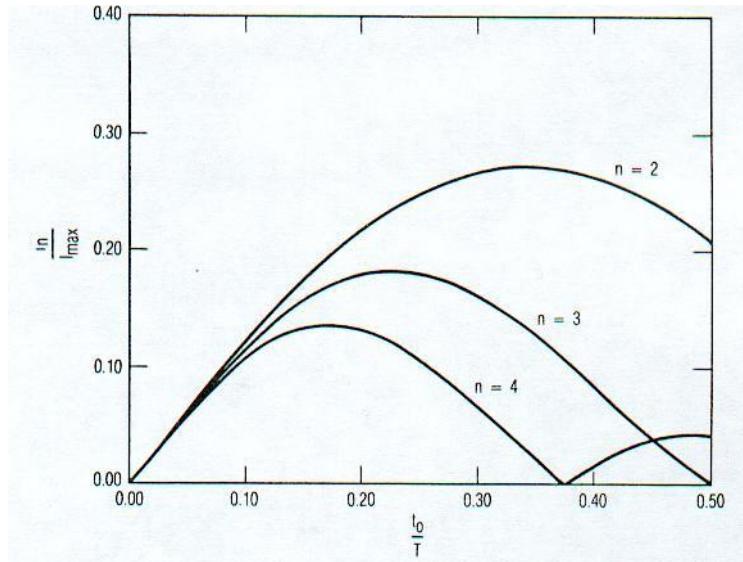


Fig. V-4. Harmonic drain current components as a function of t_o/T when the drain current waveform is a half sinusoidal pulse train.

The maximum reverse gate voltage that the FET can tolerate establishes one limit on t_o/T . If the gate voltage varies between V_{gmax} and the peak reverse voltage V_{gmin} , then the phase angle θ_t over which $V_g(t) > V_t$ is

$$\theta_t = 2 \cos^{-1} \left(\frac{2V_t - V_{gmax} - V_{gmin}}{V_{gmax} - V_{gmin}} \right) \quad (\text{V-7})$$

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and the bias voltage that achieves this value of θ_t is

$$V_{gg} = \frac{V_{g\max} + V_{g\min}}{2} \quad (\text{V-8})$$

Note that $\{\theta/360^\circ = t_o/T\}$. The current in the load is I_n .

For the voltage V_L across the load to vary between $V_{d\max}$ and $V_{d\min}$:

$$|V_L(t)| = I_n R_L = \frac{V_{d\max} - V_{d\min}}{2} \quad (\text{V-9})$$

and the optimum load resistance is

$$R_L = \frac{V_{d\max} - V_{d\min}}{2 I_n} \quad (\text{V-10})$$

Because I_n is relatively small compared to the current I_1 in a Class-B amplifier, R_L in a multiplier is usually much larger. The output power P_{Ln} at the n^{th} harmonic is

$$P_{Ln} = \frac{1}{2} I_n^2 R_L = \frac{1}{2} I_n \frac{V_{d\max} - V_{d\min}}{2} \quad (\text{V-11})$$

As with a power amplifier, the dc drain bias voltage is halfway between $V_{d\max}$ and $V_{d\min}$; that is

$$V_{dd} = \frac{V_{d\max} + V_{d\min}}{2} \quad (\text{V-12})$$

The dc power is

$$P_{dc} = V_{dd} I_{dc} = V_{dd} I_o \quad (\text{V-13})$$

Substituting I_o from equation (V-4), we have

$$P_{dc} = V_{dd} I_{d\max} \frac{2t_o}{\pi T} \quad (\text{V-14})$$

and the dc-RF efficiency is

$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}} \quad (\text{V-15})$$

Because the harmonic output current in a multiplier is usually much less than the fundamental current in an amplifier, the efficiency is much lower in a FET multiplier than in a FET amplifier.

The RF input power can be approximated using the fact that the drain is short-circuited at the fundamental frequency. Then, the input of the FET can be modeled as a series connection of resistances $\{ R_s + R_i + R_g \}$ and $C_{gs}(V_{gg})$. The excitation source must generate an RF voltage having the peak value $\{ V_{gmax} - V_{gg} \}$ across C_{gs} .

If the source is matched, the power available from the source must equal P_{in} :

$$P_{av} = P_{in} = \frac{1}{2} (V_{gmax} - V_{gg})^2 \omega_p^2 C_{gs}^2 (R_s + R_i + R_g) \quad (\text{V-16})$$

The conversion gain G_c is equal to

$$G_c = \frac{P_{Ln}}{P_{av}} \quad (\text{V-17})$$

For a matched input, this gain is the power gain G_p

$$G_p = \frac{P_{Ln}}{P_{in}} \quad (\text{V-18})$$

Therefore, as the power-added efficiency of a FET multiplier is

$$\eta_a = \frac{P_{Ln} - P_{in}}{P_{dc}} \quad (\text{V-19})$$

the power gain is related to the power-added efficiency by

$$\eta_a = \eta_{dc} \left(1 - \frac{1}{G_p} \right) \quad (\text{V-20})$$

A final consideration is the choice of V_{dmax} and V_{gmin} . Both must be chosen so that the drain-gate avalanche voltage is not exceeded. The maximum drain-gate voltage is approximately $\{ V_{dmax} - V_{gmin} \}$ so we have the limitation (equation V-1)

$$V_{dmax} - V_{gmin} < V_a \quad (\text{V-21})$$

where V_a is the drain-gate avalanche voltage.

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Note: This relation is more restrictive than equation (V-1) while V_{dmax} and V_{gmin} cannot be chosen independently.

B – WORKING EXAMPLE

We wish to design a FET doubler that has an input frequency of 10 GHz. The FET has the following parameters:

$$V_a = 12.0 \text{ V}$$

$$V_t = -2.0 \text{ V}$$

$$R_s = 2.0 \Omega$$

$$R_i = 2.0 \Omega$$

$$R_g = 1.0 \Omega$$

$$R_d = 2.0 \Omega$$

$$I_{dss} = 80 \text{ mA} \quad \text{at} \quad V_{ds} = 3.0 \text{ V}$$

$$L_s = 0.005 \text{ nH}$$

$$C_{gs} = 0.25 \text{ pF} \quad \text{at} \quad V_{gs} = V_{gg}$$

$$C_{gd} = 0.08 \text{ pF}$$

$$C_{ds} = 0.10 \text{ pF}$$

We use the Cubic Curtice model of I_d

$$I_d = (A_0 + A_1 V + A_2 V^2 + A_3 V^3) \tanh(\alpha V_{ds}) \quad (\text{V-22})$$

where the parameters are (for $\beta = 0$)

$$A_o = 0.09670$$

$$A_1 = 0.11334$$

$$A_2 = 0.04853$$

$$A_3 = 0.00801$$

$$\alpha = 1.5$$

The design process is:

Step 1- Find the device operating parameter values:

From the I-V curves shown on Figure V-5 or using equation V-22, we estimate

$$I_{dmax} \approx I_{dss} = 80 \text{ mA} \quad \text{and} \quad V_{dmin} = 1.0V \text{ (the value at the knee).}$$

V_{gmin} and V_{dmax} must obey the constraint expressed by equation (V-21)

$$V_{dmax} - V_{gmin} < V_a = 12V,$$

so we can choose $V_{gmin} = -7.0V$ and $V_{dmax} = 5.0V$.

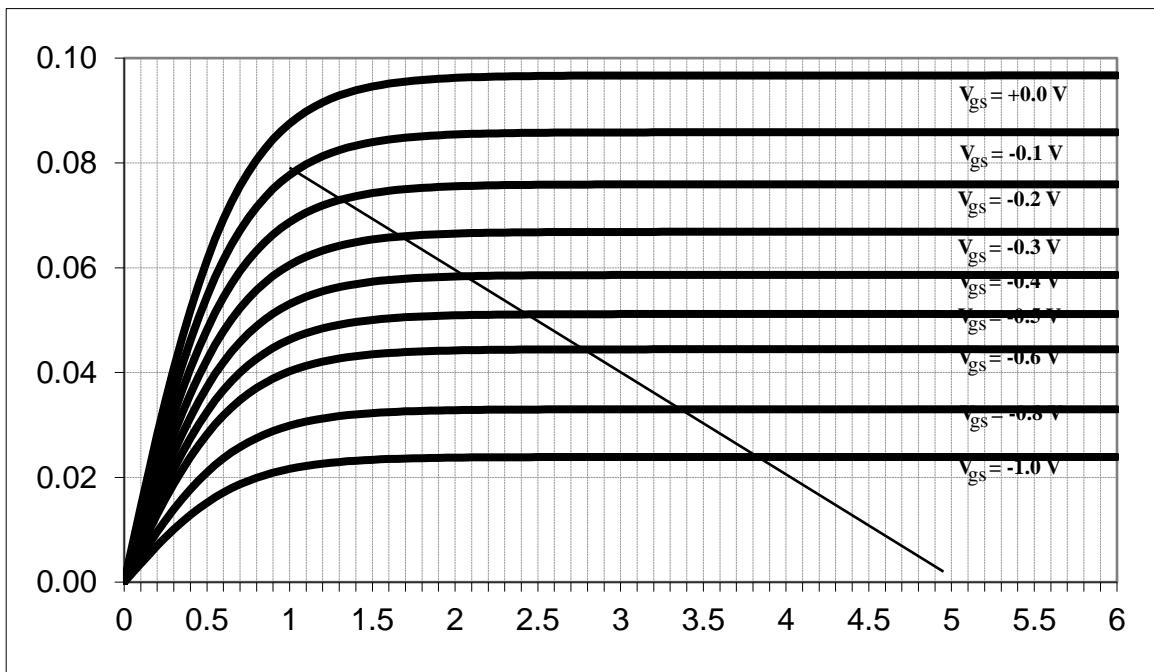


Fig. V-5. I-V characteristics for the worked example.

We also choose $V_{gmax} = 0.2V$, slightly below the lowest value that allows rectification. Equations (V-8) and (V-12) give

$$V_{gg} = \frac{V_{gmax} + V_{gmin}}{2} = \frac{0.2 - 7}{2} = -3.4V$$

$$V_{dd} = \frac{V_{dmax} + V_{dmin}}{2} = \frac{5.0 + 1.0}{2} = 3V$$

Substituting these values into (V-7) gives

$$\theta_t = 2 \cos^{-1} \left(\frac{2V_t - V_{gmax} - V_{gmin}}{V_{gmax} - V_{gmin}} \right) = 2 \cos^{-1} \left(\frac{2 * (-2.0) - 0.2 - (-7.0)}{0.2 - (-7.0)} \right)$$

$$\theta_t = 2 \cos^{-1}(0.388) = 134.4^\circ \quad \text{or} \quad 2.36 \text{rd}$$

$$\Rightarrow \frac{t_o}{T} = \frac{134.4}{360} = 0.37$$

Figure V-4 shows that this value is close to the optimum value for a doubler ($n = 2$) and that

$$I_2 = I_{d\max} \frac{4t_o}{\pi T} \left| \frac{\cos(2\pi t_o/T)}{1 - (4t_o/T)^2} \right| = I_{d\max} \frac{4}{\pi} 0.37 \left| \frac{\cos(2\pi 0.37)}{1 - (4 * 0.37)^2} \right| = I_{d\max} 0.471 * \frac{0.68}{1.19}$$

$$I_2 = 0.269 I_{d\max} = 21.6 \text{ mA}$$

The dc drain current is given by equation V-5:

$$I_o = I_{d\max} \frac{2t_o}{\pi T} = 80 * \frac{2}{\pi} * 0.37 = 19 \text{ mA}$$

Step 2- Determine the circuit parameters

Equation (V-16) can now be used to find the input power

$$P_{in} = \frac{1}{2} (3.6)^2 (2 * \pi * 10^{10})^2 (0.25 * 10^{-12})^2 (5)$$

$$P_{in} = 6.48 * 3.947 * 10^{21} * 6.25 * 10^{-26} * 5 = 7.99 \text{ mW} \approx 8 \text{ mW} \quad \text{or} \quad 9.0 \text{ dBm}$$

If the input is matched, the input power is equal to the power available from the excitation source.

Equation (V-11) gives the output power

$$P_{L2} = \frac{1}{2} I_2^2 R_L = \frac{1}{2} I_2 \frac{V_{d\max} - V_{d\min}}{2} = \frac{1}{2} 21.6 \frac{5.0 - 1.0}{2} = 21.6 \text{ mW} \quad \text{or} \quad 13.3 \text{ dBm}$$

Thus the conversion gain is

$$G_c = \frac{P_{Ln}}{P_{av}} = \frac{P_{Ln}}{P_{in}} = \frac{21.6}{8} = 2.7 \quad \text{or} \quad 4.3 \text{ dB}$$

The dc power (equation V-13) is equal to

$$P_{dc} = V_{dd} I_o = 3 * 19 = 57 \text{ W}$$

The dc-RF efficiency is then (equation V-15)

$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}} = \frac{21.6}{57} = 38\%$$

Note: The V_{gmin} and V_{dmax} choice is not subjective but based on the following constraints:

- The I - V characteristics limits
- The predicted value of t_o/T must be close to the optimum value.
- The bias drain current that must be approximately equal to $I_{ds}/2$ (i.e., at the middle of the load line).

As the initial values require some experience to estimate, a designer can also use the following procedure:

- Select the optimum value of t_o/T . Here for the doubler (see Figure V-4):

$$n = 2 \text{ gives } t_o/T = 0.37.$$

- Note the corresponding value of

$$I_n/I_{dmax} = I_2/I_{dmax} = 0.27.$$

- Deduce the I_n value:

$$I_n = I_2 = 0.27 * I_{dmax} = 0.27 * I_{dss} = 0.27 * 80 = 21.6 \text{ mA}$$

- Estimate the V_{gmin} voltage knowing that $V_{gmax} = 0.2\text{V}$ and $V_{dmin} = 1\text{V}$ are good approximations for almost all FETs:

$$\cos\left(\frac{134.4^\circ}{2}\right) = \frac{2V_t - V_{gmax} - V_{gmin}}{V_{gmax} - V_{gmin}} = \frac{2*(-2) - 0.2 - V_{gmin}}{0.2 - V_{gmin}}$$

$$V_{gmin} = -7.0\text{V}$$

- Deduce the V_{dmax} voltage:

$$V_{dmax} - V_{gmin} < V_a = 12\text{V} \quad \Rightarrow \quad V_{dmax} = 5.0\text{V}.$$

- Determine the bias voltages V_{gg} and V_{dd} :

$$V_{gg} = \frac{V_{g\max} + V_{g\min}}{2} = \frac{0.2 - 7}{2} = -3.4V$$

$$V_{dd} = \frac{V_{d\max} + V_{d\min}}{2} = 3V$$

- Obtain the dc drain current (equation V-5)

$$I_o = I_{d\max} \frac{2t_o}{\pi T} = 80 * \frac{2}{\pi} * 0.37 = 19 \text{ mA}$$

- Determine the circuit parameters

* Input Power [Equation (V-16)]

$$P_{in} = \frac{1}{2} (3.6)^2 \left(2 * \pi * 10^{10} \right)^2 \left(0.25 * 10^{-12} \right)^2 (5) \approx 8 \text{ mW}$$

or 9.0 dBm

* Output Power [Equation (V-11)]

$$P_{L2} = \frac{1}{2} I_2^2 R_L = \frac{1}{2} I_2 \frac{V_{d\max} - V_{d\min}}{2} = 21.6 \text{ mW}$$

or 13.3 dBm

* Conversion gain [Equation (V-17)]

$$G_c = \frac{P_{Ln}}{P_{av}} = \frac{P_{Ln}}{P_{in}} = \frac{21.6}{8} = 2.7$$

or 4.3dB

* Dc power [Equation (V-13)]

$$P_{dc} = V_{dd} I_o = 3 * 19 = 57 \text{ W}$$

* Dc-RF efficiency [Equation (V-15)]

$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}} = \frac{21.6}{57} = 38\%$$

Step 3- Determine the input-output impedances

The load is found using Equation (V-10)

$$R_L = \frac{V_{d\max} - V_{d\min}}{2I_n} = \frac{5.0 - 1.0}{2 * 21.6 * 10^{-3}} = 92.6 \Omega$$

and in order to resonate the output capacitance C_{ds} , there must be a susceptance in parallel with the load of

$$X_L = -2\omega_p C_{ds} = -2 * 2 * \pi * 10^{10} * 0.1 * 10^{-12} = 12.5 \text{ mS}$$

Converting this load to impedance gives

$$Z_L(2\omega_p) = \frac{1}{(1/92.6) - j12.5 \cdot 10^{-3}} = (39.5 + j46.2)\Omega$$

The input impedance is

$$Z_{in}(\omega_p) = R_s + R_i + R_g + \frac{1}{j\omega_p C_{gs}} = (5 - j63)\Omega$$

Step 4- Determine the matching input-output networks

The rest of the design involves realizing the input and output matching networks. The output-matching network is a filter that short circuit the drain at the fundamental frequency and unwanted harmonics, followed by matching elements.

OUTPUT:

A half-wave filter is ideal for the output of a doubler. It consists of a cascade of alternating high and low impedance transmission line sections each $\lambda/4$ long at ω_p :

- They have a $\lambda/4$ long at ω_p : Maximum rejection at ω_p
- They have a $\{ 2\lambda/4 = \lambda/2 \}$ long at $2\omega_p$: No rejection at $2\omega_p$
- They have a $\{ 3\lambda/4 = \lambda/2 \}$ long at $3\omega_p$: Maximum rejection at $3\omega_p$

Moreover, from Figure V-4 we see that $I_4 \approx 0$ at $\{ t_o/T = 0.37 \}$ so the fourth-harmonic output should be very low.

But this structure presents two limitations:

- It cannot be used for the frequency tripler.
- It is a very narrow band structure. Any frequency variation would degrade dramatically the circuit performance.

Therefore, a band-pass filter could be a good alternative to filter the output but an idler circuit is required to short the second harmonic (add a stub at $2\omega_p$).

INPUT:

The gate should be short-circuited at the second-harmonic frequency. A shorted stub $\lambda/4$ long at ω_p is adequate to provide the termination. This transformer has no effect on the excitation but is $\lambda/4$ at $2\omega_p$ and thus short-circuits the gate at this frequency.

But this structure presents two limitations:

- It is a very narrow band structure.
- It cannot be used for the frequency tripler because both ω_p and $3\omega_p$ could be present at the input.

Therefore, a low-pass filter could be a good alternative to filter the input.

A complete layout of the frequency doubler is shown on Figure V–6 (From Maas).

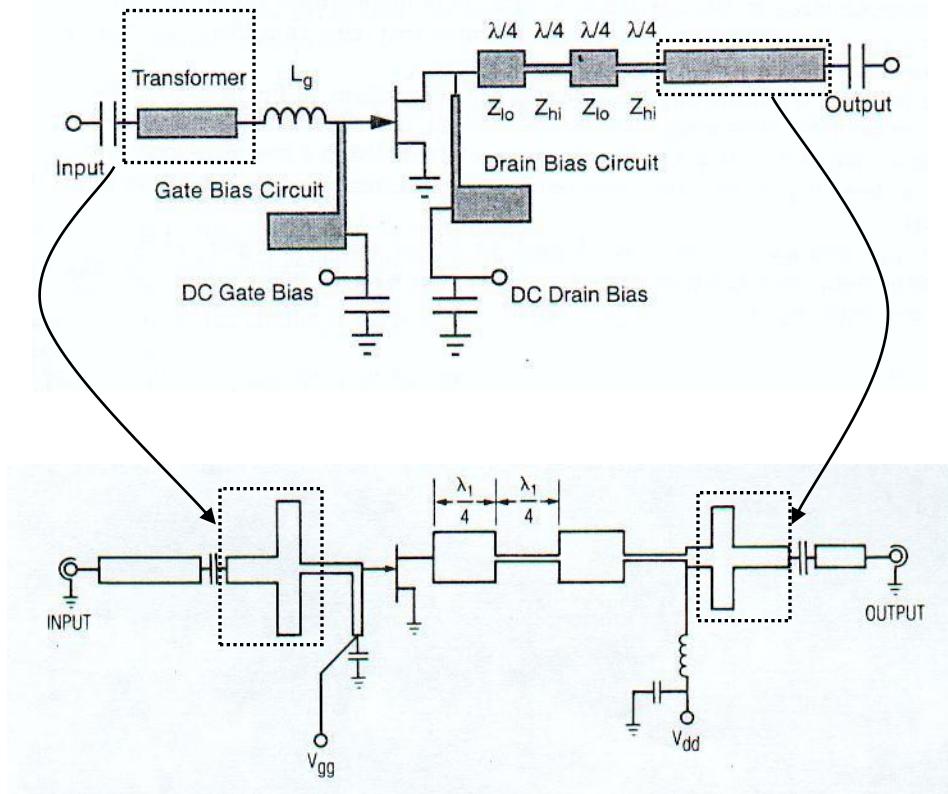


Fig. V-6. Circuit of the FET frequency doubler.

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Analysis of Frequency Multiplier Circuits

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Frequency Multipliers

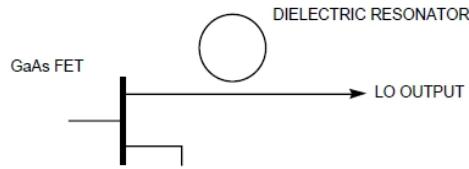
Julian Rosu, YO3DAC / VA3IUL, <http://www.qsl.net/va3iul>

There are few approaches how to generate a high frequency signal for microwaves frequencies.

Direct Signal Generation -

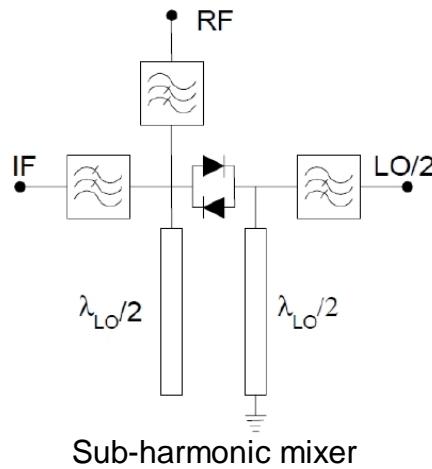
First approach is to generate the high frequency directly, at the fundamental, using an oscillator tuned on the desired frequency. Few sensitive issues appears here due to high working frequency as, stability, jitter, phase noise, pulling, pushing, low output power, and cost of the active component to meet the performances.

A FET oscillator may be stabilized by a dielectric resonator. Problems may involve in this situation are: phase noise, frequency stability and accuracy.



Sub-Harmonic Mixer -

Another approach how to minimize the issues of a high frequency oscillator is to use a Sub-Harmonic mixer.

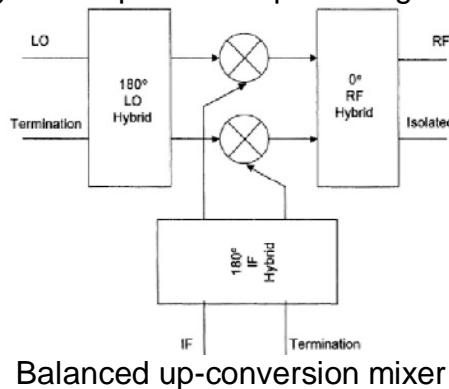


- Sub-harmonic mixers are useful at higher frequencies when it can be difficult to produce a suitable LO signal. They have the LO input at frequency = LO/n.
- Sub-harmonic mixers use anti-parallel diode pairs and they produce most of their power at “odd” products of the input signals. Even products are rejected due to the I-V characteristics of the diodes.
- Attenuation of even harmonics is determined by diodes “balance”. The diode “matching” is critical in this type of mixers.
- The short circuit $\lambda_{LO}/2$ stub at the LO port is a quarter of a wavelength long at the input frequency of LO/2 and so is open circuit. However, at RF frequency this stub is approximately a half wavelength long, so providing a short circuit to the RF signal.
- At the RF input the open circuit $\lambda_{LO}/2$ stub presents a good open circuit to the RF but is a quarter wavelength long at the frequency LO/2 and so is short circuit.

Up-Conversion Mixer -

The third option to generate a high frequency signal is to use an up converter. The design of an up converter has typically received much less attention in terms of design methodology than down converter design, which is common approach in most of the receiver designs. There are some aspects to up converter design which are not relevant to down converters, and vice versa.

- An up-conversion mixer requires high linearity and low noise to minimize the amount of spurious power spread into adjacent channels.
Have to take careful attention at LO amplitude, and LO-to-RF isolation.
- A good approach for an up-conversion mixer is the balanced mixer which provides good common-mode rejection to suppress LO feed-through and good linearity.
- The LO level should provide a reasonable compromise between conversion gain and LO power, but should not limit the 1 dB gain-compression input voltage.

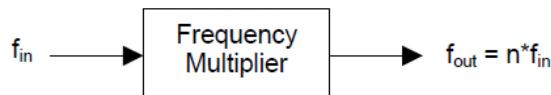


Frequency Multipliers –

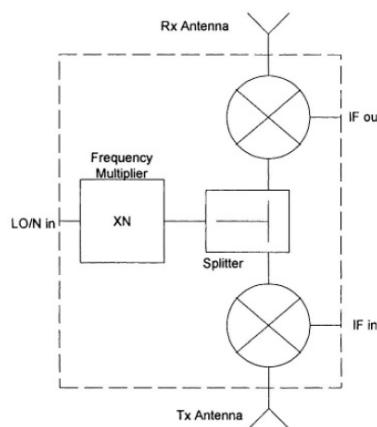
Another alternative method to generate high frequency signal power with low phase noise is to generate a high-quality lower frequency signal and employ a frequency multiplier to deliver the high frequency output at the desired frequency. This approach is the subject of this paper.

Frequency multipliers will always be a way of generating the highest frequencies.

- A frequency multiplier has the property that the frequency of the output signal has an integer multiple of the input frequency.



This approach is commonly adopted in microwave transceivers.



Frequency multiplier based microwave transceiver block diagram

Even if a multiplier introduces no Phase Noise of its own, the process of frequency multiplication even by an ideal, noiseless multiplier, inevitably increases the Phase Noise.

- The reason for this unfortunate characteristic is that a frequency multiplier is in fact a phase multiplier, so it multiplies the phase deviations as well as the frequency of the input signal.
- A square-wave contains odd harmonics. However, by varying the duty cycle of the waveform, so that rectangular-wave results, even order harmonic content can be introduced.
- The 2nd harmonic content of a rectangular-wave peaks when the duty cycle is 25%, and a 3rd harmonic peaks when duty cycle peaks 16%.
- The minimum Carrier-to-Noise degradation, ΔCNR , in decibels, caused by an ideal frequency multiplier is:

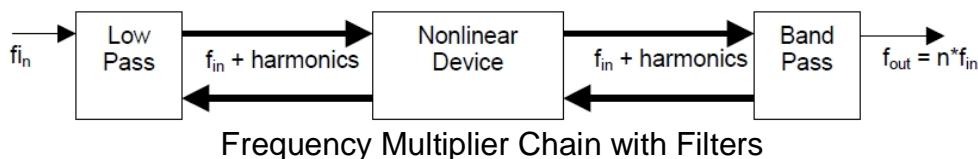
$$\Delta CNR_{[dB]} = 20 \cdot \log(N) \quad \text{where } N \text{ is the multiplication factor.}$$

- Thus, a frequency doubler ($N=2$) degrades CNR at the input signal by at least 6dB and a quadrupler ($N=4$) degrades CNR by at least 12dB.

Multiplying a very stable low-frequency reference signal can still produce signals with better Phase Noise than producing them directly in the microwave frequency range.

- For example typical Phase Noise of a 10 MHz Crystal Oscillator is: -170 dBc/Hz @ 100 kHz offset.
- Using a multiplier chain ($10 \times 24 = 240$) to get a 2.4 GHz signal, degrades this Phase Noise by $20 \cdot \log(240) = 48$ dB, yielding: $-170 \text{ dBc/Hz} + 48 \text{ dB} = -122 \text{ dBc/Hz}$ @ 100 kHz offset.
- Compare this Phase Noise to a standard LC-tank oscillator working directly at 2.4 GHz, which has a typical Phase Noise of -100dBc/Hz @ 100 kHz offset.

A frequency multiplier circuit should contain a nonlinear device and filters that enable to select the desired component at the output and separate the source from the generated harmonics.



- The nonlinear device will produce voltages of higher order from the current of the first harmonic. One of these voltages is of the desired order and will be allowed to exit through the band-pass filter. Low-pass and band-pass filters will present high impedance to all unwanted harmonic voltages.
- But it turns out that if we allow the currents of the other harmonics to flow, the intermodulation products of those harmonics will contribute to the desired harmonic of the output frequency. That means we should try to short the currents of the non-desired harmonics.
- As we want to deliver as much power as possible to the load the frequency multiplier should be matched at the input (for the input frequency) and at the output (for the output frequency).

To obtain higher order frequency multiplication we can cascade several multipliers. This can increase conversion efficiency but also increases complexity.

There are different possibilities concerning the nonlinear device:

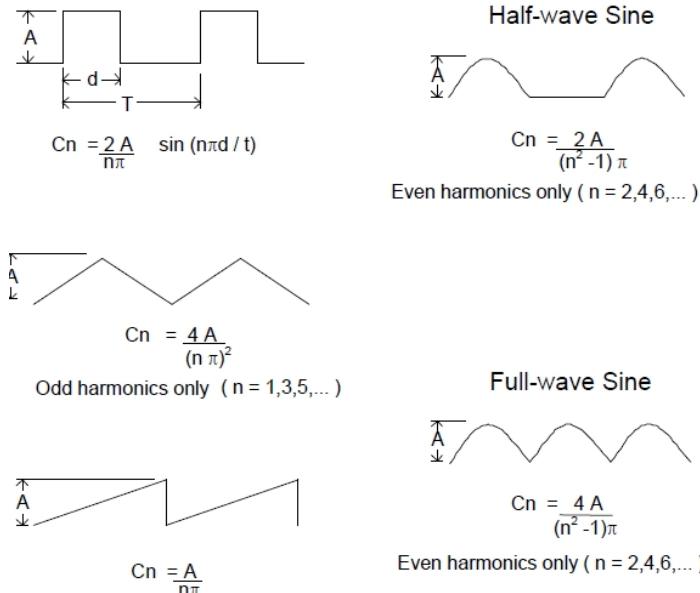
- We need a device with a nonlinear characteristic in order to produce higher order harmonics.
- The nonlinear characteristic might be a nonlinear I-V or C-V relationship.
- Usually wideband multipliers use a nonlinear I-V characteristic, but when we want to design a frequency multiplier with high efficiency, and not high bandwidth, we prefer the nonlinear C-V characteristic. For example a varactor diode has a nonlinear C-V characteristic.

Frequency Multipliers Waveforms

Any non-sinewave repetitive waveform contains energy at harmonics of the fundamental frequency.

The task is to create a non-linear circuit that produces a waveform with significant signal strength at the desired harmonics.

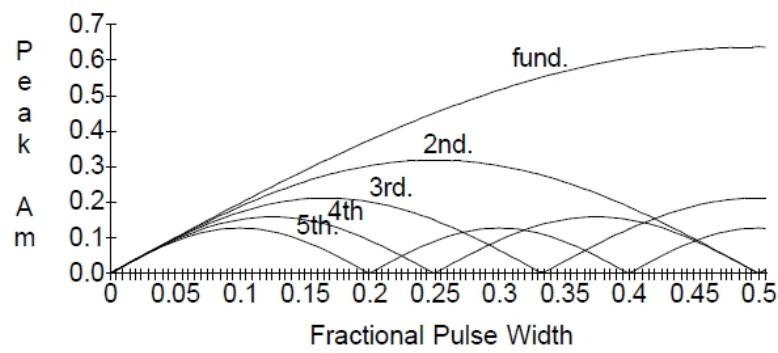
Figure below shows the amplitude terms (peak value of the n^{th} harmonic sine wave) for various waveforms.



Harmonic amplitude terms for various waveforms (C. Wenzel)

- Can be seen that waveforms with fast edges have larger high frequency harmonics.
- Harmonics without vertical edges have n^2 in the denominator, but the waveforms with fast edges only have n in the denominator.
- The timing (duty-cycle) between the positive and negative edges of a pulse determines which harmonics are emphasized. For example, a 50% duty-cycle square-wave has only odd harmonics. In this situation the timing is wrong for the buildup of even-harmonic energy, but a 25% duty-cycle contains large even harmonics: the edges occur at the right time to reinforce certain even harmonics.

Figure below shows the harmonic content of a square pulse as a function of its duty-cycle.



Square Pulse Harmonic content vs Duty-Cycle (C. Wenzel)

As was mentioned before the chart suggests that the most 2nd harmonic energy will be generated when the duty-cycle is 25%. But it can also be seen that if the duty-cycle is increased to 33% then the third harmonic drops to zero which could simplify output filtering with little drop in the desired 2nd harmonic.

Frequency Multipliers Characteristics

- Conversion Loss and Maximum Input Signal Power**

Semiconductor diodes used in microwave frequency multipliers are essentially lossy passive devices and for this reason they dissipate energy. Embedding circuits also dissipate energy. As a result, multiplier's input/output power conversion efficiency is less than unity.

Conversion Loss used to characterize microwave frequency multiplier's conversion efficiency is defined as the ratio of the available source power P_{in_source} to the output harmonic power $P_{out_harmonic}$ delivered to the load.

Conversion Efficiency is defined as the ratio of the output power P_{out} delivered to the load to the available power of the input source P_{in} , and usually is expressed in percent.

The goal of the circuit design is to minimize the conversion loss (or maximize the conversion efficiency) for a given device and input/output frequencies.

When get low conversion efficiency, virtually all the input power is dissipated in the nonlinear element. The maximum input power is limited by the device power handling capability and must be clearly stated when specifying a frequency multiplier.

- Source and Load Impedance**

One of the conditions for a diode frequency multiplier to achieve minimum conversion loss is that optimum source and load impedances should be provided to the diode.

The source impedance should be very close to the complex conjugate of the multiplier input impedance Z_{in} to minimize reflection loss at the input.

The load impedance should be equal to the optimum load value, otherwise leads to an increased conversion loss or decreased output power.

- Bandwidth**

BW represents the output or input frequency range over which conversion loss is in the specified limits.

- Harmonics**

A nonlinear device produce undesired harmonics along with the desired ones, and this might affect the performance of the system where the multiplier is used.

- Noise Conversion**

In all practical situations the resulting noise sidebands are subject of frequency conversion together with the carrier. The multiplier devices add their own noise, and is important to predict the resulting output noise spectrum.

- Phase Noise Conversion**

All frequency multipliers will increase the phase noise by the same factor (N) that they multiply, because frequency and phase are both multiplied. In dB this would be $20 \log N$.

Diode Frequency Multipliers

Diode frequency multipliers can be generally classified as being of varistor (Schottky barrier diode) or varactor type.

In the first case, frequency multiplication is performed by a nonlinear resistance or conductance with consequent poor conversion efficiency but a very large potential bandwidth.

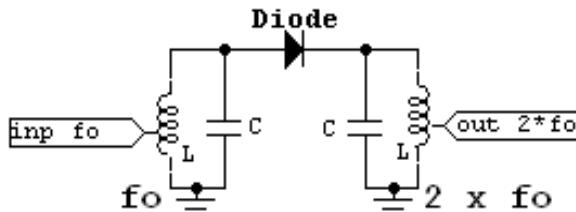
In the varactor case a nonlinear reactive element (with nonlinear capacitance) is used.

Varactor type multipliers have high potential conversion efficiency, but exhibit a narrow bandwidth and a high sensitivity to operating conditions, and sometimes stability problems.

In theory, a cascade of low-order multipliers usually has greater efficiency than a single high-order multiplier, but must consider the additional losses in cascading two multipliers (it is invariably necessary to use an isolator between them), and especially the additional cost.

Resistive (Varistor) Frequency Multipliers

- Resistive frequency multipliers use the nonlinear I-V characteristic of a Schottky-barrier diode to distort a sinusoidal waveform. This distortion generates harmonics.
- The more is distorting the input sinusoid, the greater the harmonic currents in the diode, but the maximum still not very great because resistive frequency multipliers are not very efficient.
- In theory a diode doublers have 6dB conversion loss ($1/N^2$) but in reality the conversion loss is about 10dB and there is no reason to make higher-harmonic resistive multipliers.
- The advantage of resistive multipliers is, they are very broadband.



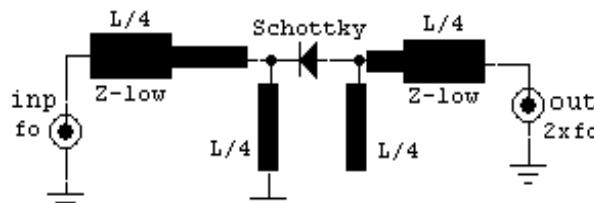
Simplified model of a Resistive (diode) Frequency Doubler

The parallel LC resonators are ideal because they short-circuit the diode at the unwanted harmonics, decoupling the input from the output, and put the diode in parallel with the input at the fundamental frequency and in parallel with the output at the second harmonic.

The inductor can be tapped to optimize the source and load impedances of the diode.

The frequency doubler using microstrip lines presented below is suitable for microwave frequencies.

- The circuit uses a $\lambda/4$ at f_0 , short-circuited through a stub at the input side of the Schottky diode (which is equivalent to $\lambda/2$ at $2f_0$), which is used to create a short-circuit at $2f_0$ to prevent the output power generated in the diode from traveling backward.
- Similarly use a $\lambda/4$ at f_0 open-ended stub at the output side, which creates an RF short at f_0 and causes the input signal penetrating through the diode to be reflected back to the diode.
- A section of the transmission line is used as an inductor to resonate the diode junction capacitance.
- The $\lambda/4$ impedance transformers at the input and output are used to transform 50 ohms source and load to optimum diode impedance terminations.



Microwave Microstrip Frequency Doubler

Varactor Diode Frequency Multipliers

A nonlinear reactance also can distort the sinusoidal signal.

- The pros and cons of varactor multiplier are the opposite of those of resistive multiplier.
- A varactor is capable of higher efficiency and higher power than a resistive multiplier, theoretically 100% for all harmonics, but they are very narrowband.
- A design issue of varactor multipliers is they are extremely sensitive to almost every parameter of the circuit, and small changes in the circuit parameters (tuning reactances, bias voltages, input power level, etc) change the output power.
- Making a varactor multiplier work (and keep working) needs a lot of empirical tuning.
- Varactor diode frequency multipliers in general generate very little noise (phase- as well as amplitude noise). The only noise source is the thermal noise of the series resistance of the varactor and the circuit loss resistances.

- The power capability of a varactor multiplier is limited by the device's break-down.
- The varactor always has a parasitic resistance in series, which dissipates power.

In order to minimize the loss power, one would tend to present an open for all the undesired harmonics, resulting in zero current and therefore no loss.

At the example of the pure square-law diode we see that it produces only a 2nd order harmonic directly. This is the reason to present a short to the undesired (intermediate) harmonics.

- The shorting circuits are called idlers.
- Without idlers the varactor multiplier does not generate harmonics efficiently beyond the 2nd harmonic.
- If a current at the 2nd harmonic is prohibited, we don't get the desired higher order harmonics.
- If current is allowed at the 2nd harmonic, it will mix with the first harmonic and generate therefore higher order harmonics.
- A varactor tripler (x3) can be obtained only with a second harmonic idler.
- A varactor quadrupler (x4) could have a 2nd harmonic idler, or both a 2nd harmonic and a 3rd harmonic idler.
- A varactor quintupler (x5) would likely have at least 2nd and 3rd harmonic idlers.

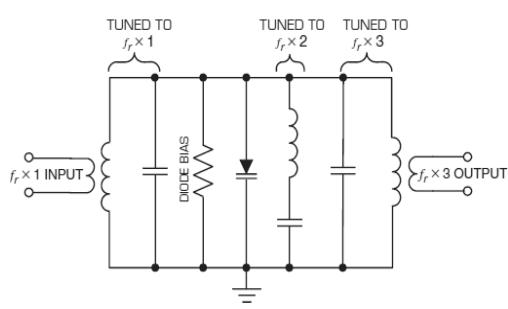
Idlers are usually realized as short-circuit resonators that are separate from the input and output matching circuits.

In practice, idlers are usually realized by a series resonance that is chosen more for its convenience than for high performance.

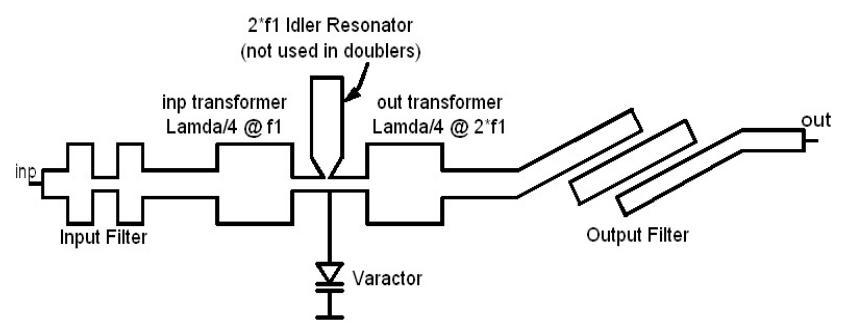
- Frequently, the series resonance of the varactor's package is used as an idler at high frequencies, and tuning elements are often included to tune the resonance precisely to the desired harmonic.
- To minimize power dissipation and thus to obtain high efficiency, is essential to use high unloaded Q (low-loss) idler resonators.
- Both phase noise and amplitude noise are strongly dependent on the level of the input signal pumping the diode.
- Varactor frequency multipliers are relative unstable. Their instability is a kind of chaotic process, not a simple oscillation.

Controlling the broadband embedding impedance characteristic very carefully is the best way to insure good stability. In particular, the input source and output load must be linear and not vary with input or output level. One must not drive a mixer's LO port directly from a multiplier, or the multiplier directly from another multiplier; an isolator should be used. The input and output networks must not have any spurious resonances.

Introducing a resistor in the diode's DC return path, this current can be used to bias the diode. The resistor also helps to reduce the sensitivity of the output power level to the input power level; as input drive is increased, the resulting increase in DC current further reverse-biases the diode, reducing the multiplier's efficiency and leveling the output power. The design of the bias circuit often has a strong effect on stability. Low frequency resonances in the bias circuit are a common cause of instability.



Lumped elements Frequency Tripler



Distributed Elements Frequency Doubler

A variant of varactors are Schottky-Barrier varactor diodes which can obtain output frequencies of up to several hundred of GHz.

- One of the most important advantages of Schottky-Barrier based multipliers is the generation of odd harmonics without filtering the even ones.
- This capability is based on the symmetry of the electrical characteristics for unbiased devices. Thus, the load impedances for even harmonics have no effect on the efficiency characteristic.

Step Recovery Diode and PIN Diode Frequency Multipliers

Step Recovery Diodes (also called snap-off diodes) are based on a PIN configuration.

They are commonly employed in the design of frequency multipliers of high order.

Step Recovery Diodes have relatively little capacitance change under reverse bias and are used for higher efficiency applications.

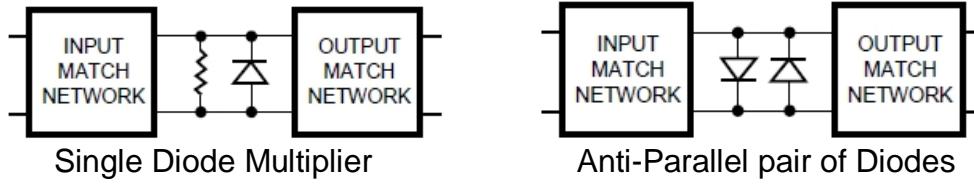
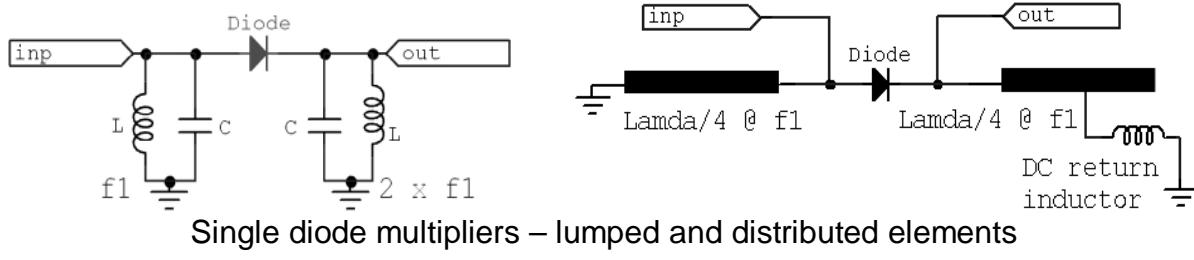
A conventional step recovery diode multiplier consists of a diode, a biasing resistor, and matching filters at input and output. The output filter reflects the un-tuned harmonics back to the diode where they mix to form additional power at the tuned frequency.

- Step Recovery Diodes do not require idler circuits to enhance efficiency (as varactors).
- The SRD multiplier is a reactive multiplier and theoretically doesn't have the efficiency limitation ($1/N^2$) as resistive multipliers.
- In the design of high-order frequency multipliers, the efficiency of Step Recovery Diodes is much higher than that of varactor diodes. There is, however, a limit to the output frequency of the multiplier circuit.

Single Diode multiplier is useful mainly for low-cost, low-performance applications or high frequency waveguide structures where fundamental frequency is easy to reject. A single diode multiplier has the advantage of easy to provide DC bias to it, which will help optimizing the multiplier.

A conventional diode multiplier can use one diode or an anti-parallel pair of diodes.

The additional diode results in the suppression of even order products, the enhancement of odd order products, and the elimination of the bias resistor.

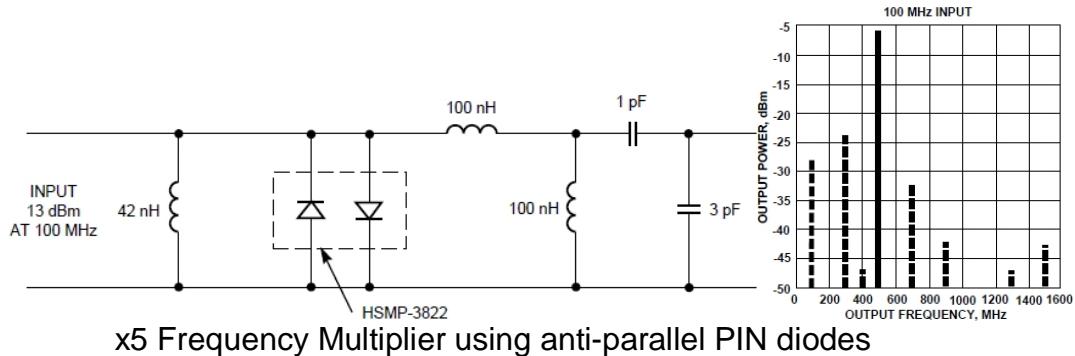


Balanced Diode Multipliers have significant advantages compared to single-ended multipliers; the most important are increased output power and inherent rejection of the fundamental frequency and of certain unwanted harmonics.

The input or load impedance of a balanced multiplier in some cases differs by a factor of two from that of a single-diode multiplier; therefore, a balanced multiplier sometimes provides more satisfactory input or load impedance.

The antiparallel diode connection is probably the simplest form of a balanced multiplier; it rejects even harmonics of the input frequency and consequently can be used only as an odd-order multiplier.

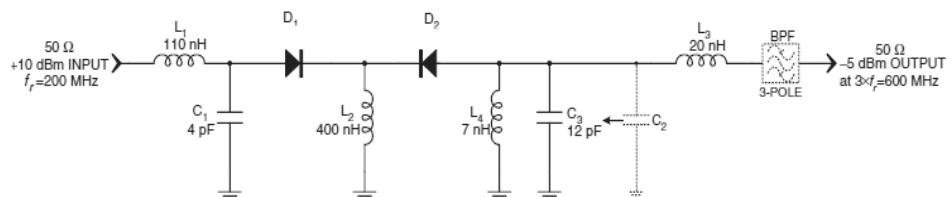
In an antiparallel-diode multiplier, each diode effectively short circuits the other at the second harmonic, so each diode acts as a type of idler for the other. This circuit does not reject the fundamental frequency, however, so it requires an output filter.



x5 Frequency Multiplier using anti-parallel PIN diodes

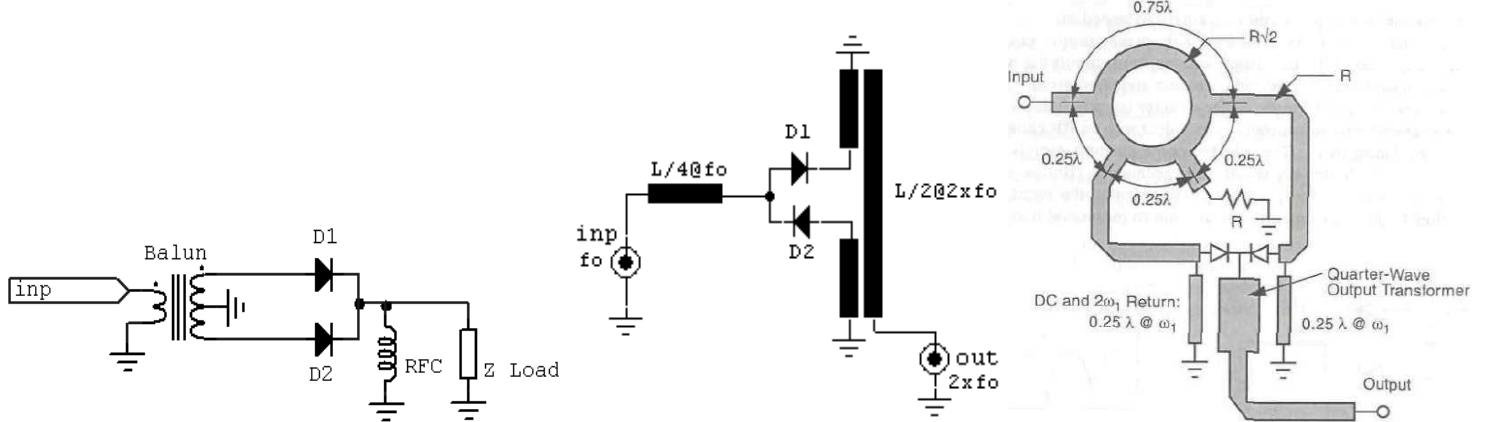
The above circuit is an x5 multiplier operating from a 100 MHz input at +13 dBm, and frequency output at 500MHz and level at about -6dBm. The input was matched with a shunt inductor, and other passive components were added to the output to provide filtering of unwanted signals.

Because the stability of a varactor multiplier is sensitive to small unbalance between the diodes, varactor multipliers are rarely realized as anti-parallel circuits.



Frequency Tripler using Step Recovery Diodes

The circuit below shows a singly balanced multiplier using a balun transformer. The difference compared to a DC power supply circuit (which looks like) is, that in a power supply we are looking only for DC component, filtering all the harmonics, when here we are looking for 2nd harmonic, shorting the DC current using an RF choke.



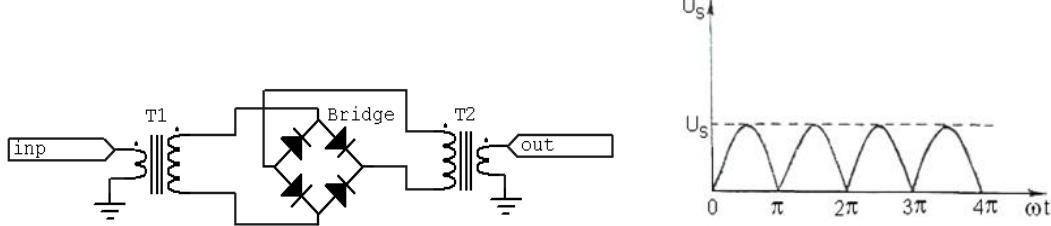
Singly Balanced frequency doublers using: Transformer balun, Microstrip balun and Rat-Race Hybrid

The **Bridge Rectifier** circuit is a practical way to realize resistive frequency doublers.

The design of these multipliers is not the same as the design of a diode ring mixer because the diodes are connected as in a different manner. The ring mixers require baluns when the bridge rectifier requires transformers.

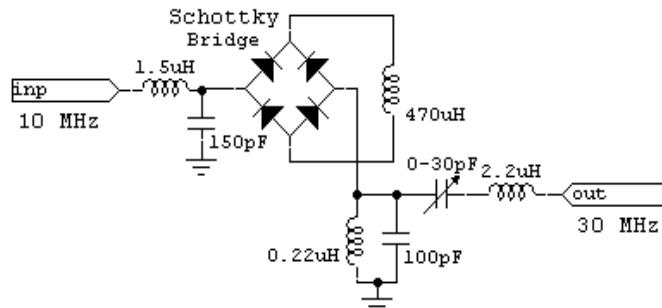
The voltage and current waveforms in the balanced bridge multiplier are identical to those of a full-wave rectifier in a DC power supply. The current consists of a train of half-sinusoidal pulses, which has no odd harmonic components.

Thus, the multiplier inherently rejects the two most troublesome harmonics, the first and third, and the fourth is usually weak enough to require little or no filtering.



Bridge Diode Frequency Doubler

Charles Wenzel got an RF Design Award for the bridge frequency tripler presented below.



Wenzel Bridge Diode Frequency Tripler

How the circuit works:

- The heart of the multiplier is a sinewave to squarewave converter circuit, which basically is simply a full-wave bridge diode (Schottky barrier) with an inductor short-circuiting the DC terminals.
- The inductor is chosen to have high impedance at the operating frequency so that an AC input results in DC in the inductor.
- This DC flows through alternate pairs of diodes due to the commuting action of the input voltage.
- Therefore, if one AC terminal of the bridge is driven with low impedance sinewave, the other AC terminal will supply a squarewave to a low impedance load.
- The load must have low impedance since the compliance of this current source is exactly equal to the input voltage.
- Because the diodes switch at the input signal's zero crossing the circuit introduce a minimum of AM/PM conversion.
- The input matching network it provides a low impedance to ground for the switching current; and it isolates the input from the switching current.
- The output network presents the required low impedance to the bridge while directing the desired harmonic to the output.
- The conversion efficiency is as high as diode frequency doublers, even though the multiplication factor is higher.

Active Frequency Multipliers

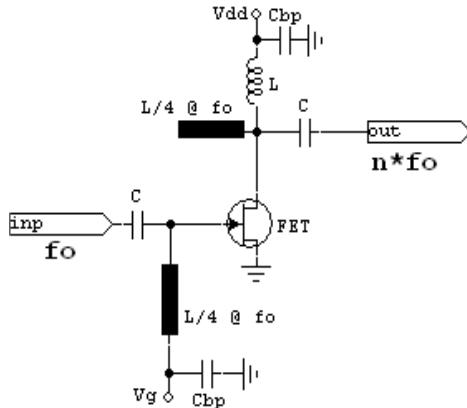
The main reason using active frequency multipliers is they got better efficiency compared to diode frequency multipliers, at the expense they have worst noise levels compared to varactor diodes. In contrast to diode multipliers which always exhibit loss, FETs or BJTs multipliers can achieve conversion gain over broad bandwidth while getting also good DC to RF efficiency.

The same as amplifiers the active frequency multipliers work in different classes.

A practical form for an active frequency multiplier is to operate in equivalent Class-B power class, where they are very stable and have good gain, efficiency, and output power.

- An active FET frequency multiplier generates harmonics by rectifying the sinusoidal input signal when it is biased near its turn-on point (pinch-off), and the input sinusoid turns the device on over part of its cycle.
- The condition is obtained by applying a positive drain voltage and a negative voltage to the gate. A practical application is to replace the negative supply to a self-bias source resistance, and a gate grounding resistor.
- The duty cycle of the input signal is adjusted to maximize the desired output harmonic.
- The higher the harmonic, the shorter the duty cycle must be.
- For a frequency doubler the optimum duty cycle is about 25% (1/4) when for a frequency tripler is about 16% (1/6).

Figure below shows the circuit of a basic broadband frequency multiplier that uses an ideal FET.



Broadband Active Frequency Multiplier (FET)

- The output resonator is tuned to the n^{th} harmonic of the excitation frequency, so it short circuits the FET's drain at other frequencies, especially the excitation frequency (f_0) by using an $\lambda/4$ open stub.
- The gate-bias voltage V_g in an efficient FET multiplier must be equal to or less than (more negative than) the threshold voltage, V_t . In this case the FET's channel conducts only during the positive half of the excitation cycle, and the drain conducts in pulses; the shape of the pulses is approximately a rectified cosine.
- The duty cycle of the pulses varies with the DC gate bias, V_g .
- If $V_g = V_t$ the duty cycle is 50%,
- If $V_g < V_t$ (the usual situation), the FET is turned off over most of the excitation cycle. The duty cycle in this case is less than 50%.
- If V_g is much smaller than V_t the magnitude of the peak reverse voltage establishes a limit on the difference.

The second important bias point (after Class-B) is with zero gate voltage, which sometimes is referred as Class-A multiplier. This bias point should give the same performance as the pinch-off, if the gate voltage swings from zero to pinch-off and a low-impedance is connected to the drain.

Microwave transistors are unconditionally stable only within certain frequency ranges, usually above a certain minimum frequency, and we know that the load termination at the fundamental frequency has a major effect on circuit stability.

- Because the load termination controls the series and parallel resonance of the transistor parasitics, and is controlling the peak of the rectified current or the distorted drain voltage, it will affect the multiplier gain, input impedance and bandwidth.
- The proper drain termination is the one that induces the highest peak current. This is obtaining by short-circuit at the fundamental frequency. Ideally the load should be short circuit at all harmonic

frequencies, but the presence of a load at a specific harmonic deviates the signal trajectory in the input plane and the load line becomes a function of frequency.

- Sometimes using other terminations, especially an open-circuit drain termination at the fundamental frequency, has advantages over a short circuit. The primary advantage of using other terminations is that greater gain can be achieved, although the increase in gain usually is the result of undesirable feedback and getting unpredictable oscillation.
- To get a good conversion gain the input power should not be very high. The required input power is proportional to square of f_0 (f_0^2), so the required input power increases 6 dB per octave; or, in other terms, the available gain decreases by 6 dB per octave. If the input is well matched across a broad bandwidth, a gain slope inevitably results.

The generation of harmonics using FET transistors can be done not only from current or voltage clipping, but also due to mixing of fundamental frequency, and any one of the generated harmonics.

One way to use mixing is to reflect all generated harmonics back to the drain and the other is to feed them back to the gate.

- The initial step in an active multiplier design is to find the performances of the active device at fundamental frequency, looking to parameters as: transconductance gm , transition frequency f_t , and the maximum oscillation frequency f_{max} .
- The transconductance (gm) has a direct impact in the device's power performance and multiplication gain, and f_t and f_{max} determined the limits to be used as a frequency multiplier.

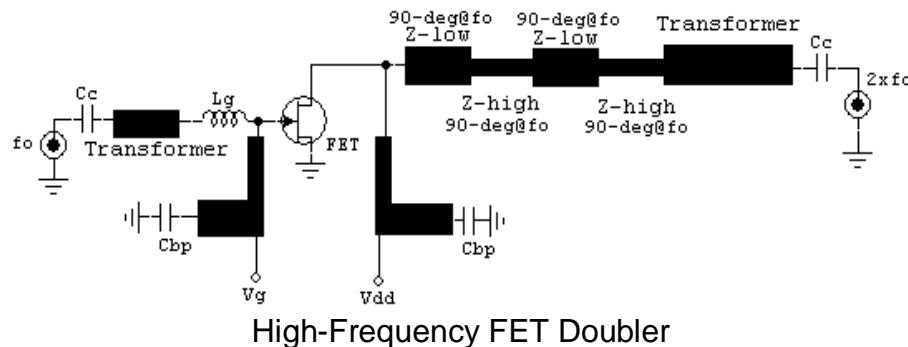
Harmonic Load Pull Test

This is a method which employs no device model and is essentially an experimental process. This method is very useful designing a nonlinear frequency multiplier.

- The active device is inserted into a circuit that has the input tuned at the fundamental frequency and the output tuned at the desired harmonic frequency.
- The active device is than removed and the matching networks are measured using a Vector Network Analyzer, getting the desired impedances which to be applied to the device.
- After that, a conventional linear simulator could be used to synthesize the matching network.

Frequency FET Doublers

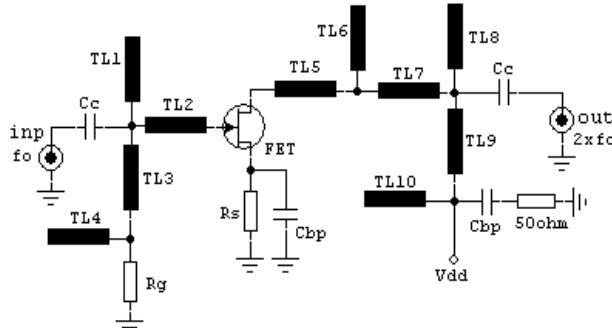
Below is presented a **High-Frequency Doubler** using a high frequency FET transistor.



- To get good input VSWR and maximum power transfer, the input is conjugate matched using microstrip distributed and lumped elements.
- For moderate bandwidth (less than 30% of the center frequency), can resonate the input capacitance with a series inductor. For uniform conversion gain may need to match the input best at highest frequency of the band.
- The output matching network it consists of a filter, to short-circuit the drain at the fundamental frequency and unwanted harmonics, followed by a matching transformer.

- A half-wave filter is ideal for the output; it consists of a cascade of alternating high- and low-impedance transmission-line sections, each $\lambda/4$ long at f_0 ; these sections are $\lambda/2$ long at 2^*f_0 and $3\lambda/4$ long at 3^*f_0 . So, the frequencies of maximum rejection occur at f_0 and 3^*f_0 , but the filter has no rejection at the output frequency 2^*f_0 .
- The imperfect output termination could make the multiplier unstable and cause fundamental frequency leakage.

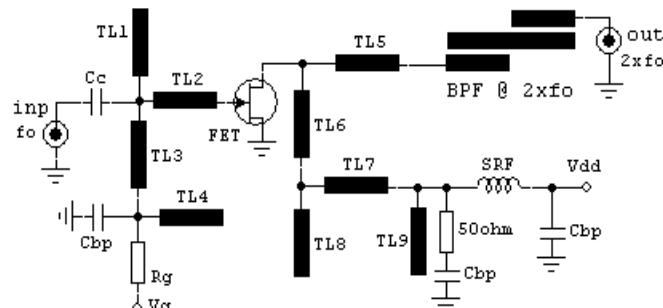
The **Narrow-band Frequency Doubler** presented below contains the matching transmission line elements TL1 and TL2, and the bias filter elements TL3 and TL4.



Single Ended Frequency Doubler – Narrowband

- The drain circuit use the transmission line phase-shifter TL5 to adjust the phase of the fundamental frequency impedance, and a harmonic band pass filter.
- The output BPF it is composed of $\lambda/4$ transmission lines TL6, TL7 and TL8, which block the fundamental frequency and the 3rd harmonic, and present 50 ohms termination at the 2nd harmonic.
- The electrical angles (phase) of the gate and drain transmission lines, TL5 and TL6, affect the multiplication gain up to 3dB.
- The drain bias filter is composed of elements TL9 and TL10 and their function is to isolate the bias from the generated 2nd harmonic.
- The RC circuit in parallel with the power supply is for overall stabilization.

The **Wide-band Frequency Doubler** presented below use a transmission line (TL5) in series with the output BPF to adjust the phase of the impedance at the fundamental frequency.



Single Ended Frequency Doubler - Wideband

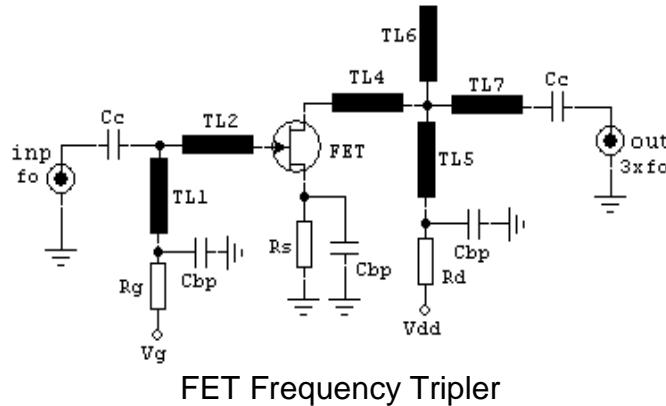
The BPF rejects the fundamental and the 3rd harmonic frequencies. There is also a band-stop filter (TL7, TL8, TL9) which blocks the 2nd harmonic, and presents low-loss at fundamental and 3rd harmonic.

Frequency FET Triplers

An important difficulty in frequency triplers is the need to short circuit the drain at the unwanted harmonics.

- For example a frequency doubler is easy to do using a $\lambda/4$ stub, which effectively shorts the first and third harmonic, while the fourth and higher harmonics are weak enough to neglect. But is not very simple for terminating the drain in a frequency tripler.
- The output network can be difficult to design; the inevitable result is a suboptimum termination, which makes very hard to optimize efficiency and get the risk of instability.

This is an example of a FET frequency tripler:



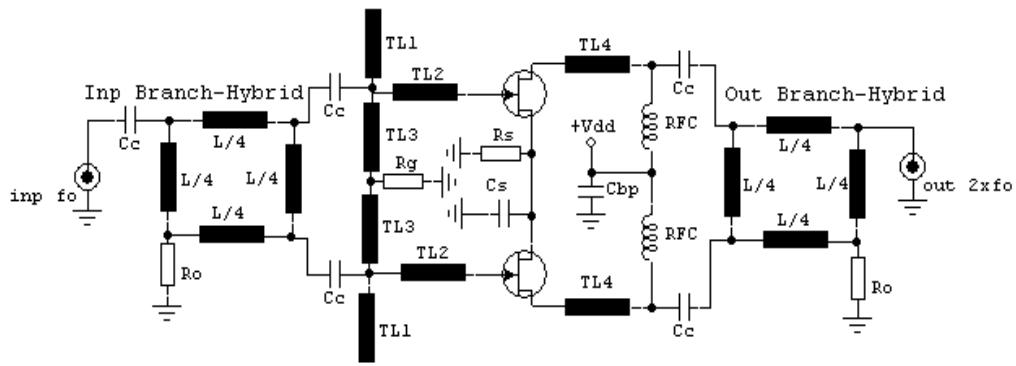
FET Frequency Tripler

- The input stub, grounded at high frequencies by a capacitor, provides a match for the fundamental input frequency, while in the same time it facilitates bias injection at the gate of the FET device by providing some decoupling.
- The bias scheme adopted for the frequency tripler was a self-bias arrangement with resistor between source and ground. Such a self-bias configuration tends to bias a FET device towards pinch-off, with the resistor value determining how close the device is to pinch-off. The larger the value of the closer the bias point is to pinch-off. If the gate bias is connected to an external supply, an option effectively to over-write the self-bias setup is made available.
- At the output, a double stub arrangement has been placed. These stubs get multiple functions. First, they form an output match for the desired 3rd harmonic signal. Secondly, they implement some filtering of undesirable fundamental and 2nd harmonic leakage to the output. Using here the real life stubs, it can be difficult to filter the fundamental without rejecting the desired 3rd harmonic at the same time. This happened when considers the simplest stub arrangement to reject the fundamental, which is an open circuit $\lambda/4$ stub. However, such a stub is long $3\lambda/4$ at the 3rd harmonic and tends to reject this frequency as well. As a consequence, the design of the output stub pair involved a compromise in terms of fundamental and 2nd harmonic rejection, without excessively loading the 3rd harmonic response.
- The output stubs is essentially a short circuit stub, the high frequency short being provided by a capacitor to ground. This stub also facilitates drain bias injection.

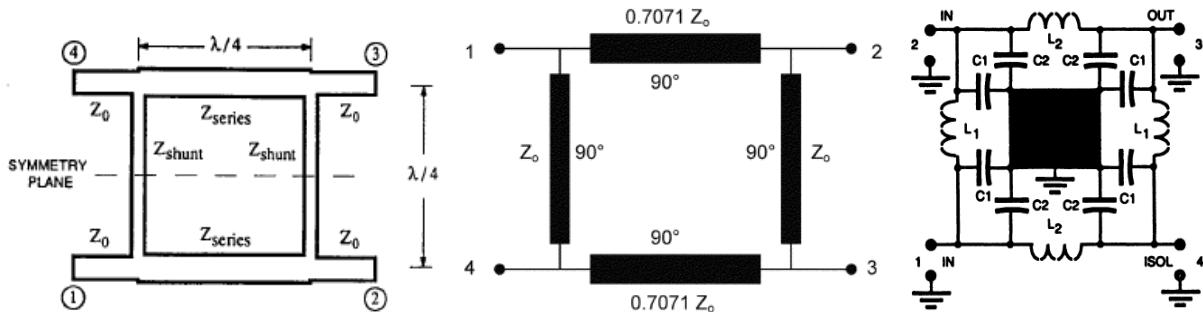
Balanced Frequency Multipliers

Reasons using of Balanced Frequency Multipliers are:

- they have improved input match over wide bandwidth,
- they have good isolation between multiplier stages,
- they are very stable since the device is terminated in 50 ohms over a wideband frequency.



Balanced Frequency Doubler using Branch Line Hybrids



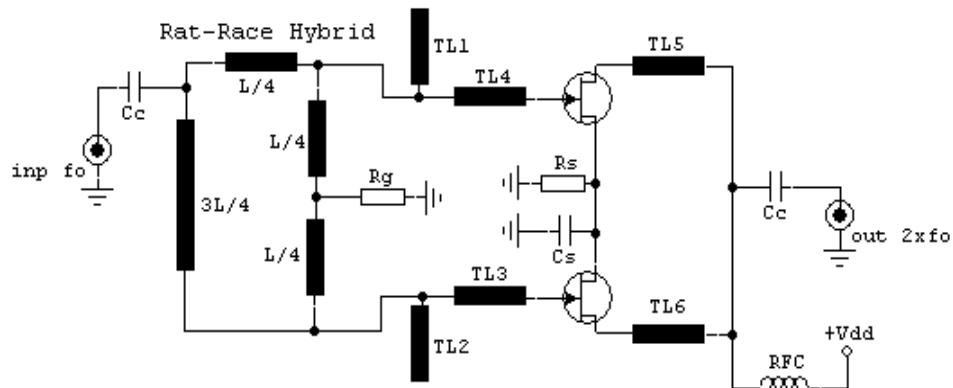
Branch Line Hybrid and the Distributed and Lumped equivalents

- The input hybrid coupler introduces a 90° phase shift and the output hybrid another 90° .
- Therefore, the odd harmonics are 180° out of phase, are cancelled at the output port, and dissipated at the coupler termination.
- The even harmonics at the output port are in phase and added in power.
- A balanced multiplier has 3dB greater output power than an equivalent single-device circuit.
- The main bandwidth limitation is given by the FETs input and output matching networks not matched for wideband response.
- The circuit is self-biased using TL3 and Rg gate to the ground and Rs as source resistor. The bias is chosen to be near pinch-off point.

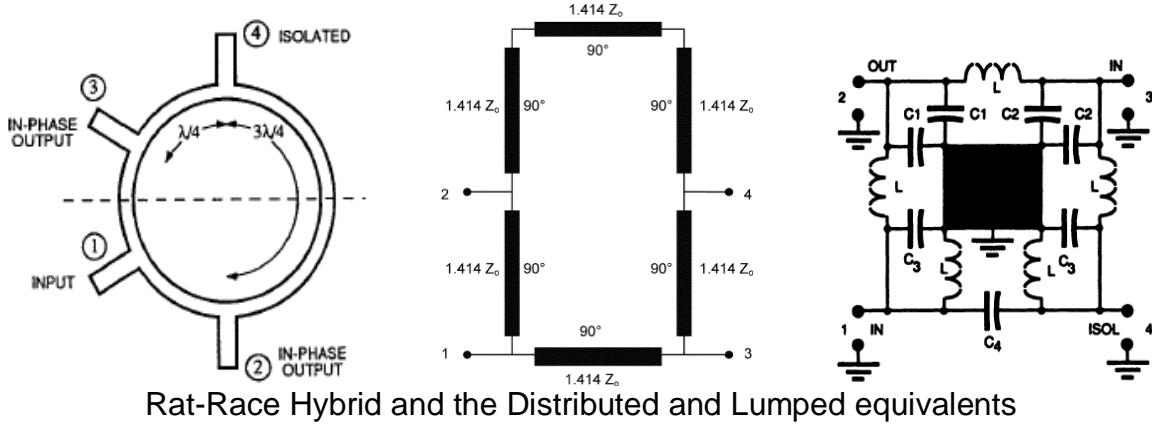
Balanced to Unbalanced Frequency Doubler

Another option is to use only at the input a 180° Rat-Race hybrid to drive each device in anti-phase.

- In this way the fundamental drain currents are also in anti-phase and good rejection is obtained by paralleling both drains, and the drain connection point becomes a virtual ground for fundamental and for all odd harmonics.
- The even harmonics of the drain currents in the two FETs have no phase difference, however, so the drain-current components at those frequencies combine in phase at the output.



Balanced to Unbalanced Frequency Doubler using Rat-Race Hybrid

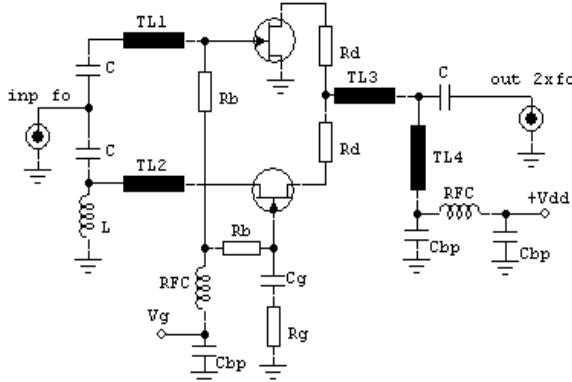


Rat-Race Hybrid and the Distributed and Lumped equivalents

- To get a constant gain at the output, the gates matching networks are designed for maximum gain at fundamental high-end and around 3dB less gain at the low-end of the useful band.
- The disadvantage of this topology is sensitivity to device DC imbalances and input matching networks, compared to the balanced multiplier using hybrids at both, input and output.
- Any imbalance is reflected back to the generator requiring an attenuator at the input to minimize the resulting standing wave.

Balanced Frequency Doubler using Active Balun

The frequency doubler using an active balun presented below is suitable for small size circuits, replacing the passive balun topologies.

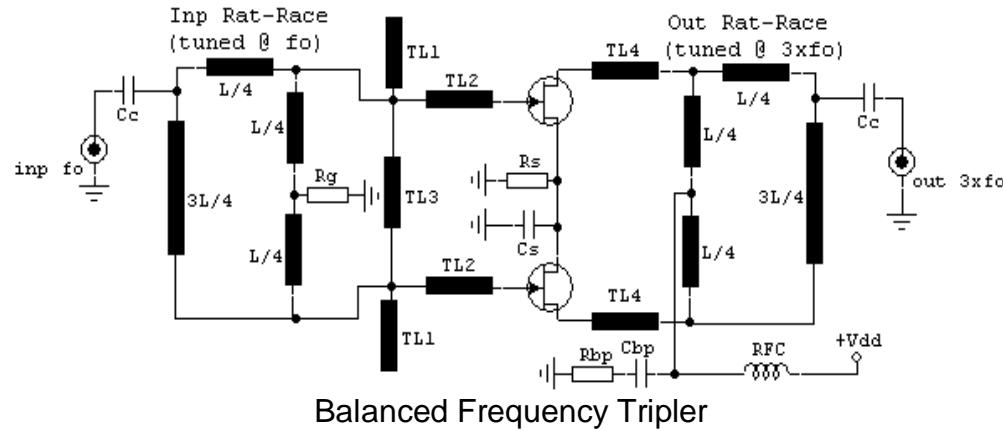


Balanced Frequency Doubler using Active Balun

In this frequency doubler, a simple combination of Common-Gate FET and Common-Source FET provides the required 180° phase difference for the cancellation of the fundamental.

- This active balun has the advantage getting small size at low frequencies.
- The stability has to be controlled, in contrast to a passive balun, and the circuit should be unconditionally stable for all input impedance attached.
- To get unconditional stability and to avoid negative resistances at gate and drain of the Common-Gate FET, a series resistance R_g , is added to gate. This reduces the gain, but it improves stability by decreasing the loop gain at the same time. In addition, two series resistors R_d are added in both drain connectors to decrease the loop gain.
- The frequency doubler has a short-circuited stub TL_4 and a series transmission line TL_3 for an output impedance adjustment at the connection of the two drains. These elements provide a short for the fundamental and additional match for the 2^{nd} harmonic.
- The bias point was chosen at $V_g=0$ to obtain high fundamental suppression and 2^{nd} harmonic.

Balanced Frequency Tripler



- The input match is made with open-circuited stubs TL1, and high-impedance lines TL2.
- The $\lambda/4$ TL3 connecting both inputs introduces a short at the 2nd harmonic, improving the performance.
- The output match contains only a $\lambda/4$ high impedance transmission lines TL4, to parallel tune the drain output impedance at the fundamental frequency.
- The device is self-biased and the source resistor Rs is decoupled with Cs.

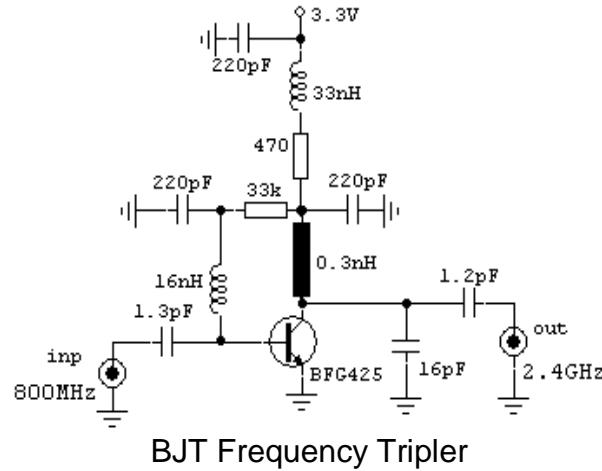
Higher Order FET Frequency Multipliers

- The direct generation of harmonics of higher order can be obtained by biasing the device at different conduction angles.
- For even order the device is biased in Class-AB similar for frequency doubler, in order to maintain a rectified sinusoidal drain current which is reach in even harmonics.
- For odd order harmonics the optimum bias condition is the one that generates an output waveform with distorted positive and negative peaks. The first option would be to bias the device in Class-A, about the center of the drain current, and apply a high power at the gate.
- The magnitude of higher harmonic components like 5th, 6th, 7th, etc, becomes too small, requiring a high load resistance to compensate the reduction in output power.

BJT Frequency Multipliers

The theory of bipolar multipliers is essentially the same as that of FET multipliers. A few notes on the differences, however, are in order.

- Unlike FETs, whose channel currents are limited to a little over $Idss$, bipolar devices do not have such a strict limit.
- Silicon BJTs experience high-level injection effects, which tend to limit the peak current and reduce transconductance at high collector current.
- Bipolar devices have a large, strongly nonlinear base-to-emitter capacitance. Because of that capacitance, BJT multipliers are susceptible to modes of oscillation that are not unlike those of junction varactor multipliers for example. As with varactors, the best (and simplest) way to avoid such instability is to short-circuit the base and drain at all unwanted harmonics. Have to verify also that active DC bias supplies do not exhibit negative resistance or couple the collector to the base at low frequencies.
- Because multiplying devices are turned off under quiescent conditions, BJT multipliers should not be current-biased; they must be biased from a voltage source, ideally with a series resistance.

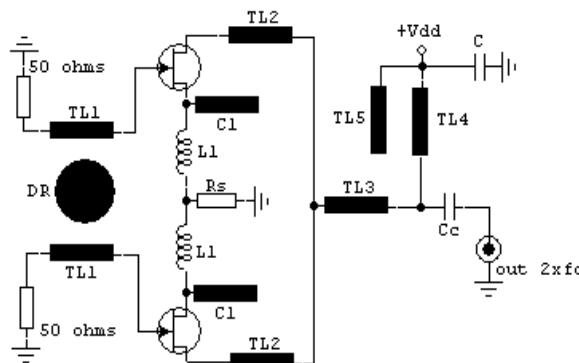


BJT Frequency Tripler

Balanced Push-Push Harmonic Oscillator

Another option generating high frequency signal, using most of the characteristics of the frequency multipliers, is the Harmonic Oscillator.

Below is presented an example of a balanced harmonic oscillator.



Balanced Push-Push Harmonic Oscillator

- The push-push harmonic oscillator employing two transistors, each oscillating at one half the desired output frequency.
- The transistors oscillate out-of-phase with respect to each other, causing the fundamental frequency to cancel and the second harmonic to add in phase.
- Push-push designs have several advantages over other topologies. Designing at one half the frequency increases resonator Q, decreases the parasitics which appear, and extends the useful frequency range of transistors.
- The dielectric resonator is placed between the two gates transmission lines (TL1)
- Biasing the circuit in Class-AB, guarantees the start-up and stable oscillation, and also the generation of even harmonics at the output.

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Modeling and Design Aspects of Millimeter-Wave and Submillimeter-Wave Schottky Diode Varactor Frequency Multipliers

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Abstract—Design and optimization of Schottky varactor diode frequency multipliers for millimeter and submillimeter wavelengths are generally performed using harmonic balance techniques together with equivalent-circuit models. Using this approach, it is difficult to design and optimize the device and multiplier circuit simultaneously. The work presented in this paper avoids the need of equivalent circuits by integrating a numerical simulator for Schottky diodes into a circuit simulator. The good agreement between the calculated and published experimental data for the output power and conversion efficiency originates from the accurate physical model. The limiting effects of multiplier performance such as breakdown, forward conduction, or saturation velocity are discussed in view of the optimum circuit conditions for multiplier operation including bias point, input power, and loads at different harmonics. It is shown that the onset of forward or reverse current flow is responsible for the limitation in the conversion efficiency.

Index Terms—Frequency multipliers, harmonic balance technique, numerical modeling, Schottky diode modeling, semiconductor simulation, submillimeter-wave multipliers.

I. INTRODUCTION

VARACTOR frequency multipliers play a vital role in developing all-solid-state power sources at terahertz frequencies. The key points in the progress of the performance of Schottky varactor frequency multipliers have been the enhanced physical insight into and optimization of submillimeter-wave Schottky diode operation [1], the improvement in frequency multiplier analysis methods since the original work of Siegel and Kerr [2]–[5], and in physical analytical Schottky diode models [5]–[9], as well as numerical physical device models [4], [10]–[12]. The performance of active devices is defined not only by their inherent characteristics, but also by the embedding circuit. This coupling can be taken into account by including a numerical physical model into a circuit simulator [10], [11], [13]. The main problem in frequency varactor circuit design today is the inability to reproduce the experimental results

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without additional empirical parameters. Furthermore, the limitations of multiplier operation at high powers and/or high frequencies is not well understood. Finally, a predictive design and circuit analysis tool is still missing, which is essential for the design of integrated frequency multipliers.

The scope of this paper is to present a circuit analysis tool, which works without empirical parameters and is able to predict the required device and circuit parameters of a frequency multiplier. We focus on the circuit design and operation aspects of frequency multipliers for millimeter and submillimeter bands. As a design tool, we employ the harmonic balance method (HBM) together with a physics-based drift-diffusion (DD) numerical device simulator. Our simulator incorporates accurate boundary and interface conditions for high forward as well as reverse bias, including impact ionization, nonconstant recombination velocity, self-consistent incorporation of the tunnelling, and image-force effects [11]. The validation of the numerical simulator has been performed by comparison of simulated device and circuit characteristics with experimental results obtained for submillimeter-wave Schottky diodes fabricated at the Technical University Darmstadt (TUD), Darmstadt, Germany, and the University of Virginia (UVa), Charlottesville, and for a number of multiplier circuits published in the literature [4], [5].

The integration of numerical simulators for active devices into circuit simulators avoids the need of an equivalent-circuit model extraction. This new philosophy accounts for the device–circuit interaction and provides another degree of freedom to improve the performance of circuits because they can be designed from both a device and circuit point-of-view.

The simulation tool utilized in this paper and its implementation are presented in Section II. The validation of the tool is outlined in Section III, including a comparison of measured dc and RF performance characteristics with simulated values. In Section IV, an analysis of the performance of the frequency multipliers is presented together with an identification of the limiting mechanisms. Simulated results and a detailed discussion for the limiting mechanisms are provided in Section V, including breakdown and velocity saturation effects. Based on these results, the synthesis of an optimum doubler and tripler circuit is dealt with in Section VI. The optimization of the device parameters such as doping concentration and profile, layer thicknesses, etc. are omitted in this paper, but will be dealt with in a future paper. This paper concludes with a summary of the results.

II. SIMULATION TOOL BASED ON PHYSICAL DEVICE MODEL

The HBM is the most common technique for the design of large-signal nonlinear microwave circuits. The HBM depends critically on the accuracy of the nonlinear element model employed in the analysis. This model must be valid for a wide range of frequencies, drive levels, and embedding impedances. The electrical and RF performance characteristics of submillimeter-wave Schottky diodes and frequency multiplier circuits investigated here are based on an accurate physical model, which combines DD current transport with thermionic and thermionic-field emission currents imposed at the Schottky contact.

The model for the carrier transport throughout the bulk is based on an extended one-dimensional (1-D) DD formulation [14]. 1-D simulations are adequate for the current flow under the Schottky metal, whereas two-dimensional (2-D) effects like current spreading can be accounted for by analytical formulas. The governing equations are Poisson's equation and continuity equations for electrons and holes as follows:

$$\nabla \cdot (\epsilon \nabla \varphi) = -q(N_d^+ - n + p) \quad (1)$$

$$\nabla \cdot J_n - q \frac{\partial n}{\partial t} = q(R - G) \quad (2)$$

$$J_n = -q\mu_n n \frac{d}{dx}(\varphi + \varphi_n) + kT\mu_n \frac{dn}{dx} \quad (3)$$

$$J_{\text{tot}} = J_n + J_p + J_{\text{disp}} = J_n + J_p + \epsilon \frac{\partial E}{\partial t} \quad (4)$$

$$\varphi_n = \frac{\chi}{q} + \frac{kT}{q} \ln N_c + \frac{q}{16\pi\epsilon x} \quad (5)$$

where φ is the electrostatic potential, ϵ is the permittivity, and n, p, N_d^+ are the electron concentration, hole concentration, and ionized impurity donor concentration, respectively. J_n , R , and G are, respectively, the electron conduction current density, the recombination rate modeled by the Schockley–Read–Hall recombination, and the generation rate currently restricted to impact ionization [14]. Further, μ_n , T , χ , and N_c represent the field-dependent electron mobility, temperature, affinity, and density of states in the conduction band, respectively. Similar equations also hold for holes. In (5), the conventional formulation of the position-dependent conduction band potential is augmented by the image force term. In contrast to previous publications, we do not introduce direct barrier lowering of the Schottky barrier height [15]. The simulation domain is divided into a nonuniform mesh of approximately 100 mesh points and the simulation time is of the order of minutes for one frequency point.

A. Boundary and Interface Conditions

Dirichlet boundary conditions are imposed at all metal contacts for Poisson's and carrier continuity [14]. In the present model, thermionic and thermionic-field transport at the Schottky barrier is introduced by means of an interface condition at the maximum of the barrier at the point x_m [16].

The position of the maximum is no longer at the metallurgical Schottky contact because of the influence of the bias-dependent image force lowering. The interface condition for the carrier transport is based on the assumption that the carrier distribution can be modeled by a displaced Maxwellian

$$J_n = qn(x_m)v_n - qn_0(x_m)v_r. \quad (6)$$

Here, $n(x_m)$ is the electron concentration at the maximum of the barrier and $n_0(x_m)$ represents a *quasi-equilibrium* density of electrons—the density that would be present at the top of the barrier if the electrons could be brought into thermal equilibrium without disturbing the potential distribution. v_r is the classical recombination velocity $v_r = \sqrt{(kT/2\pi m_e)}$. v_n is the recombination velocity after assuming a displaced Maxwellian shifted by a drift velocity v_{drift}

$$\begin{aligned} v_n &= v_r \cdot F(\xi) \\ &= v_r \left[\exp(-\xi^2) - \sqrt{\pi}\xi \operatorname{erfc}(\xi) \right] \end{aligned} \quad (7)$$

$$\xi = v_{\text{drift}} \sqrt{\frac{m_e}{2kT}} \quad (8)$$

$$v_{\text{drift}} = \frac{-J_n}{qn(x_m)}. \quad (9)$$

In this formulation, it has been assumed that the Schottky contact is located at $x = 0$. This interface condition prevents the unphysical effect of carrier accumulation at the interface [17], [18]. Between the point x_m and the metallurgical contact, the potential is assumed to vary linearly. No mesh points are required here for the calculation of the potential and current densities. Newton's method, Gummel's method, as well as a hybrid Newton/Gummel solution method are used for the solution of (1)–(5) with the interface conditions given in (6)–(9).

Tunnelling transport through the barrier is important for Schottky diodes with high doping in the epitaxial layer. In our model, the time-independent Schrödinger equation is solved for arbitrary piecewise-linear potential barriers using the transfer matrix approach [19], [20]. The grid defined for Poisson's equation is also used for Schrödinger's equation in the volume of the device, but a number of additional grid points are generated between x_m and the metallurgical contact in order to accurately resolve the shape of the conduction band in this region. The new expression for the current density can be represented by a simple integration [21] if the transmission coefficient $T(E_n, E_t, V)$ is independent of the transversal component of the kinetic energy E_t and the distribution function is of Maxwellian type for the transversal component of the kinetic energy

$$J_n = \frac{A^* T}{k} \int_{E_{\min}}^{\infty} T(E_n, V) \left[f_s(E_n, V) - f_m(E_n) \right] dE_n \quad (10)$$

$$E_{\min} = \max \left\{ E_{F_m}, \min \{E_c\} \right\} \quad (11)$$

where A^* is the Richardson constant, T is the lattice temperature (carrier heating is not considered), $T(E_n, V)$ is the trans-

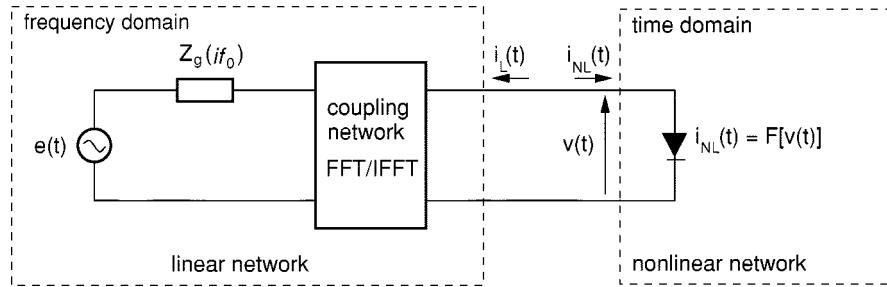


Fig. 1. Schematic drawing of the partitioning of the physical model and linear circuit for the harmonic balance calculations.

mision coefficient for the tunnelling transport, E_n is the energy for the normal component of the carrier velocity, f_s and f_m are the electron distributions in the semiconductor and metal, respectively, E_c stands for the conduction band in the semiconductor, and E_{Fm} is the Fermi level in the metal. We have assumed that f_s is a displaced Maxwellian distribution and f_m is a Maxwell-Boltzmann distribution. If tunnelling is not considered, this equation is similar to that proposed in [16].

B. Coupling the Physical Device Model with Circuit Simulation

Active devices are usually modeled as lumped equivalent circuits in commercial harmonic balance codes. There exist several algorithms for the HBM [2], [22], [23], some of which have been specifically designed to deal with physical device simulators [24]. The selected algorithm for this study is based on the solution of a system of nonlinear equations using a modified Newton's algorithm or Powell's algorithm, or the optimization of an error function by using the Levenberg–Marquardt (LM) algorithm [25]. The LM algorithm is utilized in the current simulations because of its efficiency.

In our case, the linear circuit is represented by the general coupling matrix, defined by $ABCD$ network parameters, and the generator impedance $Z_g(f)$, as can be depicted in Fig. 1.

The harmonic balance error equation for each harmonic i is then

$$\begin{aligned} F_i(V) &= 0 \\ &= V_i - E_i \cdot H_i - I_i(V) \cdot G_i, \quad \text{for } i = 1, \dots, N_{\text{harm}} \end{aligned} \quad (12)$$

where

$$H_i = \frac{1}{A_i - Z_g(if) \cdot C_i} \quad (13)$$

$$G_i = \frac{Z_g(if) \cdot D_i + B_i}{Z_g(if) \cdot C_i - A_i} \quad (14)$$

E_i are the phasors of the excitations, and I_i and V_i are the harmonic components of the current and voltage at the diode terminals. In the case of frequency multipliers, E_i is comprised of the dc voltage component and a single sinusoidal signal. The diode is always matched at the fundamental frequency. Six to twelve harmonics are considered in these simulations, and the impedances at the higher harmonics are set to 0.001Ω for both the resistive and reactive components, if not otherwise specified.

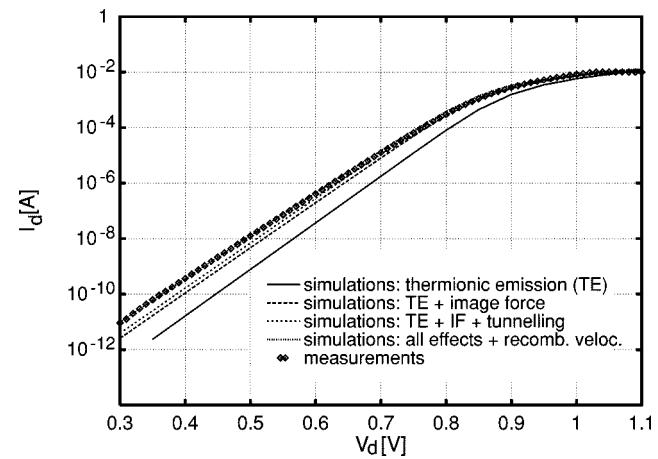


Fig. 2. Measured current voltage characteristic of a varactor Schottky diode compared to simulated values for the diode D1038 from TUD. The diode parameters are indicated in Table I.

All the parasitic elements of the diode are absorbed in the embedding network and included in the impedance seen by the junction at the different frequencies involved in the multiplier operation.

III. VALIDATION OF THE PHYSICAL MODEL

The physical model has been validated with measurements for a large number of diodes in the doping range of $N_{D,\text{epi}} = 3 \cdot 10^{16}/\text{cm}^3 \sim 3 \cdot 10^{17}/\text{cm}^3$, different epitaxial layer thicknesses and various diode diameters ranging from $1 \mu\text{m} \sim 20 \mu\text{m}$. The simulated current voltage characteristic for all diodes agree excellently with the respective measurements. An example is given in Fig. 2 for the diode D1038. The parameters of all the diodes analyzed in this paper are provided in Table I.

The contribution of the individual components to the total diode current is indicated in Fig. 2. The simulated capacitance voltage characteristic is also in excellent agreement with the measured values, as demonstrated in Fig. 3. The simulation is extended up to the breakdown voltage, where the junction capacitance is known to increase rapidly with reverse voltage [26].

The RF performance of the simulation tool has been discussed in [12]. We have performed simulations for two frequency multipliers published in the literature [4], [5]. In the simulations, we do not use any fitting parameters. In all simulations, a barrier height for the Pt Schottky contact of $\varphi_{b0} = 0.99 \text{ eV}$ is assumed.

The output power and efficiency versus the input power have been plotted in Fig. 4 for a frequency doubler ($2 \times 100 \text{ GHz}$)

TABLE I
SCHOTTKY DIODE PARAMETERS FOR
DEVICES FROM TUD AND UVa

Diode	Epitaxial Layer		$V_{bd,DC}$ (V)
	doping (cm^{-3})	length (μm)	
D734	10^{17}	0.350	-10
D1038	3×10^{17}	0.560	-8
UVa 6P4	3.5×10^{16}	1.0	-20 [4]
UVa 2T2	1.0×10^{17}	0.60	-11 [33]
for D734/D1038	substrate doping: $2 \times 10^{18} cm^{-3}$		
	length: 80-100 μm		

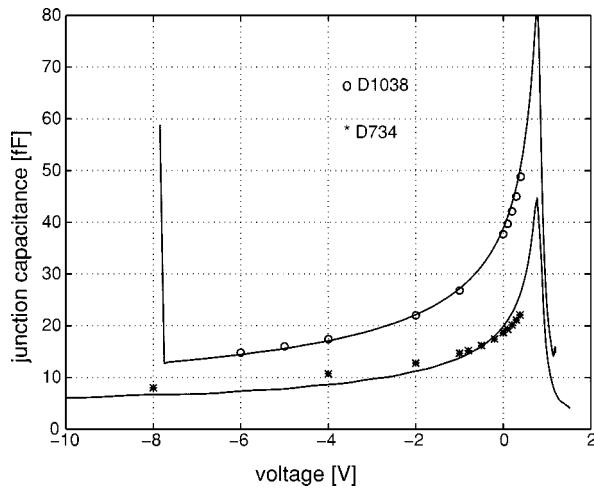
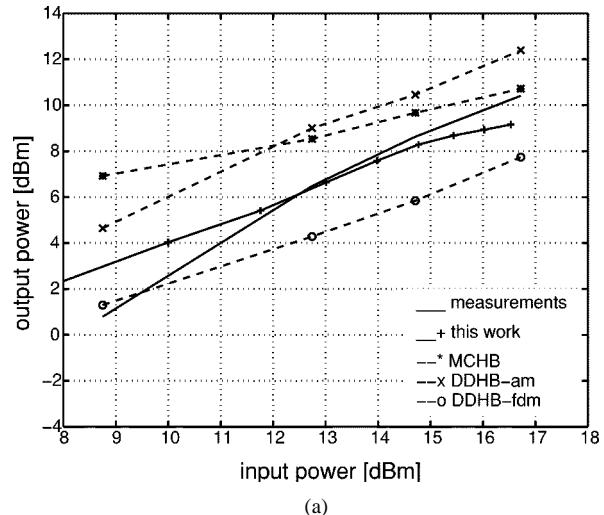


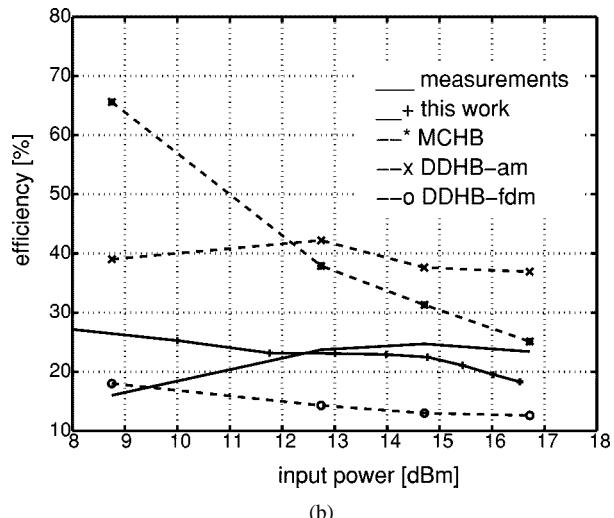
Fig. 3. Comparison between the measured (symbols) and calculated (solid lines) capacitance voltage characteristic for two diodes from the TUD D1038 and D734. The diode parameters are indicated in Table I.

utilizing a UVa 6P4 Schottky varactor. The results have been taken from [4] with additional simulations achieved with our model (solid line with “+” symbols). The techniques used in Fig. 4 are indicated as: 1) MCHB: self-consistent ensemble Monte Carlo harmonic balance simulator; 2) DDHB-fdm: drift-diffusion harmonic balance simulator with *field-dependent mobility*; and 3) DDHB-am: drift-diffusion harmonic balance with constant *average mobility*. All simulators overestimate the output power [see Fig. 4(a)] and the efficiency [see Fig. 4(b)] of the doubler at $P_{in} \leq 10$ dBm. Results from our model agree well above $P_{in} \geq 11$ dBm and reproduce the measured power slope. The bias voltage was $V_b = -10$ V, and the loads at harmonic frequencies were set to $Z_g(nf_0) = (0 + j0) \Omega$ for $n > 2$, while at the fundamental frequency, the diode was matched. The load impedance at the output $Z_g(2f_0)$ was optimized for maximum output power for each input power and obeys a value of $Z_g(2f_0) \approx (70 + j200)\Omega$ at an input power $P_{in} = 14$ dBm. The unrealistic simulated results at low input powers originate from the perfect match of the diode at each power level in contrast to the experimental setup, where the loads have been optimized for high-power levels.

This is emphasized in Fig. 4(b), which shows that the results from the Monte Carlo code predict efficiencies close to the theoretical limit at low input power levels, whereas the measured efficiency is low and increases with power level. In our simula-



(a)



(b)

Fig. 4. (a) Calculated and measured output power and (b) conversion efficiency as a function of the input power for a frequency doubler at $f_0 = 100$ GHz [4]. The solid line with symbols “+” denotes the results from our model, the solid line shows the experimental results from [4], and the dashed lines represent calculated results from [4].

tions, we have used the geometrical area and it is outlined below that our results would still improve when an effective diode area would have been employed.

We have also compared our simulations with the measured data for a frequency multiplier using a similar diode at $f_0 = 80$ GHz [5], illustrated in Fig. 5. At the output, the balanced diode configuration has been simulated as a direct parallel connection of two identical diodes. The agreement with measured data is very good. Simulations of the same arrangement at $f_0 = 160$ GHz also agree well at high-input power levels. Although the simulations presented in Figs. 4 and 5 have been performed at different frequencies and with different circuit structures, we achieve very good agreement at large power levels, which demonstrates the capabilities of the simulation tool.

IV. ANALYSIS OF VARACTOR-BASED MULTIPLIER CIRCUITS

The results from a successful circuit analysis of frequency multipliers should predict the following parameters determining

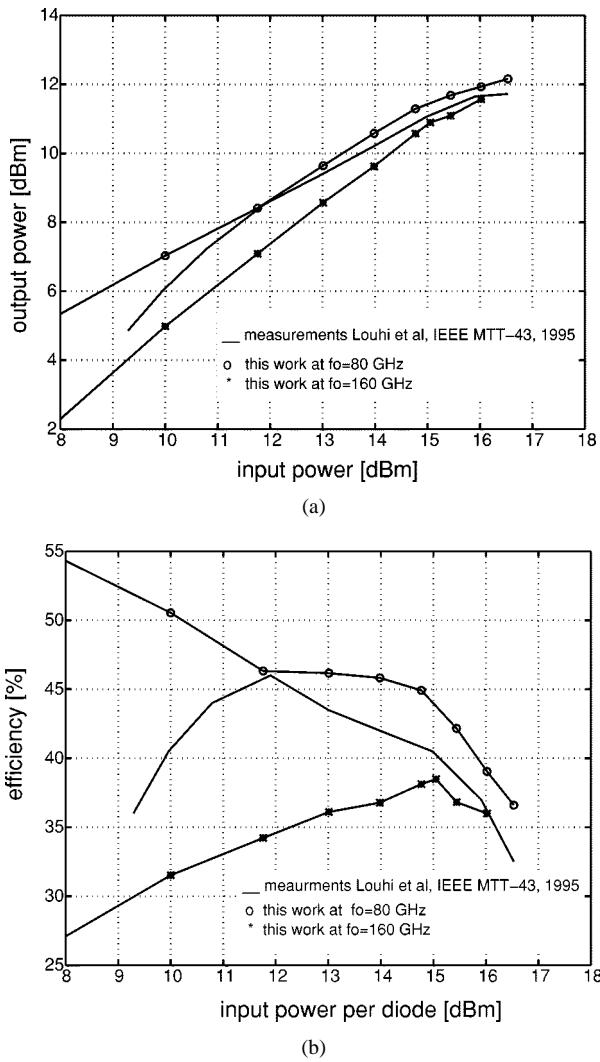


Fig. 5. (a) Calculated and measured output power and (b) conversion efficiency as a function of the input power for a frequency doubler at $f_0 = 80$ GHz [5]. The symbols “o” “*” denote the results from our model at $f_0 = 80$ GHz and $f_0 = 160$ GHz, respectively, and the solid line shows the experimental results from [5].

the multiplier performance for a given diode structure: output power P_{out} , conversion efficiency η , embedding impedances at the fundamental, output, and idler frequencies at the diode terminals, bias voltage V_{bias} , and load impedances at the remaining harmonics. All conventional multiplier design methods are based on an equivalent circuit of the Schottky diode presented in Fig. 6(a) [1], [2], [27]. However, this simple model cannot explain the decrease in conversion efficiency beyond a certain input power level, which has been frequently observed in experimental results. Improved intrinsic diode models have to be utilized in this case, as shown in Fig. 6(b) and (c), which describe the physical behavior of the device with increasing accuracy. As has been pointed out by Grajal *et al.* [12], at low-input powers equivalent-circuit models, including electron velocity saturation phenomena [see Fig. 6(b)] are sufficient to accurately predict the multiplier performance. However, at high-power levels and near the maximum of the conversion efficiency, only accurate physical models [see

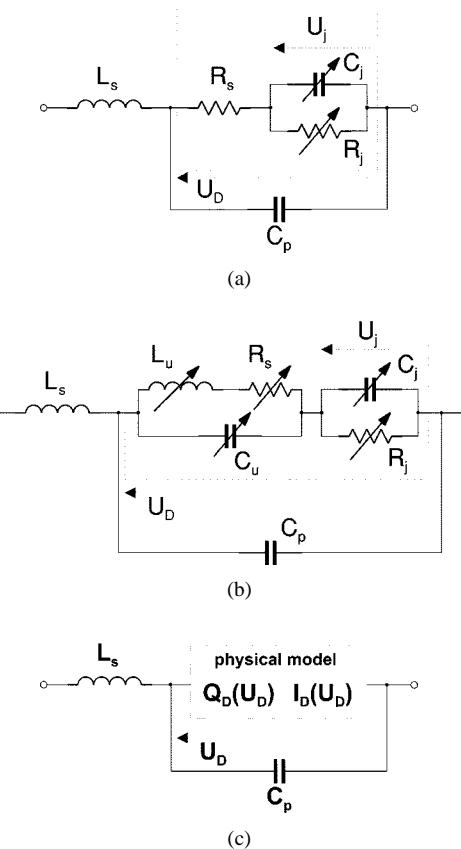


Fig. 6. Equivalent circuits for different Schottky diode varactor models. (a) Constant series resistance model. (b) Variable series resistance model. (c) Proposed physical model including all effects.

Fig. 6(c)] provide reasonable prediction of the multiplier performance.

In Fig. 6(a) and (b), the Schottky junction is modeled by a parallel connection of a voltage-dependent nonlinear capacitance and resistance. The series resistance due to the undepleted region in the semiconductor becomes a nonlinear function of the diode current density at increased current densities [see Fig. 6(b)]. The nonlinear current dependent series resistance has been considered responsible for the decrease in the conversion efficiency at high-power levels [1], [5], [27]. It has been argued that the displacement current becomes comparable to the maximum current in the material at high operating frequencies. An empirical current-dependent series resistance has been introduced in order to fit the measured results, according to Fig. 6(b). It has to be emphasized that the above analysis did not include breakdown effects and its impact on the RF operation of the frequency multiplier. Furthermore, the series resistance increases when the current density in the diode approaches the maximum current density

$$J_{\max} = qN_D v_{\max} > J_{\text{disp}} = \frac{\partial Q}{\partial t} = \frac{\partial(qN_D w)}{\partial t} \quad (15)$$

with J_{disp} being the displacement current. Dividing both sides by the available number of electrons yields the maximum velocity with which the edge of the depletion region can move

$$v_{\max} > \frac{\partial w}{\partial t} \quad (16)$$

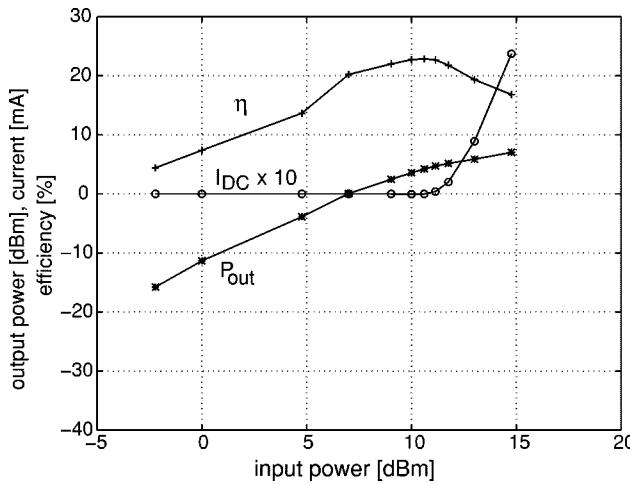


Fig. 7. Efficiency, output power, and dc current at $V_{bias} = -3$ V for the D734 varactor Schottky diode.

where w is the width of the depletion region. Hence, (16) is equivalent to the argument that the displacement current density must be less than the maximum current density in the semiconductor in the undepleted region $J_{disp} < J_{max}$. It cannot be equal to the maximum current density because this would assume a zero conduction current in the depletion region.

The equivalent-circuit models require a separation of physical effects into individual equivalent-circuit elements, an extraction of the equivalent-circuit element values from measurements distinct from the operating conditions, and an identification of equivalent-circuit elements with combined effects at high powers and high frequencies, which is very difficult to achieve.

Therefore, a physical model is proposed, which is based on results from the previous section. Such an approach enables us to concurrently optimize the device electrical and geometrical parameters together with attainable output power, conversion efficiency, and the required loads at the specific harmonics.

Although we agree that the current saturation mechanism becomes important at very high frequencies, typically above 300-GHz fundamental frequency, but it has only a marginal effect on efficiency decrease at frequencies below 200 GHz, which were considered in [1]. The diode 6P4 shows velocity saturation effects only because of its very low doping concentration in the epitaxial layer. We suggest that the limitation in varactor operation is due to the initiation of varistor operation with a concurrent onset of dc current flow at either end of the current–voltage characteristic. For example, we have used the Schottky varactor diode D734 from TUD, similar to the diode 2T2 from UVa for simulations of frequency doublers and triplers with our simulation tool. It can be inferred from Figs. 7 and 8 that the maximum conversion efficiency coincides with the onset of the dc current through the diode. In Fig. 7, the dc current is positive due to forward conduction, as can be depicted from the time-domain waveforms given in Fig. 9. In contrast to this, the dc current component in Fig. 8 is negative, originating from impact ionization when the total voltage exceed the breakdown voltage in the device, as indicated in Fig. 10. Independently of dc current polarity, the maximum of the

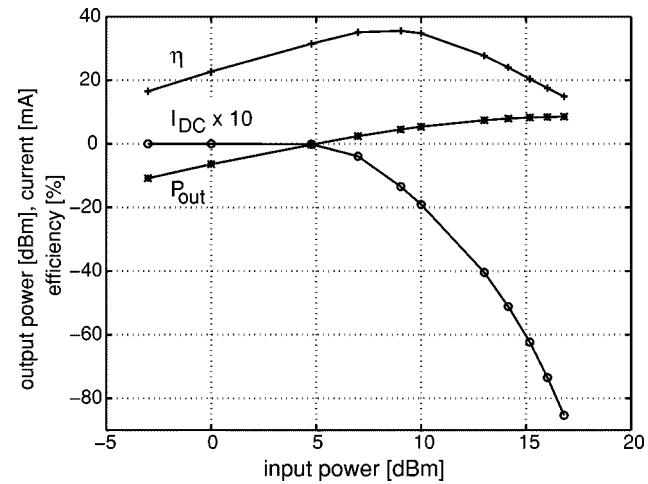


Fig. 8. Efficiency, output power, and dc current at $V_{bias} = -7$ V for the D734 varactor Schottky diode.

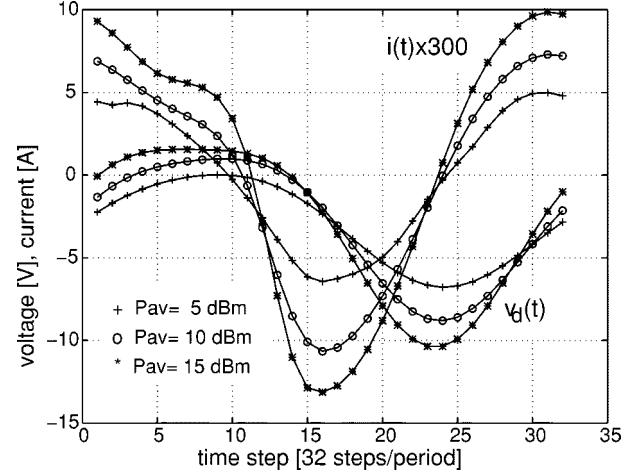


Fig. 9. $v_D(t)$ and $i_D(t)$ versus time for $V_{bias} = -3$ V for the D734 varactor Schottky diode. Operating frequency is $f_0 = 50$ GHz. The time scale is 32 points per period.

conversion efficiency coincides with the onset of current flow, whereas the output power further increases with increasing input power. The increase in output power is due to the mixed varactor/varistor operation and the decrease in the efficiency at high-power levels originates from the conversion of the RF signal into dc power. The dc power is then delivered to the circuit or dissipated in the device, respectively. It is important to observe that the input power level for maximum efficiency does not coincide with the power level for maximum output power. Fig. 11 shows that, at low input power levels, the efficiencies for the bias voltage $V_{bias} = -5$ V and $V_{bias} = -7$ V are nearly equal. The reason is that the capacitance is nearly constant for voltages lower than -7 V. Hence, no effective capacitance modulation takes place for the negative semicycles. The slight increase in the capacitance for $V_{bias} = -5$ V has an effect on the tripler performance, but the doubler circuit is insensitive to this small variation. Hence, the results for the efficiency of the doubler circuit are very similar for these two bias conditions. Similar results have been obtained for the tripler circuit, as indicated in Fig. 12.

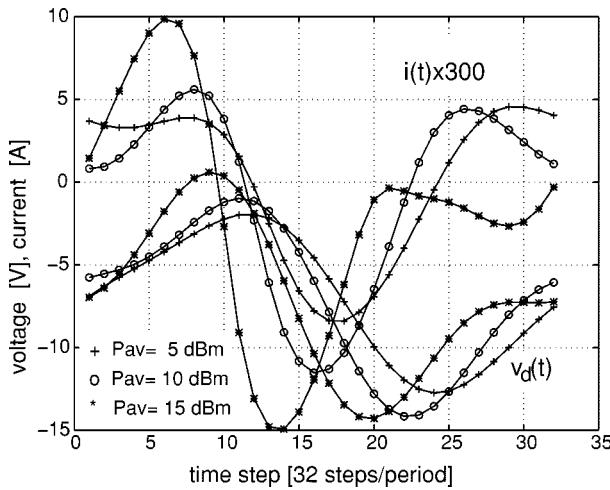


Fig. 10. $v_D(t)$ and $i_D(t)$ versus time for $V_{bias} = -7$ V for the D734 varactor Schottky diode. Operating frequency is $f_0 = 50$ GHz. The time scale is 32 points per period.

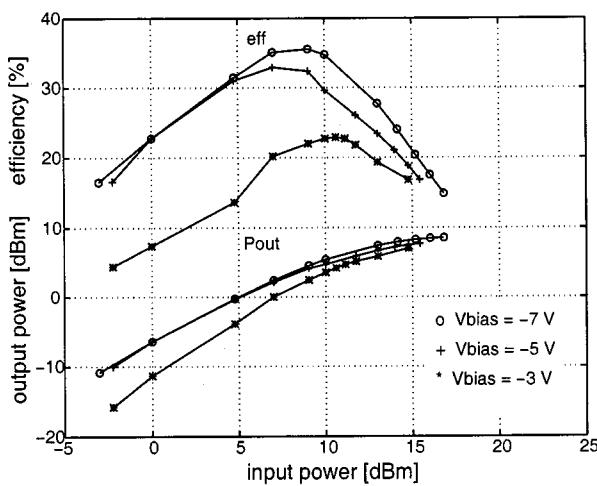


Fig. 11. Frequency-doubler conversion efficiencies and output powers with D734 diode for three different bias conditions $V_{bias} = -3$ V, $V_{bias} = -5$ V, $V_{bias} = -7$ V. Operating frequency is $f_0 = 50$ GHz.

V. MECHANISMS AND PARAMETERS LIMITING MULTIPLIER PERFORMANCE

There exist three major mechanisms responsible for the limitation of the output power and conversion efficiency: forward conduction, reverse breakdown, velocity saturation. These mechanisms have a direct impact on the multiplier circuit performance such as the bias point, the maximum voltage swing, embedding impedances, and the load impedances at the higher harmonics. The forward conduction mechanism is independent of frequency and restricts the positive voltage swing of the sinusoidal signal at the device terminals. The reverse breakdown mechanism is frequency dependent and limits the signal excursion in the reverse direction. It can also lead to current saturation in a well-designed diode by the increased current flow due to impact ionization.

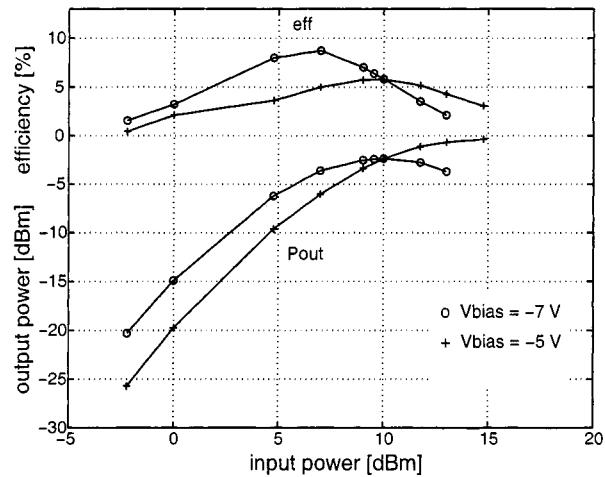


Fig. 12. Frequency-tripler conversion efficiencies and output powers with D734 diode for two different bias conditions $V_{bias} = -5$ V and $V_{bias} = -7$ V. Operating frequency is $f_0 = 50$ GHz.

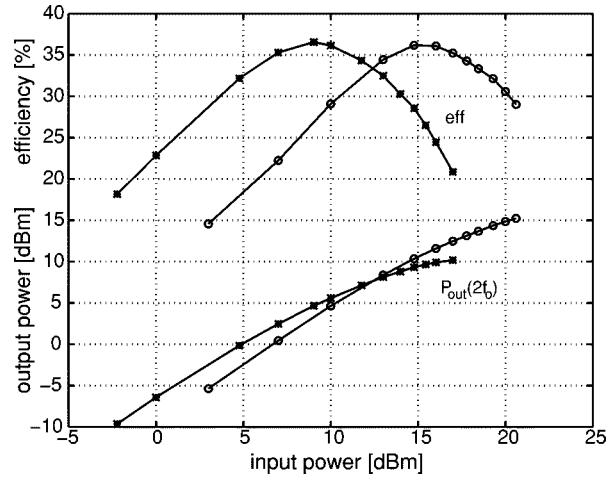


Fig. 13. Calculated output power and conversion efficiency as a function of the input power for two TUD D734 Schottky varactors. The bias voltage is $V_{bias} = -5$ V and optimum loads are chosen at the second and third harmonic. The fundamental frequency is $f_0 = 50$ GHz. The symbols “*” are for a diode diameter of $6.7 \mu\text{m}$ and the symbols “o” stand for results with a diode diameter of $13.4 \mu\text{m}$.

A. Impact of the Bias Point and the Series Resistance on Multiplier Performance

It should be observed in Fig. 11 that the output power levels for all bias conditions ultimately converge to similar values, however, with high dc currents. Operating the diodes at high dc currents is not desirable due to reliability and burnout problems associated with high-current high-voltage operation. Therefore, the bias point for maximum conversion efficiency for a particular diode is the point with maximum RF amplitude excursion without dc current generation, as $V_{bias;opt} = (V_D - V_{bd;RF})/2$, where V_D is the diffusion voltage and $V_{bd;RF} \approx -14$ V is the RF breakdown voltage for D734. The maximum conversion efficiency can also be shifted with regards to the input power by utilizing Schottky diodes with different areas. Fig. 13 illustrates calculated results for two Schottky varactor diodes D734 with different anode diameters. The maximum conversion efficiency is shifted toward lower values of the input power when

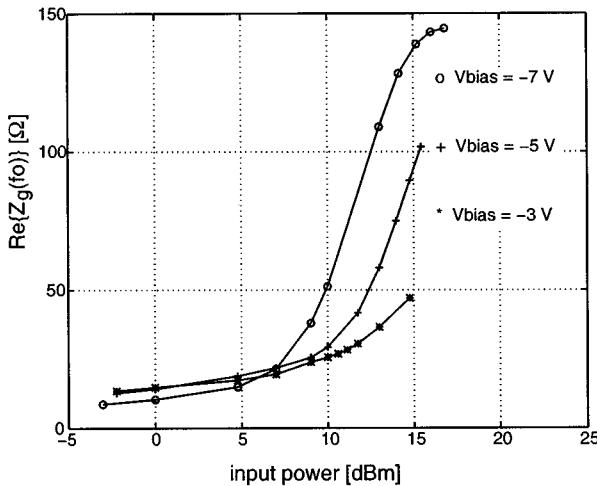


Fig. 14. Variation of the real part of the diode impedance calculated from the physical model as a function of the input power at bias voltages $V_{\text{bias}} = -3 \text{ V}$, -5 V , -7 V for the diode from Fig. 7.

the diode area is decreased. The demand for maximum conversion efficiency at a prescribed input or output power uniquely determines the diode area. The optimum value is a function of the doping concentration, frequency, and desired output power. Highest output powers are achieved with large anode diameters because the output power and displacement current both scale with the area. Whenever sufficient power is available to pump the diode up to maximum conversion efficiency and an appropriate matching is realizable, a large-area diode will provide improved output power performance.

As demonstrated in [1] from DD physical calculations, the real part of the diode impedance rises strongly with input power level. We can reproduce this increase, which is illustrated in Fig. 14 for the diode used in Figs. 7–10. Note that, in the case of reverse breakdown, the real part of the diode impedance increases dramatically by a factor of more than 12. Such large changes in the series resistance cannot be solely attributed to lowering of the mobility. One possible reason is that, at reverse breakdown, the total diode resistance never reaches the zero-bias series resistance values due to the high fields in the space-charge region. The interpretation of the numerical results in Fig. 14 in terms of equivalent-circuit elements is not simple and the identification of the individual mechanisms with particular equivalent-circuit elements is almost impossible in the case of breakdown. In this case, the physical model should be used for the accurate characterization of the diode.

B. Impact of Breakdown Effect on Different Operating Conditions

As pointed out above, the generation of charges due to impact ionization plays a vital role in multiplier performance. The model for the generation of carriers due to avalanche multiplication is based on the following:

$$G = \frac{1}{q} (\alpha_n |\bar{J}_n| + \alpha_p |\bar{J}_p|) \quad (17)$$

$$\alpha_{n,p} = A_{n,p} \exp \left[- \left(\frac{E_{\text{crit}}}{|E_{n,p}|} \right)^{\beta_{n,p}} \right] \quad (18)$$

where α_n and α_p stand for the ionization coefficients for electrons and holes, J_n and J_p are the electron and hole current densities, $\beta_{n,p}$ and $A_{n,p}$ indicate empirical parameters for the calculation of the ionization coefficients, $E_{n,p}$ is the electric field in the space-charge region, and E_{crit} denotes the critical field for charge generation, respectively. Some authors have pointed out that the RF breakdown voltage is frequency dependent and can be significantly different from the dc breakdown voltage [30], [31]. This has also been observed in our simulations. One possible explanation for the frequency dependence is that, at high frequencies, the conditions for avalanche are achieved for only a short period of time and, therefore, the carriers in the material may not gain sufficient energy to ionize other carriers. Additionally, the carrier density does not follow the field change in unison because the carrier generation G also depends on the number of carriers already present, which is described through (2). This happens although the impact ionization rates $\alpha_{n,p}$ in (17) follow the field change nearly instantaneously.

C. Velocity Saturation Mechanism at High Frequencies

High-frequency operation of frequency multipliers is limited by the velocity saturation effect. It has been outlined in [32] that the current saturation mechanism should not occur for well-designed diodes at all operating frequencies. This can be achieved by choosing a sufficiently high doping density in the device $N_D \geq J_{\text{disp}}/qv_{\max}$. The limited carrier velocity in materials such as GaAs determines the upper bound for the rate of change of the space-charge width. Ultimately, the signal frequency becomes larger than the maximum electron velocity (for electrons in GaAs $v_{\max} \approx 2.8 \cdot 10^7 \text{ cm/s}$) and the space-charge cannot be modulated. This is the case for the 6P4 diode at frequencies around 100 GHz because of the low doping concentration. At such high frequencies, other frequency-multiplying mechanisms or different materials like InAs or InSb must be considered. It is shown in Fig. 15 that the edge of the depletion region can follow the voltage waveform at 100 GHz, but cannot follow the voltage waveform at 700 GHz. In Fig. 15, the Schottky diode contact is located on the right-hand side of the diagram. It can be seen that the value for maximum depletion width $w_{\max} \approx 80.55 \mu\text{m}$ remains nearly constant for the three frequencies, whereas the difference between the minimum and maximum value of the depletion width Δw decreases strongly with increasing frequencies. The decreased Δw leads to a smaller modulation of the space-charge region during one period of the exciting signal, which, in turn, leads to a smaller capacitance modulation. This asymmetry is probably due to the finite time required to empty the space-charge region, while the space-charge region can be rapidly filled with mobile charges. The transition between the space-charge region and the undepleted region is abrupt at 100 GHz and slopes with increasing frequencies.

The design procedure at high frequencies differs from that at low frequencies because the breakdown voltage is no longer the limiting factor. Hence, maximum output power and conversion efficiency is achieved when the current density is smaller than the saturation current [see (15)]. This determines the optimum doping. The epi-layer thickness is then chosen for minimum

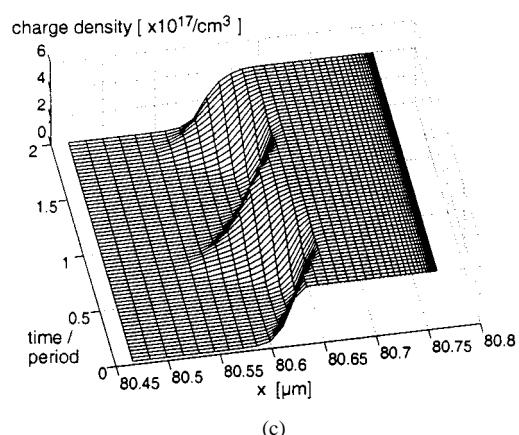
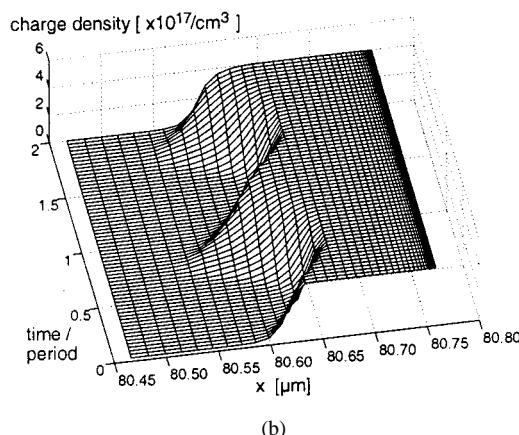
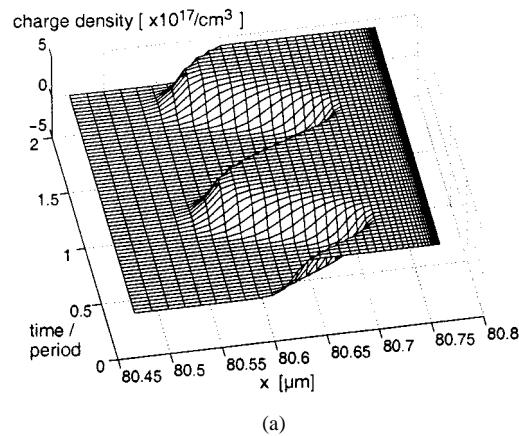


Fig. 15. Variation of the edge of the depletion region with applied RF voltage at (a) signal frequency of 100 GHz, (b) signal frequency of 500 GHz, and (c) signal frequency of 700 GHz. The epi-layer doping is $N_{\text{epi}} = 4 \cdot 10^{17}/\text{cm}^3$, the epi-layer thickness is $t_{\text{epi}} = 560 \text{ nm}$, diode diameter is $5 \mu\text{m}$.

series resistance. The circuit is operated at larger capacitance values (lower reverse bias).

VI. SYNTHESIS OF OPTIMUM FREQUENCY MULTIPLIERS

It has been demonstrated in [12] that the multiplier circuit is more sensitive to changes in the embedding impedances at low-input power levels as compared to high-input power levels. This is independent of the diode considered in the simulations.

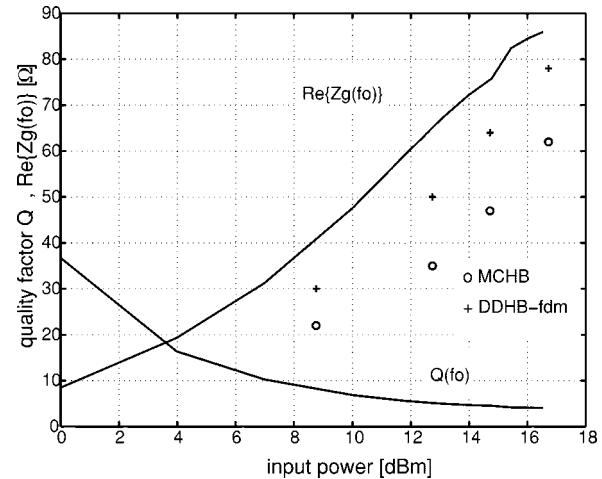


Fig. 16. Quality factor Q and the real part of the diode impedance $\Re\{Z_g(f_0)\}$ as a function of input power for the diode 6P4. The operating conditions are the same as in Fig. 4.

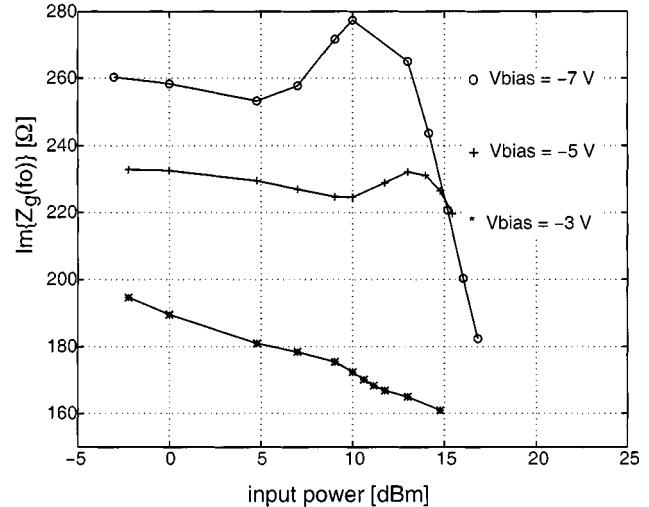


Fig. 17. Imaginary part of the diode embedding impedance $\Im\{Z_g(f_0)\}$ as a function of input power for the diode D734 for three different bias points.

The sensitivity can be defined in terms of a quality factor at the respective frequency

$$Q(f_0) = \frac{\Im\{Z_g(f_0)\}}{\Re\{Z_g(f_0)\}}. \quad (19)$$

The real part of the diode impedance vary with input power and frequency, whereas the imaginary part varies essentially only as a function of frequency. When the quality factor Q is large, the circuit is more sensitive to changes in frequency.

The quality factor Q and the real part of the diode input impedance versus input power are illustrated in Fig. 16 for the 6P4 diode. The imaginary part has been omitted because it changes by less than 10% for all power levels. It can be seen that $Q(f_0) \approx 35, \dots, 13$ at low-power levels below $P_{\text{in}} < 6 \text{ dBm}$. For high-input power levels, the variation of the load is weak ($Q \approx 4$) and all simulations show a strong increase of $\Re\{Z_g(f_0)\}$ in accordance with [1], [5].

TABLE II

MAXIMUM CONVERSION EFFICIENCY OF A FREQUENCY DOUBLER AND TRIPLEX FOR $P_{av} = 7$ dBm AT THREE BIAS POINTS. THE DIODE USED IN THE ANALYSIS IS D734. THE FUNDAMENTAL FREQUENCY IS 50 GHz. FOR THE DOUBLER, THE LOAD IMPEDANCE AT THE THIRD HARMONIC IS $Z_g(3f_0) = 0 + j0$. FOR THE TRIPLEX, THE LOAD IMPEDANCES AT THE SECOND AND FOURTH HARMONIC ARE $Z_g(2f_0) = (0 + j0)\Omega$, $Z_g(4f_0) = (0 + j0)\Omega$

multiplier	V_{bias} (V)	η (%)	$Z_g(2f_0)$ Ω	$Z_g(f_0)$ Ω
doubler	-3	22.5	$25 + j100$	$26.9 + j185.3$
	-5	31.2	$25 + j125$	$22.0 + j226.8$
	-7	37.2	$25 + j150$	$23.0 + j275.5$
triplex			$Z_g(3f_0)$ Ω	$Z_g(f_0)$ Ω
	-3	2.8	$19 + j70$	$20.1 + j173.6$
	-5	5.0	$17 + j80$	$16.3 + j213.5$
	-7	8.7	$12 + j90$	$17.2 + j258.2$

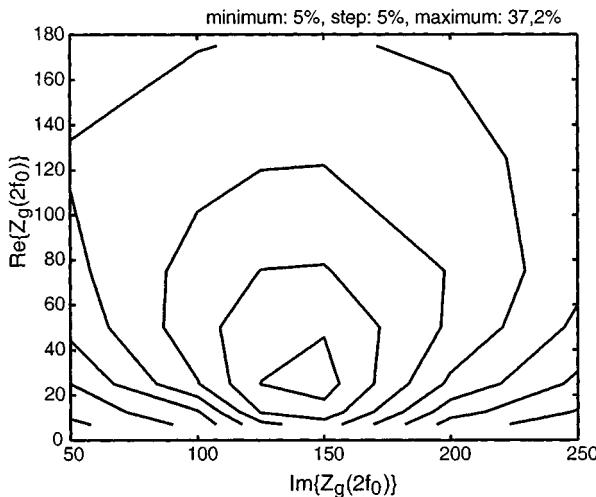


Fig. 18. Sensitivity of the efficiency to $Z_g(2f_0)$ for $V_{bias} = -7$ V and $P_{av} = 7$ dBm.

The imaginary part of the embedding impedance for the diode D734 is shown in Fig. 17. It can be inferred from Fig. 17 that the imaginary part changes little with increasing input power, up to a value where a substantial breakdown current is generated in the diode, which increases the junction capacitance in accordance with Fig. 3. Table II summarizes the results obtained for the analysis of a frequency doubler and frequency triplex, respectively, using the diode D734 at a fundamental frequency of $f_0 = 50$ GHz. It can be inferred from the tables that the optimum impedance for the frequency triplex is slightly lower as compared to the frequency doubler.

Once the optimum conditions for a multiplier have been determined, the tuning capabilities of the multiplier circuit are investigated for the extraction of realizable tuning elements. Fig. 18 shows the conversion efficiency as a function of the circuit impedance at the second harmonic $Z_g(2f_0)$ for an input power level of 7 dBm, which coincides with the maximum of the conversion efficiency at a bias voltage of $V_{bias} = -7$ V. It can be deduced from Fig. 18 that for $Z_g(2f_0)$ different from the optimum load $Z_{g-opt}(2f_0)$, the efficiency and output power drop rapidly to very low values. Furthermore, it can be seen that

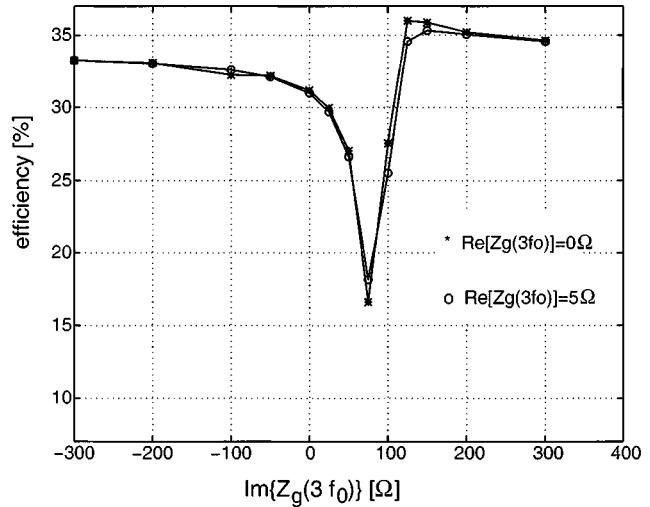


Fig. 19. Sensitivity of the efficiency of the frequency doubler to $Z_g(3f_0)$ for $V_{bias} = -5$ V and $P_{av} = 7$ dBm.

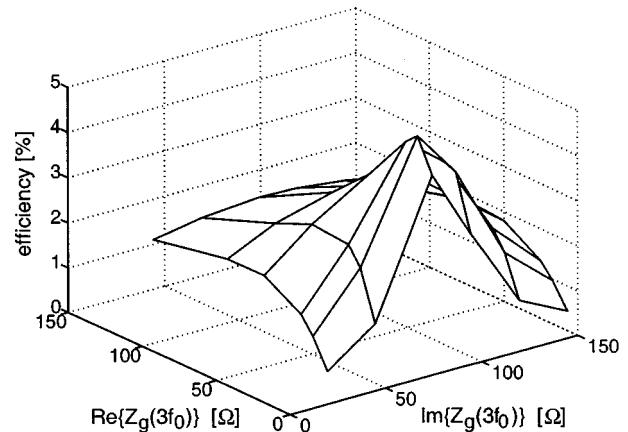


Fig. 20. Sensitivity of the conversion efficiency of a frequency tripler to $Z_g(3f_0)$ for $V_{bias} = -5$ V and $P_{av} = 7$ dBm.

decreasing the optimum value for $\Re\{Z_g(2f_0)\}$ has a stronger effect than increasing it.

Exploiting the resonance between a pure reactance and the effective device capacitance at the third harmonic, the efficiency can be further increased by $\approx 5\%$ according to Fig. 19 ($V_{bias} = -5$ V, $Z_g(2f_0) = (25 + j125)$ Ω , and $P_{av} = 7$ dBm). This efficiency improvement is sustained even for slightly lossy realizations of the circuit.

Fig. 20 shows the conversion efficiency for the frequency triplex as a function of the load at the third harmonic $Z_g(3f_0)$. The loads at the second and fourth harmonic are chosen short circuits in this figure and the bias voltage is $V_{bias} = -5$ V. Similarly to the results obtained for the frequency doubler, the optimum operation is sensitive to variation of the embedding impedance for an impedance different from the optimum load impedance $Z_{g-opt}(3f_0)$. The selection of the impedance of the idler is crucial in frequency triplexes. This point is exemplified in Fig. 21. The simulations have been performed with $V_{bias} = -5$ V and $Z_g(3f_0) = Z_{g-opt}(3f_0)$. The results obtained from this analysis ($\eta_{opt} \approx 15\%$) suggest that the load at the second and fourth harmonic can be treated

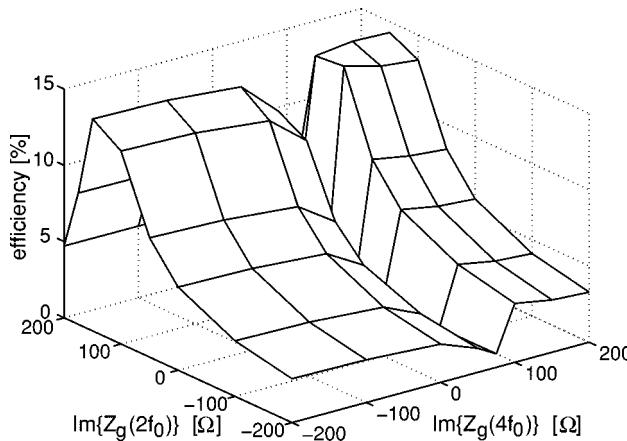


Fig. 21. Sensitivity of the conversion efficiency of a frequency tripler to the idler circuit $Z_g(2f_0)$ and to the load at the higher harmonic $Z_g(4f_0)$ for $V_{bias} = -5$ V and $P_{av} = 7$ dBm.

independently and the impedance value at the idler frequency is more important than the load at the fourth harmonic. The resonance for the idler frequency requires inductive loads and, in the vicinity of the maximum efficiency, the sensitivity of the efficiency to variation in the impedance values is higher for increasing values of $\Im\{Z_g(2f_0)\}$.

In frequency doublers and triplers, the optimum load at the third and fourth harmonic, respectively, does not depend on the power level. A load different from short circuit at even higher harmonics has only a marginal effect on the multiplier performance.

VII. CONCLUSIONS

The degree of freedom that arises as a consequence of the coupling of a numerical model for Schottky diodes and a harmonic balance circuit simulator has enabled us to study the different operation regimes and the physical limitations of the frequency multiplier performances. It has also demonstrated its usefulness to design multipliers from the circuit point-of-view: bias, input power, and loads at different harmonics.

We have obtained good agreement between published experimental results and our calculations for device and multiplier characteristics operating at frequencies up to 320 GHz with our enhanced DD model coupled to a harmonic balance simulator.

We have demonstrated that, at low input power levels, the operation of the multiplier is mainly determined by the embedding circuit and the choice for the dc operating point of the diode. The discrepancies observed in many simulation between the measured and calculated results can be explained by mismatching effects and do not originate from device physics. In contrast, at high-power levels, the embedding circuit exhibits only minor contribution to the overall performance of the multiplier and impact ionization in the device is responsible for output power saturation and conversion efficiency decrease at high output powers.

It has been demonstrated that the onset of the dc current is responsible for the decrease of the conversion efficiency at high-power levels. The impact of the breakdown effects, the velocity saturation, and the forward conduction on frequency multiplier

performance has been discussed in detail. Simulated results suggest that the output power approaches similar values at high input power independent of the choice of the bias point. At these power levels, the embedding circuit is determined by the increase of the real part of the input impedance. It was also found that an appropriate load at the high harmonics could improve the efficiency independently from the power level.

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Computer-Aided Design of Step Recovery Diode Frequency Multipliers

Jian Zhang and Antti V. Räisänen, *Fellow, IEEE*

Abstract—Through the study of the step recovery diode (SRD) models, a method for improving the efficiency of CAD of SRD frequency multipliers is proposed. By reducing the nonlinearity of the SRD model to an appropriate extent, the simulation and optimization of SRD frequency multipliers can be carried out more easily and faster. Systematic design and optimization of an SRD frequency multiplier is described. Simulation results of this SRD frequency multiplier are compared with experimental results.

I. INTRODUCTION

ONE OF THE most outstanding characteristics of the step recovery diode (SRD) is the high conversion efficiency with high frequency multiplication order. It provides a method for generating power at high frequencies by using a low cost oscillator. SRD frequency multipliers are typically used in hybrid local oscillators, especially where low phase noise is required: in terrestrial communications, satellite communications, TVRO, mobile communications. Input frequencies could extend down to 10 MHz and output frequencies up to 94 GHz [1], [2].

Another typical application of the SRD is as a comb generator in microwave and millimeterwave samplers, which are used in frequency counters, sampling scopes, phase locked synthesizers, and network analyzers [3]–[5].

In the past, designs of SRD frequency multipliers were mainly based on the method of Hamilton and Hall [6]. In this approach, the SRD was modeled as an ideal conductor for the conducting state and a capacitor for the nonconducting state. By this assumption, the SRD frequency multiplier could be simplified to two separate circuits called the input circuit and the output circuit. The advantage of this approach is the simplicity of the analysis.

However, in real circuits the SRD does not act like a simple switch between the conducting state and the nonconducting state. The transition from the conducting state to the nonconducting state has a finite transition time [7]. Furthermore, the input and output circuits affect each other in a complicated way. Therefore, a circuit designed by this method must be adjusted experimentally. Good performance could still be achieved by cut and try. And if the circuit were built in waveguide, we would have more flexibility for adjusting it.

With the increasing demand of integrated circuits, more accurate designs are required to develop the circuits in a medium where adjustment is not possible. Of course, there are other reasons which influence the medium of the circuit;

microstrip circuits have small size, low weight, high reliability, while waveguide has low loss and high power handling capability. In parallel, the development of computer technology and computer-aided design tools provides us with the possibility of the simulation and optimization of the circuits to achieve an accurate design and optimum performance.

Moreover, the idealized model used in the method of Hamilton and Hall cannot be used directly in commercial circuit simulators, since the circuit-solving algorithms used by simulators are based on algorithms like the Newton-Raphson algorithm. The constitutive relationships of the device must be differentiable with respect to voltage and current, and these derivatives must also be continuous with respect to voltage and current.

To realize the CAD of SRD circuits, we developed a new SRD model which is more accurate by considering the voltage ramp during the transition process, and which can be directly used in commercial circuit simulators [8].

However, SRD frequency multipliers cannot be analyzed as readily as varactor or resistive diode multipliers [9]. Harmonic-balance analysis of the SRD frequency multiplier can be troublesome because of the strong nonlinearity of the diode, the large number of harmonics involved, and the possible instability make convergence precarious. In addition to choosing an advanced simulator for good convergence, other efforts should be made to find the correct solution efficiently for this type of circuit.

In order to improve the efficiency of CAD of SRD frequency multipliers, we have investigated the modeling of the diode and characteristics of SRD frequency multipliers. The results show that reducing the nonlinearity of the model of the diode to some extent while optimizing the circuit does not change the characteristics of the circuit radically. On the other hand, the efficiency of the CAD of this kind of circuit is greatly improved and the analysis itself is more easily and faster accomplished.

In this paper, we shall first discuss the modeling of the SRD. Then, the method of reducing the nonlinearity of the model is proposed and the simulation results with different degrees of nonlinearity of the model are compared. A systematic design of an SRD frequency multiplier is given as an example. Finally, the simulation results of this SRD frequency multiplier are compared with experimental results.

II. NONLINEARITY OF SRD

The SRD, which is also called the snap-off diode or charge storage diode, was first recognized in the early 1950's. The diode was modeled in a way that it behaves as a two-state

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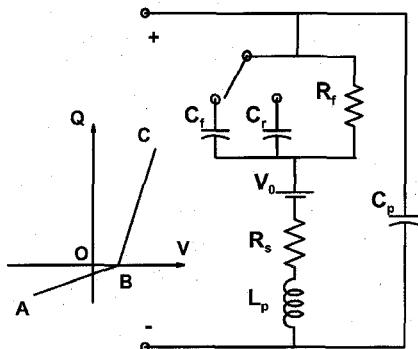


Fig. 1. Conventional model of SRD.

capacitor of large capacitance (forward bias capacitance C_f) under forward charge storage state and small capacitance (reverse bias capacitance C_r) under reverse bias, with zero switching time between states, as shown in Fig. 1. Analyses of resonant and nonresonant circuit performance using this model describe the first-order diode behavior very well [6], [7].

Nevertheless, the forward state capacitance, which is a diffusion capacitance determined by a large number of free carriers in a finite volume, can not physically be infinite. The transition time, in which an SRD switches between forward and reverse states, cannot be zero, either.

The transition process was studied and modeled by Moll and Hamilton [7]. Based on it, a new model was established by Zhang and Räisänen [8]. During the transition process, the voltage (V) across the diode and the stored charge (Q) in the intrinsic or lightly doped layer can be described approximately by

$$V = \frac{I_R}{\varepsilon v A} \left[\frac{W^2}{4} - W \sqrt{Q} \sqrt{\frac{2D}{I_R}} \right] \quad (1)$$

where v , A , and D are the average velocity of carriers in the space charge limit range, the working area of the diode and the ambipolar diffusion constant, respectively. I_R is the reverse current when the diode is reverse biased. W is the width of the field free intrinsic center region.

Examining (1) we can see that this transition process can be described by a parabolic function, which can be determined by the two state capacitance corresponding to the conducting state (C_f) and nonconducting state (C_r) of the diode, respectively.

Using the continuity conditions at the points where the transition starts and ends, we obtain the equation describing this transition process

$$Q = \begin{cases} \frac{C_r V}{2\phi} \left(V + \frac{C_r \phi}{C_f - C_r} \right)^2 - \frac{C_r^2}{2(C_f - C_r)} \cdot \phi & 0 < V < \phi, \\ C_f V - \frac{C_f - C_r}{2} \cdot \phi & V \geq \phi \end{cases} \quad (2)$$

where ϕ is the contact potential at which the transition starts.

The characteristic of the diode, illustrated in Fig. 2, shows that the nonlinearity of the diode model is closely related to the forward bias capacitance C_f . While modeling the diode, we can extract this parameter through a DC measurement on the SRD. When the SRD is forward biased, the p - n junction acts like a dynamic or nonlinear resistor (R_f). The relationship of

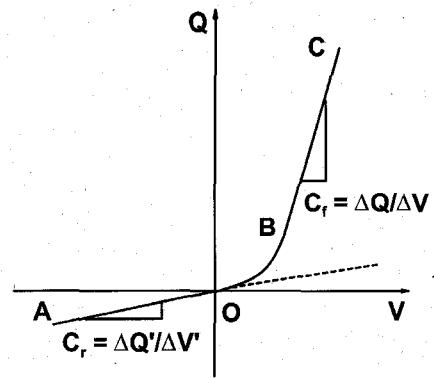
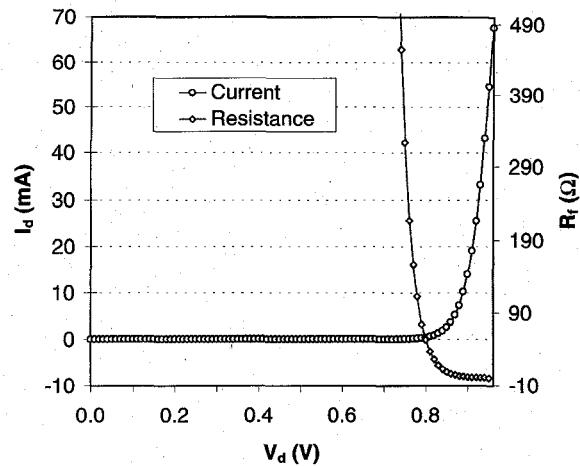


Fig. 2. Modified model of SRD.

Fig. 3. I - V curve of SRD (HP-5082-0835).

C_f , R_f and the minority carrier lifetime τ can be related as given by Kotzebue [10],

$$\tau = R_f C_f \quad (3)$$

where τ is usually given by the manufacturer, and R_f can be obtained from the I - V characteristic of the SRD.

We have measured an SRD (HP-5082-0835) made by Hewlett-Packard, and its I - V curve is shown in Fig. 3. It can be seen that the forward bias resistance turns into a very small and nearly constant resistance right after the diode is forward biased. In this case, the value of the forward resistance is of the order of 0.1 ohm, which corresponds to a forward bias capacitance C_f of 100 nF. The minority carrier lifetime τ of 10 ns is given by the manufacturer.

However, the depletion capacitance of this diode, which is used as the reversed bias capacitance C_r in our model, is given as about 0.3 pF. Comparing with the calculated C_f above shows the very strong nonlinearity of the diode model. Directly using this model in circuit simulators would definitely cost a lot computational resources and most probably cause convergence problems.

In the simulation of circuits, good initial conditions are sometimes critical for convergence. Besides that, they often help the simulator use less computational resources (time and memory) to find the correct solution. Normally, there is a way to set initial conditions in the simulator. Using a simplified

or less ill-behaving circuit is one way to find good initial conditions.

Another process for obtaining convergence when simulating circuits is to start with values of certain components that work and then to move toward the desired values. For instance, in an amplifier circuit there may be a resistor that can be used to lower the amplifier's gain. The simulator may be able to find a solution to the circuit under a low-gain condition. Then, if the component's value is swept toward the desired value, the simulator may be able to find a final solution.

From the characteristic of SRD shown in Fig. 2 we know that the smaller is the forward bias capacitance, the less nonlinear is the diode model. Thus, we can at first reduce the nonlinearity of the diode model by changing the forward bias capacitance to a smaller value. The reduction of the nonlinearity of the model may very possibly help the simulator to find a solution, which can be used to obtain the desired final solution efficiently.

In order to find a solution to our problem, we have investigated the effect of changing the forward bias capacitance to a smaller value while modeling the diode. At first, we investigated the effect of the reduction on the circuit characteristics. Taking the SRD HP-5082-0835 as an example, we know that the forward bias capacitance (C_f) is about 100 nF, while the reverse bias capacitance (C_r) is about 0.3 pF. Using the equivalent circuit in Fig. 1 to calculate the input impedance in the forward charge storage state, we can see that, when the fundamental frequency is high enough, e.g., 1 GHz or higher, and C_f larger than 0.1 nF, C_f actually does not contribute much to the input impedance with typical parasitic parameters $C_p = 0.2 \text{ pF}$, $R_s = 1.3 \Omega$, and $L_p = 1 \text{ nH}$. And in the reverse bias state, the characteristic of the diode depends only on the reverse bias capacitance C_r . Therefore, if we change C_f to an appropriate lower value according to the fundamental frequency, the characteristic of the circuit will not be radically changed. However, as we shall see in the following simulations, the simulation of the circuit is much faster and easier.

It should be noted that the calculation of the forward bias capacitance by using the I - V curve is approximate. The relationship described by (3) was obtained under the assumption of zero transition time. From the I - V characteristic of the diode shown in Fig. 3 we can see that the highly nonlinear capacitance characteristic is accompanied by a highly nonlinear shunt resistance which depends on the forward bias voltage and RF input power. Therefore, the degree of reduction depends on how much C_f is changed, and the operating conditions of the diode. More accurate method of extracting the parameter C_f should be studied in the future.

III. DESIGN AND SIMULATION OF SRD FREQUENCY MULTIPLIER

Based on the SRD model proposed by Zhang and Räisänen [8], the simulation is directly done with the HP Microwave and RF Design System® (MDS), on a HP workstation (HP 85180). A systematic design of the SRD frequency multiplier is given first.

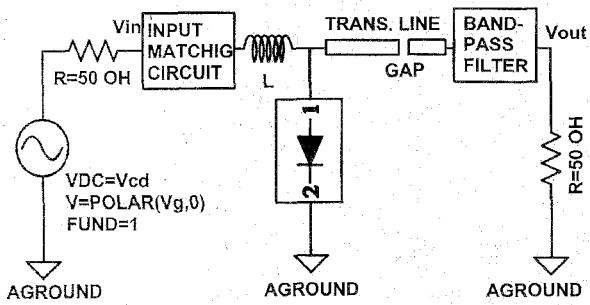


Fig. 4. Schematic of the SRD frequency multiplier circuit.

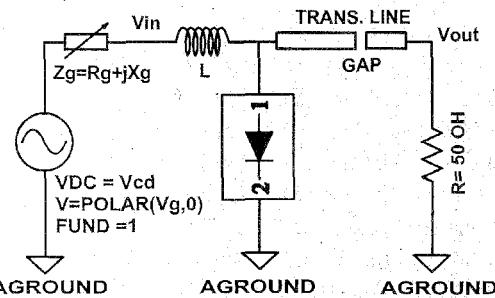


Fig. 5. Simulation circuit for determining optimum source impedance.

The SRD frequency multiplier can be divided into two parts: the comb generator, which is rich in harmonics of fundamental frequency; and the bandpass filter, which is used to extract the desired harmonic from the output of the comb generator. The circuit is illustrated in Fig. 4, in which the bandpass filter and the output circuit of the comb generator, namely the transmission line and gap, form the output circuit of the frequency multiplier.

Normally, the output circuit of the comb generator is simply a piece of 50Ω transmission line. Here, a gap is added in the transmission line, which can be used to block the DC and partially reflect the RF output. It also provides us with more design freedom for optimization of the circuit.

When the output circuit of the comb generator is chosen, a corresponding input circuit can be designed. First, the driving inductor L in Fig. 4 can be estimated by using Hamilton and Hall's method [6]. The details of the calculation are omitted here, but are shown in [11]. Then, the input matching circuit can be designed by using MDS.

The circuit used for determining the optimum source impedance is shown in Fig. 5. The optimum source impedance can be defined as the source impedance which gives the maximum conversion efficiency at the desired harmonic. Note that the circuit in Fig. 5 is basically a comb generator. Since it is going to be used as a part of the frequency multiplier, the output circuit is not just a 50Ω transmission line. Thus, the transmission line and the gap can be optimized to give the maximum conversion efficiency, though the output signal should be filtered further.

Once this optimum source impedance is known, an impedance matching circuit can be designed to match the diode to a 50Ω source. Finally, the driving inductor can be realized by means of a microstrip line. Calculation of a straight microstrip line inductor is simple and an example

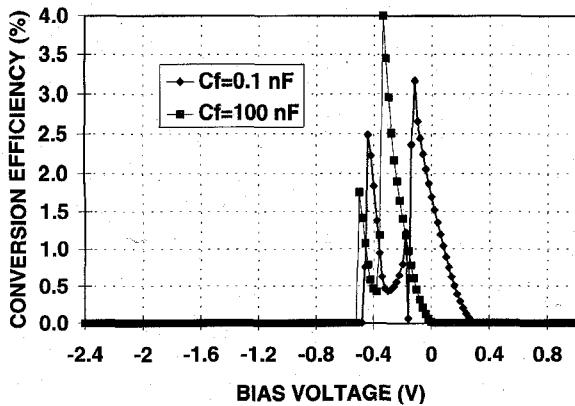
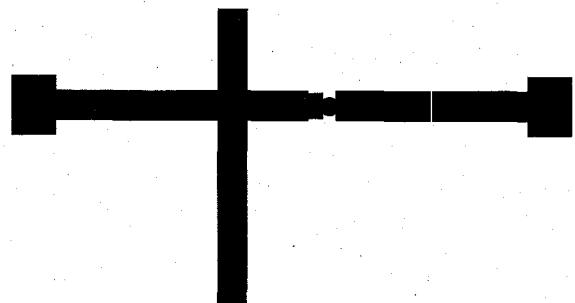


Fig. 6. Simulated results of conversion efficiency vs. bias voltage.

TABLE I
USED COMPUTATIONAL RESOURCES IN
SIMULATIONS OF AN SRD FREQUENCY MULTIPLIER

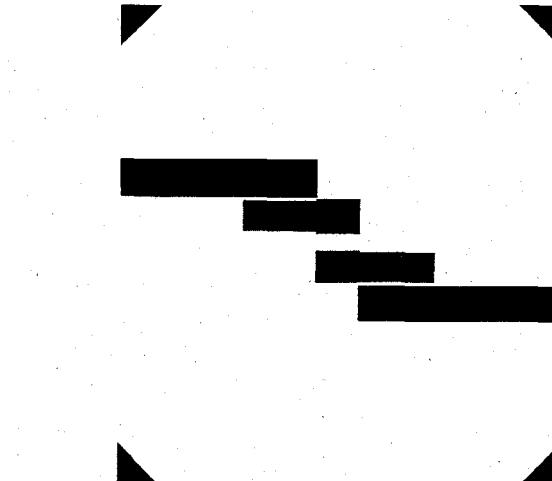
C _f (nF)	CPU (second)	Virtual Memory Used (MB)
100	3690	3.15
0.1	1104	3.15

Fig. 7. Layout of an SRD comb generator. Substrate: RT/Duroid, $\epsilon_r = 2.33$, $h = 1.57$ mm.

is given in [11]. This part of the circuit can be optimized either at this stage or together with the output circuit of the frequency multiplier at a later stage.

The design of output circuit of the frequency multiplier consists mainly of the design of a bandpass filter. The bandwidth of the filter should be determined according to the specific application. Normally, narrow band coupled line bandpass filter is used; whereas wide band bandpass filter could also be employed for a particular application [12]. The design method can be found in other literature [13], [14]. Here a microstrip coupled-line bandpass filter is designed and simulated by using MDS.

Once the designs of the comb generator and the bandpass filter are accomplished, they can be put together to form the frequency multiplier. Apparently, the filter can extract the desired harmonic from the comb generator, and drop the

Fig. 8. Layout of a microstrip coupled line bandpass filter. Substrate: RT/Duroid, $\epsilon_r = 2.33$, $h = 0.79$ mm; scale: 2:1.

unwanted harmonics. However, since the output of the comb generator is very rich of harmonics and the desired harmonic could be a very high order harmonic, the effects of all those unwanted harmonics can not readily be neglected. Therefore, the input matching circuit and the output circuit consisting of a transmission line, a gap and a bandpass filter should be re-optimized to get the optimum performance, e.g., the high conversion efficiency.

In order to verify the method for improving the efficiency of the CAD of the SRD frequency multiplier presented above, we designed a 10×1.25 GHz SRD microstrip frequency multiplier. A large voltage excitation source corresponding to an input power of 13 dBm at 1.25 GHz was used for the harmonic-balance simulation. At first, the circuit was optimized for a high conversion efficiency with C_f equal to 0.1 nF. Then the circuit was refined experimentally. Thereafter, the harmonic-balance analyzes with swept bias voltage were carried out with C_f equal to 0.1 nF and 100 nF and compared with the experiment.

The simulation results are shown in Fig. 6. It can be seen that the shapes of these line pairs are essentially the same. The lines with different C_f are shifted to the right or left of the other. The conversion efficiency is a little lower with lower C_f , which corresponds to the weaker nonlinearity of the model. The shifting of lines is partially due to the different degree of the nonlinearity. Furthermore, in a strongly nonlinear circuit, the low-order mixing frequencies generated by high-degree nonlinearity cannot be neglected readily; thus, the excitation of a strongly nonlinear circuit may offset the DC operating point.

The computational resources required for different C_f are listed in Table I. The results in Table I indicate that the computation time is much less for lower C_f than that for higher C_f . The comparison is made under the condition of the same memory used, as can be seen in the table. Furthermore, it should be pointed out that the simulation with higher C_f shows more trouble in convergence, especially in the case of inappropriate initial conditions.

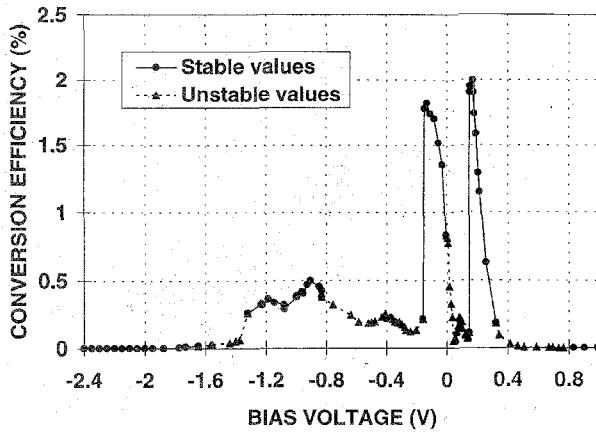


Fig. 9. Experimental results of conversion efficiency vs. bias voltage.

IV. EXPERIMENTS

Experiments were done with the multiplier. The comb generator and bandpass filter were built separately. Their layouts are shown in Figs. 7 and 8, respectively. The HP ceramic packaged SRD (HP-5082-0835) was used. The substrate thickness of the comb generator was chosen to match the ceramic package. The bandpass filter could also be integrated on the same substrate as the comb generator. However, a separate bandpass filter, which has more freedom in choosing substrates, and which provides the flexibility of experimentation, was used.

The input signal was a 1.25 GHz sinusoidal signal at the power level of 13 dBm, which was measured directly at the input port of the multiplier with a spectrum analyzer (Tektronix 2782). The DC bias voltage was applied through a bias tee. The output power was measured at the 10th harmonic using the same spectrum analyzer.

The experiment was carried out by changing the bias voltage and recording output power. The conversion efficiency was calculated by dividing the output power by the available power at the input port. The measured results are shown in Fig. 9. The points connected with dashed-lines represent cases where the output signal showed spurious behavior, caused by spurious oscillations in the circuit.

Fig. 9 shows that the conversion efficiency varies with bias voltage in a similar way as in the above simulations. The lower experimental efficiency than the calculated result is caused by the loss of the circuit.

It should be noted that the parasitics arising from mounting the packaged diode have been neglected in the simulations. However, both the simulation and experiment show that the circuit is quite sensitive to the length of the transmission line between the diode and the gap in the output circuit, which is closely related to the mounting structure of the diode. Therefore, the effects of diode mounting structure should not be neglected in more accurate analyzes. Numerical electromagnetic analyzes of the effects of the diode mounting structure should be done for better modeling of the hybrid SRD frequency multiplier.

V. CONCLUSION

The CAD of SRD frequency multipliers can be made more efficient and easier to accomplish by the method of reducing

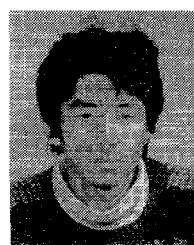
the nonlinearity of the SRD model in the simulation. The experiment shows that the simulated results can be used to guide the SRD frequency multiplier design very well to achieve a high conversion efficiency. An efficiency of more than 2% was achieved at 12.5 GHz with a 10th harmonic multiplier using microstrip circuits. In general, the method could also be applied to CAD of circuits using other very strong nonlinear devices.

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Antti V. Räisänen (S'76-M'81-SM'85-F'94), for a photograph and biography, see this issue, p. 2165.

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Very-High-Rank Avalanche Diode Frequency Multiplier

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AND J. MICHEL

Abstract—Recent experimental observations on silicon avalanche diode multipliers operated at about 35-GHz output frequency are presented. High-rank (up to 35) frequency multiplication is achieved with output power over 250 mW and conversion loss of 13 dB. The possibility of frequency multiplication by any integer n ranging from 8 to 35 with the same diode and without any idler circuit is pointed out. It is concluded that any output frequency can be selected between 28 and 39 GHz by varying the input frequency and the circuit tuning.

The utilization of the nonlinearity of the avalanche in an avalanche diode enables frequency multiplication [1]. This mode of operation is somewhat analogous to frequency multiplication by varactor diodes but the avalanche behaves as a nonlinear inductor as opposed to the nonlinear capacitance effect found in varactor diodes [2]-[5]. This means that, for avalanche diodes in multiplication mode, the depletion layer width can be constant so that the series resistance is much smaller than in varactor diodes. Besides, the violent nonlinearity of the avalanche allows frequency multiplication by any integer n , up to a very-high harmonic rank without any idler circuit.

A computer program has been developed to design the semiconductor device and has been very useful for impedance matching between the diode and the circuit.

Diffused p^+ -n junctions have been used. The electrical field profiles show that they are close to p-i-n type (Fig. 1). The breakdown voltages are of about 20 V and the junction diameter of about 70 μm .

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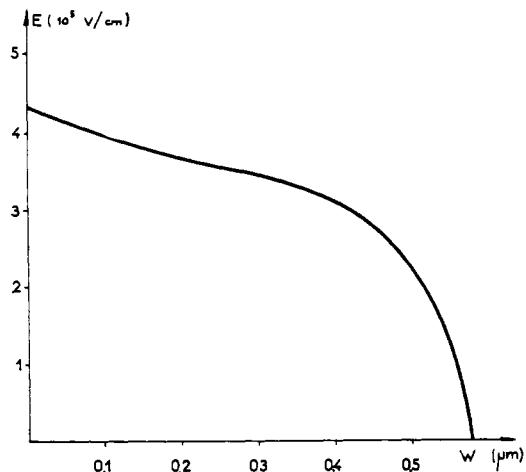


Fig. 1. Measured "field profile" of the diodes used in frequency multiplier.

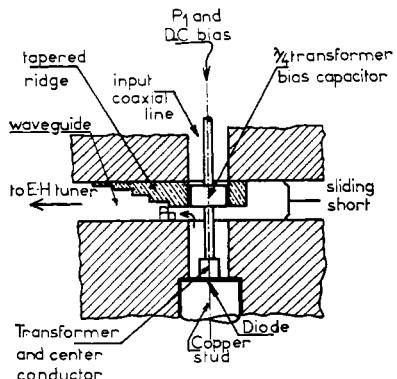


Fig. 2. Multiplier circuit.

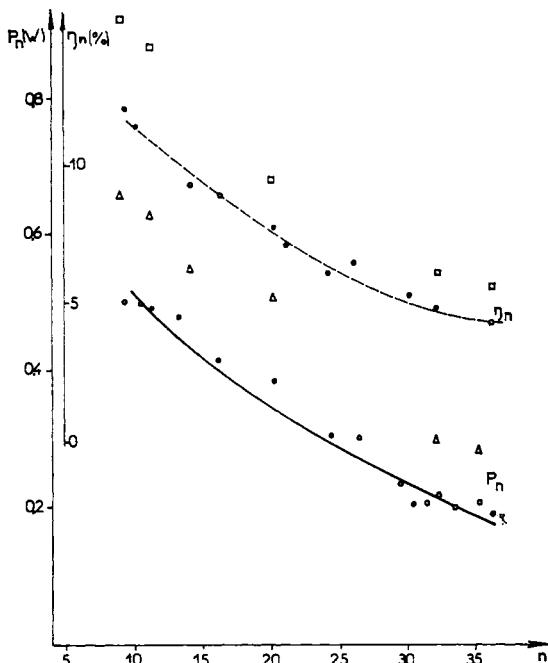


Fig. 3. Output power and conversion rate versus harmonic rank. The solid lines are the output power and corresponding conversion rate obtained with the same packaged diode; the data are the maximum output power and corresponding conversion rate obtained with unpackaged diodes.

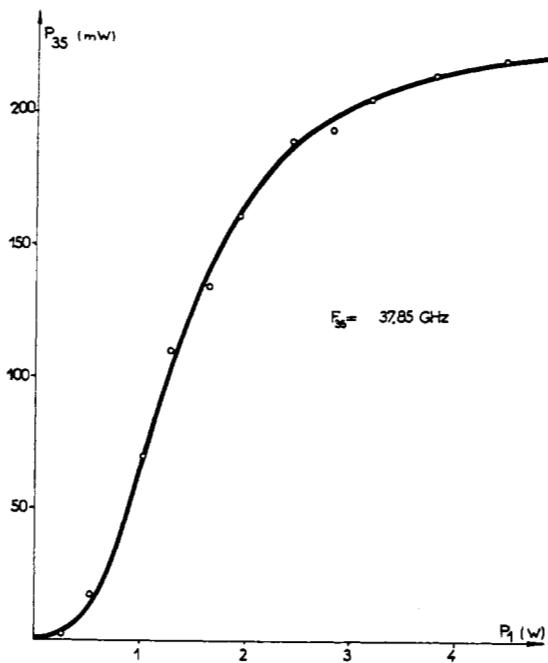


Fig. 4. Output power versus input power in multiplication by 35.
 $F_{35} = 37.85 \text{ GHz}$, $P_0 = 2.5 \text{ W}$.

for this output frequency range (30–40 GHz). Two types of diode structure have been used: standard S4 packaged diodes and diodes without encapsulation whose contact features are similar to those used in beam lead technology. These diodes provide negligibly small output power in the IMPATT mode.

The multiplier tests are made with the circuit shown in Fig. 2. The diode terminates a matched low-impedance coaxial line which passes through the waveguide. The input power and dc bias current are fed by this coaxial line. The harmonic power generated by the diode is coupled to the rectangular waveguide by a coaxial-to-waveguide transition matched by a tapered ridge junction. Tuning is achieved by a sliding short circuit at one side and an E-H tuner at the other.

The nonlinearity of the avalanche increases as the input frequency decreases which enables increasing harmonic order for output frequencies of the same order. This is shown in Fig. 3. The harmonic rank is varied by a change in the input frequency and circuit tuning. The solid lines are obtained with the same S4 packaged diode. The data are the maximum output powers and corresponding conversion losses obtained with unpackaged diodes. The output frequencies range from 30 to 35 GHz. In multiplication by 9 output power of 640 mW is achieved with conversion loss of 8.2 dB while in multiplication by 35 the output power is still as high as 280 mW with a conversion loss of 13 dB.

A typical output power as a function of the input power in multiplication by 35 is shown in Fig. 4. This curve is obtained with a constant dc power of 2.5 W. The circuit is tuned for maximum output power for each point of input power. The output power begins to saturate at about 220 mW corresponding to 13-dB conversion loss. As the dc voltage across the diode is a decreasing function of the input power at constant dc bias current, the dc power decreases when the input power increases, so that at high input power for a constant dc bias current the overall efficiency is nearly reduced to the conversion loss.

Another interesting aspect is that any output frequency can be achieved between 28 and 39 GHz by a change in the input frequency from 1 to 1.2 GHz and in the circuit tuning in order to select a particular harmonic. The output power varies on the order of 2 dB over the output frequency range for a constant input power.

All these results are obtained with at least a 15-dB ratio between the power on the selected frequency and the power on all the other harmonic frequencies.

In conclusion, we have described the main results obtained with a high-rank frequency multiplier without idler circuit using avalanche diodes. This type of multiplier seems to be very attractive for those

applications where high power, stabilized frequency, and ease in output frequency tuning is needed.

The noise figure in multiplication by 35 seems to be similar to that obtained in multiplication by 10 which is much better than in the ATT mode (26 dB at 10 kHz from carrier) [4].

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An Internally Striped Planar Laser with 3-μm Stripe Width Oscillating in Transverse Single Mode

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Abstract—A new type of stripe-geometry laser is proposed. A very small lateral current spreading and a transverse single-mode oscillation are realized in this structure with a near-field pattern as narrow as 3 μm.

INTRODUCTION

In optical communication it is necessary to realize a single-mode operation of a semiconductor laser with a narrow near-field pattern for the coupling with a optical fiber. The diameter of the core of the clad-type fiber for a single-mode transmission is about 3 μm for a fractional difference of refractive index of 1 percent and a wavelength of 9000 Å.

Various types of stripe-geometry laser have been proposed [1]–[4] to obtain a low current and a single-mode oscillation. In this letter, we propose an "internally striped planar (ISP) laser." The ISP laser is very well suited for the coupling with a clad-type fiber, for the ISP laser structure enables one to obtain a stripe as narrow as 3 μm.

STRUCTURE AND FABRICATION

The structure of the ISP laser is shown in Fig. 1. Unlike the other types of stripe-geometry laser [1]–[4], the ISP laser has "n-p-n-p" grown layers. The internal stripe p-Ga_{0.7}Al_{0.3}As is formed in the upper n-Ga_{0.7}Al_{0.3}As layer by selective diffusion techniques. When Al content, layer thicknesses, and doping levels are properly controlled, the upper n-Ga_{0.7}Al_{0.3}As layer acts as a current-intercepting region and the stripe p-Ga_{0.7}Al_{0.3}As as a current-conducting region, as can be understood by the V-I characteristics shown in Fig. 2.

The lateral current spreading is smaller in the ISP laser than in the planar stripe laser [4], for the current spreading in the ISP laser takes place mostly in the active p-GaAs layer. When compared with the proton-bombardment-insulated laser [3], although the current spreading may be larger, the lateral optical confinement may be better in the ISP laser because of a higher refractive index in the proton-bombarded region.

The "n-p-n-p" structure is made by an ordinary successive solution growth method. The first n-Ga_{0.7}Al_{0.3}As layer is about 3 μm thick, using Sn as a dopant; the second active p-GaAs layer is 0.6–1 μm thick, using Si; the third n-Ga_{0.7}Al_{0.3}As layer is about 1 μm thick, using Sn; the last p-GaAs layer is about 1 μm thick, using Ge.

The stripe p-Ga_{0.7}Al_{0.3}As is formed by selective diffusion techniques using ZnAs₂ as a diffusant source. A masking layer against Zn diffusion is a deposited SiO₂ layer with etched-off windows.

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Effects of Active Microwave Device Parameters on Microwave Harmonic Frequency Generators

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Abstract

Modern microwave and RF systems are increasingly utilizing internal frequency upconversion techniques. This paper develops improved methods of designing active microwave frequency multipliers utilizing MESFET and HEMT devices. The methods extend and improve the accuracy of classical techniques developed over the past few years.

I. INTRODUCTION

Many RF and microwave systems require internal generation of higher frequency signal power than resident in some fundamental low frequency utilized in the system. Traditionally, such higher frequencies have been created by heavily driving nonlinear passive diodes at some fundamental frequency and following this with stages of amplification to achieve power at a harmonic frequency. More recently, microwave transistors have been employed in this capacity. They provide definite advantages over their passive counterparts such as conversion gain and isolation. Consequently, they are considered more efficient in component savings and high frequency signal production. [1].

II. HARMONIC GENERATION

To create harmonics of a fundamental frequency signal (f_0), MESFET and HEMT devices are frequently employed in a system configuration as shown in Figure 1.

The model for a class of active devices (MESFET/HEMT) which may be utilized in the configuration of Figure 1 is shown in Figure 2.

This device model reveals several mechanisms for the production of frequency multiples of a fundamental input frequency (f_0). Among these are the nonlinearities of (C_{gs}), (C_{gd}), diodes, nonlinearities in the controlled current source with respect to (V_{ds}) and (V_{gs}) and the nonlinear conductors $g_{ds} = \frac{dI_{DS}}{dV_{DS}}$.

In order to utilize the active device for frequency multiplication, a *frequently used* procedure is to bias the device gate at below pinchoff and operate it so that it will conduct only over a portion of the fundamental drive frequency cycle: an idealized version of the device model (Figure 2) is then employed to compute the optimum *conduction angle* which will produce the maximum signal output at a certain harmonic.

This procedure, in essence, utilizes a greatly simplified version of the device model as shown in Figure 3.

The current model I_{DS} in this *ideal model* is a highly simplified current which is linearly related to V_{gs} down to pinchoff and is zero for lower gate voltages. The present paper utilizes quantitative results based on actual PHEMT models (Figure 2) and simplified versions to establish the effects of the real world parasitics (which are evident in the complete model of Figure 2) on true harmonic generation.

To illustrate the critical nature of the impact on

the traditional design technique, Figure 4 shows a conduction angle plot for the model of Figure 3. This is the standard form utilized in traditional design where the appropriate conduction angle is selected (e.g. conduction angle = 80° for $n = 3$). The current paper will develop, by systematic step-by-step analysis, the effects of the parasitics and realistic device parameters have on multiplier design. An example is shown in Figure 5, where a realistic current source I_{DS} has been substituted for the idealized model used previously in Figure 3 (no other changes were introduced).

Table 1 shows the different elements of complexity introduced to this initial *ideal model* of Figure 3. Column 1 shows the names of the different cases tested. Column 2 shows the elements present in each model. For each case, the harmonic current vs. conduction angle was quantified using simulations in Advanced Design System (ADS). Case A is the ideal model, shown in Figure 3. The first element of complexity added was the non-linear gate-source capacitance C_{gs} , shown in Table 1, case B. For case C, the linear I_{ds} current source was replaced with one having a quadratic I_{ds} vs V_{gs} relationship [2], [4]:

$$I_{ds} = I_{dss} * (1 - V_{gs}/V_p)^2 \quad (1)$$

Case D contains an I_{ds} current source having a quadratic I_{ds} vs V_{gs} relationship and includes the output conductance g_{ds} . In case E, the linear I_{ds} of case A is replaced with a I_{ds} current source utilizing the Angelov model [5], which models and actual PHEMT transistor. In case F, the full PHEMT model (Fig. 2) is tested.

Figures 5-8 show a comparison of the normalized output current vs conduction angle. A perusal of these figures reveal that so-called "optimum" operating biases and drive levels via proper conduction angle are no longer appropriate. In the case of a typical doubler design, the second harmonic content (Figure 6) is to be maximized. The ideal model of case A would require the expected conduction angle of around 120 degrees. However, when device models containing the quadratic I_{ds} current source (cases C, D) are utilized, a conduction angle of around 135 degrees would be optimum. The model representing the actual PHEMT (case F), would have optimum second harmonic output between 20 and

60 degrees. For the case of a tripler design, similar differences in the optimum choice of conduction angle exist. The optimum conduction angle for each case is summarized in Table 2.

The similarities between cases also give some hints as to which elements provide the greatest source of non-linearity. It is clear that case A is similar to case B, case C is similar to case D, and case E is similar to case F. This suggests that the I_{ds} current source is the dominant source of non-linearity over the entire 360 possible degrees of conduction angle.

III. CONCLUSION

This paper has examined design techniques for active microwave multipliers utilizing realistic active device data. It has demonstrated through systematic analysis that in order for significantly improved accuracy, realistic device models must be employed. The results suggest that more realistic multiplier design rules for physical real world multiplier designs are necessary.

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IV. FIGURES

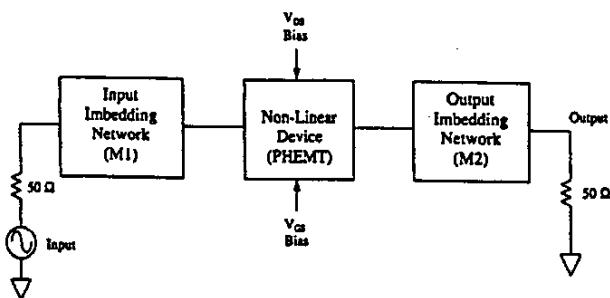


Figure 1. Block Diagram of harmonic generation system

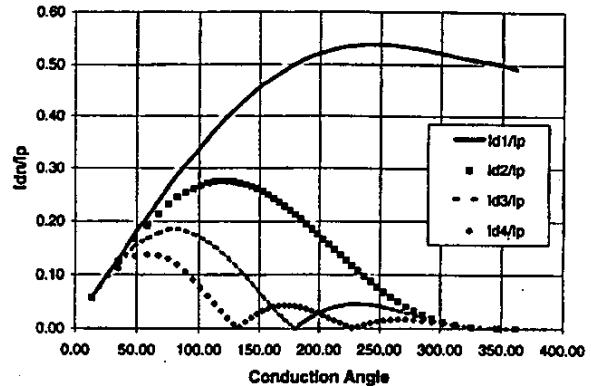


Figure 4. Normalized output current vs conduction angle for simplified device model.

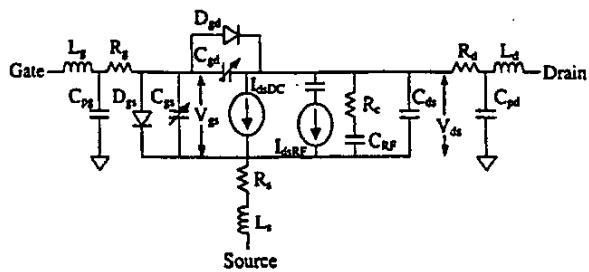


Figure 2. PHEMT Device Model

Case	Elements
A	Linear I_{ds} vs V_{gs} current source, Gate-Drain Diode (D_{gd}), Gate-Source Diode (D_{gs})
B	(D_{gd}), Gate-Source Diode (D_{gs}), Nonlinear Gate-Source Capacitance (C_{gs})
C	Quadratic I_{ds} vs V_{gs} current source, Gate-Drain Diode (D_{gd}), Gate-Source Diode (D_{gs})
D	conductance (g_{ds}), Gate-Drain Diode (D_{gd}), Gate-Source Diode (D_{gs}), Model), Gate-Drain Diode (D_{gd}), Gate-Source Diode (D_{gs})
E	PHEMT device model including all elements (see Figure 2)
F	

Table 1. Model elements for each case tested.

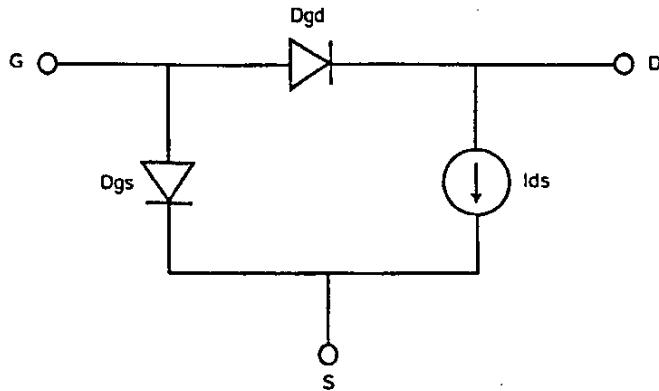


Figure 3. Simplified Device Model

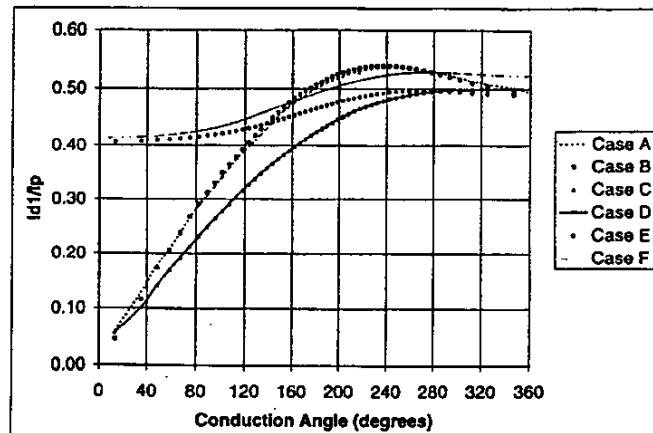


Figure 5. Normalized fundamental output current vs conduction angle.

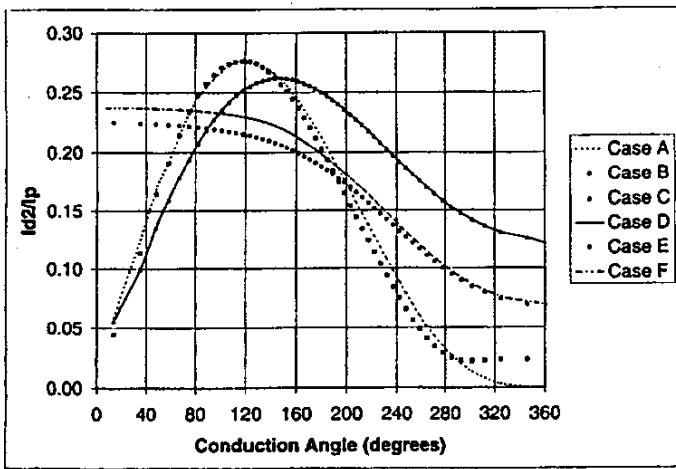


Figure 6. Normalized second harmonic output current vs conduction angle.

Case	Approximate Optimum Conduction Angle ($2f_0$)			
	f_0	$2f_0$	$3f_0$	$4f_0$
A	230	120	80	60
B	230	120	80	60
C	360	135	100	75
D	360	135	100	75
E	255	20 - 60	20 - 40	20 - 40
F	280	20 - 60	20 - 40	20 - 40

Table 2. Approximate optimum conduction angle for each case tested.

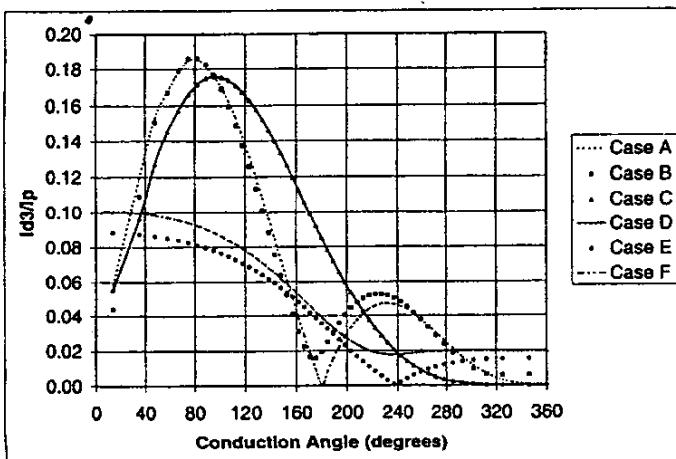


Figure 7. Normalized third harmonic output current vs conduction angle.

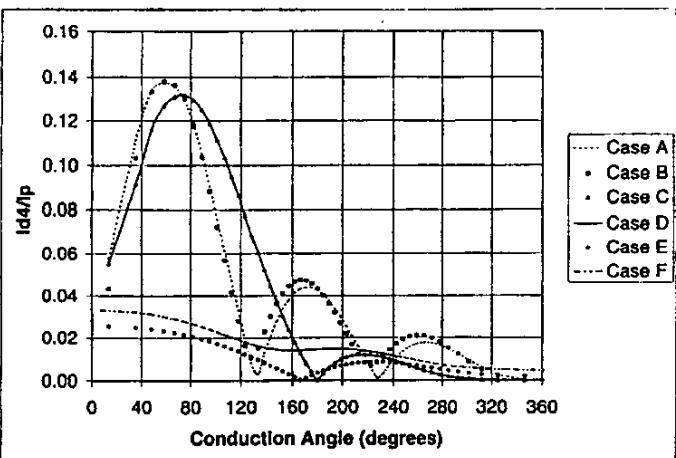


Figure 8. Normalized fourth harmonic output current vs conduction angle.

A 150 to 220 GHz Balanced Doubler MMIC Using a 50 nm Metamorphic HEMT Technology

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Abstract — A coplanar millimeter wave doubler MMIC covering the entire G-band was developed. Based on a 50 nm metamorphic HEMT technology, the circuit demonstrates an output power of more than –12 dBm between 150- and 220 GHz for an input power of 0 dBm. By increasing the input power to 12 dBm an output power exceeding 0 dBm was obtained in the frequency range between 180- and 220 GHz. Good fundamental rejection was ensured by using a Marchand Balun for balancing the design. The doubler was also used to provide the LO signal for a 170 to 200 GHz resistive FET mixer, yielding a conversion loss of 10 dB.

I. INTRODUCTION

Active and passive millimeter and submillimeter-wave sensors penetrate the frequency range up to 1 THz. Applications are radiometric imagers focused on the atmospheric windows at 94 GHz, 140 GHz and 220 GHz as well as atmospheric sounders and environmental sensors at frequencies where characteristic resonance frequencies of molecules exist [1]. Also, next generation automotive collision avoidance radars and short range industrial sensors come into play in environmentally harsh conditions were optical and ultra-sonic sensors fail due to dust and pollution. Not all of these systems are realizable with direct detection systems where the RF signal is directly rectified to DC and then processed. Local oscillator sources are needed in RADARs, spectrometers, synthetic aperture systems to provide phase synchronous down conversion, to measure absorption, or simply as illumination to enhance the contrast of a scene to be observed. Frequency generation beyond 100 GHz is generally a demanding task, which is mostly solved with varactor multipliers. As InP based HEMT transistors advance in performance, there is the possibility of realizing active FET frequency multipliers monolithically up to frequencies as high as 220 GHz. The advantages of active FET multipliers are their broad bandwidth and good conversion efficiency, in contrast to resistive diode multipliers which are broadband but inefficient or varactor multipliers which demonstrate good conversion properties only over a narrow

bandwidth [2]. A narrow band HEMT doubler at 164 GHz was already demonstrated in [3].

In this paper, we describe the development of a balanced broadband frequency doubler in a coplanar environment based on a highly advanced 50 nm MHEMT technology.

II. TECHNOLOGY

The technology employed is a metamorphic HEMT structure, grown on semi-insulating 4" GaAs substrates. The metamorphic buffer layer consists of a linear $\text{In}_x\text{Al}_{0.48}\text{Ga}_{0.52-x}\text{As}$ ($x = 0 \rightarrow 0.52$) grading, that finally yields the InP lattice constant. The layer structure comprises a composite channel consisting of an 80 % In main channel for high carrier velocity. Furthermore, a 53 % indium content sub-channel was introduced, which helps to reduce impact ionization and thus improves the breakdown behavior. The on-state breakdown voltage achieved with the described layer structure is 1.5 V, and the off-state breakdown voltage is about 2.0 V. E-beam lithography with a four layer PMMA resist was used to pattern the T-shaped gate with a final foot print length of 50 nm. The Pt-Ti-Pt-Au gates are fully passivated using a CVD deposited silicon-nitride. The active device area is mesa defined using a chemical wet etch.

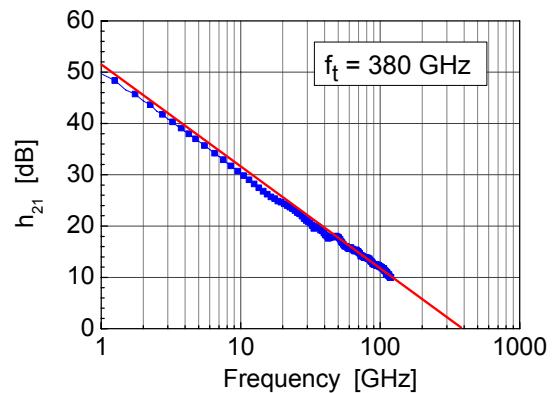


Fig. 1. Current gain for a $2 \times 30 \mu\text{m}$ MHEMT with extrapolated f_t .

Using this process technology a maximum extrinsic trans-conductance of 1600 mS/mm was measured, resulting in an equal transit frequency (f_t) and maximum frequency of oscillation (f_{max}) of 380 GHz for a $2 \times 30 \mu\text{m}$ device as displayed in Fig. 1. The maximum current of the device structure is 1300 mA/mm. Accelerated life time tests in air were performed at 200, 220 and 240 °C channel temperature and at 1 V drain bias. The failure criterion was a 10 % degradation of the maximum transconductance. Based on a log-normal distribution, an activation energy of 1.6 eV and a median life time of 2×10^6 hours at a channel temperature of 125 °C were calculated. More details on our metamorphic HEMT technology can be found in [4].

III. CIRCUIT DESIGN

The circuit topology employs a balanced design using coplanar line technology as shown in Fig. 2. The MMIC consists of a planar Marchand balun at the input to divide the incoming signal equally onto two branches with 180 degrees of phase-shift. The advantages of a Marchand balun are the broadband frequency response, exact phase difference and very good amplitude balance throughout the entire band of operation. The balun used in this circuit comprises of two coupled line sections of 155 μm length. The performance was verified with electro magnetic (EM) simulations using Agilent Momentum and Ansoft HFFS. It is important to mention that the resistivity of the used metal layer has to be taken into account in EM simulations because of significant loss. This is due to the fact, that design rules allow only a thin metal layer to layout tight spacing of the lines, needed, to achieve sufficient coupling. The balun is followed by the gate bias section which is also used for matching at the input of the FETs.

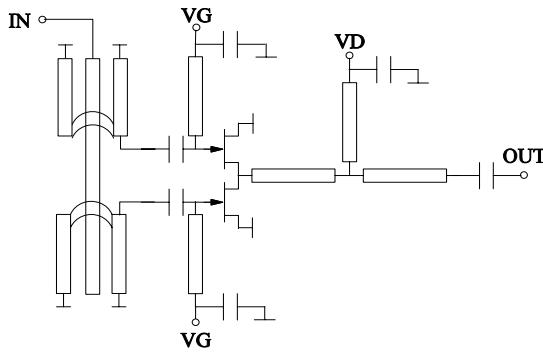
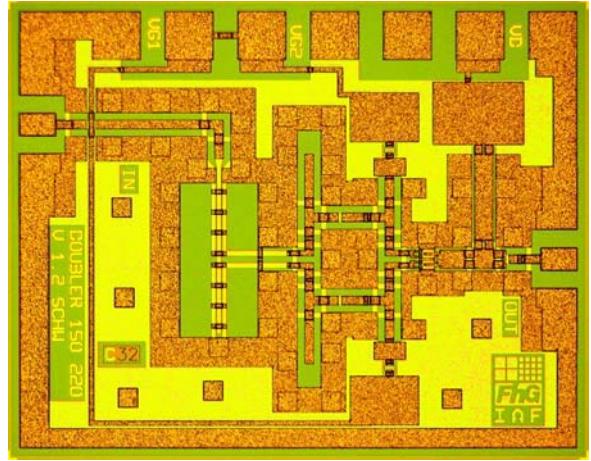


Fig. 2. Circuit diagram of the balanced G-band doubler.

The active devices have a gate width of $2 \times 30 \mu\text{m}$ and are biased in a class B manner. The FET's layout is realized by truncating the gate bus of a $4 \times 30 \mu\text{m}$ transistor layout into two halves. This way, the drain connection of the two FETs is as short as possible which in turn guarantees the cancellation of the fundamental signal at the drain.

The second harmonic frequency matching is done by the drain bias network. It is straight forward because the shorting of the fundamental frequency at the output is implemented by the balanced design [5]. Simply spoken, the difficulties in achieving the right load conditions at the output was circumvented by putting more effort on the input side at half of the frequency. A photograph of the doubler MMIC is shown in Fig. 3.



For this configuration an output power of more than -12 dBm was achieved from 150 to 220 GHz, with a maximum output power of -6 dBm at 180 GHz, as shown in Fig. 5.

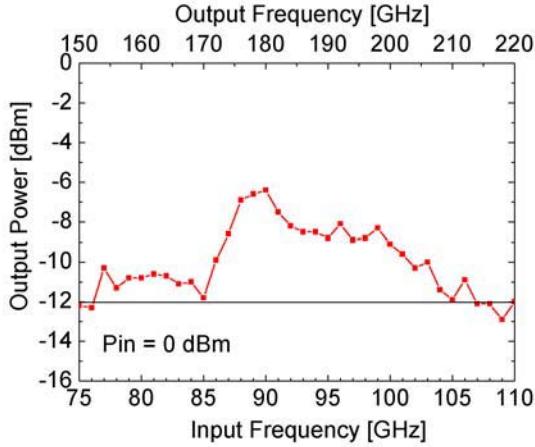


Fig. 5. Output power of the G-band doubler MMIC for 0 dBm input power.

The gate voltage was adjusted to 0 V and the drain voltage to 0.8 V resulting in a 25 mA quiescent current. More input drive power of approximately 12 dBm was available between 90 GHz and 110 GHz from an in-house build medium power amplifier module. By using this module to increase the input power, the output power at the doubled frequency could be kept above 0 dBm, again having the maximum power level at 180 GHz with 4 dBm as shown in Fig. 6.

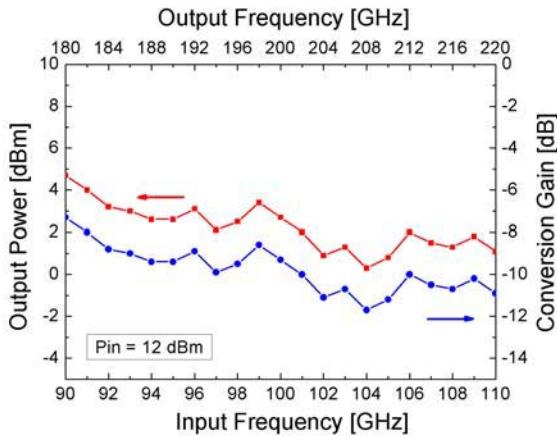


Fig. 6. Output power and conversion gain of the G-band doubler for 12 dBm input power.

At 12 dBm input power, the gate voltage was reduced to -0.2 V to achieve the best conversion properties. With 1 V drain bias, the circuit consumes 25 mA of drain current in operation, which is equal to a current density of 200 mA/mm. Additionally, input power sweeps at 90, 100 and 110 GHz were performed. The smooth behavior of the multiplied signal over the input power variation implies stable operation, as indicated in Fig. 7. Also, with

no input signal applied, no output power is measured. This is important as sometimes multipliers with high conversion efficiencies show oscillations and are therefore acting as sub-harmonic injection locked oscillators.

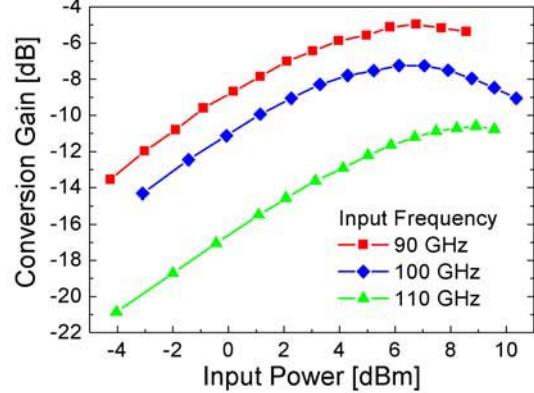


Fig. 7. Conversion gain versus input power of the G-band doubler MMIC for frequencies of 90, 100 and 110 GHz .

To evaluate the yield of the circuit across one wafer, the power level at 220 GHz output frequency was measured for an input power of 0 dBm at 110 GHz at the input of the chip. The DC yield was exceeding 90 %. If a minimum output power of -13.5 dBm was chosen for selection criteria, the RF yield accounted to 50 %.

V. APPLICATION OF THE DOUBLER CHIP AS LO SOURCE FOR A DOWNCONVERTER

To approve the applicability of the developed doubler MMIC, it was used as a local oscillator source for a single ended resistive FET mixer. A resistive FET mixer was chosen because of its ability to perform well at very high frequencies with low LO power [6].

A doubler and a mixer chip were mounted on a silicon substrate with the doubler's output and the mixer's LO input placed as close as possible to keep the connecting bond wires short. The mounted chips are shown in Fig. 8.

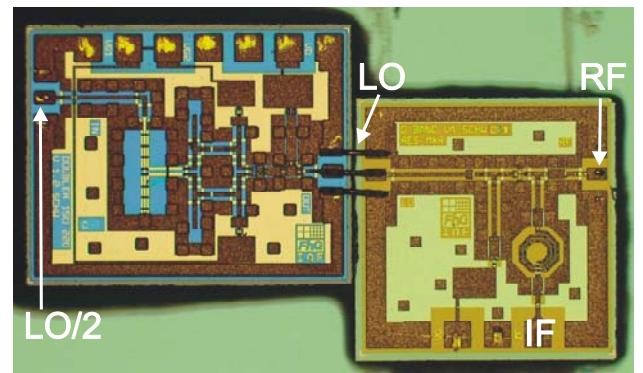


Fig. 8. Doubler MMIC left, and mixer MMIC right, mounted on a silicon substrate with interconnecting bond wires.

To contact the chips during the measurement, DC and RF on-wafer probes were used. The input signal of the doubler was provided using again the W-band HP source module and the MPA module to provide approximately 12 dBm input power at the doubler input. The RF signal was supplied using a G-band S-parameter extension module from Oleson, operated in CW mode. The output power of the Oleson module was characterized before the measurement using the ELVA-1 G-band power sensor. The down converted signal was measured with a spectrum analyzer. To calculate the conversion loss of the mixer, probe and cable losses were accounted for. The doubler mixer combination showed good conversion properties between 170 and 200 GHz with a conversion loss of around 10 dB for a single-side-band (SSB) measurement and an IF frequency of 1 GHz. Above 200 GHz, the mixer conversion loss dropped off sharply, as can be seen in Fig. 9.

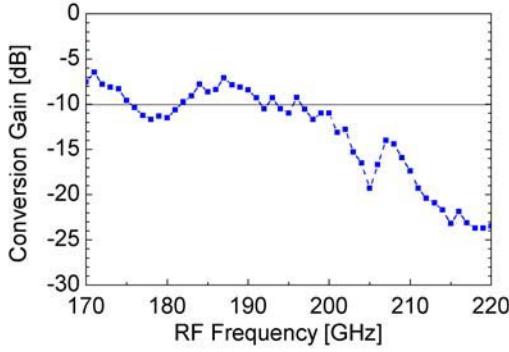


Fig. 9. Measured conversion loss of the doubler-mixer combination from 170 to 220 GHz at an IF frequency of 1 GHz.

VI. CONCLUSION

A broadband doubler MMIC, covering the frequency range from 150 GHz to 220 GHz was realized. The balanced FET multiplier chip was fabricated using a 50 nm gate-length metamorphic HEMT technology and demonstrated a conversion loss better than 12 dB over the entire G-band for an input power of 0 dBm. With 12 dBm of input power, an output power of more than 0 dBm could be achieved between 180 GHz and 220 GHz. Also, the ability of the doubler to serve as a LO source for a mixer was demonstrated, yielding a SSB conversion loss of approximately 10 dB between 170 and 200 GHz.

VII. AKNOWLEDGEMENTS

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High-Efficiency Terahertz Frequency Triplers

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Abstract — Design and experimental analysis of high-power and high-efficiency frequency triplers to the 220 GHz and 440 GHz bands are presented. Test data for the 220 GHz tripler show 23 mW output power with 16 % efficiency. Test data for the 440 GHz tripler show 13 mW output power with 12 % efficiency. The 3 dB bandwidth for both triplers is about 7 %. This performance is comparable to the best reported in the literature at these frequencies. There are no mechanical tuners and thus the triplers may be electronically swept to any frequency in the band. The triplers comprise a waveguide housing, a pair of quartz microstrip circuits and a Virginia Diodes (VDI) GaAs Schottky varactor chip. The simple circuit topology makes it easy to assemble the multipliers and bias the varactors. A version to 800 GHz has been designed and should be available for testing in 2007. The design is scalable to frequencies above 1 THz.

Index Terms — Terahertz, frequency conversion, millimeter wave circuits, GaAs Schottky diodes, waveguide components.

I. INTRODUCTION

The terahertz band spanning the gap between the infrared and millimeter waves is perhaps the least utilized portion of the electromagnetic spectrum. This is primarily due to the lack of suitable electronic components, particularly signal sources with the requisite power and frequency agility to make them useful for communications, imaging, remote sensing and spectroscopic systems. One of the most productive means of generating terahertz radiation has been through frequency multiplication of fundamental microwave sources. The workhorse technology for terahertz frequency multiplication has been the GaAs Schottky diode. These majority carrier devices are characterized by high electron mobility which enables them to be used at terahertz frequencies. [1]

Sources based on frequency multiplication offer many advantages for generating terahertz radiation. The fundamental microwave oscillators are a mature technology offering high output power and efficiency, low noise, electronic tuning and compact design. VDI's current generation of millimeter-wave and terahertz frequency multipliers exhibit wide fixed-tuned bandwidth, high power handling, high efficiency and compact size [2, 3]. The combined microwave oscillator, power amplifier and frequency multiplier cascade provides a very compact, broadband, electronically swept source at frequencies from 30 GHz to well above one terahertz [4, 5]. The 440 GHz tripler reported here was developed as part of a local oscillator system for an 874 GHz radiometer being developed by the NASA Goddard Space Flight Center for atmospheric measurements of ice concentration in clouds.

II. DESIGN

A sketch and schematic diagram of the 440 GHz tripler circuit are shown below in Fig. 1. The tripler comprises a metal waveguide housing split in the E-plane, a pair of quartz microstrip circuits, a VDI GaAs Schottky varactor diode chip and a pair of bond-wires used in the DC bias network. The varactor is a planar flip-chip type with four anodes arranged in anti-series. The chip has a center pad that is soldered to the microstrip line on the quartz circuit and two outer pads that are soldered directly to the waveguide block. This is not a balanced arrangement, but rather the diodes are situated in parallel across an unbalanced microstrip line. The parallel diode arrangement provides an improved thermal path for heat flow from the diodes to the metal waveguide block.

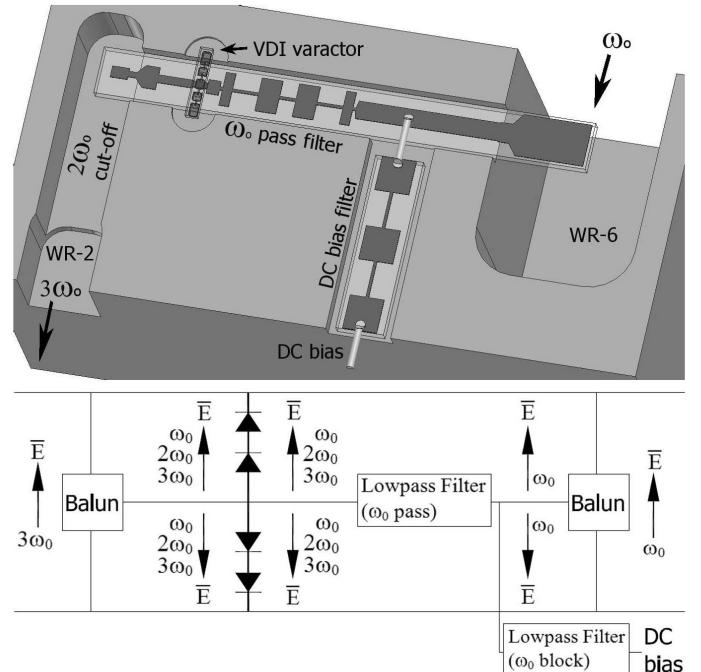


Fig. 1 Sketch and schematic of the 440 GHz frequency tripler. The waveguide block is split in the E-plane and the top half removed to expose the circuits. The waveguide backshorts are machined in a fixed position.

The 220 GHz and 800 GHz tripler circuit topologies are similar but use different varactor chips comprising 6 anodes and 4 anodes respectively. In all three cases, the varactor chips are discrete flip-chips that are soldered to the block and quartz embedding circuit. However, the varactor could easily be

integrated with the embedding circuit if desired with little change to the embedding circuitry [6].

Assembly is relatively simple. First, the circuits are aligned and glued into the block. The varactor chip is then soldered to the block by heating the entire assembly. The varactor chip is aligned to small markers fabricated on the circuit. A pair of 1-mil wires are then bonded to the DC bias circuitry as illustrated in Fig. 1.

A. First Harmonic (ω_0) Circuit

The fundamental excitation at ω_0 transitions from the WR-6 rectangular waveguide to the microstrip circuit via an E-plane probe. The signal propagates through the ω_0 lowpass filter to the varactor diodes. Propagation in the side-channel is blocked by a lowpass DC bias filter. The output waveguide is cut-off at ω_0 and acts as a first harmonic backshort. The length and characteristic impedances of the intervening microstrip lines form the primary tuning elements of the first harmonic embedding impedance.

B. Second Harmonic ($2\omega_0$) Idler Circuit

At the second harmonic, the ω_0 lowpass filter presents an effective short at the point where the diode chip contacts the microstrip line. The idler impedance is thus primarily determined by the inductance of the diode package. Except for conductor losses and parasitic series resistance in the diodes, the idler impedance is purely reactive. As the frequency of operation extends from the band center, the second harmonic coupling to the output microstrip lines gradually increases. However, the output waveguide width is sufficiently reduced near the E-plane probe to cut-off propagation at all second harmonic frequencies. The output waveguide is later stepped to a standard width as shown in the sketch.

C. Third Harmonic ($3\omega_0$) Circuit

The third harmonic signal is coupled to the output waveguide via an E-plane probe. The characteristic impedances and lengths of the microstrip lines from the varactors to the ω_0 pass filter and output waveguide form the primary tuning elements of the third harmonic embedding impedance.

D. Linear Analysis

The three dimensional embedding structure was analyzed using Ansoft's High Frequency Structure Simulator (HFSS™). To reduce the solve space and complexity of the problem, the structure was broken up into four main sections; 1) the input waveguide transition to microstrip including the bias filter, 2) the ω_0 bandpass filter, 3) the varactor chip and nearby microstrip and 4) the transition from microstrip to output waveguide. S-parameter ports were defined within the varactor chip to sample the impedances seen at the anodes. The microstrip sections in 2) and 3) were also cut in half with a magnetic wall to further reduce the solve space.

S-parameter data from the four HFSS models were imported into Agilent's GENESYS™ microwave simulator and connected with microstrip lines. The lengths and characteristic impedances of the transmission lines were varied to achieve optimal embedding impedances at the fundamental, second and third harmonic frequencies. Some of the tuning elements affect impedances at more than one harmonic. Therefore all embedding impedances were optimized simultaneously. Fortunately, it is possible to obtain a nearly optimal solution over a reasonably wide bandwidth without resorting to mechanical tuners.

The Smith Chart in Fig. 2 shows the simulated impedances of the 440 GHz frequency tripler at the fundamental, second harmonic idler and third harmonic frequencies. The swept bands are 135-155 GHz, 270-310 GHz and 405-465 GHz respectively. The impedances at the band centers are nearly optimal at the first and second harmonics. The reactive part of the third harmonic impedance is also nearly optimal at the band center. The real part of the impedance at the third harmonic is somewhat larger than desired.

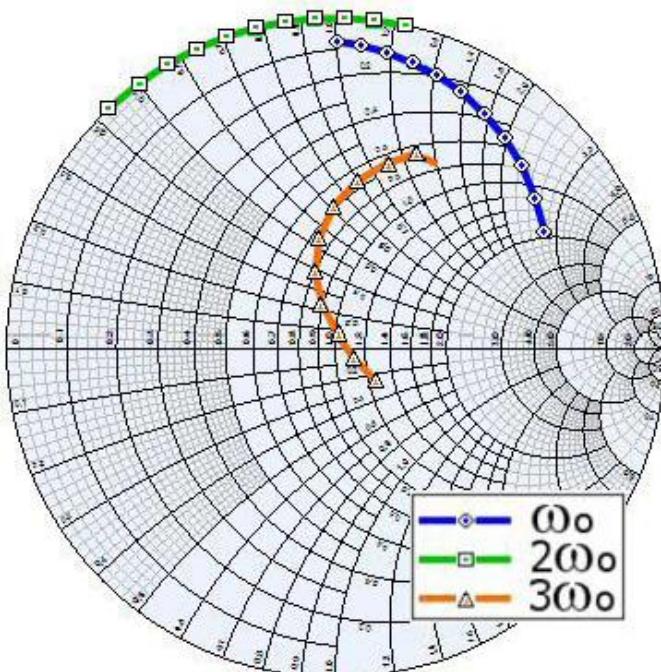


Fig. 2 Smith chart showing the simulated harmonic impedances of the 440 GHz frequency tripler.

E. Non-linear Analysis

Agilent's HARBEC™, a harmonic balance simulator, was used to analyze the non-linear behavior of the varactor. The varactor was terminated at each harmonic using the impedances determined in the linear microwave simulations. Voltage bias was optimized at each frequency to achieve the highest output power and efficiency. Loss mechanisms considered in the analysis include a 4Ω series resistance in

the varactor, 0.2 dB loss in the input waveguide, 0.6 dB loss in the output waveguide and 0.6 dB loss in the microstrip. The waveguide and microstrip losses were calculated in HFSS. Simulated output power for the 440 GHz frequency tripler using 55 mW excitation is shown in Fig. 3. The simulated output power is 2.5 dB higher than the measured value at this drive level. The discrepancy is likely due in part to higher than estimated conductor losses.

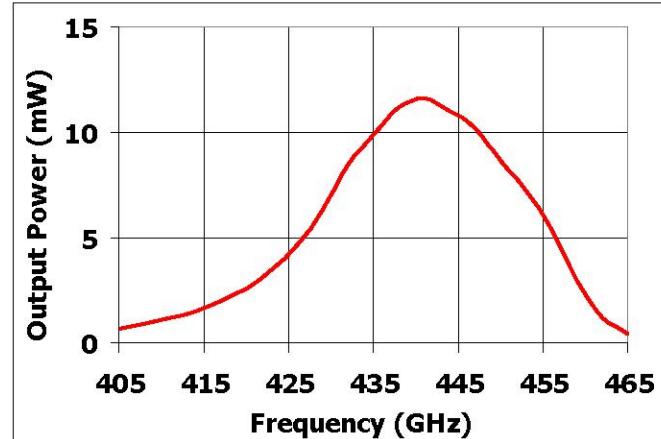


Fig. 3 Harmonic balance simulation of the 440 GHz tripler with 55 mW excitation. Embedding impedances were derived from HFSS simulations. Loss mechanisms considered in the analysis include 4 Ω series resistance in the varactor and 1.4 dB circuit loss.

The graph in Fig. 4 shows simulated input return loss for the 440 GHz tripler. The return loss is greater than 10 dB over a 17 GHz band from 436–453 GHz. The return loss was simulated with a 55 mW input drive. Simulations for the 220 GHz and 800 GHz triplers yield similar results.

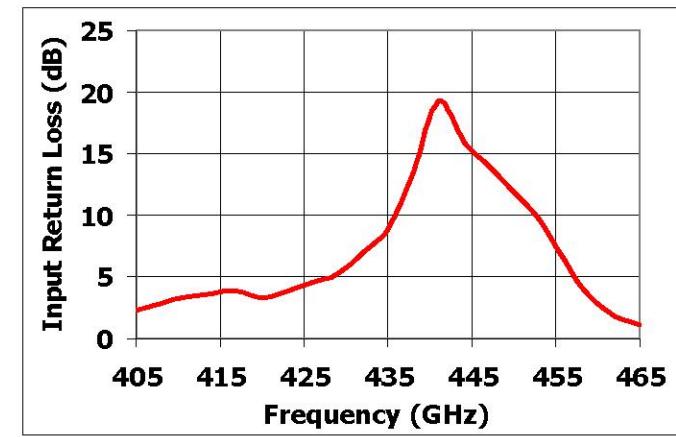


Fig. 4 Simulated input return loss of the 440 GHz tripler.

III. EXPERIMENTAL RESULTS

Input power was provided by a microwave YIG oscillator, MMIC amplifier and a chain of VDI high-power frequency doublers [2]. The input power to the tripler was monitored through a calibrated directional coupler using either a

calibrated Agilent V-band power sensor for measurements in the band 65–75 GHz or an Erickson calorimeter for frequencies above 75 GHz. Output power was measured with an Erickson calorimeter using an appropriate waveguide adapter. No corrections were made for loss in the Erickson power sensor. All power measurements are referenced to the tripler waveguide flanges and are not corrected for internal loss. Fig. 5 shows measured output power for the 440 GHz frequency tripler for input excitation from 15 mW to 75 mW. Peak output power is 9 mW and the 3 dB bandwidth is 7 %. The graph in Fig. 6 shows frequency tripling efficiency as a function of input drive power. The peak efficiency is 12 %. By removing the input coupler we were able to achieve 13 mW.

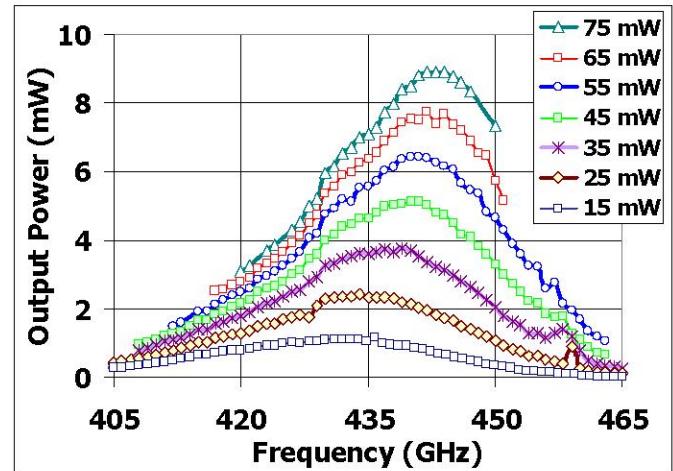


Fig. 5 Measured output power from the 440 GHz frequency tripler. The legend denotes drive power at the fundamental.

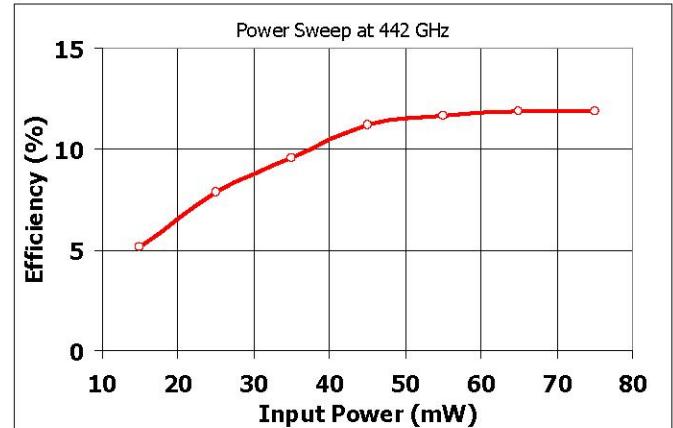


Fig. 6 Measured efficiency as a function of input drive power for the 440 GHz tripler. Peak efficiency is 12 %.

The graph in Fig. 7 shows measured output power for the 220 GHz frequency tripler for input excitation from 25 mW to 150 mW. Peak output power is 23 mW and the 3 dB bandwidth is 7 %. The graph in Fig. 8 shows frequency tripling efficiency as a function of input drive power for the 220 GHz tripler. The peak efficiency is 16 %.

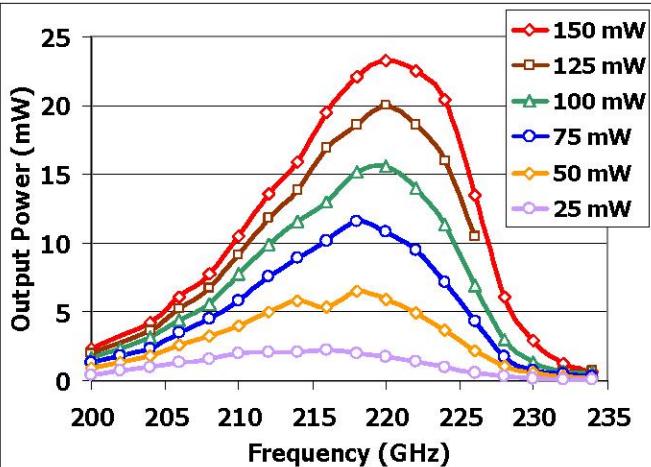


Fig. 7 Measured output power from the 220 GHz frequency tripler. The legend denotes drive power at the fundamental.

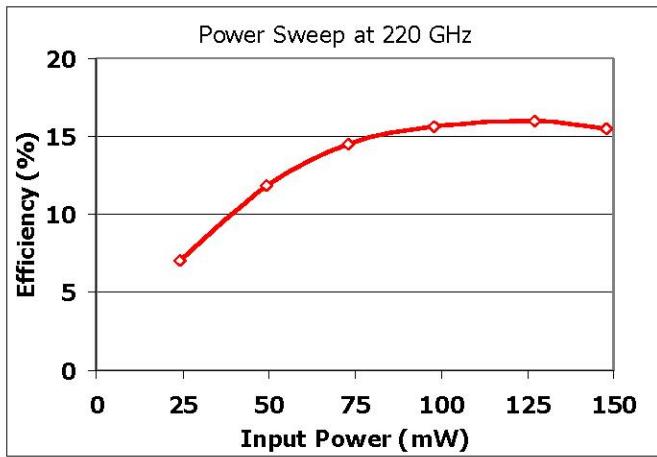


Fig. 8 Measured efficiency of the 220 GHz frequency tripler as a function of input power. Peak efficiency is 16 %.

IV. CONCLUSION

Frequency triplers were designed to bands centered at 220 GHz, 440 GHz and 800 GHz. The design is readily scalable to frequencies above 1 THz. The triplers comprise a metal waveguide housing with a single split in the E-plane, a discrete VDI GaAs Schottky varactor flip-chip, a quartz microstrip embedding circuit and a quartz bias filter circuit. The quartz circuits have a gold metallization pattern on one side and are very simple to fabricate in large quantities using photolithographic techniques. Assembly using the flip-chip varactors has proven to be relatively simple, although future integration of the varactor and embedding circuit should be straightforward, further simplifying the assembly process.

Test data for the 220 GHz tripler show 23 mW output power with 16 % efficiency. Test data for the 440 GHz tripler show 13 mW output power and 12 % peak efficiency. The 3 dB bandwidth for both triplers is about 7 %. This bandwidth is achieved without using mechanical tuners and thus the triplers

may be electronically swept to any frequency in the band. The varactors were originally designed for balanced frequency doublers. Varactors optimized for the tripler architecture should yield improved results. To the best knowledge of the author, the measured performance of these triplers surpasses the best found in the literature at these frequencies [7-12].

ACKNOWLEDGEMENT

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Terahertz Multiplier Circuits

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Abstract — Robust radiation sources in the 1-2 THz range have been sorely lacking from the repertoire of terahertz technologists and scientists. This paper will review the progress in chip fabrication technology, based on planar GaAs Schottky diodes, that has enabled the design and fabrication of multiplier circuits working well into the terahertz range. Recent results obtained with multiplied sources in the 1-2 THz range will be summarized.

Index Terms — Terahertz technology, LO sources, frequency multipliers, Schottky diodes, heterodyne receivers, varactors.

I. INTRODUCTION

Recent years have seen an explosion in the use of terahertz technology for a number of applications such as contraband detection, surveillance, terrain mapping, DNA identification, and tissue identification [1]. Though a number of systems have been demonstrated in the 100-600 GHz range there are distinct advantages to operating at even higher frequencies. For certain other applications, such as spectroscopy and radio astronomy, there is need for robust instrumentation in the 1-2 THz range that will allow scientists to explore this mostly uncharted territory with broadband receivers. Thus, there is a major need to develop and demonstrate easy to use, all solid state sources in the 1-2 THz frequency range.

Conventional sources in this range include backward wave oscillators (BWOs) and FIR lasers. Both of these options are bulky and have limitations in terms of signal purity and bandwidth. In the last few years, a number of rapidly developing technologies have converged to enable compact

sources in the 1-2 THz range. Advanced EM software tools now allow precise modeling of intricate active and passive circuits with high fidelity and have allowed for desktop optimization, drastically cutting down the time from preliminary design to final build. High rpm milling machines have allowed one to utilize split block waveguide circuits with dimensions approaching tens of micrometers making them a feasible approach for terahertz circuits/packaging. Meanwhile, Ka and W-band power amplifiers have matured to a point where it is now possible to pump initial stage multipliers with hundreds of milliwatts of power in the W-band range. And finally, semiconductor device processing tools have been developed that have allowed us to design and build intricate, highly-functional multiplier chips with sub-micrometer dimensions and substrate sculpturing ideally suited for high frequency applications. The goal of this paper is to highlight the chip fabrication technology that has been developed to realize terahertz MMICs. Recent results in the 1-2 THz band will be summarized.

II. ADVANCES IN PLANAR SCHOTTKY DIODE TECHNOLOGY

At the heart of every terahertz multiplier chip is the GaAs planar Schottky anode. A schematic of the planar Schottky anode that has been developed for terahertz frequencies is shown in Figure 1 (this schematic is not to scale and certain dimensions are exaggerated for instructional purposes). A number of parasitic elements are identified on this schematic. For high cutoff frequencies it is important to minimize these parasitics. Secondly, it is important to have knowledge of

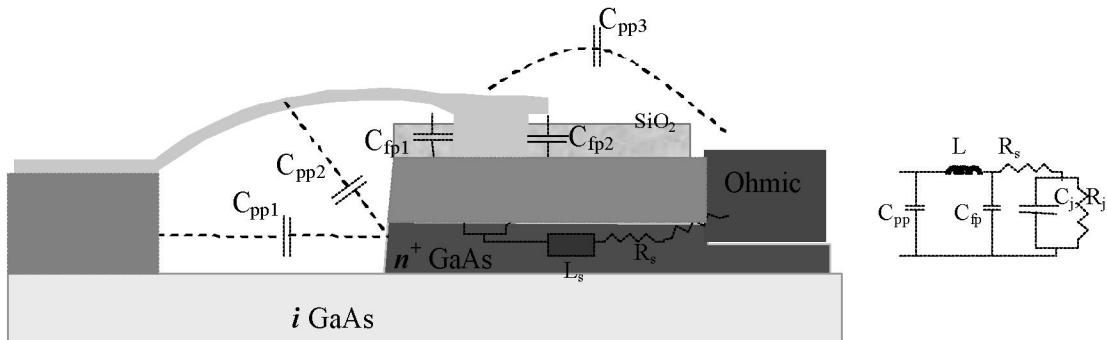


Figure 1: A schematic representation of the planar Schottky anode (not to scale) and its simple equivalent circuit are shown. For terahertz multiplier chips it is important to minimize the parasitics and design the circuit taking the parasitics into consideration.

these parasitics in order to design the circuit around the Schottky diode. Some of these parasitic capacitances are much less than 1 fF and thus are difficult to measure precisely. However, modern EM wave solvers allow one to model the chip topology with great precision and can allow one to get a feel for these parasitics by cleverly defining simulation ports. The bandwidth of a circuit can be severely limited if these parasitics are not taken into consideration.

Moreover, the anode structure should be formulated to reduce these parasitics as much as possible. One modification to the traditional planar Schottky diode fabrication process was the use of "T-gate" like structures as the Schottky anodes as compared to circular anodes. Traditionally, circular anodes patterned in a dielectric layer had been used as Schottky anodes. As the frequency of operation is increased it becomes imperative to scale the device accordingly and reduce the parasitics. However, as the anode area is scaled down to micrometer and sub-micrometer dimensions it becomes harder and harder to obtain uniform Schottky contacts since it involves the etching of the passivation dielectric. An e-beam based process was developed that basically uses an anode structure similar to the "T-gates" of high frequency transistors. It utilizes an e-beam direct write procedure and can pattern sub-micrometer structures. While the scaling feasibility of this process is a major advantage, this approach also results in lower series resistance of the device. By making the anode long and thin, the access resistance can be reduced by a factor of two [2].

A critical dimension that needs to be optimized for each anode is the distance between the anode and the edge of the ohmic contact. This needs to be reduced to decrease the series resistance, however, reducing this distance results in an increase of the fringing finger-to-pad capacitance. This distance is optimized based on the circuit impedance and the patterning is done via e-beam. Mesas smaller than $15 \times 15 \mu\text{m}^2$

have been successfully fabricated. Due to the small dimensions at these frequencies, the finger (bridge) and the anode are fabricated together to eliminate alignment concerns, resulting in self-aligned anodes. It is also critical for successful anode definition to correct for proximity effects on the e-beam since close location of the ohmic metal can have significant effect on the electron dose requirements. A close-up of a tripler chip at 1.9 THz is shown in Figure 2 (left). This is based on a balanced design and requires that both of the anodes are electrically identical. The input power is coupled via an integrated E-plane probe. The right side of Figure 2 shows a slightly different approach used for a 1.6 THz doubler. The figure shows the doubler when placed in one half of the split waveguide block. This doubler is also a balanced design, but in this particular case the anodes actually sit inside the input waveguide. Again, care must be taken to make sure that both anodes are electrically identical. Naïvely, this implies that anode sizes must be identical. However, sometimes it becomes necessary to utilize non-identical mechanical features in order to get electrically identical anodes.

Unlike their lower frequency counterparts, the terahertz chips need to be based on very thin and uniform GaAs substrates. This is important to eliminate substrate modes in the chip. The appropriate epilayers are grown by molecular beam epitaxy and an etch stop layer is grown to allow the substrate to be etched away. The completed chip is thus only a few micrometers thick ($<10 \mu\text{m}$). Such a delicate chip becomes difficult to handle and requires special precautions including placement of handling structures on the chip.

Finally, it is extremely important to design features on these chips that will allow one to package them in the appropriate circuit. All of the chips that have been described are made for split-block waveguide circuits, although the chip technology could easily lend it self to making quasi-optical structures with some minor modifications. The assembly of these devices in

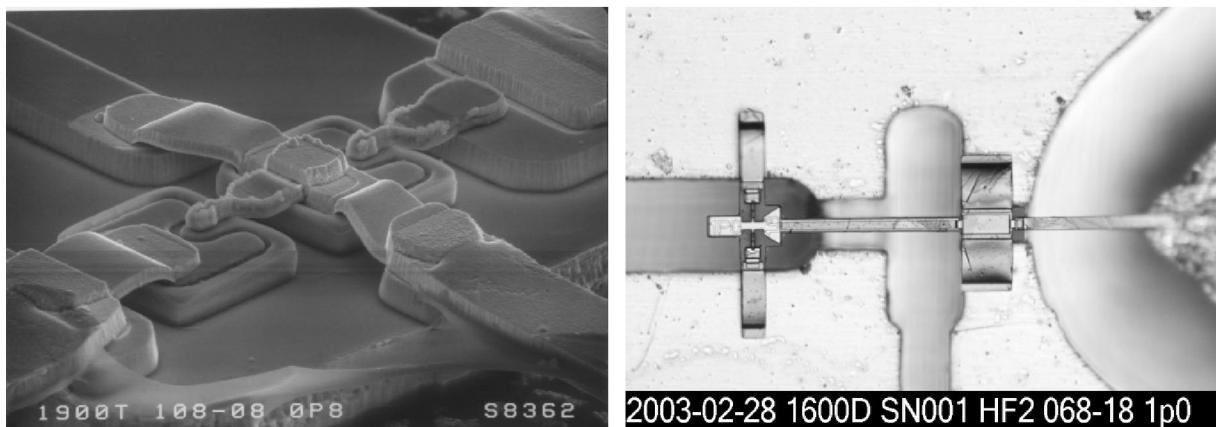


Figure 2: A close-up of a 1.9 THz tripler chip is shown in the left. The mesa is less than $15 \mu\text{m}$ long. The anodes are smaller than a square micrometer. A 1.6 THz doubler placed in the waveguide mount is shown on the right. The chip is only a few micrometers thick. Note the machined feature size of the output waveguide which is less than $50 \mu\text{m}$.

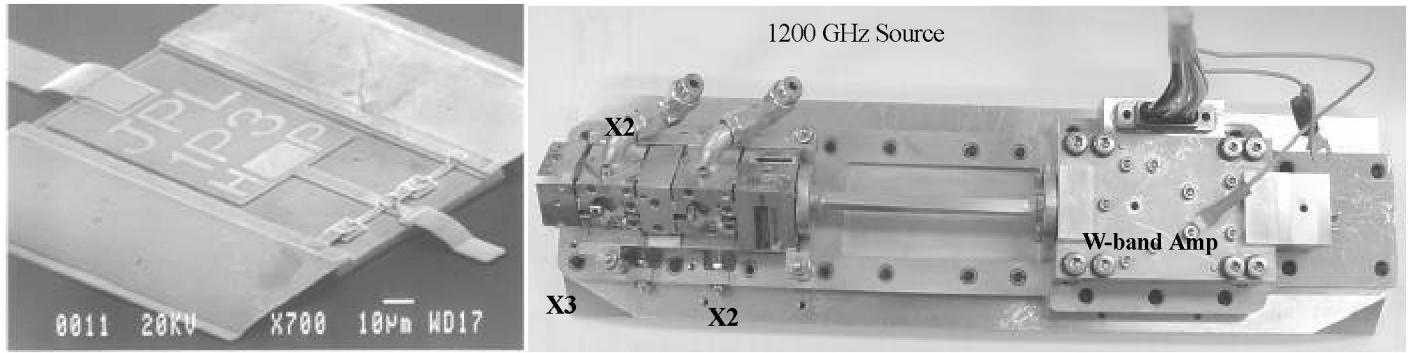


Figure 3: A 1200 GHz tripler chip is shown on the left. This chip is packaged in a waveguide block and tested as the last stage on the LO chain shown on the right. The chain on the right is driven by a 1-2 mW signal at W-band. Results from this chain are shown in Figure 4.

the waveguide blocks does not require solder or any other high temperature process. Instead, the chips are fabricated with ample beam-leads that are used both for handling purposes and for providing the DC and RF return. The devices are placed anode-side-up in the block, making it easy to visually inspect them. The diode processing details are described in [3].

III. STATE-OF-THE-ART PERFORMANCE

To test the terahertz multiplier circuits, it is important to have relatively high power sources at the input frequencies. A number of sources have been developed for this purpose and they have been detailed in previous publications [4-6]. In summary, we have sources that produce 30 mW at 200 GHz with 3dB bandwidths of 12%. Around 400 GHz we have sources that produce 5 mW with 10% bandwidths. We have sources at 600 GHz that produce over 1 mW across 15% bandwidths, and sources that produce several hundred microwatts up to 950 GHz. These sources are used to drive the terahertz multiplier circuits.

A 1200 GHz tripler chip is shown in Figure 3 (left). The chip is based on a balanced design with two anodes. The input E plane probe is shown on the left of the chip while the output probe is shown on the right. The chip is based on a few micrometers thick GaAs membrane and sits in a waveguide channel that is only 50 µm deep. The assembled LO chain to 1200 GHz is shown in Figure 3 (right). The amplifier module puts out about 100 mW across the 92-105 GHz band. This is followed by two doublers which are then used to drive the final stage tripler. At room temperature this multiplier chain can produce about 100 µW.

A 1.6 THz source was constructed from four cascaded frequency doublers. The 1.6 THz doubler was also fabricated on a few micrometer-thick GaAs membrane without a support frame. At these frequencies, mounting the device inside the waveguide block is complicated by the fragility of the device and the required high precision alignment. Similarly, the

tolerance on the machined blocks now becomes extremely important. Results obtained with chains consisting of four cascaded doublers have been presented in [7]. More recently, successful demonstrations of x2x3x3 cascaded chains to 1.9 THz have been made [8]. For cascaded chains, as has been shown before [8], cooling can provide a significant increase in output power since both the drive power and the diode efficiency are increased. In most cases the input power at W-band was limited to 100 mW. A summary of the achieved cryogenic performance is shown in Figure 4. Room temperature results with detailed descriptions from these sources have been presented previously [8,9,10].

IV. FUTURE CHALLENGES

The next challenge is to develop sources in the 2-3 THz range. This frequency range is of great importance to astrophysics. Devices working in this frequency range will push the fabrication technology to its limit, but they can be fabricated with existing technology. Quantum cascade lasers have shown significant improvement over a short period of time but they require cryogenic cooling and are inherently narrow-band sources. Finally, the next heterodyne space mission will probably utilize array detectors and thus it will be important to investigate LO sources that can be used to pump array mixers. Sources will also be needed for a variety of terahertz imaging applications. Power combining techniques will be needed to pump large-format array receivers as well as to provide high input power for stages working in the 2-3 THz range.

V. CONCLUSION

Planar Schottky-diode-based monolithic chips have been designed, fabricated and tested that provide a robust, compact and broad-band solution for terahertz sources. Though the primary application has been space-borne astrophysics missions, this technology can readily be adopted for multi-pixel imaging for both active as well as radiometric earth-based applications.

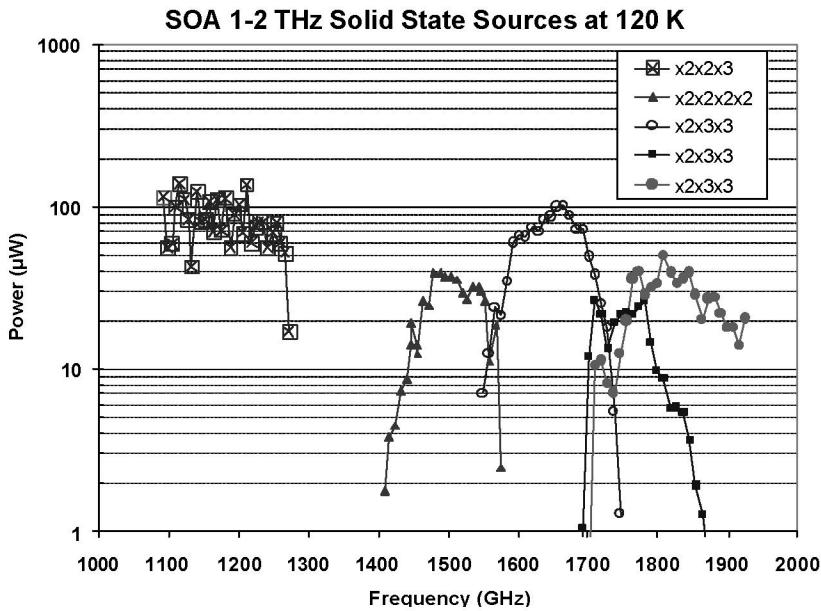


Figure 4: State-of-the-art (SOA) performance from available multiplied sources in the 1-2 THz range is shown. These data were obtained at 120 K. Power measurements at these frequencies require careful calibration and very specifically designed power meters.

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