Comparison on I-V Performances of Silicon PIN Diode towards Width Variations

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Abstract- **The performance of the PIN diode is very much depends on the chip geometry and the semiconductor material used, especially in the intrinsic region. The biasing voltage applied to the PIN diode determines the amount of holes and electrons injected into the intrinsic region and the values of its resistivity. This will give effect to the I-V performance of the PIN diode. This research studied the effects of width (and subsequently area) variations of intrinsic region of Silicon PIN diode on its I-V performance. The two dimensional structures and recipes of PIN diode are designed and simulated using Sentaurus TCAD tools. The thickness of PIN diode is kept at 40 µm while only the width is varied accordingly. Three variations of width have been chosen which are 90 µm, 80 µm, and 70 µm in order to study the impacts of width variation has on the I-V performance. Based on the simulation results, it is found that the current level is proportional to the PIN structure width.**

Keyword: PIN diode, width, I-V, Sentaurus.

I. INTRODUCTION

Semiconductor devices have played an important role in this present century for the betterment of human life in terms of cost and functionality. Generally, PIN diode is a semiconductor device commonly used in many electronic applications. PIN diode's name is attributed by its overall structure where *P* is representing P type layer, *I* is representing intrinsic layer and *N* is representing N type layer as shown in Fig. 1. The existence of intrinsic region makes it ideal for attenuator, fast switches and photo detectors. Hence, PIN diodes are used extensively in the microwave and RF application due to its ability to control the magnitude and phase of the signals [1,2]. Its exploitation as the switching element in the microwave and RF circuits is based on the difference of the characteristics of PIN diode at the forward and reverse bias condition [3].

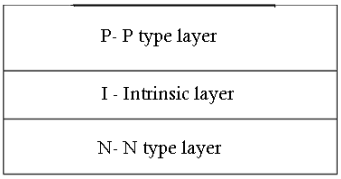

Fig. 1 PIN diode chip outline

For low frequency signals, the characteristic of PIN diode is similar to the standard PN diode. But for high frequency signals, there would not be enough time to turn off the diode. By increasing the dimension of intrinsic region, it will automatically increase the stored charges available and makes the diode to behave like a resistor. However, it will affect the turn off time and subsequently affecting the switching time.

Therefore, the work done in this research is to study the effect of the changes in I-region width on the I-V performance of Silicon PIN diode. The study is based on the two-dimensional structure of Silicon PIN diode. Three different width dimensions are selected to achieve the best comparison on the simulation result. The two-dimensional Silicon PIN diode's structure is drawn and simulated using Sentaurus TCAD to obtain the I-V characteristic of the device.

II. DEVICE STRUCTURE

The process in designing Silicon PIN diode model involves the usage of Sentaurus TCAD tools [4]. The first step is to draw the Silicon PIN diode structure based on the recipe using Sentaurus Structure Editor. The two dimensional structure of Silicon PIN diode is illustrated in Figure 2, where the structure is fully built using Silicon material. The *P* type region is doped with Boron with the concentration of $5x10^{14}/cm^3$ while the *N* type region is doped with Arsenic at $5x10^{19}/cm^3$ concentration. This leaves the middle region with the intrinsic element that acts in a similar manner as dielectric barrier between the two highly doped regions. The overall thickness is kept at 40µm and only the width is changed, therefore the area is also changed accordingly. Three different widths have been used to analyse the I-V performance, i.e. 90 µm, 80 µm and 70 µm.

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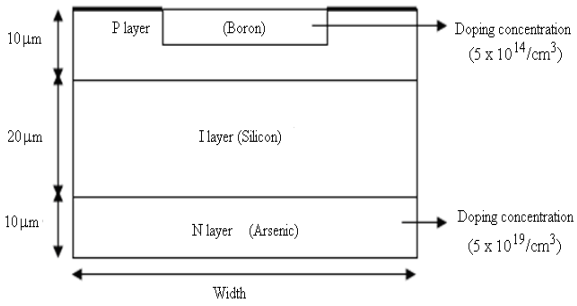

Fig. 2 Structure of Silicon PIN diode

Once the structure of PIN diode is done, then the device is simulated using the Sentaurus Device software. The model is simulated by setting up the resistance value at 1×10^{13} Ω. The simulation only considers the forward bias condition with the voltage level ranging from 0V to 10V.

III. Result and Discussion

Fig. 3 shows the simulated I-V characteristic of Silicon PIN diode for three different widths; 90 µm, 80 µm and 70 µm. Generally, the region of stored charge changes with the applied forward bias current [5]. These diodes start to operate (i.e. conducting current) when the voltage supply is above 1.7 V. For every different width of PIN diode, the current value is changed relative to the different value of voltage supply. From the result, it shows that the wider the width of Silicon PIN diode, the larger the current is for a given fixed value of voltage. The Silicon PIN diode with 70 µm width only provides current of 1.7 µA at a supply voltage of 10V while the Silicon PIN diode with 90 µm width provides current up to 4 µA at the same voltage supply.

Summary of the simulated result is tabulated in Table 1. Based on Fig. 3 and Table 1, the changes in current performance are non-linear with the changes in width. For the first 10 µm increment of width (from 70 µm to 80 µm), there is an increment of 1.3 µA (equivalent to 76.5 %) of current at voltage level of 10V. Whereas the second 10 µm increment of width (from 80 µm to 90 µm), the increment of current at voltage level of 10 V is only 1 µA (equivalent to 33.3 %).

Through the simulation of width variation of Silicon PIN diode, it is shown that the current performance is directly proportional to the width. Then, these results are compared with the calculations in P-N junction as the intrinsic region behaves in a similar manner as the depletion region for a better comparison [6]. For the calculation part, the bias voltage is set to 0.3 V. This is because the electrical behaviour of P-N junction is not linear with the bias voltage.

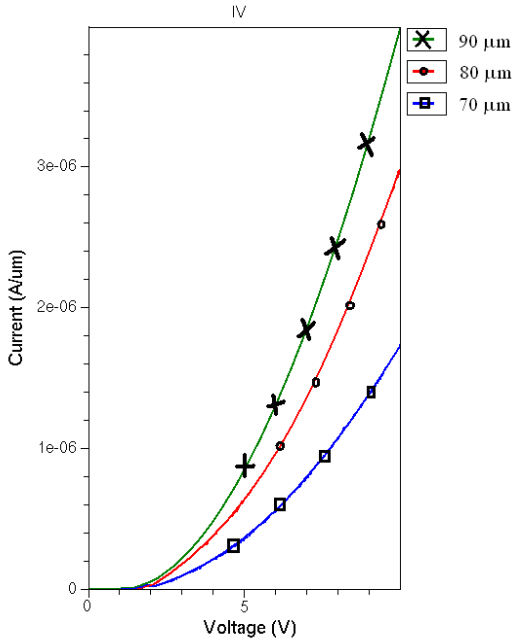

Fig.3 Simulated I-V performance of Silicon PIN diode with width variation

TABLE I
Summary of I-V Performance of Different Width of Silicon Pin Diode at Voltage Supply of 10 V

Width (µm)	Current (µA)	Difference in current increment (µA)
70	1.7	-
80	3.0	1.3
90	4.0	1.0

The prefactor to the current, I_0 for each area (i.e. width × thickness) is calculated based on (1):

$$I_0 = eA\left(\frac{D_p p_n}{L_p} + \frac{D_n n_p}{L_n}\right) \qquad (1)$$

where e is electron charge, A is area, D_p and D_n are hole and electron diffusion coefficient, respectively. p_n and n_p are the minority charge density for P side and N side of the junction, respectively. While L_p and L_n are diffusion length for holes and electron respectively.

The prefactor to the generation-recombination current is given by (2):

$$I_{0GR} = \frac{eAWn_i}{2\tau} \qquad (2)$$

where W is width, n_i is constant minority charge density value of Silicon and τ is the carrier lifetime in the depletion region.

Therefore, the total current is represented by (3) :

$$I = I_0\left[\exp\left(\frac{eV}{k_BT}\right)-1\right]+I_{GR}^{0}\left[\exp\left(\frac{eV}{2k_BT}\right)-1\right] \quad (3)$$

where V is bias voltage, k_B is Boltzmann's constant and T is a temperature.

By using all the equations above, the currents for different width are calculated based on the bias voltage of 0.3 V and the temperature is set to 300 K. The results are summarised in Table 2.

TABLE II
VALUES OF CURRENT (FROM CALCULATION) FOR DIFFERENT WIDTH OF SILICON PIN DIODE AT BIAS VOLTAGE OF 0.3 V

Width (μm)	Current (μA)
70	4.2914
80	4.9044
90	5.5175

From Table 2, it shows that for every 10 μm increment of width, the current performance is also increased by 0.613 μA at the bias voltage of 0.3 V. Here, the current performance is dominated by generation-recombination process [6].

Fig. 4 shows the comparison in terms of calculated and simulated currents' performance relative to the difference in width. The current value is seen increases as the width of Silicon PIN diode increases for both, simulation and calculation. However, please note that the bias voltage used for calculation is 0.3 V whereas the bias voltage of interest for simulation is 10 V. Thus, it proves that the current performance is directly proportional with the width of Silicon PIN diode.

IV. CONCLUSION

In this study, in order to observe the width's effect on the I-V performance, the two-dimensional silicon PIN diode with varying width has been simulated using the Sentaurus TCAD tools. Through the simulations, the current performance is directly proportional with width of silicon PIN diode. This is also proven through the calculation by adopting the method used in finding the current at P-N junction [6]. In general, a larger PIN diode has a better I-V performance due to the larger number of carrier available. However, the switching or turn off time will also be increasing. Thus, to optimise the performance of a system, the silicon PIN diode needs to be customised to suit its application. Efforts to reduce the size of PIN diode are still continuing, with the aim to further improve current drive.

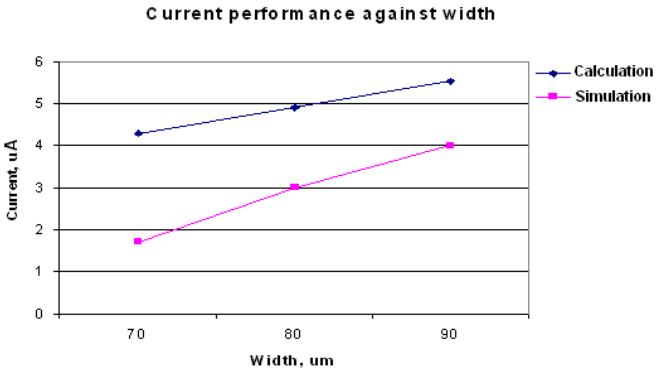

Fig. 4 Comparison of current performance between simulation and calculation

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