

ELG 6369

NONLINEAR MICROWAVE DEVICES AND EFFECTS

CHAPTER VI

MICROWAVE OSCILLATORS

A – INTRODUCTION

Oscillators are the bases of electronic systems. Signal generation is essential to electronics: in communication (carrier signals for modulation), in system conversions (periodic sweep signals for voltage-frequency conversion), in mixing (frequency conversion), in display units (signals for display circuits), in signal processing (PLLs), etc. Moreover, with the advent of modern radio systems came the need to provide stable harmonic oscillators.

What makes the design of oscillators such a difficult task is that the designer exploits a nonlinear circuit behavior using linear system tools. With such constraints, the active device model has to handle the complicated feedback mechanism. Moreover, since an oscillator has to provide power to subsequent circuits, frequency-dependent output loading plays an important role. It is for these reasons that the design of oscillators remains more an art than an exact engineering design task.

I – Definition and classification

Oscillators can be classified as crystal, RC, LC, relaxation, ring, and distributed oscillators (Figure VI-1).

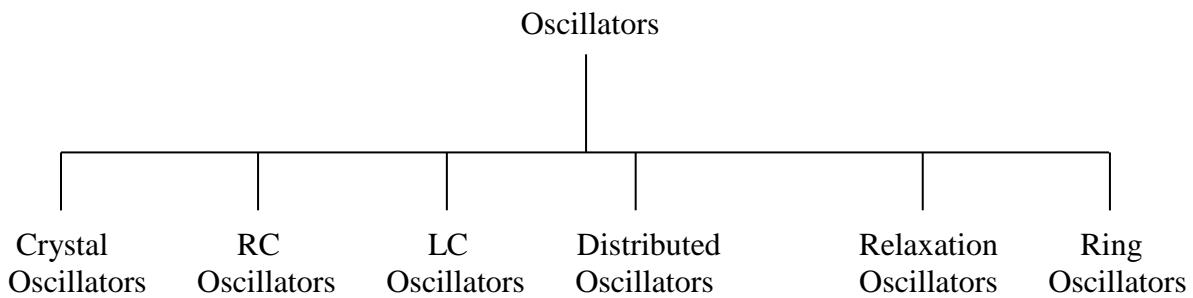


Fig. VI-1. Oscillator classification

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An oscillator is a network that is able to generate an output periodic signal without using a periodic input excitation. In other words, an oscillator can be viewed as a dc to ac converter. The principle of an oscillator topology can be explained in terms of a feedback circuit as shown in Figure VI-2.

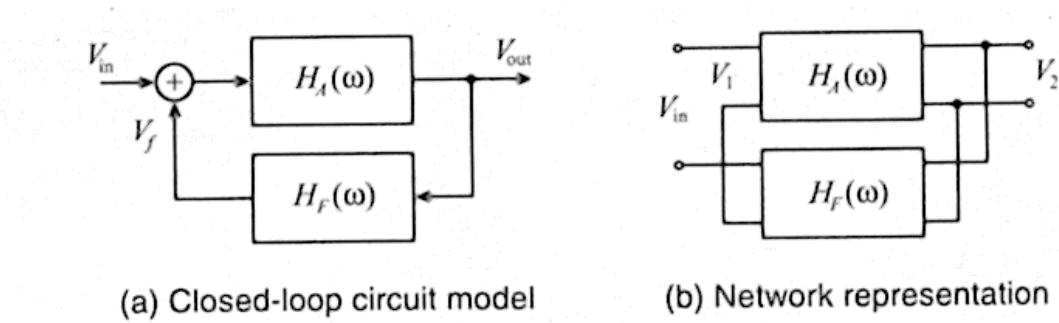


Fig. VI-2. Feedback oscillator.

In this figure, an oscillator can be viewed as a loop that causes a positive feedback at a selected frequency. Figure VI-2-a illustrates the generic closed-loop system representation, while Figure VI-2-b provides a two-port network description.

II –Constraints imposed for oscillation

The mathematical condition for a circuit to oscillate can be established based on the closed-loop transfer function:

$$H_{CL}(\omega) = \frac{V_{out}}{V_{in}} = \frac{H_A(\omega)}{1 - H_F(\omega)H_A(\omega)} \quad (\text{VI-1})$$

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where $H_A(\omega)$ and $H_F(\omega)$ are the transfer function of the amplifier stage and the feedback stage respectively.

Since there is no input ($V_{in} = 0$), we obtain the Barkhausen criterion:

$$H_F(\omega)H_A(\omega)=1 \quad (\text{VI-2})$$

If the feedback transfer function $H_F(\omega)$ is written as a complex quantity, that is

$$H_F(\omega) = H_{Fr}(\omega) + j H_{Fi}(\omega) \quad (\text{VI-3})$$

and the amplifier transfer function possesses a real valued gain,

$$H_A(\omega) = H_{Ao}(\omega) \quad (\text{VI-4})$$

we can re-express equation (VI-2) as

$$H_{Ao}(\omega) = \frac{1}{H_{Fr}(\omega)} \quad (\text{VI-5-a})$$

$$H_{Fi}(\omega) = 0 \quad (\text{VI-5-b})$$

These conditions, called *the conditions of oscillation and stability*, apply only for a steady-state situation. Initially, we have to require that $\{ H_{Ao}(\omega) * H_{Fr}(\omega) > 1 \}$ (for an increasing output voltage). However, the voltage must reach a steady state (amplitude must stabilize).

This nonlinear behavior can be explained using the gain characteristic shown in Figure VI-3. A negative slope of the curve is needed to ensure a decrease in gain for increasing voltage. At point $|V_{out}| = V_Q$, for $H_{Ao}(\omega) = H_Q(\omega) = H_{Fr}(\omega)$, the stable operating point is reached.

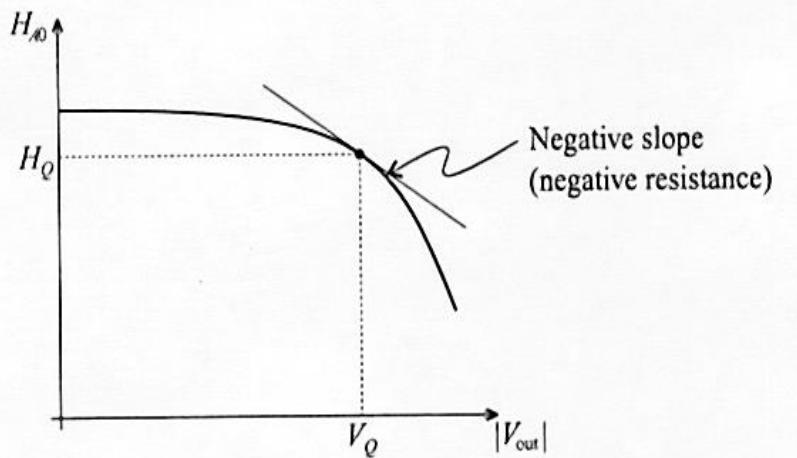


Fig. VI-3. Output voltage versus gain characteristic.

An oscillator generates a periodic output. As such, the circuit must entail a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal. A self-sustaining mechanism arises at the frequency s_o if the transfer function $H(s_o) = 1$, and the oscillation amplitude remains constant if s_o is purely imaginary, i.e.,

$$H(s_o = j\omega_o) = 1 \quad (\text{VI-6})$$

Thus, for steady oscillation, the two conditions must be simultaneously met at ω_o :

- The loop gain, $|H(j\omega_o)|$ must be equal to unity (condition of oscillation),

- The total phase shift around the loop, $\angle H(j\omega_0)$ must be equal to zero or 180° if the dc feedback is negative (condition of stability).

These oscillation criteria can be expressed in terms of negative resistance provided by a diode (e.g., Tunnel diode) or an unstable transistor (Figure VI-4).

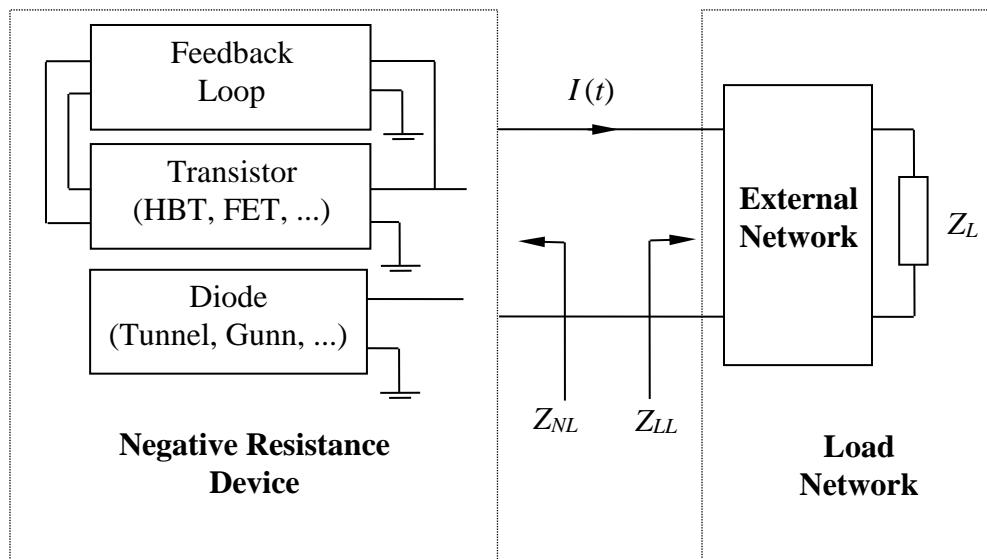


Fig. VI-4. Block diagram of an oscillator.

III –Condition of oscillation

The approach proposed by Kurokawa is usually used to define the first condition. The oscillator is equivalent to a nonlinear impedance Z_{NL} in series with a load impedance Z_{LL} that represents the load network, constituted by the load impedance Z_L and external sub-networks (buffers, resonators, etc.).

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If the current flowing the oscillator is sinusoidal, { $i(t) = I_o \cos(\omega_o t)$ }, we have

$$[Z_{LL}(\omega_o) + Z_{NL}(I_o, \omega_o)]I_o = 0 \quad (\text{VI-7})$$

By defining

$$Z_T = Z_{LL}(\omega_o) + Z_{NL}(I_o, \omega_o) = R_T + jX_T \quad (\text{VI-8})$$

we have for a nonzero current

$$R_T(I_o, \omega_o) = 0 \quad \text{and} \quad X_T(I_o, \omega_o) = 0 \quad (\text{VI-9})$$

Since the load network has a positive real part, the one of Z_{NL} should be negative. This condition can be expressed in terms of reflection coefficients Γ_{NL} and Γ_{LL} of Z_{NL} and Z_{LL} respectively (Fig. VI-5)

$$\begin{aligned} R_{NL} &= -R_{LL} \quad \text{and} \quad j(X_{NL} + X_{LL}) = 0 \\ \Rightarrow \Gamma_{NL} \cdot \Gamma_{LL} &= 1 \end{aligned} \quad (\text{VI-10})$$

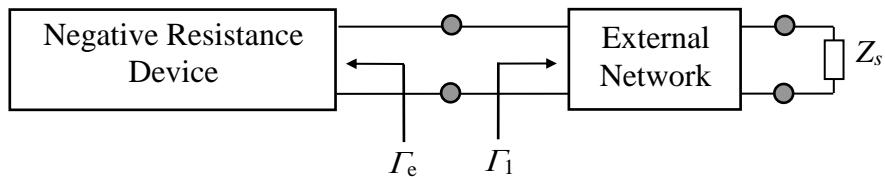


Fig. VI-5. Equivalent circuit for the condition of oscillation.

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This condition can be generalized to an N-port component. Let $[S]$ and $[S']$ be the scattering matrices of the active device (negative resistance device) and the embedded network (external network) respectively. By connecting these two networks, we obtain

$$\begin{aligned} [\mathbf{b}'] &= [\mathbf{a}] \quad \text{and} \quad [\mathbf{b}] = [\mathbf{a}'] \\ \Rightarrow \quad & \{[S][S'] - [\mathfrak{I}]\}[\mathbf{a}'] = [\mathbf{0}] \end{aligned} \tag{VI-11}$$

where $[\mathfrak{I}]$ and $[\mathbf{0}]$ refer respectively to the identity and unity matrices. Since the incident wave matrix $[\mathbf{a}']$ is not zero, the generalized condition of oscillation can be expressed

$$\det \{[S][S'] - [\mathfrak{I}]\} = 0 \tag{VI-12}$$

Or, by using impedance matrices

$$\det \{[\mathbf{Z}] + [\mathbf{Z}']\} = 0 \tag{VI-13}$$

IV –Condition of sustaining or stability

Once the oscillations are started, the generated signal must be sustained. To evaluate this concept, let us apply a small perturbation to the magnitude I_o of the current and to the complex pulsation $\{s_o = j \omega_o\}$. Expanding the impedance Z_T in Taylor series up to the first order around the point (I_o, ω_o) allows obtaining the following relation

$$Z_T \Rightarrow Z_T(I_o, \omega_o) + \frac{\partial Z_T}{\partial p} \partial p + \frac{\partial Z_T}{\partial I} \partial I_o \tag{VI-14}$$

Since Z_T must be zero, therefore, by decomposing ∂Z_T in real and imaginary parts, we can demonstrate that the oscillator is stable if the sinusoidal voltage or current returns to its steady-state value after it is perturbed. Kurokawa gives another condition for stable oscillation: in term of impedance, the condition is

$$\frac{\partial R_T}{\partial I} \frac{\partial X_T}{\partial \omega} - \frac{\partial X_T}{\partial I} \frac{\partial R_T}{\partial \omega} > 0 \quad (\text{VI-15})$$

This is the condition of stability around the point $(I_o, j\omega_o)$.

V –Condition of maximum efficiency

The impedance $Z_{NL}(I_o, \omega_o)$ can deliver a power defined by

$$P_{osc} = \frac{1}{2} Re(Z_{NL}) I_o^2 = \frac{1}{2} R_{NL}(I_o, \omega_o) I_o^2 \quad (\text{VI-16})$$

which maximal value is given by

$$\begin{aligned} \frac{\partial P_{osc}}{\partial I_o} &= \frac{1}{2} \frac{\partial \{R_{NL}(I_o, \omega_o) I_o^2\}}{\partial I_o} = 0 \\ \Rightarrow \quad \frac{\partial R_{NL}}{\partial I_o} &= \frac{2 R_{NL}}{I_o} \end{aligned} \quad (\text{VI-17})$$

B – OSCILLATOR ANALYSIS

Existing techniques for oscillator analysis can be classified as time- or frequency-domain methods. Since almost all the experimental equipment display data in the frequency domain (S-parameters), it is more convenient to use frequency-domain methods to analyze oscillators.

Today, three approaches can be used. The first is based on measured S-parameters to deduce the conditions of oscillation. The second use measurements to analytically or numerically determine the voltages across the active device that assures maximum output power. The last approach calculates the embedded network (external network).

Designers using CAD tools focus on the two last methods, since the first one is mainly experimental.

I- Analysis by the transistor S-parameters

Let $[S]$ be the S matrix of the active device. Thus the external network will be described by the inverse matrix $[S^{-1}]$. Once we measure the reflection coefficient S_{11} and the transmission coefficient S_{21} (for a given frequency), the incident power a_1 is tuned in order to maximize the device efficiency.

Accordingly, the unknown power a_2 must be minimized to assure an optimum efficiency. Let A be the gain defined as

$$A = \frac{b_2}{a_1} \quad \Rightarrow \quad a_2 = \frac{A - S_{21}}{S_{22}} a_1 \quad (\text{VI-18})$$

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Therefore, the optimum value is equal to

$$A_{opt} = \frac{1}{|S_{22}|^2 + |S_{12}|^2 - 1} \left(|S_{12}|^2 S_{21} - S_{21} - S_{22} S_{11} S_{12}^* \right) \quad (\text{VI-19})$$

The following steps can summarize this process:

- Choose a convenient range for a_1 .
- Fix a value for a_1 and measure S_{11} and S_{21} . Then, estimate a_2 to obtain S_{12} and S_{22} .
- Determine A_{opt} , deduce the ratio a_2/a_1 , then a_2 (these two quantities are independent of the reference planes). Therefore, the output parameters S_{12} and S_{22} can be obtained as well as the optimum output power.
- Vary a_1 . A curve of the optimum output power versus the incident power can be plotted.
- Select the value of a_1 that gives the highest output power. Note the corresponding a_2 in order to determine the external network.

The main limitation is in the assumption that S_{11} and S_{21} depend only of the incident power a_1 (and similarly for S_{22} and S_{12} versus a_2). This could lead to significant errors for some power devices.

II- Analysis by currents and voltages

In this approach and based on the application, the transistor is modeled by either a linear or a nonlinear circuit. The purpose is to determine the currents and voltages at the output that assure an optimum output power.

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For the general case (nonlinear), the transistor is equivalent to multifrequency P -port network (\mathbf{R} in Figure VI-6). Let \mathbf{R}' be a passive linear network connected to \mathbf{R} and defined by the impedance matrix $[\mathbf{Z}']$. The steady state behavior of the nonlinear network will not change if the impedance matrix $[\mathbf{Z}']$ satisfies the relation

$$[\mathbf{Z}'^k] [\mathbf{I}^k]^t = [\mathbf{V}^k]^t \quad k = 1, \dots, M \quad (\text{VI-20})$$

or

$$[\mathbf{Z}'^k] [\mathbf{I}_1^k \ \dots \ \mathbf{I}_P^k]^t = [\mathbf{V}_1^k \ \dots \ \mathbf{V}_P^k]^t \quad k = 1, \dots, M \quad (\text{VI-21})$$

where k represents the k th harmonic. $[\mathbf{I}^k]$ and $[\mathbf{V}^k]$ are respectively the current and voltage vectors of the network \mathbf{R} for the harmonic k .

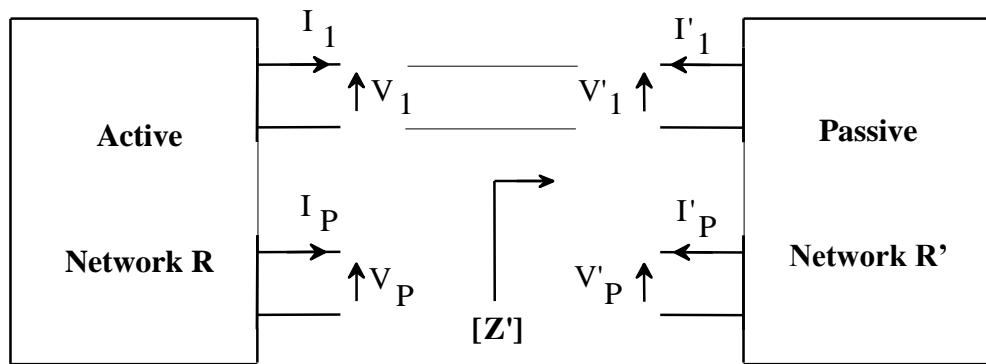


Fig. VI-6. Interconnection between the active device \mathbf{R} and the passive network \mathbf{R}' .

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Therefore, for a given port j , the elements of those vectors are the Fourier coefficients at pulsation ω

$$V_j(t) = \sum_{k=0}^M V_j^k e^{jk\omega t} \quad (\text{VI-22})$$

$$I_j(t) = \sum_{k=0}^M I_j^k e^{jk\omega t} \quad (\text{VI-23})$$

Now, for P external ports, $[\mathbf{Z}]$ could be expended in the following format

$$\begin{bmatrix} [\mathbf{Z}_P] & [\mathbf{Z}_{NP}] \\ [\mathbf{Z}_{PN}] & [\mathbf{Z}_N] \end{bmatrix} \begin{bmatrix} [\mathbf{I}_P] \\ [\mathbf{I}_N] \end{bmatrix} = \begin{bmatrix} [\mathbf{V}_P] \\ [\mathbf{V}_N] \end{bmatrix} \quad (\text{VI-24})$$

where the sub-matrices $\{ [\mathbf{Z}_{NP}], [\mathbf{Z}_{PN}], [\mathbf{Z}_N] \}$, $[\mathbf{I}_N]$ and $[\mathbf{V}_N]$ refer to network \mathbf{R} .

Since $[\mathbf{Z}']$ does not affect the internal impedance sub-matrices $[\mathbf{Z}_{NP}]$, $[\mathbf{Z}_{PN}]$ and $[\mathbf{Z}_N]$, the circuit equation becomes

$$\begin{bmatrix} [\mathbf{Z}_P] + [\mathbf{Z}'_P] & [\mathbf{Z}_{NP}] \\ [\mathbf{Z}_{PN}] & [\mathbf{Z}_N] \end{bmatrix} \begin{bmatrix} [\mathbf{I}_P] \\ [\mathbf{I}_N] \end{bmatrix} = \begin{bmatrix} [\mathbf{V}'_P] \\ [\mathbf{V}_N] \end{bmatrix} \quad (\text{VI-25})$$

where the éléments of $[\mathbf{V}'_P]$ are the voltages across network \mathbf{R}' . With respect to phase difference between voltages in order to maintain oscillations, an optimization of their values gives the optimum passive network equivalent impedance at all ports. The process consists to maximize the transistor output power by varying the voltages.

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Once the optimum voltages are determined, we have to synthesize the passive network. In Figure VI-5, the feedback loop could be shown as a two-port network, which can be modeled by either a Pi-type network or a T-type network (as shown in Figure VI-7).

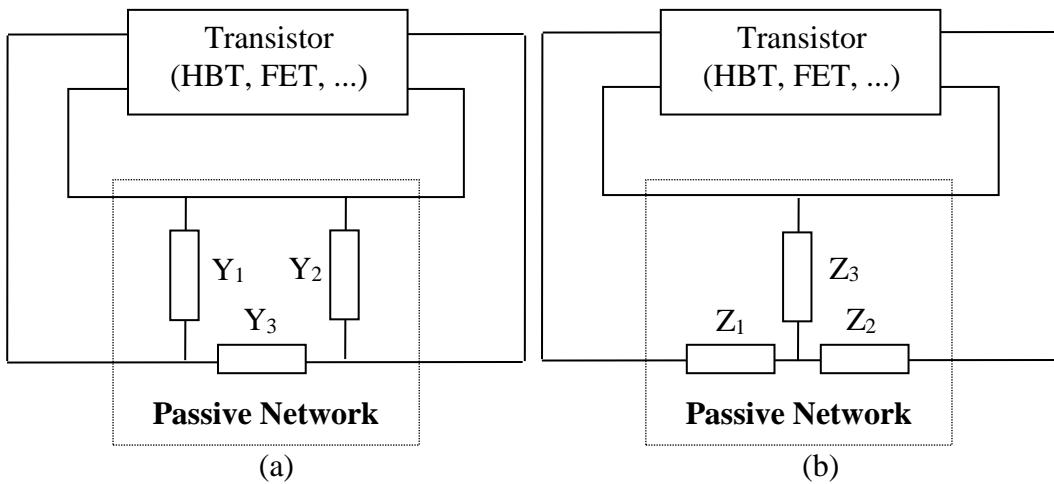


Fig. VI-7. Feedback circuits with Pi- and T-type feedback loops.

(a) Pi-type Network, (b) T-type Network

Therefore, since the passive network topology can be fully defined, the elements of the passive network (impedances or admittances) are obtained by solving a system of equations for each harmonic based on Kirchoff laws (e.g., using the harmonic balance technique).

III- Analysis by Z or Y parameters

This analysis consists on two steps. In the first, we measure the transistor small-signal S-parameters. In the second, we use optimization software to vary the most important nonlinear elements in order to come up with new large-signal S-parameters.

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Then, by varying the gain, the saturation point could be obtained. This is the point for which the power added efficiency (PAE) is maximum. PAE corresponds to the maximum output power for the oscillator.

Usually, the oscillator configuration highlights three unknown impedances or admittances (Figure VI-7-a or -b)

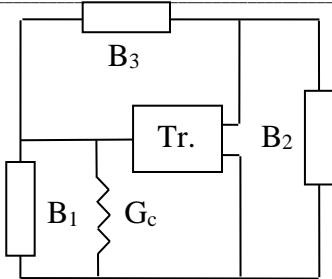
$$\{ Z_1, Z_2, Z_3 \}$$

or

$$\{ Y_1, Y_2, Y_3 \}$$

represented as " $R_i + jX_i$ " or " $G_i + jB_i$ ". Two of them are purely reactive and the real part of the third is equal to the oscillator load R_c .

Figure VI-8 shows the three alternatives for the Pi-type, while Figure VI-9 regroups the three alternatives for the T-type passive network.

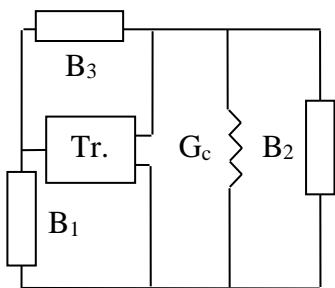


$$G_c = C_1 + A_r C_3 + A_i C_4$$

$$B_1 = C_2 + (1 - A_r)(C_4 + C_3 A_r / A_i)$$

$$B_2 = C_3 (A_r - 1) / A_i + C_4$$

$$B_3 = -C_3 A_r / A_i - C_4$$

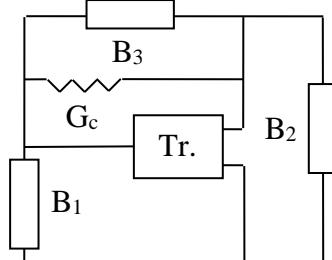


$$G_c = (C_1 + A_r C_3 + A_i C_4) / |A|^2$$

$$B_1 = C_1 (A_r - 1) / A_i + C_2$$

$$B_2 = \left(C_1 (A_r - |A|^2) / A_i + A_r C_4 - A_i C_3 \right) / |A|^2$$

$$B_3 = C_r / A_i$$



$$G_c = (C_1 + A_r C_3 + A_i C_4) / |A - 1|^2$$

$$B_1 = (C_1 + C_3) A_r / A_i + C_2 + C_4$$

$$B_2 = -(C_1 + C_3) / A_i$$

$$B_3 = (C_1 - (1 - A_r) G_c) / A_i$$

$$C_1 = -Re(Y_{11} + AY_{12})$$

$$C_3 = -Re(Y_{21} + AY_{22})$$

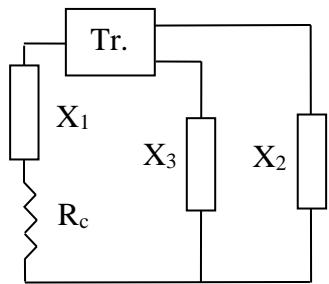
$$A = A_r + jA_i = -\left(Y_{21} + Y_{12}^*\right) / 2Re(Y_{22})$$

$$C_2 = -\text{Im}(Y_{11} + AY_{12})$$

$$C_4 = -\text{Im}(Y_{21} + AY_{22})$$

Fig. VI-8. Oscillator topology for the Pi-type passive network and optimal relations for the three admittances (Tr. = Transistor).

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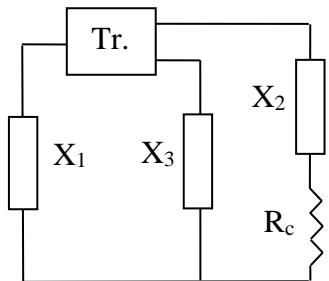


$$R_c = D_1 + F_r D_3 + F_i D_4$$

$$X_1 = D_2 - (1 + F_r)(D_4 + D_3 F_r / F_i)$$

$$X_2 = -D_3(1 + F_r) / F_i - D_4$$

$$X_3 = D_3 F_r / F_i + D_4$$

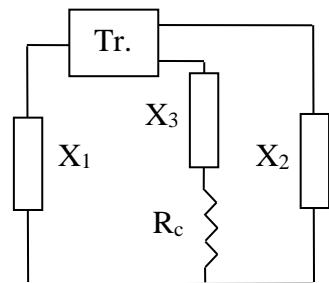


$$R_c = (D_1 + F_r D_3 + F_i D_4) / |F|^2$$

$$X_1 = D_1(1 + F_r) / F_i + D_2$$

$$X_2 = \left(D_1(F_r + |F|^2) / F_i + F_r D_4 - F_i D_3 \right) / |F|^2$$

$$X_3 = -D_1 / F_i$$



$$R_c = (D_1 + F_r D_3 + F_i D_4) / |1 + F|^2$$

$$X_1 = (D_1 - D_3) F_r / F_i + D_2 - D_4$$

$$X_2 = (D_1 - D_3) / F_i$$

$$X_3 = \frac{((1 + F_r)(D_4 - (D_1 - D_3) F_r / F_i) - F_i D_1)}{|1 + F|^2}$$

$$D_1 = -\text{Re}(Z_{11} + F Z_{12})$$

$$D_2 = -\text{Im}(Z_{11} + F Z_{12})$$

$$D_3 = -\text{Re}(Z_{21} + F Z_{22})$$

$$D_4 = -\text{Im}(Z_{21} + F Z_{22})$$

$$F = F_r + jF_i = (Z_{21} - A Z_{11}) / (A Z_{12} - Z_{22})$$

Fig. VI-9. Oscillator topology for the T-type passive network and optimal relations for the three impedances (Tr. = Transistor).

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IV- Practical aspects of VCO design

For wideband VCOs, the common-gate configuration is a popular choice. The reason for its importance is that we can achieve negative conductance over a wide frequency range by using a very simple feedback circuit (e.g., a single inductor). For the same reason, the common-base circuit is favored for realizing bipolar-transistor VCOs. Other circuit topologies are used for other types of oscillators.

F – HARMONIC OSCILLATORS

I – Introduction

Harmonic oscillators are components where one single device (the active component) functions both as a fundamental frequency oscillator and as a harmonic generator. These components deserve special attention due to their capability of generating RF power above the frequencies usually obtained from fundamental frequency oscillator. Their design requires simultaneous application of oscillator theory and frequency multiplier theory, in order to obtain a component with a reasonable performance in output power, bandwidth, and phase noise.

One can start by considering the dynamic balance of power in a microwave amplifier, depicted in Figure VI-10.

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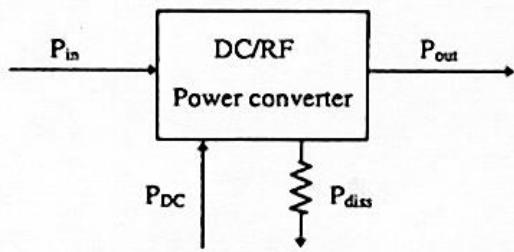


Fig. VI-10. Power representation of an amplifier

The amplifier can be seen as a DC/RF power converter, with

$$P_{in} + P_{dc} = P_{out} + P_{diss} \quad (\text{VI-26})$$

This equation can be modified to include the amplifier power gain, G , and the RF power added by the amplifier P_{ad} ,

$$P_{diss} = P_{dc} - (P_{out} - P_{in}) = P_{dc} - (G - 1)P_{in} \quad (\text{VI-27})$$

with

$$P_{ad} = P_{out} - P_{in} \quad (\text{VI-28})$$

Since the dc power is assuming to remain constant (current source), equation (VI-27) shows that under large-signal drive, the amplifier gain G has to decrease (no negative dissipated power). Applied to oscillators, the situation is similar; part of the drain energy is fed back to the gate through a coupling network in order to sustain oscillations (Figure VI-11).

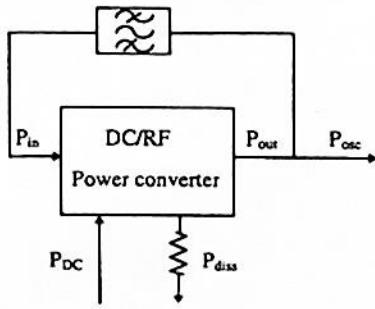


Fig. VI-11. Power representation of an oscillator.

The power balance for the oscillator is also similar to the amplifier case and can be rearranged in the following form

$$P_{osc} = P_{out} - P_{in} = P_{dc} - P_{diss} \quad (\text{VI-29})$$

where P_{osc} represents the power delivered to the load. Conventional oscillator theory states that the maximum available power from an oscillator is equal to the added power from an amplifier at the point of maximum efficiency (i.e., when the difference between P_{out} and P_{in} is maximum).

Thus,

$$P_{osc\ max} = P_{ad} = \max(P_{out} - P_{in}) \quad (\text{VI-30})$$

Note: The harmonic oscillator configuration is the same as in Figure VI-11, with the addition of a harmonic filter at the output.

For a harmonic oscillator, the output power comprises fundamental frequency power, P_{of} , plus harmonic power P_{oh} .

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Equation (VI-29) is then transformed to

$$P_{hosc} = (P_{of} - P_{in}) + P_{oh} = (P_{oh} - P_{in}) + P_{of} \quad (\text{VI-31})$$

This equation shows that an optimum harmonic oscillator should generate power at the fundamental frequency just enough to sustain oscillations, most of the output power should be delivered to the external load and the difference will be dissipated in the other harmonics. Now the condition (VI-44) becomes

$$P_{hosc\ max} = \max(P_{oh} - P_{in}) + P_{of} \quad (\text{VI-32})$$

II – Design approach

The design of harmonic oscillators starts with the design of a frequency multiplier. The objectives of a frequency multiplier are a maximum output power at the desired harmonic, a matched input for maximum efficiency, and a reasonable frequency bandwidth.

For harmonic oscillation operation, the multiplier's saturation characteristics are also required, which can be obtained from experimental measurements or through nonlinear simulation as

$$P_{oh}(P_{in}, n\omega_o) - P_{in}(\omega_o) = f[P_{in}(\omega_o)] \quad (\text{VI-33})$$

An illustration of such characteristics is presented in Figure VI-12, for a 5 to 10 GHz frequency doubler. One can observe a nonlinear relation between output power and input drive at low levels, and a saturation of the second harmonic output power after a certain input drive level.

The added power is maximized at the peak of the curve obtained for

- A matched input that maximize the gate voltage swing, a shorted load
- A shorted load for the fundamental frequency maximizing the drain current
- And a matched second harmonic drain impedance.

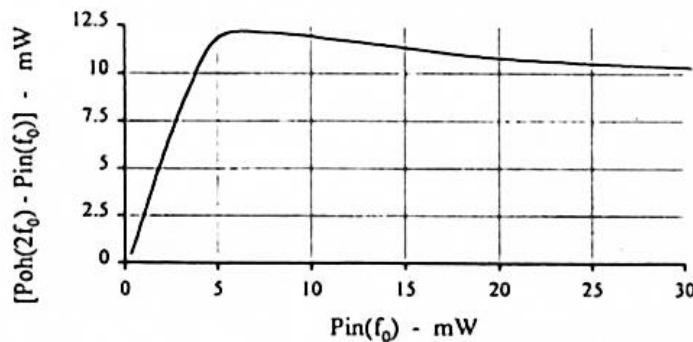


Fig. VI-12. Saturation characteristics of a frequency multiplier.

In the case of harmonic oscillators, equation (VI-32) has to be taken into consideration, where the frequency multiplier is modified to include generation of power at the fundamental frequency enough to sustain oscillations, i.e.,

$$P_{out}(P_{in}, n\omega_o) = P_{in}(\omega_o) \quad (\text{VI-34})$$

Therefore, the drain current has to be modified so that the drain power at the fundamental frequency is equal to the power absorbed by the gate.

A procedure for the design of the drain impedance at the fundamental frequency is to monitor both the gate and drain power at each iteration, using

$$P_{av} = \operatorname{Re} \left(\frac{V(\omega)I(\omega)^*}{2} \right) \quad (\text{VI-35})$$

The nonlinear analysis will provide a set of voltages and currents at the fundamental frequency and its harmonics, which can be used to generate the feedback network. The currents in the multiplier are obtained using the receptor convention (currents are defined entering at gate and drain ports). They must be modified to the generator condition, where they leave the gate and drain ports, as depicted in Figure VI-13.

The next step is to insert the device and associated currents and voltages into any of the standard oscillator coupling topologies available (either T- or P-types illustrated in Figures VI-14-a and VI-14-b). As we already described, three options are possible for each topology, with the load connected either to the drain, the gate, or the source. ***The connection of the load to the drain or source provides more power compared to the gate connection.*** The reason for higher power is due to the higher voltage and current available on the output plane.

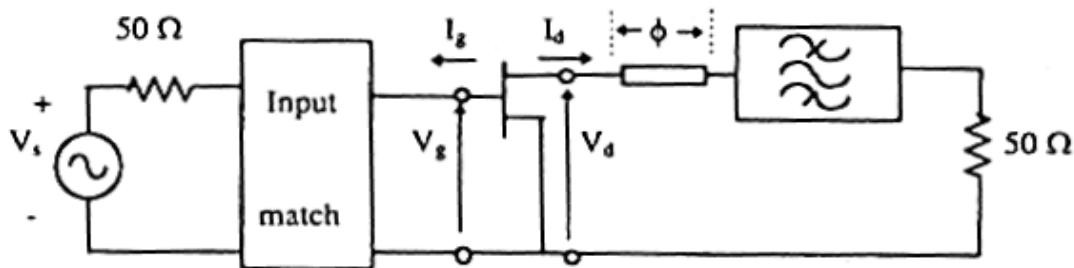


Fig. VI-13. Doubler circuit for harmonic oscillator design.

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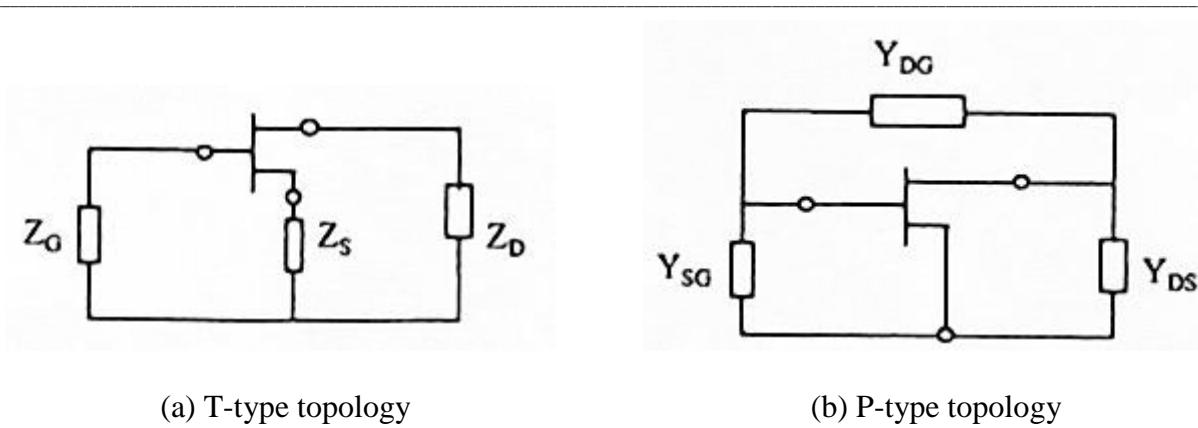


Fig. VI-14. Topology for the harmonic oscillator.

If the dc power requires grounding the source, then there is only one choice. In the case of low power oscillators, there is no preferred connection other than layout convenience. The terminations reported in Table VI-1 are for the fundamental frequency and output harmonic for the t-type topology.

The boundary current-voltage conditions have to be valid simultaneously at the fundamental frequency and at the harmonics. The set of harmonic impedances from Table VI-1 is preferred where the source impedance is shorted to ground. Table VI-2 gives the set of terminations for the P topology.

The equations required calculating the network elements as a function of currents and voltages at the fundamental frequency are in table VI-3 and VI-4.

Table VI-1. Network elements for the T topology.

Fundamental Frequency Impedances	Output Harmonic Frequency Impedances
$Z_D(\omega_0) = R_{D1} + jX_{D1}$	$Z_D(n\omega_0) = R_{Dn} + jX_{Dn}$
$Z_S(\omega_0) = jX_{S1}$	$Z_S(n\omega_0) = 0$
$Z_G(\omega_0) = jX_{G1}$	$Z_G(n\omega_0) = R_{Gn} + jX_{Gn}$

Table VI-2. Network elements for the P topology.

Fundamental Frequency Admittance	Output Harmonic Frequency Admittance
$Y_{DS}(\omega_0) = G_{DS1} + jB_{DS1}$	$Y_{DS}(n\omega_0) = G_{DSn} + jB_{DSn}$
$Y_{GS}(\omega_0) = jB_{GS1}$	$Y_{GS}(n\omega_0) = G_{GSn} + jB_{GSn}$
$Y_{DG}(\omega_0) = jB_{DG1}$	$Y_{DG}(n\omega_0) = 0$

Table VI-3. T configuration: Network elements as a function of terminal current-voltage at the fundamental frequency.

Case	Z_G	Z_S	Z_D
$Re\{Z_G\} = Re\{Z_S\} = 0$	$\frac{jRe\{V_G(I_G^* + I_D^*)\}}{Im\{I_G^* I_D\}}$	$\frac{jRe\{V_G I_G^*\}}{Im\{I_G I_D^*\}}$	$\frac{V_D}{I_D} - Z_s \left[1 + \frac{I_G}{I_D} \right]$
$Re\{Z_G\} = Re\{Z_D\} = 0$	$\frac{jRe\{I_D(V_G^* - V_G)\}}{Im\{I_G I_D^*\}}$	$\frac{V_G - Z_G I_G}{I_G + I_D}$	$\frac{jRe\{I_G(V_G^* - V_D)\}}{Im\{I_G I_D^*\}}$
$Re\{Z_D\} = Re\{Z_S\} = 0$	$\frac{V_G}{I_G} - Z_s \left[1 + \frac{I_D}{I_G} \right]$	$\frac{jRe\{V_D I_D^*\}}{Im\{I_G^* I_D\}}$	$\frac{jRe\{V_D(I_D^* + I_G^*)\}}{Im\{I_G I_D^*\}}$

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Table VI-4. P configuration: Network elements as a function of terminal current-voltage at the fundamental frequency.

Case	γ_{GS}	γ_{GD}	γ_{DS}
$\operatorname{Re}\{\gamma_{GS}\} = \operatorname{Re}\{\gamma_{GD}\} = 0$	$\frac{j\operatorname{Re}\{I_G(V_D^* - V_G^*)\}}{\operatorname{Im}\{V_D V_G^*\}}$	$\frac{j\operatorname{Re}\{V_G^* I_G\}}{\operatorname{Im}\{V_G^* V_D\}}$	$\frac{I_D}{V_D} + \gamma_{GD} \left[\frac{V_G}{V_D - 1} \right]$
$\operatorname{Re}\{\gamma_{GS}\} = \operatorname{Re}\{\gamma_{DS}\} = 0$	$\frac{j\operatorname{Re}\{V_D(I_D^* + I_G^*)\}}{\operatorname{Im}\{V_D V_G^*\}}$	$\frac{\gamma_{GS} V_G - I_G}{V_D - V_G}$	$\frac{j\operatorname{Re}\{V_G(I_G^* + I_D^*)\}}{\operatorname{Im}\{V_D^* V_G\}}$
$\operatorname{Re}\{\gamma_{GS}\} = \operatorname{Re}\{\gamma_{DS}\} = 0$	$\frac{I_G}{V_G} - \gamma_{GD} \left[\frac{V_D}{V_G} - 1 \right]$	$\frac{j\operatorname{Re}\{V_D^* I_D\}}{\operatorname{Im}\{V_D^* V_G\}}$	$\frac{j\operatorname{Re}\{I_D(V_G^* - V_D^*)\}}{\operatorname{Im}\{V_D^* V_G\}}$

Note: Although both topologies are possible from the point of view of oscillators, the T configuration is more adequate to harmonic oscillators, due to the difficulty of building a circuit where the feedback element γ_{DG} , is an open circuit at the output harmonic.

G – EXAMPLE OF A 10GHz HARMONIC OSCILLATOR

The objective is to design a second harmonic oscillator at the fundamental frequency of 5 GHz. The active device retained for this design is a FET which current-voltage curves are shown in Figure VI-15.

Two models were used. Following first the equivalent Curtice Cubic model (Table VI-5), its fitted characteristics are reported in Figure VI-16. The second approach by Statz model gave the input transfer function shown in Figure VI-17. The corresponding model parameters are related in Table VI-6. Note that we can observe a better G_{DS} match with measurements using Curtice model than Statz model. But near the pinch-off voltage, Statz model is relatively more accurate (quadratic variation of I_{DS} versus V_{GS}).

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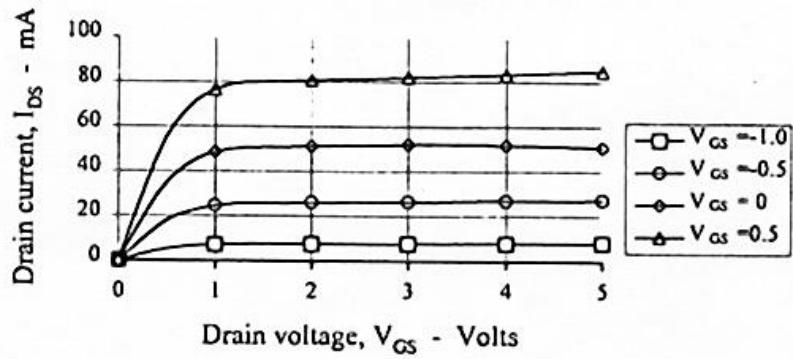


Fig. VI-15. FET I-V curves.

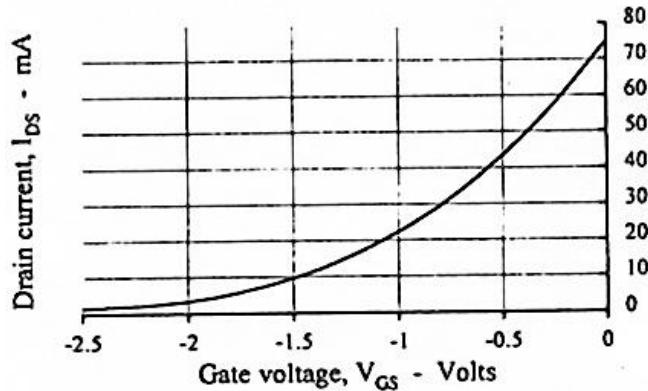


Fig. VI-16. FET transfer characteristics. Curtice cubic model.

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Table VI-5. Elements and parameter values of the FET – Curtice cubic model.

dc parameter	Value	Element	Value
A_0	0.016542 A	C_{gs}	0.527 pF
A_1	$0.0500214 V^{-1}$	C_{ds}	0.2513 pF
A_2	$0.02012 V^{-2}$	C_{gd}	0.087 pF
A_3	$1.0 \times 10^{-12} V^{-3}$	R_g	2.9 Ω
α	$2.16505 V^{-1}$	R_s	2.4 Ω
β_c	$-0.0394 V^{-1}$	R_d	5.3 Ω
		R_{ds}	618.5 Ω
		BV_{DS}	15 V
		V_{DS0}	3.0 V
		I_s	$1.0 \times 10^{-9} A$
		R_i	0.0 Ω

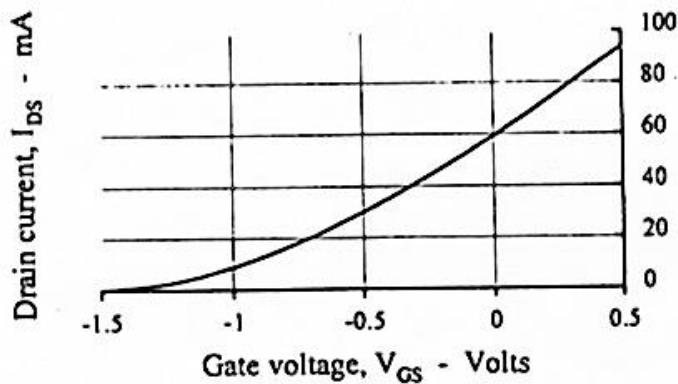


Fig. VI-17. FET transfer characteristics. Statz model.

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Table VI-6. Elements and parameter values of the FET – Statz model.

dc parameter	Value	Element	Value
α	2.035 V^{-1}	$-C_{gs}$	0.50 pF
β	0.044 mA/V^2	$-C_{ds}$	0.15 pF
B	0.29968 V^{-1}	$-C_{gd}$	0.054 pF
λ	0.015 V^{-1}	$-R_g$	4.0Ω
γ	2.16505	$-R_s$	3.0Ω
V_p	-1.5 V	$-R_d$	3.0Ω
		R_{ds}	800.0Ω
		BV_{DS}	7.0 V
		I_s	$1.0 \times 10^{-14} \text{ A}$
		R_i	0.0Ω

I – Bias

The first step is to define the device bias. For best second harmonic generation, it should be biased near the pinch-off gate voltage, V_p . However, biasing at pinch-off results in low transconductance that results in low loop gain, not adequate for starting oscillations. Thus, in order to guarantee the build up of oscillations, the device should be biased at a voltage greater than V_p , in class A mode, resulting in high value for the transconductance, as shown by the bias point A in Figure VI-18.

However, this gate bias results in lower second harmonic generation degrading the doubler efficiency. Employing a self-bias approach (point B) results in improved operation, since the increase of the RF signal generated at the beginning of the oscillations moves the gate dc level to more negative values (point C) and stabilizes the bias at a point near the pinch-off voltage. The input dc load line is also represented in the Figure. One point of the line is $V_{GS} = 0\text{V}$, $I_{DS} = 0 \text{ mA}$, and the other is $V_{GS} = V_p$ and $\{ I_{DS}/\pi = 60 / \pi = 20 \text{ mA} \}$. The drain bias is determined as the middle point between the maximum drain voltage and the saturation voltage.

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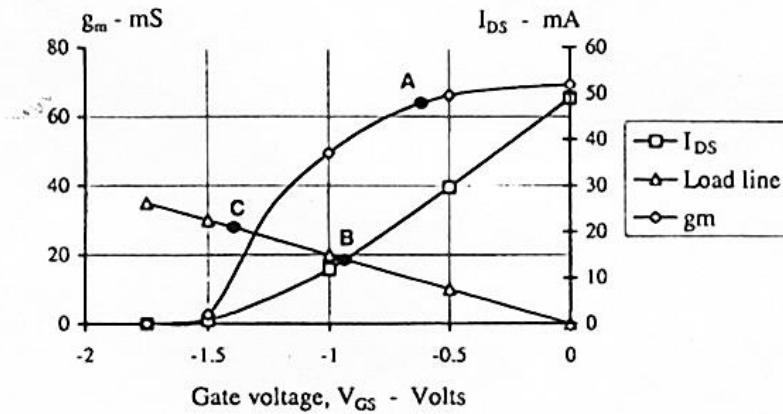


Fig. VI-18. Self-bias in harmonic oscillators.

II – Frequency doubler simulation

The second step is to simulate a frequency doubler in order to determine the current-voltage set that will produce good multiplier efficiency. The equivalent circuit of the frequency multiplier is represented in Figure VI-19. The frequency doubler network elements normalized at 5 GHz are reported in Table VI-7. This circuit provides 6dB gain with a return loss of 8 dB at 5 GHz.

The doubler characteristics were already reported (Figure VI-12). They show a power-added of 12 mW (10.8 dBm) for an input power of 5 mW (7 dBm).

The power balance for this circuit shows a gate power of 3.1 mW (5 dBm), a fundamental frequency drain power of 0.64 mW (-2 dBm) and a second harmonic power of 17.3 mW (12.4 dBm). The voltages, currents and respective harmonic powers are presented in Table VI-8.

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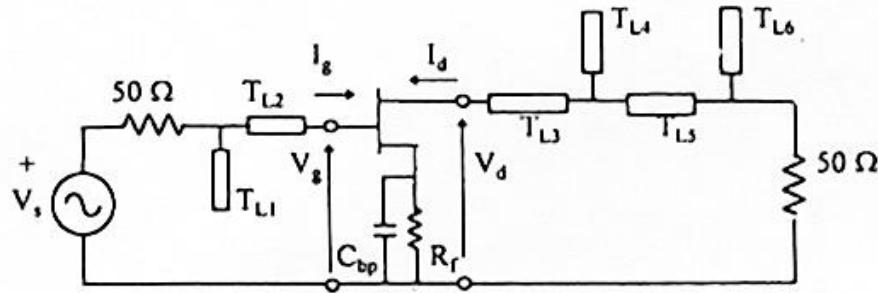


Fig. VI-19. Simplified frequency doubler circuit.

Table VI-7. Frequency doubler network elements normalized at 5.0 GHz.

Element No	Element Type	Parameters
T_{L1}	Open stub	$Z_0 = 25\Omega/\phi = 35.66^\circ$
T_{L2}	Series line	$Z_0 = 85\Omega/\phi = 69.34^\circ$
T_{L3}	Series line	$Z_0 = 62.5\Omega/\phi = 19.8^\circ$
T_{L4}	Open stub	$Z_0 = 50\Omega/\phi = 75.3^\circ$
T_{L5}	Series line	$Z_0 = 50\Omega/\phi = 110.9^\circ$
T_{L6}	Open stub	$Z_0 = 50\Omega/\phi = 95.1^\circ$
R_f	Resistor	$R = 60 \text{ ohms}$
C_{bp}		$C = 20 \text{ pF}$

Table VI-8. Current-voltage set for the frequency doubler.

Freq(GHz)	I_g (mA)	V_g (Volts)	P_G (mW)	I_d (mA)	V_d (Volts)	P_D (mW)
5.0	25.0/118.6°	2.36/34.5°	3.1	49.0/21.7°	0.53/-70.4°	0.64
10.0	2.3/111.6°	0.23/-156.4°	—	23.0/8.8°	1.70/-137.5°	17.3

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Note: From these results we have to consider that:

- The gate power (5 dBm) is 1 dB less than the available power from the generator (we have to include imperfect input match estimated here to 1 dB).
- The drain power is 0.6 mW at the fundamental frequency. It is lower than the gate power ad oscillations can be sustained is that power is fed back to the drain. We have then to **perform a new iteration** using a drain resistor that simulates the power required by the gate. Thus,

$$\Delta P = P_D - P_G = 2.5 \text{ mW} \quad (\text{VI-36})$$

Then (assuming the drain current remains the same),

$$R = \frac{2 \Delta P}{I_D^2} = 2.4 \Omega \quad (\text{VI-37})$$

The new set of I-V and resulting power at the harmonics are given in Table VI-9.

Table VI-9. Modified I-V and power to set $P_D > P_G$.

Freq (GHz)	I_g (mA)	V_g (Volts)	P_G (mW)	I_d (mA)	V_d (Volts)	P_D (mW)
5.0	25.0/119.0°	2.36/35.0°	3.1	48.0/21.7°	0.53/-83.8°	3.40
10.0	2.2/113.3°	0.22/-154.7°	—	23.0/10.6°	1.70/-135.9°	16.3
15.0	0.5/110.9°	0.02/14.0°	—	2.60/-96.3°	0.25/155.6°	0.10
20.0	0.2/-157.5°	0.05/3.2°	—	1.54/-49.2°	0.30/48.6°	—

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III - Harmonic oscillator design

The new I-V set was applied to the design of a T-type oscillator at the fundamental frequency (represented in Figure VI-20). Table VI-10 gives the resulting impedances from which the termination impedances must be synthesized.

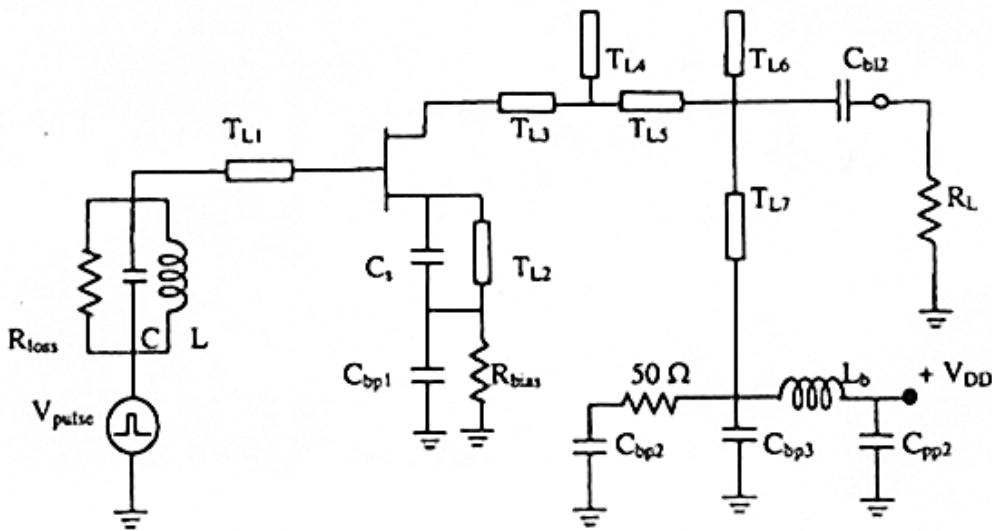


Fig. VI-20. Schematic of the harmonic oscillator.

Table VI-10. Terminating impedances for the harmonic oscillator.

Fundamental Frequency Impedances	Second Harmonic Frequency Impedances
$Z_D(\omega_0) = 0.18 + j15.48$	$Z_D(2\omega_0) = 61.3 + j40.8$
$Z_S(\omega_0) = 0.0 - j5.78$	$Z_S(2\omega_0) = 0.0$
$Z_G(\omega_0) = 0.0 + j97.7$	$Z_G(2\omega_0) = 3.5 + j100$

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IV- Small-signal check

From this table, we can note than the transistor requires capacitive impedance in the source, and both the drain and gate should be terminated by inductive impedances. After connecting those impedances to the three terminals, it is possible to check the small-signal oscillation conditions using Figure VI-21.

The analysis from the impedance point of view requires to divide the circuit into two parts, one containing the active device (impedance $Z_D(\omega_0, V)$ which is dependent on frequency ω_0 and signal amplitude V), and the other containing the resonator whose impedance $Z_L(\omega_0)$ is only dependent on frequency (a resonator response is independent on signal amplitude).

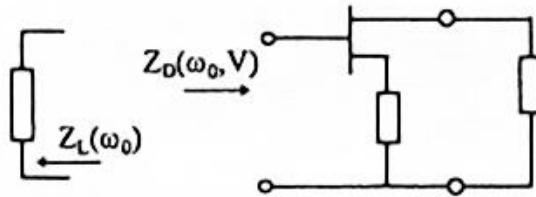


Fig. VI-21. Breaking the circuit into two components for small-signal check.

Thus, the oscillation conditions would be:

$$Re(Z_L(\omega_0)) + Re(Z_D(\omega_0, V)) < 0 \quad (\text{VI-38})$$

and

$$Im(Z_L(\omega_0)) + Im(Z_D(\omega_0, V)) = 0 \quad (\text{VI-39})$$

Therefore, the circuit impedances are:

$$Z_G(\omega_o) = -18.0 - j93.5 \Omega \quad (\text{VI-40})$$

and

$$Z_L(\omega_o) = 0.0 + j93.5 \Omega \quad (\text{VI-41})$$

At the source, the capacitance required for oscillation (C_s) is short-circuited by a $\lambda/4$ transmission line at the second harmonic. The capacitor Cbp1 shorts the bias resistor at the fundamental frequency and second harmonic.

The gate contains a tank circuit whose impedance is adjusted by transmission line TL₁ to present the required reactance at the fundamental frequency and to meet the gate impedance at the second harmonic (a very accurate matching is not essential).

The same band-stop filter employed in the doubler, TL₄ and TL₆ is used to block the fundamental. It presents a low loss at the second harmonic. The line TL₃ provides the drain impedance from table VI-10.

Simulated in time domain (with Spice), the waveforms responses are shown in Figure VI-22.

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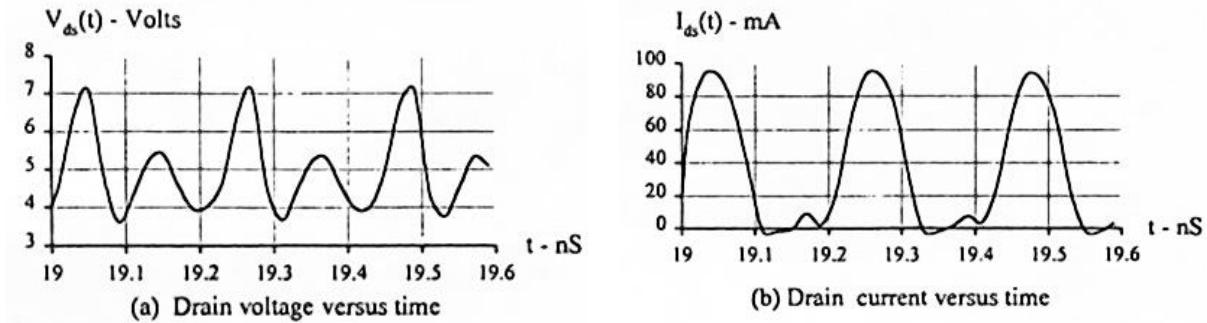


Fig. VI-22. I-V waveforms at the drain.

Figure VI-23 shows two complete cycles of the gate current. The gate current displays harmonic distortion due to the variation of input impedance within the signal period (due to the nonlinear drain current circulating in the drain circuit). Figure VI-24 represents the load voltage response where the multiplication effect is observed by comparing the period at the load with the period at the gate in Figure VI-23. Finally, Figure VI-25 shows the spectrum at the load.

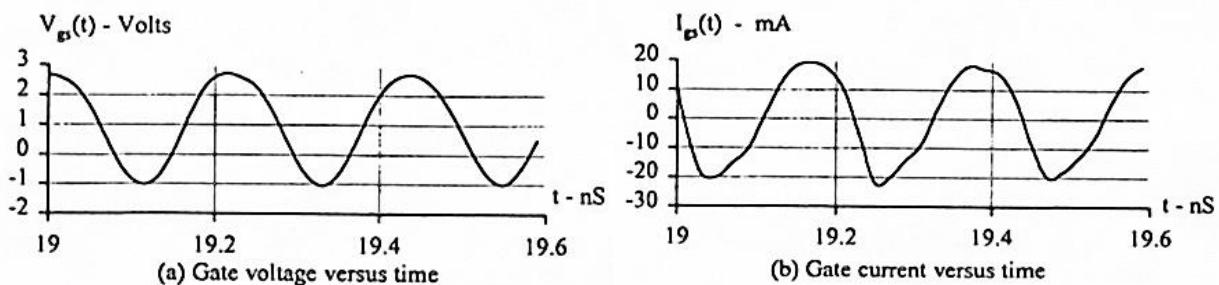


Fig. VI-23. I-V waveforms at the gate.

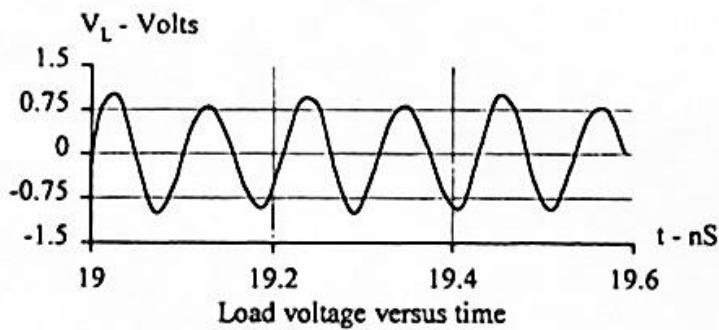


Fig. VI-24. Load voltage on the harmonic oscillator.

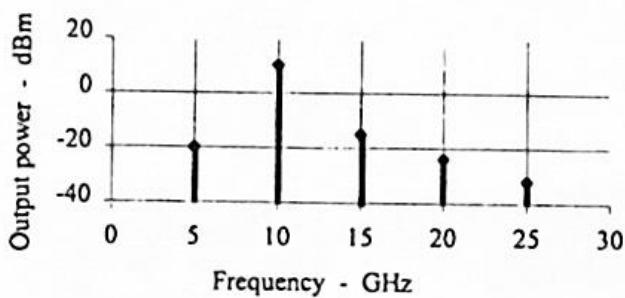


Fig. VI-25. Spectrum at the load harmonic oscillator.

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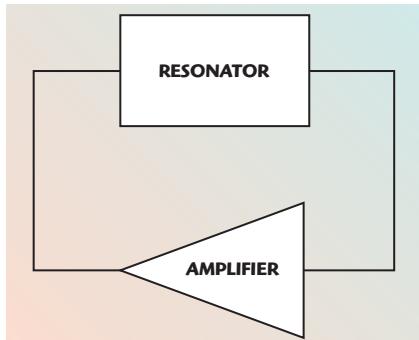
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A UNIVERSAL OSCILLATOR ANALYSIS TECHNIQUE THAT ACCURATELY ESTIMATES FREQUENCY AND OUTPUT POWER

During the last few decades, many different oscillator models and analysis techniques have been presented. From the negative impedance model, cavity type and DROs to the general feedback type, all oscillators have one common property. They are nonlinear positive feedback systems, and their electrical behavior is very hard to predict. Modern harmonic balance simulators are able to calculate parameters like oscillation frequency, power output, phase noise or harmonic content, but give little insight into the oscillator function during the design process. Many circuit simulators offer analysis functions like oscillator ports, which are mostly specialized directional couplers. Some parameters, however, like termination impedances, have to be estimated. This article presents a method with which it is possible to enlighten nearly any oscillator's behavior, and so eases and shortens the design procedure.

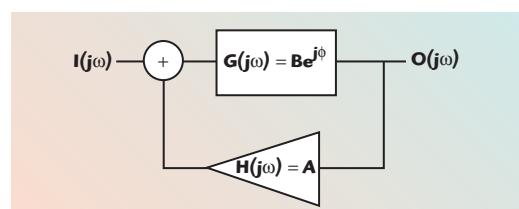
Fig. 1 Basic oscillator model. ▶



Generally, an oscillator can be seen as a positive feedback system. It usually consists of an amplifier followed by a resonator, which is fed back to the amplifier input, as shown in **Figure 1**. The amplifier task is to compensate for the losses in the resonator,

and the resonator does the frequency selection. It is of interest how these components should behave to generate the proper oscillation. **Figure 2** shows a simplified mathematical representation of a feedback system. The amplifier is assumed to have no phase shift, a gain of A , and infinite input and zero output impedance. The resonator is a simple phase shifter with an

attenuation B . The input signal $I(j\omega)$ is summed with the amplifier output signal and fed into the phase shifter. The output signal



▲ Fig. 2 Simple mathematical model of the oscillator.

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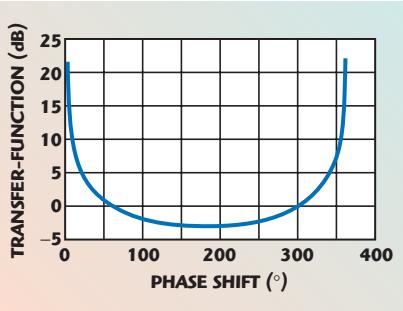


Fig. 3 Transfer-function with $A = 1$ and $B = 1$ as a function of phase shift ϕ .

$O(j\omega)$ is the output of the phase shifter and the input of the amplifier.

The transfer function of the circuit can then be stated as

$$F(j\omega) = \frac{O(j\omega)}{I(j\omega)} = \frac{Be^{j\phi}}{1 - ABe^{j\phi}} \quad (1)$$

where

$$\phi = \phi(\omega) = f(\omega)$$

and otherwise the oscillator's frequency ω is not defined. The formula stated in Equation 1 describes the behavior of a feedback loop by injecting a signal $I(j\omega)$ into the circuit while observing the output $O(j\omega)$. Therefore, to obtain a real oscillator condition without injection of an input signal, $I(j\omega)$ must fade to zero, while maintaining an output signal $O(j\omega)$. This is mathematically stated as

$$O(j\omega) = \lim_{I(j\omega) \rightarrow 0} \left(\frac{Be^{j\phi}}{1 - ABe^{j\phi}} I(j\omega) \right) \quad (2)$$

It can be seen in Equation 2 that if $I(j\omega)$ goes to zero, the other multiplication term must raise to infinity to get an output different from zero. So $A \cdot B$ must be equal to 1. **Figure 3** shows the transfer-function stated in Equation 1 with $A = 1$ and $B = 1$, as a function of the phase shift ϕ . It is easy to see that a phase shift of $n \times 360^\circ$ raises the transfer-function to infinity. For $B = A = 1$, Equation 2 can be simplified to

$$O(j\omega) = \lim_{I(j\omega) \rightarrow 0} \left(\left(j \frac{1}{2} \cot\left(\frac{\phi}{2}\right) - \frac{1}{2} \right) I(j\omega) \right) \quad (3)$$

Using the rule of L'Hospital, and with the phase going to zero for the oscil-

lating condition, the output can be calculated as

$$|O(j\omega)| = \lim_{I(j\omega) \rightarrow 0, \phi \rightarrow 0} \left(\left(j \frac{1}{2} \cot\left(\frac{\phi}{2}\right) - \frac{1}{2} \right) I(j\omega) \right) = 1 \quad (4)$$

This relation is commonly known as the Barkhausen criterion, which states that the loop gain must be 1 and the loop phase shift multiples of 360° to obtain oscillation.

TRANSFORMATION

The next question is how the numerous existing oscillator circuits can be converted to a feedback loop system. Stan Alechno showed¹ that nearly every oscillator can be converted to a common-emitter circuit, by first connecting all ground and power supply nodes, then letting them float and grounding the emitter. However, if feedback is performed inside the transistor, the circuit cannot be transformed.

Figure 4 shows an example of how a common-collector negative resistance oscillator can be transformed to a common-emitter circuit with the basic oscillator topology. As can be seen, the first conversion in (a) is to connect all the ground and power supply terminals together. This is possible, as power supply nodes represent a AC ground node, because the AC voltage is grounded by the large blocking capacitors between supply voltage and the common ground. The next step is to remove the ground from the circuit by letting all nets float. Now the ground can be placed on every node in the circuit, where it is advantageous for further analysis. In this case, the emitter of the bipolar transistor is grounded in (c). If the circuit in (c) is rearranged, the circuit in (d) appears, which shows a common-emitter circuit and a back fed resonator consisting of C_1 , C_2 , L and C .

This transformation becomes clearer if the ground node is seen as an ordinary circuit node, which is, in this case for example, the ground plane. The power supply, as previously stated, is also an AC ground node. Thus, it is possible to think of any node in the circuit to be the ground

node, and to re-sketch the circuit. However, this transformation has an impact on components that are part of the bias-supply of the active device. Since they have a DC function, their behavior changes, as the ground is connected to another node. In the original circuit, the load resistor RL is connected between emitter and ground. A DC current through this resistor will result in a voltage drop across it, resulting in a voltage increase at the emitter and base as well. The base bias resistor must take this voltage drop into account. In the rearranged circuit, the load resistor is connected to the transistor collector and the emitter is grounded. The base bias resistor now has a much larger voltage drop from power supply to the base as compared to the original circuit where the supply voltage to base voltage is lowered through the voltage drop across the load resistor RL . Consequently, the bias network must be recalculated for equal operation of the circuits. An example later in this article will show the difference between the two bias-

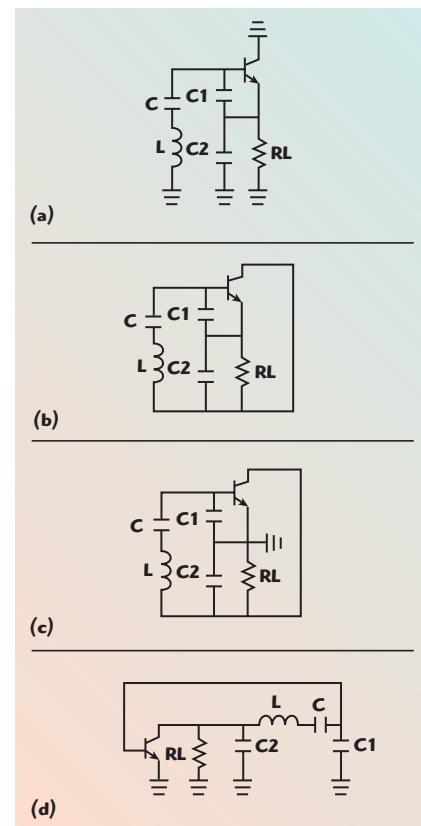
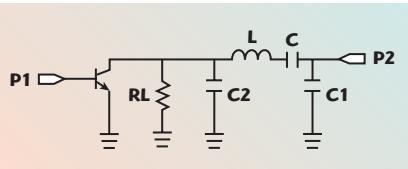
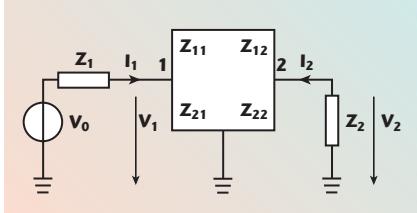


Fig. 4 Oscillator circuit transformation; (a) simplified common-collector oscillator, (b) with floating ground, (c) with emitter grounded and (d) rearrangement of c.

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▲ Fig. 5 Oscillator from Figure 4 with open loop and input port P1 and output port P2.



▲ Fig. 6 Conventional view of the oscillator in open loop analysis.

ing cases. For further analysis, the oscillator loop must be broken up, and a transfer-function can be recorded. An oscillator theory treating this problem is presented by Rhea².

CALCULATIONS

The circuit in **Figure 5** can be described by S-parameters, but then the ports P1 and P2 would be terminated in 50 Ω. This would not give the correct result for the transfer-function, since in the closed loop condition the output of the oscillator is terminated with its input's impedance and vice-versa.

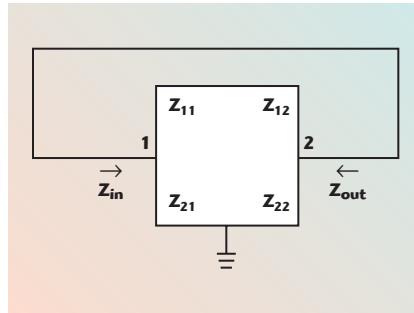
It is not easy to convert these parameters to more generality since S-parameters are defined for one characteristic impedance. For the sake of understanding, Z-parameters will now be used for defining the problem.

The function

$$\underline{Z} = T_{S \rightarrow Z}(\underline{S}) \quad (5)$$

which converts S-parameters to Z-parameters with the identity

$$\underline{Z} = \begin{pmatrix} Z_0 \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} & Z_0 \frac{2S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \\ Z_0 \frac{2S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} & Z_0 \frac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}} \end{pmatrix} \quad (6)$$



▲ Fig. 7 Oscillator with feedback.

will be used to convert the open loop oscillator circuit to the circuit in **Figure 6**, where Z_2 indicates the correct oscillator input impedance. More about two-port transformations and oscillators is given by Vendelin, et al.³

The following equations can be derived:

The forward voltage transfer function

$$\frac{V_2}{V_1} = \frac{Z_2 Z_{21}}{Z_{11}(Z_2 + Z_{22}) - Z_{12} Z_{21}} \quad (7)$$

The backward voltage transfer function

$$\frac{V_1}{V_2} = \frac{Z_1 Z_{12}}{Z_{22}(Z_1 + Z_{11}) - Z_{12} Z_{21}} \quad (8)$$

The input impedance

$$\frac{V_1}{I_1} = Z_{11} - \frac{Z_{21} Z_{12}}{Z_2 + Z_{22}} \quad (9)$$

The output impedance

$$\frac{V_2}{I_2} = Z_{22} - \frac{Z_{21} Z_{12}}{Z_1 + Z_{11}} \quad (10)$$

From Equations 7 to 10, it seems clear that all four parameters depend on the termination impedances Z_1 and Z_2 . For correct oscillator function, V_2/V_1 must be equal to 1. But since this transfer function depends on Z_2 and its value is unknown, the transfer function cannot be plotted correctly. If it is assumed for a while that there is no reverse influence from the output to the input ($Z_{12} = 0$), the parameters are simplified to

The forward voltage transfer function

$$\frac{V_2}{V_1} = \frac{Z_2 Z_{21}}{Z_{11}(Z_2 + Z_{22})} \quad (11)$$

The backward voltage transfer function

$$\frac{V_1}{V_2} = 0 \quad (12)$$

The input impedance

$$\frac{V_1}{I_1} = Z_{11} \quad (13)$$

The output impedance

$$\frac{V_2}{I_2} = Z_{22} \quad (14)$$

while Equation 11 still depends on Z_2 , Equations 13 and 14 are independent. Now, a second view on the oscillator circuit in **Figure 7** brings more light to oscillator behavior. As the output of the oscillator is connected with its input, the impedance Z_2 will result in $V_1/I_1 = Z_{11}$. This means that the oscillator looks back to its own input impedance. With this simplification and the feedback, Equation 11 reduces to

$$\frac{V_2}{V_1} = \frac{Z_{21}}{Z_{11} + Z_{22}} \quad (15)$$

By introducing the oscillation condition into Equation 15, the result is

$$1 = \frac{Z_{21}(\omega, P_s)}{(Z_{11}(\omega, P_s) + Z_{22}(\omega, P_s))} \quad (16)$$

where it is noted that the Z-parameters are a function of frequency and oscillator power P_s .

In the more general case, if $Z_{12} \neq 0$, Equation 16 does not hold anymore, and a new way of determining the impedances Z_1 and Z_2 must be accomplished formally. Oscillation can also be seen in the time domain as a wave traveling in a loop through the oscillator. This means that the wave is traveling through the circuit and is fed back to its input. Since the oscillator has a group delay, the Barkhausen criterion changes to

$$\int_0^{\omega_0} t_{grf} d\omega + \phi(0) = n \cdot 360^\circ \quad (17)$$

where

t_{grf} = the forward group delay
 ω_0 = frequency of oscillation

Equation 17 states that the group delay induces a phase shift. The oscillator can be seen as a non-reciprocal transmission line. As continuous reflection occurs in the oscillator from incorrectly terminated impedances, a wave traveling back is induced. However, since the transistor has low backward amplification, this reverse

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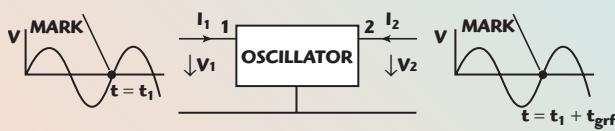


Fig. 8 Oscillator in the time domain.

Fig. 9 Equal input impedances Z_{i1} and Z_{i2} .

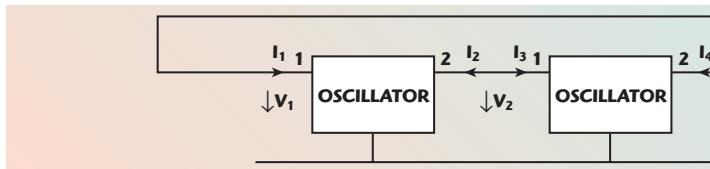
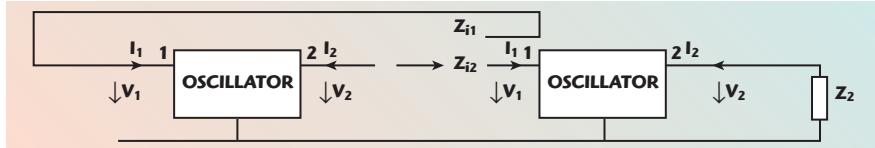
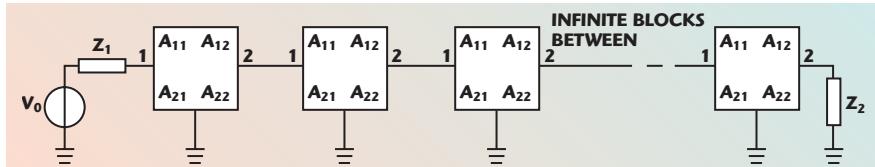


Fig. 10 Closed loop with two oscillators.

Fig. 11 Oscillator with infinite inserted two-ports A and broken up loop.



wave is heavily damped. In the case of $S_{12} = 0$ in the transistor, the reverse wave is totally blocked by the transistor and the impedances can be calculated as in Equations 13 and 14. This case is very similar to an ideal distributed isolator.

If a certain voltage zero transition in the traveling wave at the input could be marked, and if it were possible to follow it, the zero transition coming out of the oscillator circuit could be seen with a delay of t_{grf} , as shown in **Figure 8**. If it is assumed that the correct termination impedance is already known, the oscillator circuit, terminated with the correct impedance Z_2 , has the same input impedance $Z_{in} = V_1/I_1$ as the closed loop oscillator. Thus, the traveling wave out of the oscillator will have the same conditions of input impedances if it were fed back to the oscillator input or another oscillator circuit input, which is terminated with the correct impedance Z_2 .

Figure 9 shows the equal input conditions. The impedance Z_{i1} stands for the closed loop impedance and Z_{i2} for the input impedance of another oscillator circuit with the same S-parameters, terminated with the correct

will be introduced to convert the oscillator's open loop S-parameters to ABCD parameters

$$\underline{A} = T_{S \rightarrow A}(\underline{S}) \quad (18)$$

So the two two-ports transform to their ABCD equivalents A_1 and A_2 . Now the combined matrix is just

$$\underline{A}_{\text{total}} = \underline{A}_1 \times \underline{A}_2 \quad (19)$$

To get some insight into the infinite circuit of **Figure 11**, the Z-matrix of the infinite chained oscillator A-matrices will be calculated as

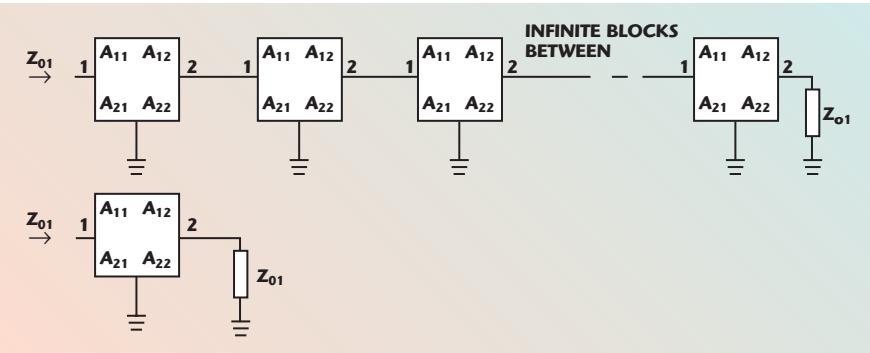
$$\begin{aligned} \underline{Z}_o &= \lim_{n \rightarrow \infty} \left(T_{A \rightarrow Z} \left(\underline{A}^n \right) \right) = \\ &\begin{pmatrix} Z_{o11} & Z_{o12} \\ Z_{o21} & Z_{o22} \end{pmatrix} \end{aligned} \quad (20)$$

This means that an infinite of \underline{A} matrices can be chained mathematically as an infinite matrix-multiplication with itself stated as \underline{A}^n , which stands for $\underline{A}_1 \times \underline{A}_2 \dots \times \underline{A}_n$. It is very interesting that the coefficients Z_{o11} and Z_{o22} converge to a fixed value which will be analytically derived later. Since an amplifier usually has a backward transfer function lower than 1, which means forward gain and backward isolation, the parameter Z_{o12} goes to zero, so with the Equations 11 to 14, Equation 20 reduces to

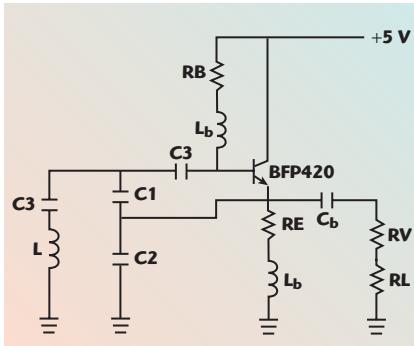
$$\underline{Z}_o = \begin{pmatrix} Z_{o1} & 0 \\ Z_{o21} & Z_{o22} \end{pmatrix} \quad (21)$$

That means that Z_{o1} is the input impedance and Z_{o2} is the output impedance of the network. With the determination of the impedances Z_{o1} and Z_{o2} the voltage transfer-function can be defined and set to 1. For the conventional oscillator analysis, Z_1 will be equal to Z_{o2} , which actually would not be used in oscillator forward analysis, and Z_2 will be equal to Z_{o1} , which is the interesting part for the transfer-function. If the loop is closed and broken up anywhere again, the calculated \underline{Z}_o matrix will have the same coefficients. If the input impedance of an infinite chain of oscillator two-ports is Z_{o1} , it will still be Z_{o1} if only one two-port is removed since there will still remain an infinite chain of oscillators. This shows that the input impedance of one single oscillator two-port must be

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▲ Fig. 12 Two-port input impedance with termination of port 2 with Z_{o1} .



▲ Fig. 13 Investigated oscillator circuit.

Z_{o1} if its output is terminated with Z_{o1} , as shown in **Figure 12**.

From this approach it seems clear that the oscillator closed loop impedances are Z_{o1} and Z_{o2} . To calculate the impedances Z_{o1} and Z_{o2} directly, the diagram for a two-port can be used with Equations 9 and 10 to obtain a solution. The definition out of (9) and (10) will then be

$$Z_{o1} = Z_{11} - \frac{Z_{21}Z_{12}}{Z_{o1} + Z_{22}}$$

and

$$Z_{o2} = Z_{22} - \frac{Z_{21}Z_{12}}{Z_{o2} + Z_{11}} \quad (22)$$

If these relations are transformed with respect to Z_{o1} and Z_{o2} , two qua-

dric equations result. The solution for these equations are:

$$Z_{o1(1,2)} = \frac{1}{2} \left(Z_{11} - Z_{22} \pm \sqrt{(Z_{11} - Z_{22})^2 + 4 \det(\mathbf{Z})} \right) \quad (23)$$

$$Z_{o2(1,2)} = \frac{1}{2} \left(Z_{22} - Z_{11} \pm \sqrt{(Z_{22} - Z_{11})^2 + 4 \det(\mathbf{Z})} \right) \quad (24)$$

As it can be seen from Equations 23 and 24, four solutions are possible, but only two of them are meaningful. The one with the positive real part is the preferred one, as the impedances should be passive in feedback designs.

The main difference between an oscillator and a transmission line is that the oscillator contains an active device, in which the input power is amplified with some gain. Thus, it is possible to get reflections and $|S_{21}| = 1$ at the same time.

This is not possible in ideal transmission lines since there S_{11} must be zero for lossless operation. The reflections in the oscillator travel backwards and have their own propagation properties. Through the reverse isolation of the oscillator, this reverse

wave is damped, but not extinguished. Since this wave is generated in every two-port in a chain, it influences the input impedance of the oscillator, which has been taken into account in Equations 23 and 24. The impedances Z_{o1} and Z_{o2} from Equation 21 can be

seen as the characteristic impedances of the traveling waves (forward and reverse), as the node voltages and input currents are equal over the whole infinite two-port chain.

SIMULATION

A simplified common-collector oscillator is designed for an oscillation frequency of 2.9 GHz and a loop power of 0 dBm. Its schematic is shown in **Figure 13**. The bipolar transistor is a BFP-420 from Infineon.

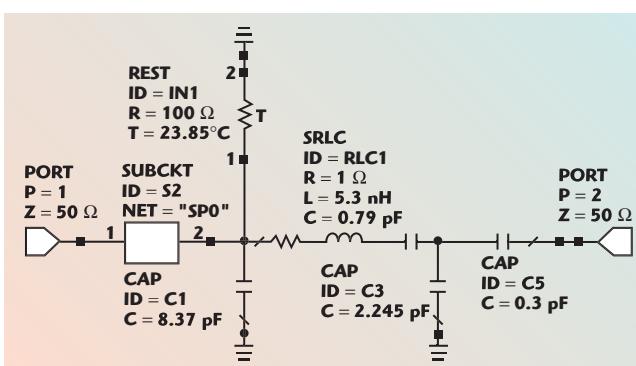
The resistors R_B and R_E are for biasing, while L_b and C_b are AC- and DC-blocking components, respectively. R_V is a coupling resistor to prevent oscillation from quenching, because of too low output load. The capacitor C_3 has been introduced to get more flexibility in frequency adjustment. After the transformation to a common-emitter configuration, the circuit can be drawn, as illustrated in **Figure 14**.

The subcircuit-block "SUBCKT" is a replacement of the BFP-420 transistor common-emitter, large-signal S-parameters for an input power of 0 dBm. Some harmonic balance simulations have been done with the pure transistor amplifier to get the different large-signal parameters at certain power levels. These large-signal parameters are only a modeling help, but they do not really exist by definition of scattering parameters, since, through the strong nonlinearities of the active device, many harmonics will be generated. The parameters are also dependent on the used power, so this part of the modeling will produce the largest error in the transfer-function behavior. The $100\ \Omega$ resistor replaces the sum of $R_V + R_L$. Blocking components such as L_b and C_b have been removed, as

TABLE I

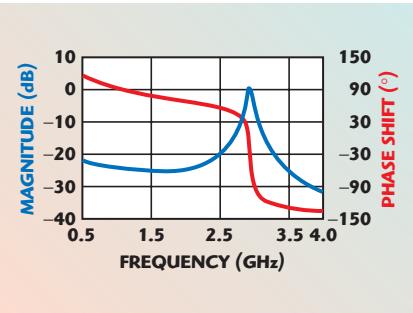
FORMULAS TO CALCULATE THE VOLTAGE TRANSFER-FUNCTION V_K IN MICROWAVE OFFICE

$NZ11 = \text{Schematic 1:Z[1,1]}$
$NZ12 = \text{Schematic 1:Z[1,2]}$
$NZ21 = \text{Schematic 1:Z[2,1]}$
$NZ22 = \text{Schematic 1:Z[2,2]}$
$ZK = 0.5^\circ(NZ11 - NZ22 + \sqrt{(NZ11 - NZ22)^2 + 4^\circ(NZ11 \cdot NZ22 - NZ12 \cdot NZ21)})$
$V_K = (ZK \cdot NZ21) / (NZ11 \cdot (ZK + NZ22) - NZ12 \cdot NZ21)$



▲ Fig. 14 Transformation of the circuit investigated.

TECHNICAL FEATURE



▲ Fig. 15 The transfer-function.

they have no influence on the oscillator analysis. Next the transfer-function is calculated with the Microwave Office Program⁴ and the formulas of **Table 1**, using Z-parameters with the result of Equation 21 introduced into Equation 7 and plotted over frequency, as shown in **Figure 15**.

Good proof that the plotted transfer-function is correct is to move the components from the output to the input. Since the oscillator analysis should be independent of the resonator location, the position of amplifier and resonator can be changed without altering the transfer-function. Even partial resonator components can be transferred from input to output and vice-versa without effect. With the component values chosen, the transfer-function is evaluated. It can be extracted that the phase shift crosses zero at 2.901 GHz, while the magnitude is -0.358 dB at the same frequency. To verify these results, an harmonic balance analysis has been set up and simulated.

One thing for which care must be taken is the different transistor biasing in **Appendix A** compared to a common-emitter circuit. It is very important that the collector-current and collector-emitter voltage stay equal to

TABLE II
COMPARISON OF THE TRANSFER-FUNCTION METHOD WITH HARMONIC BALANCE SIMULATION

	Transfer-function	Harmonic Balance	Error
Frequency (GHz)	2.9	2.9078	0.3%
Power (dBm)	0 (in base)	-0.2 (in base)	0.2 dB

the common-emitter large-signal equivalent circuit. The basic SPICE-model of the bipolar transistor is presented in the figure, with its package parasitic components. The harmonic balance simulation results are compared to the transfer-function approach in **Table 2**.

CONCLUSION

It has been shown that for many types of oscillators which can be converted to a feedback system, an accurate estimate of the oscillator frequency and output power is possible. Through linking an infinite number of oscillator open loop circuits, the true input and output termination impedances are defined. With Equations 23 and 24, these impedances can be calculated and inserted in an open loop analysis with a single oscillator circuit, from which a transfer-function can be plotted. The oscillation point can be determined by the general oscillator conditions (gain = 1 and phase shift = $n \times 360^\circ$). Using small-signal parameters, the start-up condition can be checked, and with the transistor's large-signal S-parameters at a certain input or output power, the oscillator can be designed the way that the true loop power will

meet the large-signal estimate. Since the large-signal S-parameters of the transistor are measured without the resonator circuit, the different terminations of harmonics as well as unknown reflections of the different harmonics and the fundamental frequency will influence the termination impedances. Further, the model which describes the active device must be accurate enough, as otherwise the results of the transfer-function approach will agree with the harmonic balance simulation results, but probably not the physical implementation. Good parasitic- and nonlinear modeling are obligatory. The comparison shows that the estimation error will be less than one percent for the frequency and less than 0.5 dB for power, which will be satisfying for most applications. ■

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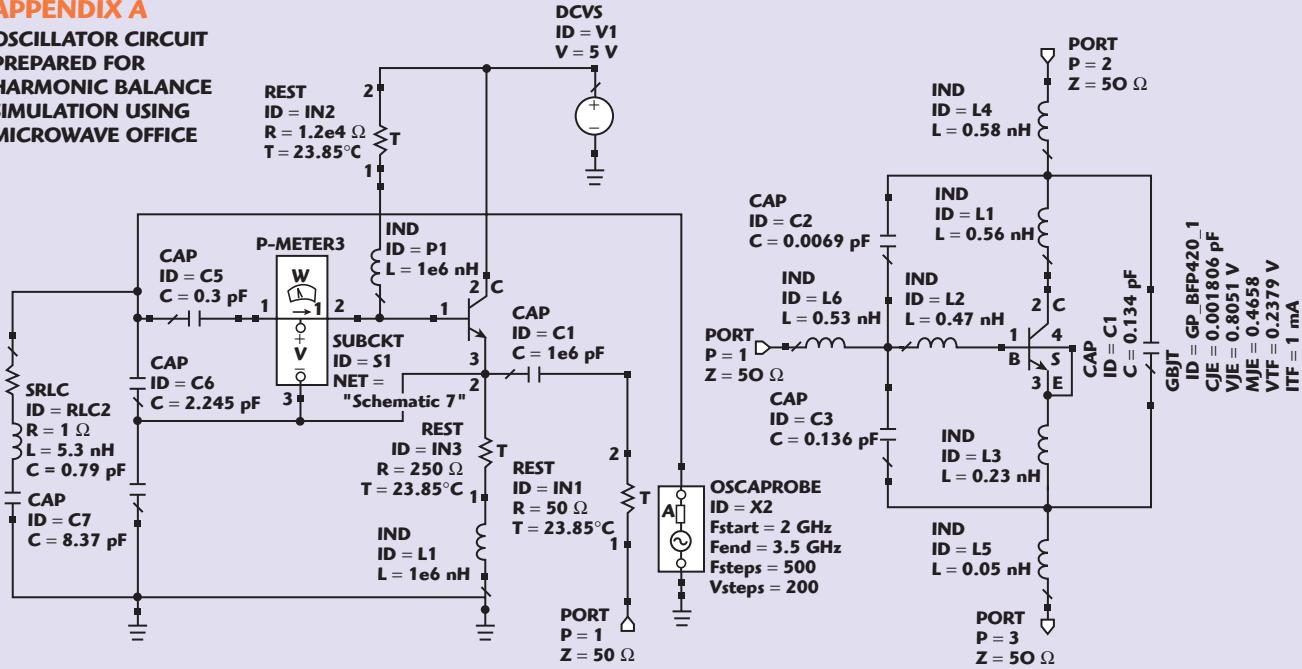
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TECHNICAL FEATURE

APPENDIX A

OSCILLATOR CIRCUIT
PREPARED FOR
HARMONIC BALANCE
SIMULATION USING
MICROWAVE OFFICE



SUMMARY

The behavior of GaAs Gunn diodes having epitaxial layer thicknesses of the order of $2 \mu\text{m}$ has been investigated. A coaxial (radial disc) bias circuit provides a resonant circuit at the fundamental operating frequency of the diode (30-50 GHz). The circuit can be tuned over a wide frequency range by various means. The harmonic components have been measured up to 110 GHz.

INTRODUCTION

Gunn as well as IMPATT diodes are inherently nonlinear devices. When such devices operate in a fundamental frequency resonant circuit, the current waveform is highly nonlinear, as has been shown theoretically in the past,^{1,2} and must therefore contain a number of harmonics. The requirement for low noise oscillators in the 90 GHz range has prompted a number of experimental and theoretical investigations concerning fundamental and harmonic operation of GaAs and InP Gunn diodes in the millimeterwave range³⁻⁸. Because the power output at the fundamental frequency decreases rapidly, but in an experimentally still unknown, and by theory not precisely predictable manner, in the range 50-100 GHz for GaAs, and 50-150 GHz for InP, harmonic operation is of practical importance. It is the purpose of this paper to describe some experimental data on GaAs Gunn diodes, operating in a coax/waveguide mount, which exhibits tunable resonances at the frequencies (30-60 GHz) corresponding to the fundamental frequency⁸, and which allows simultaneously efficient coupling at the harmonic frequencies⁹.

COAX/WAVEGUIDE CIRCUIT

The oscillator circuit used, is illustrated in fig. 1. It consists of a full height waveguide with backshort and a coaxial bias line with filter section, post and disc. The device indicated, represents the packaged device. An approximate equivalent circuit is illustrated in fig. 2 for the bias line, and fig. 3 for the portion below the disc. Because of the many reactive elements, a number of resonances are possible. The susceptance seen by the active device (-r, fig. 3), because of the very complex circuit, can be expected to have more than one zero, such that several resonances are possible, depending of course on the values of the parameters indicated in fig's 2 and 3, as well as on the waveguide dimensions. However, several possible resonances are apparent:

- I. A resonance of the entire coaxial line, including filter, post disc and device⁸.
- II. A resonance of the section below the disc, including the disc as a radial line.
- III. A resonance due to the waveguide cavity formed by the diode and the backshort.
- IV. A resonance due to the waveguide cavity formed by an effective iris (not shown) and the backshort^{7,10}.

IDENTIFICATION OF HARMONIC OPERATION

The experimental arrangement for identifying the frequencies emitted by the diodes is conventional and illustrated schematically in fig. 4. It consists of a diode with disc bias circuit and an appropriate waveguide section. Various waveguide systems are attached to the oscillator in order to monitor the frequency and power. The devices were operated cw and pulsed (200 nsec). Care must be exercised in choosing the waveguide sections and tapers with the proper cutoff frequencies. Standard tapers and specially designed tapers having

well defined cutoff frequencies (75, 50, 33 GHz) were used with W(75 - 110 GHz), V(50-75 GHz), Q(33-50 GHz) and Ka(26-40 GHz) waveguide systems.

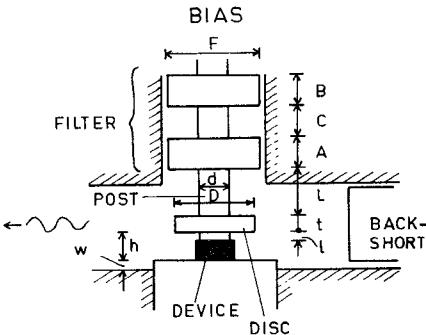
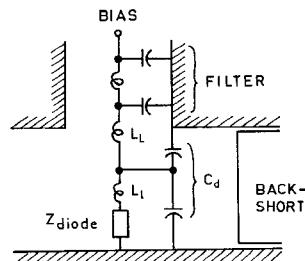
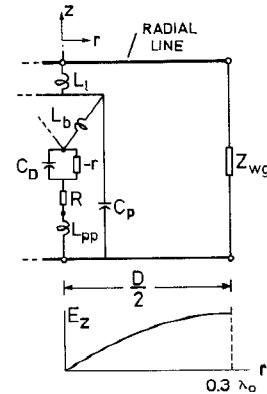


Fig. 1: Gunn oscillator with coaxial bias line



L_1 = inductance of post L
 L_L = inductance of section 1
 C_d = disc capacitance

Fig. 2: Approximate equivalent circuit of oscillator illustrated in fig. 1 at frequencies far away from $\lambda = 2D$.

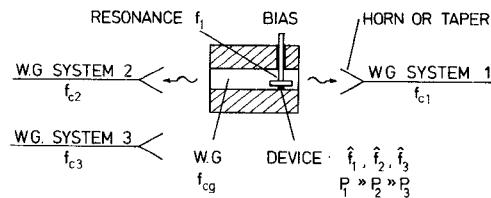


L_b = bonding wire inductance
 C_D = diode capacitance
 C_p = package capacitance
 $-r$ = diode negative resistance
 R = diode parasitic positive resistance
 L_{pp} = package post inductance
 Z_{wg} = waveguide impedance (load)

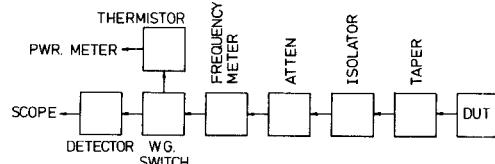
Fig. 3: Approximate equivalent circuit of disc and packaged device. The disc is represented as a transmission line.

FREQUENCY MEASUREMENTS

Experimental results of the frequency components of two diodes having different active GaAs layer thicknesses are illustrated in fig. 5. The oscillators consisted of short (5 mm) sections of waveguide in order to pass also the frequencies lying below their cutoff. The disc diameter, as well as the length of the section L were varied in order to tune the fundamental resonance from 25 to 55 GHz. The observed frequencies are indicated and are identified as second or third harmonic. The line $D = \lambda_0/2$ indicates the frequency at which the disc couples the diode optimally to the load, for a given disc diameter (λ_0 is the free space wavelength).



typical waveguide system:



f_c = cutoff frequency

\hat{f} = frequency at power maximum \hat{P}

Fig. 4: Experimental system for determining the fundamental and harmonic components of a Gunn diode oscillator.

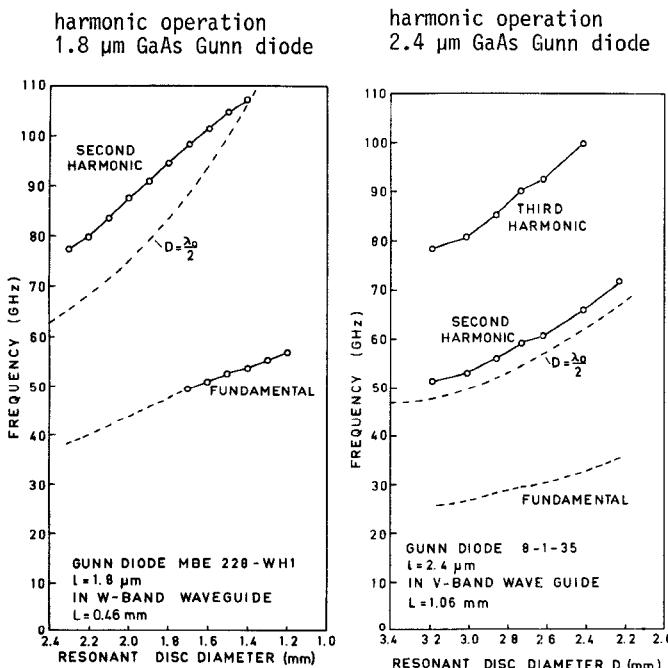


Fig. 5: Experimental results with 1.8 and 2.4 μm GaAs diodes illustrating harmonic components.

POWER MEASUREMENTS

Measurements of power for Gunn diodes (not Gunn oscillators) are an order of magnitude more difficult than frequency measurements. Optimum power output is obtained with discs corresponding to the relation $D \approx \lambda_0/2$, illustrated in fig. 5. Clearly, if the observed frequency does not correspond to the desired frequency, other parameters of the oscillator may be varied as discussed below. In fig. 6 are illustrated a portion of the fundamental and the second harmonic power output of an oscillator for several disc resonators which follow approximately the relation $D \approx \lambda_0/2$. Here a diode having an active length of 1.8 μm, grown in house by molecular beam epitaxy¹¹, was used. The true power levels are about 6 dB above those indicated. The peak fundamental power occurs at about 45-47 GHz, as was determined subsequently.

HARMONIC OPERATION-MBE GUNN DIODE

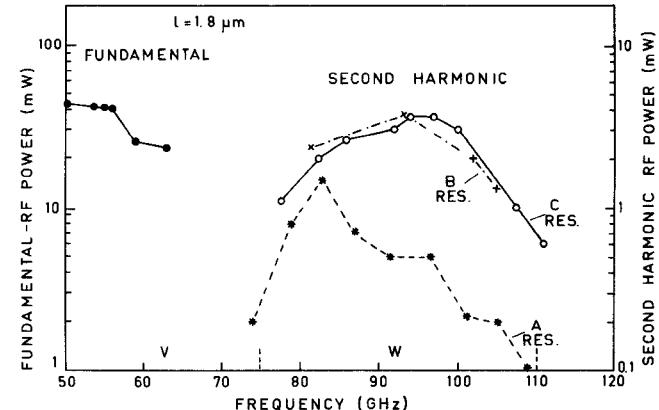


Fig. 6: Fundamental and second harmonic power of a 1.8 μm GaAs Gunn diode. Various disc sections were used to change the fundamental operating frequency.

HARMONIC OPERATION

For the harmonic operation of a Gunn diode, a complex circuit is required, fulfilling two requirements simultaneously:

1) A resonance circuit must be provided at the fundamental frequency. This is possible by means of a waveguide cavity, with the waveguide having a sufficiently low cutoff frequency^{7,10}. It is also possible by means of a coaxial circuit, made up primarily by the inductance of the post (section L) and the capacitance of the disc and the device⁸.

2) The harmonic must be coupled efficiently to the load by means of a low impedance reduced height waveguide and a backshort effective at the harmonic frequency, or a radial line⁹ of appropriate height h and diameter D (fig. 1 and 3). Best results were obtained with $L = 0$.

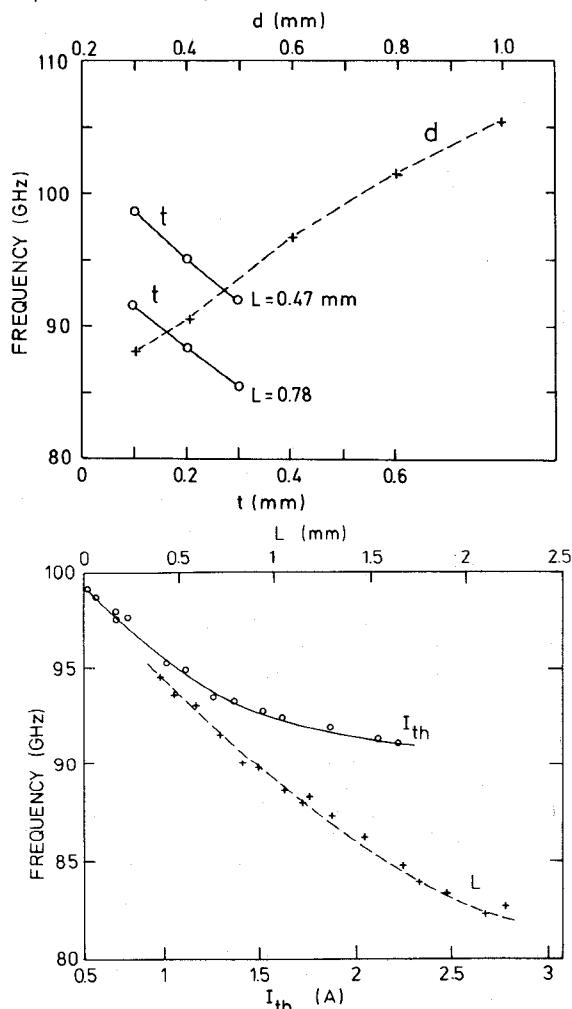
GUNN DIODES

Although we have investigated both InP and GaAs Gunn diodes, we shall report only on GaAs devices made at our own facilities. All devices were integral-heat-sink type mesa diodes, 30-130 μm in diameter, having mesa heights between 5 and 30 μm, bonded by means of single or cross type 12 x 50 μm gold ribbons into commercial packages having an alumina ring of approximately 0.4 mm inside and 0.8 mm outside diameter and 0.3 mm height. We have used GaAs epitaxial layers grown both by the conventional vaporphase epitaxy (Plessey Co.) as well as our own material grown by molecular beam epitaxy. One purpose of our investigation was to determine the power spectra of the devices at the fundamental and the harmonic frequencies for various active GaAs layer thicknesses and carrier concentrations, of which very little is known to date.

COAXIAL CIRCUIT - EFFECT OF PARAMETERS

As can be deduced from figures 1 thru 3, a change in the dimensional parameters of the coaxial circuit as well as of the package or the diode should effect the frequency. We have confirmed this for the parameters A, B, C, L, d, t, w, L_b , C_D and C_p . The variation of the frequency with four of these parameters is illustrated in fig. 7. I_{th} is directly proportional to the diode capacitance which was varied by chemically etching a diode successively smaller in cross section. In addition, it was observed that a reduction in the package capacitance from 160 fF to 40 fF caused a frequency increase of 7%. The variation with w was about 3%/mm, and with t about 10-15%/mm. The filter section which was designed for 90 GHz is an effective capacitance in the fundamental frequency range, such that primarily the parameter A will effect the frequency. We have observed a change of 3%/mm. By varying the bondwire inductance L_b , a considerable frequency change was observed; 5% by changing from a single ribbon to two crossed ribbons.

The disc capacitance can be continuously varied electrically or mechanically⁸ as illustrated in fig. 8. In fig. 9 we illustrate experimental results of a method of mechanical tuning by means of a metal pin. The individual curves for discs of different diameters are the combined disc and diode response. The true diode power spectrum is the envelope of all responses. Two diodes individually tuned in this manner have been used by us in power combining circuits.



I_{th} = diode threshold current

Fig. 7: Experimental results of the second harmonic frequency variation with several parameters.

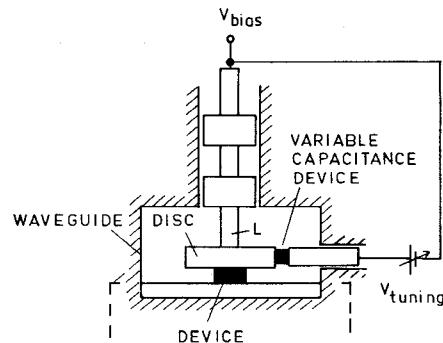


Fig. 8: Continuous frequency tuning by means of varying the disc capacitance.

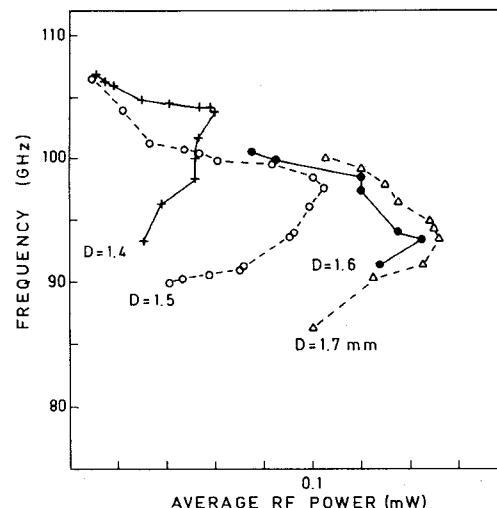


Fig. 9: Experimental results for mechanical disc capacitance tuning for four discs. The frequency shown is the second harmonic. The active length of the pulsed diode was about 2 μ m.

THE SOURCE OF THE HARMONIC POWER

Harmonic generation in semiconductors having a non-linear velocity-field characteristic has been treated in the past¹². Unfortunately, experimental details have been extremely scarce, and most theoretical treatments simply assumed a static nonlinear current-voltage characteristic, neglecting the very complex carrier dynamics occurring when the product of carrier density and active device length is about 10^{11} or higher¹. The exact source of the harmonic components will require further theoretical and experimental investigations.

CONCLUSION

Coaxial disc circuits exhibit in conjunction with Gunn diodes tunable resonances in the lower millimeterwave range. Our experimental evidence indicates that the circuit of fig. 1 behaves in a certain frequency range like a lumped element circuit. Capacitances (mechanical or electrical) may be introduced at various points, such as the disc periphery, and successfully used for broadband frequency tuning. The effect of a number of dimensional parameters of the coaxial bias line, as well as diode and package parameters, on the frequency has been presented.

An active GaAs layer thickness of 1.8 μ m is well suited for diodes with maximum fundamental power output at 47 GHz. A 90 GHz diode would require a 1 μ m layer. No reports of such a diode exist to date.

The true source for the harmonics observed in Gunn diodes is not clear at this time. If oscillators are to be incorporated in future planar circuits, such as integrated front ends, the results of our investigations indicate that fundamental frequency Gunn diodes are difficult to realize at 90 GHz. Since such circuits will make use of semi-insulating GaAs substrates, possible oscillators will be GaAs Gunn diodes, or GaAs field effect transistors operating at the second or third harmonic frequency. Another very promising device is the heterojunction bipolar transistor which may be capable of fundamental operation in excess of 100 GHz¹³.

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Fundamental and Subharmonic Excitation for an Oscillator with Several Tunneling Diodes in Series

Olga Boric-Lubecke, *Student Member, IEEE*, Dee-Son Pan, *Member, IEEE*, and Tatsuo Itoh, *Fellow, IEEE*

Abstract—Connecting several tunneling diodes in series shows promise as a method for increasing the output power of these devices as millimeter-wave oscillators. However, due to the negative differential resistance (NDR) region in the dc I–V curve of a single tunneling diode, a circuit using several devices connected in series, and biased simultaneously in the NDR region, is dc unstable. Because of this instability, an oscillator with several tunneling diodes in series has a demanding excitation condition. Excitation using an externally applied RF signal is one approach to solving this problem. This is experimentally demonstrated using an RF source, both with frequency close to as well as with frequency considerably lower than the oscillation frequency. Excitation by an RF source with a frequency as low as one sixth of the oscillation frequency was demonstrated in a proof-of-principle experiment at 2 GHz, for an oscillator with two tunnel diodes connected in series. Strong harmonics of the oscillation signal were generated as a result of the highly nonlinear dc I–V curve of the tunnel diode and a large signal oscillator design. Third harmonic output power comparable to that of the fundamental was observed in one oscillator circuit. If submillimeter wave resonant-tunneling diodes (RTD's) are used instead of tunnel diodes, this harmonic output may be useful for generating signals at frequencies well into the terahertz range.

I. INTRODUCTION

THE RESONANT TUNNELING diode (RTD) is a promising device for generating signals at millimeter wave and terahertz frequencies. It is currently the fastest solid state source, with the highest reported frequency of oscillation at 712 GHz [1]. This frequency may be further increased if a Schottky collector is used instead of the ohmic contact on the top of the device [2]. Because of its highly nonlinear dc I–V curve, which contains a negative differential resistance (NDR) region, an RTD may be used for a variety of applications such as in a self-oscillating mixer [3], frequency multiplier [4], [5] or a low-noise oscillator. Oscillation can be stabilized using quasi-optical techniques to obtain output power with a narrow spectral linewidth [6]. The main disadvantages of RTD oscillators are a small available output power and possible spurious oscillations arising from the low frequency NDR. Series integration of RTD's has been proposed to enhance the output power at millimeter wave frequencies [7], [8]. For example, the available power from ten series integrated RTD's considered in [7] is predicted to be 0.1 W at 100 GHz. A series

integrated device may be used as a unit in a power combining grid, to further increase the output power.

Due to the NDR region in the dc I–V curve of a single RTD, a circuit using several RTD's connected in series and biased simultaneously in the NDR region is dc unstable. As a result of this dc instability, there are some special considerations for an oscillator with several RTD's connected in series as compared to a single RTD oscillator. The oscillation amplitude has to be sufficiently large to cover a considerable portion of the positive differential resistance (PDR) region of the dc I–V curve [7], [8]. Besides the high frequency cutoff at which the negative differential resistance (NDR) vanishes, there is also a low frequency cutoff below which oscillation cannot be maintained [9]. The combination of the amplitude cutoff and low frequency cutoff phenomena make the occurrence of low frequency spurious oscillations highly unlikely. A simple dc battery alone cannot be used to bias all RTD's simultaneously in the NDR region of the dc I–V curve. If a dc bias voltage sufficient to bias all RTD's in the middle of the NDR region is applied gradually, the dc instability will divide this voltage so that all the RTD's are biased in the PDR region [8]. There are several ways to solve the biasing problem. One way is to use a fast electrical pulse to bias all diodes simultaneously in the NDR region [7], [8]. Alternatively, an external RF source, with frequency close to the resonant frequency of the circuit, may be used to switch the diode bias points from the PDR to the NDR region, and initiate the oscillation [10], [11]. Subharmonic excitation was also proposed and simulated [12].

In this paper, RF excitation with a frequency close to the oscillating frequency (fundamental frequency excitation) is discussed in more detail than in previous work [11], and the experimental demonstration of subharmonic excitation is presented. Due to the nonlinear multi-frequency nature inherent in the subharmonic excitation scheme, the details of the phenomena involved are quite complicated. A preliminary theoretical explanation is given in [12]. A more detailed theoretical explanation will be given later. Here, we will mainly present a phenomenological description of the experimental findings. A successful excitation was observed in many cases. Excitation with an RF source with frequency below one sixth of the oscillation frequency was demonstrated for a 2-GHz oscillator with two tunnel diodes connected in series. Strong harmonics were generated in the circuit which oscillated with a very large amplitude, due to the high nonlinearity of the tunnel diode dc I–V curve. A third harmonic signal with power comparable to that of the fundamental was observed in this circuit. If series integrated high frequency RTD's are

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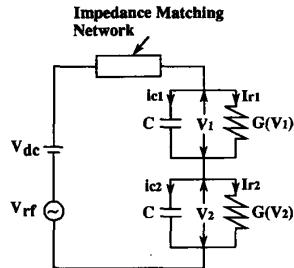


Fig. 1. Equivalent circuit of an oscillator with two tunnel diodes in series.

used instead of series connected tunnel diodes, and the third harmonic is extracted, a signal with frequencies well into the terahertz range may be obtained.

The original goal of this work is to build a millimeter-wave oscillator with several RTD's integrated in series. However, since planar RTD's are not readily available, low power tunnel diodes connected in series were used for a proof-of-principle experiment at 2 GHz. Tunnel diodes are very similar to RTD's, and are commercially available in a planar package. The performance of an oscillator with several RTD's connected or integrated in series is expected to be similar to the performance of an oscillator with several tunnel diodes connected in series.

II. THEORETICAL CONSIDERATIONS

A qualitative explanation of the RF instability of a dc stable condition, valid for both fundamental and subharmonic excitation will be presented here. A simple circuit model for an oscillator with two tunnel diodes connected in series is shown in Fig. 1. Each diode is represented as a parallel connection of a nonlinear conductance and a capacitance. Capacitances are assumed to be equal and independent of voltage. All parasitics including series resistance are included in the impedance matching block. If a dc bias voltage sufficient to bias both diodes in the middle of the NDR region is applied gradually, the dc instability will divide this voltage so that one diode is biased on the first rising branch of the dc I-V curve (V_{dc1} in Fig. 2), while the other diode is biased on the second rising branch (V_{dc2} in Fig. 2). The same constant resistive current flows through both diodes and there is no current through the capacitors. The total voltage drop across both diodes is assumed to be equal to the applied dc voltage (the voltage drop across the series resistance is neglected). Hence, before an RF signal is applied

$$I_{r1} = I_{r2}, \quad (1a)$$

$$i_{c1} = i_{c2} = 0, \quad (1b)$$

$$V_{dc1} \neq V_{dc2}, \quad (1c)$$

$$V_{dc1} + V_{dc2} = V_{dc}. \quad (1d)$$

When an RF signal is applied, the dc components of the resistive currents will change, due to the high nonlinearity of the dc I-V curve of the tunnel diode. Assuming the change is slow within one RF period, the changing dc component of the current and the voltage may be defined as the average value over one RF period. Rectified I-V curves, calculated using

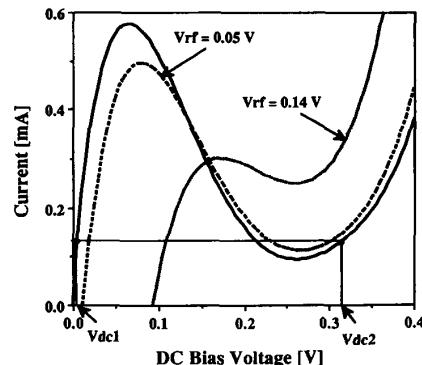


Fig. 2. DC I-V curve and rectified I-V curves for $V_{rf} = 0.05$ V and $V_{rf} = 0.14$ V for a single tunnel diode.

the procedure described in [13], are shown in Fig. 2 for RF voltage amplitude of 0.05 and 0.14 V. This explanation is only qualitative because we have not taken into account the detailed RF amplitude for each diode. For the diode biased on the first rising branch the dc component of resistive current I_{r1} will decrease, whereas for the diode biased on the second rising branch the dc component of resistive current I_{r2} will increase. Since the total dc and RF current through both diodes has to be constant at any instant in time, in addition to RF capacitive currents there will exist transient capacitive currents i_{c1} and i_{c2} that have to compensate for this change of the averaged resistive currents

$$I_{r1} + i_{c1} = I_{r2} + i_{c2} \quad (2)$$

where the quantities in (2) are the dc components defined over one RF period. If the RF voltage drop on both diodes is assumed to be small, so that it does not affect the dc voltage drop, the transient capacitive currents are then

$$i_{c1} = C \frac{dV_{dc1}}{dt}, \quad (3a)$$

$$i_{c2} = C \frac{dV_{dc2}}{dt}. \quad (3b)$$

During the transient process, capacitive currents have to be of opposite sign, because voltages V_{dc1} and V_{dc2} cannot simultaneously increase or decrease, while the total dc voltage remains constant. Therefore i_{c1} will be positive as shown in Fig. 2 and V_{dc1} will increase, whereas i_{c2} will be negative and V_{dc2} will decrease. Once the dc components of the resistive currents through both diodes are equal, the diodes' bias points are switched from the PDR to the NDR region and the dc bias voltage is equally divided.

A very small RF excitation signal may be used for switching, because even a small RF amplitude produces a large current decrease at bias points on the first rising branch of the dc I-V curve. Any frequency in the operational range of the oscillator may be used for switching. However, after the excitation is turned-off, oscillation cannot build-up and be sustained for all excitation frequencies. If the turn-off time of the RF signal is fast, this transition is less critical and there is a better chance that the oscillation will be present. For fundamental excitation, the turn-off time is not critical,

TABLE I
ONE-DIODE OSCILLATOR DESIGN AND PERFORMANCE

CIRCUIT	DESIGN				EXPERIMENT		
	V _{rf} [V]	P [dBm]	R _d + jX _d [Ω]	X _d / R _d	f [GHz]	P [dBm]	Q _{ext}
1D1	0.136	-18.68	-32.2 -j135.1	4.2	2.0205	-19.83	6
1D2	0.140	-18.76	-30.4 -j136.1	4.5	2.0206	-20.00	10
1D3	0.154	-19.50	-22.6 -j139.7	6.2	2.0651	-20.83	22
1D4	0.164	-20.90	-15.6 -j142.1	9.1	2.0681	-22.33	42

TABLE II
TWO-DIODE OSCILLATOR DESIGN AND PERFORMANCE

CIRCUIT	DESIGN				EXPERIMENT		
	V _{rf} [V]	P [dBm]	R _{2d} + jX _{2d} [Ω]	X _{2d} / R _{2d}	f [GHz]	P [dBm]	QR
2D1	0.136	-15.68	-61.3 -j259.4	4.2	/	/	/
2D2	0.140	-15.76	-57.8 -j261.2	4.5	1.9879	-18.00	2
2D3	0.154	-16.50	-42.9 -j267.9	6.2	1.9316	-19.17	2
2D4	0.164	-17.90	-29.6 -j272.3	9.2	1.9730	-21.33	3
2D5	0.176	-23.65	-10.1 -j276.1	27.3	1.8650	-26.90	/

because the oscillator is only switching from the locked mode to the free-running mode. If an RF signal with a frequency that is an integer fraction of the oscillation frequency is used for the excitation, the nonlinear tunnel diode will generate harmonics at the fundamental oscillation frequency. Intuitively, if one of the harmonics coincides with or is close to the oscillation frequency of the circuit, the turn-off time of the excitation signal may not be critical. While the excitation signal is decreasing, the desired signal already exists and if large enough may be amplified and sustained after the excitation ceases. Since a nonlinear, reactive oscillator circuit may act as a divider as well, two thirds of the oscillation frequency can also be used for the excitation. In this case, two thirds generate one third of the excitation frequency, which is then multiplied to produce the desired signal. For larger amplitude oscillators, excitation frequencies may be further away from exact integer fractions of the desired frequency, because the circuits are more stable overall.

III. EXPERIMENTAL SETUP

Back tunnel diodes manufactured by Metelics Co. were used for the experiment. The diode characteristics and oscillator configuration are described in [11]. Several one-diode and two-diode oscillators were designed at 2 GHz for oscillation amplitudes between 0.136 V at which maximum power output occurs, and 0.176 V at which large signal negative conductance

almost vanishes [11, Tables I and II]. In Tabs I and II, loss due to the series resistance of the diode was taken into account when the output power was calculated. The distance between the two diodes was limited by the diode package to about 0.5 mm. For two-diode oscillators, the distance between the packages was taken into account for impedance calculations, and the output power was calculated as twice that of the corresponding one-diode oscillator.

The experimental set-up is shown schematically in Fig. 3. An HP 8350B sweep oscillator with an HP 83592C plug-in was used as an external RF source. The turn-off time of the RF signal for this generator is 20–50 ns, depending on the frequency and the power of the signal. The RF excitation is applied to the oscillator circuit through a circulator. The dc bias voltage was applied through a bias-T network, and the dc current was monitored during the experiment. The oscillator signal was detected by an HP 8562A spectrum analyzer. The loss between the signal generator and the oscillator is about 2 dB, and between the oscillator and the spectrum analyzer it is about 3 dB. This setup is very similar to that of the reflection injection-locking scheme [14]. However, the major difference is that in this experiment the excitation signal is applied only for several seconds. The oscillator is not necessarily injection-locked to the external RF signal during the excitation. Once initiated, the output signal of the oscillator is completely independent of the excitation signal power and frequency.

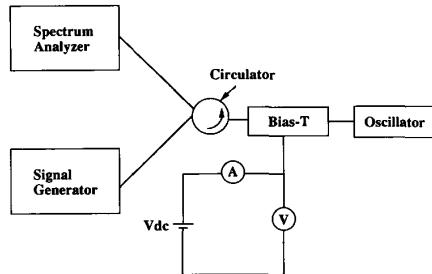


Fig. 3. Schematic diagram of the experimental setup. The external RF signal was applied only for several seconds.

IV. FUNDAMENTAL FREQUENCY EXCITATION

A dc voltage of 0.33 V, sufficient to bias both diodes in the middle of the NDR region, was applied to each two-diode oscillator. As a result of dc instability, both diodes were initially biased in the PDR region, one at 0.01 V and the other at 0.32 V, with 0.1 mA of bias current. An RF signal with frequency close to the expected oscillation frequency of 2 GHz was applied for several seconds. During excitation, the bias current increased to 0.23 mA and the oscillation signal appeared. After turning the excitation signal off, the oscillation was present in all circuits, except for circuit 2D1, which indicates that its designed oscillation amplitude was below the amplitude cutoff level required for sustained oscillation [7], [8]. The oscillation frequency and output power for oscillators 2D2–2D5 is shown in Table II. After excitation, the bias voltage was slightly increased to maximize the output power. Circuit 2D5 had the largest discrepancy, 6.7%, between the designed and measured oscillation frequencies. This circuit was designed for a very large oscillation amplitude and consequently generated large harmonics that were not accounted for in the design [13]. A full harmonic balance method such as the one described in [15] should be used for a more accurate design for very large oscillation amplitudes.

Successive triggering by tuning the bias voltage was only possible with circuit 2D5. As the bias voltage was gradually increased, one diode started to oscillate; this oscillation then excited the second diode as bias was further increased. RF excitation was not necessary for this circuit. Successive triggering can only happen for very large oscillation amplitudes and a small number of diodes connected in series [8]. If more diodes are connected in series, it is harder to satisfy the large signal oscillation condition for all successive cases.

The minimum required excitation power was found to be a strong function of the oscillation amplitude. Fig. 4 shows the output power (solid line) and minimum required excitation power (dotted line) for oscillators 2D2–2D5. For relatively small oscillation amplitude circuits (2D2 and 2D3) only -32 dBm was necessary for excitation, which is 13–14 dB lower than the output power of these oscillators. For higher oscillation amplitude circuits, higher excitation power was required. For the circuit designed for the largest oscillation amplitude (2D5), the required excitation power was about 5 dB higher than the output power. Larger amplitude oscillators have a higher ratio of imaginary to real part of the total diode

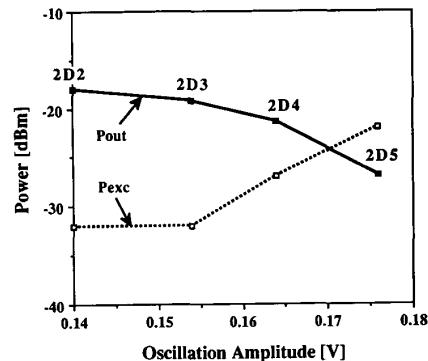


Fig. 4. Output power (solid line) and minimum required excitation power for fundamental frequency excitation (dotted line) for oscillators 2D2–2D5 as a function of the oscillation amplitude.

impedance (X_d/R_d), and therefore higher external quality factors (Q_{ext}) are expected [14, tables I and II]. Circuits with higher Q_{ext} are harder to perturb, and hence larger excitation power is required. Also, circuits designed for a larger oscillation amplitude have a higher reflection coefficient (initially, when both diodes are biased in the PDR region), and therefore less power is delivered to the diodes. After reflection is taken into account, circuit 2D5 required 5 dB higher power delivered to the diodes than circuit 2D2.

Excitation was possible over a broader frequency band centered on the oscillation frequency for circuits with higher oscillation amplitudes. For circuit 2D2, the excitation bandwidth was 80 MHz, or 4%, whereas for circuit 2D5, the excitation bandwidth was about twice as wide, 158 MHz, or 8.5%. With the excitation frequency very close to the oscillation frequency, the oscillator was injection-locked to the external RF during excitation, and the total power was lower than the power of the free running oscillator. With the excitation frequency at the edge of the excitation band, the external RF signal, the oscillation signal, and their mixing products were present during excitation, and the oscillation signal remained unchanged after the excitation was turned-off. If the excitation frequency is further away from the oscillation frequency, it will take more time for the oscillator to reach steady state after the excitation is turned off. During this time, discrepancy between bias points of individual diodes may increase sufficiently to switch them back to the PDR region. From the device point of view, larger oscillation amplitude means that more time is spent in the PDR region during each oscillation period, and hence a larger discrepancy between bias points of the individual diodes can be compensated for. Therefore, for larger amplitude oscillators, the excitation frequency can be further away from the oscillation frequency.

Since the required excitation power is more than 10 dB lower than the output power, a low power device such as a single RTD oscillator may be used as an external RF source. This kind of excitation is much easier to implement experimentally than excitation with a fast electrical pulse [7], [8]. At higher frequencies, quasi-optical techniques such as cross-polarization may be used instead of a circulator to separate the excitation and the oscillation signal [16].

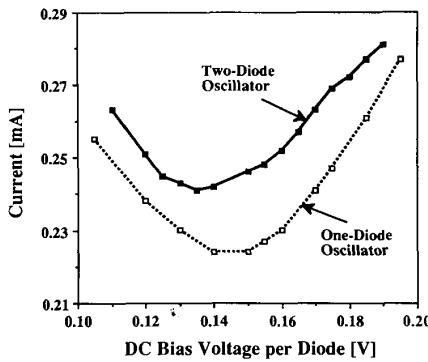


Fig. 5. Measured rectified I-V curve in the NDR region during oscillation, for two-diode oscillator 2D2 (solid line) and one-diode oscillator 1D2 (dotted line). For the two-diode oscillator voltage per diode is shown.

V. COMPARISON OF ONE- AND TWO-DIODE OSCILLATORS

One-diode oscillators were tested using the same experimental set-up. The measured output power agreed with the predicted values within 1.5 dB, and the oscillation frequency within 3.5% (Table I). Oscillator 1D1 was designed for maximum output power, determined using the procedure described in [13]. Theoretical dc to RF conversion efficiency for circuit 1D1 is 36.8%, whereas 28.2% was measured. The one-diode oscillator corresponding to 2D5 was not tested, because the diode impedance was too low to match to $50\ \Omega$ with a single-section quarter-wave transformer.

Two-diode oscillators produced 1–2 dB higher power than the corresponding one-diode oscillators. Due to the diode package there is a phase shift between the diodes, which degrades output power, and hence a full 3-dB increase in power cannot be achieved. Differences between the dc I-V curves of individual diodes also decreases output power. The length of the diode package was not accounted for in this design, and therefore the actual oscillation amplitude is probably somewhat larger (and output power lower) than predicted for the two-diode circuits.

The Q_{ext} was determined for all circuits using the injection-locking technique described in [14]. Higher oscillation amplitude circuits have higher Q_{ext} as expected. However, for one-diode oscillators, measured Q_{ext} is much higher than that predicted by X_d/R_d (Table I). There are several possible reasons for this discrepancy, such as inaccuracy in determining injection-locking power, a difference between designed and realized circuit impedance, and a transmission-line nature of the load.

For two-diode oscillators, using the same injection-locking formula [14], Q_{ext} appeared to be at least two times higher than that for the corresponding one-diode oscillators (their ratio, Q_R , is given in Table II). However, the device line for two-diode oscillators is limited by the oscillation amplitude cut-off, and hence the smaller observed lock-in frequency range (higher Q_{ext}) was probably the result of the shorter device line. Also, due to a difference between designed and realized impedance matching, two-diode oscillators may have higher oscillation amplitude than one-diode oscillators.

During oscillation, rectified I-V curves were measured in the NDR region for one-diode and two-diode oscillators. Rectified I-V curves for circuit 2D2 and the corresponding one diode oscillator 1D2 are shown in Fig. 5, with half of the voltage for the two diode oscillator. These two curves are very similar, which indicates that the two diodes are oscillating simultaneously. Measured rectified I-V curves do not follow the shape of the calculated one (Fig. 2), because during the measurement the oscillation amplitude varied as the dc bias voltage was changed.

Sideband noise was measured using a spectrum analyzer for all oscillators, and it was –94 to –98 dBc/Hz at 100 kHz away from the signal. No improvement in noise performance was observed for two-diode oscillators over one-diode oscillators, and the noise level did not depend on the oscillation amplitude.

VI. SUBHARMONIC EXCITATION

From the fundamental frequency excitation experiment, the oscillation frequency was determined for two-diode oscillators 2D2–2D5. A dc voltage sufficient to bias both diodes in the middle of the NDR region was applied, and excitation was attempted with two thirds, one half and one third of the oscillation frequency and lower. Subharmonic excitation was not possible for circuit 2D2, which was designed for the smallest oscillation amplitude. Circuits 2D3 and 2D4 had a similar behavior, with the lowest excitation frequency being one third of the oscillation frequency. For circuit 2D5, the lowest excitation frequency was below one sixth of the oscillation frequency, at 290 MHz with –3 dBm. At three fourths, four fifths and five sixths of the oscillation frequency, successful excitation was also observed for this circuit.

Fig. 6 shows the output spectrum during excitation with one third (Fig. 6(a)), one half (Fig. 6(b)), and two thirds (Fig. 6(c)) of the oscillation frequency, and the output spectrum after the excitation signal was turned-off (Fig. 6(d)) for circuit 2D3. The lowest usable excitation power for this circuit was –22 dBm for one third, –27 for one half and –19 dBm for two thirds of the oscillation frequency, which is 3 dB lower, 8 dB lower, and equal to the output power, respectively. During excitation with one third and one half of the oscillation frequency (with power levels given above), the oscillation signal was present, and its frequency and amplitude were the same as after the excitation signal was turned-off. During the excitation with two thirds of the oscillation frequency the oscillation signal was not present.

Similarly to fundamental frequency excitation, as oscillation amplitude increased excitation was possible in larger frequency bands around subharmonic frequencies. Shaded areas in Fig. 7 show the excitation frequency and power ranges for which 100% repeatable excitation was possible for circuits 2D3 (Fig. 7(a)) and 2D5 (Fig. 7(b)). For circuit 2D3, 100% repeatable excitation was possible in very narrow frequency bands, 20 MHz around one half, 10 MHz around one third, and 5 MHz around two thirds of the oscillation frequency. For circuit 2D5, these frequency bands were considerably wider, 60 MHz around one half, 110 MHz around one third, and 300 MHz around and above two thirds of the oscillation frequency.

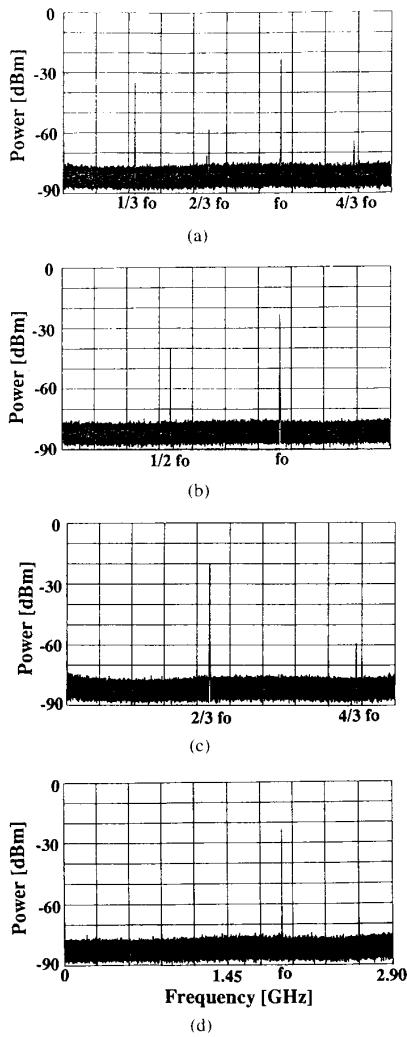


Fig. 6. Spectra during subharmonic excitation with (a) one third, (b) one half, and (c) two thirds of the oscillation frequency for circuit 2D3, and (d) spectrum of the generated signal. Incident powers are -22 , -27 , and -17 dBm, respectively, with output power -23 dBm, and 1.933 GHz. Actual output power is about 3 dB higher than shown, due to the losses in the experimental set-up. After excitation, bias voltage was slightly increased to maximize the output power.

Excitation was also possible in between these frequency bands for both circuits, but it was not 100% repeatable. Further away from the shaded areas, the probability of excitation was lower. For circuit 2D5, at frequencies in between 1.2 and 1.5 GHz it seemed that excitation bands around two thirds, three fourths, four fifths and five sixths of the oscillation frequency overlapped.

Strong power dependence of the excitation was observed for circuit 2D3 at one half and one third of the oscillation frequency (Fig. 7(a)). For low excitation power, oscillation was present and independent of the external RF signal during the excitation. For high excitation power, the oscillator was locked to the harmonic of the external RF signal during the excitation. For power in between the shaded areas excitation

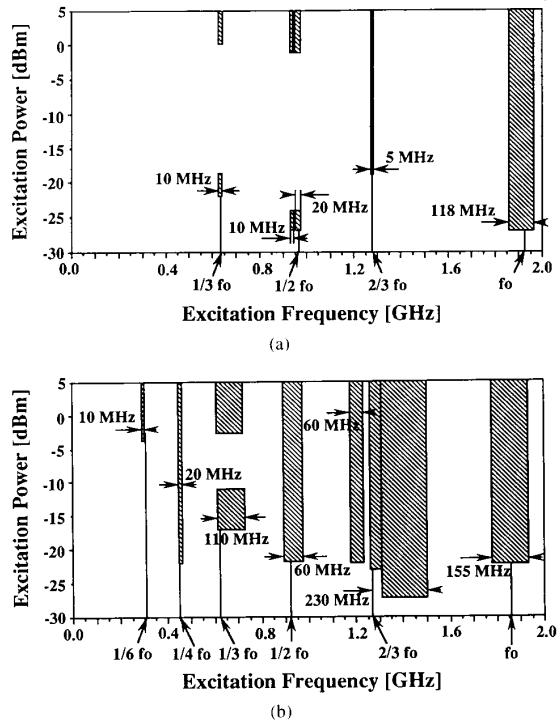


Fig. 7. Observed excitation frequency and power ranges (shaded areas) for 100% repeatable excitation for (a) circuits 2D3 and (b) 2D5. For circuit 2D3, f_o is 1.932 GHz, and for circuit 2D5, f_o is 1.865 GHz. For frequencies in between shaded areas excitation was possible, but it was not 100% repeatable.

was still possible, but it was not 100% repeatable. Further away from the shaded areas, the probability of excitation was lower. For circuit 2D5 power dependence was observed only at one third of the oscillation frequency (Fig. 7(b)), and excitation was not repeatable over a much smaller power range than for circuit 2D3. Similarly to fundamental frequency excitation, the larger oscillation amplitude circuit 2D5 required 5 dB higher minimum excitation power at one half and one third of the oscillation frequency than circuit 2D3. With one fourth of the oscillation frequency, 455 MHz, excitation was possible with low power, -22 dBm.

Due to the multi-frequency nature of subharmonic excitation, transient processes are more complicated than for fundamental frequency excitation. Therefore, more robust circuits having a larger oscillation amplitude are more likely to be successfully excited. The circuit designed for the highest output power (for the lowest oscillation amplitude above the amplitude cut-off level) required the lowest power excitation power for fundamental frequency excitation (2D2). However, subharmonic excitation was not possible for this circuit. If subharmonic excitation is required, some power has to be sacrificed for a larger oscillation amplitude. Therefore, there is a trade-off between the oscillator output power and the excitation frequency.

Subharmonic excitation may be a very useful way to initiate the oscillation at high frequencies, where signal sources are not readily available. The required power is not much higher than

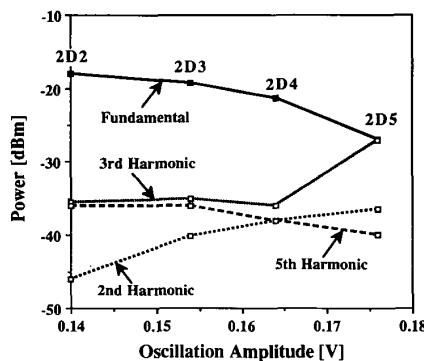


Fig. 8. Fundamental and harmonic power levels for oscillators 2D2–2D5, as a function of the oscillation amplitude. The fourth harmonic was not observed in any circuit, possibly due to the circulator loss.

that for fundamental frequency excitation. For circuit 2D3 the required power was 5 dB higher for excitation with one half of the oscillation frequency than for the fundamental frequency excitation, which is still 8 dB lower than the output power. At higher frequencies, quasi-optical filters may be used instead of a circulator to separate the excitation and the oscillation signal [17].

VII. HARMONIC GENERATION

For the dc bias point in the middle of the NDR region, the dc I–V curve of the tunnel diode appears to have odd symmetry. At large oscillation amplitudes, high nonlinearity is encountered, and consequently large harmonics are generated. Odd harmonics are expected to be larger than even harmonics, due to the odd symmetry of the I–V curve. In this experiment, the oscillator circuits were not optimized for harmonic generation, but large harmonics were still observed. Circulator loss was measured and accounted for, since harmonic frequencies were outside the circulator bandwidth of 1–3 GHz.

Harmonic levels for two-diode oscillators 2D2–2D5 are shown in Fig. 8, as a function of the oscillation amplitude. The fourth harmonic was not observed in any circuit, possibly due to the circulator loss. The third harmonic was stronger than the second in all circuits. Output power of the fifth harmonic was comparable to the third harmonic in circuits 2D2–2D4, and all harmonics were at least 15 dB lower in power than the fundamental. In circuit 2D5, the third harmonic was almost at the same power level as the fundamental. Maximum power for stable oscillation for two diodes in series (obtained for circuit 2D2) is only 9 dB higher than the power of the third harmonic in large amplitude oscillator 2D5.

Harmonic extraction may be useful for generating very high frequencies, in the terahertz range, if high frequency RTD's are used for the oscillator. If less than one sixth of the oscillation frequency is used for the excitation, and the third harmonic is extracted, a signal at almost twenty times the excitation frequency may be generated. If the RTD described in [18] is used, about 1 μ W can be obtained from a single diode at 400 GHz. The series integration scheme proposed in [7] (ten diodes integrated in series with the integrated device area increased

ten times as compared to the single diode area) may increase this power to 100 μ W. If the third harmonic is extracted, assuming that 10 dB less power than the fundamental can be obtained, 10 μ W at 1.2 THz may be generated. More power can be obtained by using quasi-optical power combining circuits such as a grid multiplier [19].

VIII. CONCLUSION

Connecting several tunneling diodes in series was shown to be a feasible method for increasing the output power of these devices as oscillators. The excitation of such an oscillator using an RF source was demonstrated in a proof-of-principle experiment, for a 2-GHz oscillator with two tunnel diodes connected in series. The excitation was successful both with excitation frequency close to as well as considerably lower than the oscillation frequency. Excitation with frequency as low as one sixth of the oscillation frequency was achieved. Very low power was required for both fundamental frequency excitation and excitation at one half of the oscillation frequency. For one circuit (2D3), the power required for fundamental excitation was 13 dB lower than the oscillator output power, whereas for excitation at one half of the oscillation frequency it was 8 dB lower than the oscillator output power. Excitation with one third of the oscillation frequency and lower required more power. Circuits that oscillate with larger amplitudes can be excited in broader frequency bands around subharmonics. Both fundamental and subharmonic excitation are much easier to implement experimentally than the alternative fast pulse excitation. Due to the highly nonlinear dc I–V curve of the tunnel diode, strong harmonics were generated in the circuit which oscillated with a very large amplitude. A third harmonic almost as strong as the fundamental was observed in that circuit. If high frequency series integrated RTD's are used for the active device, and the third harmonic is extracted, signal generation at terahertz frequencies may be possible.

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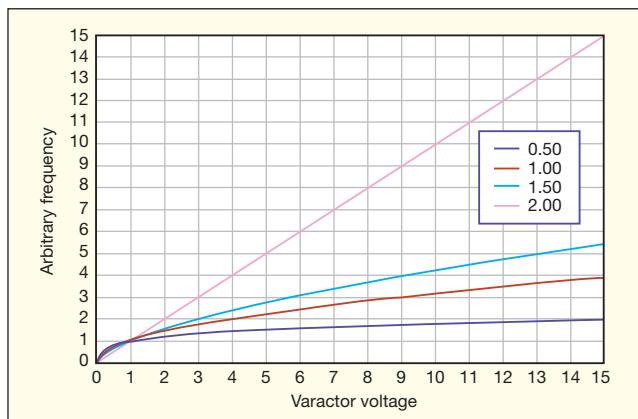
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Optimize Varactor-Tuned Oscillators

This simple model helps to understand the tuning sensitivity and linearity of a varactor diode for more predictable and precise tuning of oscillators at millimeter-wave frequencies.

MILLIMETER-WAVE FREQUENCY bands are attractive for their wide available bandwidths. There are a number of ways to generate these signals but, for each type of oscillator, it is desirable to be able to tune the source electronically, as well as in a defined, controlled, and consistent manner. By using a suitable reactive device (such as a varactor diode) for tuning these millimeter-wave oscillators, the relationship between an applied voltage and the resulting frequency can be precisely defined. This can aid the design engineer in achieving the required spectral performance at these higher frequencies.

Oscillators developed for use at millimeter-wave frequencies are typically designed around waveguide housings. Electronic tuning of a waveguide-type oscillator can be accomplished in a number of ways. Additional information can be found in the technical literature (ref. 1) and in a recent article (ref. 2). The tuning sensitivity of a millimeter-wave varactor-tuned oscillator (VTO) can be estimated by means of relatively simple models, and this article hopes to provide some sights into the tuning relationship. Usually, the approach is to keep the fixed capacity with the varactor diode as large as possible, using the varactor diode to control the resonant frequency to the greatest extent.



1. Frequency variations can occur due to variations in varactor diode voltage.

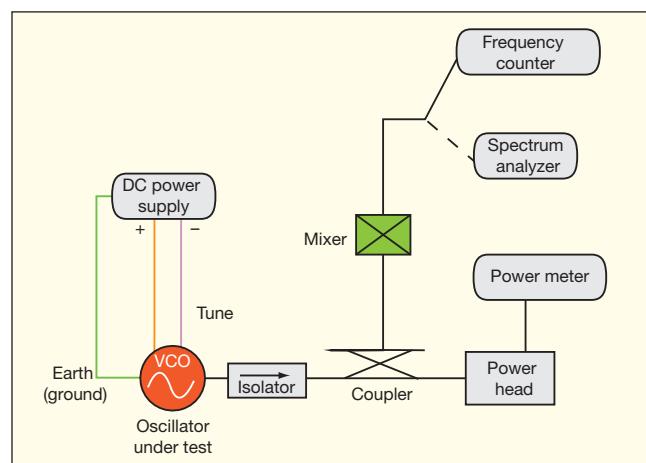
A varactor diode is essentially an active device with positive-negative (PN) junction which has reverse bias applied. This results in a movement of charge carried away from the junction, so that this region is referred to as the depletion layer. The depletion layer has charge on either side of the junction and acts like a parallel-plate capacitor. The capacitance relationship for a parallel-plate capacitor is $C = \epsilon A/W$, where:

A = the effective cross-sectional area of the device,
 ϵ = the relative dielectric constant of the depletion layer, and
 W = the width of the depletion layer.

Application of a voltage results in an increase of the depletion layer width, effectively altering the capacitance.

The typical fabrication process for a varactor diode results in a device with a mesa structure. This device can be mounted in a number of different standard and custom housings to simplify handling. The junction capacitance and associated parasitic circuit elements can be included in a simple equivalent circuit for modeling and simulation purposes.

The selection of a suitable semiconductor device for a varac-



2. This block diagram shows the instruments needed for the VCO test system.

tor diode can make an impact on the performance of the diode, although this receives little coverage in the literature. Varactors are true diodes with a clearly defined junction, which can be characterized by means of a particular doping profile; this is effectively captured in the gamma parameter for each varactor diode. The gamma parameter can be placed in two categories: abrupt and hyperabrupt. Quite simply, a varactor diode is effectively a variable reactance which is a function of some applied DC tuning voltage. More detailed models of varactor

diodes are available in the literature, which are useful for a specific package or unpackaged devices. To obtain a general understanding of a varactor diode's behavior, it would be reasonable to ignore packaging and parasitic affects in the first instance, as this allows the designer to appreciate the merits of such devices.

This basic approach leads to the following expression:

$$C_v + kV^{-\Gamma} \quad (1)$$

where:

V = control voltage;

k = a constant;

C_v = varactor capacitance; and

Γ = the gamma or doping profile.

For the case where the circuit capacitance is much greater than the varactor capacitance, or if $C_d \ll C_v$:

$$F \approx (L/C_v)^{0.5} \rightarrow F = K/(C_v)^{0.5} \quad (2)$$

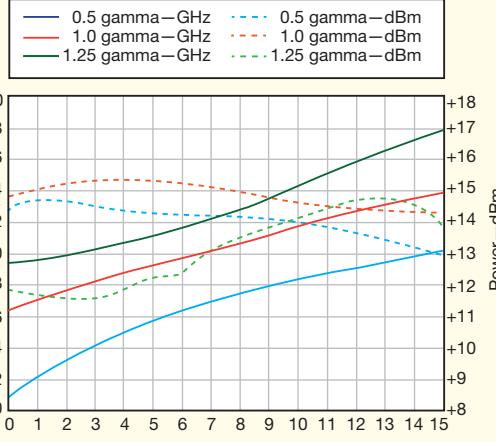
where:

F = the resonant frequency;

L = the circuit inductance; and

K = a constant.

Combining Eqs. 1 and 2 yields an expression that represents a relationship



3. These curves show the changes in frequency for different applied varactor voltages.

between frequency and voltage:

$$F = K/[k(V)^\Gamma] \rightarrow \approx V^{\Gamma/2}$$

in which the importance of the varactor material's doping profile can be clearly seen on both sides of the equation.

This very simplistic approach provides a basic relationship between frequency and the applied voltage, with Γ representing a doping constant, equal to 0.5 for an abrupt diode and 1.0 or 1.25 for a hyperabrupt diode:

$$\Gamma = 0.5 \rightarrow F \approx V^{0.25}$$

$$\Gamma = 1.0 \rightarrow F \approx V^{0.50}$$

$$\Gamma = 2.0 \rightarrow F \approx V$$

In reality, it is difficult to achieve a practical diode capable of $\Gamma = 2.0$, although devices with values equal to 1.0 and 1.25 are commercially available.

A more detailed analysis³ of a varactor's influence on frequency tuning can be complicated. This is due to the issues of the varactor construction and device to device variation, as can be seen in Fig. 1. Package assembly and parasitic circuit elements can have profound effects at high frequencies in particular the type and shape of the internal bond wires. For this analysis, a number of commercially available packaged varactor diodes were procured and installed into a W-band

Gunn oscillator to compare performance levels.

Each varactor/oscillator combination was evaluated with a test system that included a DC power supply for tuning the varactors (Fig. 2). The output of the Gunn oscillator in each case was monitored with the aid of high-frequency test instruments that included a frequency counter, spectrum analyzer, and power meter. A frequency mixer was used to translate the Gunn oscillator's outputs to frequencies within range of the test equipment.

Although the varactor package type was the same in each case, each device package had its own subtle differences in dimensions as well as in internal construction, with ramifications at the higher frequencies. Difference between sources can occur because of variations in reactance and skin effect due to fringing fields, the lengths of current paths, and various parasitic effects. No serious efforts were made to optimize the circuit, particularly for power. Measured performance is shown in Fig. 3.

The crude model and measured data demonstrate that the tuning sensitivity (and thus, linearity) can be influenced significantly by the selection of a suitable varactor diode. This also opens the possibility of tailoring the doping profile of the varactor diode to achieve a specific tuning sensitivity; this could be achieved during the semiconductor fabrication process. However, in practice, linear tuning must take into account circuit and oscillator characteristics as well as the varactor diode. MWRF

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Large Signal GaAs MESFET Oscillator Design

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Abstract—Techniques for large signal GaAs MESFET oscillator design are described which do not require repeated large signal measurements. In the first technique, small signal S -parameter measurements are used with a computer program to compute the packaged and mounted device equivalent circuit. Large signal measurements are made to determine a mathematical relationship between only those parameters which vary under large signal conditions. These relationships are included in the computer program. Then, once the equivalent circuit has been computed from the small signal S -parameter measurements, those parameters varying under large signals are incrementally altered until large signal S parameters are obtained which correspond to maximum oscillator output power. These values are used to calculate embedding element values for six oscillator topologies. A coaxial cavity FET oscillator was built and tested using the large signal design theory, and it substantially verified the design technique.

The second design technique is based on the fact that S_{21} varied more than other S parameters under large signals. By making design calculations based on S_{21} reduced to the point corresponding to maximum oscillator power, it was possible to get usable design information for an FET oscillator.

I. INTRODUCTION

LARGE SIGNAL amplifier and oscillator design has always been a somewhat difficult procedure, generally requiring extensive large signal measurements. Recently, an article by Vehovec, Houslander, and Spence [1] appeared, discussing a method of two-port device oscillator design that maximizes the output power. This method, based on known device Y parameters, resulted in linear equations for the embedding elements, with the only assumption being that the voltages are nearly sinusoidal. This requires either or both of the following conditions: 1) that the nonlinearity be of a small degree, or 2) that the embedding network satisfy Aiserman's [2] filter hypothesis. The nonlinearity of a GaAs MESFET is quite small, as evidenced by its large dynamic range and large third-order intercept in an amplifier. Thus the GaAs FET is well suited to the type of analysis used by Vehovec.

More recently, Kotzebue and Parrish [3] extended the work of Vehovec and derived a set of closed form solutions for the embedding elements of three series-type oscillators and three shunt-type oscillators. Kotzebue [4]–[6] developed a technique for large signal Y -parameter measurements at microwave frequencies, and successfully used them in large signal amplifier design. The advantage

of Y -parameter measurements is that they are measured with a short-circuited input or output; hence, there is no uncertainty as to the magnitude of the output voltage, as there is in large signal S -parameter measurements.

The difficulty with large signal Y -parameter measurements is that it is very difficult to obtain a good RF short circuit at the device terminals, particularly at microwave frequencies. While Kotzebue described a technique for making these measurements, they are not particularly easy, since no large signal measurements, either S or Y parameter, are particularly "easy" for the amplifier designer who would prefer to use data supplied by the manufacturer. S -parameter measurements are more readily accomplished than Y , but there is still the uncertainty of the input signal level relative to the output. Furthermore, harmonic effects further render measurements uncertain.

In spite of these limitations, Leighton *et al.* [7] were able to design successfully a large signal amplifier based on large signal S -parameter measurements. Maeda *et al.* [8] obtained meaningful oscillator design data at least for the oscillation frequency based on small signal S -parameter measurements. Besser [9] also obtained meaningful design information based on small signal measurements. More recently, Mitsui *et al.* [10] developed a MESFET oscillator design method using large signal S parameters. They obtained good agreement between measured and predicted performances of an MIC oscillator. Finally, the work of Gonda [11] should be mentioned in which he obtained design data from measurements of a partially built oscillator viewed as a one-port device.

In this paper two alternative approaches to large signal FET oscillator design will be described which do not require repeated large signal device measurements, but which are based upon large signal measurements.

II. THEORETICAL STUDY

A. Design Approaches

The first approach, which is described in detail in the remainder of this paper, is as follows. For the FET device to be used, small signal S -parameter measurements are made at several frequencies (or the data are obtained from the manufacturer). The S parameters measured, along with estimated device equivalent circuit values including package parasitic elements, are then inputted to a com-

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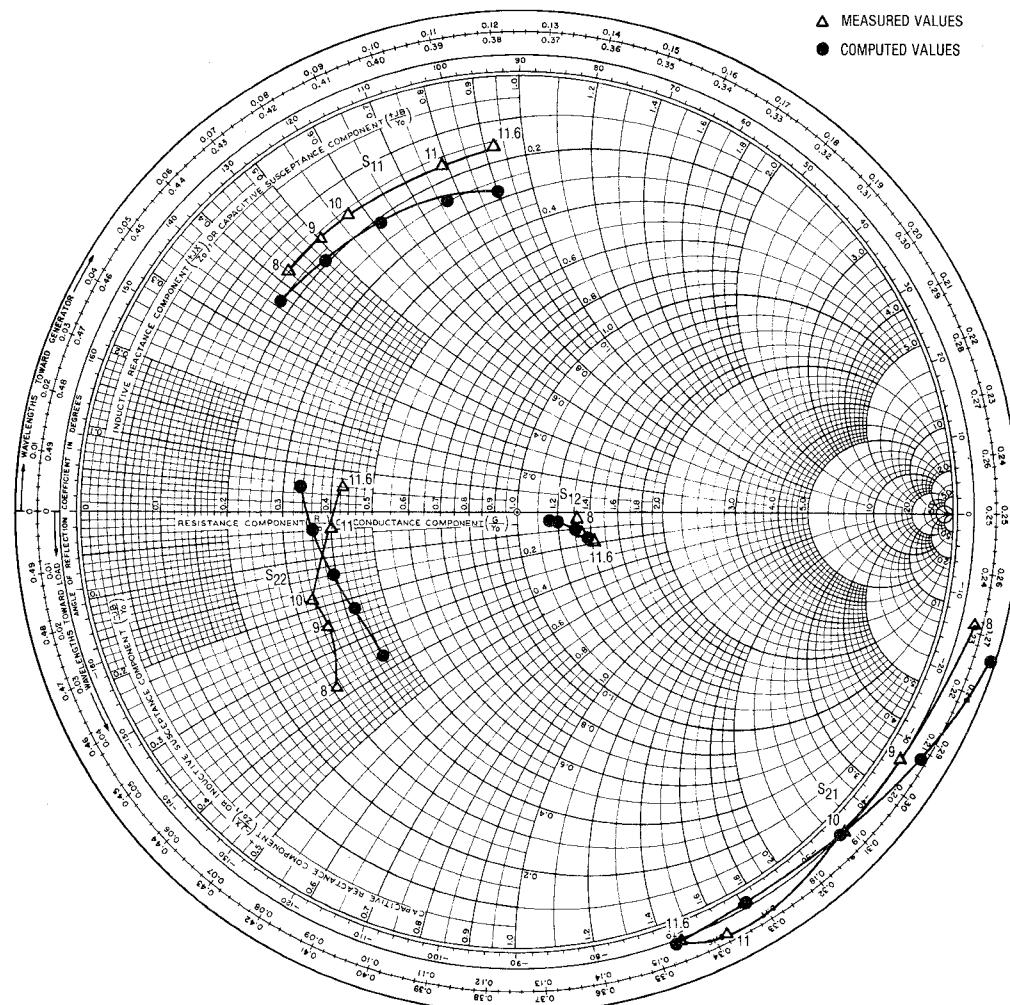


Fig. 1. GaAs FET computed and measured S parameters.

puter optimization program such as the one described by Vendelin and Omori [12]. The computer program is designed to match the measured S parameters to the S parameters computed for the device from its equivalent circuit. The computer output gives the computed S parameters, which match the inputted parameters, plus the equivalent circuit values for the active FET device and the package parasitics.

The next step, carried out by the computer, is to vary in a previously defined manner those elements of the equivalent circuit which vary under large signals. The argument here is that only a few of the equivalent circuit elements vary under large signals. Hence, it should be possible to determine which elements do vary significantly and to develop some mathematical relationship between the variable elements. Once having determined the elements which vary under large signals and their relative changes as the signal level increases, these relationships may be included permanently in the computer program. The computer, after computing the small signal equivalent circuit values, then incrementally alters only those elements which vary under large signals, and at each increment

recomputes the new set of S parameters and the corresponding two-port gain. These parameters are large signal parameters.

As the variable elements are further altered, the computed two-port gain decreases, representing the saturation effect of the device. The point on the saturation characteristic that is sought is the point of maximum power-added efficiency, which corresponds to the point of maximum oscillator power output. This, for an FET, may be closely related to the device small signal gain, as done by Pucel, Bera, and Masse [13]. At this point of maximum oscillator power out, the computer prints out the large signal S parameters. It is these S parameters which are used for large signal oscillator or amplifier design. From these parameters, impedance values for amplifier conjugate match may be determined using well-known design equations for small signal amplifiers when maximum gain is desired [14], or those developed by Kotzebue when maximum added power is desired [15]. Impedance embedding elements may also be computed for six oscillator configurations using the equations developed by Kotzebue and Parrish [3].

Less complicated than the previous approach, and consequently less accurate, is the second design approach which may be preferred since the somewhat lengthy computer program required for the first approach, and the necessary information for providing the starting point circuit element values to the computer, may not be available.

In the second approach, advantage is taken of the fact that under large signals, the magnitude of S_{21} varies much more than any other S parameter, a fact verified by large signal measurements. The simplified design approach assumes, then, that all of the S parameters except the magnitude of S_{21} are constant under large signals. The large signal magnitude of S_{21} is reduced, as before, to that value which corresponds to the maximum oscillator output power. The results obtained using this approach compare favorably with those obtained using the more complicated approach, at least for the transistors used in this study.

This summarizes the design approaches. It is, of course, necessary in the first approach to accurately measure large signal characteristics at some time, and to determine the relationship between variable parameters for the FET device. It is probably not necessary, however, to compute new relationships for each FET, since it is unlikely that the important variable parameters would be different for each device unless there had been significant process differences between device types.

B. Device Measurements

The device chosen for this study is an X-band GaAs MESFET which, when operated as an amplifier, is rated at 250-mW output at 10 GHz. The device is a one-cell geometry essentially the same as that described by Macksey *et al.* [15]. It has a gate width of 600 μm , with a gate length of about 1.2 μm . The device is packaged in the minicoax package in which the source is bonded to the ring of the package; the gate is bonded to the stud, and the drain is connected to the lid. This package is particularly well suited to oscillator application.

Small signal measurements of the FET were made first, to provide inputs to the computer program. The measurements were made using the Hewlett-Packard 8410 network analyzer system. The device was mounted on a coaxial test fixture with a thin metal ring making contact with the ring of the package for a grounded source configuration. The results for small signal measurements, from 8 to 12 GHz, are shown in Fig. 1. Also shown are the computed S parameters for the device, which will be described later.

Large signal S parameters were also measured, but because the network analyzer could not operate with power levels up to 400 mW, measurements were made using the setup shown in Fig. 2. Since this is a fairly standard technique, it will not be described in detail. Here the magnitudes of S_{12} and S_{21} were measured, as shown in

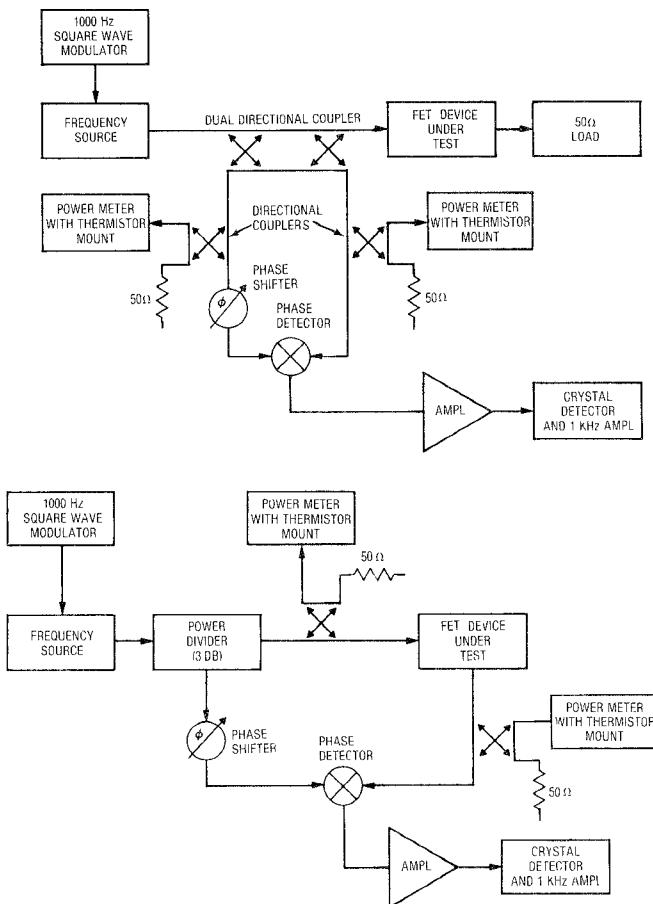


Fig. 2. S -parameter measurement test setup.

Fig. 2(b), by measuring the power loss or gain through the device using calibrated directional couplers. For phase measurements, a phase shifter was placed in the line, and the input and output waves were summed in a mixer. The phase shifter was adjusted to give a minimum signal from the mixer corresponding to 180° phase cancellation. When the device was inserted, the phase difference was measured using a calibrated precision phase shifter. The difference in phase is the phase of S_{12} or S_{21} , depending on which direction the device is inserted. S_{11} and S_{22} were measured similarly using the setup of Fig. 2(a) or the standard slotted line technique.

The results for the large signal S -parameter measurements at 10 GHz are shown in Fig. 3, in which the incident power is varied from 100 to 400 mW. Bias voltages were held constant in these measurements. If there were no changes in the S parameters when the power level was increased, and if there were no changes in dc current due to rectification, the signal level was considered small. Small signal levels were below 100 mW for both input and output.

The question may be raised as to how meaningful these measurements are, since the voltage levels on input and output will differ from those in the measurements. A number of observations may be made in answer to this,

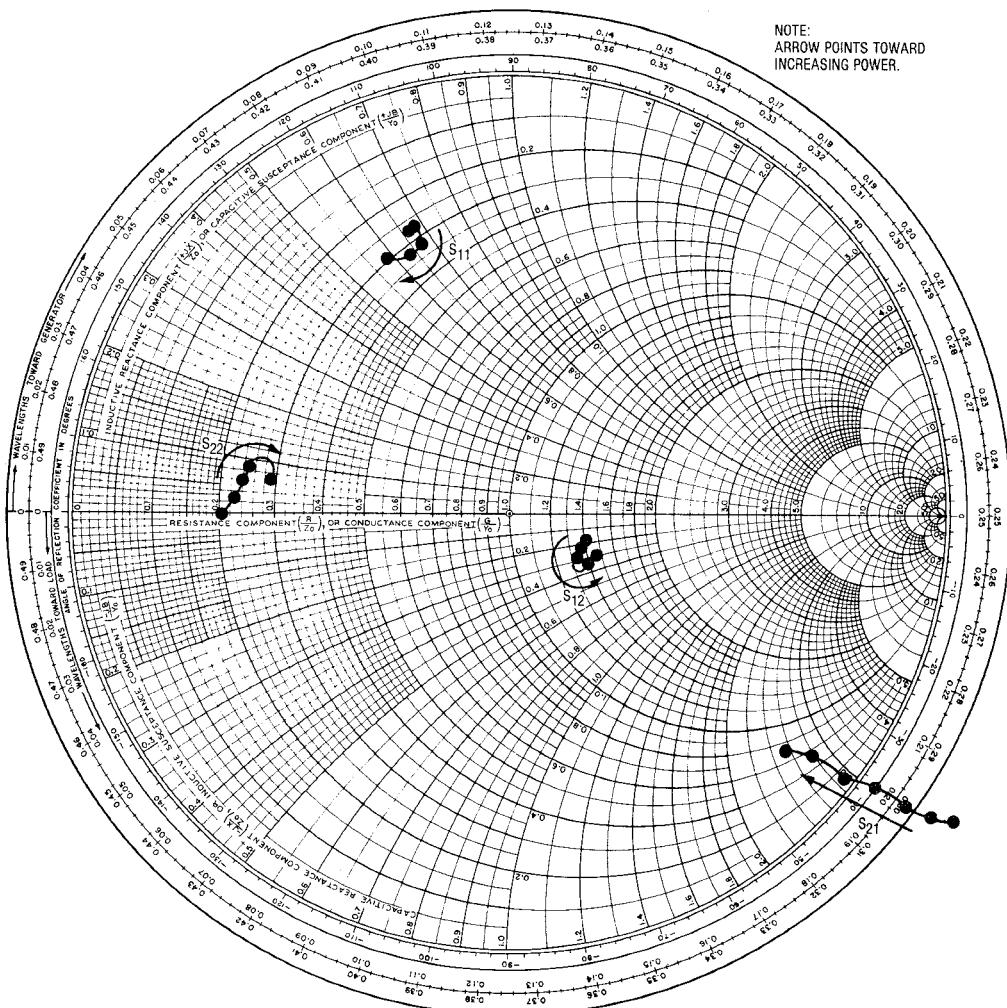


Fig. 3. GaAs FET large signal S -parameter measurements at 10 GHz.

which apply at least to the FET. First, as pointed out before, some meaningful design information was obtained even on the basis of small signal measurements. In particular, Maeda found that small signal measurements were adequate to predict frequency. This suggests that large signal effects produce primarily resistive changes. Second, Fig. 3 shows that the magnitude of S_{21} changes with power much more than do the other parameters. Since S_{21} is strongly influenced by the device transconductance g_m , it may be inferred that the changes in g_m under large signals are a predominant factor. In that case, if the relative changes in the other parameters are somewhat in error due to differing voltages on input and output, the final effect would be relatively small. Finally, since the magnitude of S -parameter changes were measured to power levels greater than those corresponding to maximum oscillation power, the S -parameter changes for an oscillator would not reach the maximum changes shown in Fig. 3. Maximum oscillation power was 100 mW while the measurements were made, with up to 400 mW incident on the device. It was concluded, then, that even though there is some error in the large signal S -parameter

measurements, it should not appreciably affect the computation of oscillator and amplifier embedding elements.

At this point, it will be shown how large signal measurements were used to predict the changes in equivalent circuit parameters under large signal conditions. Then, the series of mathematical relationships showing the large signal changes in the circuit parameters will be described for the FET studied. First, the device equivalent circuit will be considered.

C. Device Equivalent Circuit

The equivalent circuit used for the FET chip was that suggested by Vendelin and Omori [16]. This equivalent circuit is shown in Fig. 4 in the dotted portion, excluding bonding inductances. Outside of the dotted portion, the package parasitic elements and circuit coupling elements are given. The inductances L_G , L_D , and L_S represent the bonding wire inductances. In the minicoax package, with the FET chip located on the gate stud, L_G would be quite small, representing only the post inductance inside the package. The capacitances G_{GS} , C_{DS} , and C_{GD} represent the package parasitic capacitance plus some coupling

capacitance to the coax line. In the common source minicoax package, C_{GD} would be extremely small, representing the capacitance inside the package between the gate stud and drain stud. Finally, L_{GC} , L_{SC} , and L_{DC} are the coupling inductances to the coax line. To get some idea of the magnitude of these parasitics, the measurements by Monroe [17] of diode packages were used. The parasitics of the minicoax package were estimated from his measurements to provide initial values for the computer program. Initial values for other chip parameters were estimated from information supplied by the manufacturer, and from data in the paper by Vendelin and Omori [12].

In the equivalent circuit of Fig. 4, none of the parasitic parameters will vary under large signal conditions. Of the chip parameters, only the transit time τ_0 would be constant under large signals since it is a function of device geometry. By the same token, it might be expected that the contact resistances would not be affected by large signals. However, when the FET begins to saturate, energy is converted to harmonic frequencies. This energy is dissipated in device and load resistances and, to a first approximation, appears to the equivalent circuit as if the resistive losses increased. Hence, they were included as, at least, potential variables under large signals.

D. Computer Optimization Program

A computer program was written which takes equivalent circuit initial parameter values and computes a new set of S parameters S_{cy} . These are compared with the inputted set of measured S parameters S_{Mij} , and an error function generated as done by Vendelin and Omori [12]:

$$\text{E.F.} = \sum_{F=F_1}^{F_N} \left\{ W_1 |S_{M11} - S_{c11}|^2 + W_2 |S_{M12} - S_{c12}|^2 + W_3 |S_{M21} - S_{c21}|^2 + W_4 |S_{M22} - S_{c22}|^2 \right\} \quad (1)$$

where F_1 is the initial frequency, F_N is the final frequency, and W_i represents the weighting given to each set of S parameters. Measured S parameters for each frequency are stored in a file. The computed parameters are also stored, but continually change as the computed values get closer to the measured values.

In the optimization routine, selected parameters are varied randomly using a random number generator. The S parameters and error function are computed, and the error is compared with the initial error. If the error is greater than the previous error computed, the parameters again are varied until a smaller error is computed. The "initial" circuit parameters are then reinitialized to the new value, and the parameters are again randomly varied. This procedure continues until some specified maximum number of comparisons is made, or until some maximum error is reached. The program then outputs the computed S parameters and circuit element values.

A table of computed equivalent circuit values is given

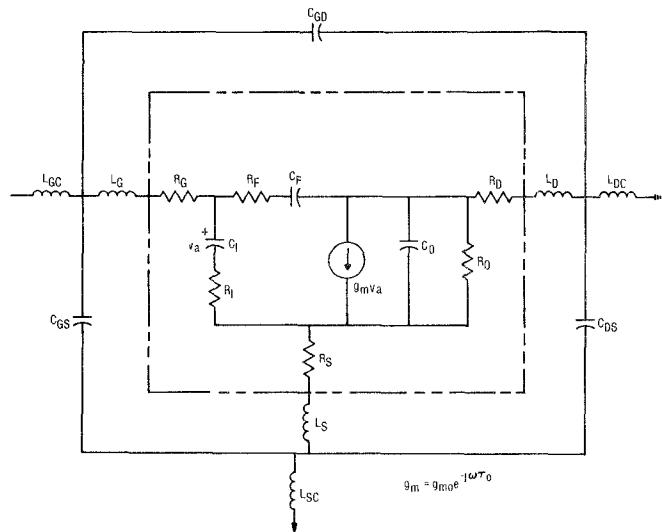


Fig. 4. FET equivalent circuit including package and mounting parasitics.

in column 1 of Table I for the FET used in this study. The next step taken was to input the measured large signal S parameters at a couple of power levels, while holding constant the parasitic elements and τ_0 . This meant that seven parameters were varied. It was found that R_F , C_F , and C_I could also be held constant with little increase in the error. The equivalent circuit values, which were computed for +24- and +26-dBm power levels, are shown in columns 2 and 3 of Table I. From these values, a tentative relationship between the relative changes in parameters was established.

The only parameter which caused difficulty was R_O . The reason for this is apparent in Fig. 3 where it may be seen that at power levels greater than +24 dBm, S_{22} abruptly changes. Below this point the changes are approximately linear with increasing power in dBm, as they are with S_{21} . Gain calculations based on S parameters measured at +26 dBm show that the gain would be only 0.87 dB. Hence, the +26-dBm level is too far into saturation. With this limitation in accuracy, approximate proportional relationships between the parameters were found to be the following:

$$\begin{aligned} R_I &\propto g_m^{-1.3} \\ R_O &\propto g_m^{0.7} \\ C_0 &\propto g_m^{-0.7}. \end{aligned} \quad (2)$$

In order to compute the large signal parameters at maximum oscillation power, the small signal equivalent circuit parameters were established by the computer optimization program as described. Then, the g_m was decreased incrementally, with the other parameters varied in accordance with the relationships of (2). At each incremental reduction in g_m , the S parameters were recomputed along with the gain. If one were interested in the 1-dB compression point, the S parameters used would be those at that point. For oscillation or large signal amplifier

TABLE I
FET COMPUTED SMALL AND LARGE SIGNAL EQUIVALENT CIRCUIT PARAMETER VALUES

FET EQUIVALENT CIRCUIT	(1)	(2)	(3)	(4)
	SMALL SIGNAL	+26 dBm	+24 dBm	+24 dBm
LS = Source Parasitic Inductance(H)=	0.200E-09			
LD = Parasitic Inductance(H)=	0.720E-09			
LG = Gate Parasitic Inductance(H)	0.133E-09			
CGS = Gate to Source Parasitic Cap(F)=	0.374E-12			
CGD = Gate to Drain Parasitic Cap(F)=	0.000E 00			
CDS = Drain to Source Parasitic Cap(F)=	0.321E-12			
RI = Gate to Source in Res.(Ohms)=	0.444E 01	7.31	6.28	6.33
CI = Input Capacitance(Farads)=	0.104E-11	0.928E-12	1.06E-11	
CF = Feedback Capacitance(Farads)=	0.416E-13	0.57E-13	0.728E-13	
RO = Output Resistance(Ohms)=	0.602E 03	296.	394.	491.
CO = Output Capacitance(Farads)=	0.420E-13	0.608E-13	0.581E-13	0.483E-13
RF = Feedback Resistance(Ohms)=	0.207E 03	438.	399.	
GMO = Low Freq Transconductance(Mhos)=	0.235E-01	0.0152	0.0193	0.0181
TO = Delay Time (Sec)=	0.741E-11			
LCS = Source Coupling Inductance(H)=	0.000E 00			
LCD = Drain Coupling Inductance(H)=	0.624E-09			
LCG = Gate Coupling Inductance(H)=	0.415E-09			
RS = Source Resistance(Ohms)=	0.164E 01			
RD = Drain Resistance(Ohms)=	0.523E 00			
RG = Gate Resistance(Ohms)=	0.825E 00			

application, the point of maximum power added gain is of interest. This corresponds to the point of maximum oscillator power, which will now be determined.

E. Maximum Oscillator Power

Pucel *et al.* [13] point out that the power-gain saturation characteristic of a FET power amplifier may be approximated by an equation of the form

$$P_0 \approx \frac{G_0 P_{\text{IN}}}{1 + G_0 P_{\text{IN}} / P_{\text{sat}}} \quad (3)$$

where G_0 is the small signal gain and P_{sat} is the saturated output power as an amplifier. The amplifier is tuned for maximum efficient gain G_{ME} at each input power level. Maximum efficient gain is defined by Kotzebue as the power gain which maximizes the two-port added power, i.e., where

$$\frac{P_{\text{out}} - P_{\text{IN}}}{P_{\text{IN}}} = \text{maximum.} \quad (4)$$

In terms of S parameters, this is given as

$$G_{\text{ME}} = \frac{\left| \frac{S_{21}}{S_{12}} \right|^2 - 1}{2 \left\{ K \left| \frac{S_{21}}{S_{12}} \right| - 1 \right\}} \quad (5)$$

$$K = \frac{1 + |S_{11}S_{22} - S_{21}S_{12}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} \quad (6)$$

where K is the Rollett stability factor. Then, the input and output reflection coefficients Γ_{IN} and Γ_{OUT} , respectively,

are

$$\Gamma_{\text{IN}} = \left[S_{11} + \frac{S_{21}S_{12}\Gamma_{\text{out}}}{1 - S_{22}\Gamma_{\text{out}}} \right]^* \quad (7)$$

$$\Gamma_{\text{OUT}} = \left[S_{22} - \frac{S_{12}S_{21}}{1 + S_{11}} \right]^*. \quad (8)$$

The use of G_{ME} is particularly well suited to large signal amplifier design.

A typical amplifier power saturation characteristic for a 1-W device is shown in Fig. 5. The maximum oscillator power occurs at the point of maximum ($P_{\text{out}} - P_{\text{in}}$), or where $\partial P_{\text{out}} / \partial P_{\text{in}} = 1$. A better approximation to this curve than given by (3) is the exponential form

$$P_{\text{out}} \approx P_{\text{sat}} \left[1 - \exp \left(\frac{-G_0 P_{\text{IN}}}{P_{\text{sat}}} \right) \right]. \quad (9)$$

From this, the point of maximum oscillator power may be computed:

$$P_{\text{osc(max)}} = P_{\text{sat}} \left[1 - \frac{1}{G_0} - \frac{\ln G_0}{G_0} \right] \quad (10)$$

and the maximum efficient gain G_{ME} , therefore, is

$$G_{\text{ME}}(\text{max oscillator power}) = \frac{G_0 - 1}{\ln G_0}. \quad (11)$$

Thus for example, an FET having a small signal $G_{\text{ME}} = 7.5$ dB with a saturated amplifier output power of 1 W would be capable of a maximum oscillator power of 515 mW. The maximum gain at this point is 4.3 dB.

The gain expression of (11) was used to determine at what gain level the large signal S parameters were to be

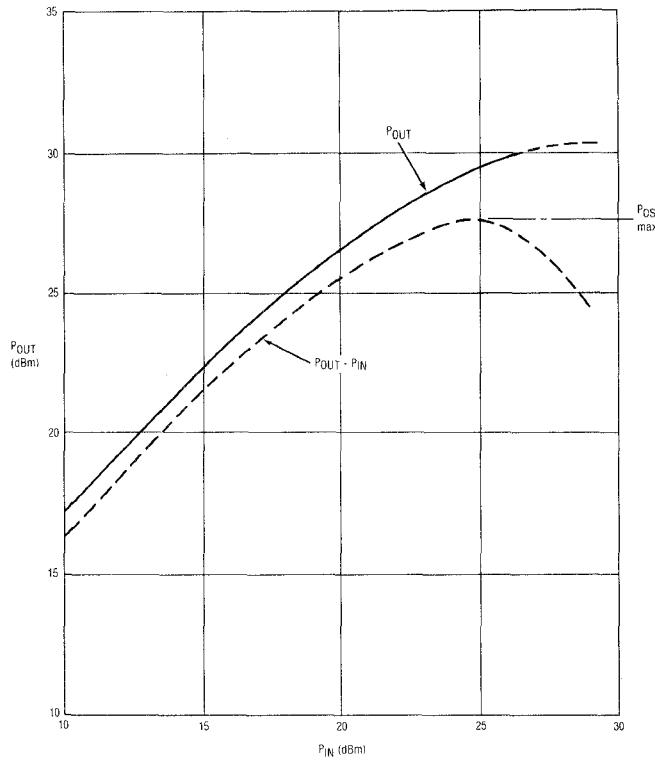


Fig. 5. Gain saturation characteristic on a 1-W FET power amplifier.

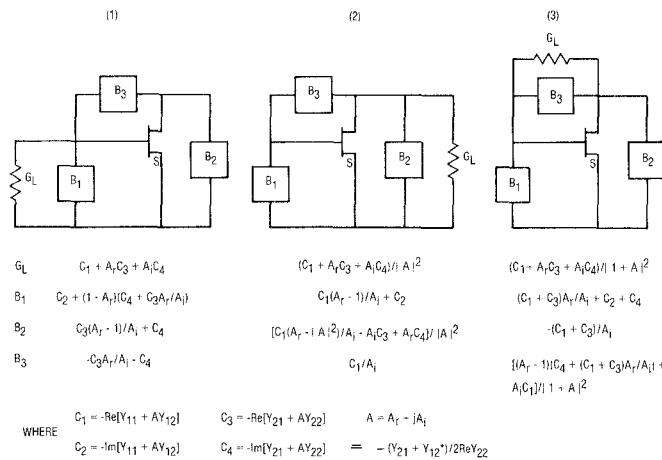


Fig. 6. Optimum embedded elements for three shunt oscillators (from Kotzebue and Parrish [3]).

used for oscillator application. Notice that it is not necessary to know the saturated output power of the transistor. All that is needed is a measurement of *S* parameters at a number of frequencies. Normally, these are available from the transistor manufacturer.

F. Oscillator Circuit Design

Having computed the large signal *S* parameters following the procedure outlined before, the embedding elements for six oscillator topologies may be computed [3]. Three shunt oscillator configurations with the design equations for the optimum embedding elements are given

in Fig. 6, and three series oscillator configurations are given in Fig. 7. Design equations are given in terms of *Y* and *Z* parameters in the figures which may be readily transformed to *S* parameters by the usual *S* to *Y* and *Z* conversion formulas. It may be added that there are, of course, other possible configurations consisting of series and shunt element combinations, but of these six, generally one or more will result in a practical design.

For the transistor which was measured, the six oscillator circuits embedding element values are given in Fig. 8. Not all of these circuit configurations can be readily realized in practice. In particular, all of the shunt oscillator config-

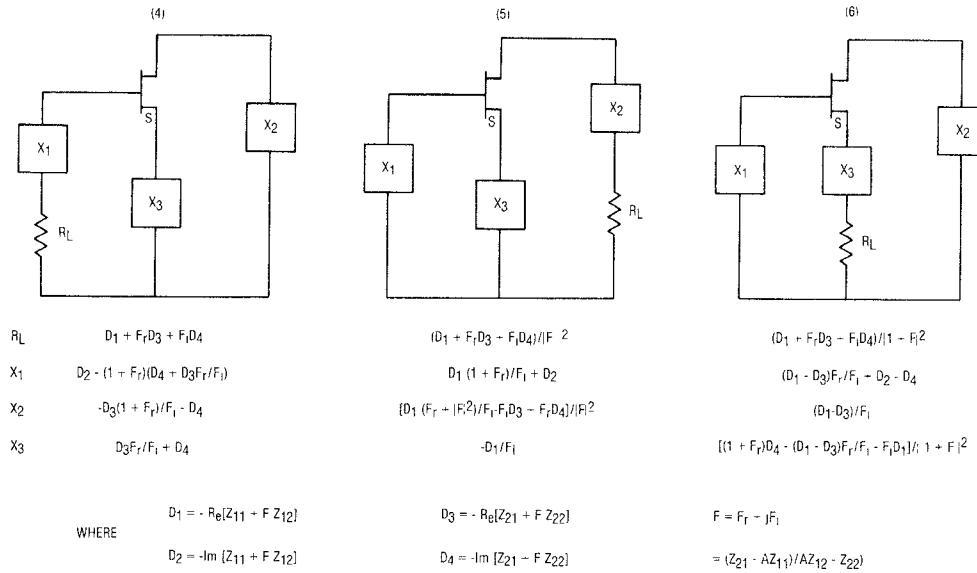


Fig. 7. Optimum embedding elements for three series oscillators (from Kotzebue and Parish [3]).

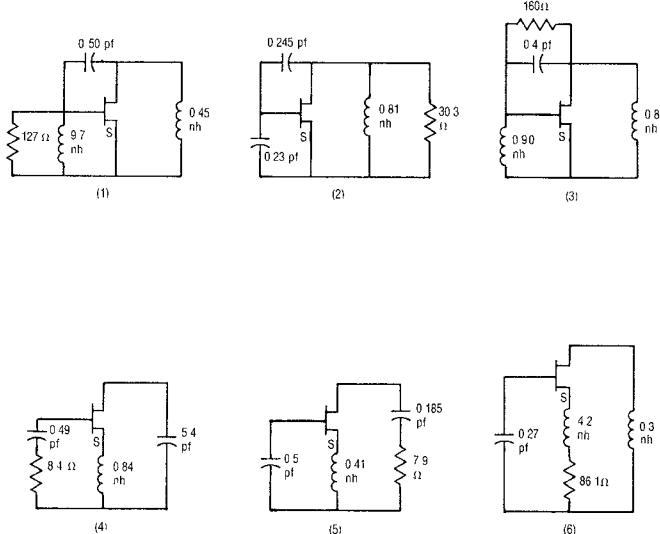


Fig. 8. Computed values of embedding elements for FET oscillator, MSX801G FET device. (a) Values for three shunt oscillators. (b) Values for three series oscillators.

urations are difficult to realize with a coax packaged device. This is due to the fact that there is no easy way physically to locate a capacitor between the gate and drain since the source ring gets in the way. The series circuits are more amenable to fabrication, particularly circuit 4 of Fig. 8. Since it is of interest to know how critical the embedding element values are as a function of signal level, Fig. 9 gives a plot of these element values as a function of two-port maximum efficient gain. Small signal levels correspond to a gain of 5.7 dB while the gain at maximum oscillator power is 3.0 dB. The figure shows that there is a significant change in oscillator embedding element values for small and large signal conditions. Likewise, Fig. 10 is a plot of embedding element values as a

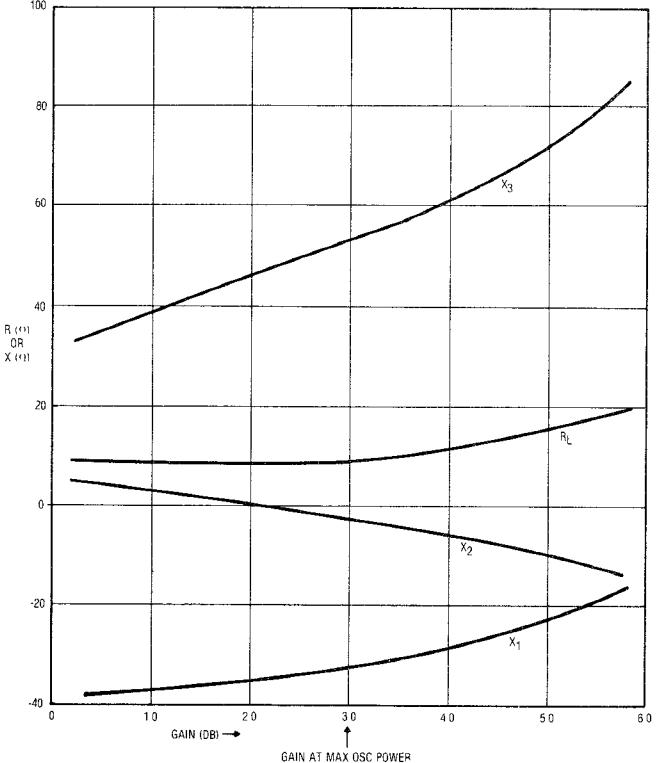


Fig. 9. Plot of computed optimum oscillator embedding elements as a function of two-port gain for circuit 4 at 10 GHz.

function of frequency for circuit 4. Again, it may be seen that the values do vary considerably with frequency.

G. Experimental Results

The oscillator which was designed and built to verify the theory was the series configuration, circuit 4 of Fig. 8. A coaxial realization of this circuit is shown in Fig. 11. The inductance from the source lead was provided by a

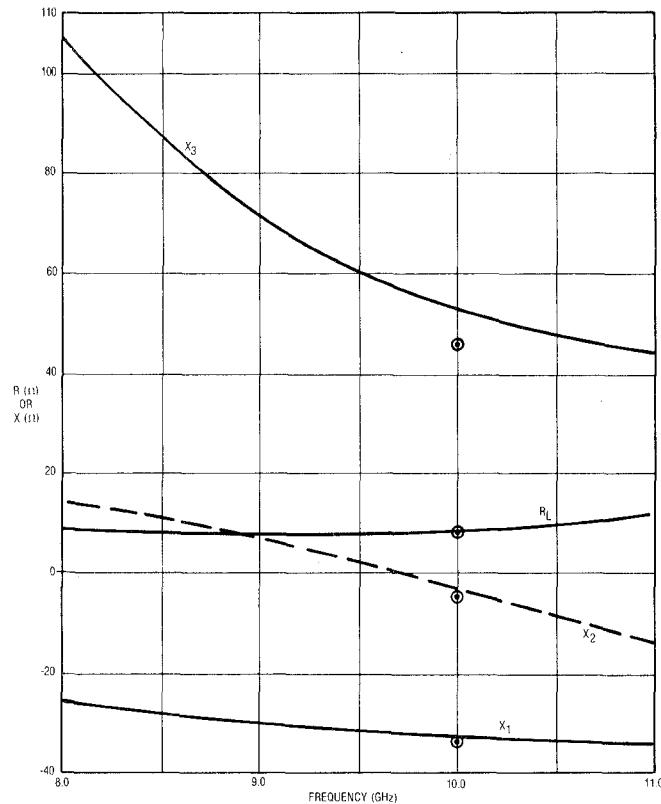


Fig. 10. Plot of optimum oscillator embedding elements as a function of frequency for circuit 4 at optimum power out.

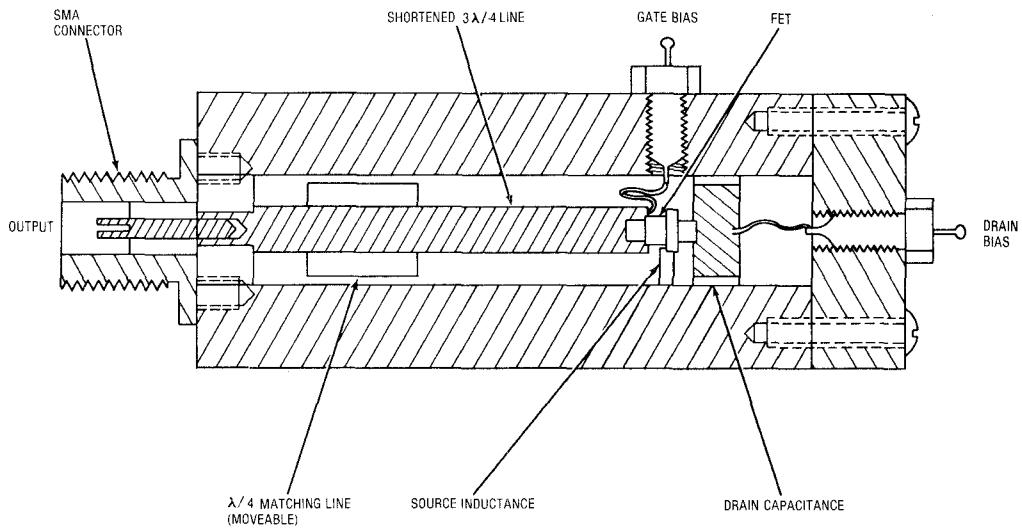


Fig. 11. Coaxial circuit FET oscillator. Realization of series oscillator configuration (4).

short length of line to the outer conductor wall of the oscillator cavity. Unfortunately, the exact size of this line was difficult to compute due to stray reactances in the shunt mounting of the short rod. The capacitance in series with the drain was obtained by use of a short length of low impedance line as shown. The series capacitance and load inductance were obtained by transforming down a shortened $\lambda/2$ 50- Ω line to a point of zero reactance, and

using a $\lambda/4$ transformer to provide the correct series resistive loading at the FET of 8.9Ω . In this circuit, the quarter-wave transformer was made movable to test the tunability of this circuit. The $\lambda/2$ line was used to increase the unloaded Q of the circuit. Since the source was grounded to the wall of the cavity, it was necessary to use a dc block on the output which is not shown in Fig. 11. Anticipated output power was $P_0 = 0.38 P_{\text{sat}}$, and, since

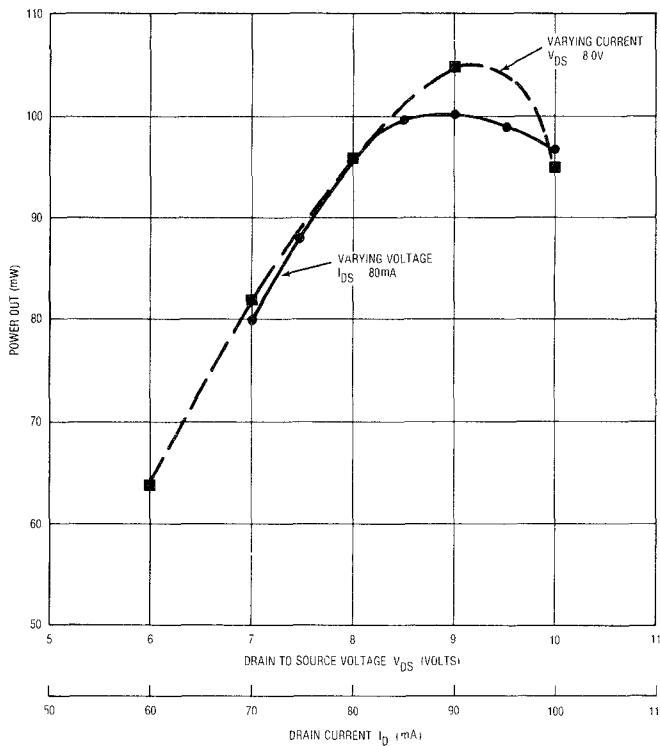


Fig. 12. FET oscillator power out versus drain-to-source voltage and drain current.

the device had a saturated output power of 250 mW at 10 GHz, then P_0 should be 95 mW. Measured output power at 10 GHz was 100 mW as computed. Fig. 12 is a plot of the measured oscillator power as a function of dc drain-to-source voltage V_{ds} and drain current I_d . Notice that a dc-to-RF efficiency of 15 percent was obtained at 8 V and 90 mA at 10 GHz.

Although no special tuning was necessary to obtain maximum output power, it was found that with the load coupled as designed to give maximum output power, the oscillator tended to be susceptible to either not oscillating at all, or oscillating at full power. This indicated that the negative resistance was so close to its maximum value that, with a slightly larger load resistance, the net zero resistance condition for oscillations was not met. It was concluded that a slightly smaller load resistance should be used to assure oscillations at the desired frequency, even though the output power might be slightly less than the maximum available.

Since the oscillator tended to not oscillate under some temperature conditions, it was retuned to 9.5 GHz in order to make temperature measurements. The oscillator frequency increased 65 MHz when reduced to -40 from +25°C and its power increased to 125 mW. When increasing the temperature from +25 to +70°C, the frequency decreased 20 MHz while the power fell to 28 mW. By increasing the drain current to 90 mA, the power came up to 60 mW. This means that, for optimum oscillator design, S parameters should be measured at the maximum temperature of operation to assure good performance.

III. SECOND DESIGN APPROACH

Up to this point, the design has been based entirely on the first approach, using computer optimization, to calculate large signal S parameters. In the second approach, just the magnitude of S_{21} is reduced until the point of maximum oscillator power is achieved. To see how close the oscillator embedding elements would be to the values obtained for the first approach, measured small-signal parameters at 10 GHz were used to compute these values, except for S_{21} which was reduced in magnitude to a value of 0.735. This corresponds to $G_{ME} = 2.96$, the value that would be calculated from (11). The value of small signal gain G_0 is calculated from (5) using the small signal magnitude of $S_{21} = 1.03$.

Results of oscillator embedding element calculations at 10 GHz are shown as circled points in Fig. 10 for circuit 4. The differences are very small; hence, it is expected that oscillator design based on this method would be quite close to the first approach. This depends to some extent on how accurately the S parameters are measured.

IV. CONCLUSION

Techniques have been described which permit accurate FET oscillator design without repeated large signal measurements. Using these techniques, a coaxial cavity FET oscillator was constructed which substantially verified the theory.

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IF Conversion Gain of Glow Discharge Lamps as X-Band Mixers for High LO Power Levels

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Abstract—Inexpensive glow discharge indicator lamps mounted in a waveguide mount are investigated as mixers at relatively high X-band local oscillator (LO) power levels. The IF conversion efficiency was found to drop off for LO power levels greater than about 30-40 mW, although no damage occurs to the lamps at higher power levels. Because of the small lamp size relative to waveguide cross section, sensitivity is much less than in the free space configuration. For many reasons the use of such devices as mixers should be much more promising at millimeter-wave frequencies than at microwave frequencies.

I. INTRODUCTION

COMMERCIAL glow discharge indicator lamps, whose individual price is ordinarily a fraction of a dollar, have been shown to exhibit rather good sensitivity to both millimeter-wave [1], [2] and microwave [3]-[5] radiation as video detectors. Utilization of this type of device for detection of electromagnetic radiation has been extended to the infrared [6], [7], visible [8]-[13], and ultraviolet [14], [15] spectral regions. The ability to sense microwave frequency with such devices has also been demonstrated [16], [17]. Other advantages of gas discharges as detectors of electromagnetic radiation include less sensitivity to ambient temperature changes [18]-[20], large dynamic range and electronic ruggedness, wide-band RF response [1], [17]-[20], and the ability to detect sudden increases in radiation levels without being damaged [17], [19], [20]. Also, they can be used in environ-

ments such as the Van Allen belt, nuclear reactors, or space systems subject to intense ionizing radiation fields [21], [22] where many other types of detectors cannot operate reliably.

The chief disadvantage is a relatively slow response ($\approx 1\text{-}\mu\text{s}$ rise time). However, the rise time is limited, not by the intrinsic detection mechanism [17], [23], but by the parasitic reactance [9]. Recent experiments indicate that such reactance effects might be minimized and rise time thus improved by miniaturizing the electrode geometry [23]. The very high intrinsic speed of response by the gas discharge *itself* is clear from the many harmonic generation and wide-band frequency-mixing operations that have been observed at frequencies as high as the optical spectral region [24]-[28]. However, as in such experiments the output is an electromagnetic wave rather than an electronic voltage signal, reactance has no effect [23].

Recent experiments have indicated the feasibility of using simple inexpensive glow discharge indicator lamps as mixers at millimeter-wave [29] and microwave [30] frequencies. In particular, one suggested advantage of such an application, in addition to low price, is to exploit the wide dynamic range of these devices by illuminating them with relatively high local oscillator (LO) power levels P_{LO} so as to make possible detection of very weak signal power levels P_S [30]. This is possible in principle because the IF signal is proportional to $(P_S P_{\text{LO}})^{1/2}$. Thus as long as the product of P_S and P_{LO} does not vary much, high LO levels may in theory compensate for weak signal levels. That varying one IF component is equivalent to varying the other has been verified for low signal and LO components [30]. The purpose of this paper is to report sensitivity limitations observed at higher X-band power levels with inexpensive commercial indicator lamps in

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A FULLY INTEGRATED CMOS VCO FOR DCS-1800 DIRECT CONVERSION RECEIVERS

The goal of this article is to prove that restrictive phase noise requirements can be achieved with a fully integrated CMOS VCO if the LC tank circuit is properly designed. The VCO has been designed in a standard two-metal layer process with 0.8 μm CMOS transistors. The measured phase noise is -103.8 dBc/Hz at 100 kHz from a 1.8 GHz carrier. The output frequency range is from 1.65 to 1.95 GHz. These phase noise and oscillation frequency values meet the requirements for a DCS-1800 direct conversion receiver. The core power consumption is 8 mA from a 5 V voltage supply.

The growing demand for mobile communications, mainly telephony, implies the need for better performance of RF transceiver architectures. A fundamental element in these front-ends is a voltage-controlled oscillator (VCO), the performance of which is a determining factor related to system limitations. Fully integrated VCOs usually suffer from poor phase noise characteristics, so a large effort is made to improve the phase noise of integrated oscillators. As the phase noise of LC

integrated VCOs highly depends on the quality factor of the tank circuit,¹ special emphasis must be made in the design of the inductor and varactor.

The phase noise performance required for mobile telecommunication standards like GSM or DCS-1800 is so restrictive that it is not easily achieved in a low cost standard technology used in a fully integrated oscillator, in large part because of the limited quality fac-

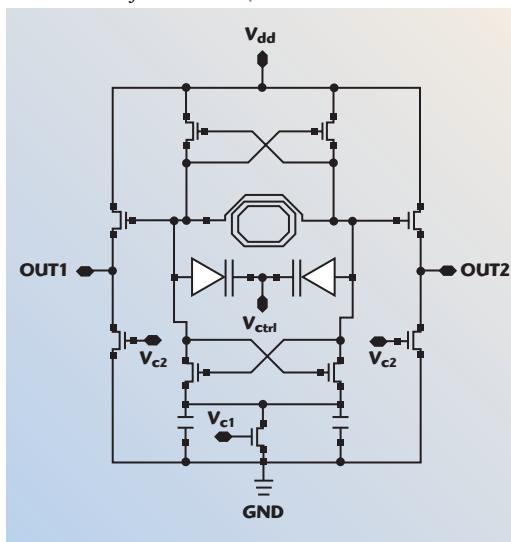
tor of the integrated inductors. However, this article will show that the proper design of the tank circuit allows the design to meet the phase noise specification.

The need for good performance suggests that most integrated RF VCOs are realized with bipolar devices, due to their low high frequency noise.^{2,3} It will be shown that an oscillator can be implemented in a “big” channel length CMOS standard technology without an excessive increase in power consumption. The technology used is a two-metal layer process with 0.8 μm CMOS transistors.

OSCILLATOR ARCHITECTURE

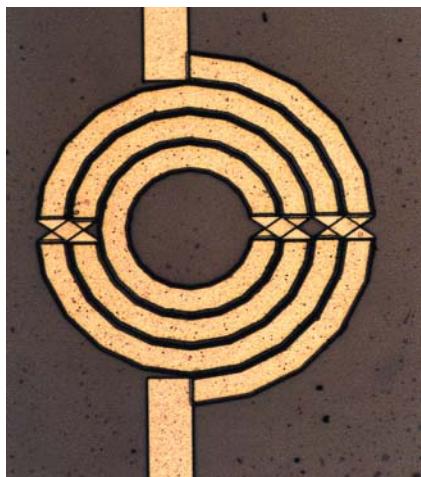
The selected architecture for the VCO with an integrated LC tank circuit is shown in **Figure 1**. It is important to mention that a differential architecture has been used to minimize effects such as voltage supply, and

Fig. 1 CMOS architecture of the VCO. ▶



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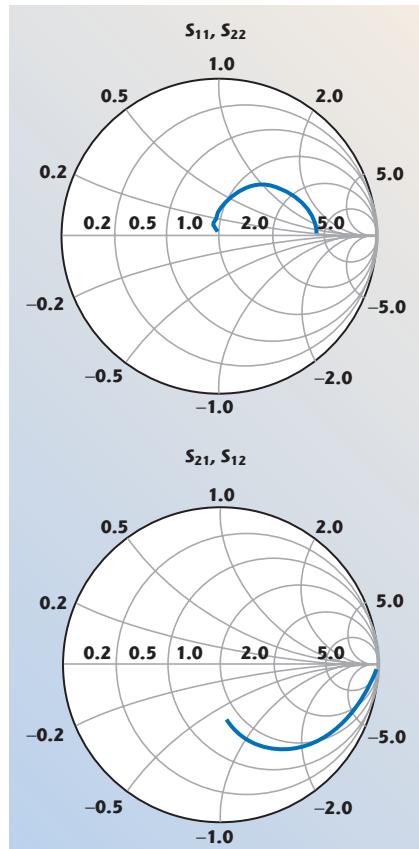


▲ Fig. 2 Microphotograph of the balanced inductor.

TABLE I

GEOMETRICAL CHARACTERISTICS OF THE BALANCED INDUCTOR

Radius (μm)	105
Width (μm)	10
Spacing (μm)	1.9
Number of turns	3.5
Number of sides	20



▲ Fig. 3 De-embedded S-parameters of the measured inductor.

current source noise and temperature variations.

There are different architectures used to integrate a MOS VCO.⁴ The CMOS configuration offers the best phase noise/power consumption ratio. Because MOS transistors need high bias currents to obtain good transconductances, this is the configuration selected to implement the oscillator, expecting a reduction in the power consumption for a same phase noise value, compared with other architectures.

Two tail capacitors have been added in parallel with the biasing current source since their presence can improve the phase noise of the oscillator.⁵ Simulations show that not only is the phase noise improved but the output power is increased with an insignificant reduction of the oscillation frequency. To select the value of these capacitors, there is a trade-off between the improvement in phase noise and output power, and the sensitivity of the oscillator to supply voltage variations⁵ and the occupied area.

Two external pins called V_{c1} and V_{c2} can control the current flowing across the core and the output stage of the VCO, respectively. This way the relation between phase noise and power consumption can be optimized.

TANK CIRCUIT DESIGN

As mentioned before, good phase noise values can be reached by a proper design of the tank circuit. Therefore, the analysis and characterization of the passive elements is a critical step in the design flow. The well-known Leeson model¹ demonstrates that the phase noise performance is highly dependent on the quality factor of the tank circuit; therefore, it is necessary to design high Q passive elements.

In the frequency range where the designed VCO works (approximately 1.8 GHz) the inductor usually dominates the quality of the tank circuit.¹ Consequently, this section will emphasize the design of this inductor.

INDUCTOR DESIGN

The two main factors that affect the quality of an inductor are its resistive and substrate losses. At low frequencies, the series resistance of the inductor metal tracks represents the dominant losses. As the frequency increases, however, eddy currents in

the tracks and substrate increase these losses. None of these effects is negligible near 1.8 GHz.

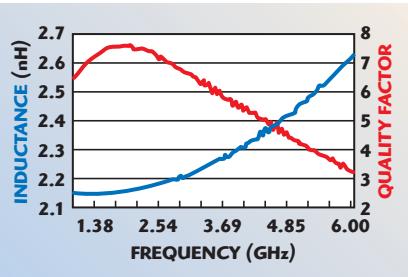
The CMOS architecture selected to design the oscillator is differential, so the tank circuit must have a differential behavior as well. The balanced one is the only type of inductor with differential behavior. Another solution is to use two standard inductors symmetrically placed. This option has been rejected due to the larger area occupied. Since the technology uses a highly conductive P type substrate, the substrate losses, and thus the area of the inductor, will determine its quality.

The selected configuration is the balanced one, due to the possibility of integrating the same inductance in less area. Balanced inductors exhibit more coupling between their turns, which means a larger inductance can be obtained than for two standard inductors symmetrically placed occupying the same area. Furthermore, this inductance is obtained with less metal length and the resistance of the inductor decreases.^{6,7} In addition, the parasitic coupling that occurs between the two inductors symmetrically placed is avoided using a balanced inductor.

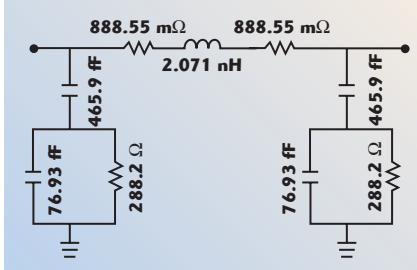
Besides substrate losses, resistive losses of the inductor cannot be neglected. In order to reduce the ohmic losses of the metal tracks two improvements have been made: the connection in parallel with longitudinal vias (except in the underpasses) of the two available metal layers to diminish the series DC resistance of the coil and the design of a hollow spiral to avoid the high resistance of the inner turns due to proximity effect.¹ A microphotograph of the balanced inductor is shown in **Figure 2** and its geometrical characteristics are presented in **Table 1**.

The measurement system used for the characterization of the passive elements consists of an HP8719ES vector network analyzer and ACP40 GSG micropipes. To calibrate the measurement system, the short open load thru (SOLT) method has been used. Finally, the four step de-embedding method⁸ has been used to remove the parasitic effects introduced by the measurement structures. The measurement results of the inductor after the de-embedding procedure are presented in **Figure 3**.

TECHNICAL FEATURE



▲ Fig. 4 Measured characteristics of the inductor.

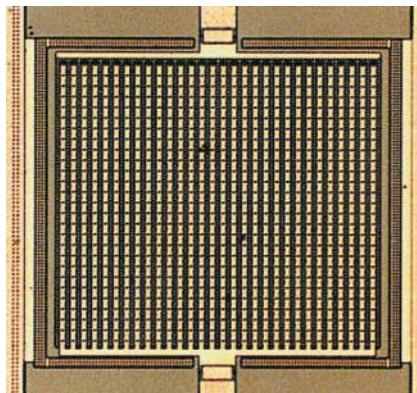


▲ Fig. 5 Π model of the balanced inductor.

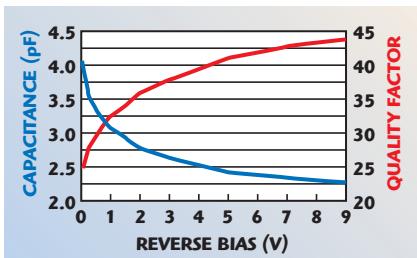
TABLE II

VARACTOR GEOMETRICAL CHARACTERISTICS

Dimensions (μm^2)	210×230
Number of P+ islands	27×30
P+ Island size (μm^2)	3.6×3.6
P+/N+ distance (μm)	1



▲ Fig. 6 Microphotograph of the varactor.



▲ Fig. 7 Measured characteristics of the varactor.

Due to the symmetry of the inductor, S_{11} and S_{22} parameters should be exactly equal, as are S_{12} and S_{21} . As seen, the measurement results of the two ports are very close together. To improve the accuracy of the measurements, after calculating the one port S-parameters using

$$S_{11_1} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}}$$

$$S_{22_1} = S_{22} - \frac{S_{21}S_{12}}{1 + S_{11}} \quad (1)$$

Their difference must be evaluated. If the calculated difference is higher than five percent the measurements are rejected and must be made again, otherwise, an average one port S-parameter is calculated

$$\text{If } |S_{11_1} - S_{22_1}| < 5\%$$

$$S_{ii_1} = \frac{S_{11_1} + S_{22_1}}{2} \quad (2)$$

With these average one port S-parameters, the inductance and quality factor of the inductor can be calculated. The results are presented in **Figure 4**.

The final step of the characterization process is the modeling of the inductor. A Π Model has been used due to its simplicity and physical sense.⁶ Moreover, it is easy to fit the model in a narrow band of frequencies. One of the limitations of the Π model is that it is not valid for modeling passive elements in high frequency ranges. However, because the designed oscillator operates at a fixed frequency, the Π model is accurate enough in the frequency range from 1.7 to 1.9 GHz. The model of the inductor is presented in **Figure 5**. The series resistance has been divided into two parts only to make explicit that the inductor is balanced.

VARACTOR DESIGN

The varactor design is based on the variable capacitance that appears in a P-N junction when it is reverse biased. The varactor consists of P+ islands diffused in an N-well and surrounded by a N+ zone. This way, the depletion zone appears around all the P+ diffusion, so the capacitance is higher as is the capacitance variation.⁶

The N-well N+ contacts are useful in decreasing the series resistance of the device. The geometrical charac-

teristics of the varactor are presented in **Table 2** and a microphotograph is shown in **Figure 6**.

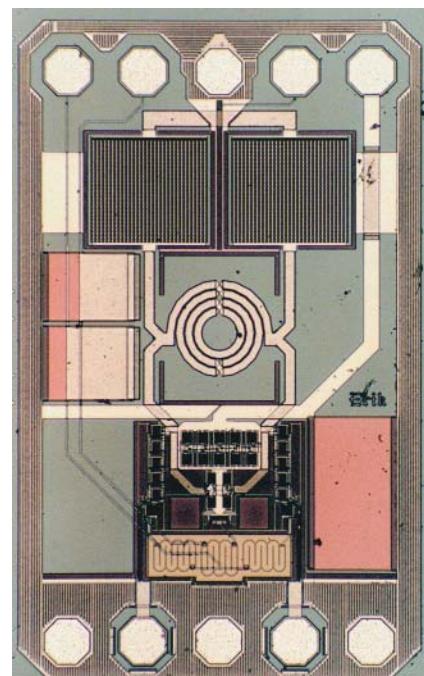
The measurement system, calibration and de-embedding methods used to characterize the varactor are the same as the ones used to characterize the inductor. The measured results are shown in **Figure 7**.

MEASUREMENTS

The oscillator response has been measured with a E4407B spectrum analyzer. DCQ-05 PPGPP microprobes have been used for the supply and control voltages, and ACP40 SGS microprobes have been used for the output signal.

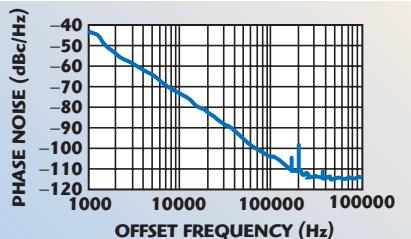
A microphotograph of the VCO is shown in **Figure 8**. In the layout, some capacitors between the DC voltage pads and ground have been added in order to stabilize the supply voltage, eliminating the high frequency variations in this voltage that can adversely affect the phase noise response. The last consideration is that various substrate contacts connected to the ground pads were added around the transistors in order to provide a stable substrate potential.

The measured phase noise response of the VCO at 1.8 GHz is shown in **Figure 9**. This measurement has been done for a bias current of 8 mA for which the optimum performance of the oscillator is obtained.



▲ Fig. 8 Microphotograph of the VCO.

TECHNICAL FEATURE



▲ Fig. 9 Phase noise of the VCO at 1.8 GHz.

TABLE III

VCO MEASUREMENT RESULTS

Oscillation frequency (GHz)	1.8
Output power (dBm)	3.3
Phase noise @ 100 kHz (dBc/Hz)	-103.8
Core power consumption (mW)	40
Tuning range (%)	16.7

With this current, the oscillator is operating in the current-limited region but near the limit of the voltage-limited region.⁵ The rest of the measurements, presented in **Table 3**, have been done with this same current.

CONCLUSION

In order to design a VCO which fulfills restrictive phase noise requirements, the first stage is to design a good quality tank circuit, which in this case is based on a balanced inductor and a PN junction varactor. The quality factor of the inductor is 7.7 at 1.8 GHz and the varactor has a quality factor between 30 and 50 depending on the applied control voltage.

A fully integrated VCO with low core power consumption that achieves the restrictive phase noise specification for DCS-1800 has been designed. The measured phase noise is -103.8 dBc/Hz at a 100 kHz offset from a 1.8 GHz carrier. The oscillator has been designed using $0.8\text{ }\mu\text{m}$ CMOS transistors; therefore, the ability of the CMOS technology to achieve good phase noise results, if a proper LC tank is designed, is demonstrated. ■

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HARMONIC OPERATION OF GaAs MILLIMETRE WAVE TRANSFERRED ELECTRON OSCILLATORS

Indexing terms: Electron devices, Gunn devices, Oscillators

Harmonic operation of GaAs millimetre wave transferred electron (TE) oscillators has been identified using a wideband waveguide system. The harmonic number was determined by precisely measuring the frequency as well as the frequency variations of the harmonic components when the oscillator was tuned mechanically or electrically. We find that GaAs TE oscillators at 94 GHz, matched to a waveguide circuit by means of a resonant disc, operate at the second or third harmonic frequency, depending on the length of the active GaAs region, which was between 1.8 and 2.6 μm .

Transferred electron devices are capable of operating over a limited frequency range above and below a transit time frequency. In the past, theory has predicted an upper frequency limit for fundamental frequency operation of approximately 60 GHz.¹ GaAs TE oscillators, however, have been operating at frequencies above 60 GHz for some time now,²⁻⁵ but with rather low efficiencies, suggesting the possibility of harmonic rather than fundamental frequency operation. Until very recently,⁶ experimental evidence of harmonic operation of TE devices has not been conclusive, although this possibility has been suggested and harmonic operation has been observed (see Reference 4 and Fig. 3 of Reference 5). It is the purpose of this letter to provide additional evidence confirming the results of a recent publication⁶ where the harmonic content of GaAs and InP TE oscillators was determined by using a wideband interferometer system. We have employed a wideband waveguide system which is capable of measuring frequencies precisely. Both CW and pulsed measurements are possible. The devices tested and reported on here were ohmic down to a temperature of 10 K. The oscillation frequencies of the devices were measured over at least two waveguide bands. The frequency changes obtained by bias voltage changes or by tuning the resonant disc circuit⁷ employed as the impedance matching network for the TE oscillators were measured precisely, and the harmonic number was determined from the relations:

$$f_n = (n/m)f_m \quad (1)$$

$$\Delta f_n = (n/m) \Delta f_m \quad (2)$$

where m and n are the harmonic indices. Thus, measuring the fundamental and second harmonic frequencies, $(n/m) = 2$. For the second and third harmonic frequencies $(n/m) = 1.5$. The frequency changes Δf were obtained by three methods giving identical results for n and m . Electrical tuning of a TE device is possible by varying the applied bias voltage. Mechanical tuning is achieved by changing the capacitance of the resonant disc circuit by means of a tuning rod or by successively varying one dimensional parameter of a resonant disc circuit as described below.

The resonant disc circuit, which is an extension of the vane-type impedance matching circuit used in the past extensively for impatt devices, is illustrated in Fig. 1. For a TE device it

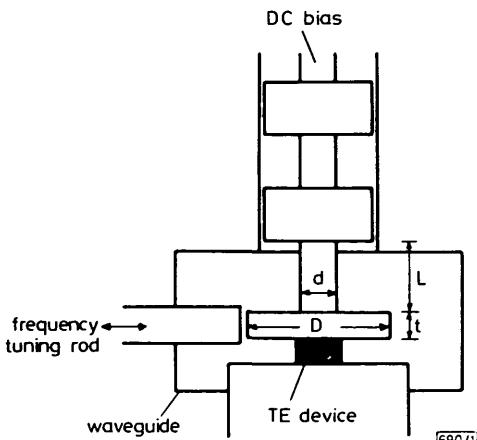


Fig. 1 Resonant disc type TE oscillator

performs two functions. It provides efficient impedance matching from the waveguide impedance level of several hundred ohms to the device level of several ohms.⁸ It also provides a resonant circuit at the fundamental device operating frequency. This is evidenced by the fact that, in a TE oscillator with a resonant disc structure, the position of the short circuit has no effect on the fundamental frequency if the harmonic components lie above the cutoff frequency of the waveguide (40 GHz for V-band, 59 GHz for W-band).

The section L in Fig. 1 behaves as an inductor, and thus an increase in L or a decrease in d cause a decrease in frequency. The disc exhibits the properties of a capacitor, with the frequency decreasing with increasing D or t . The resonant frequency of the disc-diode configuration may also be varied by changing its position in the waveguide. We have used here continuous tuning by means of a metal rod which is brought in close proximity to the disc. A typical result is illustrated in Fig. 2. Incremental mechanical tuning is possible by varying any one of the dimensional parameters d , D , t or L .

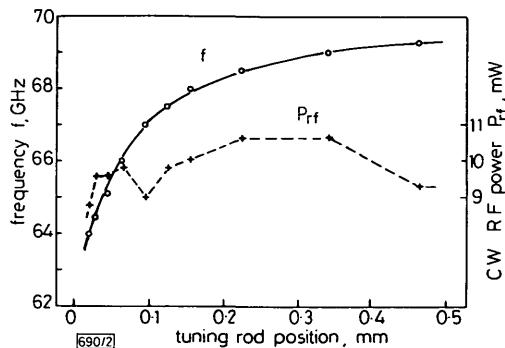


Fig. 2 Tuning characteristic of a resonant disc type TE oscillator

In our experiment, the harmonic operation of the TE diodes was determined using a short V-band (50–75 GHz) or E-band (60–90 GHz) waveguide section containing a disc resonator and the TE device, as illustrated in Fig. 1. To either side of this oscillator were attached two frequency measuring sections, one V-band, the other W-band (75–110 GHz), each containing an isolator, E-H tuner, attenuator, frequency meter and power meter or diode detector. Several different disc resonators were used in order to observe a number of frequencies. The harmonic number of the observed frequencies was determined with disc resonators which caused two frequencies to lie within the two waveguide frequency ranges. The experimental results are illustrated in Fig. 3. Here, a nominally 2.4 μm device (vapour phase epitaxy) was operated with a disc whose diameter was successively reduced from 3.19 to 2.22 mm, with a corresponding increase in the second and third harmonic

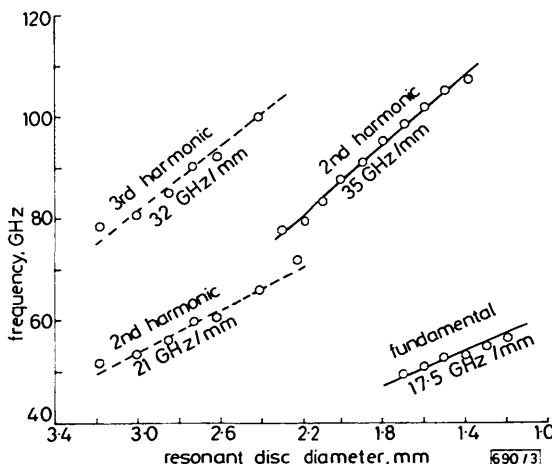


Fig. 3 Tuning characteristics of GaAs TE oscillators, showing second and third harmonic operation of 2.4 and 2.6 μm devices in a short V-band section, and fundamental and second harmonic operation of 1.8 μm devices in a short E-band section

Resonators of V-band section had dimensions $d = 0.5$, $L = 1.1$ and $t = 0.3$ mm, and those of E-band section, $d = 0.5$, $L = 0.45$ and $t = 0.3$ mm
--- 2.4 and 2.6 μm
— 1.8 μm

frequencies. Frequency excursions by means of varying the applied bias voltage can be determined precisely by the resonant cavity frequency meters, and were 0.21 and 0.33 GHz for the second and third harmonic frequencies, respectively. This ratio of 1.5 was also obtained from larger frequency excursions over several GHz obtained with the disc tuning rod. The diodes exhibited 10–15 mW CW power at 90 GHz with a maximum frequency (1 mW level) of 115 GHz. Their fundamental oscillation frequency is thus at least from 25 to 40 GHz. A second series of 2.6 μm devices (molecular beam epitaxy) exhibited essentially identical behaviour, with the exception that the output level at the third harmonic frequency was less, 5 mW at 90 GHz and 1 mW at 105 GHz. With the disc diameters shown in Fig. 3, oscillation frequencies lying within 1 GHz were measured for both the 2.4 and the 2.6 μm devices. With 1.8 μm devices (molecular beam epitaxy) the RF power output in our system was in the range 50–62 GHz and 80–115 GHz. From Fig. 3, fundamental and second harmonic operation is apparent, and was also confirmed by continuous frequency tuning. At the second harmonic frequency, the power output was maximum between 90 and 100 GHz. These devices seem to oscillate at a fundamental frequency of 40–60 GHz. The entire range of oscillation has not been determined here, since the purpose of our investigations was to prove the existence of harmonic operations.

For the frequency measurements with 1.8 μm devices, the resonators of the V-band section could not be used since they have a fundamental oscillation frequency which lies below that of the 1.8 μm devices. A set of resonators was available in conjunction with a short E-band section. These resonators had smaller diameters, with good coupling into the W-band waveguide at the second harmonic.

We should like to point out that, by employing continuous tuning at the fundamental frequency (mechanical, capacitive, magnetic), very wideband operation at W-band frequencies is possible: from Fig. 3, 30 GHz for a 1.8 μm device, and 20 GHz for a 2.6 μm device, with 45–60 GHz and 25–35 GHz, respectively, fundamental frequency tuning.

Conclusion: The results presented here indicate that GaAs TE devices are delivering useful power in the millimetre wave range at their harmonics. Harmonic operation has been proven here, and the harmonic number has been determined by tuning the oscillation at the fundamental frequency and observing the frequency change of the harmonics. Our data confirms recent results obtained by another method.⁶ It is not unreasonable to suspect that in the past a great number of observations of oscillations in the V and W bands can be attributed to harmonic operation. We may conclude that 1.8–2.0 μm devices operating at the second harmonic, or 2.2–2.4 μm devices operating at the third harmonic, are suitable as a source for 94 GHz. For 140 GHz, a 1.3–1.5 μm device, operating at its second harmonic, or a 1.7–2.0 μm device operating at its third harmonic, should be considered.

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21st August 1981

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1.3 μm InP/InGaAsP PLANAR AVALANCHE PHOTODIODES

Indexing terms: Semiconductor devices and materials, Avalanche diodes

An InP/InGaAsP planar avalanche photodiode operating at a wavelength of 1.3 μm has been fabricated by using Be implantation and a difference of impurity concentrations between two *n*-InP epitaxial layers. A sufficient guard ring effect is demonstrated by a photoresponse, and an avalanche gain of 110 is obtained at an initial photocurrent of 0.35 μA .

There has been great interest in InGaAsP avalanche photodiodes (APDs) as low noise detectors operating at a wavelength of 1.3 μm . To date all of the InP/InGaAsP-APDs reported which show a large avalanche gain at this wavelength have had a mesa structure.^{1–3} To achieve stable and reliable operation, a planar structure is crucial for an avalanche photodiode which operates at high reverse biases. In this letter we describe some initial results on a planar InP/InGaAsP-APD with two-step guard ring structure fabricated by ion-implantation and liquid phase epitaxy techniques.

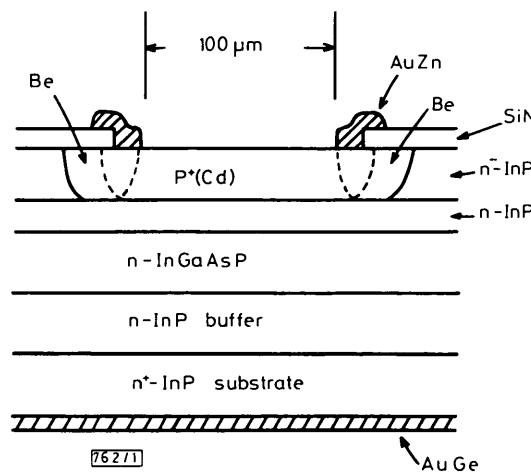


Fig. 1 Cross-sectional view of diode

The cross-sectional view of the diode is shown in Fig. 1. The *n*-InP layer was grown as a buffer layer on a (100) S-doped InP substrate on the buffer layer and two layers of *n*-InP were grown on it. The carrier concentration of the quaternary layer obtained by *C/V* technique was $1 \times 10^{16} \text{ cm}^{-3}$ and the thickness was 2 μm . The wavelength of fundamental absorption edge was 1.36 μm . The carrier concentration of the upper InP layer was $3.5 \times 10^{15} \text{ cm}^{-3}$ and was designed to be lower than that of the lower InP layer ($1 \times 10^{16} \text{ cm}^{-3}$). The thickness of the upper and lower InP layers were 2 μm and 1 μm , respectively. The guard ring was formed in the upper InP layer by using ion-implantation of Be at 150 keV. The net doping level was $5 \times 10^{13} \text{ cm}^{-2}$. After the implantation, the wafer was annealed at 750°C for 20 min. The *p*⁺ region was made by Cd diffusion from a CdP₂ source at 500°C for 3 h. Ohmic contacts to the *p*⁺- and *n*⁺-InP were made by alloying

Short Papers

Performance and Design of Microwave FET Harmonic Generators

MADHU S. GUPTA, RICHARD W. LATON,
AND TIMOTHY T. LEE

Abstract— Experimental measurements of the power gain of a 4- to 8-GHz frequency doubler, employing a single-gate GaAs MESFET device and a microstrip circuit, are reported. The measured performance provides design guidelines, and is explained in terms of FET characteristics. In particular, the multiplication gain is largest when the FET is biased near pinchoff.

I. INTRODUCTION

The nonlinear characteristics of microwave field-effect transistors have recently been used in the design of frequency multipliers by us [1] and by other authors [2], [3]. Both single-gate and dual-gate FET devices have been employed as harmonic generators in the published experiments. The advantages of the FET over a varactor diode in a harmonic generator include better isolation, and a multiplication gain which exceeds unity. This paper reports detailed experimental measurements of the performance of a frequency doubler constructed with a single-gate GaAs microwave MESFET device. The purpose of this work is to 1) experimentally determine the optimum operating conditions (i.e., dc bias and input signal level) which can serve as a guide in design, and 2) qualitatively explain the nature of the operating characteristics of the frequency doubler in terms of the known nonlinear behavior [1] of MESFET devices. The maximum multiplication gain achieved in these experiments is 3 dB, which is higher than that previously reported for single-gate devices.

II. EXPERIMENTAL ARRANGEMENT AND RESULTS

Fig. 1 shows the frequency doubler circuit, as well as the experimental setup used for measuring the performance of the circuit. The device used is a packaged MSC 88001 microwave GaAs MESFET, mounted in a microstrip circuit in grounded-source configuration. The input and the output frequencies were 4 and 8 GHz, respectively. The input and output ports of the FET are matched and tuned at their respective frequencies by microstrip stubs; in addition, external coaxial stub tuners were also used to optimize the doubler performance by varying the impedances presented to the device at various harmonic frequencies. All the components used in the circuit are designed for use up to X-band (12.4 GHz), which includes both the input and the

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output frequencies as well as the third harmonic; the impedances at the fourth and higher harmonics are thus dependent on the tuners and the out-of-band response of the components like bias tees. The output circuit also filters out the undesired harmonics, thus improving the spectral purity of the output.

The principal performance parameter of interest in these experiments was the multiplication gain, defined as the ratio of the second harmonic power output to the fundamental frequency power input. Many other parameters of interest, such as the bandwidth and the spectral purity of the output, are very strongly dependent on the circuit and are not determined by the inherent characteristics of the FET device used. The present experiments attempted to establish the dependence of the gain on the device, independent of the tuning circuit, by optimizing the circuit for maximum gain; all gain values reported below are measured under such optimized conditions.

The measured power gain of the frequency doubler is plotted in Figs. 2–4 as a function of the operating conditions. Fig. 2 shows the variation of gain with the gate-to-source dc bias voltage V_G of the FET, for different constant values of the drain-to-source dc bias voltage V_D , at a fixed value of input RF power level $P_{in} = 11$ dBm. Fig. 3 shows the variation of gain with V_D for some constant V_G values, also for the same P_{in} . Finally, Fig. 4 shows the gain variation with P_{in} for two different values of V_G and at $V_D = 4$ V. The conclusions that can be drawn from these plots, and the justification of the nature of observed variations in terms of the device behavior, are discussed in the following.

III. INTERPRETATION OF RESULTS IN TERMS OF FET MODEL

The experimental results reported can be qualitatively understood in terms of the known nonlinear characteristics of microwave MESFET's. One approximate and convenient description of the device characteristics is in the form of a quasi-static equivalent circuit [1]. Briefly, this circuit should include 1) a bias-dependent input (gate-to-source) capacitance, and 2) an output (drain-to-source) current source, controlled by the input and output voltages as indicated by the FET dc characteristics. In particular, the controlled current at the output becomes independent of the input signal when the input voltage either 1) causes forward conduction in the input junction, or 2) reverse biases the junction beyond pinchoff. This simplified model of device behavior explains the following major features of results in Figs. 2–4.

1) Over the entire useful range of V_G , extending from values for which the gate junction is forward biased to values for which it is reverse biased beyond pinchoff, the gain becomes a local maximum at two values of V_G : one near 0 and the other near V_p , the pinchoff voltage of the device, which is approximately 4 V for the devices used. To a first approximation, this can be understood to be due to a one-sided clipping of the input fundamental frequency waveform, either at positive or at negative peaks, which results in the generation of second harmonic component.

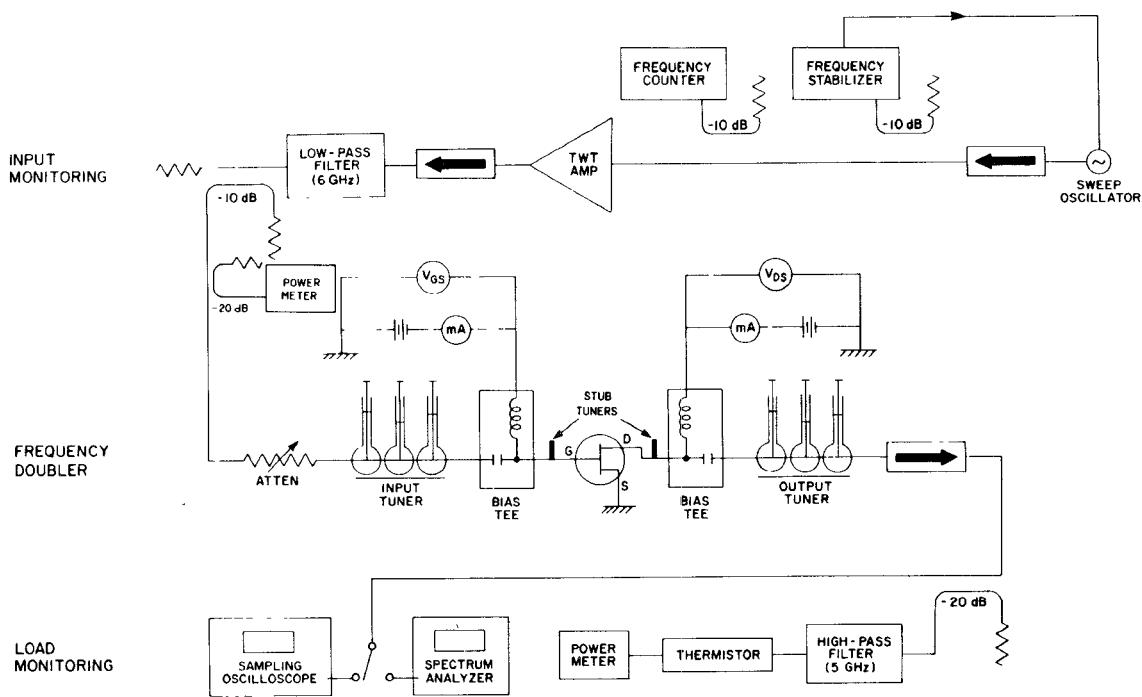


Fig. 1. FET frequency doubler circuit and the experimental arrangement for multiplication gain measurement.

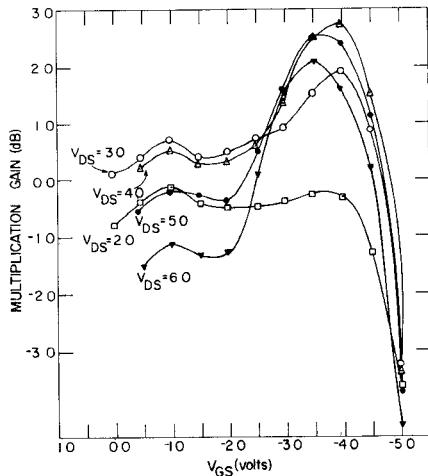


Fig. 2. Multiplication gain of the 4- to 8-GHz frequency doubler as a function of gate and drain dc bias voltages, for a fixed RF input power level of 11 dBm.

For a gate voltage in between these two values, the input waveform will be clipped at both positive and negative peaks; the resulting waveform then approaches a square wave, in which the second harmonic content is low. This obviously oversimplified explanation is further supported by the observation that the generation of third harmonic is largest at a gate bias of approximately $V_p/2$. The gain falls rapidly for gate voltages which forward bias the gate junction, or which bias it beyond pinchoff. This can be understood to be due to the small duty cycle for which the transistor is then in the active region.

2) For large values of V_D , the gain maximum is considerably higher for V_G near pinchoff than for V_G near 0. This is partly due to the sharper clipping at pinchoff, but primarily due to the smaller input (i.e., gate-to-source junction) capacitance at pinchoff, so that the same input power results in a larger voltage swing at the input, and therefore a larger drain current swing at the output.

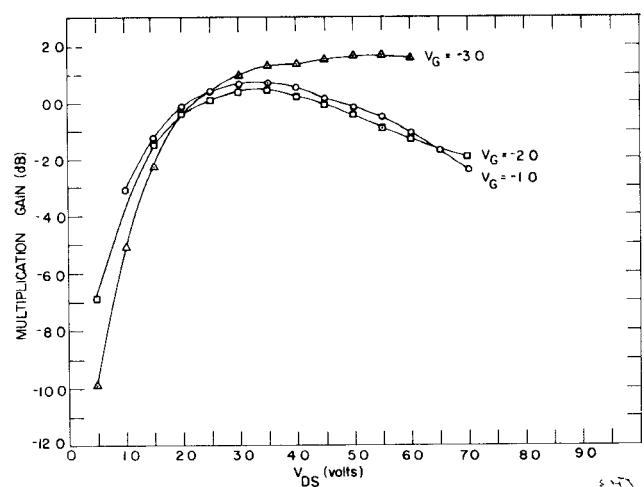


Fig. 3. Multiplication gain variation with drain bias voltage for a fixed input power level of 11 dBm

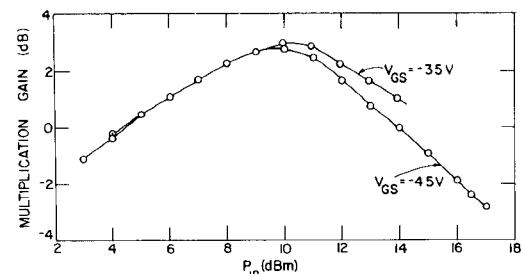


Fig. 4. Multiplication gain of the frequency doubler as a function of the input RF power level for a fixed drain voltage of 4 V.

3) Near its maximum, the multiplication gain is a sensitive function of V_G , but is relatively insensitive to V_D , provided that V_D is large (above 3 V in the present case); when V_D becomes

smaller, the gain drops. This behavior is to be expected on the basis of the FET drain characteristics; the drain current is independent of V_D when V_D is large, and drops to lower values when V_D is small.

4) The power gain of the frequency doubler increases with increasing input power level at small values of P_{in} , reaches a maximum (about 3 dB at 10-mW input in the present case), and then decreases for further increase in P_{in} . The gain expansion at low power levels can be understood from the fact that the device is nearly linear for small signals; the nonlinearity, and hence the harmonic generation, becomes significant only as the signal level becomes large. For very large signals, the output of the device is saturated so that a gain compression occurs.

IV. CONCLUSIONS

The multiplication gain of the FET frequency doubler is strongly dependent upon the choice of dc bias voltages. The gain can be maximized by selecting a gate-to-source voltage near pinchoff, and a drain-to-source voltage of approximately the same magnitude. When the bias has been thus optimized, the multiplication gain shows a maximum with respect to the input signal power level.

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On the Design of Transitions Between a Metal and Inverted Strip Dielectric Waveguide for Millimeter Waves

S. BHOOSHAN AND R. MITTRA

Abstract—The results of a study of three types of transitions between the rectangular metal waveguide and the inverted strip guide are reported. Reflected power measurements from each type of transition and insertion-loss measurements for configurations involving the three transitions have also been carried out. The procedure of determining the optimum parameters for the transition is quite general, and has the potential for being extended to other dielectric structures.

I. INTRODUCTION

The need for an efficient transition between dielectric and metal waveguides at millimeter-wave frequencies has been recently recognized. The literature on open dielectric structures shows that almost no details of a study of dielectric-metal waveguide transition exist. However, the transitions used to study the effects of such structures could be the basis for investigation [1]. The chief difficulty encountered when studying such transi-

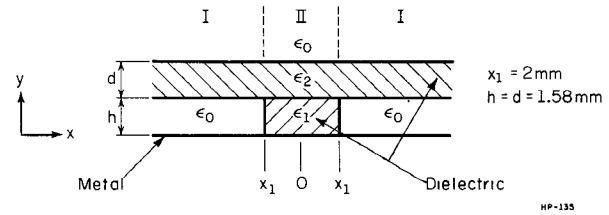


Fig. 1. Cross section of inverted strip guide with typical dimensions.

tions is that the wave must pass from an open-waveguiding structure to a closed one, and vice versa, with the field configuration undergoing a complete metamorphosis through the transition region. In this paper, we report the results of an experimental study of several transitions on the basis of the reflected power and insertion loss for these transitions. The dielectric guide used was the homogeneous inverted strip guide, whose cross section is shown in Fig. 1.

II. DETAILS OF THE STUDY

Two types of transitions were studied: 1) a direct metal to dielectric guide transition, depicted in Fig. 2, and henceforth called transition T-1; and 2) horn-type transitions shown in Figs. 3 and 4, henceforth labeled T-2A and T-2B, respectively.

The study is divided into two parts: a) reflected power measurements from the transition; and b) insertion-loss measurements for a length of dielectric guide introduced between two rectangular metal waveguides which serve as the input and output ports.

A. Reflected Power Measurements

The reflected power measurements for the transition between the metal and dielectric guides were conducted using a length of guide with the transition at its input port. A typical experimental setup consisted of a Y-junction circulator, whose three ports were connected to an RF source, the transition under test, and a power-measuring device. The power from the RF source was incident on the transition, and the power reflected from the same was measured to determine the reflection characteristics. The metal waveguide at the output port of the test setup was terminated by a matched load.

On the basis of these experiments, it was found that the reflection phenomenon in the transition occurs chiefly at two points: (i) at the junction of the metal waveguide and the lower dielectric strip; and (ii) between the lower strip and the top plate of the homogeneous inverted strip guide. The first type of reflection loss can be minimized by inserting an optimum length of taper of the lower strip into the metal waveguide, such that the lower strip is closely matched to the metal guide. The results of the experiments for the determination of the optimum length have been tabulated in Table I, where I_L^* is equal to the optimum value of the inserted length I_L , as shown in Fig. 2. In these measurements, the reflected power was at least 8 dB down as compared to the incident power.

Minimization of the second type of reflection loss can be achieved by using a horn-type feed, as in transitions T-2A and T-2B. Here the tapered top plate was inserted into the horn and the length inserted was adjusted to an optimum value, such that a minimum insertion loss was obtained. A horn-type feed was also instrumental in decreasing considerably the power radiated at the junction by about $\frac{1}{2}$ dB.

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TABLE V

Grid	n	Upper bound on S^2	Lower bound on S^2	Error in refinement near sing.	Error in refinement for infin.	Error in remaining region	Total error
1.2.2	47	55.74	52.02	0.541	1.740	1.441	3.722
1.2.4	57	55.24	52.35	0.465	1.137	1.286	2.888
1. ∞ . ∞	32	54.75	52.76	0.183	0.549	1.259	1.991
2.4.4	156	54.31	53.04	0.193	0.754	0.323	1.270
2.4.8	192	54.10	53.22	0.176	0.403	0.296	0.876
2. ∞ . ∞	77	53.90	53.41	0.044	0.146	0.293	0.483
4. ∞ . ∞	215	53.71	53.57	0.013	0.052	0.074	0.139

For the problem with $b = , a = 1, \epsilon_1 = 10\epsilon_0$.

improve the solution on these two grids the best strategy is to place more refinements for the unbounded region, i.e., grids 1.2.4. and 2.4.8.

VI. CONCLUSION

In this paper some ideas on error assessment in the finite element method have been introduced for field problems. It has been shown how these ideas can be used to choose an optimum grid refinement pattern at a singularity and for an unbounded region. It has also been shown how the effect of arbitrarily assuming a zero solution outside some finite region can be assessed. By looking at element by element contributions to the error, those elements or groups

of elements making major contributions to the error can be identified and singled out for refinement.

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Short Papers

Analysis of a Microwave FET Oscillator Using an Efficient Computer Model for the Device

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Abstract—This paper presents a time domain analysis of a microwave 10-GHz FET oscillator, which employs a practical and efficient computer model for the FET. Good agreement is demonstrated between the predicted and measured performance. A sensitivity analysis of the circuit is per-

formed with respect to some of the FET parameters. This is useful information to estimate performance variation in production.

I. INTRODUCTION

In the last decade the GaAs MESFET has become an important and useful microwave device. Many microwave components can be built using this device—amplifiers, oscillators, switches, mixers, etc. To enable an accurate and efficient design of components using MESFET's it is useful to have a fast and reasonably accurate large signal model for the device. The basic model of Shockley [1] was shown to be invalid for GaAs short channel FET (modern microwave FET's belong to this category).

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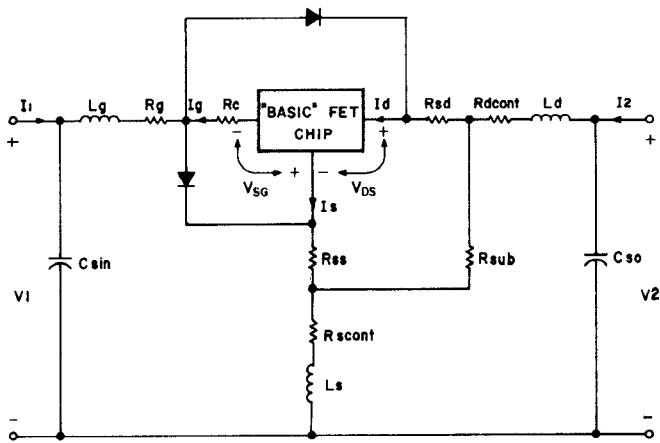


Fig. 1. Assembled MESFET chip model.

Thus, much work has been done in the last decade on FET modeling (see reference list of [2]). Most of this work is on numerical simulation, which is useful for understanding device operation; however, it is impractical for analysis and design of networks.

Recently a new model was developed by Madjar and Rosenbaum [2]–[4]. This model is almost entirely analytic, and thus very fast. It was shown to be practical and useful in the analysis of power amplifiers, oscillators, and frequency multipliers [2]. In this paper the new model is used to analyze a practical oscillator circuit suggested by Johnson [5]. Some of the predicted results are compared to the measured performance reported by Johnson. This way, two goals are achieved: 1) the usefulness and accuracy of the new model is demonstrated in a practical circuit; and 2) some of the properties of the particular oscillator are obtained. A brief description of the new model is given in Section II. The oscillator circuit to be analyzed is described in Section III. The simulation results are presented in Section IV.

II. THE COMPUTER MODEL

The new large signal computer model which is derived from basic principles is presented in detail in [2] and in a shorter form in [3], [4]. The region directly under the gate metalization is characterized by the mathematical relationship between the instantaneous currents and voltages

$$I_g = GVSG \frac{dV_{SG}}{dt} + GVDS \frac{dV_{DS}}{dt} \quad (1)$$

$$I_d = I_{con} + DVSG \frac{dV_{SG}}{dt} + DVDS \frac{dV_{DS}}{dt} \quad (2)$$

The currents and voltages are defined in Fig. 1. The conduction current, I_{con} , and the 4 capacitive coefficients ($GVSG$, $GVDS$, etc.) are functions of V_{SG} , V_{DS} and are calculated by the computer model. This representation is compatible with the state space approach in network analysis.

The complete equivalent circuit of the MESFET chip is given in Fig. 1. In addition to the basic FET characterized by (1) and (2), the model contains: R_{ss} , R_{sd} , bulk resistance of the regions between gate-source and gate-drain; and R_c , charging resistance of the channel. These quantities are calculated by the computer model. The other elements must be estimated by the user: L_g , L_s , L_d , wire bond inductances; C_{sin} , C_{so} , input and output stray capacitances; R_g , R_{scont} , R_{dcont} , contact resistances of the electrode metalization; and R_{sub} , parasitic resistance of the semi-

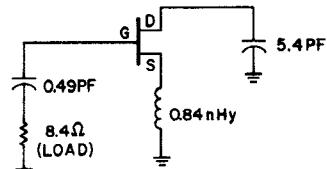


Fig. 2. Circuit diagram of the oscillator

insulating substrate. The two diodes represent the rectifying junctions drain-gate and source-gate, respectively.

III. THE OSCILLATOR CIRCUIT

The FET oscillator that was analyzed is the one suggested by Johnson [5]. Its ac circuit is given in Fig. 2 (the component values correspond to a 10-GHz oscillation frequency). The figure does not include the biasing arrangement. The device used is a Texas Instruments FET in a coaxial package. Its equivalent circuit is as shown in Fig. 1 with the addition of an inductance in series with the gate and drain ports. Johnson has calculated by curve fitting methods the values of the parasitic elements in the equivalent circuit. These values were used in our simulation.

The important device parameters used in the simulation are: doping level, 10^{17} cm^{-3} ; gate length, $1.2 \mu\text{m}$; gate width, $600 \mu\text{m}$; and epitaxial layer thickness, $0.3 \mu\text{m}$. To prevent long transient times before steady-state is reached (and the accompanying long computation times), RF chokes and bypass capacitors are to be avoided in the simulated circuit. To achieve this, two changes were made in the circuit of Fig. 2: 1) the 5.4-pF capacitor was merged with the additional parasitic drain inductance to a single inductance; 2) the series RC combination in the gate was replaced by its parallel equivalent. Due to these changes, steady state was obtained in less than 15 cycles of the fundamental frequency.

The state equations of the oscillator circuit were derived, and their solution in the time domain was obtained by means of a standard IBM routine, RKGS, which employs the Runge-Kutta method. The waveforms, thus obtained, were Fourier analyzed by the IBM routine FORIT, yielding the frequency domain properties of the oscillator.

IV. SIMULATION RESULTS

In this section the results of the 10-GHz oscillator circuit simulations are presented. The simulations were performed for a dc drain voltage of $V_{DS} = 8 \text{ V}$ and several values of gate voltage V_{SG} (corresponding to different values of dc current I_D). Fig. 3 shows the oscillator fundamental output power versus the dc current. The measured curve is from Johnson [5], who realized the $8.4\text{-}\Omega$ load (Fig. 2) by a coaxial transformer from $50 \text{ }\Omega$. This transformation is accompanied with some circuit loss. This loss is accounted for in the simulation by an additional resistance of $21 \text{ }\Omega$ in parallel with the $8.4\text{-}\Omega$ load (total load resistance, $6 \text{ }\Omega$). This value of resistance is reasonable (approximately 25-percent power loss), and gives the best fit to the experimental curve in Fig. 3. Obtaining each data point in Fig. 3 involves one full run of the computer program. The execution time for each run is approximately 30 s on a CDC 6600 computer.

The harmonic content of the output voltage waveform was determined from the Fourier analysis. Typically, the second harmonic level is at least 15 dB below the fundamental, and the third harmonic level is at least 27 dB below the fundamental. This good spectral purity (with no high- Q resonant circuits) is

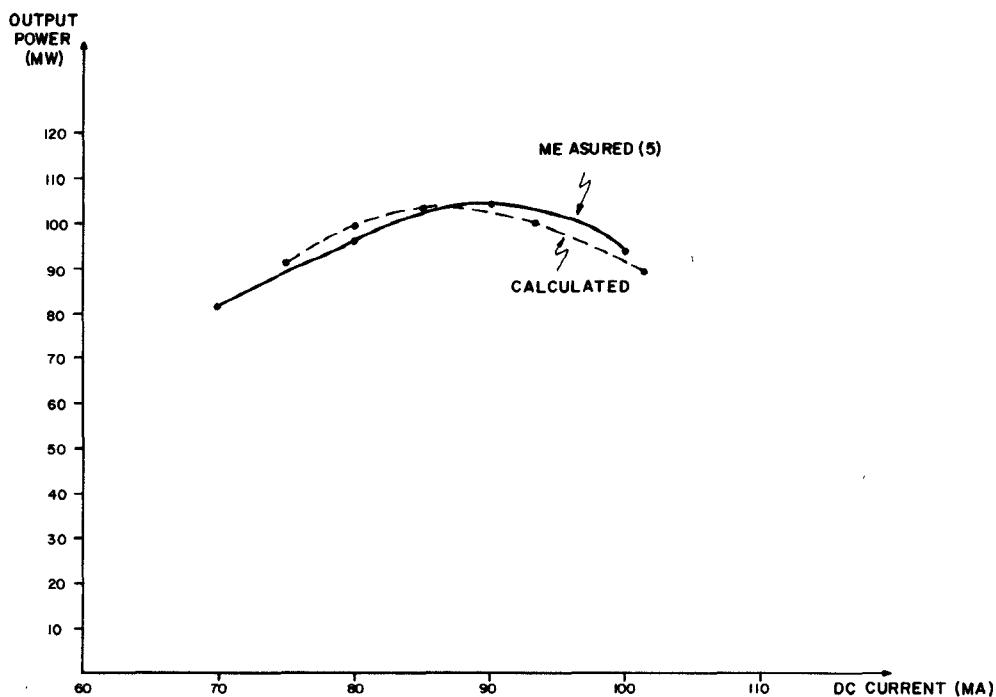


Fig. 3. Measured and calculated output power of the oscillator

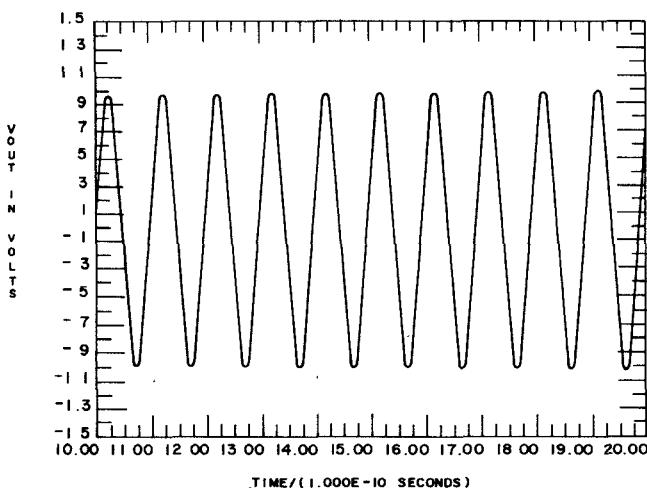


Fig. 4. Output voltage waveform.

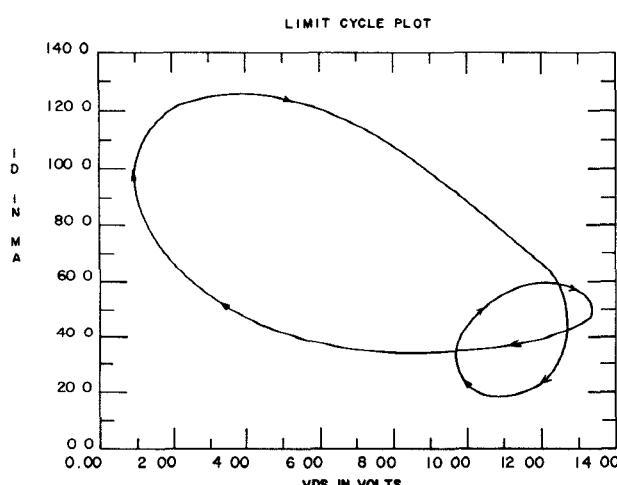


Fig. 5. Limit cycle plot.

probably due to the inability of the device to support such high frequencies. Fig. 4 presents the output voltage waveform in steady-state for one of the simulation runs. The good spectral purity is clearly evident.

Fig. 5 is a limit cycle plot. It shows the functional relationship between the drain current and voltage over one full cycle in steady state. The arrows indicate the direction of increasing time.

To test the sensitivity of this oscillator to the key device parameters two additional simulations were performed for a dc current of 85 mA. In one simulation the doping level was changed to $9.5 \cdot 10^{16} \text{ cm}^{-3}$ (5-percent decrease). The resulting output power is 101 mW (compared to 104 mW in Fig. 3), namely a decrease of about 3 percent. So the sensitivity of the output power to the doping level is not large. In the second simulation the epitaxial layer thickness was changed to $0.29 \mu\text{m}$ (3-percent decrease). The resulting output power is 89 mW, namely a decrease of 15 percent!

V. CONCLUSIONS

A practical FET microwave oscillator circuit was analyzed by the use of a new large signal model for the FET. Some of the simulation results were compared to published experimental data, and were in good agreement. The properties of the oscillator were investigated, and were found to be well predicted by the model.

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Large-Signal Technique for Designing Single-Frequency and Voltage-Controlled GaAs FET Oscillators

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Abstract—A systematic procedure is described for designing fixed-frequency and voltage-tuned GaAs FET oscillators for optimum large-signal performance. The approach is based on the use of a large-signal FET model for de-embedding dominant device nonlinearities, leading to a method which is both accurate and simple to apply. The viability of the technique is demonstrated with a 17-GHz fixed-frequency oscillator and a 7.4 to 13.1-GHz varactor-tuned oscillator. Design considerations as well as measured performance characteristics are discussed in detail.

I. INTRODUCTION

Continuing efforts to improve GaAs FET performance characteristics have predominantly been focused on amplifiers for both low-noise and high-power systems applications at increasingly higher microwave frequencies. The GaAs FET is also an attractive candidate for use in efficient microwave oscillators, including broad-band tunable sources. From the point of view of nonlinear device operation, the two types of circuits are quite similar. Thus, except for a few secondary aspects, device technology and device characterization techniques developed for amplifier purposes can be readily carried over to meet GaAs FET oscillator design needs as well.

Prior to the development of methods for describing and predicting large-signal GaAs FET behavior, oscillator designs have relied chiefly on small-signal criteria. Although these criteria generally lead to accurate predictions of oscillating frequency, they are of limited value when it comes to optimizing efficiency and RF output power performance. To cope with this difficulty, methods [1], [2] based on so-called large-signal device S-parameters have been proposed. The large-signal S-parameters provide a linearized description of fundamental frequency device-circuit interaction at elevated drive levels for device terminating impedances in the vicinity of those prevailing during measurement (typically 50 Ω). The amount of error inherent in the approximation becomes increasingly significant, the further the actual terminations deviate from their 50-Ω reference value. This is easily visualized with the help of a simple device model containing third-order nonlinearities [3]. In a practical oscillator design, where there are no predetermined bounds on the values the actual terminating impedances can assume, the viability of the large-signal S-parameter approach thus becomes questionable.

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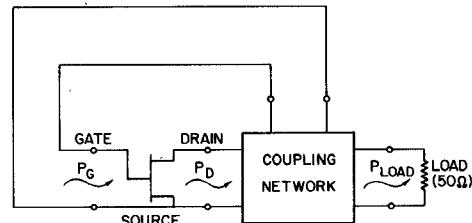


Fig. 1. GaAs FET oscillator.

Recently, a new method [4], [5] has been outlined which is aimed at overcoming previous limitations. It relies on a large-signal device model for de-embedding the dominant nonlinearities, leading to an exceptionally simple formulation of the optimum conditions for oscillation, while maintaining accuracy in predicting large-signal oscillator performance. This paper presents a comprehensive description of the technique and its experimental verification, supplying the details necessary to apply the method and to judge its reliability in assessing large-signal oscillator behavior. The general design approach for fixed-frequency oscillators is discussed in Section II, followed by the experimental verification thereof with a 17-GHz oscillator circuit in Section III. The application of the technique to voltage-controlled oscillators is described in Section IV, with an example of a VCO, tunable from 7.4 to 13.1 GHz, presented in Section V.

II. DESIGN OF FIXED-FREQUENCY OSCILLATORS

A. Basic Requirements for Achieving Optimum Oscillator Performance

The task of designing a transistor oscillator may be portrayed as that of synthesizing a three-port lossless coupling network (Fig. 1) which 1) yields a single stable state of oscillation, and 2) delivers maximum RF output power to an external (50-Ω) load for given bias conditions.

Approaches for satisfying the first constraint are relatively straightforward and are primarily concerned with parasitic oscillations and hysteresis effects. Spurious oscillations caused by parametric phenomena are normally absent in GaAs FET circuits, due to the dominance of resistive-type nonlinearities in the device. Consequently, states of oscillation and potential hysteresis effects can be checked out in the frequency domain [6] by recording

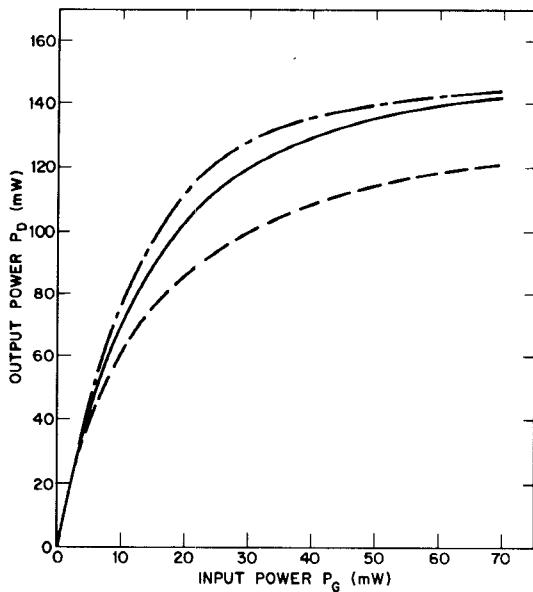


Fig. 2. Measured and approximated saturation characteristics for a single cell of an Avantek M110 GaAs FET at 8.5 GHz. — measured. - - - approximation (3). - · - · - approximation (4).

series and parallel system resonances under small-signal conditions, and then determining which of them—besides the one associated with the principal state of oscillation—might cause trouble. A conservative assessment is often appropriate in anticipation of circuit tolerances and spreads in device characteristics.

An obvious precaution is to choose coupling network configurations with minimum complexity in order to avoid, a priori, unnecessary resonances. This pertains especially to ones close to the principal frequency of oscillation. To suppress parasitic oscillations more remote from the principal frequency, additional stabilizing elements might be required. In single-frequency oscillators this can normally be achieved by augmenting the bias circuitry with lumped *RLC* elements, strategically placed so as not to interfere with RF output power performance.

Measures directed at satisfying the second constraint on the three-port coupling network (maximizing output power) are more complex and are the main topic of this paper. The general problem is to derive a systematic procedure for defining and implementing the optimum device terminating impedances and drain-to-gate feedback that produce maximum RF output power, P_{load} , while oscillating at only one frequency. For a lossless coupling network

$$P_{\text{load}}(\omega_0) = \max\{P_D(P_G, \omega_0) - P_G(\omega_0)\} \quad (1)$$

with P_D the RF power delivered by the transistor to its drain termination (Fig. 1), and P_G the power fed back into the gate port of the device to sustain oscillation at the angular frequency ω_0 . With reference to the basic oscillation requirement for establishing resonance at ω_0 , fundamental frequency *large-signal conjugate matching conditions* at both ports of the device are hereby implied for every pair of values (P_D, P_G). Equivalent to (1) is the familiar condition

$$\frac{\partial P_D(P_G, \omega)}{\partial P_G(\omega)} \Big|_{\omega=\omega_0} = 1. \quad (2)$$

To find the solution satisfying (2), the device saturation characteristics $P_D(P_G, \omega_0)$ must first be determined. The most direct approach is to acquire the data through measurement. This is a straightforward but relatively inconvenient task, provided a large-signal setup is available. In an attempt to circumvent the inconvenience associated with such measurements, the use of suitable approximations will be explored in this paper for describing saturation characteristics and determining optimum load conditions.

B. Empirical Description of Device Nonlinear Characteristics

With respect to the saturation function $P_D(P_G, \omega_0)$ two analytical approximations proposed in the recent literature [7], [2] are

$$P_D(\omega_0) = \left(\frac{1}{P_G(\omega_0) \cdot \tilde{\Gamma}(\omega_0)} + \frac{1}{P_{D\max}} \right)^{-1} \quad (3)$$

$$P_D(\omega_0) = P_{D\max} \cdot \left\{ 1 - \exp \left(-\tilde{\Gamma}(\omega_0) \cdot \frac{P_G(\omega_0)}{P_{D\max}} \right) \right\} \quad (4)$$

with $P_{D\max}$ the *maximum* achievable saturated output power for given bias conditions, and $\tilde{\Gamma}$ the *small-signal* maximum available power gain for the device in common source configuration. (Throughout this paper, the tilde is used to mark small-signal quantities.) As an illustrative example, Fig. 2 compares measured characteristics with those predicted from (3) and (4) for the 0.5- μm Avantek device used in experimental circuits described later on. The values provided by (4) are especially attractive, exhibiting a maximum deviation of less than 0.5 dB across the entire dynamic range. Equally good agreement has also been observed with devices from other manufacturers, such as with Texas Instruments 1.0- μm and 1.7- μm gate length devices [8], suggesting a more general applicability of (4) to

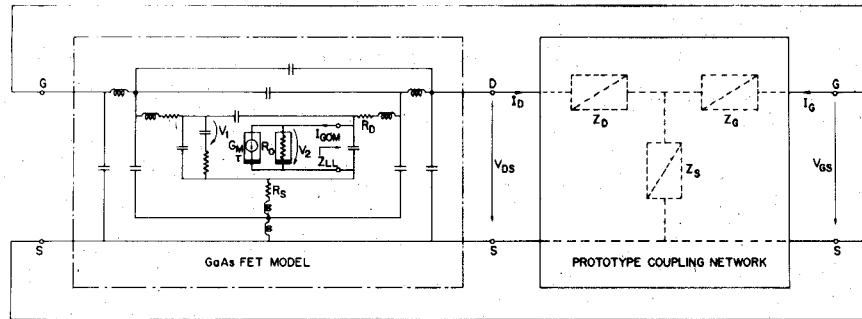


Fig. 3. Oscillator circuit with model of GaAs FET and two-port prototype of three-port coupling network.

GaAs FET's as a whole. Hence, (4) has been adopted as a viable approximation for use with in the present approach.

With $\tilde{\Gamma}(\omega_0)$ and $P_{D\max}$ parameters that can easily be determined, (2) and (4) lead to explicit optimum solutions for $P_D(\omega_0)$ and $P_G(\omega_0)$ [2], included for later reference:

$$P_{D\text{opt}}(\omega_0) = P_{D\max} \cdot \left(1 - \frac{1}{\tilde{\Gamma}(\omega_0)}\right) \quad (5)$$

$$P_{G\text{opt}}(\omega_0) = P_{D\max} \cdot \frac{\ln \tilde{\Gamma}(\omega_0)}{\tilde{\Gamma}(\omega_0)}. \quad (6)$$

Large-signal conjugate matching conditions at the device ports are assumed in these solutions, but the actual values of the corresponding device terminating impedances still remain undefined. In an effort to bypass large-signal measurements altogether, it would be desirable if the missing information could be acquired, again, through the use of empirical approximations. Unfortunately, this is not as easily accomplished as in the case of the power saturation characteristics, where the phase of the signal is not a primary concern. The problem arises from the device parasitics obscuring the intrinsic nonlinear mechanisms in a way which complicates the circuit design and is different for each individual device. The difficulty is resolved by employing a large-signal model to de-embed the intrinsic nonlinearities, resulting in an exceptionally simple composite solution to both the large-signal impedance question and the previous optimum feedback problem.

Due to the similarity between nonlinear device operation in power amplifiers and in oscillators, the results obtained in previous amplifier-oriented studies [8], [9] become applicable to the present design effort as well. The model used here, as depicted in the boxed-in portion of Fig. 3, recognizes only nonlinearities associated with the transconductance G_M and the output resistor R_O . These two elements produce the nonlinear fundamental-frequency effects of practical significance. Comprehensive verification of this claim has been provided in [8] based on demonstrated agreement between measurements and model predictions involving three different device geometries.

The values of the linear model elements and the small-signal values of the nonlinear elements are derived from measured small-signal S -parameters using familiar curve-fitting techniques. The model topology in Fig. 3 is, thereby, somewhat more elaborate than is generally required in amplifier applications. The additional complexity stems from the need to more readily distinguish between individual parasitic contributions when the device is used in a

configuration that differs from the one employed during initial experimental device characterization. Section V presents an example of such a situation, where a common-drain VCO design is based on a model derived from conventional common-source data.

The main issue is, of course, the assessment of the large-signal behaviors of the nonlinear elements and finding their optimum operating conditions. According to the model definition [8], [9], the instantaneous values for G_M and R_O can be described as time-invariant functions of the voltage across the intrinsic gate capacitor and the voltage across the intrinsic drain-source terminals. With reference to Fig. 3, it thus follows that the mode of oscillation is uniquely determined by three basic parameters, namely the fundamental frequency Fourier components of the two voltages, V_1 and V_2 , and the intrinsic load impedance Z_{LL} . By relying on these as principal design variables, the optimum gate-to-drain feedback and optimum load conditions, discussed earlier in terms of device-external power and impedance parameters, lend themselves to a particularly simple and coherent formulation.

C. Optimum Intrinsic Load Impedance

Due to the characteristics of the governing nonlinear mechanisms, the solutions for V_1 , V_2 , and Z_{LL} are all interrelated and, in principle, cannot be sought independently from one another. Nevertheless, it has been found that an independent approximation can be employed successfully in the case of Z_{LL} without introducing errors of practical significance. The approximation is based on the observation that both nonlinear model elements are resistive in nature and that, hence, the fundamental frequency current I_{GOM} (Fig. 3) through their parallel combination must be exactly out of angular phase with V_2 , the voltage across them. To satisfy the resonance requirement at the oscillating frequency ω_0 , noting that Z_{LL} includes the drain-source capacitance of the device

$$\text{Im}\{Z_{LL}(\omega_0)\} = 0. \quad (7)$$

The functional relationship between the instantaneous value of I_{GOM} and the instantaneous values of V_1 and V_2 fully define the combined nonlinear properties of G_M and R_O . This relationship, when plotted, establishes what has been termed the "dynamic I - V -characteristics" of the intrinsic device [9]. With regard to these characteristics, which are symbolically represented in Fig. 4, $Z_{LL}(\omega_0)$ can be interpreted as describing a resistive load line in accordance with (7). At low drive levels the optimum value of

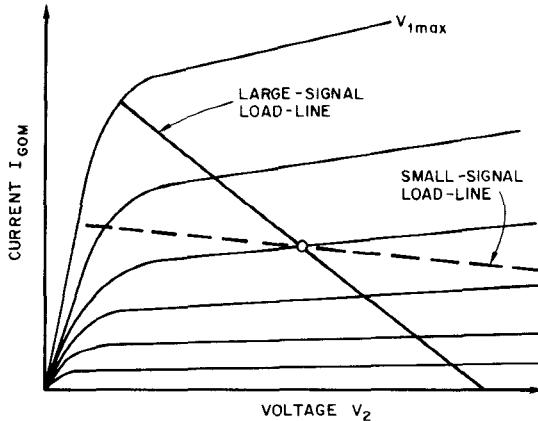


Fig. 4. Large-signal versus small-signal load lines in the I_{GOM} - V_2 plane.

$Z_{LL}(\omega_0)$ is equal to the small-signal value of R_O . This value is implicitly used in designs that rely entirely on small-signal device information. The optimum large-signal solution is determined by the value $Z_{LL}(\omega_0) = R_{LL\text{opt}}$ which maximizes the available power at the drain-source port of the device for a given amplitude of V_1 . As visualized in Fig. 4, large-signal and small-signal solutions are expected to differ considerably. It is also readily apparent that implementing a resistive value for $Z_{LL}(\omega_0)$ automatically leads to conjugately matched external device ports as prescribed by the resonance condition.

The optimum load-line resistance $R_{LL\text{opt}}$ is a function of drive level, but asymptotically approaches a limit value as the device is driven into saturation. The actual drive level is determined by (2) and typically requires device operation at around 2 to 3 dB of gain compression. The optimum load line under these conditions turns out to be very close to the limit case, suggesting the use of this limit value as an approximation to $R_{LL\text{opt}}$.

For given bias voltages, the limit value corresponds to the load line that yields the maximum product of current swing times voltage swing in the dynamic I_{GOM} - V_2 plane, with V_1 varying between the bounds determined by pinch-off and gate forward conduction (Fig. 4). Simple graphical means can be applied to find the asymptotic load line, provided the bounding forward conduction I_{GOM} - V_2 curve is known. This curve could be acquired with the quasi-static modeling technique [9], based on four or five small-signal device S-parameter measurements at selected bias-voltage combinations. The approach pursued here, though, is to establish an estimate derived from 1) the measured static device I_{DS} - V_{DS} characteristics, 2) the similarity between these and the dynamic characteristics [9], and 3) the knowledge of the small-signal values of the resistive model elements at the nominal bias point. The errors experienced when relying on this estimate for determining the asymptotic load-line impedance prove to be relatively insignificant when compared to uncertainties arising from typical spread in device characteristics. This assertion is supported by both of the oscillator examples investigated in detail later, whose designs rely on this approximation.

D. Optimum Intrinsic Voltage Feedback Conditions

The next step is to derive optimum values for V_1 and V_2 , $V_{1\text{opt}}$ and $V_{2\text{opt}}$, that satisfy the feedback condition (2). This is accomplished by relying on the solutions (5) and (6) given in terms of device-external power levels and relating these to the intrinsic voltage variables V_1 and V_2 . As for the conditions at the conjugately matched drain port of the device (Fig. 1), the optimum power level $P_{D\text{opt}}$ to be substituted into (5) can be written as

$$P_{D\text{opt}}(\omega_0) = \gamma \cdot \frac{|V_{2\text{opt}}(\omega_0)|^2}{R_{LL\text{opt}}} \quad (8)$$

The proportionality factor γ can be estimated based on knowledge of the small-signal model parameters. Neglecting drain-to-gate feedback yields (Fig. 3)

$$\gamma \approx \frac{R_{LL\text{opt}} - R_S - R_D}{R_{LL\text{opt}}} \quad (9)$$

as a viable working assumption. The saturated value of $P_{D\text{opt}}(\omega_0)$ is determined by $V_{2\text{max}}$, the square-wave peak-to-peak voltage swing of V_2 along the $R_{LL\text{opt}}$ load line as constrained by pinch-off and forward conduction of the Schottky barrier:

$$P_{D\text{max}} \approx \gamma \cdot \frac{2}{\pi^2} \cdot \frac{V_{2\text{max}}^2}{R_{LL\text{opt}}} \quad (10)$$

Device-circuit interaction at the gate port is known to be essentially power-independent, leading to a proportionality between $P_{G\text{opt}}$ and $|V_{1\text{opt}}|^2$ analogous to (8). Although the exact relationship can, of course, be calculated in a straightforward way from the small-signal device model, it can also be approximated, for practical purposes, by

$$P_{G\text{opt}}(\omega_0) = \gamma \cdot \tilde{G}_M^2 \cdot \left(\frac{\tilde{R}_O \cdot R_{LL\text{opt}}}{\tilde{R}_O + R_{LL\text{opt}}} \right)^2 \cdot \frac{1}{\tilde{\Gamma}(\omega_0)} \cdot \frac{|V_{1\text{opt}}(\omega_0)|^2}{R_{LL\text{opt}}} \quad (11)$$

with \tilde{G}_M and \tilde{R}_O the previously determined small-signal values for transconductance and drain-source resistance,

respectively (Fig. 3). Substituting (8), (10), and (11) into (5) and (6), while also taking the time-delay τ (Fig. 3) into account, yields

$$V_{2\text{opt}}(\omega_0) = \frac{\sqrt{2}}{\pi} \cdot V_{2\text{max}} \cdot \sqrt{1 - \frac{1}{\tilde{\Gamma}(\omega_0)}} \cdot e^{-j\omega_0\tau} \quad (12)$$

and

$$V_{1\text{opt}}(\omega_0) = \frac{\sqrt{2}}{\pi} \cdot V_{2\text{max}} \cdot \frac{1}{\tilde{G}_M} \cdot \frac{\tilde{R}_O + R_{LL\text{opt}}}{\tilde{R}_O \cdot R_{LL\text{opt}}} \cdot \sqrt{\ln \tilde{\Gamma}(\omega_0)} \quad (13)$$

whereby the phase angle of $V_{1\text{opt}}$ has arbitrarily been set equal to zero. These solutions are implicitly based on the interrelationship between V_1 and V_2 , represented by

$$|V_2| = \frac{\sqrt{2}}{\pi} \cdot V_{2\text{max}} \cdot \sqrt{1 - \exp \left\{ -\frac{\pi^2}{2} \cdot \left(\tilde{G}_M \cdot \frac{\tilde{R}_O \cdot \tilde{R}_{LL\text{opt}}}{\tilde{R}_O + R_{LL\text{opt}}} \cdot \frac{|V_1|}{V_{2\text{max}}} \right)^2 \right\}}. \quad (14)$$

It is noted that this postulated expression is independent of device parasitic effects, unlike the approximation (4) which (14) replaces.

E. Synthesis of Optimum Coupling Network

Once the values of Z_{LL} , V_1 , and V_2 have been defined in accordance with the preceding outline, the device-external voltages and currents V_D , V_G , I_D , and I_G , are fixed. Their values can be calculated from the model by way of a sequence of simple variable substitutions into Kirchhoff equations. The model topology permits these substitutions to be carried out without the need for an explicit matrix inversion. Assuming, again, the coupling network in Fig. 1 to be lossless, the power delivered to the 50Ω external load then follows from (1), noting the current direction convention used in Fig. 3

$$P_{\text{load}}(\omega_0) = \text{Re} \{ V_D(\omega_0) \cdot I_D^*(\omega_0) \} + \text{Re} \{ V_G(\omega_0) \cdot I_G^*(\omega_0) \}. \quad (15)$$

Due to having neglected, in effect, parasitic feedback internal to the device when deriving (12) and (13), expression (15) will give a value for P_{load} that falls slightly short of the actual maximum. The deviation is typically of the order of 0.5 dB. The true optimum can be sought by repeating the evaluation of (15) for a series of perturbed values of $V_{1\text{opt}}$ and $V_{2\text{opt}}$ consistent with (14). This simple iterative procedure was used in both of the oscillator examples to be discussed.

The next step is to derive coupling network configurations that satisfy the boundary conditions specified in terms of the prescribed voltages and currents at the external device ports. Minimum complexity networks that provide the required four degrees of freedom contain three

TABLE I
PROTOTYPE ELEMENT VALUES FOR T-CONFIGURATION

CASE	Z_G	Z_S	Z_D
$\text{Re} \{ Z_G \} = \text{Re} \{ Z_S \} = 0$	$j \frac{\text{Re} \{ V_G \cdot (I_G^* + I_D^*) \}}{\text{Im} \{ I_G^* \cdot I_D^* \}}$	$j \frac{\text{Re} \{ V_G \cdot I_G^* \}}{\text{Im} \{ I_G \cdot I_D^* \}}$	$\frac{V_D}{I_D} - Z_S \left(1 + \frac{I_G}{I_D} \right)$
$\text{Re} \{ Z_G \} = \text{Re} \{ Z_D \} = 0$	$j \frac{\text{Re} \{ I_D \cdot (V_D^* - V_G^*) \}}{\text{Im} \{ I_G \cdot I_D^* \}}$	$\frac{V_G - Z_G \cdot I_G}{I_G + I_D}$	$j \frac{\text{Re} \{ I_G \cdot (V_G^* - V_D^*) \}}{\text{Im} \{ I_D \cdot I_G^* \}}$
$\text{Re} \{ Z_S \} = \text{Re} \{ Z_D \} = 0$	$\frac{V_G}{I_G} - Z_S \left(1 + \frac{I_D}{I_G} \right)$	$j \frac{\text{Re} \{ V_D \cdot I_D^* \}}{\text{Im} \{ I_D \cdot I_G^* \}}$	$j \frac{\text{Re} \{ V_D \cdot (I_D^* + I_G^*) \}}{\text{Im} \{ I_D^* \cdot I_G \}}$

TABLE II
PROTOTYPE ELEMENT VALUES FOR II-CONFIGURATION

CASE	Y_{GS}	Y_{GD}	Y_{DS}
$\text{Re} \{ Y_{GS} \} = \text{Re} \{ Y_{GD} \} = 0$	$j \frac{\text{Re} \{ I_G \cdot (V_D^* - V_G^*) \}}{\text{Im} \{ V_G^* \cdot V_D \}}$	$j \frac{\text{Re} \{ I_G \cdot V_G^* \}}{\text{Im} \{ V_G^* \cdot V_D \}}$	$\frac{I_D}{V_D} + Y_{GD} \left(\frac{V_G}{V_D} - 1 \right)$
$\text{Re} \{ Y_{GS} \} = \text{Re} \{ Y_{DS} \} = 0$	$\frac{\text{Re} \{ V_D \cdot (I_D^* + I_G^*) \}}{\text{Im} \{ V_G^* \cdot V_D \}}$	$\frac{Y_{GS} \cdot V_G - I_G}{V_D - V_G}$	$j \frac{\text{Re} \{ V_G \cdot (I_D^* + I_G^*) \}}{\text{Im} \{ V_D^* \cdot V_G \}}$
$\text{Re} \{ Y_{GD} \} = \text{Re} \{ Y_{DS} \} = 0$	$\frac{I_G}{V_G} + Y_{GD} \cdot \left(\frac{V_D}{V_G} - 1 \right)$	$j \frac{\text{Re} \{ I_D \cdot V_D^* \}}{\text{Im} \{ V_D^* \cdot V_G \}}$	$j \frac{\text{Re} \{ I_D \cdot (V_G^* - V_D^*) \}}{\text{Im} \{ V_D^* \cdot V_G \}}$

lumped circuit elements in the form of two reactances and one (lossy) complex element. The elements can be arranged either in a T- or a Π -configuration, thereby defining a two-port prototype of the actual three-port coupling network. An example of a T-configuration is indicated in Fig. 3. The lossy element, which implicitly accounts for the external 50Ω load in the actual circuit, can in principle occupy any one of the three possible locations in either of the prototype circuits. The resulting generality permits essentially all oscillator design alternatives of practical interest to be treated in a simple unified way. Also, it should be noted that the approach can easily be adapted to include configurations which do not fit the basic T or Π format.

The actual choice between T- or Π -configuration is primarily determined by the necessity to minimize the number of resonances in the vicinity of ω_0 in order to avoid parasitic oscillation effects. The choice is particularly crucial in broad-band VCO designs. For gate and drain operating near series resonance, for instance, the series-element T-configuration is generally preferred. This situation normally occurs when using devices in chip form. The decision of where to position the lossy element within the chosen topology is guided by physical realizability considerations. The decision process is aided by the ease with which the method allows the possible alternatives to be evaluated and their individual merits to be compared. The expressions for calculating the prototype element values from the optimum values for V_D , V_G , I_D , and I_G (Fig. 5) are summarized in Tables I and II.

The final step in the design procedure is the physical implementation of the prototype network. This step is simple in a lumped-element design as might be required for monolithic realization. The next section shows an example of a distributed implementation, while a semilumped circuit is discussed in Section V.

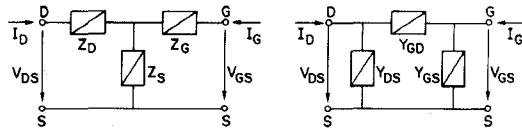


Fig. 5. The two basic prototype topologies.

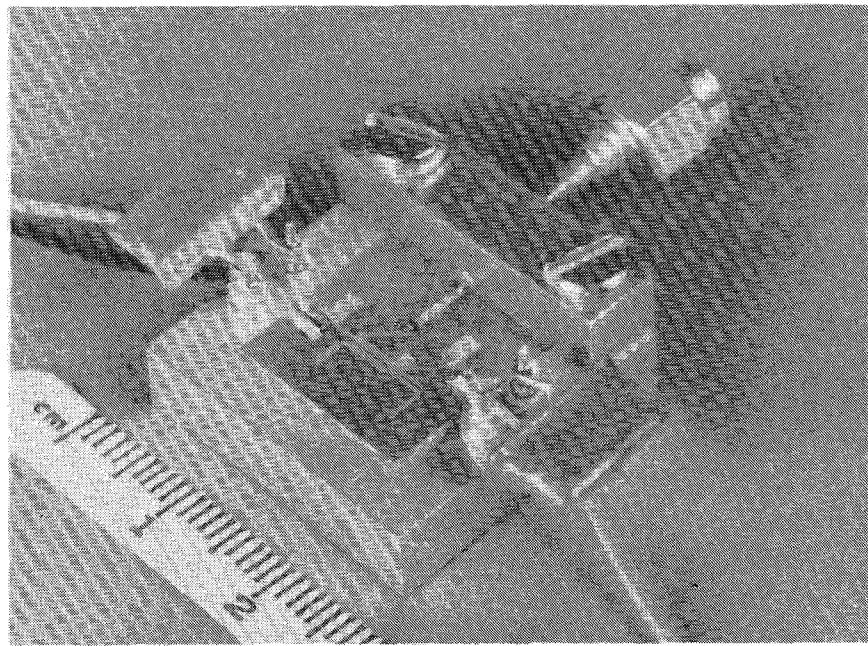


Fig. 6. Experimental 17-GHz GaAs FET oscillator with distributed element coupling network.

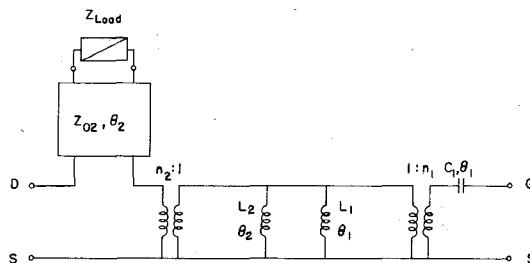


Fig. 7. Equivalent circuit of distributed 17-GHz coupling network.

III. A 17-GHz FIXED-FREQUENCY OSCILLATOR EXAMPLE

To demonstrate the viability of the technique, the described procedure has been applied to the design of a 17-GHz fixed-frequency oscillator. Its distributed element implementation, realized as a coupled-line microstrip circuit on a 0.25-mm Duroid substrate, is depicted in Fig. 6. The design is based on a T-prototype with the load element in series with the drain lead of the device. The T-configuration is evident from the equivalent distributed circuit of the coupling network shown in Fig. 7, in which inductors and capacitors symbolize short-circuited and open-circuited stubs of electrical lengths θ_1 and θ_2 , respectively, in accordance with the notation introduced by Wenzel [10]. The distributed design offers more degrees of freedom than are actually required. This flexibility can be utilized to accommodate physical realizability constraints

without adding new undesirable system resonances in the vicinity of the oscillating frequency.

The device employed in the circuit is a single cell of an Avantek M110 device [11] having a $0.5\text{-}\mu\text{m} \times 375\text{-}\mu\text{m}$ gate geometry. With the transistor biased for operation at a drain-source voltage of 4 V and a drain current of $0.6 \cdot I_{DSS}$, the design theory estimates the 17-GHz RF output power from the oscillator at 18 dBm, based on an optimum intrinsic load-line resistance $R_{LL\text{opt}} = 50 \Omega$. The estimate is in close agreement with the measured performance of the actual oscillator, yielding a maximum of 17.5 dBm of output power with 21-percent efficiency at a drain-source bias voltage of 3.8 V. By lowering the voltage to 3.0 V the efficiency increased to 25 percent while the output power dropped to 16.5 dBm. As predicted, the frequency selectivity of the distributed coupling network, in conjunction with two supplementary RC damping elements added to the

gate and drain bias circuits, effectively suppressed all parasitic oscillations.

IV. DESIGN OF VOLTAGE-CONTROLLED OSCILLATORS

The optimum design of a voltage-controlled oscillator involves meeting the criteria developed in Section II at each tuned oscillating frequency within the band of interest. This leads, in terms of prototype circuit elements, to uniquely prescribed frequency responses of their impedance values. The individual impedance functions are determined through repeated implementation of the fixed-frequency procedure for a representative set of frequency samples covering the anticipated tuning bandwidth. The choice of prototype configuration warrants particular scrutiny. This choice becomes crucial in wide-band applications where it is important to rule out in-band antiresonances that could introduce frequency jumping and hysteresis effects in the tuning characteristics. Equal care must be devoted, of course, to preserving essential prototype characteristics during the physical implementation of the oscillator circuit.

Independent of prototype configuration, the required frequency responses of the two prototype reactances generally exhibit negative slopes. Voltage-controlled elements, such as varactors or YIG-devices, are hence needed to satisfy the reactance requirements. For the sake of simplicity, the present discussion concentrates on varactor-tuned circuits for situations where frequency agility is essential, although the approach can be applied just as easily to the design of YIG-tuned oscillators. For both types of tuning it is important to note that optimum exploitation of transistor power-bandwidth capabilities will normally call for two separate tuning elements. This is illustrated with the VCO example detailed in Section V which demonstrates that substantial performance degradation results if tuning is confined to merely one circuit element.

The tuning bandwidth achievable with a specific transistor is primarily determined by the ranges of reactance values that can be spanned for given maximum varactor capacitance variation, and by the constraints associated with the physical implementation of the lossy load-related prototype element. An obvious approach to realizing the load element is to synthesize its prescribed optimum impedance function as the driving point impedance of a lossless two-port network terminated in the external 50- Ω load resistor. This problem can be solved with conventional matching techniques. As for the tuning reactances, they should preferably be implemented in lumped-element form to preserve bandwidth. In practice this is accomplished by using lengths of bond wire or other types of lumped inductors to resonate varactor capacitances. The combination of varactor and inductor(s) is chosen so that the total reactance $X_T(\omega_0)$ exhibits smooth tunability within the frequency tuning interval $\omega_L \leq \omega_0 \leq \omega_H$ in accordance with the range of reactance values specified by the prototype. In realizing a series connected prototype reactance, augmentation of the varactor with a series inductor will normally be called for, with the dual thereof applying to a

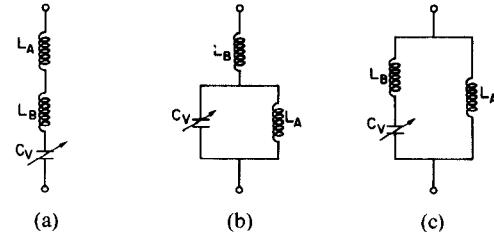


Fig. 8. Lumped-element realizations of varactor-tuned reactances.

parallel connected prototype element. Three examples are illustrated in Fig. 8, in each of which L_A represents the external inductor and L_B accounts for an assumed fixed minimum lead inductance associated with the varactor chip. For calculation purposes, it is easiest to lump varactor losses with the transistor part of the circuit. With a maximum achievable varactor capacitance ratio $\rho_{\max} = C_{V\max}/C_{V\min}$, and specified limit values $X_T(\omega_L)$ and $X_T(\omega_H)$, the inductor L_A , and the relationship between varactor capacitance C_V and angular oscillating frequency ω_0 for the series type circuit in Fig. 8(a) must be chosen according to

$$L_A = \frac{\omega_L \cdot \rho_{\max} \cdot X_T(\omega_L) - \omega_H \cdot X_T(\omega_H)}{\omega_L \cdot \omega_H \cdot ((\omega_L \cdot \rho_{\max} / \omega_H) - (\omega_H / \omega_L))} - L_B \geq 0 \quad (16)$$

$$C_V(\omega_0) = \frac{1}{\omega_0 \cdot (\omega_0 \cdot L_A + \omega_0 \cdot L_B - X_T(\omega_0))}, \quad \omega_L \leq \omega_0 \leq \omega_H. \quad (17)$$

The analogous expressions for the parallel resonated circuit in Fig. 8(b) are

$$L_A = \frac{(\omega_L \cdot \rho_{\max} / \omega_H) - (\omega_H / \omega_L)}{(\omega_H / (X_T(\omega_L) - \omega_L \cdot L_B)) - (\omega_L \cdot \rho_{\max} / (X_T(\omega_H) - \omega_H \cdot L_B))} \geq 0 \quad (18)$$

$$C_V(\omega_0) = \frac{1}{\omega_0} \cdot \left(\frac{1}{X_T(\omega_0) - \omega_0 \cdot L_B} + \frac{1}{\omega_0 \cdot L_A} \right), \quad \omega_L \leq \omega_0 \leq \omega_H. \quad (19)$$

For the circuit in Fig. 8(c) one obtains

$$L_A = \frac{1}{P \pm \sqrt{P^2 - Q}} \geq 0 \quad (20)$$

$$C_V(\omega_0) = \frac{1}{\omega_0} \cdot \left(\omega_0 \cdot L_B - \frac{1}{(1/X_T(\omega_H)) - (1/(\omega_0 \cdot L_A))} \right)^{-1}, \quad \omega_L \leq \omega_0 \leq \omega_H \quad (21)$$

with

$$P = \frac{1}{2} \cdot \left\{ \frac{\omega_L}{X_T(\omega_L)} + \frac{\omega_H}{X_T(\omega_H)} - \frac{1}{L_B} \right\}$$

$$Q = \frac{\omega_L \cdot \omega_H}{X_T(\omega_L) \cdot X_T(\omega_H)} - \frac{1}{L_B}$$

$$\cdot \frac{(\omega_H / X_T(\omega_L)) - (\omega_L \cdot \rho_{\max} / X_T(\omega_H))}{(\omega_H / \omega_L) - (\omega_L \cdot \rho_{\max} / \omega_H)}.$$

Naturally, situations also arise where (16)–(21) indicate the need for supplementing the varactor with a capacitor rather than an inductor. The net effect is to reduce the actual capacitance variation. The simplest solution involves relaxing the requirements on ρ_{\max} by utilizing only part of the total available capacitance variation ρ according to

$$\rho = \frac{\omega_H \cdot (X_T(\omega_H) - \omega_H \cdot L_B)}{\omega_L \cdot (X_T(\omega_L) - \omega_L \cdot L_B)} < \rho_{\max} \quad (22)$$

and

$$C_V(\omega_0) = \frac{1}{\omega_0 \cdot (\omega_0 \cdot L_B - X_T(\omega_0))}, \quad \omega_L \leq \omega_0 \leq \omega_H. \quad (23)$$

In assessing the limitations associated with the varactors it should be observed that RF varactor voltage swings in practical oscillator circuits can be quite large. It is thus essential to adequately account for the large-signal varactor properties, which can be accomplished through direct large-signal impedance measurements [12]. The chief consequence of elevated RF drive is to lower the effective varactor capacitance value and to increase losses, whereby the discrepancies between small-signal and large-signal values are most apparent for bias voltages at which the RF voltage starts swinging into the forward bias region. When compared to predictions based solely on small-signal varactor characteristics supplied by the manufacturer, this translates into reduced tuning bandwidth, particularly at the low end.

The optimum RF power level achievable for each frequency setting decreases with increasing frequency due to transistor gain rolloff. However, if merely an overall lower limit on output power is specified, it is possible to trade excess power available at the lower frequencies against additional bandwidth and relaxed physical realization constraints. This can be accomplished by allowing both the intrinsic load-line resistance and the intrinsic voltage feedback ratios to deviate from their respective calculated optimum values $R_{LL\text{opt}}$ and $V_2(\omega_0)/V_1(\omega_0)$, $\omega_L \leq \omega_0 \leq \omega_H$. A numerical optimization scheme analogous to the one applied to the design of a negative resistance VCO [13] can be employed to assist in the tradeoff evaluation. This approach has not been pursued in the present investigation. Rather, the example described in the following section illustrates how possible tradeoffs can be assessed and implemented without the need for sophisticated computational tools.

V. EXAMPLE OF A BROAD-BAND VARACTOR-TUNED OSCILLATOR

The goal set for this example was to achieve a flat output power response over the frequency range from 8.0 to 12.0 GHz utilizing the 750- μm total gate width of the two-cell 0.5- μm gate-length Avantek device [11]. Both T- and Π -type configurations were investigated, applying the procedure outlined in the previous section. All Π -type solutions disqualified themselves because of in-band antiresonances.

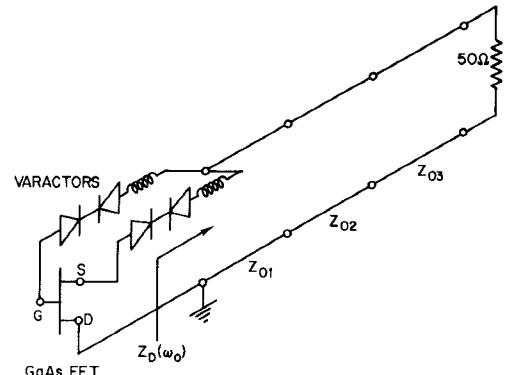


Fig. 9. Schematic of broad-band tunable oscillator circuit.

The T-configuration with the load-element in series with the gate of the device was also discarded due to severe tuning bandwidth limitations dictated by the pertinent realizability constraints. Between the two remaining feasible T-type alternatives the one with the load element in series with the drain lead appeared most attractive.

A schematic of the chosen overall circuit concept is shown in Fig. 9. The prototype load element is synthesized as a cascade of three transmission line elements terminated in 50Ω . The drain of the device is grounded to facilitate realization in microstrip. Each of the two tuning elements contains a series combination of two individual varactors, in order to use commercially available Microwave Associates MA 46629 hyperabrupt varactor chips and still achieve the low capacitance values associated with wide-band tunability. To preserve bandwidth, lumped inductors are employed, implemented in the form of interconnecting bond wires.

Designing an oscillator to maintain the optimum intrinsic load impedance $R_{LL\text{opt}}$ at all frequencies within the band can be accomplished, as discussed previously, by calculating the corresponding prototype element impedance responses and correlating them with physical realizability. If tradeoffs are to be considered, the calculations must be repeated for a representative number of values of $R_{LL} \geq R_{LL\text{opt}}$ and $V_2/V_1 \geq V_{2\text{opt}}/V_{1\text{opt}}$. The compilation of the data can be accomplished very efficiently due to the simplicity of the individual analyses. A set of mutually compatible solutions is then chosen from the data so as to establish prototype frequency characteristics in accordance with the tradeoff objectives. For a given prototype configuration and given technological limits on minimum varactor size, tradeoffs involving the physical implementation of the load element are generally the primary contributors to design flexibility. To illustrate this, the prototype load element impedance for the present VCO example has been plotted in Fig. 10(a) and 10(b) as a function of frequency F and intrinsic load-line resistance R_{LL} for two specific values of V_2/V_1 . The response yielding maximum RF power at each frequency setting corresponds to the locus for $R_{LL} = R_{LL\text{opt}} = 30 \Omega$ in Fig. 10(b). Also indicated in Fig. 10(b) is the more readily implemented characteristic labeled Z_D which represents the driving point impedance of the

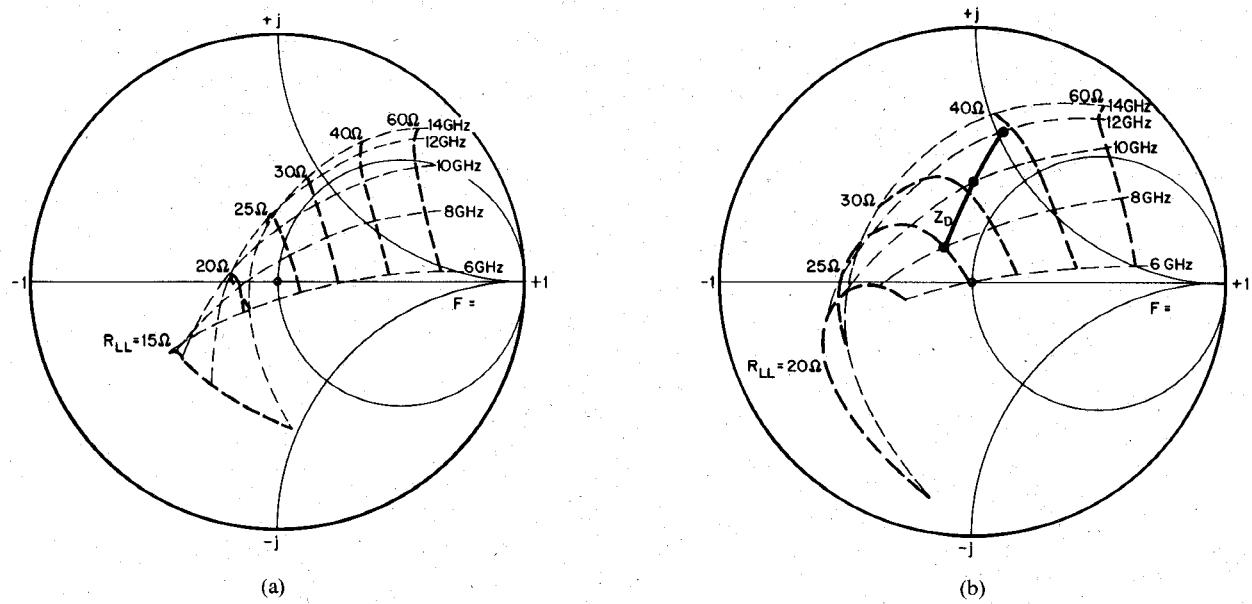


Fig. 10. Prototype load impedance Z_D , normalized to $Z_0 = 10 \Omega$, as a function of frequency F and load-line resistance R_{LL} . (a) $V_2/V_1 = 0.8 \cdot V_{2\text{opt}}/V_{1\text{opt}}$; (b) $V_2/V_1 = V_{2\text{opt}}/V_{1\text{opt}}$.

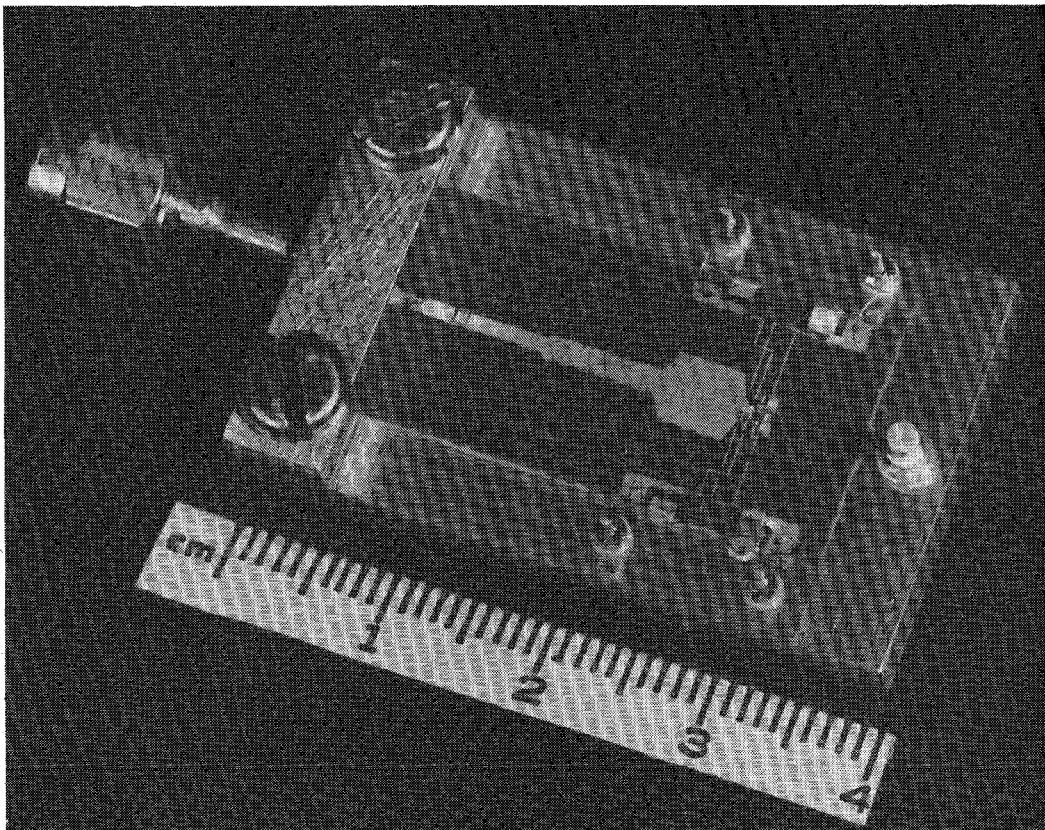


Fig. 11. Varactor-tuned 7.4- to 13.1-GHz GaAs FET oscillator.

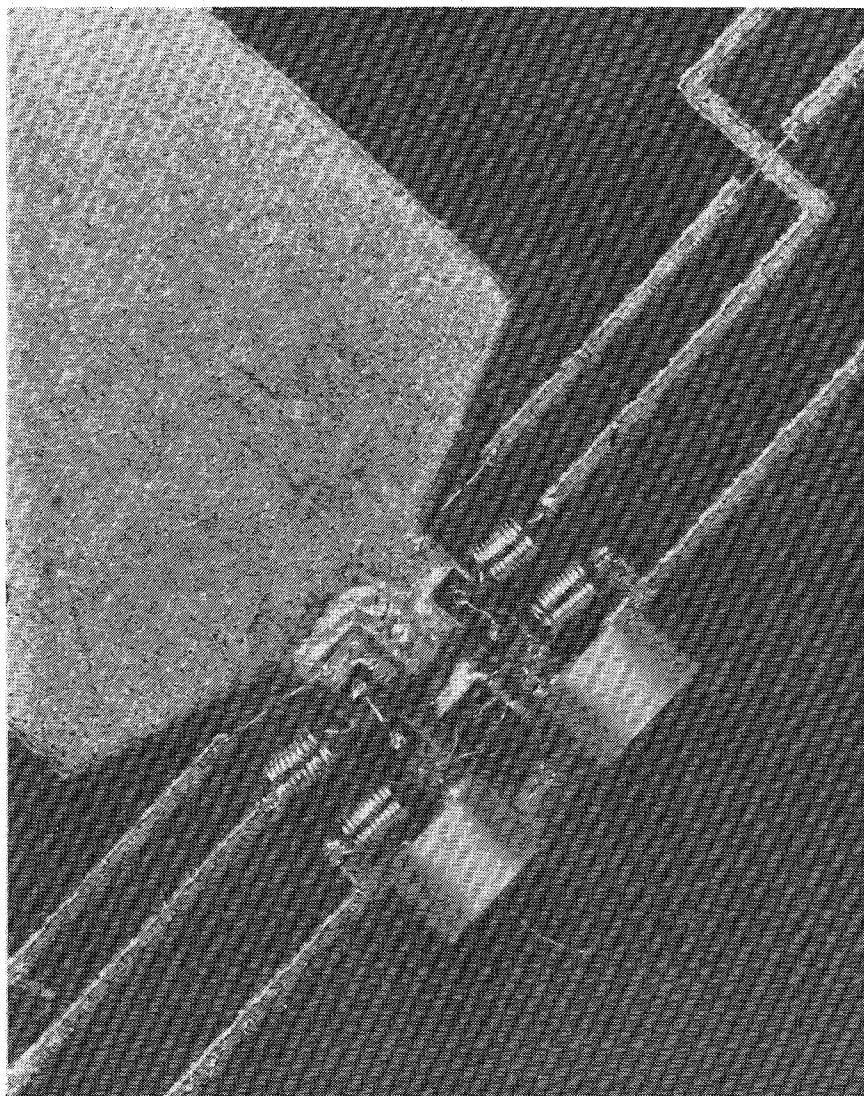


Fig. 12. Close-up view of transistor and dual tuning arrangement.

cascaded transmission line structure indicated in Fig. 9. Improved realizability was achieved through sacrifice of only 0.5 dB in minimum output power, while flattening the output power versus frequency response at the same time.

The actual oscillator circuit, built on a 0.25-mm Duroid substrate, is depicted in Fig. 11. A close-up view of the immediate vicinity of the transistor and the tuning arrangement is given in Fig. 12. The miniature 0.3-mm diameter choke coils, consisting of ten turns of 25- μ m diameter gold wire, supply the bias voltages to the transistor and the varactors. The coils are connected to RF short-circuited high impedance quarter-wavelength stubs to form a broadband composite bias circuit. Effective in-band safeguarding against spurious oscillations is accomplished by adding a 50- Ω resistor in parallel with the bias chokes at gate and source.

The oscillator design is based on a conservative maximum capacitance ratio $C_{V_{\max}}/C_{V_{\min}}$ of 6:1. The reason for this conservative assumption was to provide enough built-in latitude in order to obtain the specified 8.0- to 12.0-GHz bandwidth without involving post-design tweaking of the circuit. (This would have called for replacing

bond wires which was judged impractical.) The capacitance ratios of the actual varactors used were in excess of 6:1, providing a larger tuning interval than initially specified, namely from 7.4 to 13.1 GHz. Measured and predicted RF output power responses are given in Fig. 13, together with the associated gate and source varactor tuning voltages V_{VG} and V_{VS} , respectively. The agreement between experiment and prediction is judged to be well within the range of uncertainty determined by spread in device characteristics and circuit tolerances.

The main purpose of the example has been to verify the viability of the design technique rather than to demonstrate, for instance, maximum bandwidth capabilities. It was noted, however, that disconnecting the two 50- Ω stabilizing resistors increased the tuning range by an additional 500 MHz. This did not impair smooth tunability as long as the varactor bias voltages tracked monotonically according to Fig. 13. However, unlike the situation with the stabilizing resistors in place, the signal exhibited a tendency to "break up" at midband frequencies when the tracking criterion was relaxed.

The present technique is based on the observation that

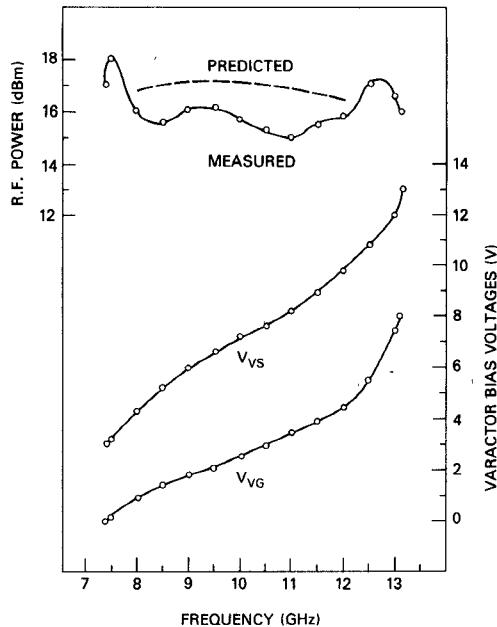


Fig. 13. Measured and predicted RF output power performance, together with associated gate and source varactor tuning voltages V_{VG} and V_{VS} , respectively.

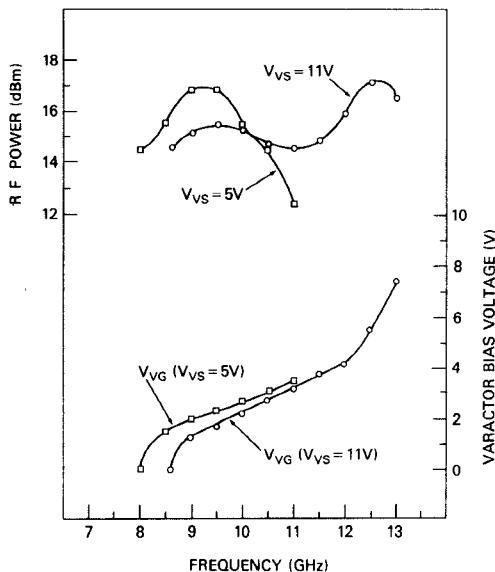


Fig. 14. Measured tuning characteristics for fixed values of source varactor tuning voltage V_{VS} .

two independent tuning elements are needed to obtain optimum performance with a given transistor. In order to assess the actual impact of the approach described here, a conventional single element tuning arrangement was simulated by holding V_{VS} fixed, while varying only the more frequency sensitive gate varactor bias voltage V_{VG} . Fig. 14 shows the tuning characteristics of the oscillator with the source varactor biased at $V_{VS} = 5$ V and $V_{VS} = 11$ V, respectively. The bandwidth in the latter case spanned 8.6 to 13.0 GHz, representing the *maximum* frequency range obtainable when restricted to tuning only at the gate. Thus, in this particular experiment, using *two* tuning elements as opposed to *one* leads to an increase in bandwidth of 30 percent. Even though this remains an isolated test example,

it nevertheless provides insight into the practical significance of the role played by the second tuning element.

VI. CONCLUSIONS

A generalized approach to designing GaAs FET oscillators has been described. Among the distinguishing features are its reliability in predicting large-signal oscillator performance and the underlying simplicity of the overall procedure. The crux of the method is to de-embed the nonlinearities of the transistor with the help of a circuit-type model, leading to a concise formulation of optimum oscillating conditions in terms of intrinsic voltage and current variables. It has been demonstrated that the essential information regarding device nonlinearities can be adequately

reconstructed, for practical purposes, from the static I_{DS} – V_{DS} curves and the small-signal model of the device. This provides an attractive alternative to deriving the information from actual large-signal measurements. The technique has been successfully applied to the design of a fixed-frequency and a broad-band varactor-tuned oscillator, yielding good agreement between predictions and experiments. In the case of the varactor-tuned circuit it has been shown, in particular, that two independent tuning elements are indeed essential if the power-bandwidth capabilities of the transistor are to be fully exploited, whereby the same arguments apply to YIG-tuned circuits.

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10-GHz 10-W Internally Matched Flip-Chip GaAs Power FET's

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MUTSUYUKI OTSUBU, AND TAKASHI ISHII

Abstract—A newly developed internally matched configuration for a flip-chip GaAs power field effect transistor is presented. In this structure, gate and drain electrodes of the FET chips are directly connected to the lumped dielectric capacitors in the matching networks by thermocompression bonding using no wire. A power output of 10 W with 3-dB gain and a power added efficiency as high as 14 percent has been realized at 10 GHz.

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I. INTRODUCTION

RECENT advances in GaAs field effect transistor technology have steadily improved the power output and power gain capabilities of the device over the frequency range from S- to Ku-band [1]. Nowadays, solid-state power GaAs FET amplifiers are extensively used in telecommunication and phased array radar systems [2], [3]. High power output levels in the X-band frequency range are demanded for these applications.

For obtaining higher power output, various types of

Design of a C-Band Microstrip Voltage Controlled Oscillator Using an Electromagnetic-Harmonic Balance Co-Design Technique

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Abstract—A Voltage Controlled Oscillator (VCO) was designed for operation in C-Band for use in a microwave point-to-point radio system. Microstrip technology was chosen for resonator implementation since it offers ease of manufacturing and frequency adjustment. The design was performed using an Electromagnetic (EM)-Harmonic balance Co-design technique in order to achieve first pass success. The measured frequency versus tune voltage data shows excellent agreement with simulation. Maximum deviation of 2% between the two was observed. The VCO tuned from 4.3 GHz to 5.4 GHz as the tuning voltage was varied from 0 to 9V representing a tuning bandwidth in excess of 20%. Phase noise over the tune range was better than -108dBc/Hz at 100 kHz offset.

Keywords- *VCO; Oscillator; Microstrip; Electromagnetic Simulation; Resonator; Varactor; Harmonic Balance; Tuning; Negative Conductance*

I. INTRODUCTION

Tunable oscillators which provide ease of manufacturing, and adaptation to multiple frequencies are desirable for multi-functional communication systems operating over several frequency bands. These facets coupled with good performance and rapid implementation demand techniques that permit first pass design success. This work discusses a methodology which utilizes a combination of rapid simulation based on lumped element models, scattering parameter tables and closed form electromagnetic (EM) simulation networks. Then this simulation is followed by careful co-simulation using planar EM and harmonic balance techniques applied to the circuit board and active circuit respectively. The initial process assists in quickly establishing circuit topologies that permit design targets to be achieved and initializing computer aided design (CAD) layout. Iterative simulation and progressive CAD layout quickly identifies critical element placements and permits re-adjustment of the printed card network prior to exhaustive EM simulation.

The use of harmonic balance for design of frequency selective circuits is well established and has been used for many years. Similarly, electromagnetic simulation tools have been previously used to accurately extract parasitics. However, a closed loop design technique demonstrating the use of EM and harmonic balance co-design technique and the correlation

of measured data with simulated data is not readily available in the literature. This is especially true for VCO design. This work attempts to fill the gap.

II. DESIGN

Initial circuit design is based on mapping techniques applied to an oscillator circuit operating in the common base configuration. This process consists of plotting regions on the Smith Chart which permit sufficient negative conductance to support oscillation for the desired frequency range. Mapping regions are a function of the load impedance, series feedback reactance, and resonator characteristics. The fundamentals as outlined in the work by Kurokawa [1] are extended over the desired tuning range. The active circuit topology is analyzed for input reflection coefficient [2] which is influenced by CAD layout and associated modeled parasitics. Subsequently, resonator design is investigated again based on simple transmission line models to permit fast and preliminary assessment of circuit operation. Linear simulation permits valuable guidance; for example open loop Bode analysis and loaded Q calculations [3] permit assessment of frequency range, feasibility of meeting the oscillation criteria over the tuning range, and phase noise. Linear mapping techniques based on the bilinear transformation permit visualizing the interaction of the active device two port S-parameters and series feedback reactance and assist in establishing the load network. Equation writers within the simulation tools are an excellent aid in the design phase. For example the bilinear transform using the relation

$$\frac{1}{\Gamma_{in}} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (1)$$

permits linking the input reflection coefficient of the active device, Γ_{in} with series feedback [4, 5] and the load impedance in terms of Γ_L with the oscillator system loaded Q , Q_L . This is possible since both terms are a function of the open loop transmission gain and phase and are calculated from the oscillator open loop S-parameters and the relation

$$Q_L = -\frac{1}{2} \omega_0 \frac{\partial \phi}{\partial \omega}. \quad (2)$$

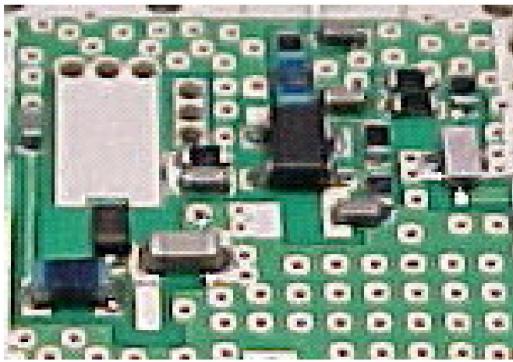


Fig. 1 Fabricated C-Band VCO on 20 mil thick Rogers 4350

All of these parameters are obtained from linear analysis, operating frequency, and network group delay ($\frac{\partial\varphi}{\partial\omega}$), part of reserved variables in simulation tools [6]. During the design phase the evaluation of loaded Q obtained from linear analysis is collaborated with the non-linear analysis of oscillator phase noise. As an example, this technique served as an invaluable tool in assessing the desired impedance transformation between the resonator and the active device. A tapped transmission line with an adjustable length (see Fig. 1) and tapping position is refined in EM simulation. The correlation between loaded Q and phase noise is evident during this development. Before the design phase and simulation it is imperative to gauge the accuracy of the models representing the critical elements in the circuit. The active device and resonator, specifically the varactor and the non-linear device model including package parasitics of the transistor should be validated. Early in the development phase it was found that measured device small signal S-parameters and S-parameters obtained from non-linear simulation at identical bias conditions showed poor correlation.

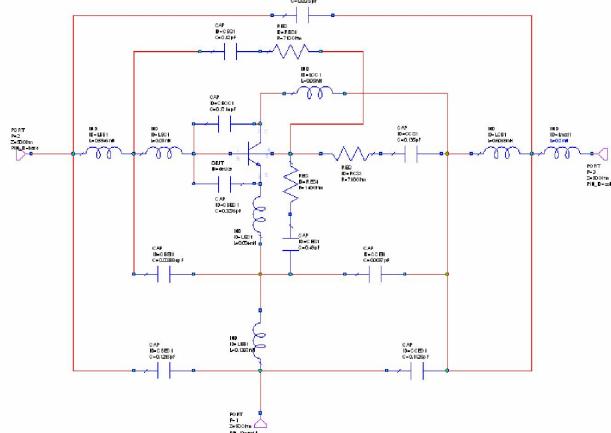


Fig. 2 Small-signal transistor model including parasitic package elements

The Gummel-Poon model provided for a SiGe HBT device permitted reasonable correlation only over a narrow range of bias voltages. A new device selection was required. A straight forward check of linear against non-linear derived S-parameter data over frequency and proper data agreement was achieved only after package parasitics were refined, see Fig. 2. The

match in active device linear data and data obtained from non linear simulation was further verified over a wide range of bias voltages. Similar attention must be directed to the varactor, in particular the package model and the supporting printed circuit board (PCB) pads, crucial in establishing agreement with measurement.

PCB pads supporting components and the location of reference planes marking the location of the component models must be addressed with care. This issue is discussed in the following section in more detail. Where ever possible, passive elements were placed into the simulator using Spice equivalent models as opposed to S-parameter tables. Although the models were created based on measured S-parameter data de-embedded from the measurement test set, it is convenient, particularly when frequency extrapolation is required to describe the passive elements in lumped form. As an example, the output filter network uses parameter table entry but was not de- embedded from the test set. Furthermore the pad shapes were not identical to the test set. Nevertheless good agreement with simulated data including details in amplitude rejection around the 2nd harmonic was observed. However there is discrepancy in the frequency response between measured and simulated data beyond 13 GHz. The VCO schematic is shown in Fig. 3 and the corresponding board layout is shown in Fig. 4. The iterative design flow associated with these techniques is shown in Fig. 5.

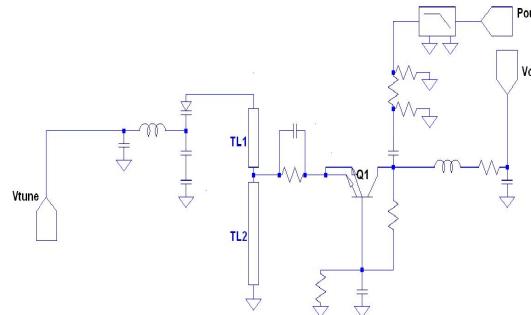


Fig. 3 VCO circuit diagram.

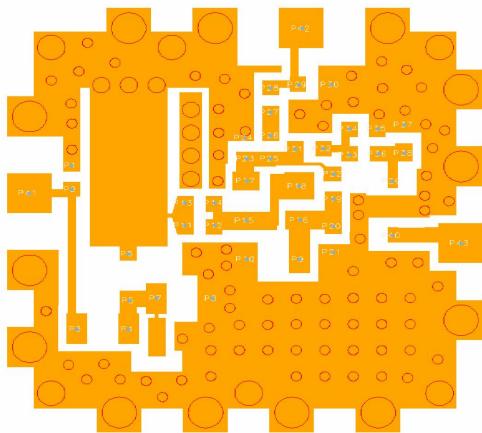


Fig. 4 VCO layout for planar EM simulation

III. EM-HARMONIC BALANCE CO-SIMULATION

The VCO board layout was imported in Momentum, a planar EM simulation tool in ADS [7]. The layout file was exported from the CAD layout tool in DXF file format. Internal ports were attached the pads, see Fig. 4. EM-simulation was performed from 50 MHz to 18 GHz. The frequency range was chosen so that the lower frequency range allows convergence of the DC solution when the harmonic balance engine is run. The higher end of the frequency end is chosen so that all harmonic frequencies of interest (up to 5th harmonic) are covered.

The simulation time on a dual-core Intel Xeon Machine with 4 GB of RAM is approximately 20 hours. The simulation time could be significantly reduced to less than 6 hours if the RF mode was enabled in Momentum. The difference between the tune curve characteristic result obtained using the Microwave and the RF mode in Momentum for similar artwork as Fig. 4 was less than 22 MHz at 5.3 GHz or 0.5 %.

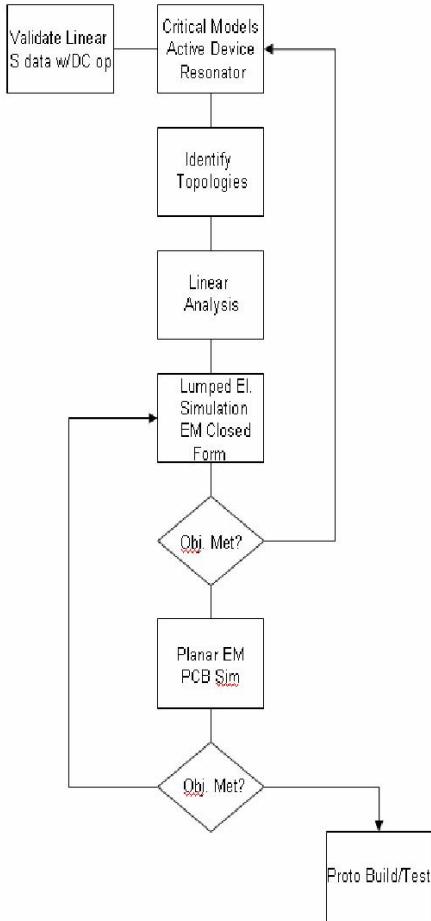


Fig. 5 Flowchart showing EM-Harmonic balance co-simulation design technique for VCO design.

The reference plane location must be carefully chosen in the planar EM simulation tool since it directly affects the parasitic element values. The worst case situation with largest

parasitic is represented by insetting the reference plane location from the edge of the pad by a length equal to that of the component termination pads. If the ports are located on the edge of the pad it represents the best case situation. For this work the reference plane was chosen in the middle of the pad. Ports were also attached at various tapping location on the transmission line in the resonator network. The 46 port S-parameter data was then exported from Momentum in touchstone format and subsequently imported into Microwave Office. Harmonic balance simulation was performed in Microwave Office [6] to evaluate the design and the effect of parasitics, see Fig. 6. This process was repeated until all performance objectives were met, see Fig. 5

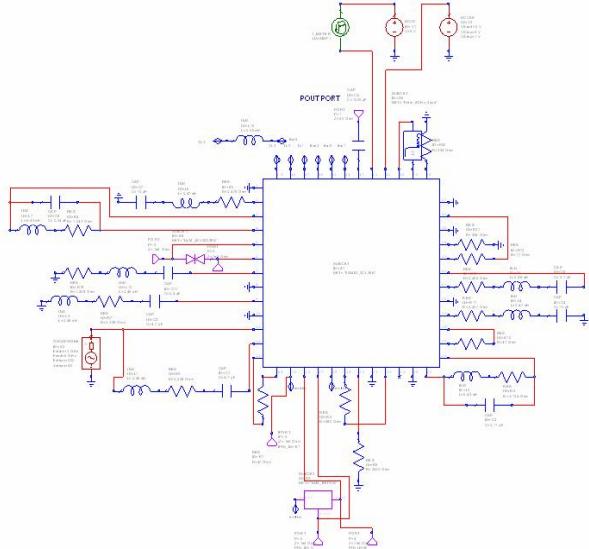


Fig. 6 EM-Harmonic balance co-simulation in Microwave Office

IV. MEASUREMENTS AND RESULTS

The VCO was measured using a board insert text fixture and Rhode & Schwarz Signal Analyzer FSUP26 [8]. Tuning data is shown in Fig. 7, and Fig. 8. The VCO tunes from 4.3 GHz to 5.4 GHz with 9 V tuning voltage. Agreement in tune frequency between simulation and measurement was better than 100 MHz representing less than 2 % error.

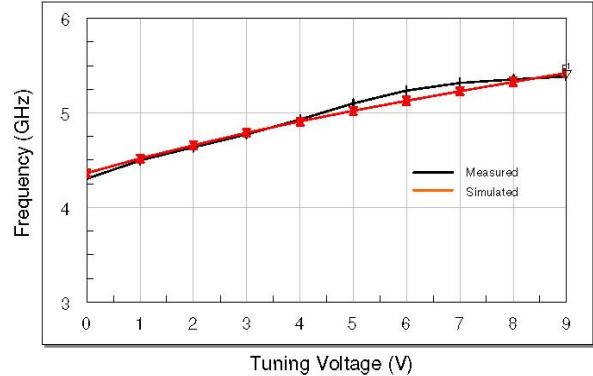


Fig. 7 Comparison of measured and simulated VCO tuning characteristics

Measured VCO phase noise was better than -90 dBc at 10 kHz offset and better than -110 dBc at 100 kHz offset, see Fig. 9.

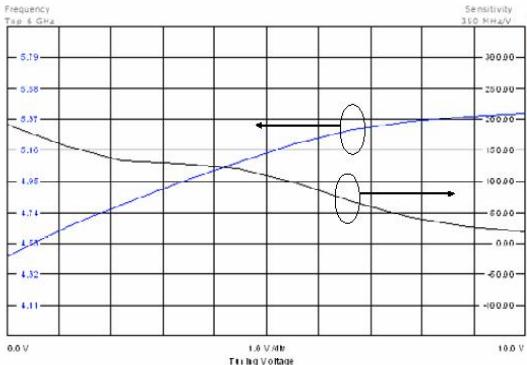


Fig. 8 Measured tuning curve and sensitivity of the VCO

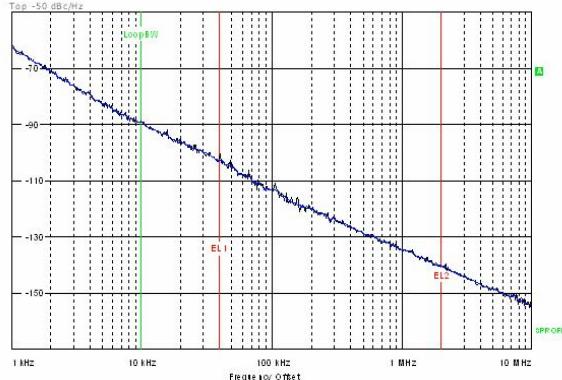


Fig. 9 Measured phase noise plot of the VCO

The power output slope with frequency agrees within 1 dB to that obtained from simulation. The measured output power was within 3 dB of simulation after correcting for test set cable loss of 1dB. Harmonic levels also demonstrate correlation within 2 dB including a notch in the 2nd harmonic response, see Figs. 10, and 11. In addition the 3rd harmonic tracks within a few dB of measured results at tune voltages up to 5 volts. Agreement at higher tune voltages is not as good, with measurements better than 10 dB lower than simulated.

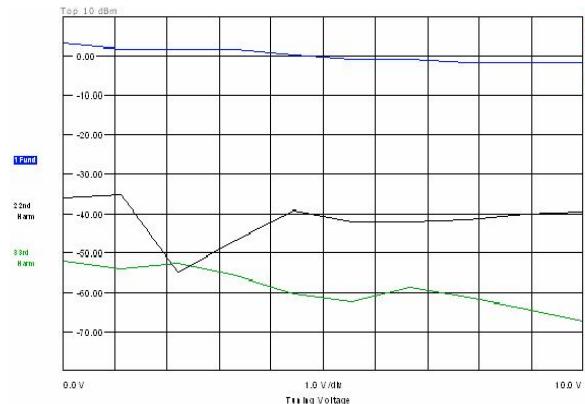


Fig. 10 Measured fundamental, 2nd and 3rd harmonic performance of the VCO

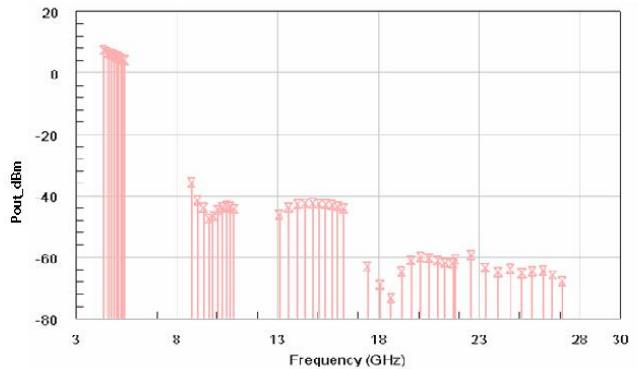


Fig. 11 Simulated power spectrum of the VCO

V. CONCLUSION

An EM-Harmonic balance co-design methodology is presented which permits accurate design of high frequency tunable oscillators. The approach leverages the accuracy of EM simulation with non-linear harmonic balance. Application of closed form EM simulation and lumped element models allows rapid assessment of the critical portions of the design and assists in CAD layout. Subsequent planar EM simulation closes the critical gap in CAD layout and assists in delivery of a design with no critical trims. Using the process outlined in this work functional oscillator with tune bandwidths in excess of 20% with no adjustments or trimming were designed with first pass success. The measured tuning characteristics of the C-band microstrip oscillator demonstrated correlation with simulated data with less than 2% error.

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Phase Noise in Oscillators

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As well known from oscillator theory, two conditions are required to make a feedback system oscillate: the open loop gain must be greater than unity; and total phase shift must be 360° at the frequency of oscillation.

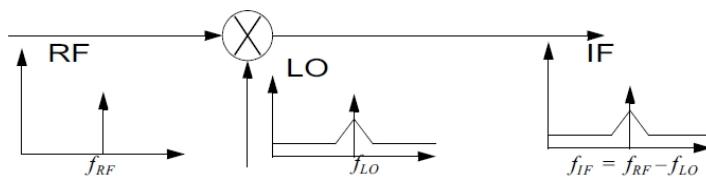
An oscillator circuit can be a combination of an amplifier with gain $A(j\omega)$ and a frequency dependent feedback loop $H(j\omega) = \beta A$.

Oscillator has positive feedback loop at selected frequency.

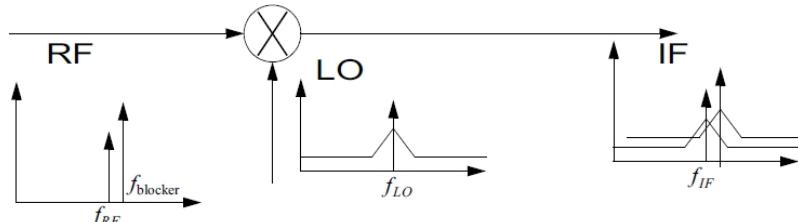
- Frequency Stability is a measure of the degree to which an oscillator maintains the same value of frequency over a given time.
- Phase Noise can be described as short-term random frequency fluctuations of a signal; is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1 Hz bandwidth at a given offset from the desired signal.
- Phase Noise is a measurement of uncertainty in phase of a signal. It is measured as the ratio of noise power in quadrature (90° out of phase) with the carrier signal to the power of carrier signal. This is opposed to AM noise which is noise in phase with the carrier signal.
- Two measurements of Phase Noise are common: the Spectral Density (SD) of phase fluctuations, and the Single Side Band (SSB) Phase Noise.
Spectral Density is twice of SSB, since this is related to total phase change, which includes both sidebands, when SSB Phase Noise corresponds to the relative level on one sideband.

The Phase Noise of a signal can only be measured by a system that has equal or better noise performance.

- Low oscillator Phase Noise is a necessity for many receiving and transmitting systems. Adjacent Channel Rejection as well as transmitter signal purity are dependent on the Phase Noise of the receiver local oscillator or transmit local oscillator.
- The local oscillator Phase Noise will limit the ultimate Signal-to-Noise ratio (SNR) which can be achieved when listening to a frequency modulated (FM) or phase-modulated (PM) signal.
- In a heterodyne system, mixing a clean low-phase-noise RF signal, with a poor phase noise (noisy) local oscillator, it will turn into a noisy IF.



- The oscillator Phase Noise is transferred to the carrier to which the receiver is tuned and is then demodulated. The Phase Noise results in a constant noise power output from the demodulator.
- Reciprocal mixing is especially important in the presence of strong nearby interferers. The skirt from the down-converted interferer raises the noise floor for the down-converted signal well above Thermal Noise kT_B .
- In a receiver, if a blocking interferer signal is much bigger than the desired signal, than the reciprocal Phase Noise due to the blocker self noise would dominate the noise at IF.

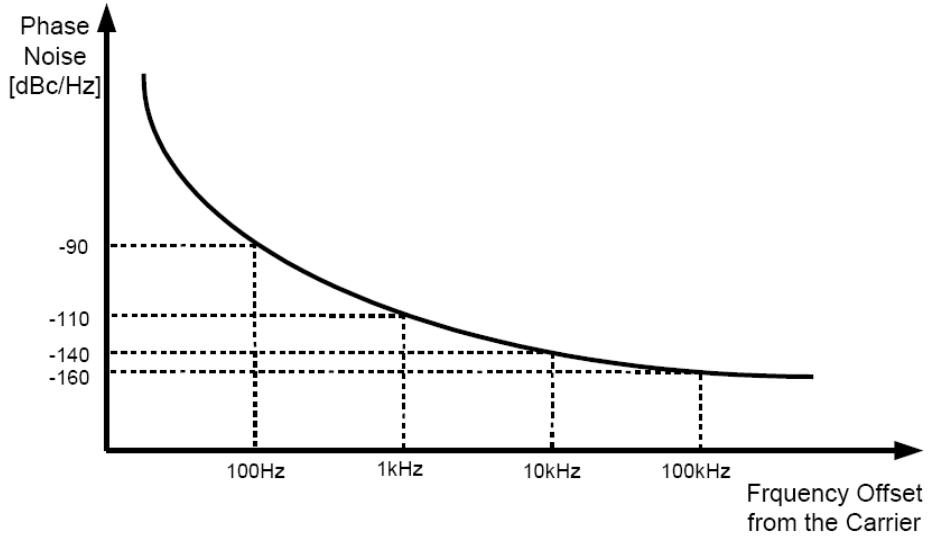


- The performance of some types of AM detectors or SSB detectors may be degraded by the local oscillator Phase Noise. Reciprocal mixing may cause the receiver noise floor to increase when strong signals are near the receiver's tuned frequency; this limits the ability to recover weak signals.
- Local oscillator Phase Noise will affect the Bit Error Rate (BER) performance of a Phase-Shift Keyed (PSK) digital transmission system. A transmission error will occur any time if the local oscillator phase, due to its noise, becomes sufficiently large that the digital phase detection makes an incorrect decision as to the transmission phase. For instance, a QPSK transmission system (used in Microwave Links, CDMA, DVB, etc) will make a transmission error if the instantaneous oscillator phase is offset by more than 45° since the phase detector will determine that baud to be in the incorrect quadrant. Digital transmission systems with smaller phase multiples are more sensitive to degradation due to local oscillator Phase Noise.
- Jitter is another factor that characterizes the oscillator signal and represents a fluctuation in the timing of the signal and arises due to the Phase Noise. Due to Jitter, the zero-crossing time of a periodic signal will vary slightly from the ideal location since the signal is not strictly periodic due to noise.

All of these effects are due to local oscillator Phase Noise, and can only be reduced by careful design decreasing the Phase Noise.

The Phase Noise of an oscillator is best described in the frequency domain where the spectral density is characterized by measuring the noise sidebands on either side of the output signal center frequency.

- Single Side Band (SSB) Phase Noise is specified in dBc/Hz at a given frequency offset from the carrier.



SSB Phase Noise places limit on receiver Adjacent Channel Selectivity (ACS) and also affects the receiver Signal to Noise Ratio.

A model for oscillator SSB Phase Noise was introduced by [David B. Leeson](#) in 1966.

$$\mathcal{L}_{PM} \approx 10 \log \left[\frac{FkT}{A} \frac{1}{8Q_L^2} \left(\frac{f_0}{f_m} \right)^2 \right] \quad \text{where:}$$

\mathcal{L}_{PM} = Single Side Band (SSB) Phase Noise density [dBc/Hz]

A = Oscillator output power [W]

F = device Noise Factor at operating power level A (linear)

k = Boltzmann's constant, 1.38×10^{-23} [J/K]

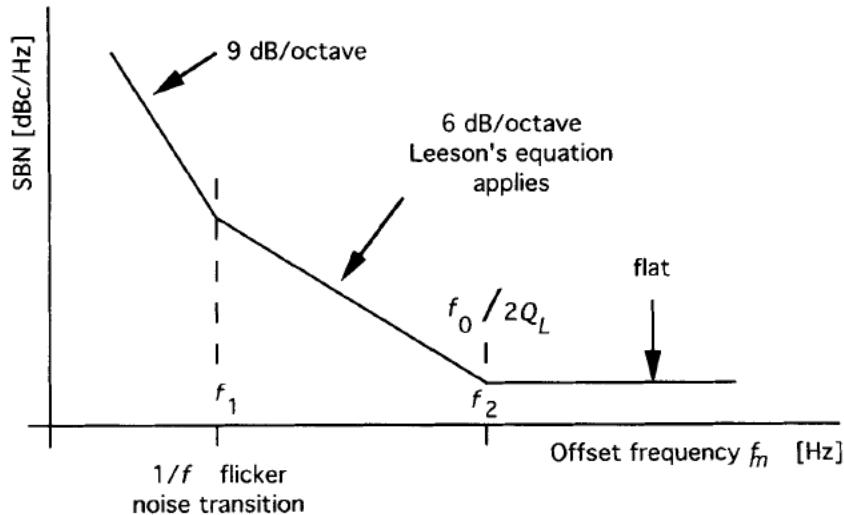
T = Temperature [K]

Q_L = Loaded-Q [dimensionless]

f_0 = Oscillator carrier frequency [Hz]

f_m = Frequency offset from the carrier [Hz]

Leeson equation only applies between $1/f$ flicker noise transition frequency (f_1) and a frequency (f_2) where white noise (flat) dominates.



Leeson equation provides several insights about oscillator SSB Phase noise:

- Doubling the Loaded-Q improves Phase Noise by 6dB.
- Doubling the operation frequency results 6dB Phase Noise degradation.

Unloaded-Q means the resonant circuit is not loaded by any external terminating impedance. In this case the Q is determined only by resonator losses.

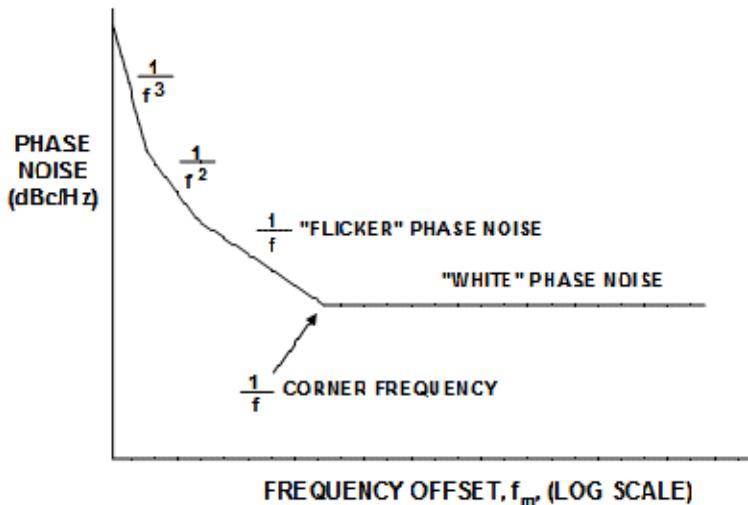
Loaded-Q represents the width of the resonance curve, or phase slope, including the effects of external components. In this case the Q is determined mostly by the external components.

- It is a common design mistake to achieve high Loaded-Q values by using a very loosely coupled resonator. The under-coupling results in increased overall resonator loss requiring an extra amount of gain to compensate it, which in turn, results in thermal noise increase.
- Resonator loss is a function of its unloaded and loaded Q-factors and is given by:

$$L(\text{dB}) = 10 \log \left(\frac{1}{1 - \frac{Q_L}{Q_U}} \right)^2$$

For example, in a simple feedback oscillator, the minimum Phase Noise is achieved when the resonator Loaded-Q is set to one half of its Unloaded value ($Q_L = 0.5 * Q_U$) that corresponds to a 6 dB resonator loss.

Other oscillator schemes may require different optimum coupling values due to different design goals and trade-offs.



- In the figure above Phase Noise in dBc/Hz is plotted as a function of frequency offset (f_m), with the frequency axis on a log scale. Note that the actual curve is approximated by a number of regions, each having a slope of $1/f^x$, where $x = 0$ corresponds to the "white" phase noise region (slope = 0 dB/decade), and $x = 1$ corresponds to the "flicker 1/f" phase noise region (slope = 20 dB/decade). There are also regions where $x = 2, 3, 4$, and these regions occur progressively closer to the carrier frequency.

- Leeson equation assumed that the $1/f^3$ and $1/f^2$ corner occurred precisely at the $1/f$ corner of the device. In measurements, this is not always the case.
- The Phase Noise of an oscillator depends by the noise of the open-loop amplifier and by the half-bandwidth of the resonator. If the amplifier has no $1/f$ noise region, the oscillator will have $1/f^2$ noise below the half-bandwidth. Unfortunately, all the active devices have some sort $1/f$ region.
- If the $1/f$ “flicker” corner frequency is low, the oscillator will have $1/f^2$ noise slope until that corner frequency is reached. This is the case with many LC oscillators.
- The $1/f$ region might be due to either active device or resonator. In many cases the noise of the resonator dominates, especially in the case of crystals or SAW devices. In this situation, the crystal should be presented with impedance that doesn't degrade the Q, or else the Phase Noise will also be degraded.

Oscillator harmonics can be filtered out by a simple Low Pass Filter, when the spurious close to the carrier can only be minimized by careful oscillator design.

Rules for designing a low Phase Noise oscillator:

- Maximize the resonator Loaded-Q. To do this (but trading with gain), in the series resonant circuits use a large Inductor, and in parallel circuits use a large Capacitor. Coupling the resonator tightly to the oscillating device, and minimize the coupling of the load to the circuit.
- A 10dB increase in Loaded-Q results in a 20dB improvement in Phase Noise.
- Build the resonator using high-Q components, having constant and quiet noise.
- Low losses are required in all of the constituent parts of the circuit including PCB. To be carefully considered the series resistance of the reactive components. Coupled losses in the rest of the circuit should be at most equal to the resonator losses. To get best Phase Noise, the resonator losses should be x3 the circuit losses.
- Use an active device with low noise figure at low frequencies.
- Use an active device with low $1/f$ flicker noise, with good bias circuit. The DC current set to get the best $1/f$ flicker noise should be the oscillator device current.
- There is effectively a trade-off between Gain and Phase Noise performance in microwave transistors, both for the additive or multiplicative noises.
- Maximize the output Signal Power vs Noise Power of the oscillator. However, the output power increase should be implemented very carefully, since severe Phase Noise degradation can occur because of the active device noise elevation at compression.
- Extract the output signal through the resonator to the load, thereby using the resonator transmission response selectivity to filter the carrier noise spectrum.
- Optimize (and do trade-offs) in noise reduction where is needed, especially consider close-in noise vs large offset noise requirements.
- Power Supply (V_{CC}) and tuning voltage (V_{tune}) returns must be connected to the printed circuit board ground plane. VCO ground plane must be the same as that of

the printed circuit board and therefore all VCO ground pins must be soldered direct to the printed circuit board ground plane.

- Adequate RF grounding is required. Several chip decoupling capacitors must be provided between the V_{CC} supply and ground.
- Good, low noise power supplies must be used to prevent AM noise. Ideally, DC batteries for both supply (V_{CC}) and tuning (V_{tune}) voltages will provide the best overall performance.
- The biasing circuit of the active device should be properly regulated and filtered to avoid any unwanted signal modulation or noise injection. Variations on the supply voltages or currents may also cause undesirable output power fluctuations and frequency drift.
- The active device should work in Class-A, to minimize the limitations in the stage that drives the resonator.
- Carefully control the limiting amplitude mechanism, so as not introduce AM noise. A signal limiter can be placed either before or after the active device, keeping its output well below the compression level.
- AM-PM conversion is minimized by choosing a 90° crossing angle between the device line and the load line.
- Phase perturbation can be minimized by using high impedance devices such as FETs, where the Signal-to-Noise ratio of the signal voltage relative to the equivalent noise voltage can be made very high.
- Output must be correctly terminated with good load impedance. It is also a good practice to use a resistive pad between the VCO and the external load.
- Connections to the tuning port must be as short as possible and must be well screened, shielded, and decoupled to prevent the VCO from being modulated by external noise sources. A low noise power supply must be used for tuning voltage.
- Minimize *Frequency Pushing* by the Gate or Base voltage of the transistor. Frequency Pushing is a shift in the oscillation frequency usually caused by a change in the transistor bias voltage.
- Avoid saturation of the active devices at all cost, and try to have either limiting or automatic gain control (AGC) without degradation of the Q of the resonator. Saturation of the active device can also lower the loaded-Q since the device losses will then add to those of the resonator.
- Use active components with low 1/f-noise. Flicker noise in active devices is also known as 1/f noise because of the 1/f slope characteristics of the noise spectrum (the amplitude varies inversely with frequency). Mainly traps associated with contamination and crystal defects in the emitter-base depletion layer cause this noise (in BJTs case). These traps capture and release carriers in a random fashion. The time constant associated with the process produce a noise signal at low frequencies.
- Transistors made in different processes have different 1/f noise corners. JFETs are the best (~1kHz), followed by BJTs (~5kHz), than CMOS (~1MHz), and GaAs are the worst (~10MHz).
- Consider using noise reduction via feedback, or feed-forward noise reduction techniques.

Rules for designing a low Phase Noise Voltage Controlled Oscillator (VCO):

In a Phase-Locked Loop (PLL) a Voltage Controlled Oscillator (VCO) will always have some spurious signals present on its output.

The amplitude and frequency of these spurious modulations may vary as the local oscillator is tuned.

- Poor layout of the phase-locked loop oscillator circuitry (VCO) may increase the amplitude and number of the output spurious signals.
- Oscillator Phase Noise has two components: Phase Noise resulting from direct upconversion of white noise and flicker noise ($1/f$ noise), and Phase Noise resulting from the changing phase of the noise sources modulating the oscillation frequency.
- In VCO design another source of Phase Noise increase are the non-linear capacitors (varactors) used in the LC resonator and its control lines.
- In a VCO, have to maintain the Q of the resonator by avoiding forward bias on the varactor tuning diodes, limiting the signal swing across the tuning diodes to prevent heating and thermal effects. This can be achieved by placing the varactor circuit in the gate or base if possible.
- The noise from the varactor diode resistance can also become the dominant noise source. For good Phase Noise, the carrier signal effectively appearing across the varactor noise resistance should be maximized to maintain good Signal-to-Noise ratio at this point. By transforming the noise load resistance seen by the oscillating device to a lower value in the matching circuit, the Power-to-Noise ratio across the varactor can be maximized, although at the expense of tuning bandwidth since the matching circuit will restrict the obtainable capacitance variation.
- There is a compromise in order to avoid breakdown, saturation, or overheating effects in the varactor. These will all reduce the Loaded-Q.
- When frequency of the carrier increases, it is more difficult to achieve good Phase Noise
- It's easy to achieve good Phase Noise when the frequency range covered by VCO is narrow; the tuning bandwidth must be small. Generated energy should be coupled from the resonator rather than from another portion of the active device so that the resonator limits the bandwidth.
- Increasing tuning sensitivity (measured in MHz / V) degrades Phase Noise.
- For a given frequency it's easy to achieve good Phase Noise in VCO's using a wide tuning voltage range.
- Temperature affects the Phase Noise. In a range of -55°C to $+85^{\circ}\text{C}$ the variation is ± 3 dB of the Phase Noise.
- Using of back-to-back varactor diodes in the tuning circuits has been found to eliminate effects of tuning circuit diode noise on oscillator signal spectral performance.

Characteristics of the ideal resonator for low Phase Noise oscillator:

- High Group Delay (high resonator Loaded-Q).
- High operating frequency.
- Low Loss.
- Moderate Drive Capability.
- Low frequency sensitivity to environmental stress (vibration, temperature, etc.).
- Good short-term and long-term frequency stability.
- Accurate frequency set-on capability.
- External frequency tuning capability.
- No undesired resonant modes or higher loss in undesired resonant modes or undesired resonant mode frequencies far from desired operating frequency.
- High manufacturing yield of acceptable devices.
- In-circuit resonator effective Q can be determined by intentionally altering the circuit phase shift by a known amount and measuring the resultant oscillator signal frequency shift.

Passive components in the oscillator circuit also exhibit short-term instability.

- Passive components (resistors, capacitors, inductors, reverse-biased, varactor diodes) exhibit varying levels of flicker-of-impedance instability whose effects can be comparable to or higher than that of the sustaining stage amplifier 1/f AM and PM noise in the oscillator circuit.
- The oscillator frequency control element (i.e., resonator) can exhibit dominant levels of flicker-of-resonant frequency instability, especially acoustic resonators.

Rules to select a transistor and its bias for designing a low Phase Noise oscillator:

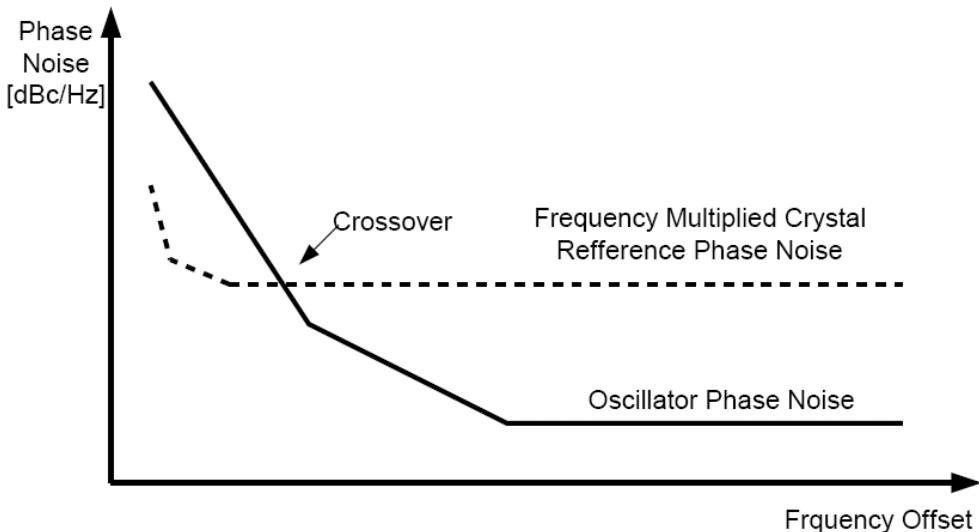
- The best oscillator transistor is a device with the lowest possible noise figure and lowest f_T . A commonly used criteria is: $f_T \leq 2 * f_{osc}$.
- Meantime, doing a trade-off, have to use a high frequency transistor having small junction capacitance and operate at moderately high bias voltage to reduce phase modulation due to junction capacitance noise modulation.
- Low 1/f noise of the transistor in the oscillator is very important, because the 1/f noise appears as sideband noise around the carrier frequency of the oscillator output signal.
- The 1/f noise is directly related to the current density in the transistor.
Transistors with high I_{Cmax} used at low currents have best 1/f performance.
For low Phase Noise operation use a medium power transistor. If you need your output power to be achieved at 6-9 mA, select a transistor with I_{Cmax} of 60-90 mA. However, the f_t of a transistor drops as current is decreased. Additionally, the parasitic capacitances of a high current transistor are higher due to the larger transistor structure required.

- In BJTs as V_{CE} increases, the flicker corner increases as the white noise increases, but the magnitude of the 1/f noise is constant. As base current increases, the flicker corner frequency increases with the magnitude of the 1/f noise and the increased shot noise current.
- The effect of flicker noise can be reduced through RF feedback. An unbypassed emitter resistor of 10-30 Ω in a BJT circuit can improve the flicker noise by as much as 40 dB. The proper bias point of the active device is important.
- In a well-designed near-class-A oscillator, the frequency is determined primarily by the resonator. As the loaded-Q is increased, the active device parasitic reactances become less significant in determining the oscillation frequency. Thus, changes in these parameters from device to device, with temperature and with supply voltage, have less effect. A simple test of how well the active device reactances are isolated from the resonator is to observe the operating frequency as the supply voltage is varied.
- Precautions should be taken to prevent modulation of the input and output dynamic capacitances of the transistor; which will cause amplitude-to-phase conversion and therefore introduce noise.
If phase shift in the transistor changes, the oscillation frequency will change until the loop phase shift returns to zero. Thus phase modulation in the amplifier causes frequency modulation of the oscillator.
- Device with low noise figure combined with a small correlation coefficient.
- Device with relative high output power.
- Device with low output conductance.
- Device with reasonably high input impedance.
- Meeting an impedance condition at the input of the active device, which can be achieved by optimization of the feedback factor and which leads to optimum impedance noise matching.
- Device with low multiplicative noise (1/f AM and especially 1/f PM).
- Device having drive capability consistent with resonator drive level and loss.
- Low noise in ALC/AGC circuits and/or in-compression amplifier operation.
- Low gain and phase sensitivity to DC supply and circuit temperature variations.
- Device with low Group Delay (wide bandwidth).
- Device with high load circuit isolation.
- Device with minimal number of adjustable and bias components.
- Ease of alignment and test.
- Device with good DC efficiency.

In a PLL the design of the loop filter can affect the Phase Noise of the system:

- Within the loop bandwidth, the Phase Noise of the oscillator will tend to cancel itself, leaving a Phase Noise essentially equal to the frequency multiplied Phase Noise of the crystal reference.
- Multiplied Phase Noise of the crystal reference at particular frequency offset is equal with reference Phase Noise at the same frequency offset plus $20 \cdot \text{LOG}(N_{\text{VCO_divider}})$ plus 1dB (multiplication efficiency factor).

- Outside the loop bandwidth, the Phase Noise of the oscillator is not canceled, and will continue to decrease, until reaching its half bandwidth, $\omega_0/2Q$ or 1/f corner frequency. Since the Q of the crystal reference is very large, its half bandwidth is very small, and its frequency multiplied Phase Noise will remain relatively flat down to very small frequency offsets. Further, at some moderate frequency offset, this multiplied phase noise power spectral-density will be crossed by the decreasing oscillator phase noise power spectral-density.
- The bandwidth of the loop should be chosen equal to the frequency offset of this crossover.
- The PLL loop bandwidth is not a barrier frequency with a discontinuity on either side of the barrier; it can be approximated as such with the proviso that small errors around the offset frequency equal to the loop bandwidth are accepted.



- The role of the loop filter, which is a low-pass filter inserted between the phase comparator and the VCO control voltage circuit, eliminates the high frequency component of the phase correction pulse generated by the phase comparator so that the only the DC component is provided to the VCO.
- As a rule of thumb, the cut off frequency of the low-pass filter is chosen as equal or less than comparison frequency divided by ten; $F_{\text{cutoff}} < (F_{\text{comparison}} / 10)$
- Usually the low-pass filter is an RC network. The analysis of the Phase Noise performance shows that the Phase Noise depends on the resistor value, part of the low-pass filter. The higher the resistor, the higher is its contribution to the Phase Noise.

Phase Noise in Crystal Oscillators

One of the most important characteristics of crystal oscillators, besides they can provide good frequency stability, is that they can exhibit very low Phase Noise.

In many oscillators, any spectral energy at the resonant frequency will be amplified by the oscillator, resulting in a collection of tones at different phases.

In a crystal oscillator, the crystal mostly vibrates in one axis, therefore only one phase is dominant.

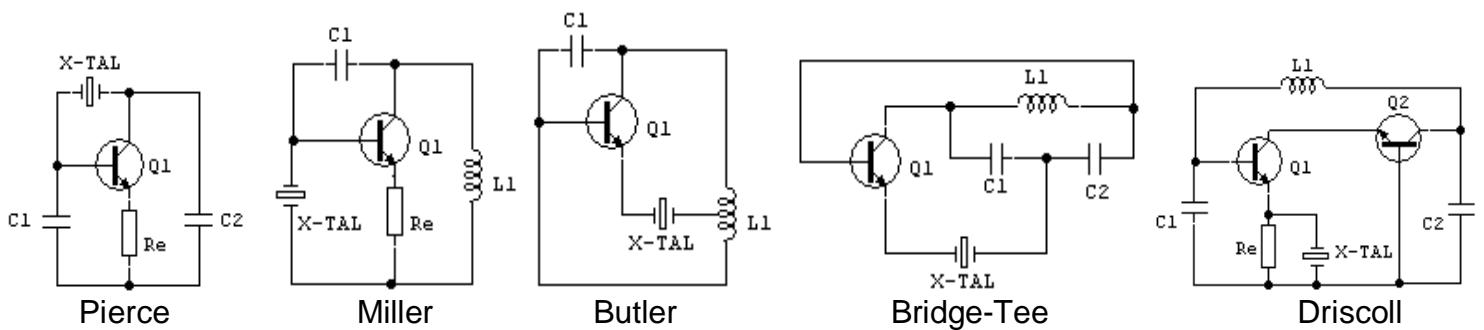
- At lower offset frequencies approaching the carrier, the Phase Noise is determined by the quality Q of the crystal resonator. For example a 100MHz crystal has a considerably lower Q than a 10MHz crystal, so the noise is higher at the low offsets.

The amplitude of **1/f flicker noise in crystal resonators** is a very important parameter of oscillators used in various applications.

- To get accurate models of the 1/f frequency noise in the resonator itself, this should be independent of the noise generated by the afferent electronic circuit.
- Was discovered that the amplitude of the 1/f frequency noise in a crystal depends not only on the Q of the resonator but also on the volume between the electrodes. Since the amplitude of 1/f noise depends on active crystal volume, to get low close-in Phase Noise we have to use the lowest overtone and lowest resonator frequency.
- Extra noise source is associated with electrode-crystal interface. A resonator having smaller electrodes would have lower 1/f flicker noise than other with the same resonant frequency and Q, but with larger diameter electrodes.
- The decrease in electrode area would increase the impedance and degrade the wideband noise, but for most resonators the wideband noise is dominated by the electronics of the oscillator.
The increase in series resistance decreasing the electrode diameter by a factor of 4 would be probably the limit from the standpoint of wideband noise.
This change might lead in a change of the oscillator loop gain.
- Thus for application specifically requires minimum close-in Phase Noise, lower frequency crystals may be used, when for low noise floor applications (wideband noise), the highest frequency crystal which satisfies long term stability requirements should generally be used.
- Also was discovered that 1/f frequency noise in a crystal is virtually independent of the loaded-Q of the resonator, when we know that in a practical oscillator circuit there is a dependence of the Phase Noise on loaded-Q, because the sustaining electronics contribute to the overall noise level.
- The crystal resonator plate can be cut from the source crystal in many different ways. The orientation of the crystal cut influences the crystal's frequency stability, Phase Noise characteristics, aging characteristics, thermal characteristics, and other parameters. A special cut (SC - Stress Compensated), is a double-rotated cut developed for oven stabilized oscillators with low Phase Noise, and good aging characteristics. This special cut SC is less sensitive to mechanical stresses, and has faster warm-up speed, higher Q, better close-in Phase Noise, less sensitivity to spatial orientation, and less sensitivity to vibrations.

Various topologies of crystal oscillators exhibit different performances mainly due to the limiting functions of the circuit, and of the loaded-Q of the crystal resonator.

In many instances decision of selection of particular type of crystal oscillator configuration is made on the basis of short-term frequency stability.



In most anti-resonant circuit configurations (such as Pierce and Miller configurations), the out-of-band impedances may become reactive due to the sharp reactance vs frequency characteristic exhibited by the crystal unit.

The series-mode circuits (as Butler and Bridge-Tee configurations) are more effective in reducing the wideband noise floor (up to 10dB compared to anti-resonant circuit).

The main disadvantage of series-mode circuits is the large degradation in crystal unit loaded-Q (due to limiting of the transistor). For example the effective value for crystal unit loaded-Q is about 120.000 for the Pierce circuit, and 24.000 for Bridge-Tee circuit.

- When limiting occurs, the transistor is turned *OFF* for a time portion of the signal waveform, time when the impedance seen by the crystal resonator at the transistor emitter contains a large value component at the signal frequency. This component of transistor impedance (which becomes increasingly large as the excess gain in the sustaining stage is increased) it will degrade the oscillator loaded-Q.
- In addition, the degradation in crystal loaded-Q can produce degradation in oscillator long-term frequency stability. This includes changes caused by environment (temperature, humidity) long-term power supply variation, and short-term effects (vibration and power supply ripple).
- Thus, better output noise spectrum could be obtained using a crystal oscillator in series-mode configuration, employing class-A non-limiting action in the sustaining stage transistor.
- The limiting function in a crystal oscillator may be controlled by:
 1. Auxiliary low-noise AGC circuits (a portion of the amplified RF signal is rectified and used to control the RF gain of the sustaining stage).
 2. Back-to-back Schottky diodes incorporated in the oscillator circuit, so that the diode RF impedance presented to the sustaining stage (and hence the RF gain) decreases with increasing the RF level.
 3. Incorporation of a second self-limiting transistor stage in the oscillator sustaining circuit, in a manner such that its effect on crystal unit loading is insignificant.

In 1972 M.M. Driscoll developed a very low Phase Noise series-mode crystal oscillator employing two transistors connected in cascode configuration.

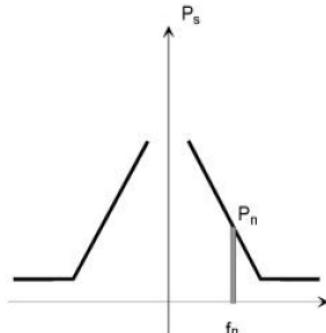
- The quartz crystal resonator is used as an un-bypassed emitter load on Q1.
- Unlike the common Butler or Bridged-Tee circuits, Q1 is *ON* during the full cycle of the signal waveform, since the limiting function is provided in Q2.
- Connecting the crystal between emitter of Q1 and ground increase the crystal loaded-Q. Reducing the emitter impedance by increasing the bias current of Q1 avoid over-dissipating power into the crystal.

Measuring the Oscillator Phase Noise

Generally the Spectral Density, or Phase Noise, of an oscillator is measured in dBc (dB below the carrier) in a bandwidth of 1Hz at an offset frequency f_n .

The Phase Noise, therefore, is related to the output power.

The Noise Power and the curve can have different shapes based on the noise sources.



$$\text{Phase Noise}_{[\text{dBc}/\text{Hz}]} = 10 * \text{LOG} (P_n / P_s)$$

P_n = Noise Power in 1Hz Bandwidth at particular frequency offset (f_n) in Watts

P_s = Carrier signal power in Watts

- A. The simplest and fastest method of determining the Phase Noise of an oscillator is the direct measurement using a Spectrum Analyzer.

For this measurement, the tested oscillator must fulfill the following conditions:

- The oscillator drift must be small relative to the Spectrum Analyzer sweep time since otherwise the oscillator frequency varies during the sweep, leading to distorted results. The synthesizers commonly used in radio communications fulfill this condition since they are locked to a stable reference.
- The Phase Noise of the local oscillators of the Spectrum Analyzer must be low enough to ensure that the characteristics of the tested oscillator and not those of the Spectrum Analyzer are determined.

Factors that limit the analyzer's ability to correctly measure the Phase Noise of a signal:

- IF (RBW) filter bandwidth, verses noise bandwidth.
- IF filter type and shape factor.
- Analyzer's local oscillator stability - residual FM.
- Analyzer's local oscillator stability - noise sidebands.
- Analyzer's detector response to noise - peak detector introduces errors.
- Analyzer's log amplifiers response to noise.
- Noise floor of the analyzer.

When measure the oscillator Phase Noise using a Spectrum Analyzer the following equation can be used for direct reading in dBc/Hz, for particular Resolution Bandwidth (RBW) set on the analyzer:

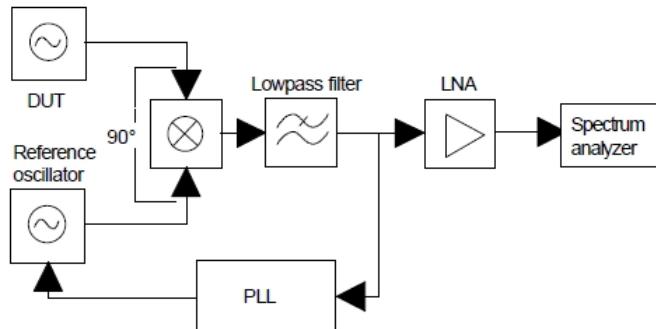
$$\text{Phase Noise}_{[\text{dBc}/\text{Hz}]} = \text{Carrier Power}_{[\text{dBm}]} - \text{Noise Power@Freq_offset}_{[\text{dBm}]} - 10 * \text{LOG} (\text{RBW}_{[\text{Hz}]})$$

Spectrum Analyzers generally only measure the scalar magnitude of noise sidebands of the signal and are not able to differentiate between amplitude noise and phase noise. In addition, the measurement process is complicated by having to make a noise measurement at each frequency offset of interest, sometimes a very time consuming task.

B. Another Phase Noise measurement can be done using a Reference Oscillator and a Phase Detector:

- The Phase Detector converts phase difference between its two inputs into a voltage. When the phase difference between the two inputs is 90° (quadrature) the Phase Detector output will be 0 volts.
- Any phase fluctuations around the quadrature point will result in a voltage fluctuation at the output of the Phase Detector.
- The Phase Detector output can then be digitized and processed to obtain the phase noise information desired.
- Additionally, the Phase Detector technique also enables residual/additive noise measurements for two-port devices.

Several methods have been developed based upon the phase detector concept. Among them, the Reference Source / PLL (Phase Locked Loop) is one of the most widely used methods.



Phase Noise measurement using a Reference Oscillator and a Phase Detector

- The reference oscillator is synchronized to the measured oscillator by means of a PLL of a very small bandwidth.
- The PLL sets the phases of the two oscillators to a difference of 90° .
- The Phase Noise of the DUT is eliminated within the loop bandwidth.
- The sum noise power of the reference and the test oscillator obtained outside the loop bandwidth is present at the output of the phase detector.
- This output signal is amplified by means of an LNA (Low Noise Amplifier) and displayed on a Spectrum Analyzer starting at a frequency of 0Hz.

This method offers the advantage of a very wide dynamic range, provided that the reference oscillator is of a very high spectral purity. Often, two identical oscillators are used for measurements on crystal oscillators, and the assumption made that the two

oscillators have the same Phase Noise. In this case, 3 dB is subtracted from the result because the noise powers add up.

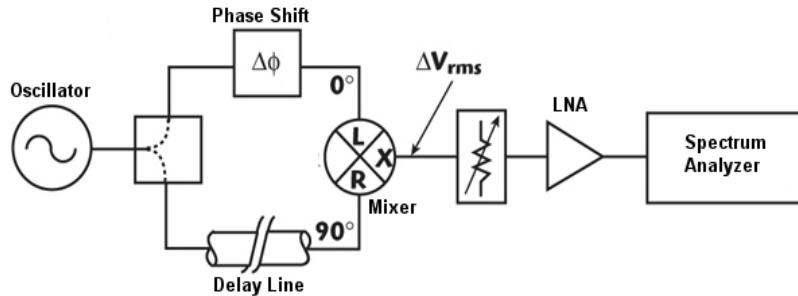
Also this method yields the widest measurement coverage (e.g. the frequency offset range is 0.01 Hz to 100 MHz).

This method is insensitive to AM noise and capable of tracking drifting sources.

The disadvantages of this method are:

- The method requires two oscillators at the same frequency that have to be synchronized to each other.
- An extra PLL and a Low Noise Amplifier are needed.
- Calibration is complex because the gain of all components is included in the result. Calibration is made by mistuning the two oscillators relative to each other and measuring the AC voltage obtained at the output of the LNA.
- Requiring a clean, electronically tunable reference source, and that measuring high drift rate sources requires reference with a wide tuning range.

C. The Frequency Discriminator method is another variation of the Phase Detector technique with the requirement of a reference source being eliminated.



- The signal from the tested oscillator is split into two channels.
- The signal in one path is delayed relative to the signal in the other path.
- The delay line converts the frequency fluctuations to phase fluctuations.
- Adjusting the delay line or the phase shifter will determine the phase quadrature of the two inputs to the mixer (phase detector). Then, the mixer (working as a phase detector) converts phase fluctuations to voltage fluctuations, which can then be read by the baseband Spectrum Analyzer as a frequency noise.
- The frequency noise is then converted as a phase noise reading.

The Frequency Discriminator method degrades the measurement sensitivity (at close-in offset frequencies) but is useful when the tested oscillator is a noisier source that has high-level, low-rate phase noise, or has high close-in spurious sidebands which can make problems for the phase detector PLL technique.

- A longer delay line will improve the sensitivity but the insertion loss of the delay line may exceed the source power available and cancel any further improvement.
- Longer delay lines limit the maximum offset frequency that can be measured.
- This method is best used for free-running sources such as LC oscillators or cavity oscillators.

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Graphical method for the Phase noise Optimization applied to a 6 -GHz fully integrated NMOS differential LC VCO

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Abstract— This paper describes the design and the optimization in terms of phase noise of a fully integrated NMOS Voltage Controlled Oscillator (VCO) using a 0.25 μm BICMOS SiGe process. A three-dimensional phase noise analysis diagram and a graphical optimization approach is presented to optimize the phase noise of the VCO while satisfying design constraints such as tank amplitude, power dissipation, tuning range and start up conditions. At 2.5 V power supply voltage, the optimized VCO features a simulated phase noise of -118 dBc/Hz at 1 MHz frequency offset from a 6.12 GHz carrier. The VCO is tuned from 6.1 GHz to 7.9 GHz with a tuning voltage varying from 0 to 2.5 V, and a power dissipation of only 7.4 mW.

Keywords: *phase noise, Optimization, graphical method, VCO, NMOS technology.*

I. INTRODUCTION

Voltage controlled oscillators are essential building blocks of modern RF transceivers architectures. The VCO performances in terms of tuning range, power dissipation and phase noise determine most of the basic performances of a complete transceiver.

Due to the evolution of wireless communication systems, the design of integrated oscillators implies many challenges to circuit designers as it involves multiple variables. To overcome these challenges and optimize the phase noise of the oscillator, an accurate graphical optimization method is presented in [1] by Hajimiri & al. The process of this optimization is performed through the minimization of phase noise while satisfying all different design constraints such as startup conditions, tank amplitude and tuning range. Nevertheless, in [1], the bias current of the VCO, which is an important parameter for the phase noise optimization, is chosen arbitrary to the maximum current allowed by the specifications. This choice does not constitute an optimal optimization strategy. Indeed, let us remind that a simplified and widely used phase noise model separates the amplitude

behavior versus the bias current into two operation modes named voltage and current-limited regimes [2]. Thus the phase noise decreases in the first regime until it reaches the stable transition point located between the two regimes. So, the desired bias current point for the optimum phase noise and power consumption performances is located at the intersection of these two regimes.

Due to this considerations, the aim of this work is first, to determine the optimum bias current of the VCO using a three dimensional phase noise representation using a parametric analysis and second, starting from this optimal current, to use the graphical optimization method proposed in [1] and adapted to our 6 GHz NMOS only LC VCO architecture.

This paper is organized as follow. In section II, the cross coupled LC-VCO architecture chosen as application example for the proposed method is described. The graphical optimization method is also presented in detail for the chosen LC VCO architecture. Section III presents the simulation results of the optimized VCO in order to show the accuracy of the presented method. Finally, we give some concluding remarks in section IV.

II. VCO TOPOLOGY AND OPTIMIZATION APPROACH

A. VCO topology

Figure 1 shows the simplified VCO schematic used and based on the well-known cross-coupled NMOS differential topology. The LC tank is made of a symmetric center-tapped inductor and a differentially tuned varactor. The cross connected NMOS differential pair provides the negative resistance to compensate for the tank losses. The tail current source is a simple NMOS current mirror. In these conditions, the width and the length of the NMOS tail transistor must be increased to reduce the flicker noise which lowers significantly the close-in phase noise of the VCO [3]. A tail

capacitor C_T is used to attenuate both the high-frequency noise component of the tail current and the voltage variations on the tail node. This latter effect results in more symmetric waveforms and smaller harmonic distortion in LC-VCO outputs [4], [5].

B. Optimization approach

For this LC VCO architecture, the adopted optimization methodology which is based on the following steps is detailed:

- Specifications definition ;
- VCO model determination ;
- Optimum Bias conditions determination ;
- Phase noise graphical optimization ;
- Phase noise estimation using the optimum parameter found in the previous step.

In the following sub sections, the process of modelization and optimization of the LC-VCO topology is analyzed step by step.

1) VCO model determination

The equivalent circuit model of the oscillator is shown in Figure 2, where the broken line in the middle represents either the common mode or ground.

The frequently appearing parameters in this model are the tank loss g_{tank} , effective negative conductance g_{active} , tank inductance L_{tank} and tank capacitance C_{tank} given by:

$$2g_{\text{tank}} = g_d + g_v + g_L \quad (1)$$

$$2g_{\text{active}} = g_m \quad (2)$$

$$L_{\text{tank}} = 2L \quad (3)$$

$$2C_{\text{tank}} = 4C_{gd} + C_{db} + C_{gs} + C_L + C_V \quad (4)$$

a) Inductor model

As explained in section II-A, the inductor used is a symmetric center-tapped inductor. The global inductance value is about 1.2 nH and the differential quality factor is equal to 19 at 6 GHz. Let us note here that we consider that the inductor has been designed in order to obtain a maximum Q factor at 6 GHz. Using the model in [1], the effective parallel equivalent conductance of the inductor, g_L , is given by:

$$g_L = \frac{1}{R_p} + \frac{R_s}{(\omega L)^2} \quad (5)$$

where R_p and R_s represents the parasitical elements of the inductance.

b) Varactor model

The varactor used is based on NMOS transistors in inversion mode. We modelize the varactor as an ideal capacitance in series with a resistor R_v . The varactor quality factor is equal to 200 at 6 GHz, and the effective parallel equivalent varactor conductance, g_v , is then given by:

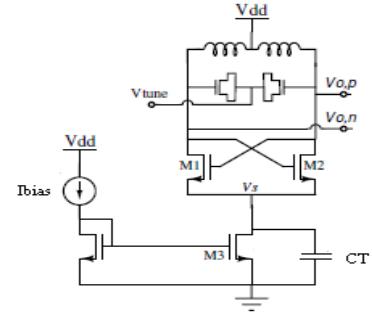


Figure 1. Conventional VCO schematic

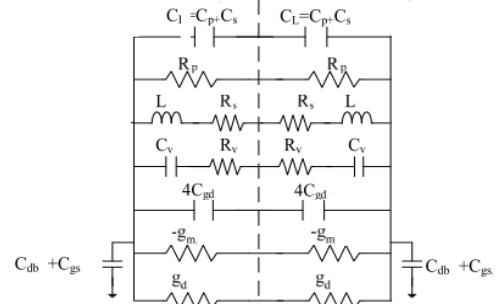


Figure 2. Equivalent oscillator model

$$g_v = \frac{1}{R_v} = \frac{C_v \omega}{Q_v} \quad (6)$$

Where R_v is the MOS varactor parasitic serie resistance and Q_v represent the quality factor of the varactor.

c) Transistor model

The very useful NMOS transistor analytical model described in [6] is used for the graphical optimization and visualization of design constraints.

2) Optimum Bias conditions determination

Let us remind that the aim of this part is to determine the optimum bias current of the VCO for a minimum phase noise. To do so, a program developed in Maple in which we exploit the following expression describing the phase noise model (pn) of the VCO is used [7].

$$Pn(f_{\text{offset}}) = \left[\frac{1}{16\pi^2 f_{\text{offset}}^2} \cdot \frac{L^2(2\pi f_0)^2}{V_{\text{tank}}^2} \right] [2kT(g_L + g_v + g_d)] \quad (7)$$

Where k is the Boltzmann constant, T is the temperature, V_{tank} is the oscillation amplitude, f_0 is the oscillation frequency, f_{offset} is the offset frequency from the carrier, γ is equal to 5/2 and g_d is the output conductance.

So, for each value of I_{bias} the tank voltage and the phase noise are calculated using equation 8. Figure 3 shows a three-dimensional representation of the LC-VCO phase noise. In this figure, the (x-y) plane describes the bias condition of the VCO and the z-axis corresponds to phase noise prediction. Thus, an initial optimal bias condition for which the phase noise is estimated to be at the minimum is selected. The

coordinate of this minimum for this 6-GHz VCO is given by: $I_{\text{bias}} = 3.4 \text{ mA}$ and $P_n(1 \text{ MHz}) = -116.71 \text{ dBc/Hz}$.

3) Phase noise graphical optimization

Using the previous model for the chosen LC VCO, the process of optimization consists in the representation of the design constraints in the variable plane; therefore let us, first of all, define the design variables.

a) Design variables

There are many initial design variables associated with the specified VCO: the geometric parameters of the on-chip spiral inductors, the MOS transistors dimensions (W_n and L_n) and the maximum and minimum values of the varactors ($C_{v,\max}$ and $C_{v,\min}$). The number of these design variables can be reduced as explained in the following: First, the geometric parameters of the inductors are fixed in order to obtain a high inductor quality factor as mentioned previously. Second, the channel length L_n is set to the minimum allowed by the process technology for maximum transition frequency (F_T) and transconductance g_m . Third, the ratio $C_{v,\max}/C_{v,\min}$ is maximum. Therefore, the varactor introduces only one design variable ($C_{v,\max}$).

Finally, we reduce the number to only two design variables, the transistors width W_n and the maximal varactor capacitance $C_{v,\max}$ which will be referred to C in the following. Consequently, the design constraints will be represented in the (W_n, C) plane.

a) Design constraints

The main goal of the optimization is to minimize the phase noise of the VCO while satisfying all design constraints such as tank amplitude, startup condition, power dissipation and tuning range.

In these conditions, and in order to ensure a large enough voltage swing, the tank amplitude is required to be larger than $V_{\text{tank},\min}$ so that:

$$V_{\text{tank}} = \frac{I_{\text{bias}}}{g_{\text{tank},\max}} \geq V_{\text{tank},\min} \quad (8)$$

Where $V_{\text{tank},\min}$ is chosen to be equal to 1 V and $g_{\text{tank},\max}$ is the maximum tank conductance.

Moreover, the startup condition is fixed by:

$$g_{\text{active}} \geq \sigma_{\min} g_{\text{tank},\max} \quad (9)$$

Where $\sigma_{\min} = 3$ is the small-signal loop gain, g_{active} and $g_{\text{tank},\max}$ are the active and the tank conductance respectively.

Finally, the oscillation tuning range is limited by two values depending on the center frequency ω_0 , so that:

$$L_{\text{tank}} C_{\text{tank},\min} \leq \frac{1}{\omega_{\max}^2} \quad (10)$$

$$L_{\text{tank}} C_{\text{tank},\max} \geq \frac{1}{\omega_{\min}^2} \quad (11)$$

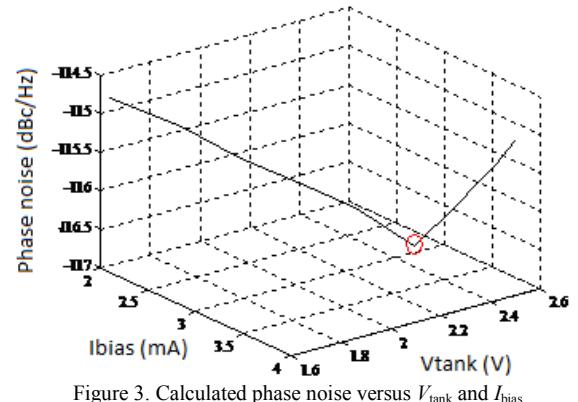


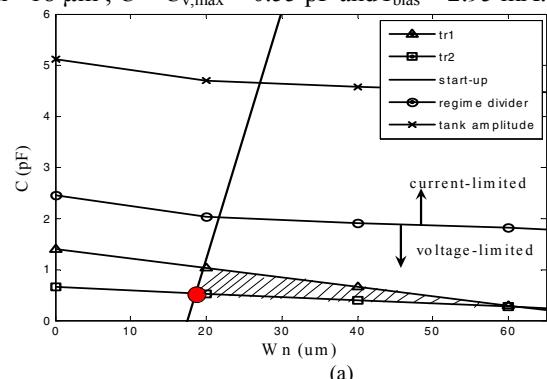
Figure 3. Calculated phase noise versus V_{tank} and I_{bias}

The design constraints given by (8) to (11) are expressed and formulated as functions of W_n and C variables, and a new program was developed in Maple which allows to calculate, for each value of the transistor width, the varactor capacitance C so that the design constraints are fulfilled. The associated curves are shown in figure 4, using the initial I_{bias} condition already determined.

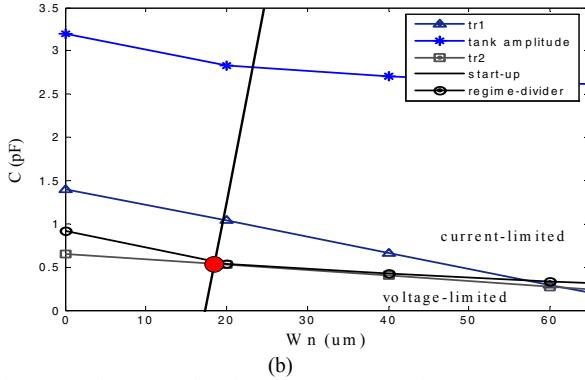
The line representing the limit of the tank amplitude is obtained using (8), the region below this line corresponds to V_{tank} greater than 1 V. The tr_1 and tr_2 lines define the maximum and minimum frequency of the tuning range, and are obtained respectively from (10) and (11). In this case, a tuning range of 25% with a center frequency of 6 GHz is obtained if a design point (a couple C, W_n) lies between the tr_1 line and the tr_2 line. The startup line is obtained from (9). Thus, to ensure proper startup of the VCO, the point must be located on the right-hand side of the startup line for $\sigma_{\min}= 3$. Finally the regime divider line presents the limit of the voltage-limited regime and the current-limited regime.

The region with shadow in figure 4(a) satisfies all the design constraints and represents a set of feasible design points. The optimum point is defined by the intersection of the startup line and tr_2 line since this point corresponds to the low parasitic capacitances values. However we can notice that the optimum point is located in the voltage limited regime (below the regime divider). Therefore, the design suffers from waste of power. As a consequence, the bias current must be reduced until the optimum is located on the regime divider line. In this case, figure 4(b) shows the optimum design with $I_{\text{bias}}=2.95 \text{ mA}$ for which no further action is necessary.

Consequently, the obtained optimum point is defined by: $W_n = 18 \mu\text{m}$; $C = C_{v,\max} = 0.55 \text{ pF}$ and $I_{\text{bias}} = 2.95 \text{ mA}$.



(a)

Figure 4. Design constraints for: (a) $I_{\text{bias}} = 3.4 \text{ mA}$; (b) $I_{\text{bias}} = 2.95 \text{ mA}$

III. SIMULATION RESULTS

In this section, simulations using spectre RF Software is performed on the VCO designed using the presented optimization process.

At the beginning, one must verify that the I_{bias} point found through the optimization method is effectively the optimum current for minimum phase noise. To do so, the phase noise at 1 MHz frequency offset versus the bias current is plotted. The curve in figure 5 shows that the phase noise decreases in the first regime and it reaches the stable transition point located between the voltage and current limited regimes. This transition point is defined by a current whose value is located between 2.9 mA and 3.1 mA.

Furthermore, as shown in figure 6, the VCO can be tuned from 6.1 GHz to 7.9 GHz, and shows a phase noise of -118 dBc/Hz at 1 MHz frequency offset from a 6.12 GHz carrier, and a current consumption of 2.95 mA from a 2.5 V power supply.

In order to show the accuracy of the presented graphical optimization method, table I presents a comparison between theoretical (presented method) and simulation (Spectre RF software) results. Let us note that, the phase noise value is calculated using (7) after optimization. As we can see, a good agreement can be found between theoretical and simulated results.

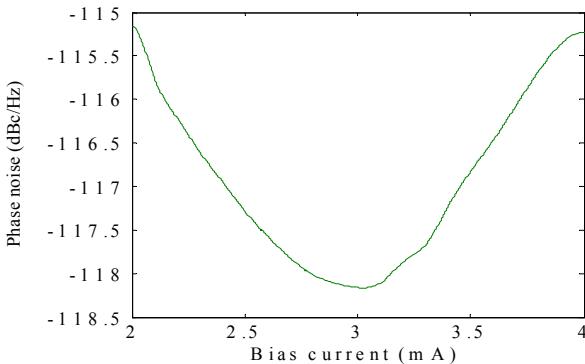


Figure 5. Phase noise versus the bias current.

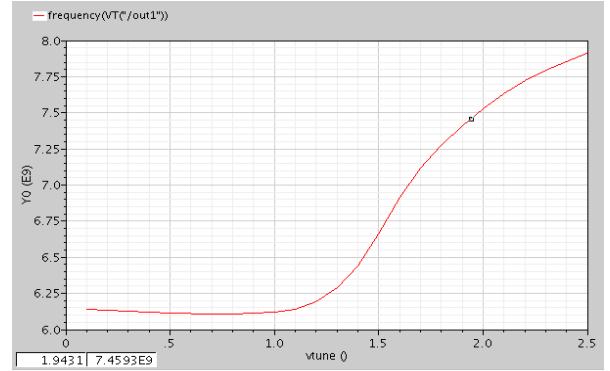


Figure 6. Tuning characteristic of the LC-NMOS VCO

TABLE I: COMPARISON BETWEEN THEORETICAL AND SIMULATION RESULTS

	Graphical Optimization	Spectre RF Software
Frequency (GHz)	6	6.12
Tuning range (%)	25	25.9
Phase noise(dBc/Hz)	-118.44	-118

IV. CONCLUSION

This paper describes a graphical method for the phase noise optimization of LC voltage controlled oscillators. It is based on a three-dimensional phase noise analysis diagram to visualize the different design constraints such as tank amplitude, startup condition and tuning range. It is shown that the design process to minimize phase noise and to obtain optimum bias condition through this illustration and using graphical optimization presents simulated accurate and systematic results. The optimized VCO achieves a phase noise of -118 dBc/Hz at 1 MHz frequency offset for a 6.12 GHz carrier frequency.

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Theory of Oscillators

1.1 Introduction

There are many types of oscillators, and many different circuit configurations that produce oscillations. Some oscillators produce sinusoidal signals, others produce nonsinusoidal signals. Nonsinusoidal oscillators, such as pulse and ramp (or sawtooth) oscillators, find use in timing and control applications. Pulse oscillators are commonly found in digital-systems clocks, and ramp oscillators are found in the horizontal sweep circuit of oscilloscopes and television sets. Sinusoidal oscillators are used in many applications, for example, in consumer electronic equipment (such as radios, TVs, and VCRs), in test equipment (such as network analyzers and signal generators), and in wireless systems.

In this chapter the feedback approach to oscillator design is discussed. The oscillator examples selected in this chapter, as well as the mix of theory and design information presented, help to clearly illustrate the feedback approach.

The basic components in a feedback oscillator are the amplifier, an amplitude-limiting component, a frequency-determining network, and a (positive) feedback network. Usually the amplifier also acts as the amplitude-limiting component, and the frequency-determining network usually performs the feedback function. The feedback circuit is required to return some of the output signal back to the input. Positive feedback occurs when the feedback signal is in phase with the input signal and, under the proper conditions, oscillation is possible.

One also finds in the literature the term negative-resistance oscillators. A negative-resistance oscillator design refers to a specific design approach that is different from the one normally used in feedback oscillators. Since feedback oscillators present an impedance that has a negative resistance at some point in the circuit, such oscillators can also be designed using a negative-resistance approach. For a good understanding of the negative resistance method, a certain familiarity with oscillators is needed. That is why the negative resistance method is discussed in Chapter 5.

1.2 Oscillation Conditions

A basic feedback oscillator is shown in Figure 1.1. The amplifier's voltage gain is $A_v(j\omega)$, and the voltage feedback network is described by the transfer function $\beta(j\omega)$. The amplifier gain $A_v(j\omega)$ is also called the open-loop gain since it is the

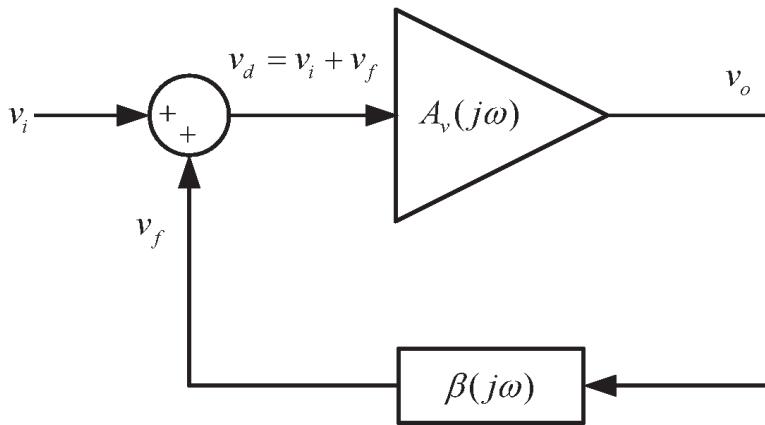


Figure 1.1 The basic feedback circuit.

gain between v_o and v_i when $v_f = 0$ (i.e., when the path through $\beta(j\omega)$ is properly disconnected).

The amplifier gain is, in general, a complex quantity. However, in many oscillators, at the frequency of oscillation, the amplifier is operating in its midband region where $A_v(j\omega)$ is a real constant. When $A_v(j\omega)$ is constant, it is denoted by A_{vo} .

Negative feedback occurs when the feedback signal subtracts from the input signal. On the other hand, if v_f adds to v_i , the feedback is positive. The summing network in Figure 1.1 shows the feedback signal added to v_i to suggest that the feedback is positive. Of course, the phase of v_f determines if v_f adds or subtracts to v_i . The phase of v_f is determined by the closed-loop circuit in Figure 1.1. If $A_v(j\omega) = A_{vo}$ and A_{vo} is a positive number, the phase shift through the amplifier is 0° , and for positive feedback the phase through $\beta(j\omega)$ should be 0° (or a multiple of 360°). If A_{vo} is a negative number, the phase shift through the amplifier is $\pm 180^\circ$ and the phase through $\beta(j\omega)$ for positive feedback should be $\pm 180^\circ \pm n360^\circ$. In other words, for positive feedback the total phase shift associated with the closed loop must be 0° or a multiple n of 360° .

From Figure 1.1 we can write

$$v_o = A_v(j\omega)v_d \quad (1.1)$$

$$v_f = \beta(j\omega)v_o \quad (1.2)$$

and

$$v_d = v_i + v_f \quad (1.3)$$

Thus, from (1.1) to (1.3), the closed-loop voltage gain $A_{vf}(j\omega)$ is given by

$$A_{vf}(j\omega) = \frac{v_o}{v_i} = \frac{A_v(j\omega)}{1 - \beta(j\omega)A_v(j\omega)} \quad (1.4)$$

The quantity $\beta(j\omega)A_v(j\omega)$ is known as the *loop gain*.

For oscillations to occur, an output signal must exist with no input signal applied. With $v_i = 0$ in (1.4) it follows that a finite v_o is possible only when the denominator is zero. That is, when

$$1 - \beta(j\omega)A_v(j\omega) = 0$$

or

$$\beta(j\omega)A_v(j\omega) = 1 \quad (1.5)$$

Equation (1.5) expresses the fact that for oscillations to occur the loop gain must be unity. This relation is known as the Barkhausen criterion.

With $A_v(j\omega) = A_{vo}$ and letting

$$\beta(j\omega) = \beta_r(\omega) + j\beta_i(\omega)$$

where $\beta_r(\omega)$ and $\beta_i(\omega)$ are the real and imaginary parts of $\beta(j\omega)$, we can express (1.5) in the form

$$\beta_r(\omega)A_{vo} + j\beta_i(\omega)A_{vo} = 1$$

Equating the real and imaginary parts on both sides of the equation gives

$$\beta_r(\omega)A_{vo} = 1 \Rightarrow A_{vo} = \frac{1}{\beta_r(\omega)} \quad (1.6)$$

and

$$\beta_i(\omega)A_{vo} = 0 \Rightarrow \beta_i(\omega) = 0 \quad (1.7)$$

since $A_{vo} \neq 0$. The conditions in (1.6) and (1.7) are known as the Barkhausen criteria in rectangular form for $A_v(j\omega) = A_{vo}$.

The condition (1.6) is known as the gain condition, and (1.7) as the frequency of oscillation condition. The frequency of oscillation condition predicts the frequency at which the phase shift around the closed loop is 0° or a multiple of 360° .

The relation (1.5) can also be expressed in polar form as

$$\beta(j\omega)A_v(j\omega) = |\beta(j\omega)A_v(j\omega)| \underline{\beta(j\omega)A_v(j\omega)} = 1$$

Hence, it follows that

$$|\beta(j\omega)A_v(j\omega)| = 1 \quad (1.8)$$

and

$$\underline{\beta(j\omega)A_v(j\omega)} = \pm n360^\circ \quad (1.9)$$

where $n = 0, 1, 2, \dots$. Equation (1.9) expresses the fact that the signal must travel through the closed loop with a phase shift of 0° or a multiple of 360° . For $A_v(j\omega) = A_{vo}$, then $|\beta(j\omega)A_{vo}|$ is the angle of $\beta(j\omega)$, and the condition (1.9) is equivalent to saying that $\beta_i(j\omega) = 0$, in agreement with (1.7). Also, for $A_v(j\omega) = A_{vo}$ and with $\beta_i(j\omega) = 0$, (1.8) reduces to (1.6). The conditions in (1.8) and (1.9) are known as the Barkhausen criteria in polar form.

When the amplifier is a current amplifier, the basic feedback network can be represented as shown in Figure 1.2. In this case, $A_i(j\omega)$ is the current gain of the amplifier, and the current feedback factor $\alpha(j\omega)$ is

$$\alpha(j\omega) = \frac{i_f}{i_o}$$

For this network, the condition for oscillation is given by

$$\alpha(j\omega)A_i(j\omega) = 1 \quad (1.10)$$

which expresses the fact that loop gain in Figure 1.2 must be unity.

The loop gain can be evaluated in different ways. One method that can be used in some oscillator configurations is to determine $A_v(j\omega)$ and $\beta(j\omega)$ and to form the loop gain $A_v(j\omega)\beta(j\omega)$. In many cases it is not easy to isolate $A_v(j\omega)$ and $\beta(j\omega)$ since they are interrelated. In such cases a method that can usually be implemented is to represent the oscillator circuit as a continuous and repetitive circuit. Hence, the loop gain is calculated as the gain from one part to the same part in the following circuit. An alternate analysis method is to replace the amplifier and feedback network in Figure 1.1 by their ac models and write the appropriate loop equations. The loop equations form a system of linear equations that can be solved for the closed-loop voltage gain, which can be expressed in the general form

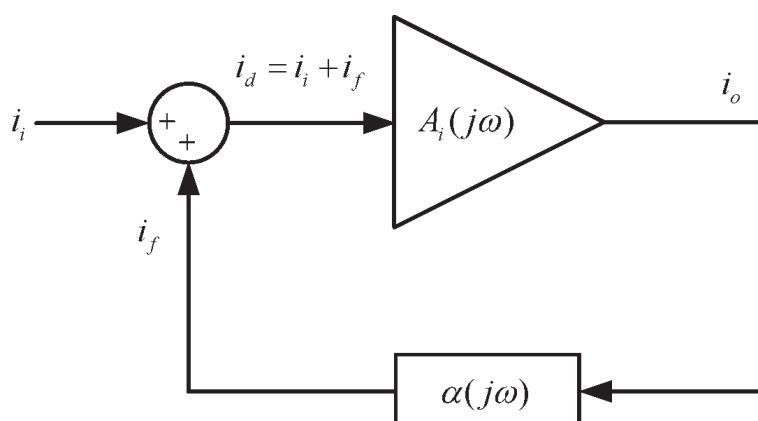


Figure 1.2 The current form of the basic feedback network.

$$A_{vf}(j\omega) = \frac{v_o}{v_i} = \frac{N(j\omega)}{D(j\omega)} \quad (1.11)$$

where $N(j\omega)$ represents the numerator polynomial and $D(j\omega)$ is the system determinant of the linear equations. In terms of (1.11) the conditions for oscillations are obtained by setting the system determinant equal to zero (i.e., $D(j\omega) = 0$). Setting $D(j\omega) = 0$ results in two equations: one for the real part of $D(j\omega)$ (which gives the gain condition), and one for the imaginary part of $D(j\omega)$ (which gives the frequency of oscillation).

From circuit theory we know that oscillation occurs when a network has a pair of complex conjugate poles on the imaginary axis. However, in electronic oscillators the poles are not exactly on the imaginary axis because of the nonlinear nature of the loop gain. There are different nonlinear effects that control the pole location in an oscillator. One nonlinear mechanism is due to the saturation characteristics of the amplifier. A saturation-limited sinusoidal oscillator works as follows. To start the oscillation, the closed-loop gain in (1.4) must have a pair of complex-conjugate poles in the right-half plane. Then, due to the noise voltage generated by thermal vibrations in the network (which can be represented by a superposition of input noise signals v_n) or by the transient generated when the dc power supply is turned on, a growing sinusoidal output voltage appears. The characteristics of the growing sinusoidal signal are determined by the complex-conjugate poles in the right-half plane. As the amplitude of the induced oscillation increases, the amplitude-limiting capabilities of the amplifier (i.e., a reduction in gain) produce a change in the location of the poles. The changes are such that the complex-conjugate poles move towards the imaginary axis. However, the amplitude of the oscillation was increasing and this makes the complex poles to continue the movement toward the left-half plane. Once the poles move to the left-half plane the amplitude of the oscillation begins to decrease, moving the poles toward the right-half plane. The process of the poles moving between the left-half plane and the right-half plane repeats, and some steady-state oscillation occurs with a fundamental frequency, as well as harmonics. This is a nonlinear process where the fundamental frequency of oscillation and the harmonics are determined by the location of the poles. Although the poles are not on the imaginary axis, the Barkhausen criterion in (1.5) predicts fairly well the fundamental frequency of oscillation. It can be considered as providing the fundamental frequency of the oscillator based on some sort of average location for the poles.

The movement of the complex conjugate poles between the right-half plane and the left-half plane is easily seen in an oscillator designed with an amplitude limiting circuit that controls the gain of the amplifier and, therefore, the motion of the poles. An example to illustrate this effect is given in Example 1.6.

The previous discussion shows that for oscillations to start the circuit must be unstable (i.e., the circuit must have a pair of complex-conjugate poles in the right-half plane). The condition (1.5) does not predict if the circuit is unstable. However, if the circuit begins to oscillate, the Barkhausen criterion in (1.5) can be used to predict the approximate fundamental frequency of oscillation and the gain condition. The stability of the oscillator closed-loop gain can be determined using the Nyquist stability test.

1.3 Nyquist Stability Test

There are several methods for testing the stability of a feedback amplifier. In general, (1.4) can be expressed in the form

$$A_{vf}(s) = \frac{v_o}{v_i} = \frac{A_v(s)}{1 - \beta(s)A_v(s)} \quad (1.12)$$

The stability $A_{vf}(s)$ is determined by the zeroes of $1 - \beta(s)A_v(s)$ provided there is no cancellation of right-half plane poles and zeroes when forming the product $\beta(s)A_v(s)$. In practical oscillators the previous pole-zero cancellation problems are unlikely to occur. If there are no pole-zero cancellation problems, the poles of $A_v(s)$ are common to those of $\beta(s)A_v(s)$ and of $1 - \beta(s)A_v(s)$. Therefore, the feedback amplifier is stable if the zeroes of $1 - \beta(s)A_v(s)$ lie in the left-half plane. In what follows we assume that there are no pole-zero cancellation problems.

The Nyquist stability test (or criterion) can be used to determine the right-half plane zeroes of $1 - \beta(s)A_v(s)$. A Nyquist plot is a polar plot of the loop gain $\beta(s)A_v(s)$ for $s = j\omega$ as the frequency ω varies from $-\infty < \omega < \infty$. Two typical Nyquist plots are shown in Figure 1.3. The Nyquist test states that the number of times that the loop-gain contour encircles the point $1 + j0$ in a clockwise direction is equal to the difference between the number of zeroes and the number of poles of $1 - \beta(s)A_v(s)$ with positive real parts (i.e., in the right-half plane). The point $1 + j0$ is called the *critical point*. To be specific, let N be the number of clockwise encirclements of the critical point by the Nyquist plot, let P be the number of right-half plane poles of $\beta(s)A_v(s)$ (which are the same as those of $1 - \beta(s)A_v(s)$), and let Z be the number of right-half plane zeroes of $1 - \beta(s)A_v(s)$. The Nyquist stability test states that $N = Z - P$ (or $Z = N + P$). If $Z > 0$ (or $N + P > 0$) the feedback amplifier is unstable and will oscillate under proper conditions. (Note: In the case that there is a right-half plane pole-zero cancellation, the Nyquist test is not sufficient to determine stability.)

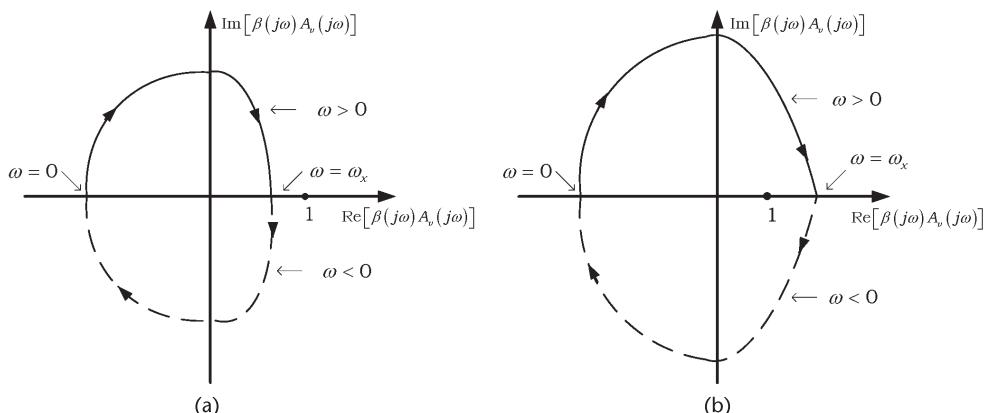


Figure 1.3 (a) A Nyquist plot of a stable feedback amplifier and (b) a Nyquist plot of an unstable feedback amplifier.

If $\beta(s)A_v(s)$ has no poles in the right-half plane, then it follows that $1 - \beta(s)A_v(s)$ has no poles in the right-half plane (i.e., $P = 0$). Thus, in this case $A_{vf}(s)$ is unstable (i.e., has right-half plane poles) only if $1 - \beta(s)A_v(s)$ has right-half plane zeroes (i.e., if $N > 0$). In other words, for $P = 0$ the feedback amplifier is unstable when $N > 0$ (since $N = Z$ when $P = 0$). When $\beta(s)A_v(s)$ is stable, the Nyquist test simply requires that the plot of $\beta(s)A_v(s)$ as a function of ω does not encircle the critical point for the feedback amplifier to be stable. An alternative way of stating the Nyquist test when $\beta(s)A_v(s)$ is stable is: “If $\beta(s)A_v(s)$ is stable, the feedback amplifier is stable if $|\beta(j\omega)A_v(j\omega)| < 1$ when the phase of $\beta(j\omega)A_v(j\omega)$ is 0° or a multiple of 360° .” This condition ensures that the critical point is not enclosed.

In the case that $\beta(s)A_v(s)$ has a pole in the $j\omega$ axis, the contour in the s plane must be modified to avoid the pole. For example, if the pole is at $s = 0$, the path moves from $s = -j\infty$ to $s = j0$, then from $s = j0^-$ to $s = j0^+$ around a semicircle of radius ϵ (where ϵ approaches zero), and then from $s = j0^+$ to $s = j\infty$. From $s = j\infty$ the contour follows a semicircle with infinite radius and moves back to $s = -j\infty$. Hence, the contour encloses all poles and zeroes that $\beta(s)A_v(s)$ has in the right-half plane.

Two typical Nyquist plots for a feedback amplifier with a stable loop gain are shown in Figure 1.3. The solid curve corresponds to $\omega \geq 0$, and the dashed curve to $\omega \leq 0$. Since $\beta(j\omega)A_v(j\omega) = [\beta(j\omega)A_v(j\omega)]^*$ it follows that the dashed curve is simply the mirror image of the solid curve. In Figure 1.3(a) the Nyquist plot does not enclose the critical point. It is seen that at the frequency ω_x the phase of $\beta(j\omega)A_v(j\omega)$ is 0° and its magnitude is less than one. Hence, the amplifier associated with this Nyquist plot is stable. A typical Nyquist plot for an unstable feedback amplifier (with a stable $\beta(s)A_v(s)$) is shown in Figure 1.3(b). For this plot $N = Z = 1$, and the closed-loop response has one pole in the right-half plane.

Example 1.1

(a) Let $\beta(s) = \beta_o$ be a real number and

$$A_v(s) = \frac{K}{s(s + 1)(s + 2)}$$

Hence,

$$\beta(s)A_v(s) = \frac{\beta_o K}{s(s + 1)(s + 2)}$$

and it follows that the number of poles of the loop gain in the right-half plane is zero (i.e., $P = 0$). Therefore, the system is stable if the Nyquist plot of $\beta(s)A_v(s)$ does not encircle the point $1 + j0$ (i.e., if $N = Z = 0$).

The Nyquist plot of $\beta(s)A_v(s)$ for $\beta_o K = 3$ is shown in Figure 1.4(a). This plot shows that the system is stable since there are no encirclements of the $1 + j0$ point.

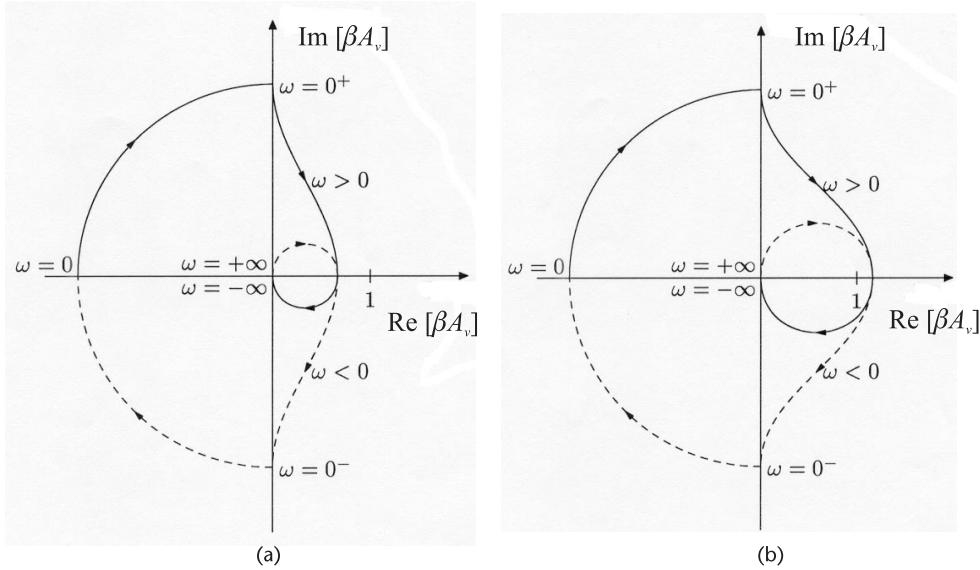


Figure 1.4 Nyquist plots for Example 1.1(a) with (a) $\beta_oK = 3$ and (b) $\beta_oK = 9$.

The resulting Nyquist plot for $\beta_oK = 9$ is shown in Figure 1.4(b). In this case, the plot of $\beta(s)A_v(s)$ encircles the $1 + j0$ point twice in the clockwise direction. Hence, $N = Z = 2$, and the closed loop system is unstable because of two poles in the right-half plane.

In this part of the example the stability depended on the value of β_oK .
 (b) Let $\beta(s) = \beta_o$ be a real number and

$$A_v(s) = \frac{K}{s(s+1)(s-1)}$$

Hence,

$$\beta(s)A_v(s) = \frac{\beta_oK}{s(s+1)(s-1)}$$

and it follows that $P = 1$, since there is a pole at $s = 1$. The Nyquist plots of the loop gain for $\beta_oK > 0$ and $\beta_oK < 0$ are shown in Figure 1.5. The solid curve in the plot corresponds to the mapping for $\omega > 0$, and the dashed curve for $\omega < 0$. Figure 1.5(a) shows that $N = 0$ when $\beta_oK > 0$, and Figure 1.5(b) shows that $N = 1$ when $\beta_oK < 0$; hence, the information in Table 1.1.

That is, the function $1 - \beta(s)A_v(s)$ for $\beta_oK > 0$ has a zero in the right-half plane, and for $\beta_oK < 0$ it has two zeroes in the right-half plane. Obviously, this feedback system is unstable for any real value of β_oK .

The information displayed in the polar Nyquist diagram can also be shown using Bode plots. Thus, the stability of an amplifier can also be determined from the Bode magnitude and phase plots of the loop gain. In terms of the magnitude and phase Bode plots of a stable $\beta(j\omega)A_v(j\omega)$, it follows that the closed-loop gain

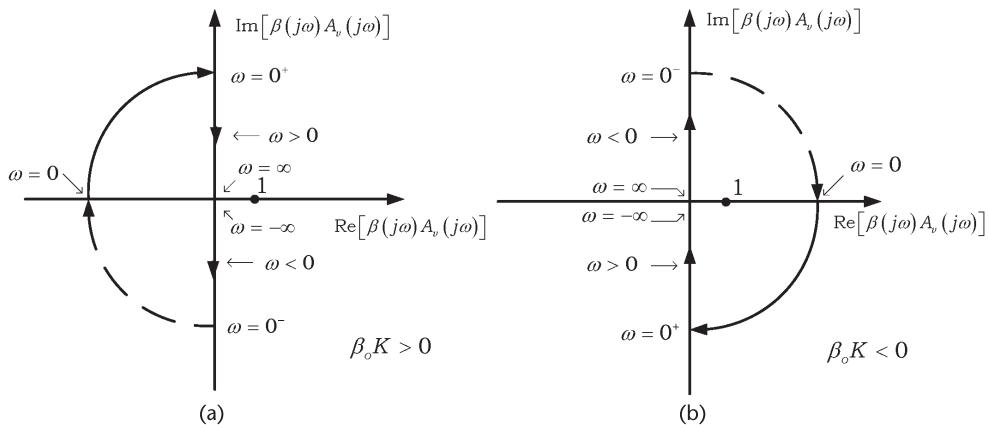


Figure 1.5 Nyquist plots for Example 1.1(b) when (a) $\beta_o K > 0$ and (b) $\beta_o K < 0$.

Table 1.1 Values of Z for Example 1.1(b)

	P	N	$Z = N + P$
$\beta_o K > 0$	1	0	1
$\beta_o K < 0$	1	1	2

is stable if $|\beta(j\omega)A_v(j\omega)|$ in dBs is smaller than 0 dB when the phase shift is 0° (or a multiple of 360°). In other words, the plot of $|\beta(j\omega)A_v(j\omega)|$ in dBs crosses the 0-dB axis at a frequency lower than the frequency at which the phase reaches 0° (or $\pm n 360^\circ$). Typical Bode plots of the magnitude and phase of a stable feedback amplifier are shown in Figure 1.6.

Two important quantities in the determination of stability are the gain margin and the phase margin (shown in Figure 1.6). The gain margin is the number of decibels that $|\beta(j\omega)A_v(j\omega)|$ is below 0 dB at the frequency where the phase is 0° . The phase margin is the number of degrees that the phase is above 0° at the frequency where $|\beta(j\omega)A_v(j\omega)|$ is 0 dB. A positive gain margin shows that the amplifier is potentially unstable. Similarly, a positive phase margin is associated with a stable amplifier. Of course, the gain margin and phase margin can also be shown in a Nyquist diagram.

Typical Bode plots of $\beta(j\omega)A_v(j\omega)$ for feedback amplifiers having one, two, and three poles with $\beta(0)A_v(0) = -K < 0$ are shown in Figure 1.7. The single-pole loop-gain function shown in Figure 1.7(a) has a minimum phase shift of 90° . Therefore, this amplifier is always stable. Figure 1.7(b) shows a loop gain having two poles. Again this amplifier is always stable because the phase shift is positive and approaches 0° only at $\omega = \infty$. Figure 1.7(c) shows a three-pole loop gain that is stable since $|\beta(j\omega)A_v(j\omega)|$ is below 0 dB at the frequency where the phase is 0° (i.e., the gain margin is negative). Figure 1.7(d) shows a three-pole loop gain that is unstable, since the phase is less than 0° at the frequency where $|\beta(j\omega)A_v(j\omega)|$ is 0 dB (i.e., the phase margin is negative).

It is of interest to see how the Nyquist and Bode plots portray the stability information and their relation to the closed loop and transient responses of the

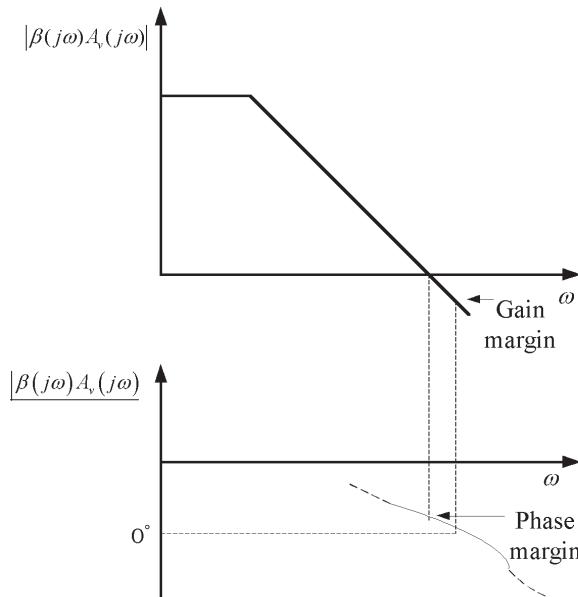


Figure 1.6 A typical Bode plot of the magnitude and phase of a stable feedback amplifier.

feedback amplifier. This is illustrated in Figure 1.8. In the Nyquist plots only the positive frequencies are shown. In the Bode plot the solid curve is for the magnitude of the closed loop response, and the dashed curve is for the phase. Figure 1.8(a) illustrates a stable feedback amplifier with a large positive phase margin. Observe the Bode plots, $|A_{vf}(j\omega)|$, and the transient response. In Figure 1.8(a), as well as in the other figures, the frequency at which $|\beta(j\omega)A_v(j\omega)| = 1$ is f_1 , and the frequency at which $|\beta(j\omega)A_v(j\omega)| = 0^\circ$ is f_2 . The phase margin in Figure 1.8(a) is positive. Figure 1.8(b) illustrates a stable feedback amplifier with a smaller positive phase margin. Observe the larger peak in the associated $|A_{vf}(j\omega)|$ response and in the transient response.

Figure 1.8(c) illustrates an ideal oscillator. The oscillation conditions are satisfied, since $|\beta(j\omega)A_v(j\omega)| = 1$ and $|\beta(j\omega)A_v(j\omega)| = 0^\circ$ at $f = f_1 = f_2$, which results in an ideal stable sinusoidal oscillation (see the plot of $v_o(t)$). Figure 1.8(d) illustrates an unstable oscillation. Observe that $|\beta(j\omega)A_v(j\omega)| > 1$ when $|\beta(j\omega)A_v(j\omega)| = 0^\circ$; hence, positive feedback occurs and $v_o(t)$ shows the associated growing sinusoidal response. Basically, Figure 1.8(c) shows what happens when the complex poles move to the imaginary axis, and Figure 1.8(d) shows what happens when the complex conjugate poles remain in the right-half plane. As we will see, there are ways to determine if the oscillation will be stable or not.

1.4 Root Locus

A root-locus plot is a convenient method to analyze the motion of the closed-loop gain poles in the complex s plane as a function of the amplifier gain, or as a function of the feedback factor. In order to use this method, the denominator of

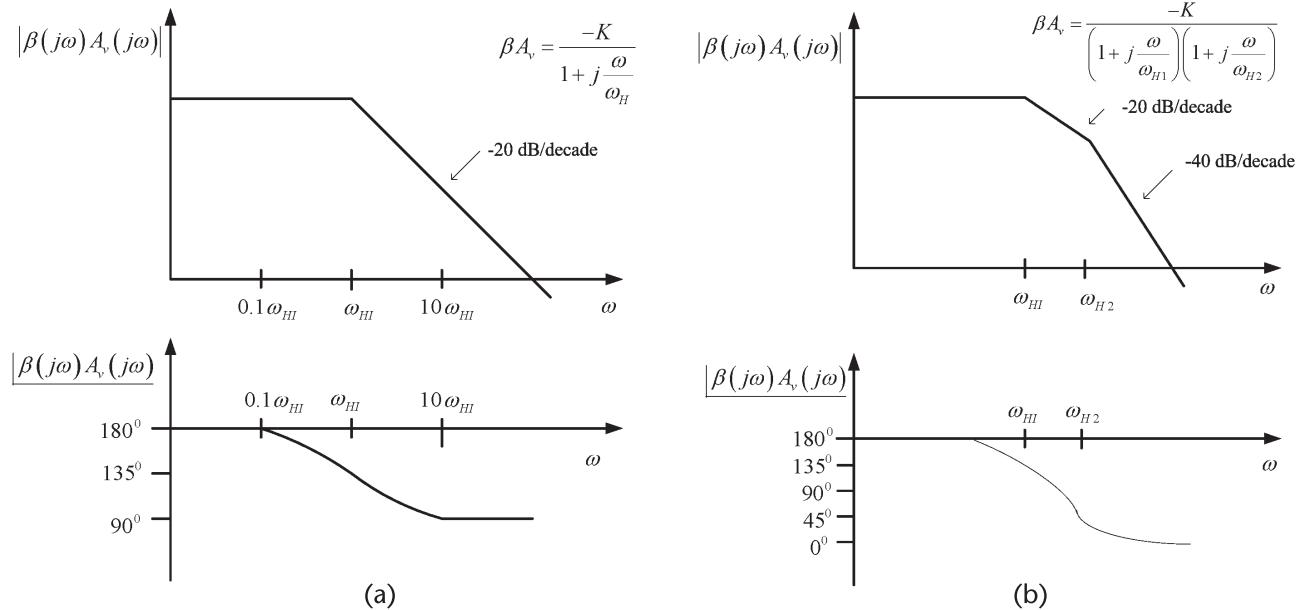


Figure 1.7 Bode plots for a loop gain having (a) one pole, (b) two poles, (c) three poles (stable case), and (d) three poles (unstable case).

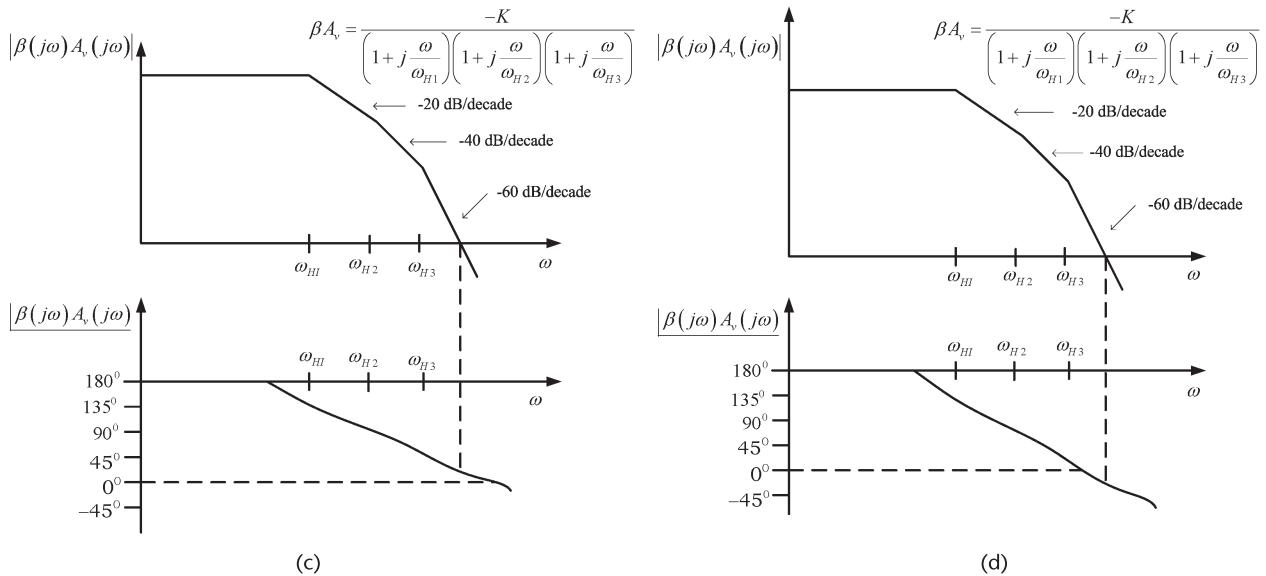


Figure 1.7 (Continued).

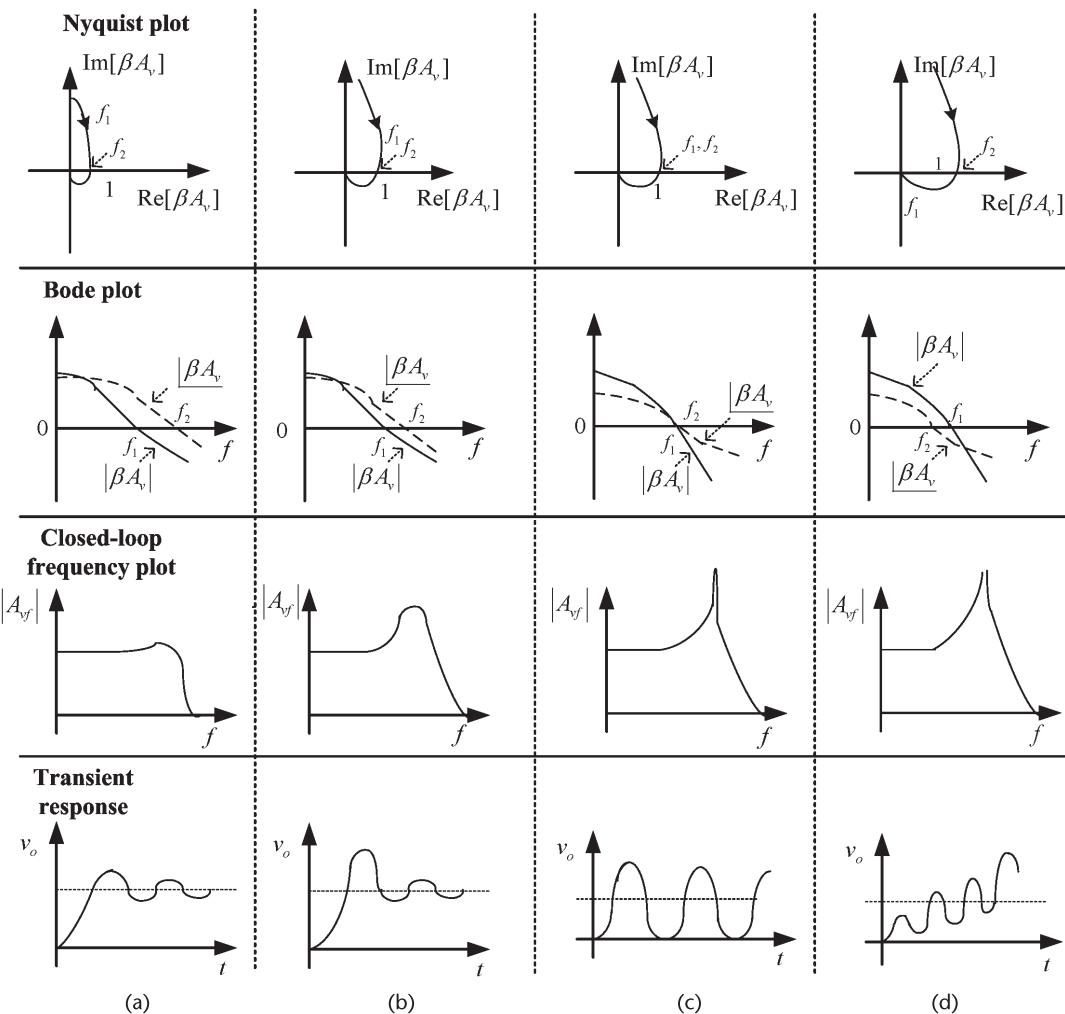


Figure 1.8 Nyquist, Bode, $|A_{vf}(j\omega)|$, and transient response plots of (a) a stable feedback amplifier with a large phase margin, (b) a stable feedback amplifier with a smaller phase margin, (c) a stable oscillator, and (d) an unstable oscillator.

$A_{vf}(s)$ is expressed in polynomial form. The stability of the feedback amplifier is analyzed by observing how the poles of $A_{vf}(s)$ move in the s plane. A typical analysis consists in studying the motion of the roots of $A_{vf}(s)$ as a function of the amplifier open-loop gain, and determining the value of gain that move the roots to the imaginary axis at $s = \pm j\omega_0$. The value of gain and the frequency ω_0 are identical to the values predicted by the Barkhausen criterion (i.e., the gain condition and the frequency of oscillation condition).

Consider the root-locus analysis of a feedback amplifier with a two-pole $A_v(s)$ given by

$$A_v(s) = \frac{A_o}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

and a constant feedback β_o , where $\beta_o < 0$, and A_o is the midband value of $A_v(s)$. Hence, $\beta_o A_o < 0$ and

$$\beta(s) A_v(s) = \frac{\beta_o A_o}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

The closed-loop gain of the feedback amplifier is given by

$$A_{vf}(s) = \frac{A_v(s)}{1 - \beta_o A_v(s)} = \frac{A_o \omega_1 \omega_2}{s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2 (1 - \beta_o A_o)} \quad (1.13)$$

The root locus of the poles in (1.13) follows from the analysis of

$$s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2 (1 - \beta_o A_o) = 0$$

as A_o varies. The root locus is shown in Figure 1.9. This plot shows that for A_o approaching zero the roots are located at $s_1 = -\omega_1$ and $s_2 = -\omega_2$. As A_o increases, the roots move along the negative real axis as shown in Figure 1.9. At a specific value of A_o , denoted by the value of $A_o = A'_o$ (see Figure 1.9), the roots are identical, and for $A_o > A'_o$ the roots become complex but remain in the left-half plane. Therefore, this feedback amplifier is stable. The value of A'_o is given by

$$A'_o = \frac{1}{\beta_o} \left[1 - \frac{0.25(\omega_1 + \omega_2)^2}{\omega_1 \omega_2} \right]$$

Of course, if $\beta_o A_o > 0$ the feedback amplifier is unstable.

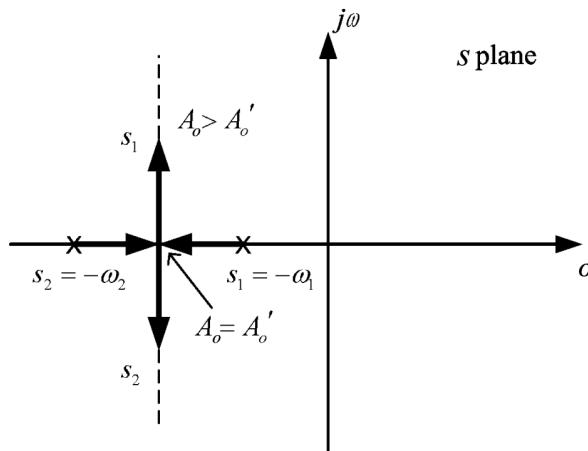


Figure 1.9 Root locus of a two-pole function $A_v(s)$.

Next, consider a three-pole $A_v(s)$ given by

$$A_v(s) = \frac{A_o}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)}$$

with a constant feedback β_o , where $\beta_o < 0$ (i.e., $\beta_o A_o < 0$). In this case $A_{vf}(s)$ is given by

$$A_{vf}(s) = \frac{A_o}{a_3 s^3 + a_2 s^2 + a_1 s + (1 - \beta_o A_o)}$$

where

$$a_3 = \frac{1}{\omega_1 \omega_2 \omega_3}$$

$$a_2 = \frac{1}{\omega_1 \omega_2} + \frac{1}{\omega_1 \omega_3} + \frac{1}{\omega_2 \omega_3}$$

and

$$a_1 = \frac{1}{\omega_1} + \frac{1}{\omega_2} + \frac{1}{\omega_3}$$

The root locus of

$$a_3 s^3 + a_2 s^2 + a_1 s + (1 - \beta_o A_o) = 0$$

is shown in Figure 1.10. For A_o approaching 0, the poles are located at $s_1 = -\omega_1$, $s_2 = -\omega_2$, and $s_3 = -\omega_3$. As A_o increases, the pole s_3 moves along the negative real axis towards $-\infty$, and the poles s_1 and s_2 become complex conjugate poles. At a certain value of A_o the poles are located on the imaginary axis at $s_{1,2} = \pm j\omega_o$ and oscillation occurs. Figure 1.10 also shows that certain values of A_o move the poles into the right-half plane.

Another open-loop gain function that can lead to oscillations is

$$A_v(s) = \frac{A_o \left(1 - \frac{s}{\omega_3}\right)}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

This function has two poles and a right-half plane zero at $s = \omega_3$. This type of transfer function occurs in the high-frequency analysis of several amplifier configurations.

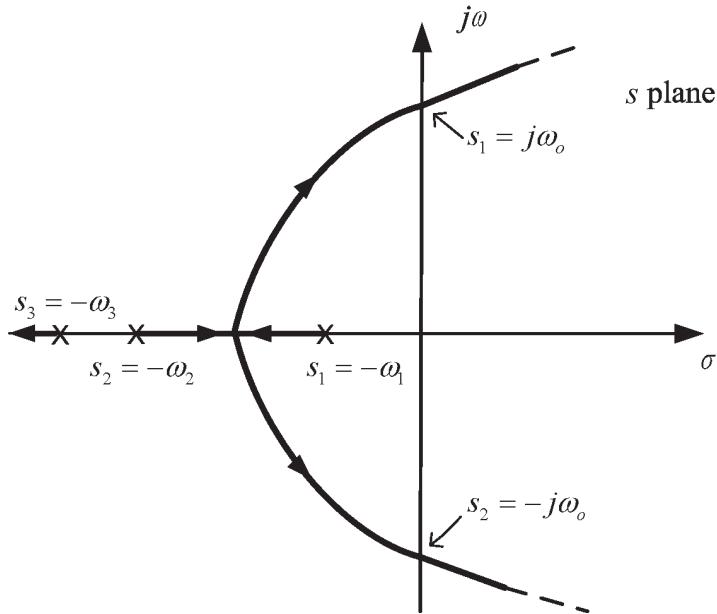


Figure 1.10 Root locus of a three-pole $A_v(s)$.

Example 1.2

Consider the open-loop gain of a CE amplifier given by

$$A_v(s) = \frac{A_o \left(1 - \frac{s}{\omega_3}\right)}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

where $A_o = 2,200$, $\omega_1 = 10^6$ rad/s, $\omega_2 = 10^8$ rad/s, and $\omega_3 = 10^9$ rad/s. Assume that the feedback factor is constant and given by $\beta(j\omega) = \beta_o = -0.1$. The loop gain is

$$\beta(j\omega)A_v(j\omega) = \frac{-0.1(2,200)\left(1 - \frac{s}{10^9}\right)}{\left(1 + \frac{s}{10^6}\right)\left(1 + \frac{s}{10^8}\right)} \quad (1.14)$$

The Nyquist plot of (1.14) is shown in Figure 1.11(a). The behavior of the function in (1.14) around the critical point is difficult to see in Figure 1.11(a). A graph showing the behavior around the critical point is shown in Figure 1.11(b). From (1.14) it follows that $P = 0$, and from the Nyquist plots in Figure 1.11(a, b) we obtain $N = 0$, since the critical point is not enclosed. Therefore, the feedback amplifier with $A_o = 2,200$ is stable, since $Z = N + P = 0$.

Next, assume that A_o is given by $A_o = 22,000$. The Nyquist plot for this case is shown in Figure 1.11(c) and the behavior around the critical point in Figure

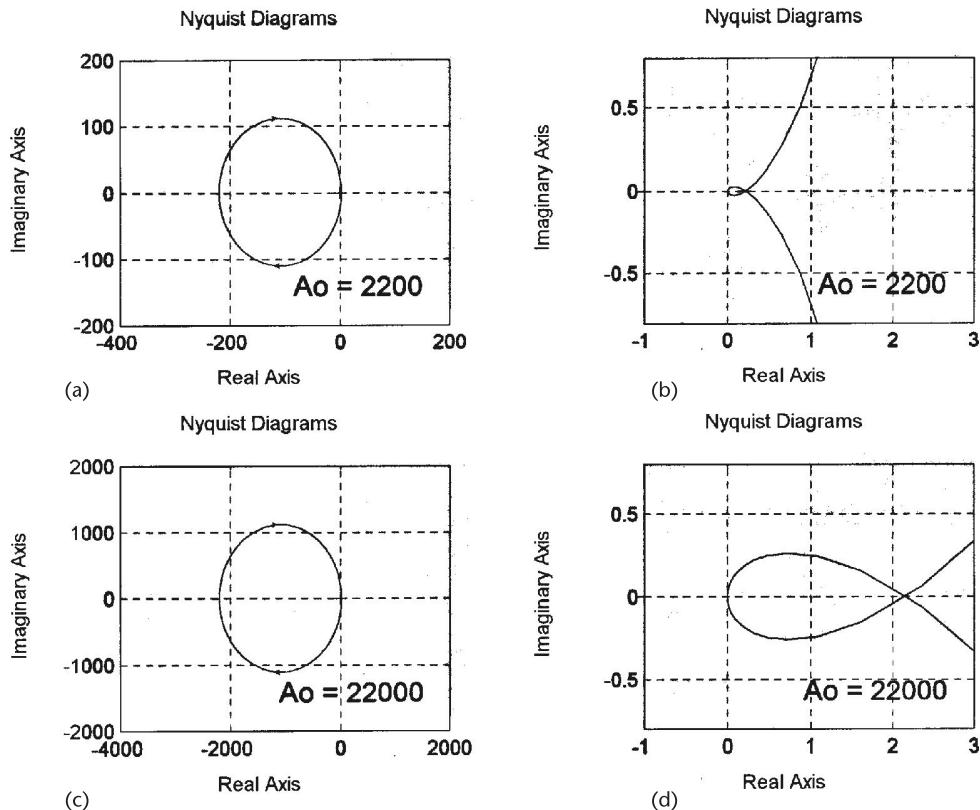


Figure 1.11 (a) Nyquist plot for Example 1.2 with $A_o = 2,220$, (b) the behavior of the loop gain (with $A_o = 2,220$) around the critical point, (c) Nyquist plot for Example 1.2 with $A_o = 22,000$, and (d) the behavior of the loop gain (with $A_o = 22,000$) around the critical point.

1.11(d). Figure 1.11(d) shows that the critical point is enclosed twice, or $N = 2$. Hence, there are two roots in the right-half plane and the amplifier is unstable with $A_o = 22,000$.

The root locus of $A_{vf}(s)$ for this example follows from the analysis of

$$s^2 + s \left(\omega_2 + \omega_1 + \frac{\omega_1 \omega_2 \beta_o A_o}{\omega_3} \right) + \omega_1 \omega_2 (1 - \beta_o A_o) = 0$$

or

$$s^2 + s(101 \times 10^6 - 10^4 A_o) + 10^{14}(1 + 0.1A_o) = 0 \quad (1.15)$$

The resulting root-locus plot is shown in Figure 1.12. For A_o approaching 0 the roots are located at $s_1 = -10^6$ and $s_2 = -10^8$. At the value of $A_o = 10,100$ the complex poles are on the imaginary axis at $s_1 = j318 \times 10^6$ and $s_2 = -j318 \times 10^6$, and oscillations occur.

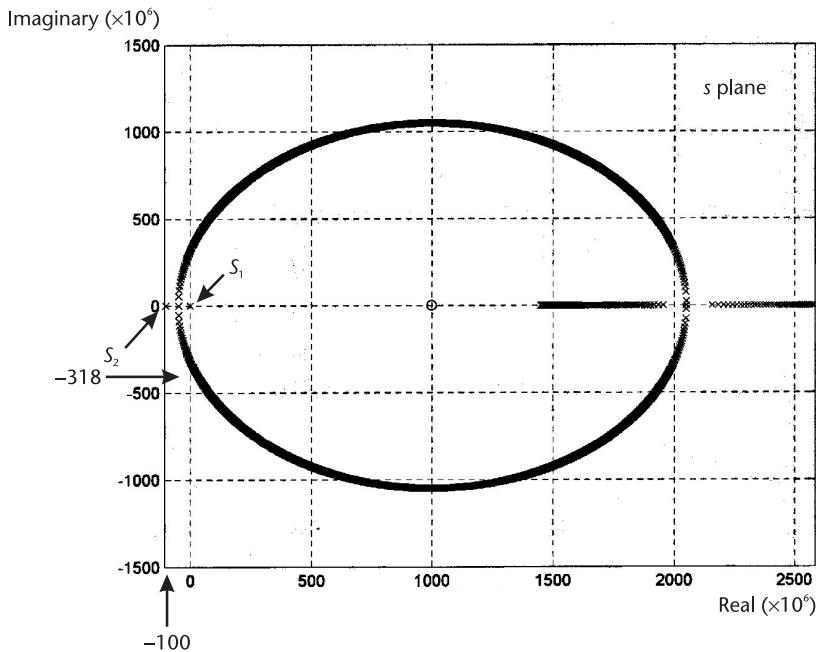


Figure 1.12 Root locus for Example 1.2.

1.5 Routh-Hurwitz Method

Another method that can be used to determine if a polynomial has right-half plane roots is the Routh-Hurwitz method. In the Routh-Hurwitz method the denominator polynomial of $A_{vf}(s)$ is written in the form

$$D(s) = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_1 s + a_0$$

The coefficients are then arranged in the following array form (known as the Routh-Hurwitz array):

s^n	a_n	a_{n-2}	a_{n-4}	.	.
s^{n-1}	a_{n-1}	a_{n-3}	a_{n-5}	.	.
s^{n-2}	b_{n-1}	b_{n-3}	b_{n-5}	.	.
s^{n-3}	c_{n-1}	c_{n-3}	c_{n-5}	.	.
.
s^1	.				
s^0	.				

which shows that a polynomial of degree n has $n + 1$ rows in the Routh-Hurwitz array. The terms b_{n-1} , b_{n-3} , b_{n-5} , etc., are the first, second, third, etc., entries in the $(n - 2)$ row. The terms c_{n-1} , c_{n-3} , c_{n-5} , etc., are the first, second, third, etc., entries in the $(n - 3)$ row. The entries are defined by

$$\begin{aligned}
 b_{n-1} &= \frac{a_{n-1}a_{n-2} - a_n a_{n-3}}{a_{n-1}} \\
 b_{n-3} &= \frac{a_{n-1}a_{n-4} - a_n a_{n-5}}{a_{n-1}} \\
 &\vdots \\
 c_{n-1} &= \frac{b_{n-1}a_{n-3} - a_{n-1}b_{n-3}}{b_{n-1}} \\
 &\vdots
 \end{aligned}$$

The entries in the first column (i.e., a_n , a_{n-1} , b_{n-1} , c_{n-1} , etc.) are called the leading entries in the array. If none of the leading entries vanish, the number of roots of $D(s)$ in the right-half plane is equal to the number of sign changes in the leading entries.

Example 1.3

Determine if the following denominator polynomials of $A_{vf}(s)$ have right-half plane roots:

$$(a) \quad D(s) = s^4 + 10s^3 + 35s^2 + 50s + 24 \quad (1.16)$$

$$(b) \quad D(s) = s^3 + s^2 + 2s + 24 \quad (1.17)$$

Solution

(a) The Routh-Hurwitz array for (1.16) is shown in Figure 1.13(a). The leading entries (i.e., 1, 10, 30, 42, and 24) are positive. Hence, $D(s)$ in (1.16) has no right-half plane roots, or $A_{vf}(s)$ has no right-half plane poles.

The polynomial in (1.16) can be shown to be equal to

$$D(s) = (s+1)(s+2)(s+3)(s+4)$$

which obviously has no right-half plane roots.

(b) The Routh-Hurwitz array for the polynomial in (1.17) is shown in Figure 1.13(b). In this case, the leading entries have two sign changes. Hence, the polynomial in (1.17) has two right-half plane roots, and therefore, $A_{vf}(s)$ is unstable. In fact, the polynomial in (1.17) can be shown to be equal to

$$\begin{array}{c|ccc}
 s^4 & 1 & 35 & 24 \\
 s^3 & 10 & 50 & \\
 s^2 & 30 & 24 & \\
 s^1 & 42 & & \\
 s^0 & 24 & &
 \end{array}
 \quad (a)$$

$$\begin{array}{c|cc}
 s^3 & 1 & 2 \\
 s^2 & 1 & 24 \\
 s^1 & -22 & \\
 s^0 & 24 &
 \end{array}
 \quad (b)$$

Figure 1.13 (a) Routh-Hurwitz array for the polynomial in (1.16) and (b) Routh-Hurwitz array for the polynomial in (1.17).

$$D(s) = (s + 3)(s - 1 + j2.6458)(s - 1 - j2.6458)$$

which has two roots in the right-half plane.

The Routh-Hurwitz method can also be used to determine at what value of the open-loop gain or feedback factor value is the closed-loop gain unstable. Example 1.4 illustrates this point.

Example 1.4

In an oscillator, the denominator polynomial of $A_{vf}(s)$ is

$$D(s) = s^2 + (3 - A_o)s + \omega_o^2 \quad (1.18)$$

where A_o is the amplifier gain and ω_o is the frequency of oscillation. Determine for what values of A_o there are right-half plane roots.

Solution

The Routh-Hurwitz array for (1.18) is shown in Figure 1.14.

The leading entries are 1, $3 - A_o$, and 2. Hence, the feedback system is stable if $3 - A_o > 0$ or $A_o < 3$. The feedback system is unstable when $3 - A_o < 0$ or $A_o > 3$. Oscillations can occur when $A_o = 3$. This oscillator is analyzed in detail in the next section.

There are some degenerate cases that can occur in the Routh-Hurwitz array. One case occurs when a leading entry vanishes, and at least one entry in the corresponding row is nonzero. The other case occurs when a complete row vanishes. For these degenerate cases the reader is referred to an appropriate textbook in control systems.

Next, the loop-gain associated with an oscillator is analyzed. The oscillator selected is the Wien bridge, which provides an example where the feedback factor and the open-loop voltage gain are evaluated separately. In many oscillators the feedback network is loaded by the amplifier, and this effect must be taken into consideration in the analysis of the loop gain.

1.6 The Wien-Bridge Oscillator

The Wien-bridge oscillator is shown in Figure 1.15. The four arms of the bridge are R_1 , R_2 , Z_a , and Z_b . The op amp maintains the voltage across two of the arms equal, since $v_- = v_+$. This oscillator can be used to analyze in closed form the conditions for oscillation, its stability, and the location of the complex poles.

$$\begin{array}{c|cc} s^2 & 1 & 2 \\ s^1 & 3 - A_o \\ s^0 & 2 \end{array}$$

Figure 1.14 Routh-Hurwitz array for Example 1.4.

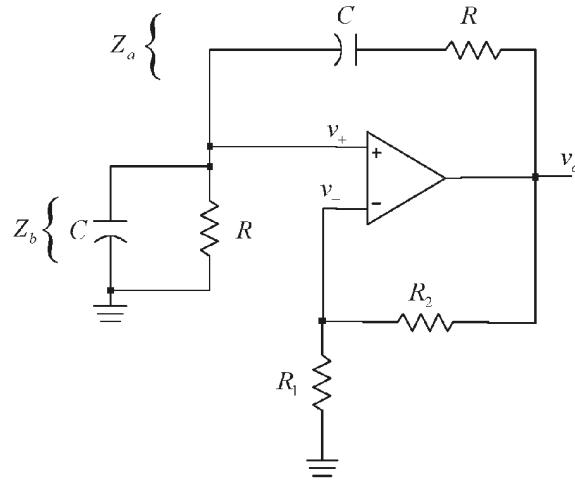


Figure 1.15 The Wien-bridge oscillator.

From Figure 1.15 it is seen that there are two feedback paths. Positive feedback occurs between v_o and v_+ through the voltage divider formed by Z_a and Z_b , and negative feedback occurs between v_o and v_- through R_1 and R_2 .

The Wien-bridge oscillator in Figure 1.15 uses an op amp in an inverting configuration (i.e., the negative feedback path) to provide the open-loop gain. The open-loop gain is constant and given by

$$A_v(j\omega) = A_{vo} = \frac{v_o}{v_+} = 1 + \frac{R_2}{R_1} \quad (1.19)$$

The voltage v_+ is given by

$$\begin{aligned} v_+ &= v_o \frac{Z_b}{Z_b + Z_a} = v_o \frac{\left(\frac{R}{1 + j\omega RC} \right)}{R + \frac{1}{j\omega C} + \left(\frac{R}{1 + j\omega RC} \right)} \\ &= v_o \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC} \right)} \end{aligned}$$

Therefore, the voltage-feedback transfer function $\beta(j\omega)$ can be written in the form

$$\beta(j\omega) = \frac{v_+}{v_o} = \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC} \right)} \quad (1.20)$$

From (1.19) and (1.20) it follows that the loop gain is

$$\beta(j\omega)A_{vo} = \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)} \left(1 + \frac{R_2}{R_1}\right) \quad (1.21)$$

For oscillation the loop gain must be unity. The frequency of oscillation and the gain condition are given by (1.7) and (1.6), respectively.

The condition (1.7) requires that the imaginary part of $\beta(j\omega)$ be zero. From (1.20) it is seen that $\beta_i(j\omega) = 0$ when

$$\omega RC - \frac{1}{\omega RC} = 0 \Rightarrow \omega = \omega_o = \frac{1}{RC}$$

or

$$f_o = \frac{1}{2\pi RC} \quad (1.22)$$

The frequency f_o is the frequency of oscillation.

At $\omega = \omega_o$ the real part of $\beta(j\omega)$ is

$$\beta_r(\omega_o) = \frac{1}{3}$$

Therefore, from (1.6) the gain condition is

$$A_{vo} = \frac{1}{\beta_r(\omega_o)} = 3$$

and from (1.19) it follows that $R_2 = 2R_1$. In practice, the gain should be greater than 3 to start the oscillation. Values of 3.1 to 3.3 are reasonable.

It is interesting to observe that the op amp uses negative feedback through R_1 and R_2 to provide the required gain A_{vo} , and it uses positive feedback through the RC networks to obtain the required closed-loop phase shift. The attenuation in the positive feedback loop must be equal to the gain A_{vo} , making the loop gain equal to one. Since the phase shift through the op amp is zero at ω_o , the phase shift through the RC networks must also be zero so the feedback signal v_+ is in phase with v_o [see (1.20) at $\omega = \omega_o$].

The frequency of oscillation can be varied by simultaneously changing the capacitance values using a ganged capacitor arrangement. In addition, different frequency ranges can be selected by simultaneously switching different values of the resistors R .

A final observation is that op amps in this book are assumed to operate from a dual power supply. Of course, op amps with a single power supply can be used if proper single-supply techniques are used.

Further insight into the Wien-bridge oscillator is obtained by analyzing the oscillator in terms of the circuit poles. The poles of the closed-loop gain $A_{vf}(s)$ are the roots of $1 - \beta(s)A_{vo} = 0$. Using (1.21) with $s = j\omega$ the roots of $A_{vf}(s)$ are given by

$$1 - \frac{A_{vo}}{3 + \frac{s}{\omega_o} + \frac{\omega_o^2}{s}} = 0$$

or

$$s^2 + (3 - A_{vo})\omega_o s + \omega_o^2 = 0 \quad (1.23)$$

The two roots of (1.23) are shown in Figure 1.16 in a root-locus plot as a function of A_{vo} . As A_{vo} varies from 0 to 1, the poles move along the negative real axis. For $A_{vo} = 1$, the poles meet at $-\omega_o$. As A_{vo} varies from 1 to 3, the poles are complex and move in a semicircular path towards the imaginary axis. For $A_{vo} = 3$, the complex poles are located at $j\omega_o$ and $-j\omega_o$, respectively. As A_{vo} increases above 3, the complex poles move into the right-half plane; and at $A_{vo} = 5$ the poles meet on the positive real axis at ω_o . For $A_{vo} > 5$, they move along the positive real axis.

The conditions that produce complex poles are now analyzed. Observe that $1 < A_{vo} < 3$ corresponds to a loop gain of $\beta(j\omega_o)A_{vo} < 1$, and $3 < A_{vo} < 5$ corresponds to a loop gain of $\beta(j\omega_o)A_{vo} > 1$. For $1 < A_{vo} < 3$ the poles produce an output voltage with an exponentially damped sinusoidal response, and for $3 < A_{vo} < 5$ an exponentially growing sinusoidal response results. In order to start the oscillation, a value of gain slightly greater than 3 is used. Thus, at the start of oscillation the complex poles are in the right-half plane and an exponentially growing sinusoidal oscillation is produced. As the amplitude of the oscillation increases, the op amp saturates and its gain decreases. When the gain is 3, the poles are on the imaginary axis (i.e., to $s = \pm j\omega_o$); and when the gain goes below 3, the poles move into the left-half plane. In the Wien-bridge oscillator in Figure 1.15, the amplitude of the sinusoidal oscillation is limited by the saturation of the op amp. Hence, the oscillation amplitude varies between approximately $V^+ - 1$ and $V^- + 1$.

Wien-bridge oscillators work very well for frequencies up to about 1 MHz. With an amplitude-limiting circuit the harmonic distortion can be less than 5%.

The Wien bridge can also be constructed with different values of the branch values of R and C . If

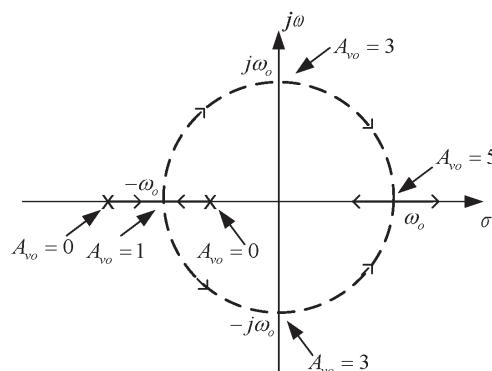


Figure 1.16 Poles of the closed-loop gain as a function of A_{vo} .

$$Z_a = R_a + \frac{1}{j\omega C_a}$$

and

$$Z_b = \frac{R_b}{1 + j\omega C_b}$$

it follows that for oscillation: $R_a C_a = R_b C_b$, and the frequency of oscillation is given by

$$f_o = \frac{1}{2\pi R_a C_a} = \frac{1}{2\pi R_b C_b}$$

The required gain of the amplifier is

$$A_{vo} = \frac{1}{\beta(j\omega_o)} = 1 + \frac{2R_1}{R_2}$$

Example 1.5

Design the Wien-bridge oscillator shown in Figure 1.15 to oscillate at 5 kHz.

Solution

A practical value of $0.01 \mu\text{F}$ for the capacitors can be selected. Then, using (1.22), the value of R is

$$R = \frac{1}{2\pi f_o C} = \frac{1}{2\pi(5 \times 10^3)(0.01 \times 10^{-6})} = 3.18 \text{ k}\Omega$$

A practical value of $3 \text{ k}\Omega$ can be used in series with a trimming potentiometer to set the frequency of oscillation at 5 kHz.

To start the oscillation, a value of $A_{vo} = 3.2$ is used. From (1.19), a gain of 3.2 is obtained with $R_2 = 22 \text{ k}\Omega$ and $R_1 = 10 \text{ k}\Omega$. The supply voltages of the op amp can be selected as 12V and -12V. The transient simulation of the oscillator, using a 741 op amp is shown in Figure 1.17. Observe that the output voltage reaches saturation producing a clipping in the output waveform and, therefore, a significant amount of distortion. This occurs because the starting condition requires $A_{vo} > 3$, and the gain of the amplifier changes when its output reaches saturation. The fundamental frequency of oscillation (i.e., $f_o = \text{freq}[1] = 5.0002 \text{ kHz}$) is close to the predicted value using $\beta(j\omega_o)A_{vo} = 1$.

Example 1.5 shows that some sort of amplitude-limiting mechanism is needed to reduce the harmonic distortion. There are several ways of accomplishing amplitude limiting. The amplitude of oscillation is determined by the loop gain, which is made to be greater than 1 in order to start the oscillation, and by the nonlinearities

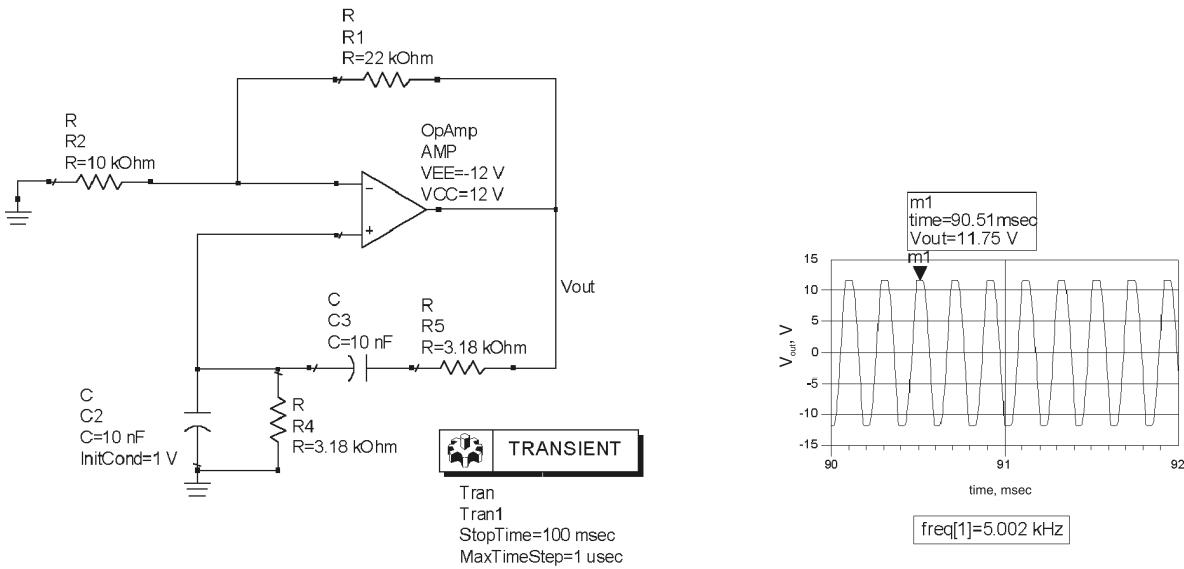
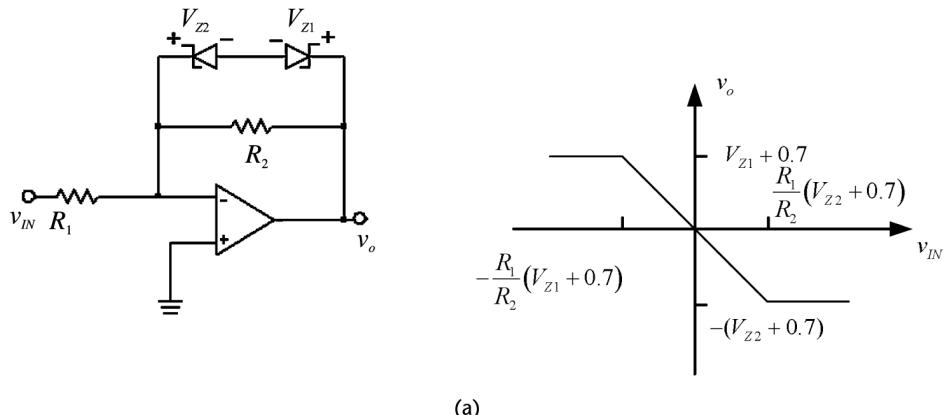


Figure 1.17 Simulation of the Wien-bridge oscillator in Example 1.5.

of the amplifier and feedback network. If the feedback network is a passive network, the nonlinearities of the amplifier determine the amplitude of oscillation. This procedure, as seen in Figure 1.17, generates unwanted harmonics since the amplitude of the oscillation is limited by the saturation voltage of the op amp. In order to remove these harmonics, a bandpass filter that passes only the oscillation frequency can be used after the amplifier. Of course, the nonlinearities of the amplifier can be avoided by limiting somehow the amplitude of the oscillation before the amplitude reaches the amplifier's saturation value. There are many circuits that can be used to limit the amplitude of the oscillator. Some of these circuits are shown in Figure 1.18.

Figure 1.18(a) shows a limiting circuit using back-to-back Zener diodes (usually $V_{Z1} = V_{Z2}$). The output is limited to $-(V_{Z2} + 0.7) < v_o < (V_{Z1} + 0.7)$. When the Zeners are not conducting, the op-amp gain is $-R_2/R_1$. The transfer function of this circuit is illustrated in Figure 1.18(a). Another limiting circuit is shown in Figure 1.18(b) with its transfer function. In this circuit the gain between v_o and v_{IN} changes from A_{v1} (when the Zeners conduct) to A_{v2} (when the Zeners are not conducting).

An amplitude-limiting mechanism is basically an automatic gain control (AGC) circuit that forces the amplifier gain to decrease when the amplitude of the



(a)

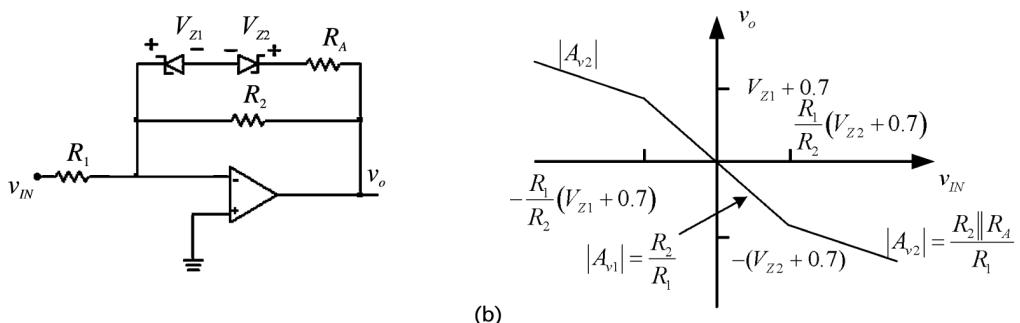


Figure 1.18 (a) A limiting circuit and the associated transfer functions and (b) another limiting circuit.

oscillation increases. Figure 1.19 shows three Wien-bridge oscillators with amplitude-limiting mechanisms. In Figure 1.19(a), when the diodes are off, the gain is $1 + R_2 \parallel R_1$; and when a diode is on, the gain is reduced to $1 + (R_2 \parallel R_3)/R_1$. The start up condition requires a gain slightly greater than 3 or

$$\frac{R_2}{R_1} > 2 \quad (1.24)$$

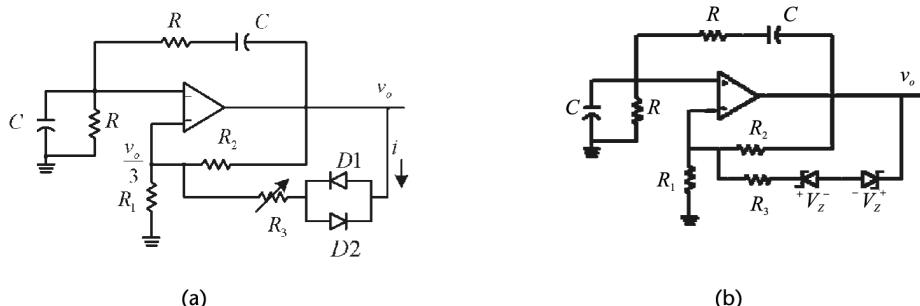
and when a diode is on, the gain should be slightly less than 3, or

$$\frac{R_2 \parallel R_3}{R_1} < 2 \quad (1.25)$$

The inequality in (1.24) can be satisfied by making it equal to a value between 2.1 to 2.2 and in (1.25) using a value between 1.8 and 1.9.

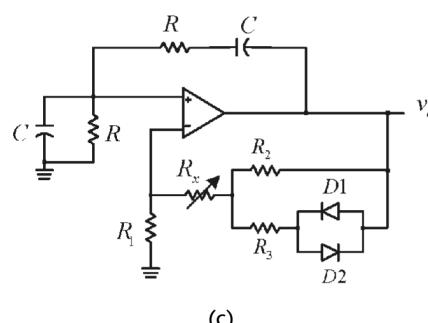
When a diode is conducting, the amplitude of the output voltage is limited. Since $v_+ = v_- = v_o/3$, a nodal equation gives

$$\frac{v_o}{3R_1} = \frac{v_o - \frac{v_o}{3}}{R_2} + \frac{v_o - \frac{v_o}{3} - V_D}{R_3}$$



(a)

(b)



(c)

Figure 1.19 Three Wien-bridge oscillators with (a, b, c) amplitude-limiting mechanism.

or

$$v_o = \frac{3V_D}{2\left(1 + \frac{R_3}{R_2}\right) - \frac{R_3}{R_1}} \quad (1.26)$$

where $V_D \approx 0.5V$ for an actual diode.

Equation (1.26) shows that the amplitude of v_o depends on R_3 . This equation can be used to obtain the value of R_3 for a given amplitude of v_o . Since in this oscillator the gain is controlled by the circuit, it provides an opportunity to verify that the location of the poles changes between the right-half plane and the left-half plane, and how the pole movement is related to the Barkhausen criterion in the determination of the frequency of oscillation (see Example 1.6).

In Figure 1.19(b) the amplitude-limiting mechanism is implemented with Zener diodes. The analysis of this oscillator is similar to the previous analysis. The output voltage is given by (1.26) with V_D replaced by $V_Z + V_D$. A simple way of designing this oscillator is to let $R_2 \parallel R_1 = 2.15$ and $(R_2 \parallel R_3)/R_1 = 1.8$, which can be satisfied with $R_2 = 2R_a$, $R_1 = 0.93R_a$, and $R_3 = 10R_a$ (R_a is a scaling factor). As an example, with $V_Z = 4.2V$, and selecting $R_a = 5 k\Omega$, it follows that $R_1 = 4.65 k\Omega$, $R_2 = 10 k\Omega$, and $R_3 = 50 k\Omega$. The amplitude of the oscillation is limited to $v_o = 9.7V$.

In Figure 1.19(c) a modification of the amplitude control circuit that produces smaller values of the control resistors is shown. For this circuit the design equations are

$$\frac{R_2 + R_x}{R_1} > 2$$

$$\frac{(R_2 \parallel R_3) + R_x}{R_1} < 2$$

and

$$v_o = \frac{3V_D}{\left(2 - \frac{R_x}{R_1}\right)\left(1 + \frac{R_3}{R_2}\right) - \frac{R_3}{R_1}} \quad (1.27)$$

Obviously, as $R_x \rightarrow 0$, (1.27) reduces to (1.26).

Usually, in these oscillators a buffer stage (i.e., a unity gain amplifier) is used to couple the oscillation signal.

The following example helps to explain why, although not exact, the Barkhausen criterion is useful in predicting the expected frequency of oscillation. As Lindberg [1] mentioned, the placement of the poles on the imaginary axis is an impossible act of balance.

Example 1.6

- (a) Design the Wien-bridge oscillator shown in Figure 1.20(a) to oscillate at $\omega_0 = 10$ krad/s with an amplitude of 2V.
 (b) Repeat part (a) for an amplitude of 10V.

Solution

- (a) From (1.22) with $C = 0.01 \mu\text{F}$ and $R = 10 \text{k}\Omega$, the desired $\omega_0 = 10 \text{ krad/s}$ is obtained.

To start the oscillation, a value of $A_{vo} = 3.2$ (or $R_2 \parallel R_1 = 2.2$) is used. This can be obtained with $R_2 = 11 \text{k}\Omega$ and $R_1 = 5 \text{k}\Omega$. From (1.26), if $V_D = 0.45\text{V}$, an amplitude of 2V is obtained with $R_3 = 73 \text{k}\Omega$; and if $V_D = 0.6\text{V}$, the value is $R_3 = 60.5 \text{k}\Omega$.

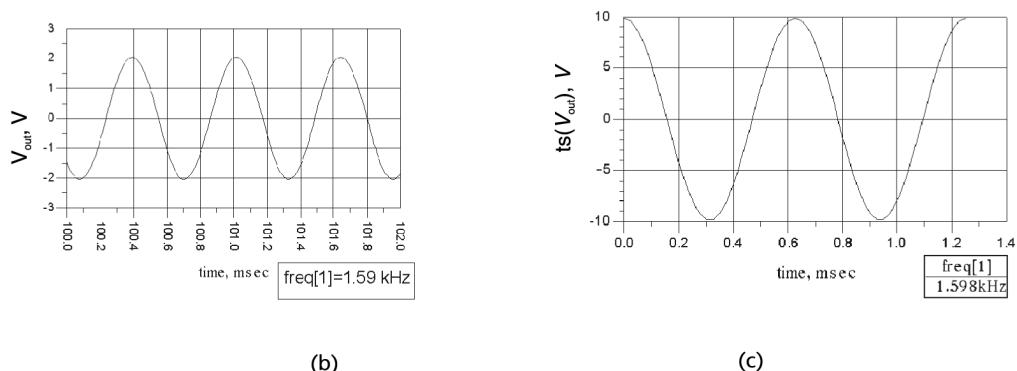
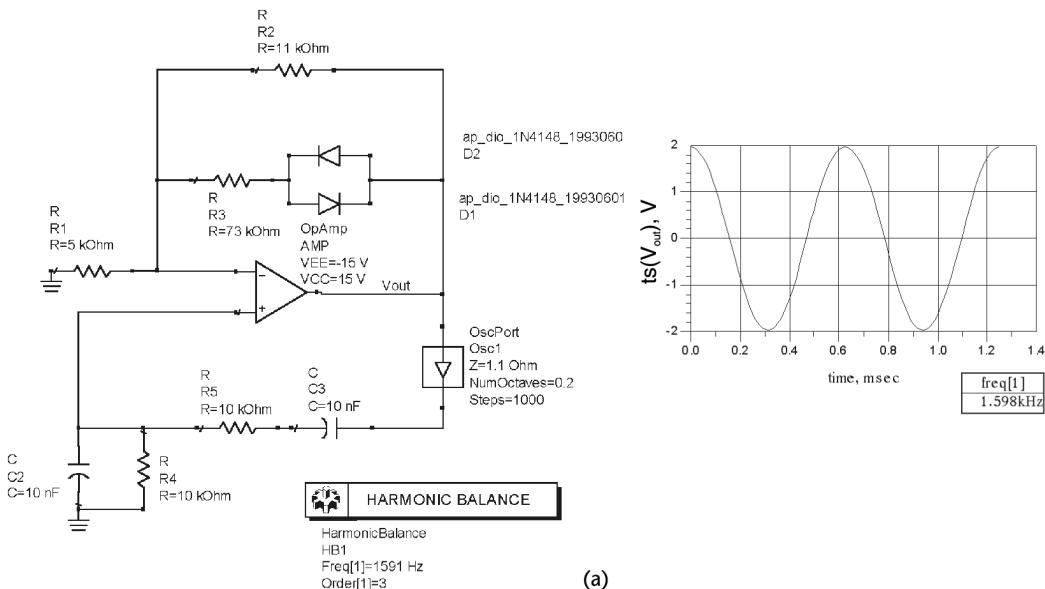


Figure 1.20 (a) ADS simulation for Example 1.6 for $v_0=2\text{V}$, (b) transient simulation results, and (c) simulation result for $v_0=10\text{V}$.

The harmonic-balance simulation of this oscillator is shown in Figure 1.20(a) with $R_3 = 73 \text{ k}\Omega$, and the transient simulation data is shown in Figure 1.20(b). The fundamental frequency of oscillation is $\text{freq}[1] = 1.598 \text{ kHz}$ (or $\omega_o = 10.04 \text{ krad/s}$). The current waveform in the diodes shows the on/off states of the diodes.

For this design, when the diodes are off the gain is $A_{vo} = 3.2$. From (1.23), the poles of the closed-loop gain are located at

$$s^2 - 2,000s + 10^8 = 0$$

or

$$s_{1,2} = 1,000 \pm j9,949.9 \quad (1.28)$$

Therefore, the poles are in the right-half plane.

When a diode conducts, the gain is reduced to

$$A_{vo} = 1 + \frac{73 \times 10^3 \parallel 11 \times 10^3}{5 \times 10^3} = 2.912$$

and the new location of the poles, using (1.23), is

$$s^2 + 880s + 10^8 = 0$$

or

$$s_{1,2} = -440 \pm j9,990.3 \quad (1.29)$$

From (1.28) and (1.29) it is seen that the poles move between the right-half plane and the left-half plane. The frequency associated with the poles in the right-half plane is $\omega_{o,1} = 9,949.9 \text{ rad/s}$, and the frequency associated with the poles in the left-half plane is $\omega_{o,2} = 9,990.3 \text{ rad/s}$. The frequency of oscillation predicted by the Barkhausen criterion is $\omega_o = 10 \text{ krad/s}$, which occurs if the poles are on the $j\omega$ axis. However, the poles of this oscillator are moving between $\omega_{o,1}$ and $\omega_{o,2}$. This variation in frequency produces a fundamental frequency of oscillation and the associated harmonics.

(b) An amplitude of $v_o = 10V$ can be obtained with $R_1 = 5 \text{ k}\Omega$, $R_2 = 11 \text{ k}\Omega$, and $R_3 = 101 \text{ k}\Omega$. When the diodes are not conducting, the poles are in the right-half plane and are given by (1.28). When a diode conducts the poles move to the left-half plane and $A_{vo} = 2.9821$. Their location is calculated using (1.23), namely,

$$s^2 + 179s + 10^8 = 0$$

or

$$s_{1,2} = -89.5 \pm j9,979.6$$

Hence, the poles of this oscillator are moving between $\omega_{o,1} = 9,949.9$ rad/s and $\omega_{o,2} = 9,979.6$ rad/s.

The simulation results are shown in Figure 1.20(c). The fundamental frequency of oscillation is 1.598 kHz.

Another Wien-bridge oscillator with an amplitude-limiting circuit is shown in Figure 1.21. In this oscillator the amplitude-limiting circuit consists of the diodes $D1$ and $D2$, and the resistors R_3 , R_4 , R_5 , and R_6 . To understand the operation of the amplitude-limiting circuit, observe that as v_o increases, the voltage at node v_y will exceed the voltage v_1 , forcing $D2$ to conduct. When $D2$ conducts, the value of v_y is $v_y = v_1 + 0.7$, and v_o is clamped at the value $v_{o(\max)}$, given by

$$v_y = v_1 + 0.7 = \frac{v_{o(\max)} R_6}{R_5 + R_6} + \frac{V^- R_5}{R_5 + R_6} \quad (1.30)$$

Since v_1 is approximately $v_o/3$, it follows from (1.24) that

$$\frac{v_{o(\max)}}{3} + 0.7 = \frac{v_{o(\max)} R_6}{R_5 + R_6} + \frac{V^- R_5}{R_5 + R_6} \quad (1.31)$$

Similarly, as v_o decreases, the voltage v_x will drop below v_1 , forcing $D1$ to conduct. When $D1$ conducts, the voltage v_x is $v_x = v_1 - 0.7$, and v_o is clamped at the value $v_{o(\min)}$, given by

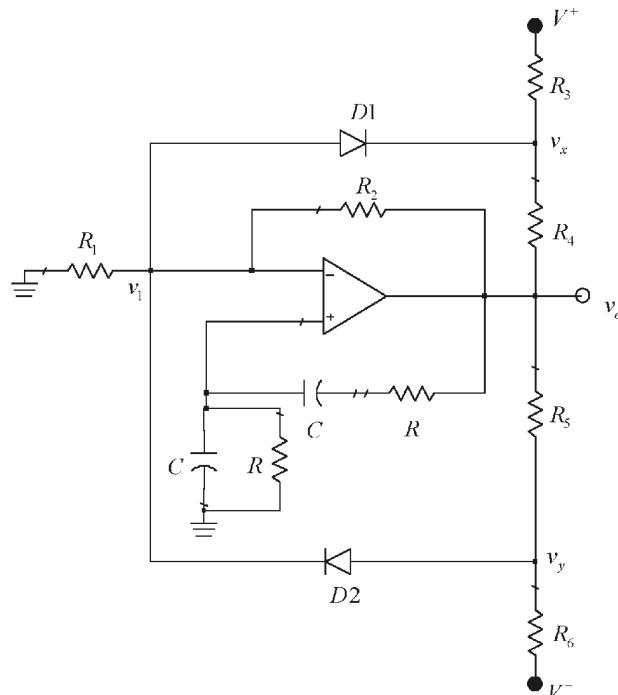


Figure 1.21 Wien-bridge oscillator with an amplitude-limiting circuit.

$$\nu_x = \frac{\nu_{o(\min)}}{3} - 0.7 = \frac{\nu_{o(\min)} R_3}{R_3 + R_4} + \frac{V^- R_4}{R_3 + R_4} \quad (1.32)$$

The simultaneous solution of (1.31) and (1.32) gives the value of the resistors that limit the output voltage to $\nu_{o(\min)} < \nu_o < \nu_{o(\max)}$. In order to obtain a symmetrical sinusoidal voltage, the selection $R_3 = R_6$ and $R_4 = R_5$ is usually made.

Example 1.7

Design an amplitude-limiting circuit for the 5-kHz Wien-bridge oscillator in Example 1.5. The amplitude of the sinusoidal output voltage is to be limited to $|\nu_o| = 5\text{V}$.

Solution

With $\nu_{o(\max)} = 5\text{V}$ and $\nu_{o(\min)} = -5\text{V}$, it follows from (1.31) and (1.32) that $R_3 = R_6 = 10.9\text{ k}\Omega$ and $R_4 = R_5 = 2\text{ k}\Omega$.

To start the oscillation a voltage gain of 3.2 is obtained with $R_2 = 22\text{ k}\Omega$ and $R_1 = 10\text{ k}\Omega$. The simulation of the oscillator is shown in Figure 1.22. Obviously, the harmonic content of the oscillator in Figure 1.22 is much less than the one in Figure 1.17.

Another way of stabilizing the amplitude of oscillation is to use a thermistor in the circuit. Thermistors with positive- and negative-temperature coefficients are available. A negative-temperature coefficient thermistor has a resistance that decreases as the temperature increases. For example, in Figure 1.15 a negative-temperature coefficient thermistor can be used for R_2 . Hence, as the amplitude of oscillation increases, the current in R_2 increases and its resistance decreases, resulting in a decrease in A_{vo} which makes $\beta(j\omega_o)A_{vo} = 1$.

A positive-temperature coefficient device that can also be used to stabilize the oscillation is a tungsten filament lamp. In low-wattage lamps, cold resistances of a few ohms to hundreds of ohms are available, with hot resistance values being about 5 to 10 times larger than the cold values. The schematic of a Wien-bridge oscillator using a filament lamp is shown in Figure 1.23. The nonlinearities associated with the lamp resistance provide a challenge in the control of ν_o .

In oscillators that use op amps the maximum frequency of operation is limited by the frequency response of the op amp. The op amp frequency response is limited by either its gain-bandwidth product or by its slew rate. The gain-bandwidth product is a *small-signal* limitation, which limits the frequency of oscillation to

$$f_o < \frac{f_T}{|A_{vo}|} \quad (1.33)$$

where f_T is the gain-bandwidth product frequency, and A_{vo} is the midband gain of the amplifier. For an inverting amplifier $A_{vo} = -R_2/R_1$, and for a noninverting amplifier $A_{vo} = 1 + R_2/R_1$.

The slew rate is a large-signal limitation, which limits the frequency of oscillation to

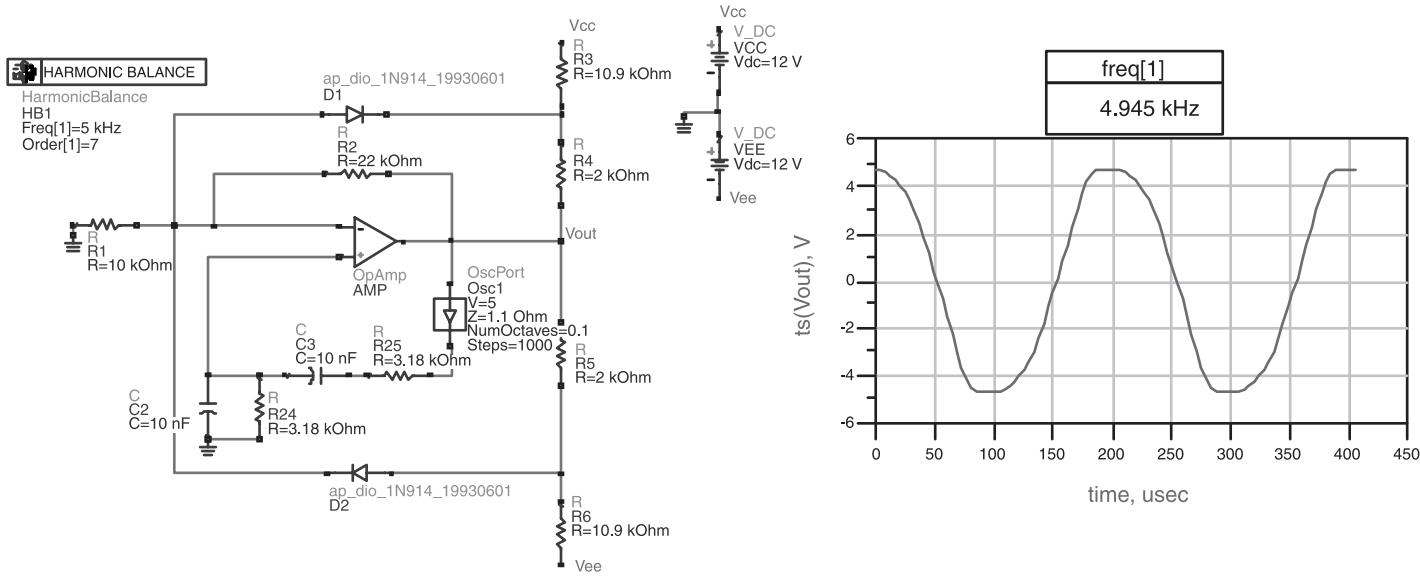


Figure 1.22 ADS simulation of the oscillator in Example 1.7.

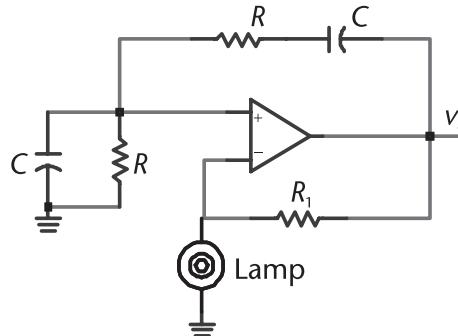


Figure 1.23 A Wien-bridge oscillator using an incandescent lamp for stability.

$$f_o < \frac{SR}{2\pi|v_o|} \quad (1.34)$$

where SR is the op amp slew rate, and $|v_o|$ is the magnitude of the output voltage.

In the absence of an amplitude-limiting circuit, $|v_o|$ is limited by the op amp saturation. A limiting circuit keeps the operation of the op amp in its linear region (i.e., away from saturation). For a designed value of $|v_o|$, the smaller of the two f_o values in (1.33) or (1.34) limits the maximum oscillation frequency. It also follows that larger values of f_o are obtained, if the amplitude of the oscillation is limited using an amplitude limiting circuit.

1.7 The Phase-Shift Oscillator

Phase-shift oscillators usually use RC networks in the feedback path. A phase-shift oscillator is shown in Figure 1.24(a). The op amp is used in an inverting configuration with a gain of $-R_2/R$. Thus, the signal experiences a phase shift of -180° through the amplifier, and the phase shift from each RC section is 60° at the frequency of oscillation, for a total phase shift in the feedback path of 180° . The total phase shift around the closed loop is 0° (i.e., $-180^\circ + 180^\circ$). If the gain condition is satisfied, the circuit will oscillate at the frequency where the total phase shift is zero.

The phase-shift network is composed of three RC sections. The following analysis provides insight into the behavior of the phase-shift network. The transfer function of the single RC section shown in Figure 1.25 is

$$\frac{v_2}{v_1} = \frac{j\omega RC}{1 + j\omega RC} = \frac{j\frac{\omega}{\omega_L}}{1 + j\frac{\omega}{\omega_L}}$$

where

$$\omega_L = \frac{1}{RC}$$

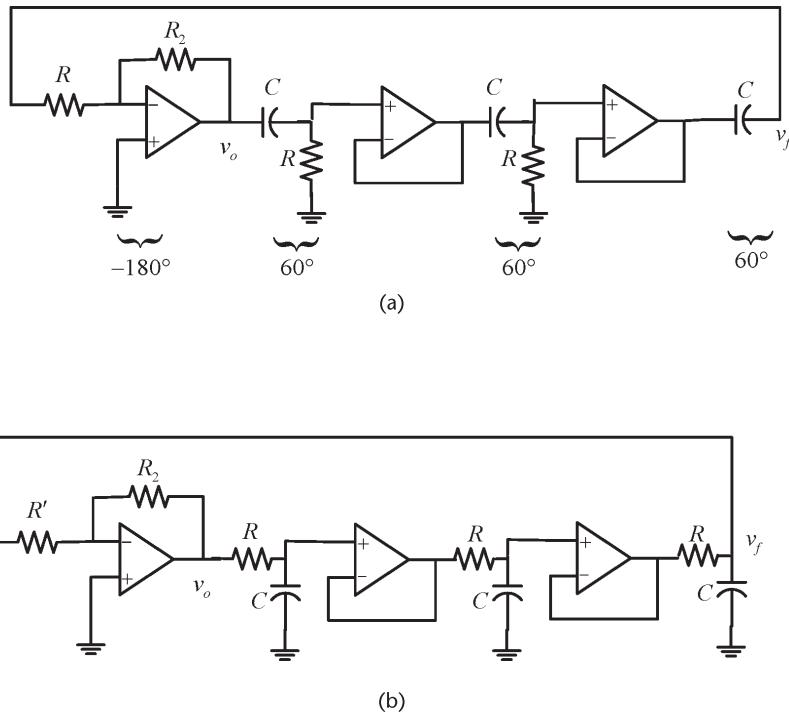


Figure 1.24 (a) A phase-shift oscillator and (b) with RC interchanged.

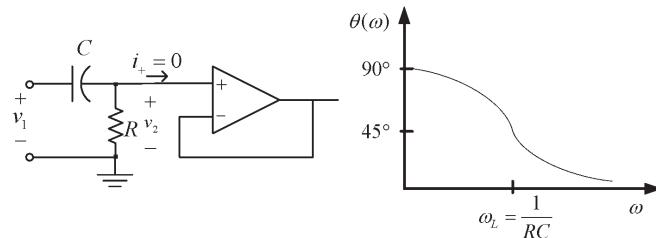


Figure 1.25 A single RC section.

Hence, the phase shift is

$$\theta(\omega) = 90^\circ - \tan^{-1} \frac{\omega}{\omega_L} \quad (1.35)$$

Equation (1.35) shows that the largest phase shift that can be obtained from a single RC section is 90° . Two RC sections will have a phase shift smaller than 180° . Therefore, a minimum of three RC sections is needed to obtain a phase shift of 180° at the frequency of oscillation.

The phase-shift network in Figure 1.24(a) is described by the feedback factor, namely,

$$\beta(j\omega) = \frac{v_f}{v_o} = \left(\frac{j \frac{\omega}{\omega_L}}{1 + j \frac{\omega}{\omega_L}} \right)^3 = \frac{-\left(\frac{\omega}{\omega_L}\right)^3}{\frac{\omega}{\omega_L} \left[3 - \left(\frac{\omega}{\omega_L}\right)^2 \right] - j \left[1 - 3 \left(\frac{\omega}{\omega_L}\right)^2 \right]} \quad (1.36)$$

The imaginary part of $\beta(j\omega)$ will vanish at the frequency

$$\omega_o = \frac{1}{\sqrt{3}RC}$$

which is the frequency of oscillation. At the frequency of oscillation it follows from (1.35) that each RC section produces a phase shift of 60° .

From (1.36) the real part of $\beta(j\omega)$ at ω_o is $\beta_r = -1/8$. Therefore, from (1.6), the gain condition is

$$A_{vo} = \frac{1}{\beta_r} = -8$$

Hence, it follows that

$$\frac{R_2}{R} = 8$$

The phase-shift oscillator in Figure 1.24(a), implemented with R and C interchanged in each RC section, is shown in Figure 1.24(b). The resistor R should be large so that it does not load the third RC section. Of course, a buffer amplifier (i.e., a unity gain amplifier) can be used between the third section and the resistor R to avoid the loading. In the configuration shown in Figure 1.24(b) the loop gain is

$$\beta(j\omega)A_{vo} = \frac{A_{vo}}{\left(1 + j \frac{\omega}{\omega_L}\right)^3}$$

Hence, it follows that the frequency of oscillation is given by

$$\omega_o = \frac{\sqrt{3}}{RC}$$

and the gain condition is satisfied with $R_2/R' = 8$.

Another phase-shift oscillator is shown in Figure 1.26. In this oscillator the RC sections are connected without isolation and, therefore, there is loading. In the last stage the resistors R and R_1 appear in parallel. The loading of R_1 can be neglected if $R_1 \parallel R \approx R$, or in some cases by removing R in the third stage and letting $R_1 = R$.

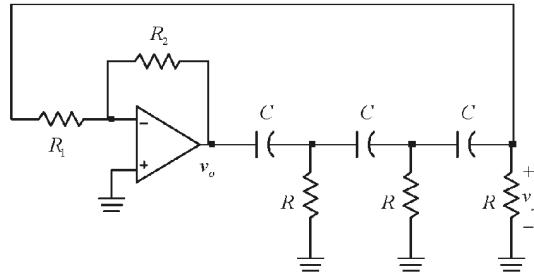


Figure 1.26 A phase-shift oscillator using a single op amp.

The analysis of the phase-shift network in Figure 1.26 with $R_1 \parallel R \approx R$ gives

$$\beta(j\omega) = \frac{v_f}{v_o} = \frac{1}{\left(\frac{1}{j\omega RC}\right)^3 + 5\left(\frac{1}{j\omega RC}\right)^2 + 6\left(\frac{1}{j\omega RC}\right) + 1} \quad (1.37)$$

The imaginary part of $\beta(j\omega)$ comes from the first and third term in the denominator, namely the odd-power terms. The imaginary part of $\beta(j\omega)$ will vanish when

$$\left(\frac{1}{j\omega RC}\right)^3 + 6\left(\frac{1}{j\omega RC}\right) = 0$$

or at

$$\omega = \omega_o = \frac{1}{\sqrt{6RC}} \quad (1.38)$$

At the frequency of oscillation the phase-shift network produces a phase shift of 180° .

From (1.37) the real part of $\beta(j\omega)$ at ω_o is

$$\beta_r(\omega_o) = \frac{1}{\frac{5}{(j\omega_o RC)^2} + 1} \quad (1.39)$$

Substituting (1.38) into (1.39) gives

$$\beta_r(\omega_o) = \frac{1}{5(-6) + 1} = -\frac{1}{29}$$

and from (1.6), the gain condition is

$$A_{vo} = \frac{1}{\beta_r(\omega_o)} = -29 \quad (1.40)$$

In Figure 1.26 the resistors R_1 and R_2 provide an inverting gain of

$$A_{vo} = \frac{v_o}{v_f} = -\frac{R_2}{R_1}$$

Hence, the start of oscillator condition is satisfied if R_1 and R_2 are selected to provide $|A_{vo}| > 29$.

To summarize, the phase-shift oscillator in Figure 1.26 will oscillate at the frequency ω_o given by (1.38) if the gain is $|A_{vo}| > 29$. The loading of the op amp is minimized by making $R_1 > 10R$.

The phase-shift oscillator in Figure 1.26 could have been implemented by interchanging R and C in the phase-shift sections. It follows that for such an oscillator the frequency of oscillation is given by

$$\omega_o = \frac{\sqrt{6}}{RC}$$

and the gain condition is $|A_{vo}| > 29$.

Example 1.8

Design the RC oscillator shown in Figure 1.26 to oscillate at 1 kHz.

Solution

Selecting the capacitor values to be $0.1 \mu\text{F}$, then from (1.38)

$$R = \frac{1}{\omega_o \sqrt{6} C} = \frac{1}{(2\pi \times 10^3) \sqrt{6} (0.1 \times 10^{-6})} = 650\Omega$$

The resistors R_1 and R_2 must provide the gain $|A_{vo}| > 29$ in order to prevent loading $R_1 \parallel R \approx R$. Letting $R_1 = 15 \text{ k}\Omega$, then $R_2 = 29R_1 = 435 \text{ k}\Omega$. A $495\text{-k}\Omega$ resistor was used to implement R_2 . This will allow for some extra gain to satisfy the start of oscillation condition (i.e., $|A_{vo}| > 29$).

This oscillator is easy to construct. However, some adjustments in the RC network (due to component variations) are necessary in order to obtain the desired frequency of oscillation. The use of precision resistors and capacitors is recommended. The simulation of this oscillator is shown in Figure 1.27. The fundamental frequency of oscillation is 1.006 kHz. Observe that the output voltage reaches saturation (i.e., $|v_o| \approx 11\text{V}$), since the circuit uses the nonlinearities of the operational amplifier at saturation to determine the amplitude of oscillation. The clipping in the output waveform produces harmonic distortion.

The harmonic distortion can be significantly reduced with an amplitude-limiting circuit. One such oscillator circuit is shown in Figure 1.28. The amplitude-limiting circuit is designed using (1.30) and (1.32), with v_1 set equal to zero (i.e., $v_y = 0.7\text{V}$ and $v_x = 0.7\text{V}$).

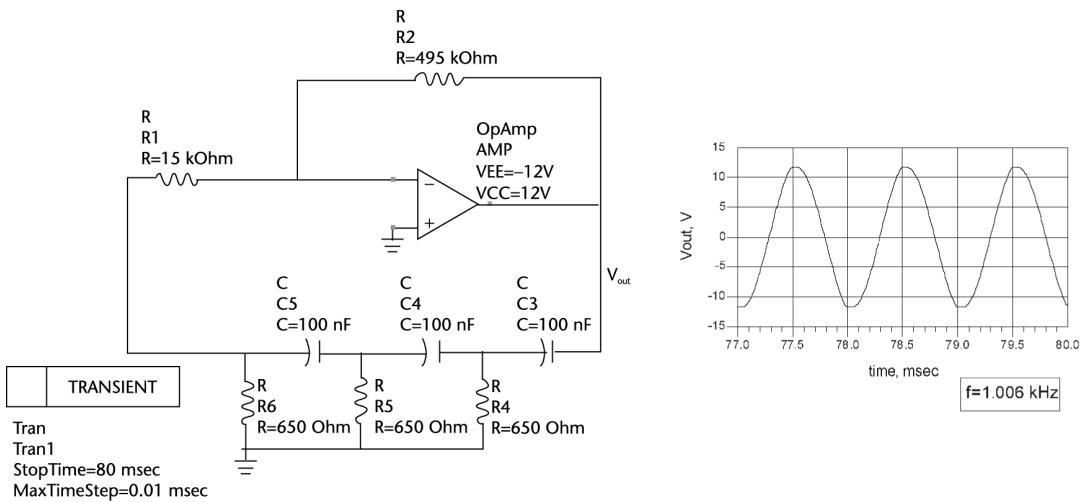


Figure 1.27 ADS simulation of the phase-shift oscillator in Example 1.8.

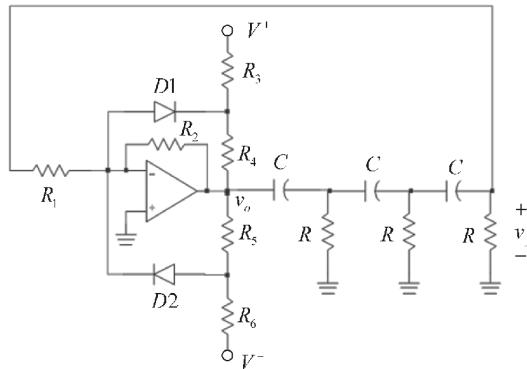


Figure 1.28 A phase-shift oscillator with an amplitude-limiting circuit.

Example 1.9

Design the phase-shift oscillator in Figure 1.28 to oscillate at 1 kHz. The amplitude of the output voltage is to be limited to ±5V.

Solution

The design of the amplitude-limiting circuit is similar to the one in Example 1.7. From (1.30), with $v_1 = 0$ and $v_{o(\max)} = 5V$, we obtain

$$0.7 = \frac{5R_6}{R_5 + R_6} - \frac{12R_5}{R_5 + R_6}$$

which can be satisfied with $R_5 = 2\text{ k}\Omega$ and $R_6 = 5.9\text{ k}\Omega$. From (1.32), for symmetry, we obtain $R_3 = R_6 = 5.9\text{ k}\Omega$ and $R_4 = R_5 = 2\text{ k}\Omega$.

The simulation is shown in Figure 1.29. The fundamental frequency of oscillation is at 1 kHz, and the total harmonic content of this oscillator is certainly less than that in Figure 1.27.

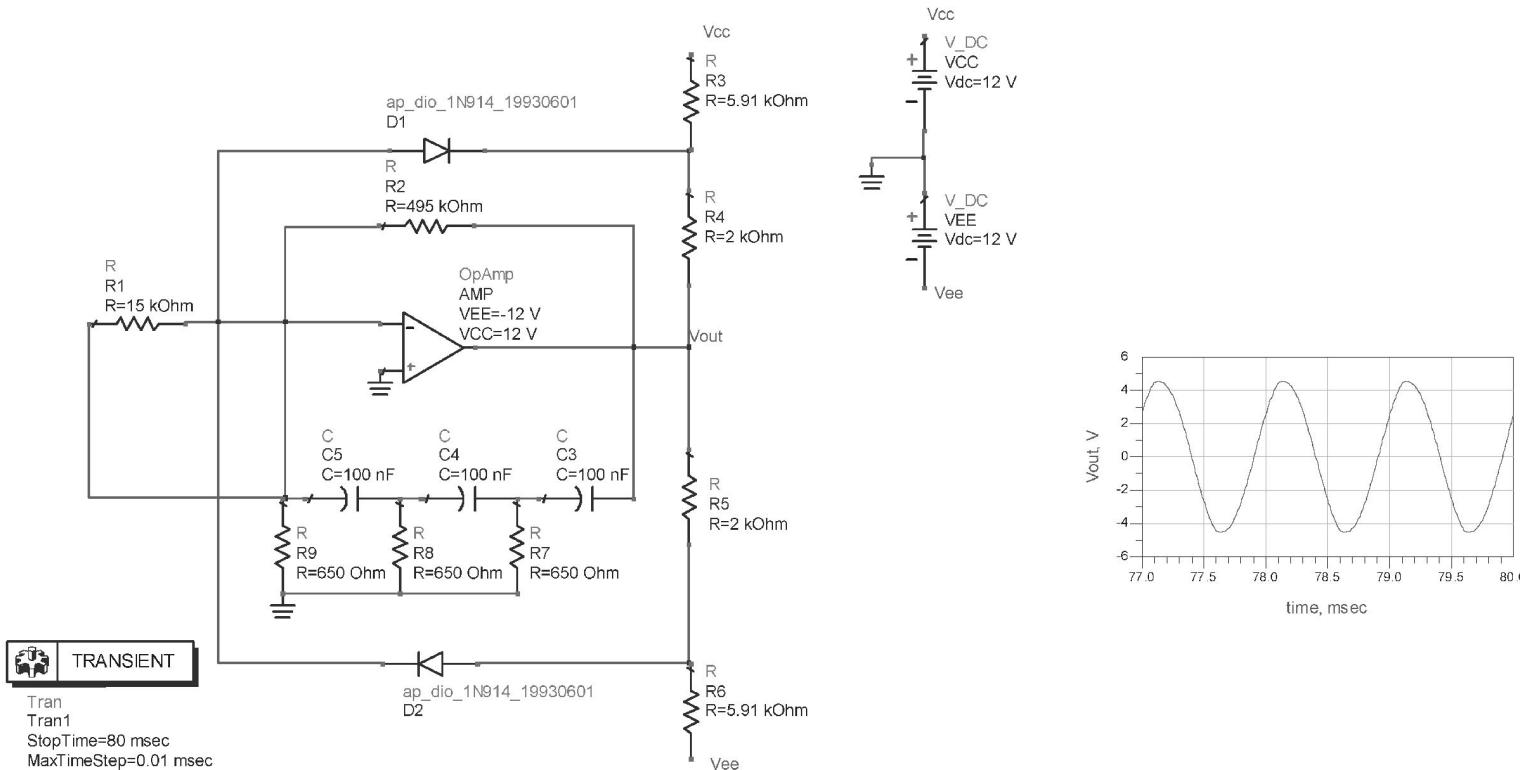


Figure 1.29 Phase-shift oscillator with an amplitude-limiting circuit.

An interesting phase-shift oscillator is shown in Figure 1.30. It is composed of three integrators with transfer function of

$$A_v(j\omega) = \frac{-\frac{1}{R_1 C}}{j\omega + \frac{1}{R_2 C}}$$

In this oscillator the gain and phase shift is distributed throughout the loop. The loop gain is

$$\beta A_v = \left(\frac{-\frac{1}{R_1 C}}{j\omega + \frac{1}{R_2 C}} \right)^3 = \frac{-\left(\frac{R_2}{R_1}\right)^3}{[1 - 3(\omega R_2 C)^2] + j\omega R_2 C [3 - (\omega R_2 C)^2]} \quad (1.41)$$

From (1.41) the imaginary part vanishes at the frequency

$$\omega_o = \frac{\sqrt{3}}{R_2 C}$$

and the gain condition follows from setting the loop gain at $\omega = \omega_o$ equal to unity, namely,

$$\beta A_v = \frac{1}{8} \left(\frac{R_2}{R_1} \right)^3 = 1$$

or $R_2 = 2R_1$.

In this oscillator the phase shift from each integrator is 120° at ω_o . Since at ω_o the gain of each stage is 1 $|120^\circ$, the three output voltages are equal in magnitude but at 120° from each other.

A quadrature oscillator produces two signals having a phase shift of 90° . Some phase-shift oscillators can produce signals in quadrature. For example, an additional

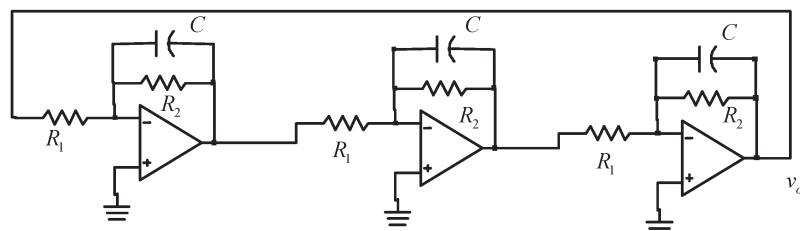


Figure 1.30 A phase-shift oscillator using op amp integrators.

RC section could have been added to the phase-shift oscillators in Figure 1.24(b), so that each section produces a phase shift of -45° , or -90° every two sections. The resulting quadrature oscillator that produces a sine and a cosine signal is shown in Figure 1.31. The amplifier gain is

$$A_{vo} = \frac{v_o}{v_f} = -\frac{R_2}{R'}$$

and the RC phase-shift network transfer function is

$$\beta(j\omega) = \frac{v_f}{v_o} = \frac{1}{\left(1 + j\frac{\omega}{\omega_L}\right)^4} \quad (1.42)$$

Hence, the loop gain is given by

$$\beta(j\omega) A_{vo} = \frac{-\frac{R_2}{R'}}{\left(1 + j\frac{\omega}{\omega_L}\right)^4} \quad (1.43)$$

It is observed that at

$$\omega_o = \omega_L = \frac{1}{RC}$$

each RC section produces a phase shift of -45° , for a total of -180° . Hence, the loop-gain phase shift is -360° . At ω_o , (1.42) gives

$$\beta(j\omega) = \frac{1}{(1+j)^4} = \frac{1}{4} e^{-j\pi}$$

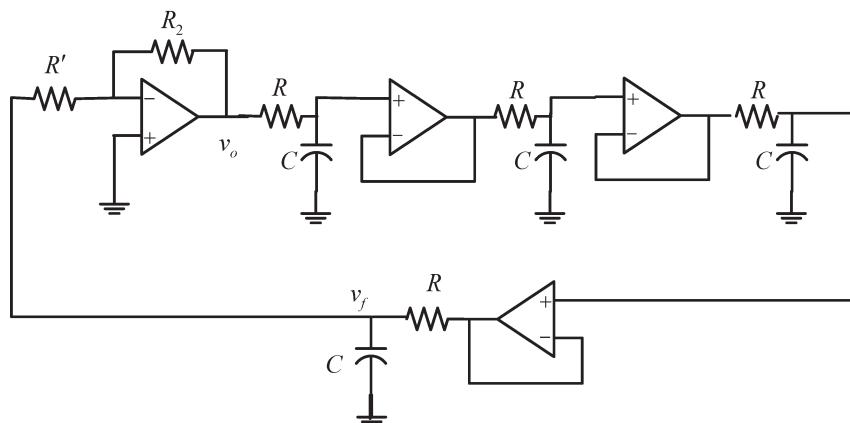


Figure 1.31 A quadrature oscillator.

Therefore, from (1.43) the required gain is

$$A_{vo} = -4 \Rightarrow \frac{R_2}{R'} = 4$$

A gain greater than 4 is required to start the oscillation (say, $A_{vo} = 4.2$).

Another quadrature oscillator is shown in Figure 1.32. The second op amp is connected as an inverting integrator; that is,

$$A_{v2} = \frac{v_{o2}}{v_{o1}} = -\frac{1}{j\omega R_2 C_2} \quad (1.44)$$

This inverter produces a phase shift of -270° (or 90°).

The first op amp is connected as a noninverting integrator; that is,

$$A_{v1}(j\omega) = \frac{v_{o1}}{v_f} = 1 + \frac{1}{j\omega R_1 C_1} = \frac{1 + j\omega R_1 C_1}{j\omega R_1 C_1} \quad (1.45)$$

and the feedback network transfer function is

$$\beta(j\omega) = \frac{v_f}{v_{o2}} = \frac{1}{1 + j\omega R_3 C_3} \quad (1.46)$$

Therefore, from (1.45) and (1.46), with $R_1 C_1 = R_3 C_3$, we obtain

$$\frac{v_{o1}}{v_{o2}} = \frac{1}{j\omega R_1 C_1} \quad (1.47)$$

which shows that the phase shift from v_{o2} to v_{o1} is -90° . From (1.44) and (1.47) the loop phase shift is 0° and oscillations occur with v_{o2} being a sine signal and v_{o1} a cosine signal.

Using (1.44), (1.45), and (1.46), the loop-gain condition is

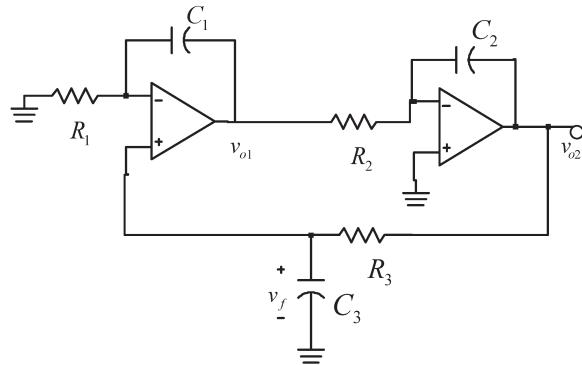


Figure 1.32 A quadrature oscillator.

$$\beta A_{v1}A_{v2} = -\frac{1+j\omega R_1 C_1}{j\omega R_1 C_1} \left(\frac{1}{j\omega R_2 C_2} \right) \frac{1}{1+j\omega R_3 C_3} = 1$$

If $R_1 C_1 = R_2 C_2 = R_3 C_3$, the loop-gain condition reduces to

$$\beta A_{v1}A_{v2} = \frac{1}{(\omega R_1 C_1)^2} = 1$$

and the frequency of oscillation is

$$\omega_o = \frac{1}{R_1 C_1}$$

In a practical quadrature oscillator circuit, the component variations affect the required RC equality, and therefore, some tuning mechanism is needed, such as a variable potentiometer to implement the resistors. In addition, an amplitude-limiting circuit might be needed to reduce the distortion.

A phase-shift oscillator using a JFET amplifier is shown in Figure 1.33. The input resistance of the amplifier (i.e., R_G) is very large and does not load the output of the phase-shift network. However, the output resistance of the amplifier is $r_d \parallel R_D \approx R_D$ and a certain amount of loading occurs. Good results are obtained by neglecting the loading and designing the oscillator based on (1.38) and (1.40), where $A_{vo} \approx -g_m R_D$.

A phase-shift oscillator using a BJT amplifier is shown in Figure 1.34(a). The BJT phase-shift oscillator works well at a frequency below 1 MHz. This is the current-controlled equivalent of the JFET phase-shift oscillator. Since the BJT is a current-controlled device, the oscillation frequency and required gain can be obtained using (1.10). The ac model for this circuit is shown in Figure 1.34(b), where it was assumed that $R_1 \parallel R_2 \gg h_{ie}$ and $1/h_{oe} = \infty$. While an approximate

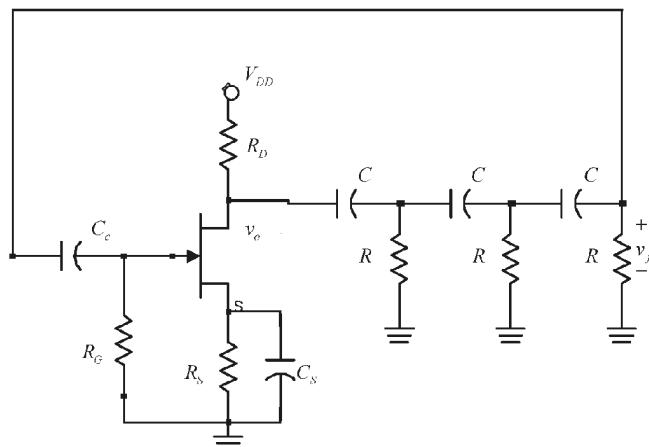


Figure 1.33 A phase-shift oscillator using a JFET amplifier.

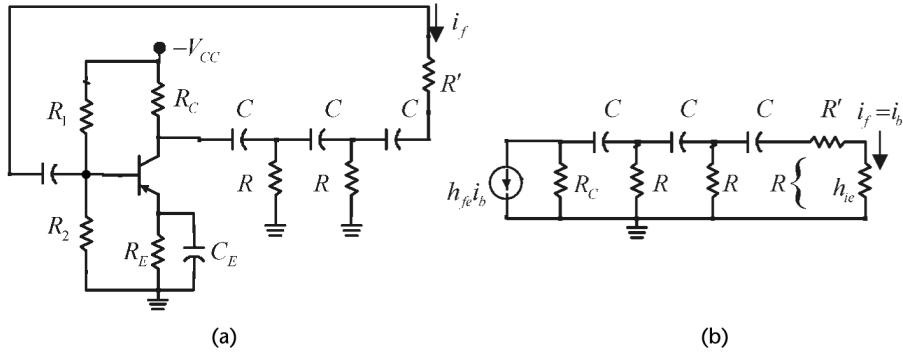


Figure 1.34 (a) A phase-shift oscillator using a BJT amplifier and (b) the phase-shift network.

design can be made by neglecting the effects of \$R_C\$ and \$h_{ie}\$ and the use of a CAD program to optimize the oscillator, it is of interest to show the complexities in the analysis due to their presence in the ac model.

In Figure 1.34(b) the resistor \$R'\$ is selected so that \$R = R' + h_{ie}\$. The feedback current is the current into the base of the transistor (\$i_f = i_b\$), and the input current (\$h_{fe}i_b\$) is the collector current. From Figure 1.34(b) it can be shown that the loop gain is

$$\beta A_v = \frac{i_f}{i_b} = \frac{-h_{fe}}{3 - \frac{1}{\omega^2 R^2 C^2} + \frac{R}{R_c} - \frac{5}{\omega^2 R R_c C^2} - j \frac{4}{\omega R C} - j \frac{6}{\omega R_c C} + j \frac{1}{\omega^3 R^2 R_c C^3}} \quad (1.48)$$

Setting the imaginary part of (1.48) equal to zero gives the frequency of oscillation, namely,

$$\omega_o = \frac{1}{RC \sqrt{6 + \frac{4R_c}{R}}} \quad (1.49)$$

At \$\omega_o\$, setting the loop gain in (1.48) equal to unity gives

$$\frac{-h_{fe}}{3 - \frac{1}{\omega_o^2 R^2 C^2} + \frac{R}{R_c} - \frac{5}{\omega_o^2 R R_c C^2}} = 1 \quad (1.50)$$

Substituting (1.49) into (1.50) results in the following gain condition:

$$h_{fe} = 23 + 29 \frac{R}{R_c} + 4 \frac{R_c}{R} \quad (1.51)$$

This equation can be solved for \$R/R_c\$ as a function of \$h_{fe}\$ to determine the minimum value of \$R/R_c\$ for oscillation. Alternatively, this value can be determined by differentiating (1.51) with respect to \$R/R_c\$ and setting the result equal to zero. That is,

$$29 - 4\left(\frac{R_c}{R}\right)^2 = 0 \Rightarrow \frac{R}{R_c} = \sqrt{\frac{4}{29}} = 0.372$$

With $R/R_c = 0.372$, (1.49) gives $h_{fe} = 44.5$. This is the minimum value of h_{fe} for oscillations. For $h_{fe} = 44.5$ the circuit will oscillate at the frequency given by (1.49). In practical circuits, the transistors' h_{fe} are much larger than 44.5, and the tolerances in the resistors and the capacitors usually makes them unequal (especially in the capacitors). Hence, a variable resistor can be used for R_c , and its value changed until the loop gain is slightly larger than unity and the circuit oscillates at the desired frequency with low distortion. The frequency of oscillation will still be closely predicted by (1.49). Another practical way of building this oscillator is to use a variable resistor for R' .

The RC phase-shift network is one specific case of the general phase-shift network shown in Figure 1.35. It can be shown that for this network

$$\beta(j\omega) = \frac{v_f}{v_o} = \frac{1}{\left(\frac{Z_1}{Z_2}\right)^3 + 5\left(\frac{Z_1}{Z_2}\right)^2 + 6\left(\frac{Z_1}{Z_2}\right) + 1} \quad (1.52)$$

Equation (1.52) shows that oscillations can be obtained with other combinations of Z_1 and Z_2 , provided that $\beta_i(\omega) = 0$. For example, Z_1 can represent a resistor and Z_2 an inductor. Of course, the frequency of oscillation depends on the impedances used. Observe that Z_1 and Z_2 cannot both be reactive, because in such case $\beta(j\omega)$ will not have an imaginary part.

1.8 Active-Filter Oscillators

Many oscillators that use an active-filter feedback path have been proposed. Basically, in these oscillators the poles of an active filter are adjusted to lie on the $j\omega$ -axis at the desired frequency of oscillation. To start the oscillation the poles must be slightly on the right-half plane. A summary of these types of oscillators can be found in [2].

In this section three active-filter oscillators are analyzed to illustrate their design procedure. A simple second-order low-pass filter with positive feedback is shown in Figure 1.36. For this oscillator

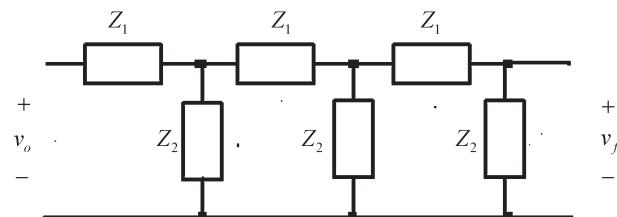


Figure 1.35 A general phase-shift network.

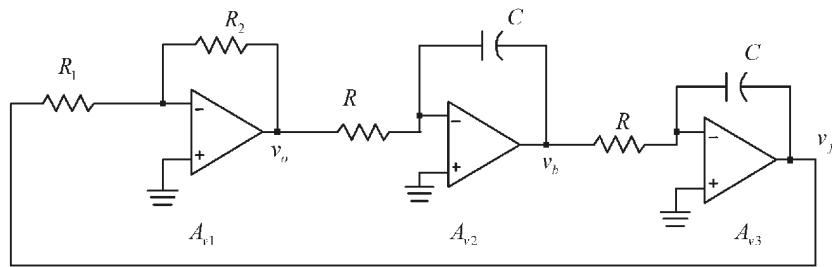


Figure 1.36 A simple active-filter oscillator.

$$A_{v1} = \frac{v_o}{v_f} = -\frac{R_2}{R_1}$$

$$A_{v2} = \frac{v_b}{v_o} = -\frac{1}{j\omega RC}$$

and

$$A_{v3} = \frac{v_f}{v_b} = -\frac{1}{j\omega RC}$$

Therefore, the loop gain is

$$\beta A_{v1} A_{v2} A_{v3} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{\omega RC}\right)^2$$

and the condition for oscillation (i.e., loop gain equal to one) is satisfied at

$$\omega_o = \frac{1}{RC} \sqrt{\frac{R_2}{R_1}}$$

Next we consider the use of bandpass filters in the implementation of oscillators. Figure 1.37 illustrates an oscillator that uses a bandpass filter in the feedback loop. The voltage transfer function for this filter is

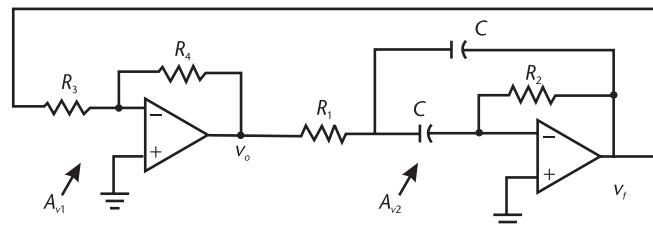


Figure 1.37 An oscillator using a bandpass filter.

$$A_{v2} = \frac{v_f}{v_o} = \frac{-\left(\frac{1}{R_1 C}\right)s}{s^2 + \frac{2}{R_2 C}s + \frac{1}{R_1 R_2 C^2}} = \frac{-2Q\omega_o s}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}$$

where

$$Q = \frac{1}{2} \sqrt{\frac{R_2}{R_1}}$$

and

$$\omega_o = \frac{1}{C \sqrt{R_1 R_2}} \quad (1.53)$$

The loop gain is

$$\beta A_{v1} A_{v2} = \left(\frac{R_4}{R_3}\right) \frac{2Q\omega_o \omega}{\omega \left(\frac{\omega_o}{Q}\right) + j(\omega^2 - \omega_o^2)}$$

which shows that the frequency of oscillation is given by (1.53), and the gain condition is

$$\frac{R_4}{R_3} 2Q^2 = 1 \Rightarrow \frac{R_4}{R_3} = 2 \frac{R_1}{R_2}$$

An oscillator configuration that uses a Twin-T filter in the feedback path is shown in Figure 1.38. The Twin-T filter consists of two Tee-shaped networks

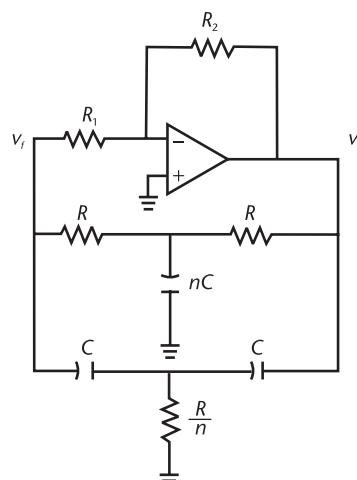


Figure 1.38 An oscillator using a Twin-T filter.

connected in parallel. These Twin-T filters are also known as band-reject filters or notch filters. In the Twin-T filter shown in Figure 1.38, the elements connected to ground have values of nC and R/n , respectively.

The transfer function of the Twin-T filter in Figure 1.38 is

$$\beta(s) = \frac{v_f}{v_o} = \frac{s^2 + \left(\frac{2}{n} - 1\right)\omega_o^2}{s^2 + \omega_o\left(n + \frac{2}{n} + 1\right)s + \omega_o^2} \quad (1.54)$$

where

$$\omega_o = \frac{1}{RC} \quad (1.55)$$

and n is a number such that $n \geq 2$.

Observe that if $n = 2$, (1.54) reduces to

$$\beta(s) = \frac{s^2 + \omega_o^2}{s^2 + 4\omega_o s + \omega_o^2} \quad (1.56)$$

which is the transfer function of a Twin-T filter commonly used as notch filter. Of course, the transfer function in (1.56) has a zero at ω_o , which is responsible for the “deep” notch of this filter.

The gain of the op amp is $A_{vo} = -R_2/R_1$. Setting the loop gain of the oscillator equal to 1 gives

$$-A_{vo} \frac{s^2 + \left(\frac{2}{n} - 1\right)\omega_o s + \omega_o^2}{s^2 + \omega_o\left(n + \frac{2}{n} + 1\right)s + \omega_o^2} = 1$$

or

$$(1 - A_{vo})s^2 + \left[n + \frac{2}{n} + 1 - A_{vo}\left(\frac{2}{n} - 1\right)\right]\omega_o s + (1 - A_{vo})\omega_o^2 = 0$$

Therefore, the required gain is

$$A_{vo} = -\frac{n + \frac{2}{n} + 1}{1 - \frac{2}{n}} \quad (1.57)$$

and the frequency of oscillation is given by (1.55). Equation (1.57) shows that an oscillator designed with $n = 2$ in the Twin-T filter requires an infinite gain. Hence, for oscillator purposes $n \geq 2.5$ is more practical.

Example 1.10

Design the Twin-T filter in Figure 1.38 to oscillate at $\omega_o = 1 \text{ krad/s}$ (or $f_o = 159 \text{ Hz}$) with $n = 4$.

Solution

Letting $R = 10\Omega$, it follows from (1.55) that $C = 0.1 \mu\text{F}$. From (1.57), the value of A_{vo} with $n = 4$ is $A_{vo} = -11$. To start the oscillation we let $R_2/R_1 > 11$, or $R_1 = 50 \text{ k}\Omega$ and $R_2 = 660 \text{ k}\Omega$. The op amp supply voltages are $\pm 15\text{V}$.

The simulation of the oscillator is shown in Figure 1.39. The resulting oscillation is at 161.9 Hz. The notch associated with the Twin-T filter (high Q) makes the resulting oscillation fairly clean of harmonics.

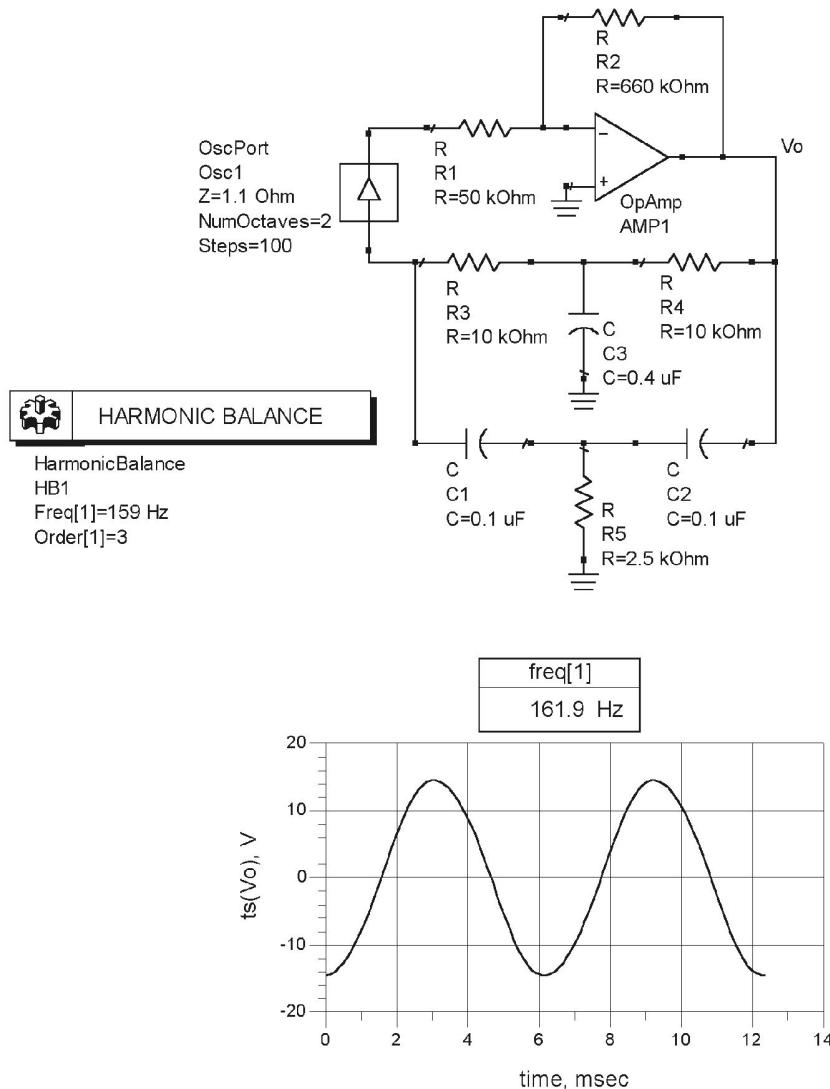


Figure 1.39 ADS simulation for the Twin-T oscillator in Example 1.10.

References

- [1] Lindberg, E., "Oscillators—An Approach for a Better Understanding," *Proceedings of the 2003 European Conference on Circuit Theory and Design*, Krakow, Poland, 2003.
- [2] Lindquist, C. S., *Active Network Design with Signal Filtering Applications*, Santa Cruz, CA: Steward & Sons, 1977.

PICmicro™ Microcontroller Oscillator Design Guide

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Designing a clock oscillator without some knowledge of the fundamental principals of acoustic resonators is possible but fraught with the uncertainty of "cut and try" methods. While the oscillator may be made to run with the chosen resonator, it is quite likely that the unit will be slightly off the intended frequency, be grossly off frequency because it is operating on an unintended mode, or have unacceptable temperature characteristics because the wrong resonator was chosen for the application.

This application note is primarily for informational purposes. It is intended to help the designer of clock oscillators understand the parameters of crystal resonators and the terminology of the crystal resonator industry, both of which tend to be somewhat mysterious and arcane to the uninitiated. Details of crystal cuts and rotations, for instance, are of no use to the oscillator designer, only the designer of crystals. The oscillator designer still needs to understand and be able to predict the performance and trade-offs associated with these parameters. This is not an in-depth or rigorous treatment of acoustic resonators, but a practical guide, which should allow the designer to gain a basic understanding, and to help in choosing and specifying resonators.

INTRODUCTION

The main purpose of the oscillator in PICmicro microcontrollers, or almost any other microcontroller, is to provide a reliable clock for the controller processes. At the most basic level, the clock provides a timing interval to account for circuit rise times and to allow data to stabilize before that data is processed. This is a "synchronous" process. The clock also provides an opportunity for the programmer to perform time keeping of several types. In the PICmicro, the clock also drives hardware dedicated to timekeeping. The applications may include keeping "real time", or timing sensitive processes such as serial data communication. The accuracy of these timing applications is dependent upon the accuracy of the clock oscillator.

Design Challenges

The PICmicro microcontrollers offer unique design challenges because they are uniquely flexible. Flexibility usually demands difficult decisions on the part of the designer, but offers otherwise unattainable performance. The multiple oscillator options and wide range of operating voltages require awareness of advantages and trade-offs of various configurations. The PICmicro designer must be able to accurately predict stability performance of various configuration and then obtain that performance from the PICmicro clock in order to successfully implement these functions.

Wide Voltage Range

The PICmicro operates over such a wide voltage range that the oscillator parameters may be the limiting factor in the operation of the controller. If low power operation at low voltages is desired, the loop gain must be raised in order to insure reliable clock operation. If a nominal supply voltage is available, the loop gain must be reduced in order to prevent excessive power dissipation in the crystal. If battery operation is intended, then a careful balance must be struck between reliable operation at the low voltage, and damaging delicate resonators, or spurious oscillations at the high voltage when the battery is fresh.

Low Power

The outstanding performance of the Low Power option places a burden on the designer who would take advantage of this feature. The frequency chosen must be the lowest practical. Attention must be paid to the reactances associated with the crystal so as not to excessively load the oscillator output and cause excessive power consumption.

Low Cost

The low cost of the PICmicro series presents a challenge in finding commensurately low-cost components to complete the design. The relationship between cost and performance when various types of resonators are considered, is far from linear. The low cost of PICmicro microcontrollers, may remove them from the position of being the cost driver in some designs, challenging the designer to aggressively seek cost reductions in components which were previously not considered. The second challenge offered by such economical parts is that of new applications which were not considered practical before the advent of PICmicro processors.

THEORY OF OSCILLATORS

Conditions necessary for oscillation

An oscillator is a device which operates in a closed loop. This condition can be difficult to analyze, but the techniques for analysis are as valid for motor speed controls as it is for phase lock loops and oscillators. Oscillators are somewhat unique in that they are intentionally unstable, but in a controlled manner. In order for oscillation to occur in any feedback system, two primary requirements must be met. The total phase shift must be zero or 360° at the desired frequency and the system gain must be unity or greater at that frequency.

The Ideal Oscillator

The ideal oscillator has a perfectly flat temperature coefficient, is 100% power efficient, has no limits on operating frequency, has no spurious modes, has a perfect output wave shape, and is available in the high degrees of miniaturization which exists in semiconductors. This oscillator of course, does not exist. The primary limiting factor for most oscillator parameters is the resonator. The following is a discussion of the trade-off, potential advantages and primary disadvantages of several popular types of resonators, and how they will behave in a PICmicro oscillator design.

RESONATOR BASICS

There are several types of resonators available to the designer of microprocessor clocks. They all provide trade-offs between performance, size, frequency range and cost. Resonators for clock oscillators usually fall into two basic groups. These are quartz and ceramic resonators. Historically, ceramic resonators came into use in oscillators much later than quartz crystals and derive all of their terminology and conventions from the longer history of quartz crystals. A third type of clock oscillator is the RC (resistor / capacitor). This oscillator is a relaxation type, and employs no resonator as such. While this type requires the same basic conditions for oscillation to occur it is better described using different techniques and analogies.

Quartz Resonators

Quartz is the crystalline form of silicon dioxide. This same material, in amorphous form, is commonly found as beach sand and window glass. As a crystal, it exhibits piezoelectric effects as well as desirable mechanical characteristics. A quartz crystal resonator is an acoustical device which operates into the hundreds of MHz. Its resonance and high Q are mechanical in nature, and its piezoelectric effects create an alternating electrical potential which mirrors that of the mechanical vibration. Although it is one of the most common of naturally occurring crystals, natural quartz of sufficient size and purity to be used in the manufacturing suitable resonators, is unusual and expensive. Almost all modern resonators are manufactured using cultured quartz, grown in large autoclaves at high temperatures and pressures.

Whether naturally occurring or cultured, quartz crystals occur as six-sided prisms with pyramids at each end. This raw crystal is called a "boule". In an arbitrary coordinate system the Z, or optical axis, runs the length of the crystal, connecting the points of the pyramids at each end. If one views this hexagonal bar on end, three lines may be drawn between each of the six opposing corners. These are called X axes. Perpendicular to each X axis is a Y axis, which connects opposite pairs of faces. When the boule is cut into thin plates or bars called blanks, the cut of the saw is carefully oriented either along, or rotated relative to one of these axes. Orientation of the saw is chosen based on the mode of vibration for which the plate is intended, and the desired temperature profile. Plates are usually rounded into discs. Types of crystal cuts are named for the axis which the cutting angle is referenced when the blanks are cut from the boule. After being cut and rounded, the blanks are lapped to frequency and any surface finishing or polishing is done at this time. Electrodes are deposited on the blanks by evaporation plating, and the blank is mounted in the lower half of the holder. It is finished to the final frequency by fine adjustments in the mass of the electrode plating, either by evaporation or electroplating. The top cover is then hermetically sealed by one of several methods, which include cold welding and solder sealing.

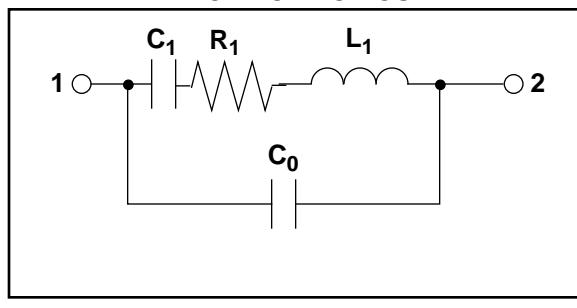
Most crystals made today are A-T cut, which employ a thickness mode. This mode provides the highest frequency for a given thickness of the plate, and the best possible frequency stability over most temperature ranges. Many other modes of vibration are possible. Flexure modes are usually bar shaped, and are used for low frequency (near 100 kHz) resonators. Tuning fork crystals are a special case of this type.

Ceramic Resonators

Unlike quartz resonators, which are cut from a single crystal, a ceramic resonator is molded to a desired shape instead of grown. The material is polycrystalline form of barium titanate, or some similar material. The electrical model is almost identical, with the addition of one resistor, as the material is intrinsically conductive. The material is artificially made to exhibit piezoelectrically active by allowing it to cool very slowly, as in growing a quartz crystal (not nearly as long a time), but in the presence of a strong electric field. The molecular electric dipoles align themselves with the applied electric field. When the material has cooled, the alignment of the electric dipoles is retained, which is equivalent to piezoelectricity.

These materials have elastic properties that are not as desirable as quartz, and so their performance is not equal to that of quartz resonators. Specifically, ceramic resonators have far lower Qs and frequency deviations due to temperature on the order of 1000 to 10000 times greater than that of an A-T cut quartz crystal. The cost of ceramic resonators is much lower however, because the material is not grown under the extreme and expensive conditions that are necessary for quartz. They are also much smaller than A-T cut quartz resonators, particularly at frequencies under 2 MHz.

FIGURE 6: RESONATOR EQUIVALENT ELECTRICAL CIRCUIT



Since the "Q" of ceramic resonators is generally lower than quartz, they are more easily pulled off frequency by variations in circuit or parasitic reactances. This is desirable if a circuit is designed with a variable element, as greater tuning range is realized. It is not desirable if the highest possible stability is the design goal, because the resonator will be more susceptible to variation in parasitic reactances, such as capacitors formed by circuit board etch, and temperature variations of intended circuit reactances. These variances will add to the already substantial deviation over temperature of the resonator itself. If your stability needs are modest however, ceramic resonators do provide a good cost / performance trade-off.

Equivalent electrical circuit

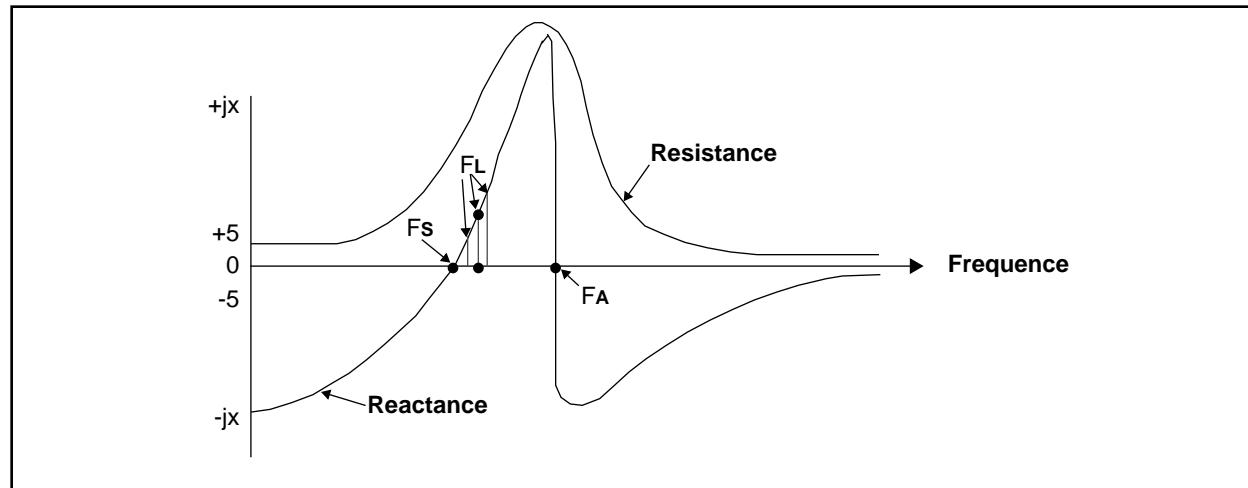
The circuit shown in Figure 6 is a close approximation of a quartz or ceramic resonator. It is valid for frequencies of interest to the PICmicro designer. Not all of the parasitic elements are shown as they are not important to this discussion. In this circuit, L_1 and C_1 are the reactances which primarily determine the resonator frequency, while a series resistor represents circuit losses. A shunt capacitor, C_0 , represents the holder and electrode capacitance.

Because L_1 and C_1 are associated with mechanical vibration of the crystal, these are commonly referred to as motional parameters, while C_0 is called the static capacitance. The reactance of L_1 and C_1 are equal and opposite at the series resonant frequency, and their magnitude is very large as compared to R_1 . The phase shift at the series resonant frequency is zero, because the reactances cancel. The series resonant frequency is calculated as shown in Equation 1.

EQUATION 1: SERIES RESONANT FREQUENCY

$$F_s = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

FIGURE 7: REACTIVE vs. FREQUENCY PLOT



The actual series resonant frequency as determined by the zero phase point is slightly lower than this calculation because of the effects of C_0 , and for practical purposes can be considered identical. This fact may be useful to those designing tunable crystal oscillators. These resonator parameters are generally considered to be constant in the region of the main resonance, with the exception of R_1 . A plot of reactance over frequency is shown in Figure 7. The point labeled F_S is the series frequency, while F_L is the frequency where the crystal is resonant with an external load capacitor. Operation at this point is sometimes called parallel resonance. F_A is the frequency where the crystal is anti-resonant with its own electrode capacitance. Only the region below F_A is useful as an oscillator. Notice that the resistive component begins to rise, before F_S and continues steeply above F_S . This makes operation with small load capacitors (large reactances) difficult. One must be sure that if the resonator is specified to operate at a load capacity that the maximum value of R_1 is specified at that operating point. The zero phase shift point is the most common method of identifying the exact series resonant frequency. When the series frequency is known, operation at a load reactance is easily calculated as follows:

EQUATION 2: OPERATION AT A LOAD REACTANCE

$$\frac{\Delta F}{F_S} = \frac{C_1}{2(C_0 + C_L)}$$

where ΔF is the deviation from F_S to F_L , F_L is the operating frequency when in series with a load capacitor, F_S is the series resonant frequency (without any load capacitor), and C_L is the load capacitor.

The value of R_1 at the frequency F_L can be approximated by:

EQUATION 3: VALUE OF R_1 AT THE FREQUENCY F_L

$$R_1 = R_L \left(\frac{C_L}{C_0 + C_L} \right)^2$$

The reactance slope in the region of the series resonance can be approximated by:

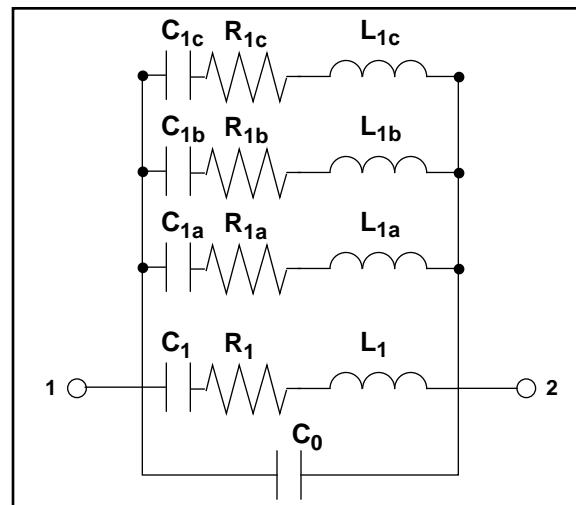
EQUATION 4: REACTANCE SLOPE IN REGION OF SERIES RESONANCE

$$\frac{\Delta X}{\left(\frac{\Delta F}{F} \right)} \approx \frac{10^6}{\pi F C_1}$$

where ΔX is the reactance difference, in Ω , from series, at which of course the reactance is zero. $\Delta F/F$ is the fractional frequency deviation from series resonance. F is the frequency of interest in MHz, and C_1 is the crystal static capacitance of Figure 6. This is only accurate in the region of series resonance and the accuracy declines as frequencies further away from series are considered. This parameter is useful in determining the optimum C_1 , which the designer might specify in order to have the correct tuning sensitivity for any frequency adjustments, or given a crystal C_1 , what tuning sensitivity will result from various reactive components.

The ratio of the reactance of L_1 or C_1 to R_1 is arbitrarily designated as Q . This is also known as quality factor, and applies to any reactive component. The series resonant frequency of the crystal is the sum of the total series reactances. Quartz A-T cut crystals exhibit spurious modes which are always found at frequencies just above the main response. These are always present and are not associated with activity dips. There are also odd ordered mechanical overtone modes. Any of these modes (spurious or overtone) can be modeled as duplicates of the primary RLC electrical model, and placed in parallel with it (Figure 8). Notice however, that there is only one C_0 . Near the resonance of each series circuit, the effects of the other resonances may be considered negligible. Each resonance of course, has its own motional properties, the one of primary interest here is the R_1 of each resonance. The R_1 usually increases with increasing overtones, making higher overtones more lossy. The PICmicro designer must take care to specify the crystal spurious to always be of higher resistance than the desired response. This can be achieved in a well designed resonator. A heavy metal such as gold, as an electrode, will discourage higher overtones, by virtue of its higher mass. Crystals designed for high frequencies, almost always use a lighter material, such as aluminum. Electrode size also plays an important role.

FIGURE 8: EQUIVALENT CIRCUIT FOR SPURIOUS AND OVERTONE MODES



OSCILLATORS

Phase and Gain

As stated earlier, two conditions must be met for oscillation to occur. The phase shift must be zero or 360° at the desired frequency, and the total system gain must be one greater or at that frequency. Logic gates or inverters are convenient for this purpose. They have large amounts of gain, limit cleanly, produce square waves, and their output is appropriate for directly driving their respective logic families. Most oscillators in this family use an inverting amplifier, as shown in Figure 13. The phase shift is 180° through the gate, and the two reactances at either end of the crystal are chosen to provide an additional 90° each, bringing the total to the required 360° . The primary effect of changes in phase is to shift the operating frequency (to tune the crystal). The primary effect of changes in gain is to cause the oscillator to cease functioning when reduced, or cause spurious modes and excess power to be dissipated in the crystal when increased.

Oscillation will occur at the frequency for which the total phase shift is 360° . This is true for any frequency (or resonator response) for which the gain is greater than unity (including unwanted responses). The series resistor (R_S) is used to adjust the loop gain, and to provide some isolation from reactive loads for the amplifier. The lower limit of loop gain is determined primarily by the need for sufficient excess gain to account for all variations, such as those caused by temperature and voltage (not just in the amplifier, the crystal resistance may change as a function of temperature). The upper limit of loop gain should be that where it becomes possible (or at least likely) for the oscillator to operate on a spurious mode. In some resonators damage to the resonator is the overriding concern regarding drive level. If the stability requirement is rather "loose" the stability problems may not be the first indications of trouble. Excessive drive levels in tuning fork types for instance, may cause damage to the point that the crystal unit fails. It is important to estimate drive levels before operation begins, include and adjust a series resistance appropriately, and by measurement, verify the results.

Estimating Drive Levels

The drive levels may be estimated with the following steps. First find load impedance presented by crystal network, including phase shift capacitors and amplifier input impedance. This is found by the following:

EQUATION 5: LOAD IMPEDANCE

$$R_n \equiv \frac{X_c^2}{R_S + R_{OSC1}}$$

where R_N is the network impedance. X_C is the reactance of one phase shift capacitor (assuming they are the same). R_{OSC1} is the input impedance of the OSC1 pin (should include reactance). R_S is reactance + resistance at operating frequency ($R_S + X_S$).

The current delivered into this impedance is found by:

EQUATION 6: CURRENT DELIVERED

$$I_n \equiv \frac{V_{OUT}}{R_S + R_N}$$

where I_n is the RMS current drawn by the network. V_{OUT} is the OSC2 output RMS voltage. R_N is calculated above. R_S is described above. The current which passes through the crystal then is found by:

EQUATION 7: CURRENT THROUGH CRYSTAL

$$I_S \equiv \frac{V_C}{R_S + R_{OSC1}}$$

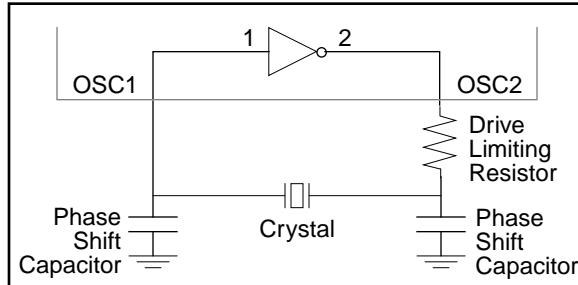
The power dissipated by the crystal is then found by I_S squared times the crystal R_1 .

Controlling Drive Levels

When designing any oscillator, one should take care not to lower the loaded Q of the resonator by inserting any resistive components between the phase shift capacitors (or any other reactive components) and the crystal. If it is necessary to reduce the drive level to the crystal, or lower overall loop gain, resistance should be inserted between the amplifier output, and the crystal (Figure 9). This method is much better than changing load reactances, which will have no significant effect on gain until the frequency has been pulled well away from the design center. This will also have the more significant effect of raising operating current, because if no series resistor is present, larger reactance of the phase shift capacitor will load the OSC2 output directly. If a very low drive level is required, such as with tuning fork type crystals, the series resistor is the best method. The resistor should be adjusted until the unit just runs with a typical crystal at the lowest operating voltage, and resulting drive measured at the highest operating voltage. The actual resistor value is best determined experimentally with a representative sample of crystals, and a broad range of values should be satisfactory. In general, the point where oscillation stops for any crystal unit (within specified parameters), is the resistor's upper limit. The lower limit may be 0Ω , for a less fragile crystal type, depending on the operating frequency. If no spurious or overtone modes are encountered, it is likely that the oscillator may have relatively little excess

gain at that operating frequency. If resulting drive level at higher voltage is still unacceptable, then supply voltage variations must be reduced.

FIGURE 9: PICMICRO OSCILLATOR CIRCUIT



Measuring Drive Levels

Drive levels cannot be easily measured with any certainty by reading voltages at each end of the crystal. This is because of the phase shift which is present in varying degrees, depending on how close to series resonance of the crystal, the oscillator is operating. It is much more reliable and accurate to measure the crystal current with a clip-on type oscilloscope current probe. This probe may require an outboard amplifier in order to measure very low drive levels. It is also important to accurately know the series resistance of the crystal under the same operating conditions of frequency and drive level. This information is easily obtained with a network analyzer or a modern crystal impedance meter. While the oscillator designer may not be equipped with such a meter, the manufacturer of the crystal most certainly should be, and resistance data should be provided for at least one, and perhaps several possible drive levels, if variations in drive are expected.

UNDESIRED MODES

Mechanical resonators are not perfect devices. They exhibit many spurious responses, either continuously or over narrow temperature ranges. If a quartz resonator is swept with a R.F. network analyzer, several smaller responses will be seen just above the main response. These are always present in mechanical plate resonators. For oscillator applications, they must be specified to have a lower response than desired mode. The crystal designer can control these to some extent by varying plate geometry and electrode size. These spurious modes are usually similar in nature to the main response, and do not vary in relation to it to any important degree. Other spurious are caused by completely different modes of vibration, and have radically different temperature curves. These may lay unnoticed until a temperature is reached where the two temperature curves intersect. At this one temperature, the spurious mode traps some of the mechanical energy created by the main mode. This causes a rise in the series resistance, usually accompanied by an unacceptable change in frequency. With a very small change

in temperature, the effect will disappear. This is known as an "activity dip", activity being a dimensionless mechanical property which is inversely proportional to resistance. These can also be successfully specified away in most resonators. Any response of the resonator, be it from spurious, or mechanical overtones, may control the oscillator output frequency if phase and gain criteria are met. In some unusual circumstances, the oscillator may run simultaneously on two or more modes. In general, the fundamental response of any mechanical resonator is usually the largest (lowest loss), and the oscillator will run on this response if no other circuit elements are introduced which favor higher frequencies. If the desired frequency is such that the third overtone, begin the first available (mechanical overtones are always odd ordered), is below 15 or 20 MHz, the oscillator may occasionally run at around three times the desired frequency. This may only happen every third or fifth time the unit is activated. The unit may start correctly, but jump to higher overtone when the unit is exposed to a very narrow temperature range, but remain there after the temperature has changed. The best fix for this problem is usually a reduction in overall loop gain. Occasionally a crystal may have a very low resistance at overtone modes as well as the fundamental. In this case it may be useful to specify overtone modes, as spurious and guarantee at least a -3dB difference between the overtone and the fundamental responses. This condition will already exist for 99% of the resonator designs, and is not usually specified.

It is also best not to insert any large reactances which would compete with the Q of the crystal for control of the oscillator output frequency. If this is done (say, for the purpose of adjusting the oscillator frequency), the tuning reactance (usually a variable capacitor) must be accompanied by an equal reactance of the opposite sign in order to bring the total loop reactance back to zero (unless the crystal is designed to operate with that large series reactance, which could cause other problems). If the oscillator is pulled far enough from the series frequency, the rising crystal resistance will lower the loaded Q of the crystal until the reactance slope of these components competes with that of the crystal. This will cause the oscillator to "run" on these components instead of the crystal, the loop being completed by the C_0 of the crystal. The component with the steepest reactance slope will control the frequency of the oscillator. The tuning sensitivity of these components will also be directly proportional to the magnitude of their reactances. Any unwanted variation of these components will have increased consequences for the stability of the oscillator. Another source of spurious is a relaxation mode which is caused by the amplifier bias circuits and the phase shift capacitors. The loop is completed through the crystal C_0 . Again, a series resistor will usually solve this problem, although in some cases the amplifier bias values may need to be changed.

Load Capacitors

In gate or logic type oscillators, the crystal is usually manufactured to be slightly inductive at the desired frequency, and this inductance is canceled by the two phase shift capacitors. The primary purpose of these capacitors is to provide the phase shift necessary for the oscillator to run. Their actual value is relatively unimportant except, as a load to the crystal, and as they load the output when no series resistor is used. These reactances are the sum total of selected fixed capacitors, any trimmer capacitors which may be desired, and circuit strays. If a loop is considered from one crystal terminal through one phase shift capacitor through ground and the second phase shift capacitor, to the second crystal terminal, all the reactances including the crystal motional parameters must add up to zero, at the desired operating frequency.

As a crystal load, all circuit reactances external to the crystal should be thought of as a series equivalent. In order to know the total load reactance seen by the crystal, the total shunt reactances on either terminal are summed, and the series equivalent is calculated. This should include the OSC1 and OSC2 terminal reactances, but these are negligible if they are sufficiently small when compared to the phase shift capacitors. The value of these capacitors, is then chosen to be twice the specified load capacity of the crystal. If some adjustment of the frequency is necessary, one of the phase shift capacitors can be chosen at a smaller value, and the difference made up by a variable capacitor placed across it. An alternative method is to place a larger value trimmer capacitor in series with the crystal. The value of the trimmer capacitor must be chosen along with the phase shift capacitors, all in series, to give the correct load capacity. Frequency should not be adjusted by shunting the crystal with a capacitor. If it is desired to use a crystal which is finished at series resonance, an inductor of equivalent reactance to half of the phase shift capacitor, must be placed in series with the crystal.

STABILITY

General

Frequency stability is the tendency of the oscillator to remain at the desired operating frequency. Its deviation from that frequency is most conveniently expressed as a dimensionless fraction, either in parts per million (PPM) or a percentage. Absolute deviations in Hz must always be referenced to the operating frequency, which is less convenient and not universal. In the following discussion of temperature characteristics, one can see that the fractional deviations are universal without any direct effect of operating frequency. In order to calculate a total frequency stability, various separate elements must be identified and quantified. Not all parameters of frequency stability are important to each design. The various items which effect the frequency of an oscillator are: the temperature profile of the resonator, the reso-

nator's room temperature frequency tolerance (also known as "make tolerance"), its long term frequency drift which is normally known as ageing, and its sensitivity to other circuit reactances. Is it possible to adjust it to the exact desired frequency? If not, how big is the error due to other component tolerances. Due to the complexity of this combination, most crystal manufacturers will offer a standard crystal which is guaranteed to be ± 100 PPM over -20°C to $+70^\circ\text{C}$, or ± 30 PPM over -0°C to $+60^\circ\text{C}$. Note that the temperature coefficients of some of the curves in Figure 7 are much smaller than this over the same temperature range. Large portions of these tolerances are devoted to make tolerances and circuit component tolerances. The room temperature items can be relatively simple to specify in the resonator design. If careful attention is paid to specifying the crystal, or designing the oscillator to accommodate a standard crystal, more of the total stability requirement can be devoted to the temperature profile, or the overall stability requirement can be reduced. The temperature profile, however, is subject to other circuit influences external to the resonator. These may be somewhat more difficult to perceive and control. If, for example, the chosen resonator is an A-T cut or tuning fork type, possessed of a nominal temperature profile of less than 50 PPM over the desired temperature range, external influences, such as capacitor temperature coefficients, may play an important part in the overall stability of the oscillator. If however, a ceramic resonator is chosen, its temperature profile of 40 to 80 PPM/C will dominate the oscillator stability, and 5 or 10 PPM shift from changes in amplifier impedance or capacitor temperature coefficients will not be important. The designer may choose a crystal even when the overall stability specification (of the oscillator) does not require it, giving large design margins. If any amount of testing or adjustment of the oscillator frequency is needed with the lower cost resonator, the crystal may be more cost effective. When designing any resonator as part of a simple logic type oscillator circuit (Figure 9), some attention should be given to swapping the amplifier reactances (that is to make them a very small part of the sum total circuit reactance) with the phase shift capacitors, and any other circuit reactances. This is at least, a good design practice. The largest reactance has the most effect on the operating frequency. It follows then that the motional parameters, which have very large reactances, dominate the equation for the total reactance, and so the operating frequency of the oscillator.

Another good design practice, is to specify only as much pullability as is required to accommodate the make tolerance and ageing of the resonator, and tolerance of other circuit elements. Pullability is a function of the ratio of C_1 to C_0 . As the reactance of the crystal C_1 increases it becomes more stable in relation to outside reactive influences. It also becomes more difficult to intentionally adjust its operating frequency. If too high a C_1 is specified, the resonator will be sensitive to external influences, and the effect of these influences may be as large or larger than the temperature profile. If the

C_1 is to small, it may not be possible to adjust the unit exactly to the desired operating frequency. The small electrode size needed to realize a low C_1 may also concentrate the mechanical energy in a very small percentage of the blank, causing unpredictable behavior. In order to quantify pullability in terms of C_1 to C_0 ratio and load capacitance (refer to the Equivalent Electrical Circuit section).

A-T Cuts

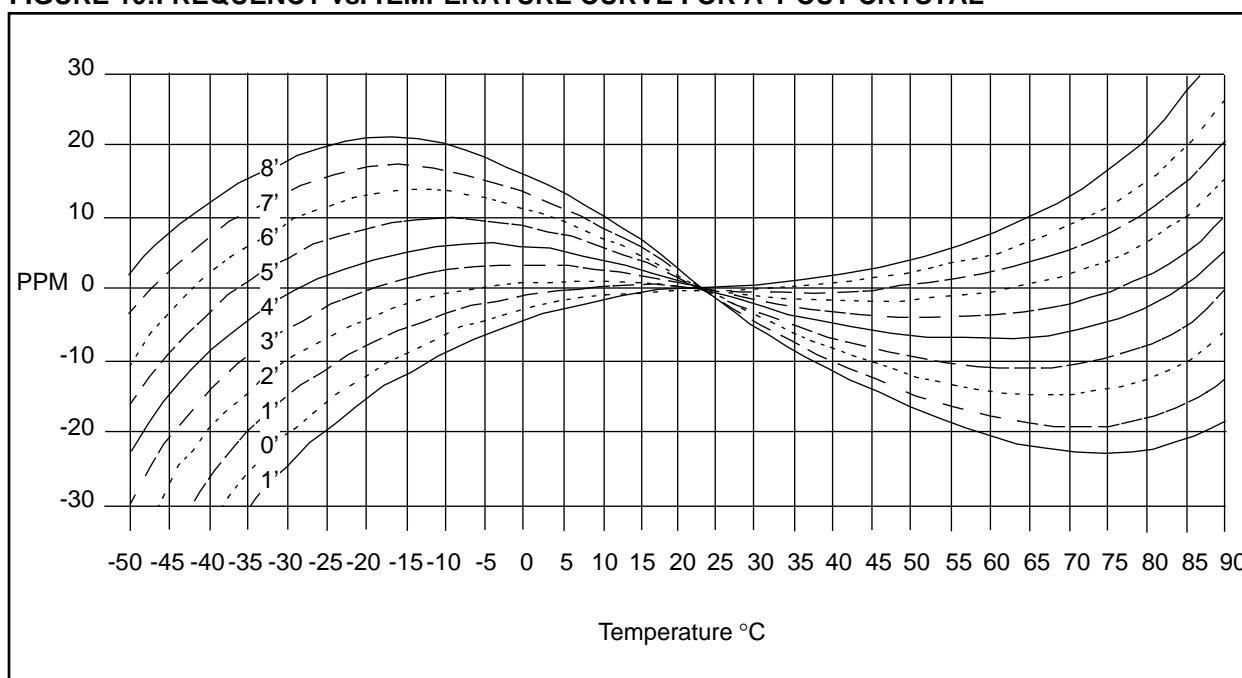
The A-T cut crystal and its variations, is by far the most popular resonator in the world today. A-T cut crystals are popular because the "S" shaped temperature curve is centered very near room temperature, typically around 27°C. This temperature profile is compact, symmetrical, and most manufacturers are able to provide good control of the cut angle.

Because most of the crystals manufactured in the last 40 years have been A-T cuts, they are very well understood and documented. This is important because while temperature coefficients can be calculated from the mechanical properties, such as elastic constants, they can (and have been) measured with much more accuracy. When the temperature coefficients are accurately known, the temperature profile can be calculated for an individual set of conditions. Figure 10 is a family of temperature curves of A-T cut crystals used for this purpose. Each curve represents a possible crystal at incremental changes in the cut angle. The practical limit for accuracy of the cut is about ± 1 minute of angle, and in any lot of crystals there will be variations of about ± 1 minute. The designer will create a box around these curves using the desired temperature limits as the vertical sides, and the desired frequency tolerance for the horizontal lines,

as shown in Figure 10. If the curves are spaced at intervals of one minute of angle, then the specification is a practical one if three of these curves (± 1 minute) fit within the outlined area. It is possible to purchase crystals with a closer tolerance, but this is mostly a matter of yields, rather than a better process. The steeply increasing cost will reflect the higher reject rate.

When purchasing a crystal, do not attempt to specify a specific angle, rather specify a frequency deviation between turning points, with tolerances. The mathematics of these curves, is represented by a linear term between two turnover points, whose inflection point is at or near 27°C. The temperature above the high turnover and below the lower turnover, are characterized by cubed terms (very steep). This was described by Bechman in the late 1950s as a third order polynomial. This can be seen in Appendix A. Notice that as the linear portion of the curves between turnover points approaches zero slope, the turnover points move closer together. This tends to limit the temperature range over which very small stabilities can be realized. If the required operating temperature range is inside of the range of the turnover points, a low angle is desirable. If so specified, most manufacturers will provide a crystal with temperature profiles on the order of ± 5 to ± 10 PPM over modest temperature ranges for a reasonable cost. If the desired operating temperature range is outside of the range of turnover points, a higher angle is desirable in order to keep the frequency at extreme temperatures within the same realm as deviation between turnover points. This may approach ± 60 PPM for large temperature ranges, but is still far less than the smallest deviations achievable with other resonators over the same temperature range.

FIGURE 10:FREQUENCY vs. TEMPERATURE CURVE FOR A-T CUT CRYSTAL



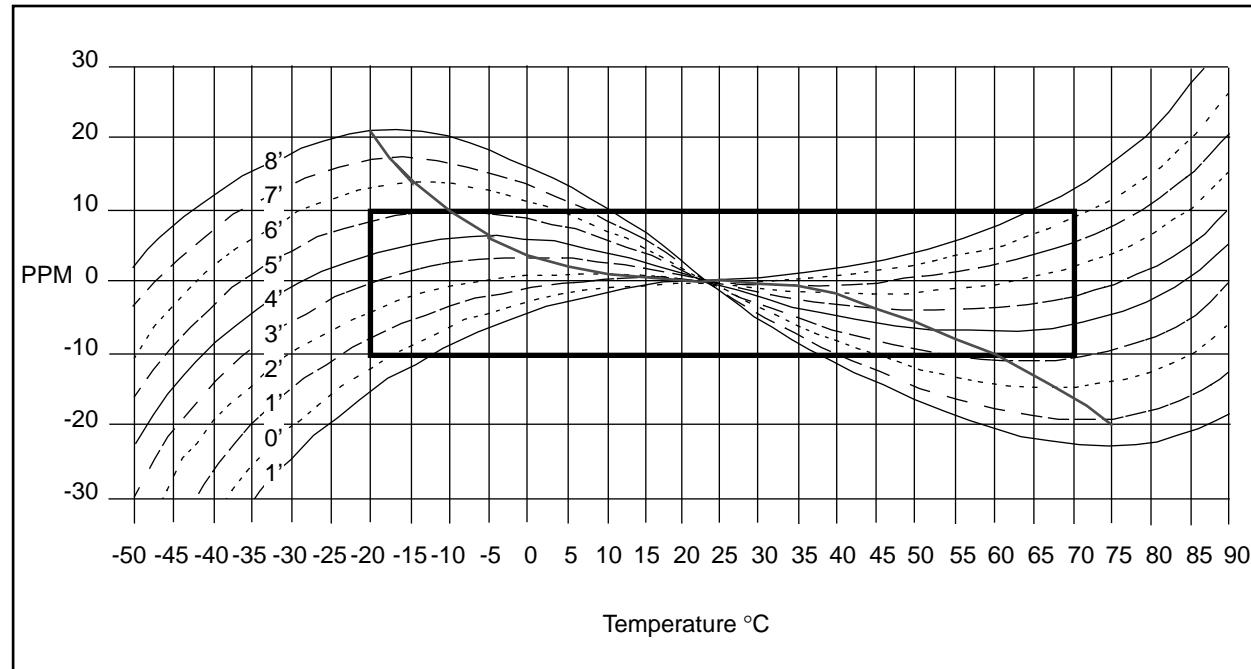
What is not immediately obvious is that if a linear frequency shift with temperature is applied to a frequency curve the result is a rotation of the curve which will eventually match another member of the curve family. There is no other distortion of the temperature curve if the frequency shift is linear, such as from a temperature compensating capacitor. This fact also gives a convenient graphical technique to estimate the effect of temperature coefficients of other components. There exist several flaws in this picture of the A-T cut temperature profile, which may prevent the PICmicro designer from completely realizing the stability suggested by the curves in Figure 10.

The first problem which may arise when choosing a crystal angle based upon these curves, is that there may occur some rotation of the crystal angle due to external circuit influences. The most common influences are that of reactive components (inductors and capacitors). Most inductors have a slight positive temperature coefficient, while capacitors are available in both positive and negative temperature compensating types. Non-compensating type capacitors vary greatly depending on the dielectric from which they are manufactured. The best capacitors for frequency determining elements, are ceramic types with NPO (flat) temperature coefficients. Avoid at all cost, capacitors made from Z5U material. These have a large temperature coefficient and are unsuitable even for supply line decoupling or D.C. blocking capacitors. This is because a slight change in the R.F. impedance which shunts the Vcc and Vdd pins, will have an effect

on the output impedance of the amplifier, and so an effect on frequency. The effect will be on the order of a few PPM, and may well be of secondary importance, depending on the stability requirement. A word about D.C. voltages and crystals. It is permissible to place a D.C. voltage across the terminals of the crystal. This does cause a small change in frequency, but that change is not significant for stabilities of ± 5 PPM or greater.

The second problem is one of dynamic temperature performance. When the unit has stabilized at any temperature on the curve, the frequency will agree with the curve. While the temperature is slowing however, the frequency may be in error as much as 5 to 15 PPM depending on the temperature change. This effect is caused by mechanical stresses placed on the blank by temperature gradients. These can be minimized by thermally integrating the crystal, and joining it to a larger thermal mass. One oscillator engineer has been known to attach a block of alumina (ceramic) to both of the crystal pins in order to join them thermally. Any other mechanical stresses placed upon the pins or leads of an A-T cut crystal unit will also result in a dramatic frequency shift (if the unit is not damaged first). This is to be avoided.

FIGURE 11:FREQUENCY vs. TEMPERATURE SPECIFICATION FOR A-T CUT CRYSTALS



The third item which will cause a deviation from the curves of Figure 10, is spurious response. This is known in the crystal industry as an activity dip. This name originates from a time when the series resistance was referred to as crystal activity, and the frequency change is accompanied by a marked rise in series resistance. This phenomenon occurs when mechanical energy is coupled from the normal thickness shear mode into another undesired mode of vibration. Several other modes are possible for finite plate resonators, and they will usually resonant at frequencies well away from the design frequency. These modes will often have radically different temperature profiles, and may intersect with the profile of the desired mode at only one very narrow range of temperatures (much less than 1°C). This makes an activity dip difficult to spot in normal testing. Those which are discovered are often around room temperature where temperature changes are more gradual. This coupling between modes is greatly effected by drive level, and the best crystal may exhibit a dip if grossly overdriven. Fortunately, most manufacturers today can produce a crystal which is free of significant dips if so specified. As the accompanying rise in resistance is occasionally large enough to cause oscillation to halt, the PICmicro designer should always specify activity dips to be less than 1 PPM, even if the overall stability requirement is much larger than this. In the interest of low cost and flexibility, the designer may also specify activity dip in terms of a maximum change in resistance.

The other important effect on frequency stability of A-T cut crystals, is ageing. This is the long term frequency shift caused by several mechanisms, the most notable being mass loading of the resonator, causing the frequency to shift ever downward. Because this is the primary mechanism, the cleanliness of the interior of the unit is of prime importance. This is in turn greatly effected by the method used to seal the unit, and the type of holder chosen. If the unit is subjected to excessive drive levels, the frequency may age upwards, indicating electrode material is being etched off of the blank. A good general purpose high frequency crystal using a solder seal holder may be expected to age about 10 to 20 PPM / year maximum. Resistance weld holders will average 5 to 10 PPM / year, and for high stability applications, cold weld crystals are available at ageing rates of 1 to 2 PPM / year. The ageing rates of most crystals will decay exponentially, the most change being in the first year. Ageing rates are different if the unit is operated continuously, but aging will continue even if the unit is not operated.

32 kHz Watch Crystals

The typical 32 kHz watch crystal is a tuning fork type. This is a special case of a flexure mode (N -T cut). The unusual nature of this flexure type is that it is indeed shaped like a tuning fork. This shape gives the crystal a very small size for its low frequency of operation and is almost always manufactured in the NC 38 holder. This is a tube 3 mm x 8 mm. This type is available at frequen-

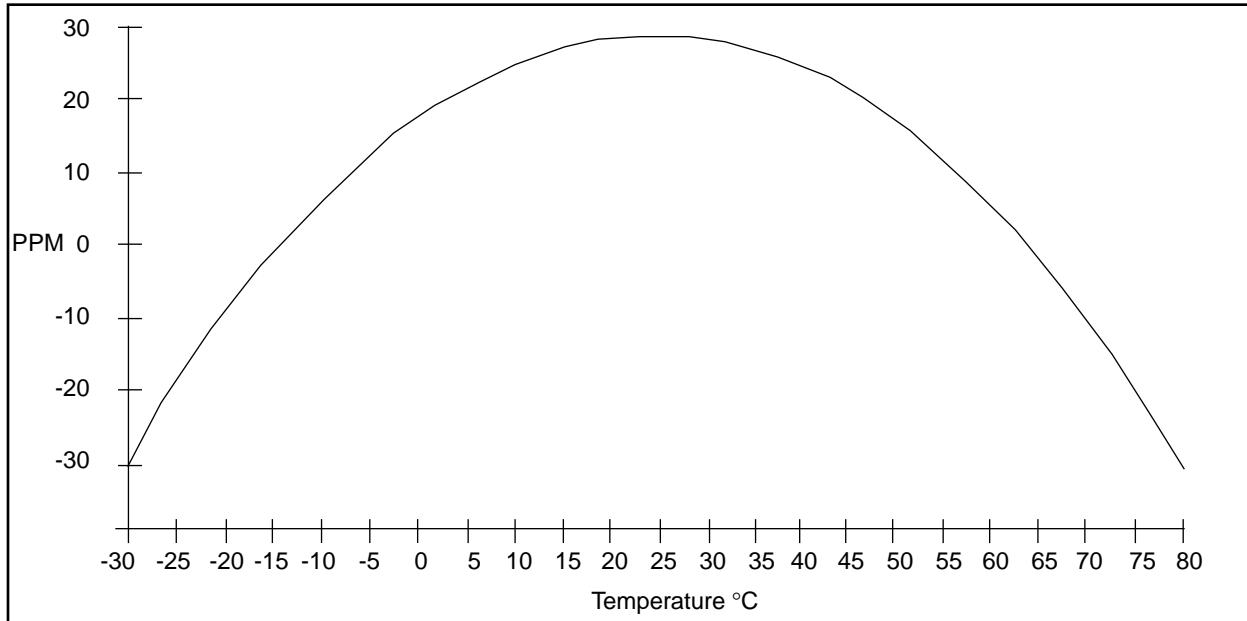
cies from 10 to 200 kHz, although 32.768 kHz is by far the most popular frequency. The frequency is of course 215, which is ideal for time keeping applications, and being so low is ideal for low-power applications. This type is generally less stable than higher frequency A-T types, but is much better than ceramic resonators, the primary attraction being the possibility of very low operating power drains. The PICmicro LP option was designed with this crystal in mind. It has a parabolic temperature profile of about .04 PPM / (°C) 2. The turnover point of the temperature profile is near 25°C. In order to calculate the change in frequency it is only necessary to square the difference in temperature from 25°C and multiply by .04. The temperature profile is shown in Figure 12. The C₁ is on the order of .002 pF, which will make design for frequency adjustment possible but not trivial. The make tolerance is usually about 20 PPM at best, making some adjustment necessary for most applications. The series resistance of this type is very high, on the order of 30,000Ω. It is imperative that care be taken to limit the drive to the crystal. Only a fraction of a mA of crystal current will damage this unit, possibly causing it to cease oscillation. This is best done with a series resistor between the OSC2 pin and the junction of the crystal lead and phase shift capacitor (Figure 12). If the frequency is moving upward in a continuous manner, the drive level is probably too high. A portion of this change will be quite permanent.

Ceramic Resonators

Ceramic resonators are the least stable type available other than the Resistor/Capacitor networks. The temperature profile is a much distorted parabolic function, somewhat resembling that of some capacitors. Temperature coefficient is on the order of 40 to 80 PPM /°C. Typical specified stability for -20°C to +80°C is ± 0.3% (3000 PPM). The C₁ can be as high as 40 pF, making the oscillator extremely vulnerable to circuit influences external to the resonator. The R_s however is on a par with A-T type crystals, at around 40Ω. The positive features of this type are the small size, low cost, and relative simplicity of designing it into a PICmicro part. Because these have a very low Q, the start-up time can be very good, although with the large phase shift capacitors necessary at low frequencies where this would be an advantage, the bias stabilization time will probably dominate the start-up characteristics. If the stability requirements are very modest, this will be a good choice.

R/C Oscillators

The PICmicro parts can be configured to operate with only a resistor and a capacitor as frequency determining elements. This is a very low cost method of clocking the PICmicro. The stability achieved this way is at best only adequate if the only thing required of the oscillator is to keep the PICmicro marching along to the next instruction. The main effects on stability are that of the switching threshold of the OSC1 input, and the temperature coefficient of the resistor and capacitor.

FIGURE 12:FREQUENCY vs. TEMPERATURE FOR NC38 TIMING FORK TYPE CRYSTAL

HOW TO CHOOSE A RESONATOR

Type Trade-offs

The primary trade-offs for a designer when choosing a resonator are frequency, size, stability and cost. The lowest cost oscillator is the RC type. This also has the worst stability. The components however tend to be reliable and small, whereas resonators are in general larger and have limitations on the amount of physical punishment they can absorb.

A-T cut crystals have the best overall stability and are available in frequencies from 1 MHz to the upper limit of the PIC16C5X part, and in a roughly 0.5 "square package". T-05s and 0.3 "square packages" are available at higher costs, down to a frequency of around 5 MHz A-T cut crystals also have a smaller overall temperature profile which the designer has the best chance of specifying and controlling. Temperature stabilities on the order of ± 10 PPM are possible over modest temperature ranges. The A-T cut can be sufficiently reluctant to move off frequency, in response to parasitic reactance changes, that it can fully realize these small deviations over temperature. Such is not always the case with other resonator types or incorrectly specified crystals.

Ceramic resonators offer smaller size and slightly lower cost, although in large quantities, microprocessor grade crystals (± 100 PPM) can be competitive. Ceramic resonators will, however, suffer from temperature stabilities in the 0.3% to 0.5% region. This is a significant step down from quartz crystals of any kind.

A designer must choose a resonator which is available in the desired frequency range, has acceptable temperature characteristics, has the lowest cost

package which is appropriate for that resonator and is suitable for the mechanical packaging of the oscillator chosen. A-T STRIP resonators are normal A-T cut resonators in which the resonator blank is cut in a long strip rather than a disc, and the electrodes cover a much higher percentage of the quartz blank. A standard A-T cut crystal is a thickness mode resonator, and is usually cut in the form of a disk. The electrodes usually cover only a small portion of the blank. The remainder of the blank, not covered by the electrodes, can be thought of as support structure. By removing this support structure, the size of an A-T cut resonator can be greatly reduced. This type of construction violates several rules having to do with thickness to diameter ratios and greatly reduces the overall mass of the blank. This results in reduced performance in the form of slightly less predictable temperature stability, and dramatically reduced power handling capabilities. The A-T STRIPs are generally available up to 20 MHz, depending on the manufacturer.

Tuning Fork type resonators are a type of flexure mode resonators. They are made from quartz, are very small and available at a cost which is competitive with microprocessor grade A-T cut crystals. Tuning forks have a predictable parabolic temperature coefficient, but any drive power in excess of their very low specified level will deteriorate this quickly.

If stability requirements are beyond what is achievable with a good, A-T cut crystal, the next option is to drive the OSC1 pin with an external oscillator. A good Temperature Compensated crystal(X) Oscillator (TCXO) is expensive when compared to crystal resonators. Stabilities of ± 1.0 PPM over large temperature ranges are common.

Price discounts for volume quantities do not always occur, because each unit must be individually compensated. This varies greatly with the stability and temperature range, and so of course does the price, which in any case will be much higher than any resonator, which the PICmicro designer might consider.

Size and Performance

It is generally true that as a designer considers resonators of smaller size, he or she is faced with decreasing overall performance. Even the A-T cut crystal, which has the best stability discussed here, will become less stable as size is reduced, especially when plate area is reduced in relation to the spot as in a STRIP A-T. One important factor is the thermal inertia represented by the mass of the blank. The bigger the blank, the slower it is to follow the changes in temperature. When the blank changes temperature too quickly, it will deviate from the temperature profiles. The frequency will return to this point once the blank has stabilized at the new temperature, but may be well off the profile during a temperature slew. This problem becomes greater as the size of the blank is decreased. Some stability issues are due to the unusual motional parameters associated with certain miniature resonators. Some low frequency types have a C_1 which is larger than the holder capacitance (C_0), making it extremely easy to tune and vulnerable to external influences. Most miniature types have parabolic temperature coefficients which are large enough to make them inferior to A-T cut crystals as well as A-T STRIP cuts, and not only suffer from temperature transient problems as mentioned above, but it is also difficult to control their cut angle and finish frequency. Tuning forks have a somewhat more predictable if larger temperature profile. Almost all miniature types will not perform well (or sometimes at all) with excessive drive levels. The drive power to the resonator must be controlled, and usually one resistor is sufficient.

Cost and Performance

The lowest cost timing system, of course, is the RC type. This rugged, low cost and small timing system is useful only for the most forgiving timing applications. If all you need is something to keep the PICmicro moving, this is a good choice. The next step in cost is most likely the ceramic resonator. Its size is smaller than most A-T cut crystals, but its frequency stability is measured in percent, rather than PPM. A high C_1 also makes it vulnerable to external influences.

Tuning fork types, like all others, vary in price. They may cost less than the ceramic resonator, if a standard frequency is acceptable, or may cost more than an A-T cut if a nonstandard frequency is ordered. Tuning forks usually have a very low C_1 contributing to overall stability. This may actually make it difficult to trim to frequency. Tuning forks have a relatively controllable parabolic temperature curve. A-T cuts have the best overall stability but their cost varies greatly. A-T cuts have an additional advantage in that their temperature

profile is the most easily controlled. This offers some flexibility in specifying the angle of cut. A low angle may be ordered for minimum deviation near room temperature, or a high angle may be ordered to give minimum deviation at extreme temperatures. Standard frequencies and loose specifications for motional parameters will yield cost and delivery competitive with ceramic resonators. Any nonstandard parameters will raise the cost quickly and almost certainly rule out any "off the shelf" part. It will be necessary to specify a nonstandard crystal, if the greatest possible stability is to be "wrung out" of an A-T cut crystal.

Packages

Quartz crystals have a large and mostly obsolete stable of resonator holders to choose from. This is because of the much longer history of quartz crystals. Most of the nomenclature used to describe them, and the technology used to develop them, comes from the MIL-STD system. These include the H/C 6, which is about .750" square, and is only necessary to accommodate the lowest frequency A-T cut. The H/C 43 is only about .500" square, and probably accounts for most of the crystal production in the world today. The H/C 45 is still smaller at about .350" square. There are many other standard part numbers which are variations of these, with pins or wire leads, thin version and short versions, and several different methods of sealing the package. Most manufacturers offer their own nonstandard variations of these, as well as clever ways to surface mount them. Most of these variations however, have their origins in the standard H/C parts. The method used to seal the package will have the greatest impact on price and ageing. Solder sealed crystals are usually the least expensive owing to the modest equipment requirements, and simplicity. Resistance weld is slightly more costly, and cold weld is a distant third. This may be changing as more large volume production is implemented with resistance welded packages. Because more exotic (expensive) materials are involved in the cold weld and resistance weld packages before any crystal is mounted in it, is doubtful that this order of cost will change very much. Both solder sealed and resistance welds leave some residue, which over long periods of time contaminate the blank. This causes long term frequency shifts, known as ageing. Cold welded crystals cost more because of more expensive materials which must be used, and expensive tooling (dies) which eventually wear out. Cold weld packages, if assembled in a clean environment, have the potential for the lowest ageing rates. Glass crystal holders have in the past held a slight advantage in ageing over cold weld types, but in the last several years, cold weld techniques have matured to where they have surpassed the glass holder in performance. Some manufacturers, because of the processes in place, may offer glass at a competitive cost. There is nothing wrong with glass holders, but these have no particular advantage over a modern cold weld package. In any case, the differences in ageing rates will not be important to all but a few PICmicro designers. Most ceramic resonators are only available in two or three packages, depending on the

manufacturer. The most popular is the dip molded, ranging from 0.3" to 04" square, with some higher frequencies available in lower profiles. Their major size advantage over crystals, if any, will be in height rather than footprint size.

Design Examples

A communications device that is designed around the PIC16C5X part and requires that connecting units have a close timing relationship. Size is not a primary factor, but cost and stability are. A high clock frequency is desired in order to obtain a good sampling rate of the input signal. The PIC16C5X-HS part is selected for a clock frequency of 8 MHz. An X-T Cut crystal is chosen and specified for a maximum frequency deviation of ± 40 PPM over -20° to +70°C. The frequency is too high for a tuning fork type, and the stability is out of the question for a ceramic resonator. An examination of A-T cut frequency deviation / temperature curves show that a ± 1 minute angle tolerance gives ± 30 PPM frequency deviation over temperature. This leaves 10 PPM for ageing over the products five-year life. An A-T STRIP is a choice but at this quantity, the A-T cut in an H/C 43 cold weld type holder, comes in at a lower bid. Since there is space in the assembly, it is chosen.

HOW TO SPECIFY A CRYSTAL

When the PICmicro designer chooses a resonator, whether it is a standard or a custom part, a specification, while not essential, is an extremely good idea. A clear specification covering all items of form, fit and function, will eliminate any possibility of confusion on the part of the manufacturer, and insure the part will be suitable for the application. The specification should communicate your requirements to the manufacturer and be an instrument by which questionable parts may be measured. Time for discussion with the manufacturer of the resonator is when the specification is being written, not after. The designer must have or gain knowledge of what parameters raise the difficulty level of manufacturing the resonator, and so the cost. Items which effect cost and levels at which these items become an issue, may vary between manufacturers. A typical crystal design sheet is shown in Figure 13. The A-T cut crystal is likely to have the most detailed specification. Other types of resonators will follow this general form with differences being mostly that of omitting many items. This data sheet is likely to become a document in a drawing package for design of a larger assembly, so the sheet begins and ends with blocks for a drawing number, sign-offs, and revisions. The title informs the manufacturer that the crystal is intended for use in an oscillator, as opposed to filters, or other applications.

Motional Parameters

The first item in crystal design is frequency and the operating load. This might include series resonance (no load), but the PICmicro designer will almost certainly use a value of about 1/2 of the phase shift capacitors, plus any trimmer capacitors which may be added. It is

customary to use a standard value here such as 20 or 32 pF, but a nonstandard value is not very difficult given modern manufacturing equipment. The frequencies possible with the PICmicro oscillator should not strain the capabilities of most manufacturers.

The second item is the "Make Tolerance". This the accuracy to which the crystal is manufactured at room temperature. This should be at least as small as the temperature deviation, and a ± 20 PPM should not effect the cost significantly. Avoid tightly specifying this value. Tolerances of ± 10 PPM and less are quite practical but more difficult and will impact cost. If the stability budget does not allow this for at least ± 20 PPM for tolerance of the crystal and associated components, then an adjustable component may be necessary. The added cost of parts and labor to adjust them must be weighed against the cost of tighter make tolerances on the crystal. This decision must be made on an individual basis.

The third item in the design parameters is the mode of vibration. This will be the fundamental mode for almost all PICmicro designers. Other possibilities include the third overtone operation, but many other parts must be added in order to insure operation on only the desired overtone. While there are some advantages to overtone operation, almost all PICmicro designers will specify the fundamental mode. Still, what may be obvious to the PICmicro designer must be conveyed to the crystal designer, and so this item should not be omitted, or minimized. Series resistance is usually a "not to exceed" value. A good fundamental mode crystal in the PICmicro operating frequency range will not be above 10 or 15Ω , although the oscillator may run with a higher value. This depends on the frequency and excess gain available from the particular model of the PICmicro part, at that frequency. The higher resistance will mean more power dissipated in the crystal, and for this reason a nominally lower value should be adhered to. The load capacity will have an effect on this value. The practically achievable series resistance will rise as the load moves the operating point away from series resonance and towards anti-resonance (Figure 12).

The motional capacitance, or C_1 , may be the most troublesome item for the PICmicro designer to specify. This item will have the single largest effect on the tuning sensitivity (intended or unintended) of the oscillator. Additionally, if the C_1 is specified to be too small, the crystal designer, who controls C_1 by adjusting the electrode size, will use a very small electrode. This will result in the drive power being dissipated by a small portion of the crystal blank, making drive related areas, such as activity dips and other spurious, more critical. If a large C_1 is specified, the unit may be unnecessarily less stable. The static capacitance or C_0 , is usually a "not to exceed" value, and it is not of much interest the PICmicro designer unless a large and specific degree of adjustability is required from the oscillator. This may be important if an electrically tunable oscillator is desired. In this case, a specific ratio of C_1 to C_0 could

be specified. This would not be a low-cost item. It is customary to leave this blank if a specific value is not desired, or the words "as required" can be placed in that location.

Other alternative methods of specifying C_1 and C_0 might include a fractional frequency deviation between series and load capacity operation. The drive level should indicate the highest drive level which the PICmicro designer estimates the crystal will experience in operation. The crystal designer would like this value to be very low, rendering it a nonissue. The PICmicro designer must specify a practical maximum value and take steps to insure that it is not exceeded. Operation at spurious modes and activity dips are just two of the possible consequences of excessive drive levels. Activity dips are not to be tolerated if reliable operation is expected. To quantify this, a maximum allowable value is placed on the frequency deviation. This should be less than 1 PPM and must be less than 5 PPM at reasonable drive levels (i.e., less than 1 mW). The maximum permissible drive level is determined somewhat by the size of the blank, the electrode, and therefore the size of the holder chosen. The crystal manufacturer should offer a realistic value.

Temperature Characteristics

The crystal manufacturer must know the temperature range over which operation is intended, and this is the first item under the heading of temperature characteristics. The temperature profile of an A-T cut crystal is controlled by the angle of cut. The desired profile is also chosen in terms of angle. When purchasing a crystal however, do not attempt to specify an angle. These angles are referenced to the crystal's atomic lattice, and are calibrated using an X-ray diffraction technique. There is little direct correlation between manufacturers. Once again the measured results, in the form of measured temperature profiles, are much more accurate, and are the final word in any process control. The PICmicro designer should specify a fractional frequency deviation with tolerances between the turning points of the temperature profile. This is the accepted industry standard for specifying temperature performance, and any crystal manufacturer will readily accept it if the tolerances are realistic. A typical temperature profile might read; "turn-to-turn 5.5 PPM, + 5.0, - 3.5".

Packages

The type of package and the method of sealing it should be specified, although it may be useful on occasion to leave this item blank. Some manufacturers are equipped especially well for a particular type of holder or sealing process, and may offer a better package than required, at a competitive price. In general however, it is best to specify this at the outset. Package types (holders) greatly effect the price of a crystal. The primary performance effect is that of ageing, though other factors, such as thermal characteristics may also be effected.

Other Resonators

Specification of the NC-38 type crystal is limited to motional parameters, as it is not a "rotated" cut. There is little the crystal designer can do to alter the temperature profile. Specifying a ceramic resonator is mostly a matter of custom frequencies, but some control of motional parameters and package variations are possible, though not common. The large temperature profile tends to dominate all other considerations.

Crystal Example

The following is a specification for a 10 MHz A-T cut crystal which the PICmicro designer is likely to choose for a high stability application. The frequency tolerance is ± 20 PPM. A rather modest C_1 of .028 pF $\pm 20\%$ is specified and the C_0 , though not specified, will be around 5 to 7 pF. It is required to operate on frequency with a 32 pF load. The maximum drive level is 1 mW, and no activity dips greater than 3 PPM will be accepted. The crystal will operate over the temperature range of - 20°C to + 70°C. The frequency deviation between turnover points, is 5.3 + 4.5, - 3.2 PPM. Notice that the turning points do not necessarily fall within the operating temperature range (Figure 10). These deviations between turning points correspond to 1, 2 and 3 minutes of angle relative to the zero coefficient angle. Although the 1 minute curve displays a smaller deviation between the turn points, if it were the center of the angle range the lower end of 0 minutes would be unacceptable due to the rapid changes at the ends of the operating range, where cubed terms are in effect. The exact deviations were computer generated for each crystal angle. These offer more detail and accuracy than is possible with graphical techniques. An alternate method of specifying this is to set a total deviation over the entire operating temperature range of about ± 8 PPM. This is not as exact, and leaves the manufacturer more freedom to interpret requirements. If the PICmicro designer is not comfortable with these concepts, this may be the best approach. One may notice a small dissymmetry in the turning deviations. This is because the chosen operating temperature range is symmetrical at about 25°C, and the inflection temperature of the A-T cut is closer to 27°C or 28°C (Figure 10). In some cases the center of the operating temperature range may be very different from the inflection point of the crystal, and in order to realize the benefit of the best angle, a frequency offset at 25°C would be needed to center the temperature profile (this would not be part of the design sheet). The package is chosen to be an H/C 49 type which has a resistance weld seal. A maximum ageing rate of 2 PPM / year is required. No unusual shock or vibration is expected for this unit. Under the area of testing, temperature testing is required only on a sample of the lot. All units will be exposed to a thermal shock, and 10 days of ageing at 85°C. Ageing is of concern, so gross leakage is specified to be tested on all the units, and a fine leak test is to be performed on a 13% sample. Any notes about the application or special concerns would complete the crystal design sheet.

THE PICMICRO ON BOARD OSCILLATOR(S)

PICMicro devices actually contains four complete oscillators which can be selected during the programming process. The selected oscillator is connected to the OSC1 and OSC2 pins, as well as the chip clock drivers by CMOS switches. In the windowed parts, these are all available to the programmer, while the OTP and QTP parts are pre-configured at the factory, and must be ordered as the desired type. The four types of oscillator available in the PIC16C5X/16CXXX series are:

- RC (resistor capacitor)
- LP (low power)
- XT (crystal < 4 MHz)
- HS (High speed)

The four types of oscillator available in the PIC17CXXX series are:

- RC (resistor capacitor)
- LF (low power)
- XT (crystal < 4 MHz)
- EC (External Clock)

The four circuits are shown in Figure 8. This unique arrangement gives the designer the ability to optimize the performance of the PICmicro in terms of clock speed, type of resonator, and power consumption.

The RC Oscillator

The RC oscillator is a relaxation type similar to the popular 555 timer. The OSC1 pin is the input to a Schmitt Trigger.

The LP oscillator

The LP, or low power oscillator, is designed to trade speed for low power operation. Although this circuit shares the same topology (schematic) as the XT oscillator, the transistors used in the LP oscillator have a higher Rdss value and draw considerably less current. This configuration is optimum for low frequency operation, because it trades the away unnecessary high frequency responses for dramatically reduced operating currents.

The XT oscillator

The XT oscillator is designed to give a compromise between high frequency performance and modest power consumption. The gain of this oscillator is as much as 15 times higher than the LP oscillator. This middle range will be used for frequencies up to 4 MHz.

The HS oscillator

The HS oscillator is designed to give the maximum gain and frequency response. The current consumption is accordingly higher. The gain is roughly five times higher than that of the XT oscillator. This gives the PICmicro the ability to operate at frequencies up to 20 MHz.

FIGURE 13:CRYSTAL DESIGN SHEET

XYZ INC.	CRYSTAL DESIGN and TEST
DRAWN _____ DATE_____	
APPROVED _____ DATE_____	
FREQUENCY @ LOAD _____	OPERATING TEMPERATURE RANGE _____
MAKE TOLERANCE _____	Frequency Deviation _____ From Turn to Turn Over Operating Temperature range
MODE OF VIBRATION _____	
SERIES RESISTANCE _____	
MOTIONAL CAPACITANCE _____	
STATIC CAPACITANCE _____	
DRIVE LEVEL _____	PACKAGE _____
SPURIOUS _____	TYPE OF SEAL _____
ACTIVITY DIPS _____	EVIORNMENTAL: VIBRATION _____ SHOCK _____
AGEING _____	
CRYSTAL TEST	
TEMPERATURE _____	GROSS LEAK _____
THERMAL SHOCK _____	FINE LEAK _____
AGEING _____	
NOTES	

FIGURE 14:EXAMPLE CRYSTAL DESIGN SHEET

XYZ INC.	CRYSTAL DESIGN and TEST
DRAWN _____ DATE_____	
APPROVED _____ DATE_____	
FREQUENCY @ LOAD <u>10 MHz @ 32 pF</u>	OPERATING TEMPERATURE RANGE <u>20 to + 70°C</u>
MAKE TOLERANCE <u>± 20 PPM</u>	Frequency Deviation _____ <input type="checkbox"/> From Turn to Turn <input type="checkbox"/> Over Operating Temperature range
MODE OF VIBRATION <u>Fundamental</u>	
SERIES RESISTANCE <u>25 Ω Max.</u>	
MOTIONAL CAPACITANCE <u>.028 pF $\pm 20\%$</u>	PACKAGE <u>H/C 49</u>
STATIC CAPACITANCE _____	TYPE OF SEAL <u>Resistance</u>
DRIVE LEVEL <u>1 mW Max.</u>	EVIORNMENTAL: N/A
SPURIOUS <u>< - 3 dB</u>	VIBRATION _____
ACTIVITY DIPS <u>< 3 PPM</u>	SHOCK _____
AGEING <u>< 2 PPM / Year</u>	
CRYSTAL TEST	
TEMPERATURE _____	GROSS LEAK <u>100%</u>
THERMAL SHOCK _____	FINE LEAK <u>13% AQL</u>
AGEING <u>10 Days at 85°C</u>	
NOTES	

APPENDIX A

The curves of Figure 10 are calculated using a general form developed by Bechmand in 1955. For any temperature T , a fractional deviation from the frequency at the reference temperature T_0 , is given in the form:

$$\frac{\Delta F}{F} = a(T - T_0) + b(T - T_0) + (T - T_0)^3$$

where:

$$a = -5.15 \times 10^{-6} * {}^\circ(\theta - \theta_0)$$

$$b = 0.39 \times 10^{-9} - 4.7 \times 10^{-9} * {}^\circ(\theta - \theta_0)$$

$$c = 109.5 \times 10^{-12} - 2 \times 10^{-12} * {}^\circ(\theta - \theta_0)$$

$(\theta - \theta_0)$ = the difference between the intended angle and the zero temperature coefficient angle, in degrees of arc.

T_0 is the reference temperature and is usually taken as 25°C. The zero temperature coefficient angle is approximately - 35.25° relative to the Y-axis. The exact angle which produces a zero temperature coefficient and the exact inflection temperature are both strongly dependent on several factors, including overtone and resonator geometry. A degree as a unit of angle is too coarse for sufficient resolution. The following coefficients are divided by 60 for units of minutes of arc.

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