Robustness of PIN Limiter Diodes to an ESD Event Based on VF-TLP Characterization

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***Abstract*—PIN limiter diodes are primarily used for protection from excess RF power in RF circuits. These diodes are positioned onboard at the I/O lines of the RF circuits. If an ESD event occurs, the first line of protection is offered by the PIN limiter diode. The main questions addressed in this letter are: Can the PIN limiter diode protect the RF circuit against ESD? If yes, then what is their ESD robustness? How do they compare against the standard ESD protection TVS diodes? This knowledge can guide the reader to understand whether or not the PIN limiter diode can help prevent ESD damage. The robustness of the diodes is investigated experimentally using a very fast transmission line pulse tester with a 10 ns pulse width and about 300-400 ps rise time. These diodes are tested for their withstand current, turn-on time at 1 A current, turn-on voltage, voltage clamp at 1 A current, capacitance, signal bandwidth, and effective package inductance. These diode parameters are essential in quantifying the component-level response of a device under test. This letter shows that the PIN limiter diodes are not a suitable replacement for the TVS diodes as an intentional ESD protection device. In case an ESD event occurs, these diodes are robust to ESD current levels up to 2.5-9 A and offer limited protection. They may effectively complement the TVS protection by offering a fast turn-on time and protection up to a certain ESD level, after which the (slower) TVS takes over.**

***Index Terms*—ESD, PIN limiter diodes, TVS, vector network analyzer (VNA), very fast transmission line pulse (VF-TLP).**

I. Introduction

ELECTROSTATIC discharge (ESD) protection has become a necessary design element in high-speed RF and microwave circuits. However, introducing ESD protection elements on RF circuits may cause RF performance degradation [1]. To prevent RF performance degradation, devices with low capacitance are designed and implemented [2]. Protection elements can be designed and implemented internally to the high-speed RF ICs, or they can be implemented using onboard external devices such as TVS components [3]. Onboard protection methods involve the use of primary and secondary protection devices [4]. The ESD protection device is placed before the component/part to be protected from ESD as shown in Fig. 1. Here, the primary onboard protection is placed near the source of the ESD stress, and the secondary protection diode (on-chip) is inside the protected device.

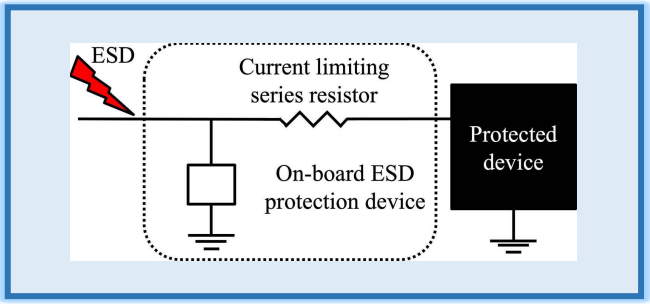

Fig. 1. Typical onboard ESD protection implementation.

Under normal operating conditions, the protection devices offer high impedance and behave as a capacitance to the signal path. When an ESD event occurs, the onboard primary protection device is intended to carry a majority of the ESD-induced current while the secondary protection device carries the remaining current. During the event, the protection device turns on and clamps to its clamping voltage. At this clamped state, the impedance of the device is low, and it diverts the ESD current from signal trace to the ground. As a result, the device is protected from the ESD event.

Take-Home Messages:

- A methodology, which helps in selecting ESD protection devices by comparing diodes for their transient and frequency domain response using a VF-TLP and a VNA.
- The PIN limiter diodes are not a suitable replacement for the TVS diodes as an intentional ESD protection device, however, PIN limiters may be sufficient in cases in which ESD to an RF trace only leads to currents of a few Ampere.
- Component-level ESD and signal integrity evaluation of diodes are presented.
- First time investigation of ESD protection properties of PIN limiter diodes comparing many models and ESD TVS.
- The device clamping voltage and the turn-on time are critical parameters to evaluate the first few nanoseconds protection capability.

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PIN diodes are used in various applications such as switches, attenuators and phase shifters [5]. PIN limiters differ from the PIN diodes based on the doping of gold atoms in the I layer (middle layer) of the diode. The gold doping in the I layer reduces the minority carrier lifetime. The time the diode takes to recover from the low impedance state back to high impedance state (after the application of RF input signal bursts) is proportional to the minority carrier lifetime. Therefore, a lower minority carrier lifetime represents a faster diode recovery time [6]. A protection device from Keysight [7] known as an integrated diode limiter, consists of two limiters which can provide both power limiting and ESD protection; i.e., utilizing limiters for an ESD protection application. The ESD robustness of PIN limiters has not been reported in the literature. The PIN limiters may also provide ESD protection, even though they are typically used as power limiters.

In this letter, the ESD protection robustness was experimentally investigated for the PIN limiter diodes with low capacitance and surface mount style packages. The diodes were tested using a VF-TLP tester with a 10 ns pulse width, and about 300-400 ps rise time. This setup has a faster rise time and a shorter pulse width than the 100 ns standard TLP waveform. The IEC 61000-4-2 specification [8] stipulates that an I/O trace of interest on the PCB or an RF-circuit will not be subjected to a direct ESD discharge. The IEC pulse is expected to occur at a different location in the system. A regular TLP pulse has a rise time of approximately 10 ns. More important parameter than the pulse width is the rise time to assess the voltage overshoot during an ESD generator discharge. A VF-TLP pulse [9] has a much faster rise time, typically 0.6 ns. A TLP waveform with a 100 ns pulse width and a rise time of 0.6 ns could be used, but it would not be possible to distinguish between two potential failure mechanisms, over-voltage due to the fast rise time and thermal damage due to the long pulse width. Thus, a narrow fast rising pulse is considered a better match than 100 ns TLP or IEC pulse.

II. ESD Protection Components

A. PIN Limiter Diodes

Fig. 2 (a) depicts a typical power limiter application using the PIN limiter diodes. These diodes are soldered from trace to ground, which is similar to the implementation to the ESD protection implementation shown in Fig. 1. PIN limiter diodes from different vendors such as Macom/Aeroflex, Skyworks, and Microsemi were investigated.

B. TVS Diodes

TVS diodes are specifically designed to protect devices against damage from ESD events. PIN diodes can be a part of the internal structure of a low capacitance TVS diode [10] as shown in Fig. 2 (b). In this TVS configuration, PIN 1 and 2 would typically be designed such that ESD robustness for both polarities is approximately equal.

The TVS diodes are one of the most effective ESD protection devices amongst the other TVS components [3] such as varistors, spark gaps, and non-linear polymers. The focus

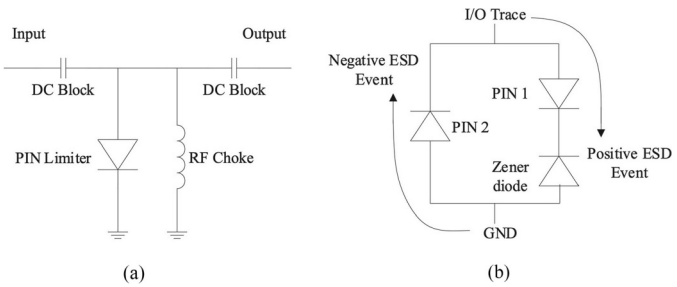

Fig. 2. (a) Typical power limiter design using PIN limiter diodes [6]. (b) Internal structure of a low capacitance unidirectional TVS diode [10].

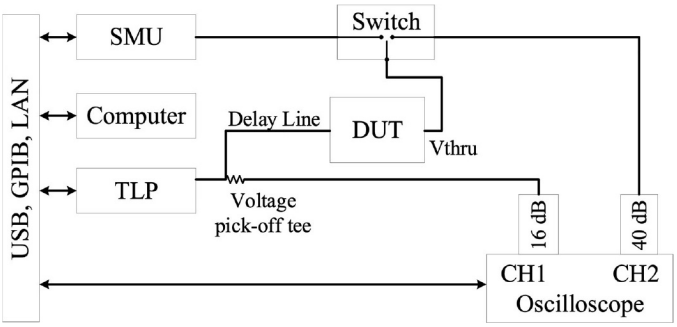

Fig. 3. Block diagram of VF-TLP measurement setup.

of this letter is to investigate the robustness of various PIN limiter diodes to an ESD event and compare it against a TVS diode [11].

III. VF-TLP Test Setup

The device under test (DUT) I-V curve was measured using an ESDEMC VF-TLP tester [12] illustrated in Fig. 3. The I-V curve was used to extract diode parameters described in detail in Section IV. To evaluate the performance of the diodes, a grounded coplanar waveguide (GCPW) prototyping PCB board was used. The VF-TLP measurement setup details are as follows:

- Non-overlapping time domain reflectometry method was used to measure the DUT current and direct voltage measurement method to measure the DUT voltage [13].
- A VF-TLP pulse width of approximately 10 ns was applied to the DUT, to evaluate the first few nanoseconds response.
- An oscilloscope with 20 GSa/s sampling rate and 6 GHz bandwidth was used. The rise time of the VF-TLP pulse measured at the oscilloscope was approximately in the range of 300 to 400 ps.
- To determine the quasi-static I-V curve, the measurement window was set at 70% to 90% of the pulse width. The measurement window setting was applied to the flat region of the waveform. A measurement window is the range of time within the pulse width where the voltage or current of the pulse is measured to calculate the DUT voltage or current in response to the applied VF-TLP pulse [14].
- VF-TLP pulse polarity: An ESD event can have both positive and negative polarities. Emphasis was placed on the

reversed bias diode clamping and its ESD current carrying capacity. In reversed bias orientation, the turn-on voltage is higher than the forward biased (p-n junction) turn-on voltages approximately in the range of 0.7 to 0.8 V. It should be noted that the forward biased polarity is much more robust than the reverse biased polarity. This argument is based on the lower power dissipation of the forward biased orientation against the reverse biased orientation. For example, for the same TLP clamp current, the forward bias diode clamp voltage is lower than the reversed bias voltage and their turn-on voltages are different. In addition, this is strictly true if the current for the forward and reverse polarity are flowing through the same device (internal to the package).

- The source measure unit (SMU) measured the leakage current of the DUT when 1 V was applied to the reverse polarity of the DUT after each TLP pulse.

IV. Diode Parameters and Measurement Results

The measurement results are shown for one PIN limiter diode Microsemi 4701-206 [15].

A. Capacitance

The capacitance is determined to be 0.25 pF at 50 MHz. The frequency point is determined from the 20 dB per decade region of the Z_{21} vs. frequency plot shown in Fig. 4 (a).

B. Frequency Bandwidth and Effective Package Inductance

A 3 dB cutoff point is chosen as the usable frequency bandwidth of the diode. The dotted line in Fig. 4 (b) represents the diode's frequency bandwidth (approximately 14 GHz). The dotted two-sided arrow is a visual representation of the 3 dB insertion loss of the diode in excess of the trace insertion loss. The diode is modeled as a series RLC circuit in the passive (non-conducting) state. The LC resonance of the diode (approximately 19 GHz) is used to calculate the effective package inductance (0.27 nH) given by the formula:

$$L_{package} = \frac{1}{C_{DUT}.(2\pi.f_{Resonance})^2} \tag{1}$$

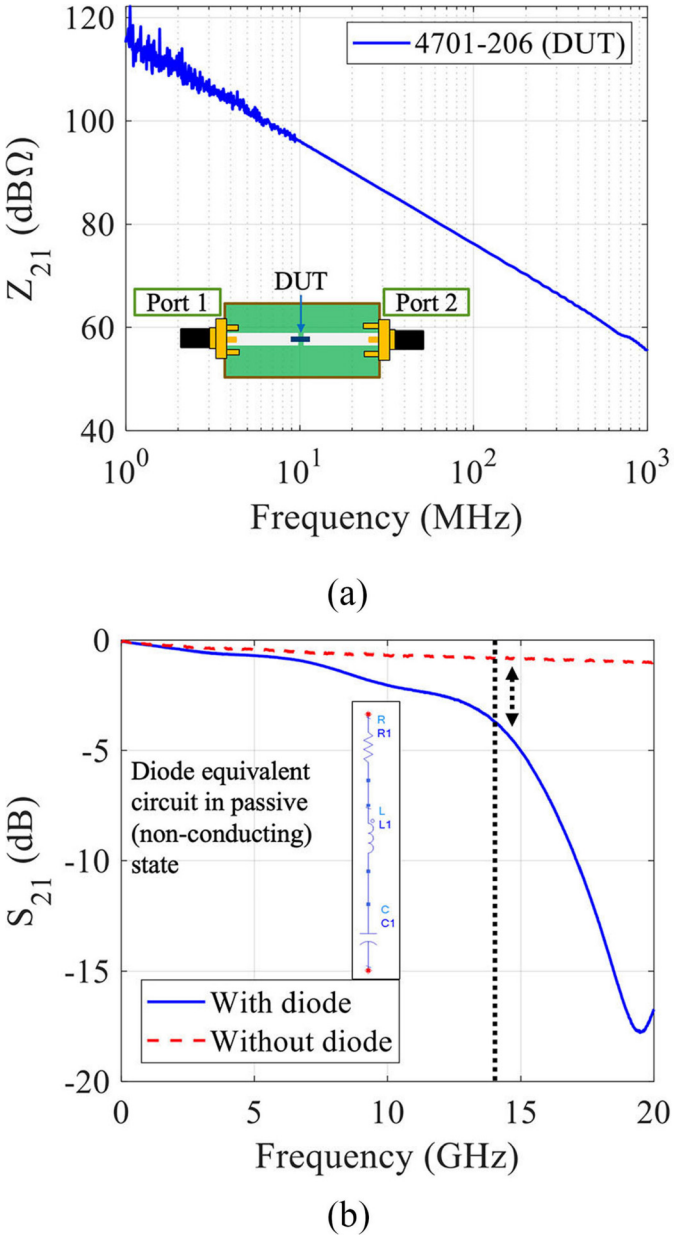

Fig. 4. (a) Diode capacitance is determined to be 0.25 pF at 50 MHz. The solid line refers to the impedance of the diode placed in series to the slot on the microstrip trace. (b) The frequency response of the diode when soldered in parallel on to the measurement GCPW PCB.

C. Turn-On Time, I-V Curve, and Leakage Current

1) Turn-On Time: Using the VF-TLP tester setup, the diode time-domain voltage and current waveforms were measured for each VF-TLP source excitation voltage. In general, the DUT voltage waveforms can have inductive overshoot, snap back behavior or the non-inductive overshoot [16] for the very first nanoseconds and then followed by a relatively flat voltage-clamping region. The non-inductive overshoot is caused due to the conductivity modulation in the silicon [17]. The qualitative illustration for the overshoot and the non-overshoot response of a diode is shown in Fig. 5. The diode clamp current is determined from the diode current waveform by applying the measurement window setting. The measurement window of 70% to 90% was applied to the diode voltage waveform, and the time-averaged voltage value was determined (VDUT). Vtrack refers to the voltage amplitude 30% above in case of an overshoot response and 30% below in case of non-overshoot response in the measured diode voltage waveform. The time associated with Vtrack voltage is called t_2. The difference between the two times t_2 and t_1 is calculated as the turn-on time. It should be noted that if a different % criteria is used for Vtrack, the turn-on time values for different diodes would change, but the overall trend and conclusions will not be affected. The diode current of 1 A is chosen as a comparison unit for the turn-on time parameter. A current of 1 A through the diode is typically used by TVS vendors for determining the diode clamp voltage [11]. In Fig. 6 (a) the vertical dotted lines represent the two time values that result in the turn-on

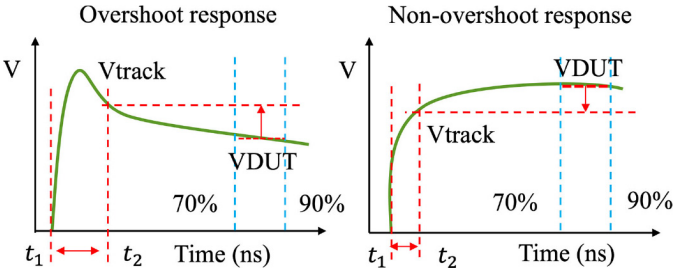

Fig. 5. The two possible diode initial responses: overshoot, or non- overshoot.

time of 2.16 ns for the TVS diode and 0.21 ns for the PIN limiter diode. It should be noted that for the PIN limiter diode at 1 A current, the waveform was considered as a non-overshoot waveform to determine the turn-on time parameter. It was observed that the TVS diode [11] voltage waveform has an overshoot response in the initial nanoseconds followed by the flat clamping region.

2) I-V Curve Plotted for a Measurement Window of 70% to 90%: The VF-TLP pulses are applied to the DUT. Each pulse generates a diode current and diode voltage waveform. The measurement window is applied to the diode voltage and current waveforms to determine the average voltage (VDUT) and current (IDUT) values. The VF-TLP currents are in the range of 10 mA to 20 A. In this measurement range, the instrument applies about 50 pulses to the DUT. This generates an array of 50 voltage and current values, which are represented in the form of an I-V curve plot as shown in Fig. 6 (b).

3) Withstand Current: The VF-TLP pulse voltage at which the leakage current increases 10x to 100x from the initial leakage current value of the diode is chosen as a selection voltage. A VF-TLP pulse voltage lower than the selection voltage is chosen as the maximum withstand voltage. At this particular VF-TLP pulse voltage (maximum withstand voltage) the current at DUT (diode) is determined as the maximum withstand current the diode can handle. It should be noted that the SMU measures the diode leakage current after the application of every VF-TLP pulse. A withstand current (IDUT) of 3.7 A (using a 10 ns VF-TLP pulse width) is determined for the diode shown in Fig. 6 (b).

4) Turn-On Voltage: The voltage at which the diode current is in the range of 1-10 mA is determined as the diode turn-on voltage. Using this definition, a value of 21.8 V is obtained from the I-V curve plot shown in Fig. 6 (b). Here, the turn-on voltage refers to the quasi-static voltage measured at 70% to 90% of the pulse width, and not to the maximum dynamic voltage.

5) Voltage Clamp at 1 A: The voltage corresponding to a diode current of 1 A is used to determine this parameter. It is a parameter provided in TVS datasheet [11] to quantify the clamping behavior of the diode. The voltage clamp for different current levels can be determined from the complete diode I-V curve shown in Fig. 6 (b). Using this parameter definition at 1 A diode current, a voltage of 28.8 V is obtained from the I-V curve plot. This voltage value indicates that for a 1 A current through the diode, this diode will clamp at a voltage of 28.8 V.

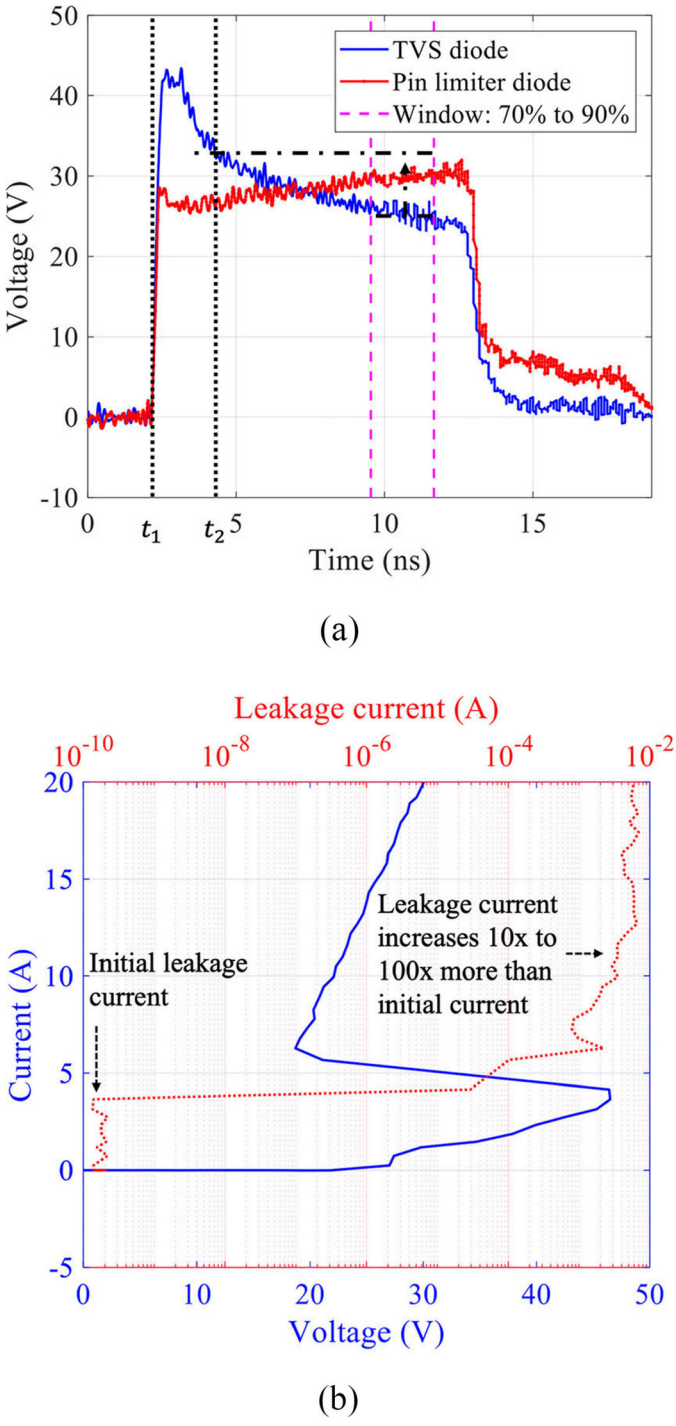

Fig. 6. (a) Turn-on time of 2.16 ns for the ESD103-B1-02ELS TVS diode and 0.21 ns for the 4701-206 PIN limiter is determined. (b) The 4701-206 PIN limiter I-V curve using the measurement window setting of 70% to 90%.

V. Discussion And Conclusion

Table I summarizes the different diodes tested, and their performance based on critical parameters. The diode capacitance, inductance, and frequency bandwidth parameters are essential to quantify the influence of the diode on signal integrity while the diode is in a passive state (during a non-ESD event). ESD withstand currents of about 2.5 A to 9 A have been observed, as well as turn-on voltages in the

TABLE I
DIODE PARAMETER CHARACTERIZATION RESULTS

Sr. No.	Diode	Package	Capacitance (pF)	Effective package Inductance (nH)	Frequency bandwidth (GHz)	Withstand Current (A)	Turn-on time (ns)	Turn-on Voltage (V)	Voltage clamp at 1 A (V)
PIN Limiter diodes									
1	MLP7130	CS19-1	0.29	0.55	8.9	3.5	0.23	30.5	37.2
2	MLP7130	CS20	0.24	1.23	6.7	3.8	0.22	28.5	33.5
3	MLP7140	CS19-1	0.29	0.52	8.8	4.5	0.24	40.3	47.4
4	MLP7110	CS19-1	0.31	0.65	7.5	7.6	0.22	50.6	52.8
5	CLA4601	219	0.37	0.64	7.2	3.0	0.16	21.7	32.2
6	CLA4601	240	0.26	0.94	7.5	2.5	0.24	21.7	34.9
7	CLA4604	219	0.38	0.68	6.7	4.4	0.17	41.0	47.2
8	CLA4604	240	0.29	0.93	7.3	3.2	0.38	40.9	48.2
9	CLA4608	219	0.57	0.67	5.9	8.7	4.53	12.6	53.4
10	4701	206	0.25	0.27	14	3.7	0.21	21.8	28.8
11	4700	206	0.21	0.26	15.9	4.3	0.21	33.2	42.0
Infineon TVS Diode									
12	ESD103-B1-02ELS	TSSLP-2-3	0.09	0.2	30	> 20	2.16	15.2	25.4

range of 20 V to 50 V. A frequency bandwidth of 6 GHz to 16 GHz is achievable, based on the different diodes tested in this letter. Diodes having smaller packages may offer larger bandwidths, due to the lower capacitance and inductance. The PIN limiter diode data was compared with an industry standard ESD TVS protection diode. Although most of the PIN limiter diodes that are shown in Table I may have faster performance for the turn-on time parameter than the ESD TVS diode, the ESD TVS diode has better performance in all other ESD diode parameters. Still, a PIN limiter diode may be part of a circuit design to protect against accidentally coupled high RF power. In this scenario, the PIN limiter diode will offer a moderate level of ESD protection.

Considering a system level ESD requirement for PIN limiter diodes, based on the faster turn-on time parameter, they can complement the TVS diode for the initial low-current ESD event. However, the TVS diode needs to turn on before the current through the PIN limiter crosses the withstand current. It should be noted that the turn-on voltage of the PIN limiter diodes are higher than that of the TVS which may limit the applicability of the PIN limiter and TVS combination. Thus, a system efficient ESD design (SEED) [4] will be needed further to evaluate a specific PIN Limiter and TVS diode combination for ESD protection application on a desired I/O trace.

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