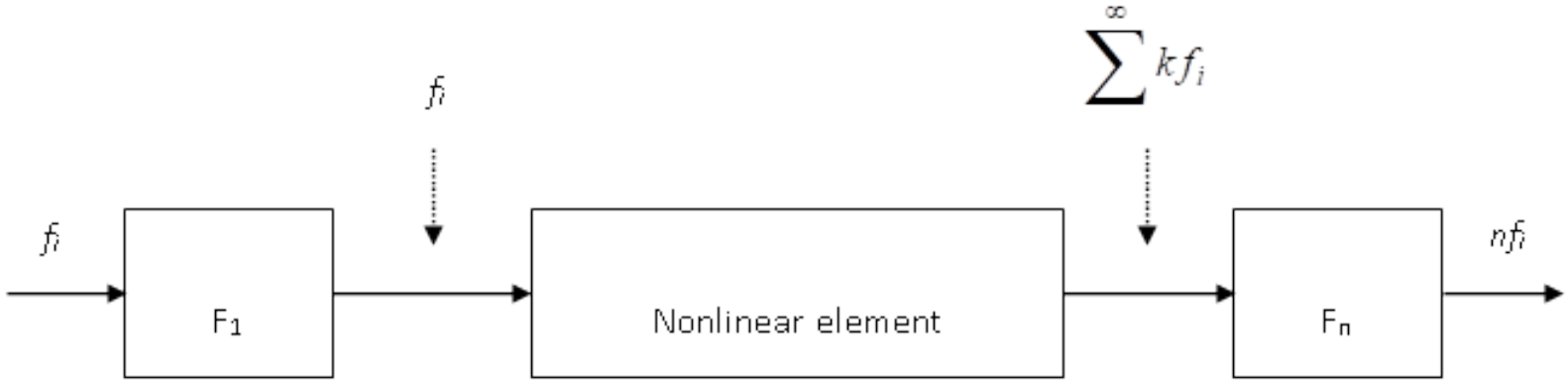
Chapter 5

Microwave Multipliers

Introduction

The waveforms used in communication systems in the millimeter and sub-millimeter ranges are often obtained from a relatively low frequency source. This is the principle of frequency multiplication, which shifts the signal from an input frequency f_i to an output frequency $n*f_i$.



The blocks F_1 and F_n are two pass-band filters centered respectively on f_i and $n*f_i$

Today, the required frequencies are generated at **relatively low powers**: it minimizes the dc power consumption that dissipates the most heat from those that may be temperature sensitive. Operating the frequency multiplier circuit at low power reduces also the levels of spurious signals and harmonics.

Most frequency multiplier circuits are now used in mixer local oscillators, in test instruments or frequency synthesizers or as low-power drivers for transmitters.

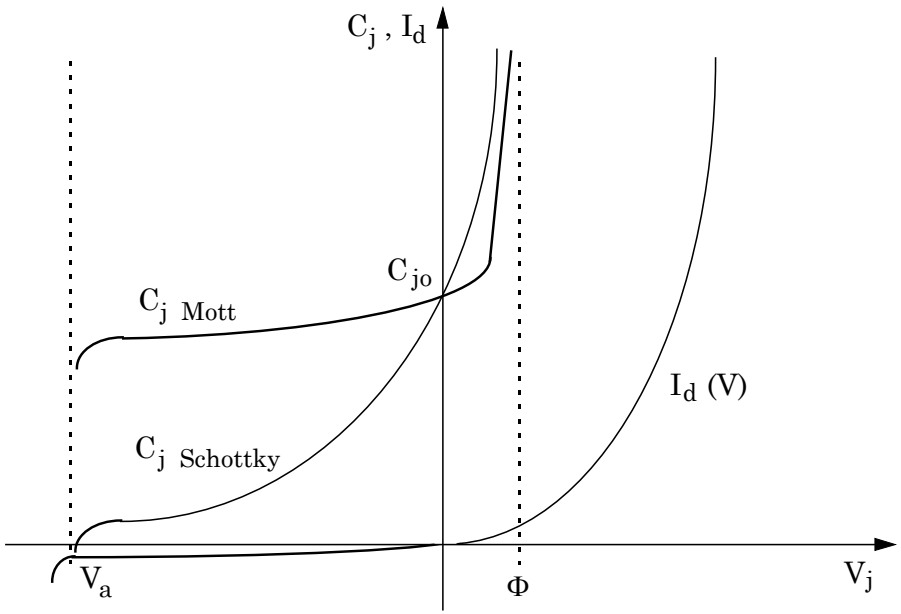
DIODE MULTIPLIERS

When used as frequency multipliers, FETs can usually achieve gain conversion over broad bandwidths while maintaining good dc-RF efficiency at these low power levels.

In contrast diode multipliers always exhibit loss. Varactor multipliers are lossy narrow-band components that operate best at moderate to high power levels.

Resistive diode multipliers (using Schottky diodes) are more broadband but have even greater loss and a limited power handling ability. Thus, the medium- to high-power driver amplifiers required by such multipliers, generate RF power that is eventually wasted in the diodes and matching networks.

As we can see, if the dc point (Q point) is beyond the barrier voltage Φ, the diode frequency multiplier is called "resistive multiplier" because it exploits the conductance characteristic of the diode.

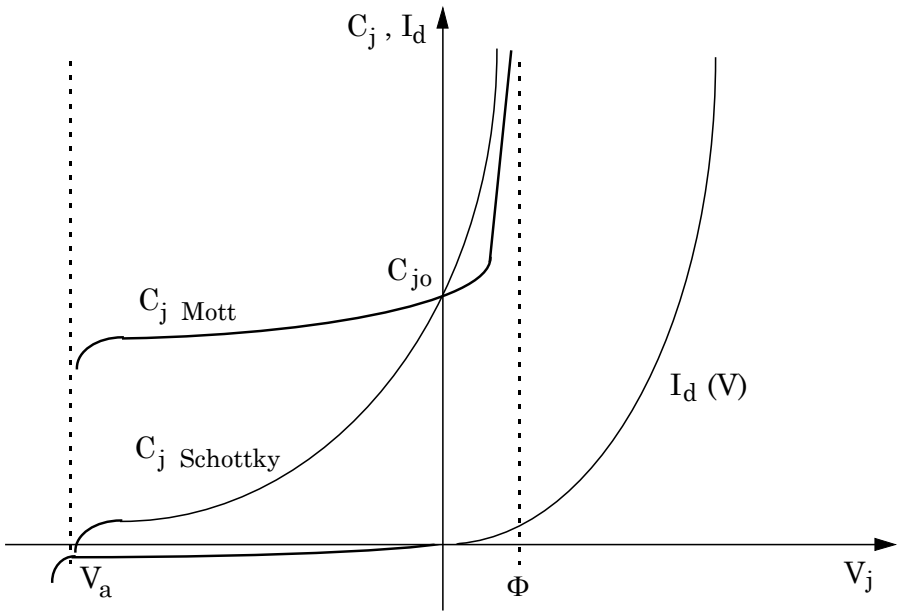


On the other hand, for a dc point between the breakdown voltage (avalanche voltage) V_a and the barrier voltage Φ, the circuit uses the capacitance variations to generate frequency multiplication.

In this last case, we must distinguish between **two** different cases. If the Q point dynamic excursion is from V_a to Φ without reaching this maximal value, the diode presents a pure reactance and such frequency multipliers are called "**reactive** circuits" or "**parametric** circuits". As for amplifiers, they exhibit a very low noise figure.

However, if the barrier voltage value is slightly exceeded, a high accumulation of charges in the nonlinear capacity during the positive cycle of the exciting signal will create a phenomenon called "**snap off effect**". This phenomenon **favors high-order multiplication**.

In fact, the discharge of a high accumulation of charges in a nonlinear capacity during the negative cycle of the signal will generate a very large number of harmonics.

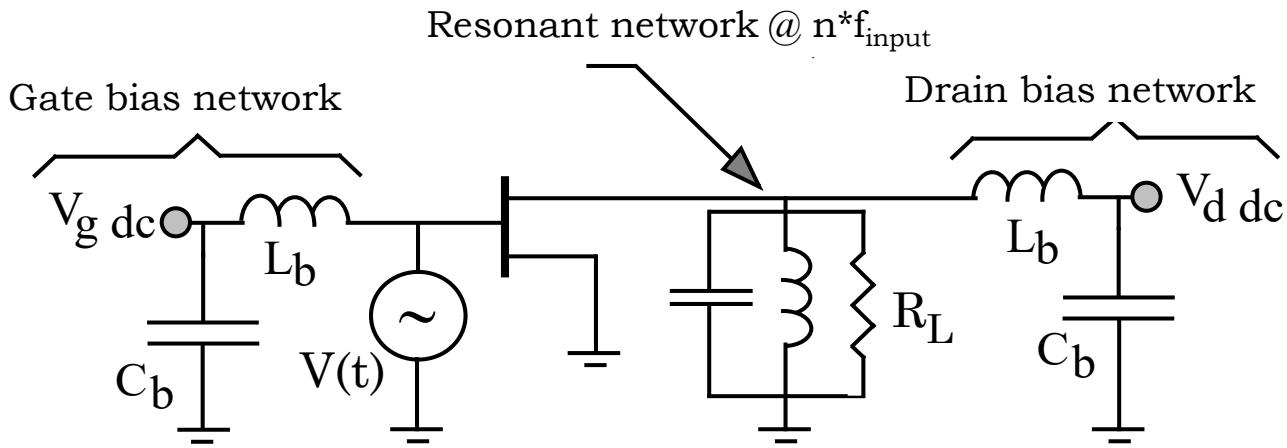


TRANSISTOR MULTIPLIERS

As already mentioned, FETs can usually achieve unity (or greater) gain conversion over broad bandwidths while maintaining good dc-RF efficiency at these low power levels.

If the MESFETs were widely used for frequency multiplication in the RF/microwave range, HEMTs are now more present in frequency multiplier circuits.

The basic scheme of an n-order transistor multiplier is similar to the amplifier one except that at the output we have a resonant circuit between the output and the load. This resonant circuit is centered on the n^{th} harmonic of the fundamental input frequency. The excitation is usually applied to the gate.



TRANSISTOR MULTIPLIERS

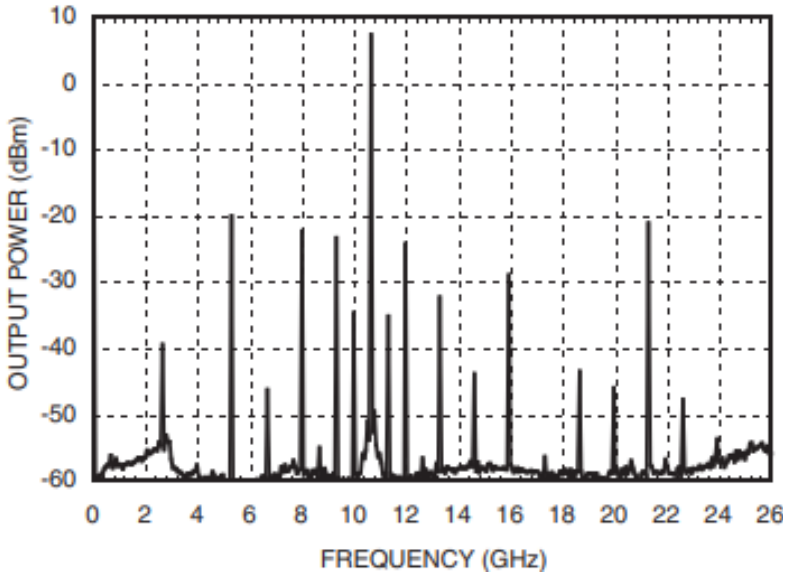
ANALOG DEVICES

HMC445LP4 / 445LP4E

v04.0210

SMT GaAs HBT MMIC x16 ACTIVE FREQUENCY MULTIPLIER, 9.9 - 11.0 GHz OUTPUT

Output Spectrum



Electrical Specifications, T_A = +25° C, Vcc= 5V

Parameter		Min.	Typ.	Max.	Units
Frequency Range, Input			618.75 - 687.50		MHz
Frequency Range, Output			9.9 - 11.0		GHz
Input Power Range		-15		5	dBm
Output Power		4	7		dBm
Sub-Harmonic Suppression			25		dBc
Input Return Loss			28		dB
Output Return Loss			7		dB
SSB Phase Noise (100 kHz Offset)	Pin= 0 dBm		-130		dBc/Hz
Supply Current (Icc)			78	104	mA

TRANSISTOR MULTIPLIERS

For an M finite number of harmonics, the nonlinear input-output voltage-current parameters can be written as

$$V_i(t) = \sum_{k=-M}^{M} V_{ik} e^{jk\omega t}$$

$$I_i(t) = \sum_{k=-M}^{M} I_{ik} e^{jk\omega t}$$

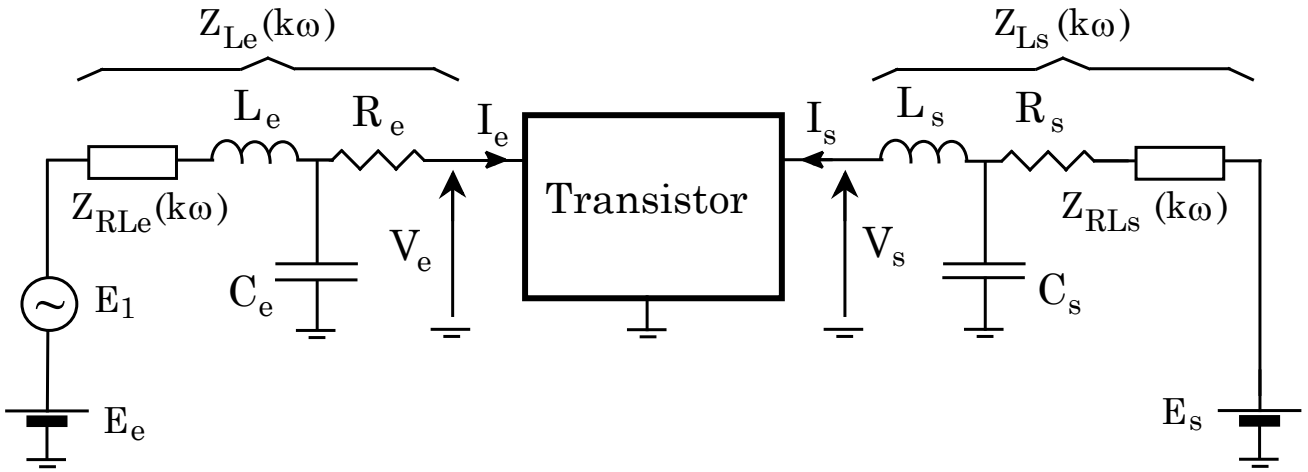
$$V_o(t) = \sum_{k=-M}^{M} V_{ok} e^{jk\omega t}$$

$$I_o(t) = \sum_{k=-M}^{M} I_{ok} e^{jk\omega t}$$

TRANSISTOR MULTIPLIERS

The figure below can be utilized for a generic FET multiplier design. The parasitic elements of gate (R_e, L_e and C_e) and drain (R_s, L_s and C_s) are assumed to be linear and added respectively to the external input-output impedances of the matching networks.

These source and load impedances are noted respectively $Z_{RLe}(k\omega)$ and $Z_{RLs}(k\omega)$.



TRANSISTOR MULTIPLIERS

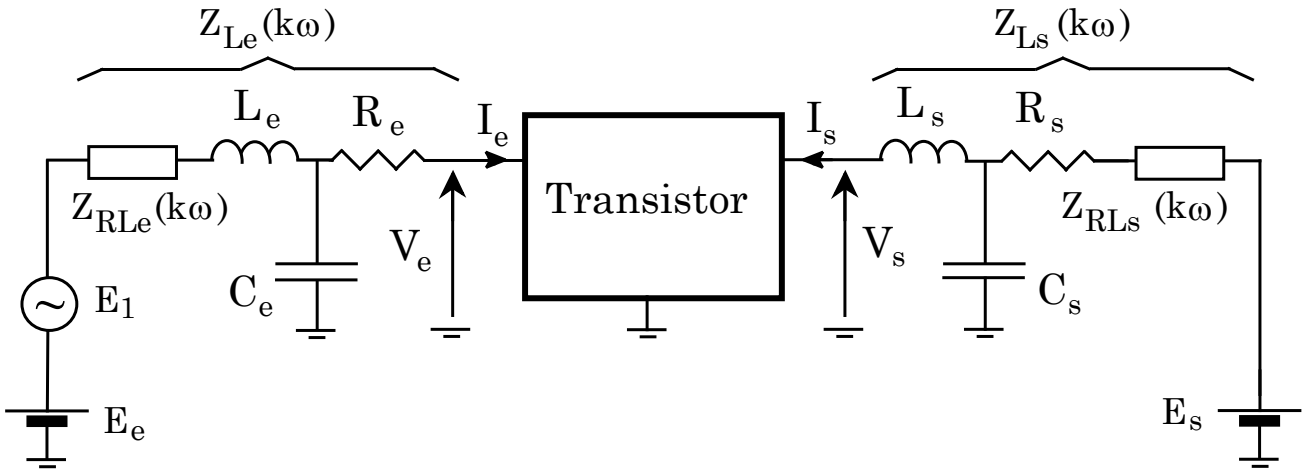
Let E_e and E_s be the bias voltages of gate and drain, respectively, and let E_1 be the input voltage.

The network equations can be written on the form of the following system

$$\left.\begin{aligned} V_{e0} &= E_e - I_{e0}\, Z_{Le}(0) \\ V_{s0} &= E_s - I_{s0}\, Z_{Ls}(0) \end{aligned}\right\} \text{ for } \quad k = 0$$

$$\left.\begin{aligned} V_{e\pm1} &= E_1 - I_{e\pm1}\, Z_{Le}(\pm\omega) \\ V_{s\pm1} &= -I_{s\pm1}\, Z_{Ls}(\pm\omega) \end{aligned}\right\} \text{ for } \quad k = 1$$

$$\left.\begin{aligned} V_{e\pm k} &= -I_{ek}\, Z_{Le}(\pm k\omega) \\ V_{s\pm k} &= -I_{sk}\, Z_{Ls}(\pm k\omega) \end{aligned}\right\} \text{ for } \quad k = 2, 3, \ldots$$



TRANSISTOR MULTIPLIERS

Because small-signal FETs can be used to realize efficient multipliers (particularly for low-order multiplication devices like doublers), a high-frequency FET multiplier chain usually consumes **little dc power and dissipates little heat**; this is an important advantage in space-based systems.

The most widely used circuit is the low-power **"Class-B" multiplier**, which operates in a manner analogous to that of a Class-B amplifier.

Such multipliers are very stable and have good gain, efficiency, and output power.

Other modes of operation can provide higher gain than the Class-B multiplier. However, this high gain is often the result of feedback effects, which may make the multiplier unstable.

Practical Design Approach

PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

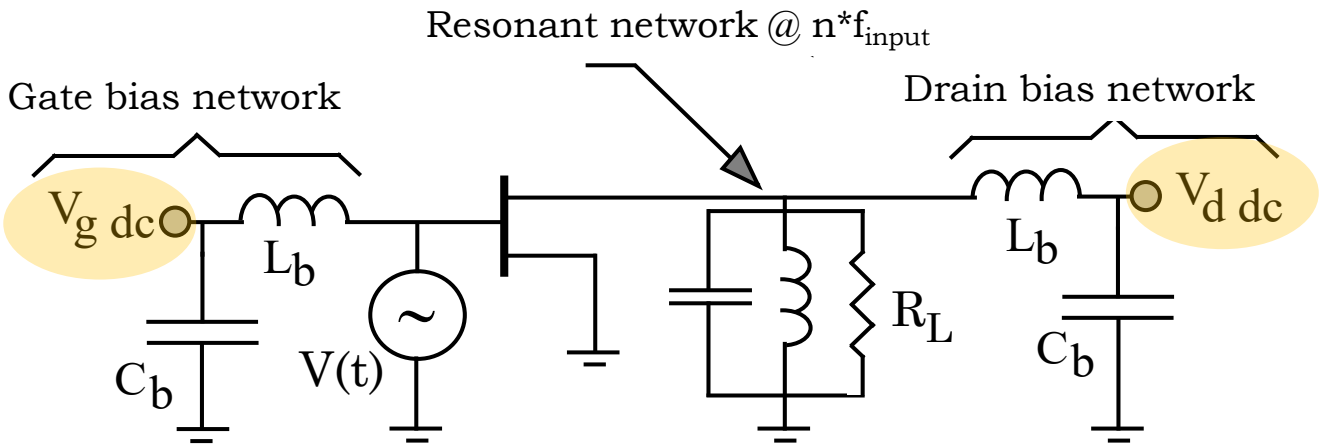
Let us examine the design of a low power Class-B multiplier that generate low-level RF output power (normally below 8-10 dBm) at low harmonics, have at least unity gain, and may have high output frequencies, sometimes in the millimeter range.

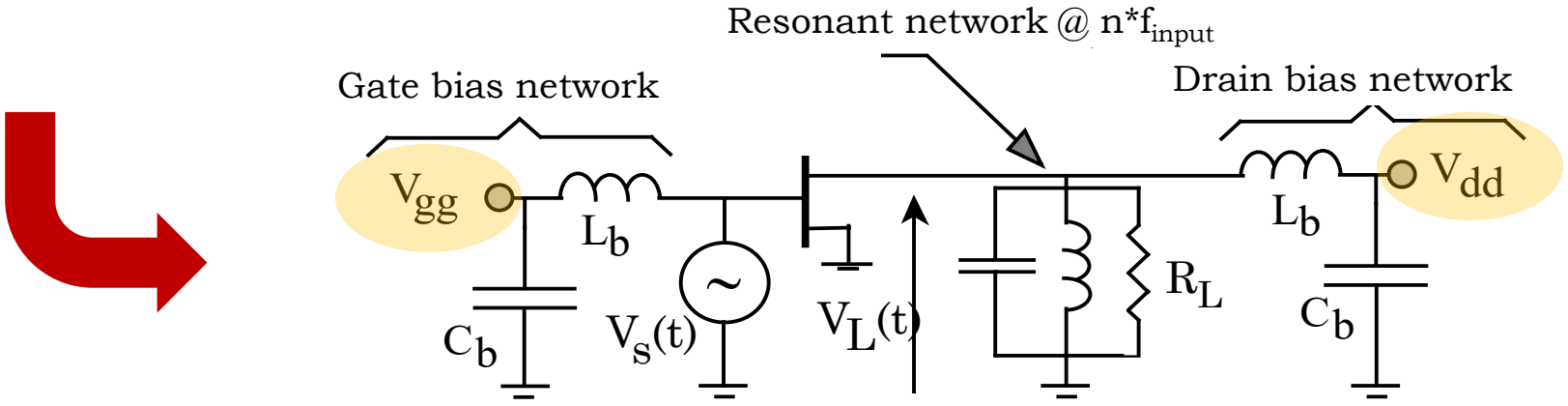
The design approach is applicable to power FET multipliers operating at lower frequencies; it will require only a larger FET with higher power.

As the multiplier is operating in Class-B, the gate is biased near the turn-on voltage V_t, the channel conducts in pulses having a duty cycle near 50% and the gate and drain are short-circuited at all unwanted harmonics of the excitation frequency.

PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

The process starts by examining the properties of a large-signal multiplier circuit that uses an **ideal FET**, then modify the circuit to include a FET having a minimal set of parasitic elements (considering internal/intrinsic bias voltages instead of external ones).

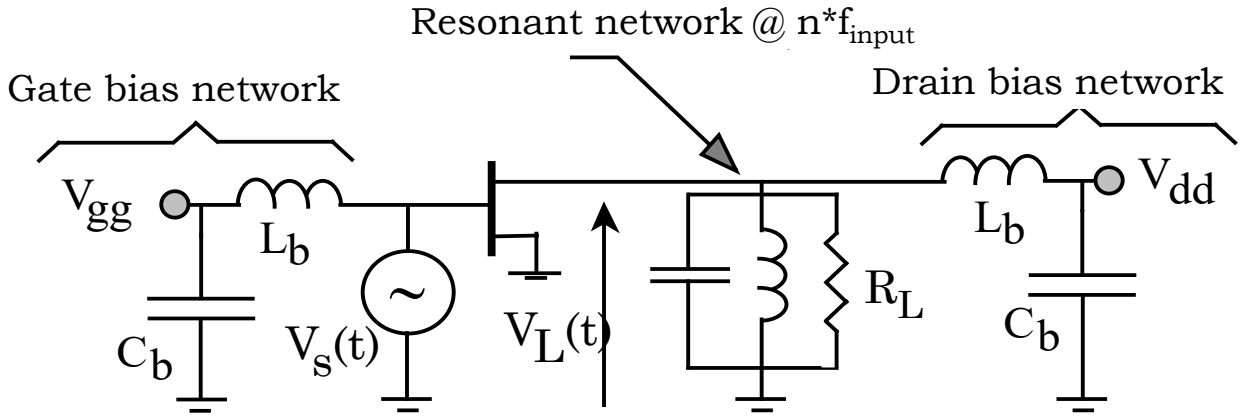




PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

The gate-bias voltage in an efficient FET multiplier must be equal to or less than (more negative than) the turn-on voltage V_t. Thus, the FET's channel conducts only during the positive half of the excitation cycle, and the drain conducts in pulses (which shape is approximately a rectified cosine or half cosine).

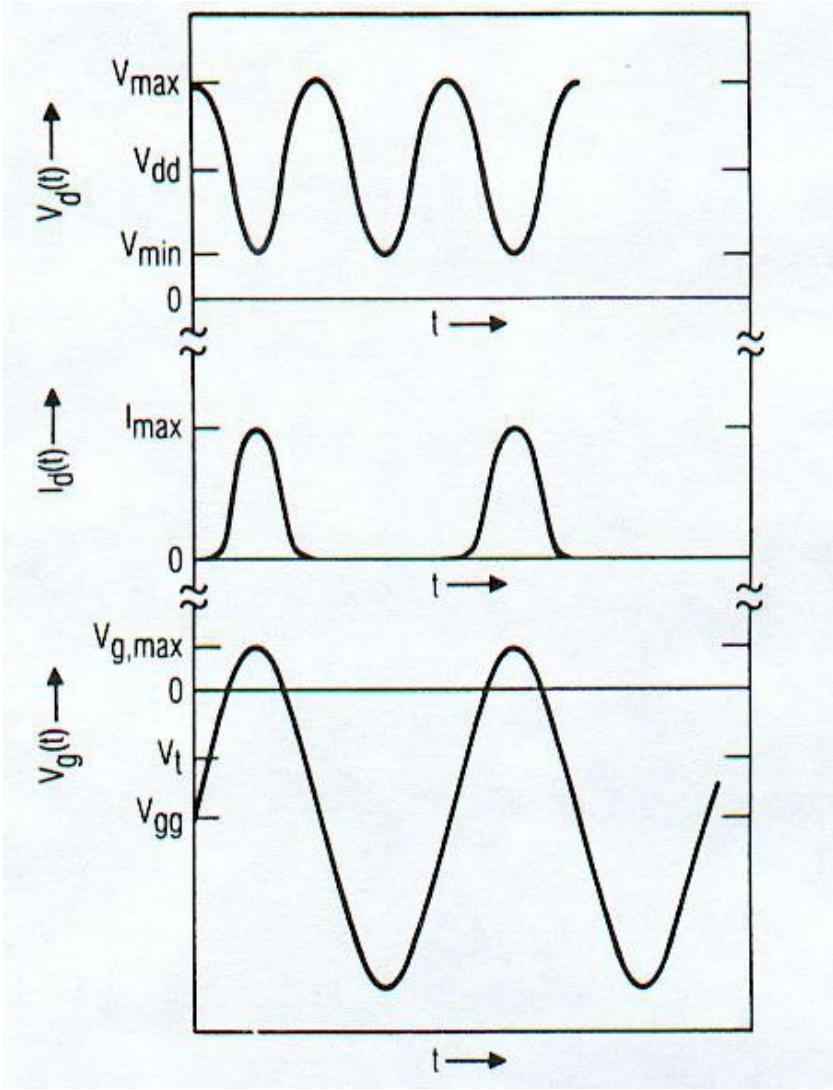
The drain-current waveform can be then modeled as a train of half-cosine pulses. The duty cycle of the pulses varies with V_{gg}: if $V_{gg} = V_t$, the duty cycle is 50%, but if $V_{gg} < V_t$ (the ideal situation), the FET is turned off over most of the excitation cycle, so the duty is less than 50%.



PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

Because the output resonator eliminates all voltage components except the one at the n^{th} harmonic, the drain voltage $V_d(t)$ is a sinusoid having frequency $n*\omega_p$.

For best efficiency, and output power, the drain voltage must vary between V_{max} and V_{min} (V_{min} is the value of drain voltage at the knee of the drain I-V curve when the gate voltage has its maximum value $V_{g\,max}$).



As the maximum negative excursion of V_g is $2V_t$, then

$$V_{\max} = V_a - 2\,|V_t|$$

where V_a is the drain-gate avalanche breakdown voltage.

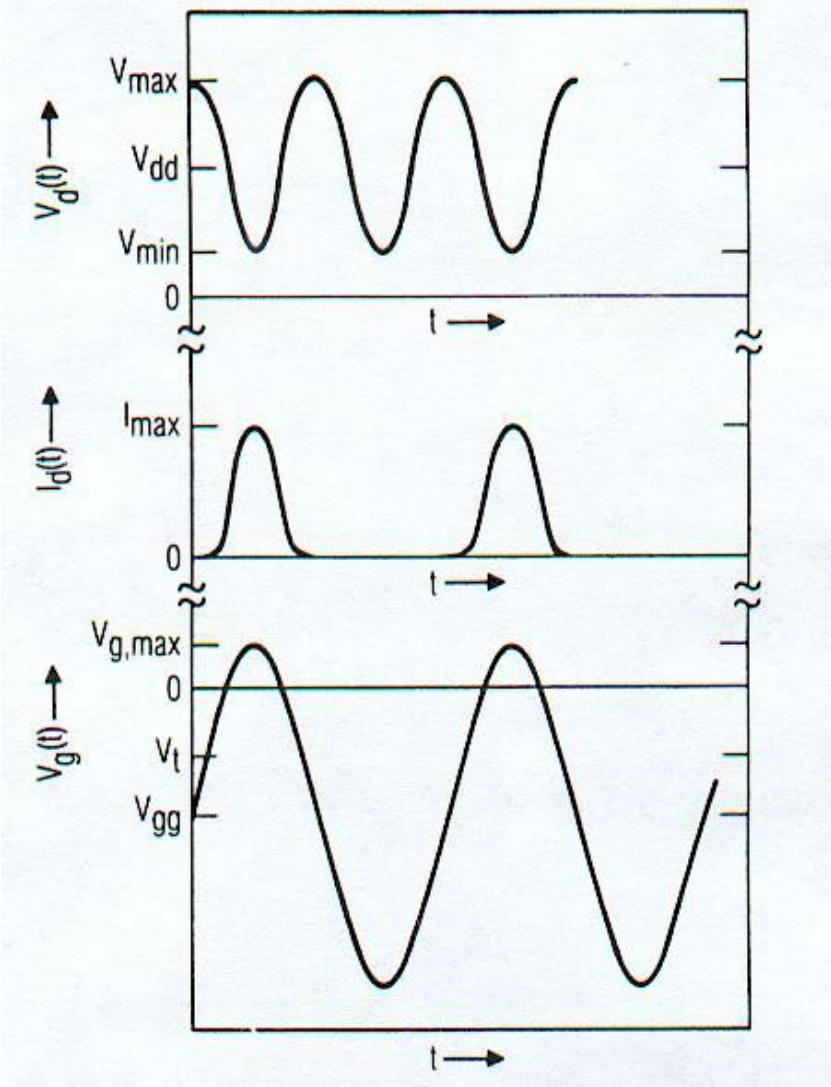
PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

V_{dd}, the dc drain voltage, is halfway between V_{min} and V_{max}.
The load conductance is equal to the slope of the load line

$$G_L = \frac{V_{\max} - V_{\min}}{I_{\max} - I_{\min}}$$

The gate voltage varies between V_{gmax}, the peak gate voltage (limited to 0.5V in MESFETs by rectification in the gate-channel Schottky junction) and $\{ 2V_{gg} - V_{gmax} \}$, a relatively high reverse voltage.

The drain current peaks at the value I_{max}, and the current pulses have the time duration $t_o \leq T/2$ where T is the period of the excitation.



PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

If we make $t = 0$ equal to the point where the current is maximum, the Fourier-series representation of the current has only cosine components

$$I_d(t) = I_o + I_1 \cos(\omega_p t) + I_2 \cos(2\omega_p t) + I_3 \cos(3\omega_p t) + \ldots$$

When $n \geq 1$, the coefficients are

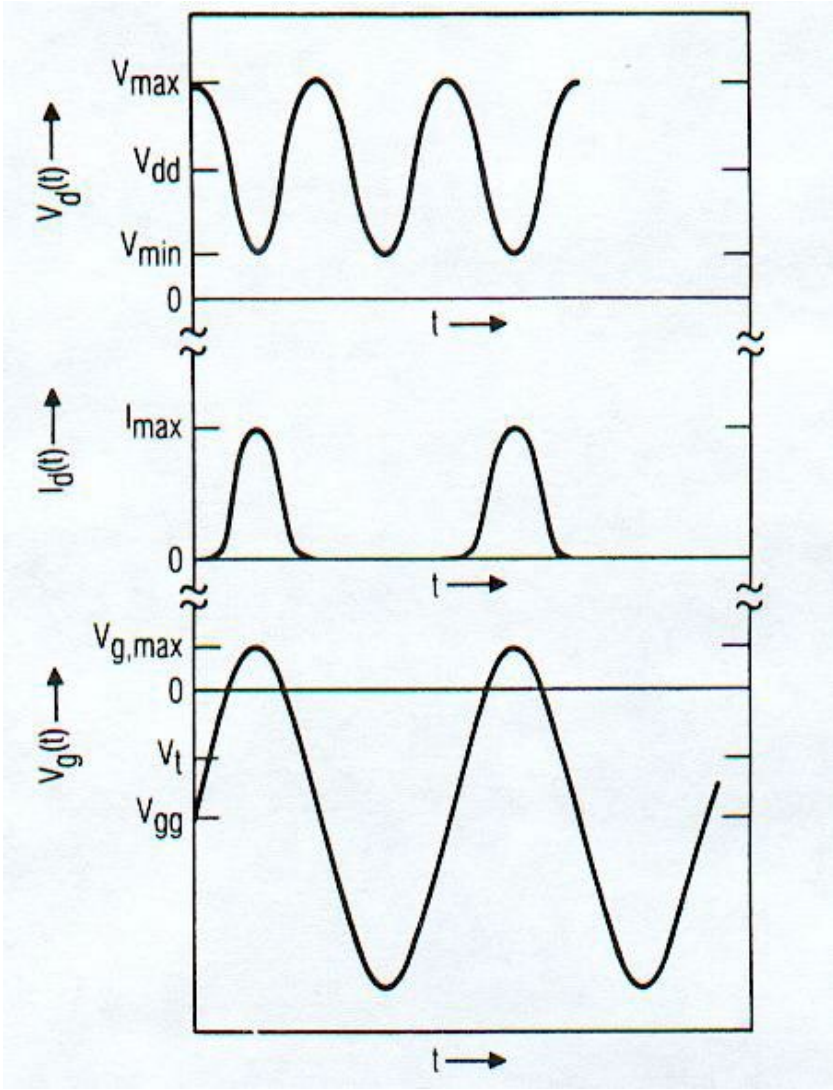
$$I_n = I_{\max} \frac{4t_o}{\pi T} \left| \frac{\cos(n\pi t_o / T)}{1 - (2n t_o / T)^2} \right|$$

and when $n = 0$,

$$I_o = I_{\max} \frac{2t_o}{\pi T}$$

When $\{ t_o/T = 1/2n \}$, $n \neq 0$, the equation is indeterminate. Then

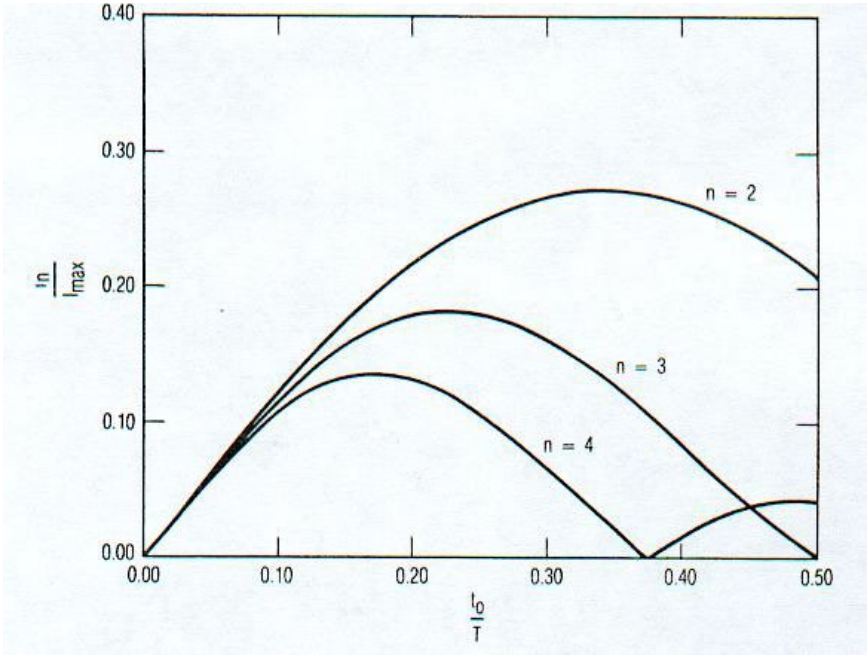
$$I_n = I_{\max} \frac{t_o}{T}$$

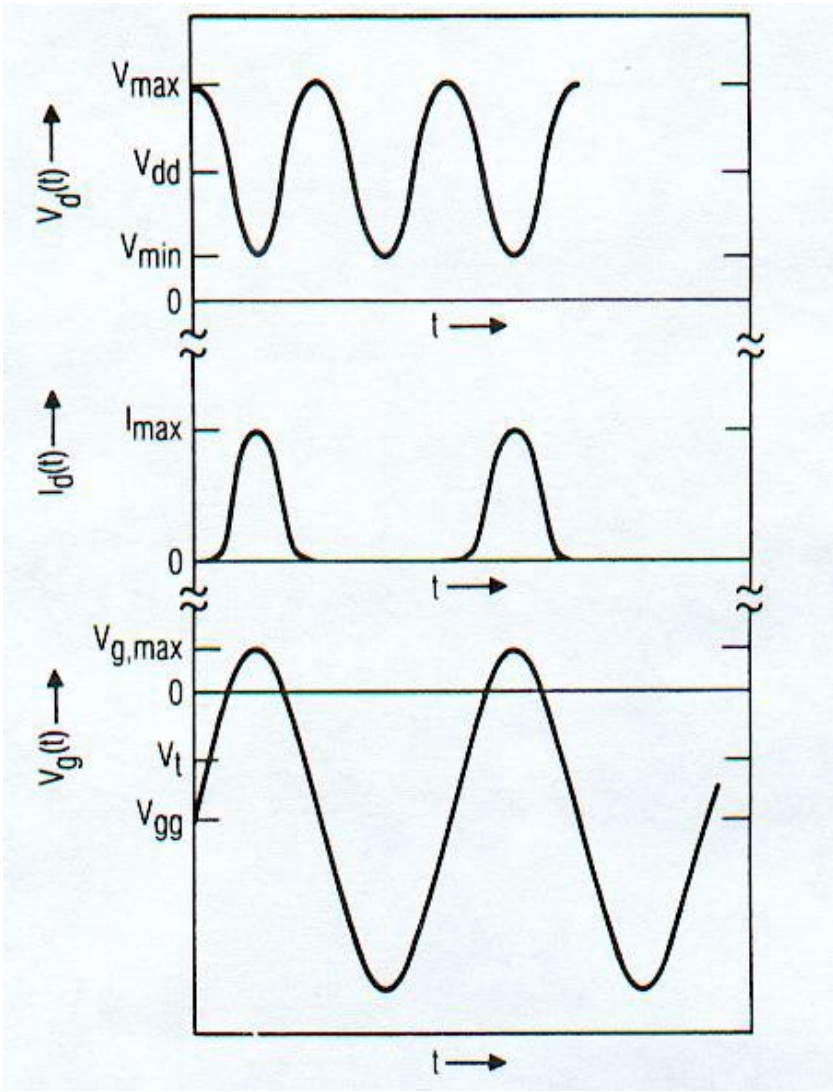


PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

As the current I_n circulates in the load R_L and contributes to output power, we must maximize I_n. To do so, we have only one degree of freedom: varying t_o/T.

The Figure below shows a plot of I_n/I_{max} as a function of t_o/T when n = 2 to 4; each of these curves has a clear maximum below $t_o/T = 0.5$. It would appear that, in order to achieve the optimum value of I_n, we need only to adjust V_{gg} so that $I_d(t)$ has the desired period of conduction t_o.



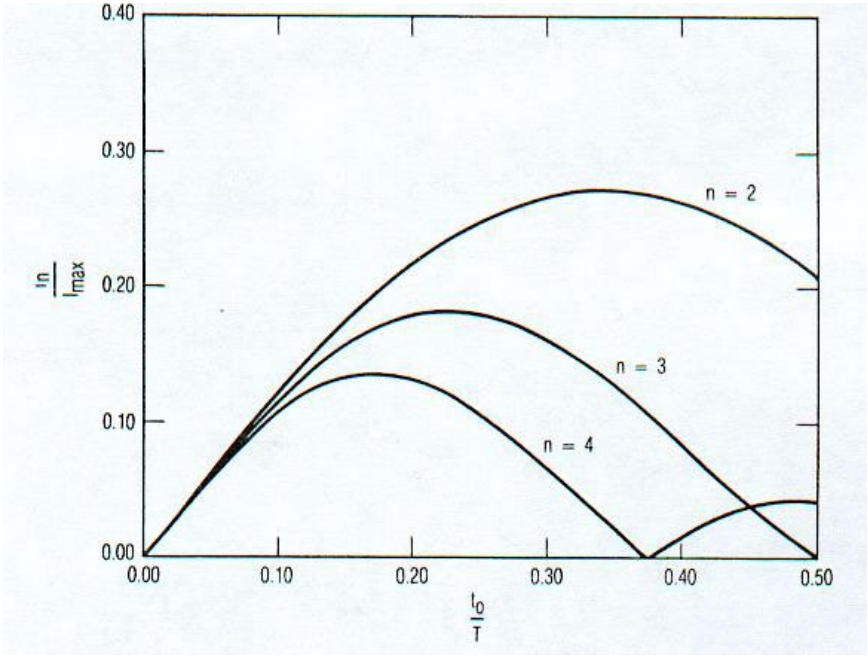


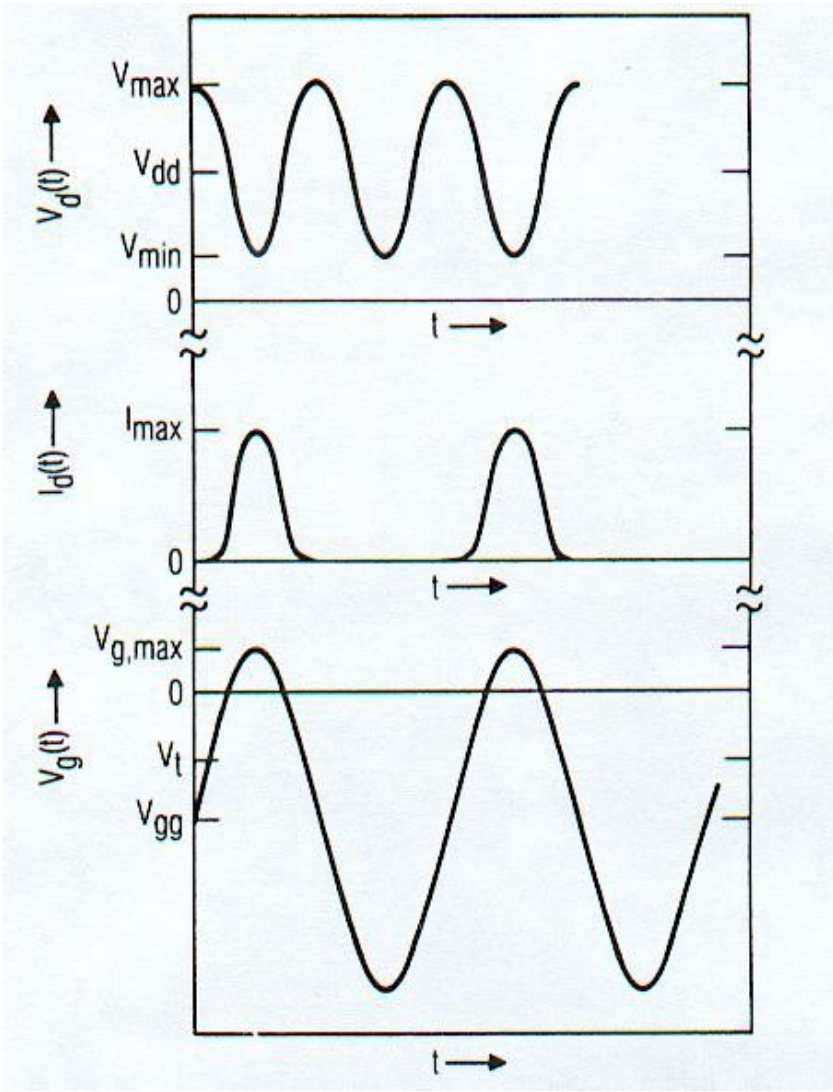
PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

Unfortunately, to achieve a short conduction period we should take into account two aspects:

- $\{ V_{gg} << V_t \}$

but this large bias would make the peak reverse voltage (i.e. $2V_{gg}$) **very large**. As in practical design, the peak drain-gate voltage can be nearly $\{ V_{max} - 2V_{gg} \}$. if V_{gg} is adjusted to make t_o/T small, the peak drain-gate voltage may be **much greater** than the avalanche voltage.

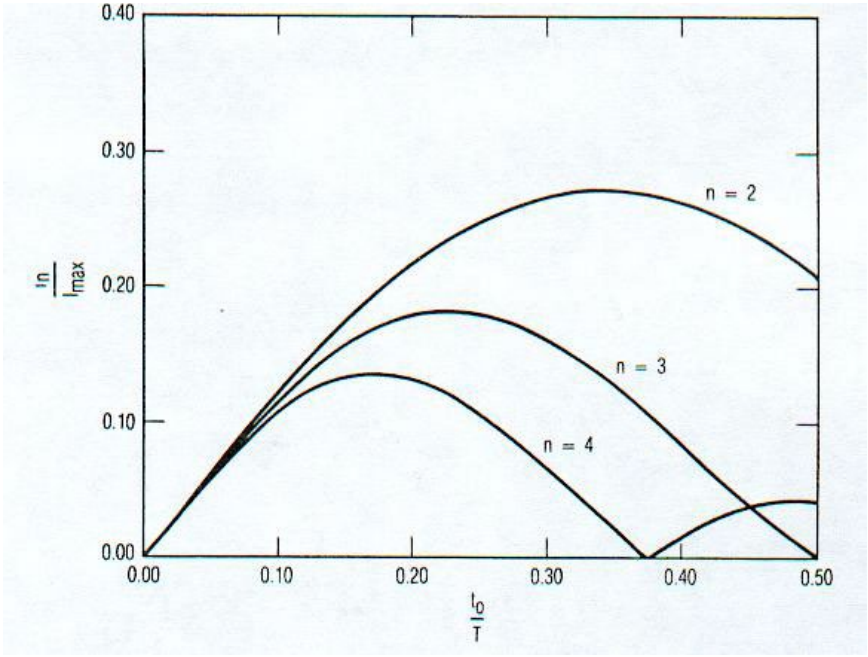


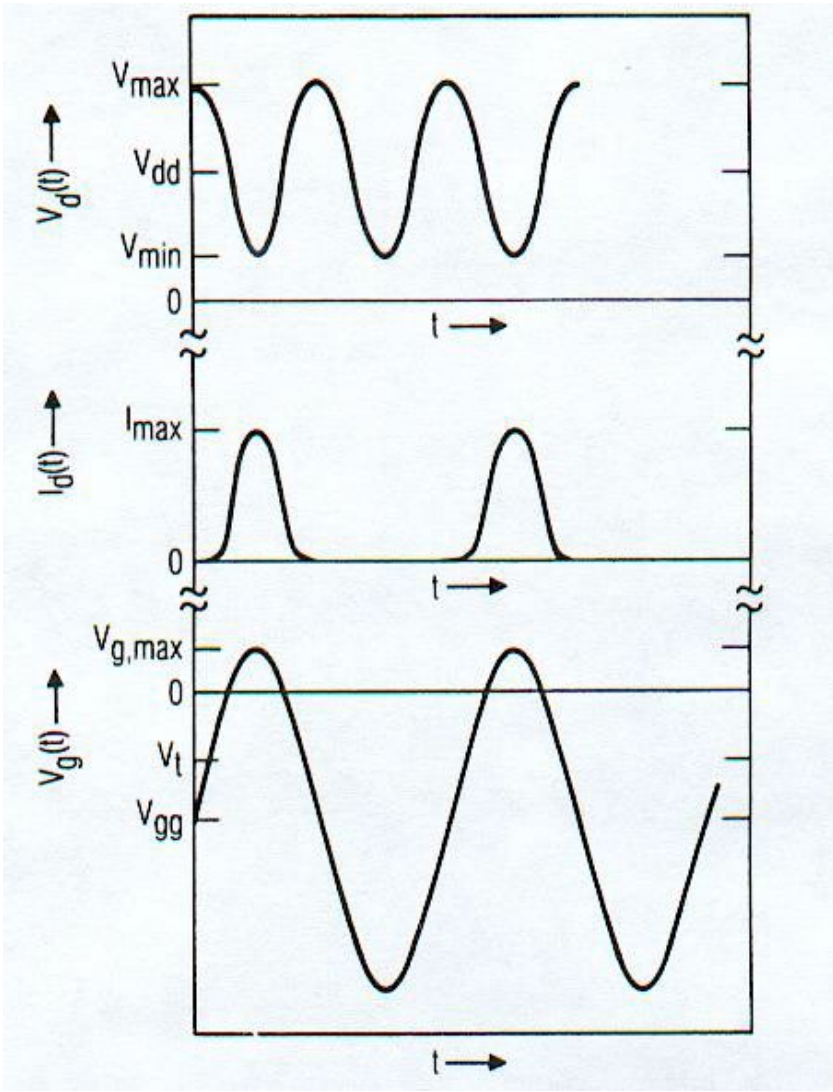


PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

Unfortunately, to achieve a short conduction period we should take into account two aspects:

- In order to achieve an acceptable output power level, the input power should be high (especially for a multiplier having an output harmonic **greater than the second**). The selected t_o/T should be then greater than the optimum value to achieve an acceptable **trade-off between gain and output power**.





PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

The maximum reverse gate voltage that the FET can tolerate establishes one limit on t_o/T. If the gate voltage varies between $V_{g\,max}$ and the peak reverse voltage $V_{g\,min}$, then the phase angle Δt over which $V_g(t) > V_t$ is

$$\theta_t = 2\cos^{-1}\left(\frac{2V_t - V_{g\,max} - V_{g\,min}}{V_{g\,max} - V_{g\,min}}\right)$$

and the optimum load resistance is

$$R_L = \frac{V_{\max} - V_{\min}}{2I_n}$$

Because I_n is relatively small compared to the current I_1 in a Class-B amplifier, R_L in a multiplier is usually much larger. The output power P_{Ln} at the n^{th} harmonic is

$$P_{Ln} = \frac{1}{2}I_n^2 R_L = \frac{1}{2}I_n \frac{V_{\max} - V_{\min}}{2}$$

PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

As with a power amplifier, the dc drain bias voltage is halfway between V_{max} and V_{min}; that is

$$V_{gg} = \frac{V_{g\,max} + V_{g\,min}}{2} \qquad V_{dd} = \frac{V_{\max} + V_{\min}}{2}$$

$$\Rightarrow \quad P_{dc} = V_{dd}\, I_{dc} = V_{dd}\, I_o \qquad P_{dc} = V_{dd}\, I_{d\,max}\, \frac{2\,t_o}{\pi\, T}$$

and the dc-RF efficiency is

$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}}$$

If the source is matched, the power available from the source must equal P_{in}:

$$P_{av} = P_{in} = \frac{1}{2}\left(V_{g\,\max} - V_{gg}\right)^2 \omega_p^2\, C_{gs}^2 \left(R_s + R_i + R_g\right)$$

The conversion gain G_c is equal to

$$G_c = \frac{P_{Ln}}{P_{av}}$$

PRACTICAL FET FREQUENCY MULTIPLIER DESIGN

For a matched input, this gain is the power gain G_p

$$G_p = \frac{P_{Ln}}{P_{in}}$$

Therefore, as the power-added efficiency of a FET multiplier is

$$\eta_a = \frac{P_{Ln} - P_{in}}{P_{dc}}$$

The power gain is related to the power-added efficiency by

$$\eta_a = \eta_{dc}\left(1 - \frac{1}{G_p}\right)$$

Working Example

WORKING EXAMPLE

We wish to design a FET doubler 10 to 20 GHz. The FET has the following parameters:

$V_a = 12.0$ V		$V_t = -2.0$ V
$R_s = 2.0\ \Omega$		$R_i = 2.0\ \Omega$
$R_g = 1.0\ \Omega$		$R_d = 2.0\ \Omega$
$I_{dss} = 80$ mA	at	$V_{ds} = 3.0$ V
$C_{gs} = 0.25$ pF	at	$V_{gs} = V_{gg}$
$C_{gd} = 0.08$ pF		$C_{ds} = 0.10$ pF
$L_s = 0.005$ nH		

We use the Cubic Curtice model of I_d $$I_d = (A_0 + A_1 V + A_2 V^2 + A_3 V^3) \tanh (\alpha V_{ds})$$

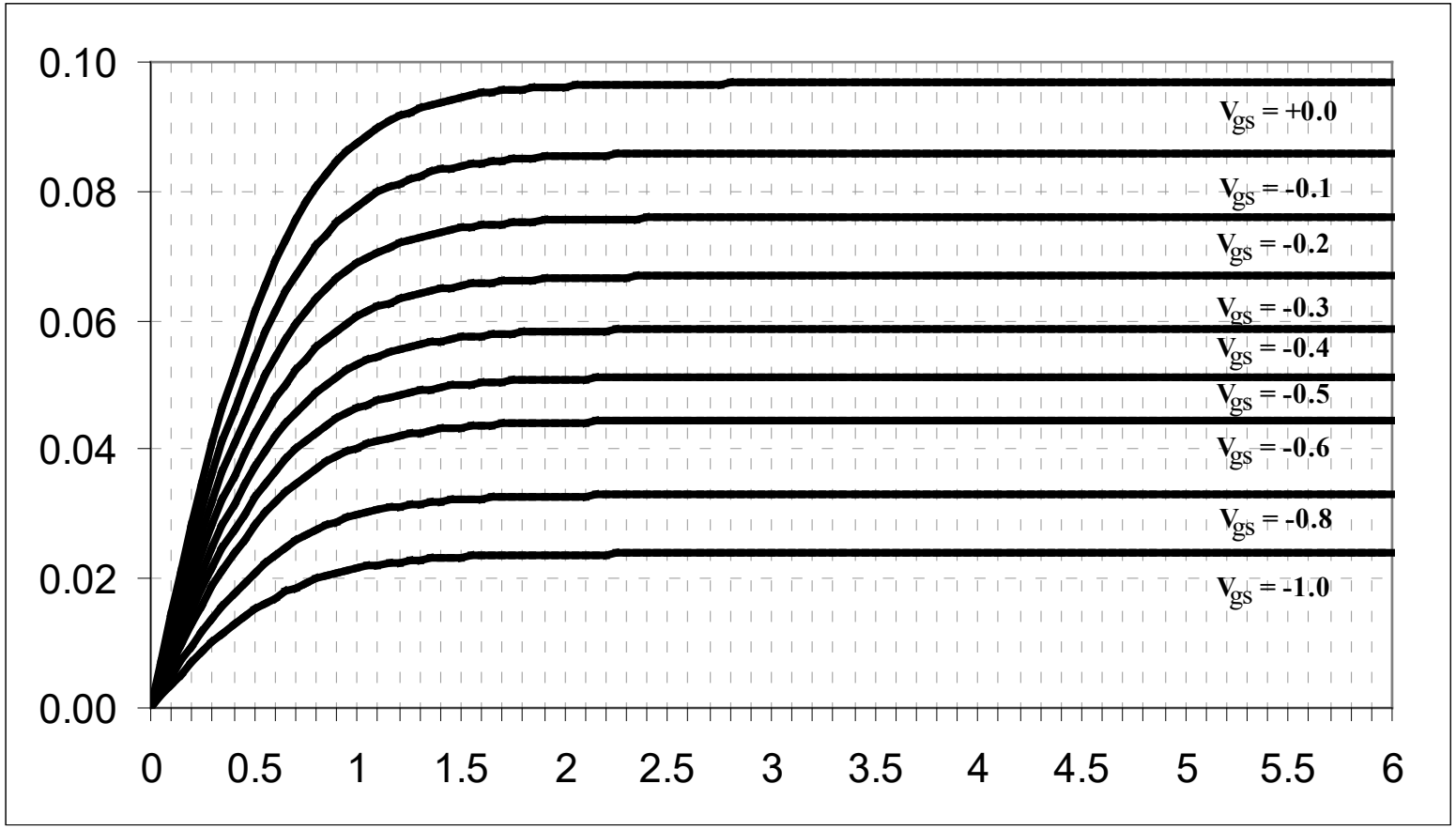
where the parameters are (for $\beta = 0$)

$A_o = 0.09670$ $A_1 = 0.11334$ $A_2 = 0.04853$ $A_3 = 0.00801$ $\alpha = 1.5$

Step 1- Find the device operating parameter values:

From the I-V curves, we estimate

$I_{max} \approx I_{dss} = 80$ mA and $V_{min} = 1.0$V (the value at the knee).



Step 1- Find the device operating parameter values:

V_{gmin} and V_{max} must obey the constraint

$$V_{\max} - V_{g\min} < V_a = 12V$$

so we can choose V_{gmin} = -7.0V and V_{max} = 5.0V.

We also choose V_{gmax} = 0.2V, slightly below the lowest value that allows rectification.

$$V_{gg} = \frac{V_{g\,max} + V_{g\,min}}{2} = \frac{0.2 - 7}{2} = -3.4V \qquad V_{dd} = \frac{V_{\max} + V_{\min}}{2} = \frac{5.0 + 1.0}{2} = 3V$$

$$\theta_t = 2\cos^{-1}\left(\frac{2V_t - V_{g\,max} - V_{g\,min}}{V_{g\,max} - V_{g\,min}}\right) = 2\cos^{-1}\left(\frac{2*(-2.0) - 0.2 - (-7.0)}{0.2 - (-7.0)}\right)$$

$$\theta_t = 2\cos^{-1}(0.388) = 134.4^{\circ} \quad \text{or} \quad 2.36\,\text{rd} \qquad \frac{t_o}{T} = \frac{134.4}{360} = 0.37$$

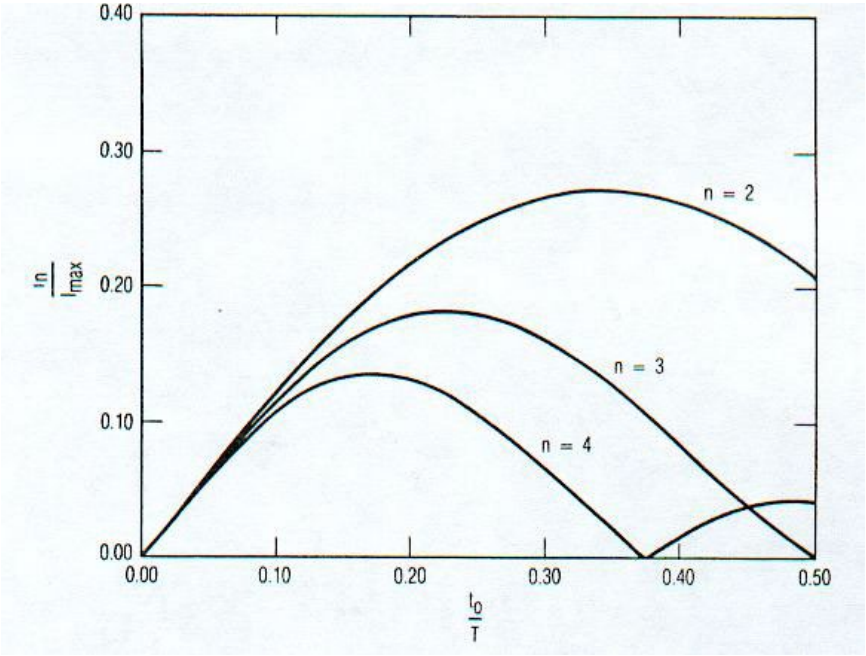
Step 1- Find the device operating parameter values:

$$\frac{t_o}{T} = \frac{134.4}{360} = 0.37$$

This value is close to the optimum value for a doubler ($n = 2$)

$$I_2 = I_{d\,max}\frac{4t_o}{\pi T}\left|\frac{\cos(2\pi t_o/T)}{1-(4t_o/T)^2}\right| = I_{d\,max}\frac{4}{\pi}0.37\left|\frac{\cos(2\pi 0.37)}{1-(4*0.37)^2}\right| = I_{d\,max}\,0.471*\frac{0.68}{1.19}$$

$$I_2 = 0.269\,I_{d\,max} = 21.6\ \text{mA}$$



The dc drain current is given by

$$I_o = I_{d\,max}\frac{2t_o}{\pi T} = 80*\frac{2}{\pi}*0.37 = 19\ \text{mA}$$

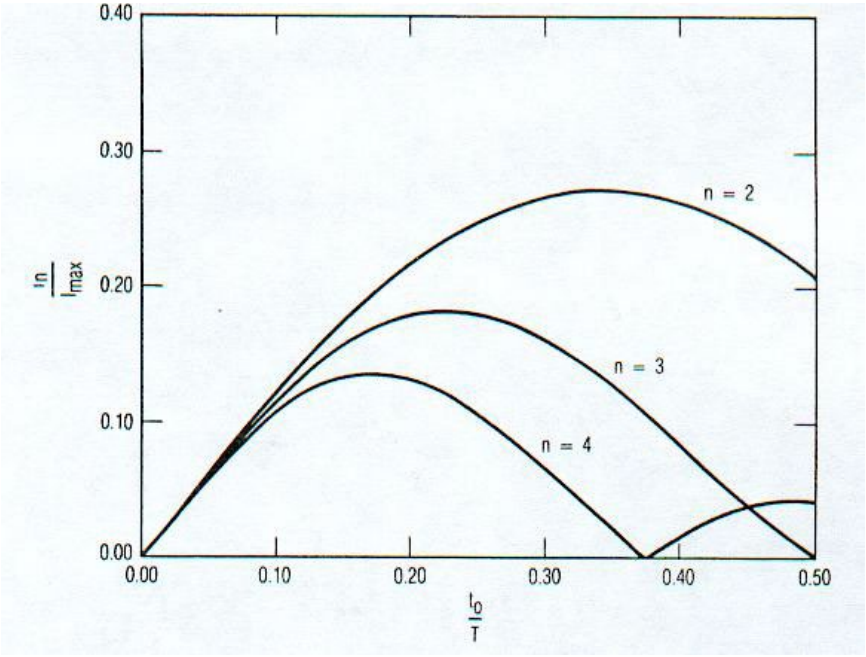
Step 2- Determine the circuit parameters:

$$P_{in} = \frac{1}{2}(3.6)^2 \left(2 * \pi * 10^{10}\right)^2 \left(0.25 * 10^{-12}\right)^2 (5)$$

$$P_{in} = 6.48 * 3.947 * 10^{21} * 6.25 * 10^{-26} * 5 = 7.99 \text{ mW} \approx 8 \text{ mW} \quad \text{or} \quad 9.0\,\text{dBm}$$

$$P_{L2} = \frac{1}{2} I_2^2 R_L = \frac{1}{2} I_2 \frac{V_{d\,max} - V_{d\,min}}{2} = \frac{1}{2} 21.6 \frac{5.0 - 1.0}{2} = 21.6 \text{ mW} \quad \text{or} \quad 13.3\,\text{dBm}$$

Thus the conversion gain is



$$G_c = \frac{P_{Ln}}{P_{av}} = \frac{P_{Ln}}{P_{in}} = \frac{21.6}{8} = 2.7 \quad \text{or} \quad 4.3\,\text{dB}$$

The dc power is equal to

$$P_{dc} = V_{dd}\, I_o = 3 * 19 = 57 \text{ W}$$

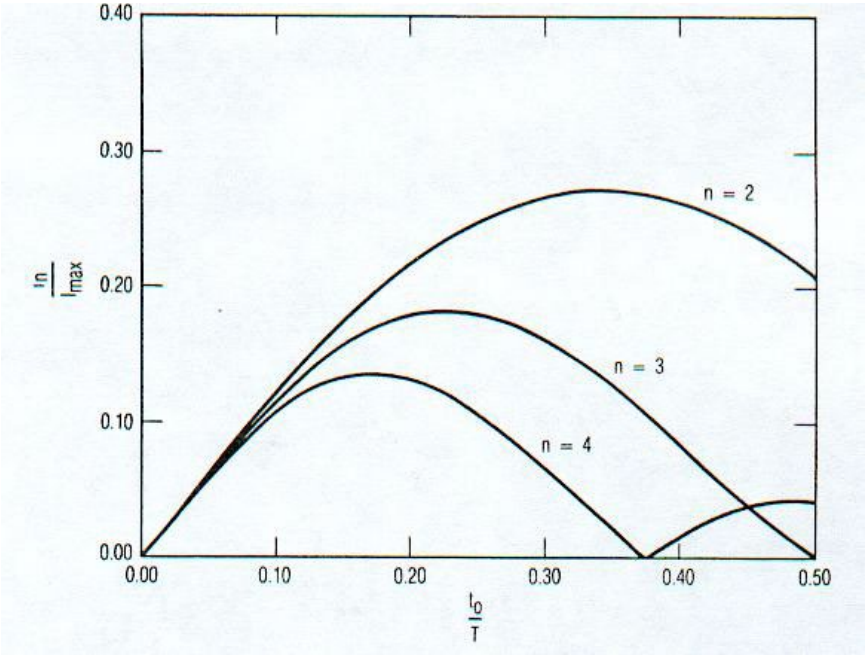
The dc-RF efficiency is then

$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}} = \frac{21.6}{57} = 38\%$$

Step 2- Hint : How to choose V_{gmin} and V_{max}:

This choice is not subjective but based on the following constraints:

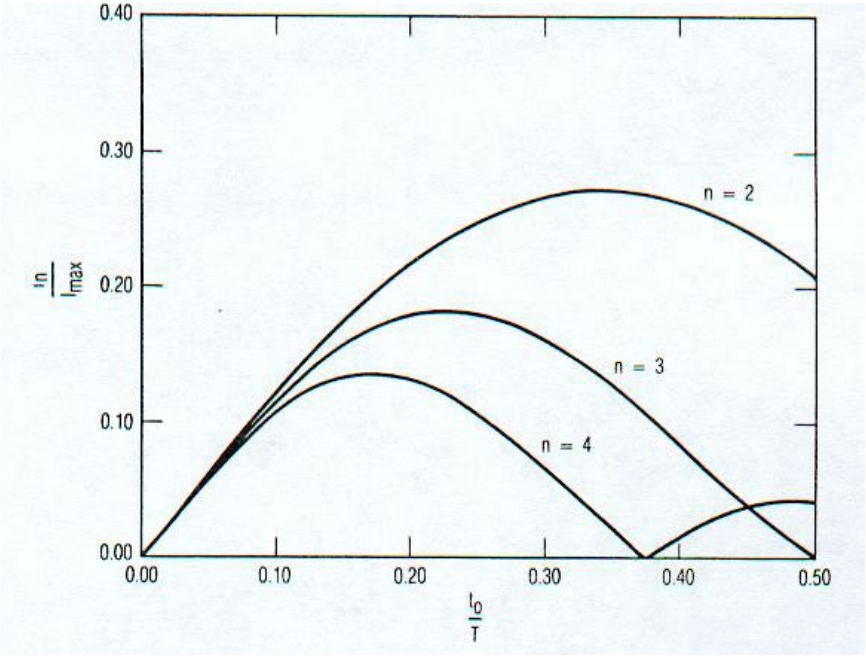
- The *I-V* characteristics limits
- The predicted value of t_o/T must be close to the optimum value.
- The bias drain current that must be approximately equal to $I_{dss}/2$ (i.e., middle of the load line).



Step 2- Hint : How to choose V_{gmin} and V_{max}:

However, as the initial values require some experience to estimate, a designer can also use the following procedure:

- Select the optimum value of t_o/T. Here for the doubler: $n = 2$ gives $t_o / T = 0.37$.
- Note the corresponding value of $I_n / I_{max} = I_2 / I_{max} = 0.27$.



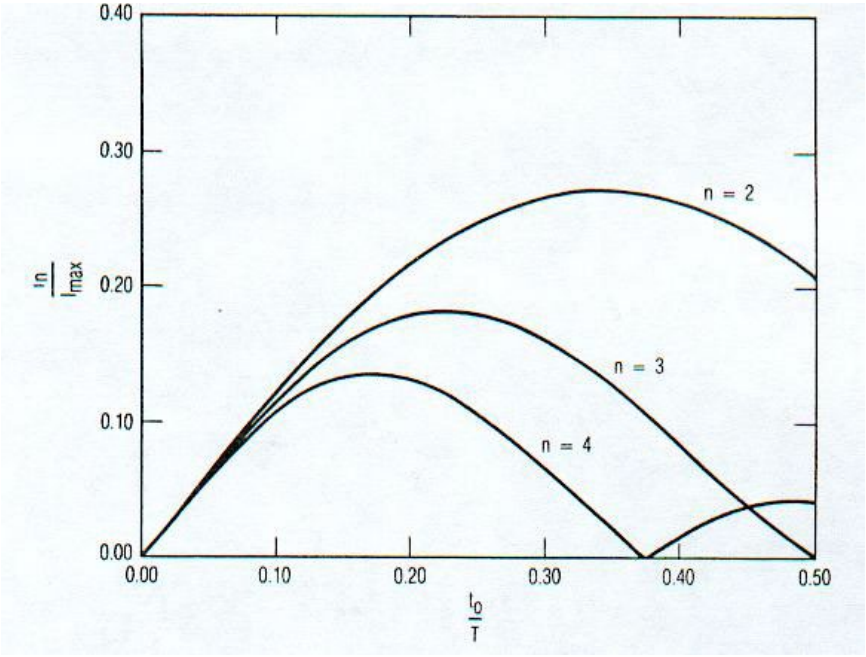
Step 2- Hint : How to choose V_{gmin} and V_{max}:

- Deduce the I_n value:

$$I_n = I_2 = 0.27 * I_{max} = 0.27 * I_{dss} = 0.27 * 80 = 21.6 \text{ mA}$$

- Estimate the V_{gmin} voltage knowing that $V_{gmax} = 0.2\text{V}$ and $V_{min} = 1\text{V}$ are good approximations for almost all FETs

$$\cos\left(\frac{134.4^\circ}{2}\right) = \frac{2V_t - V_{g\,max} - V_{g\,min}}{V_{g\,max} - V_{g\,min}} = \frac{2*(-2) - 0.2 - V_{g\,min}}{0.2 - V_{g\,min}}$$



Step 2- Hint : How to choose V_{gmin} and V_{max}:

Therefore: V_{gmin} = -7.0V

- Deduce the V_{max} voltage:

$$V_{\max} - V_{g\min} < V_a = 12\ \text{V}$$

$$V_{max} = 5.0\ \text{V}$$

- Determine the bias voltages V_{gg} and V_{dd}:

$$V_{gg} = \frac{V_{g\max} + V_{g\min}}{2} = \frac{0.2 - 7}{2} = -3.4\ \text{V} \qquad V_{dd} = \frac{V_{\max} + V_{\min}}{2} = 3\ \text{V}$$

- Obtain the dc drain current

$$I_o = I_{\max} \frac{2t_o}{\pi T} = 80 * \frac{2}{\pi} * 0.37 = 19\ \text{mA}$$

→ Determine the circuit parameters

Step 3- Determine the circuit parameters:

$$P_{in} = \frac{1}{2}(3.6)^2 \left(2*\pi*10^{10}\right)^2 \left(0.25*10^{-12}\right)^2 (5) \approx 8\ \text{mW} \quad \text{or} \quad 9.0\ \text{dBm}$$

$$P_{L2} = \frac{1}{2} I_2^2 R_L = \frac{1}{2} I_2 \frac{V_{\max} - V_{\min}}{2} = 21.6\ \text{mW} \quad \text{or} \quad 13.3\ \text{dBm}$$

$$G_c = \frac{P_{Ln}}{P_{av}} = \frac{P_{Ln}}{P_{in}} = \frac{21.6}{8} = 2.7 \quad \text{or} \quad 4.3\ \text{dB}$$

$$P_{dc} = V_{dd}\ I_o = 3*19 = 57\ \text{W}$$

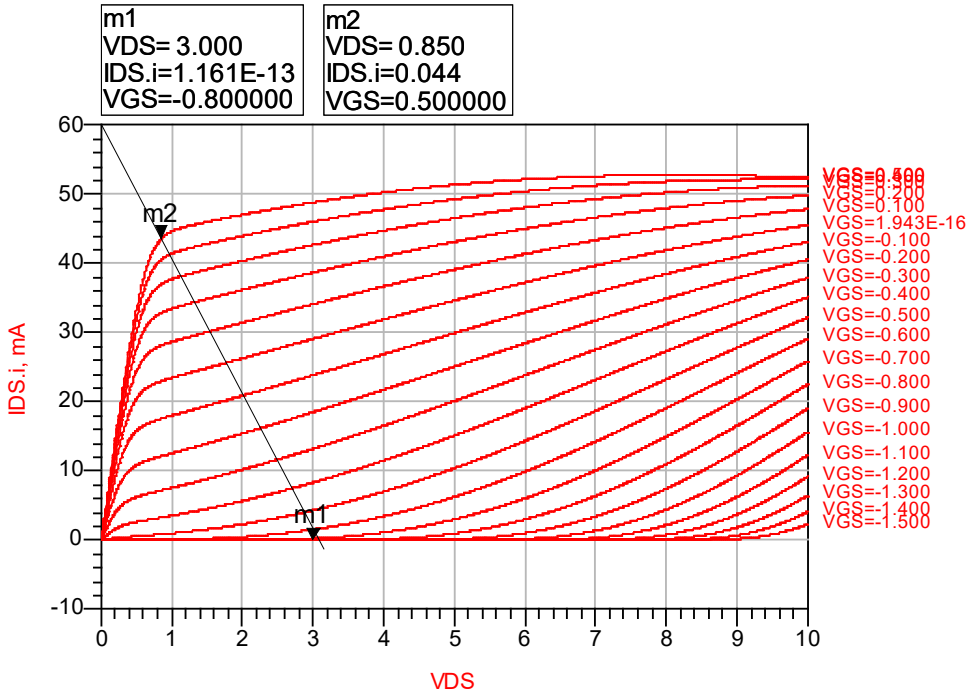
$$\eta_{dc} = \frac{P_{Ln}}{P_{dc}} = \frac{21.6}{57} = 38\%$$

$$R_L = \frac{V_{d\,max} - V_{d\,min}}{2\,I_n} = \frac{5.0 - 1.0}{2*21.6*10^{-3}} = 92.6\,\Omega$$

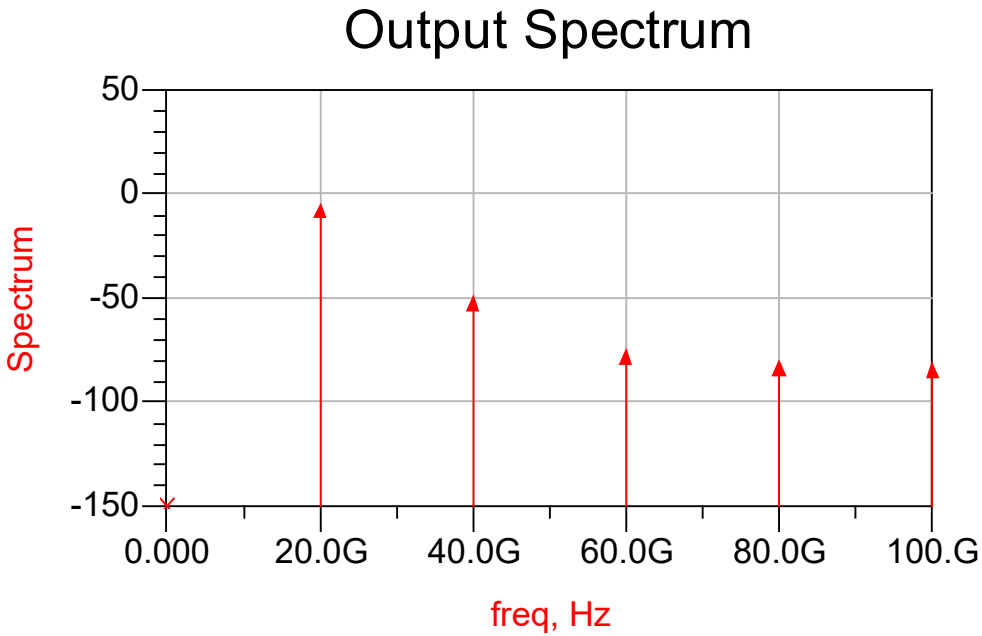
$$Z_{in}(\omega_p) = R_s + R_i + R_g + \frac{1}{j\,\omega_p\,C_{gs}} = (5 - j\,63)\Omega$$

$$Z_L(2\omega_p) = \frac{1}{(1/92.6) - j\,12.5*10^{-3}} = (39.5 + j\,46.2)\Omega$$

Designing a 20-40 GHz doubler



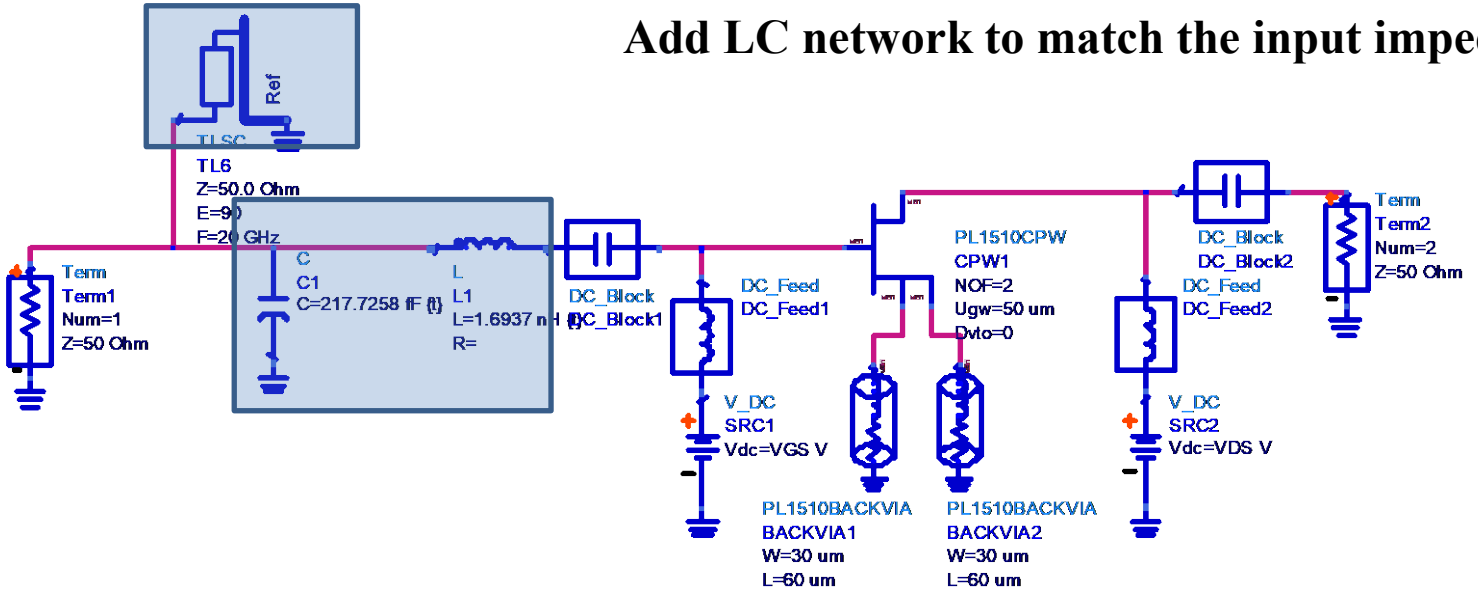
$$V_{dd} = \frac{V_{dmax} + V_{dmin}}{2} = \frac{3 + 0.85}{2} = 1.925V$$



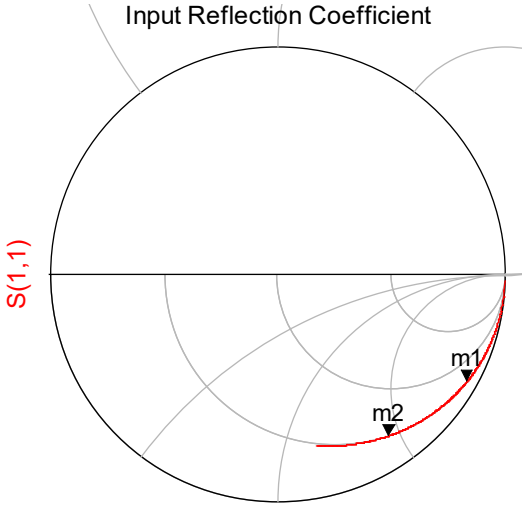
Output Power at 40 GHz is very low.

Matching is needed.

Add LC network to match the input impedance to 50 Ω

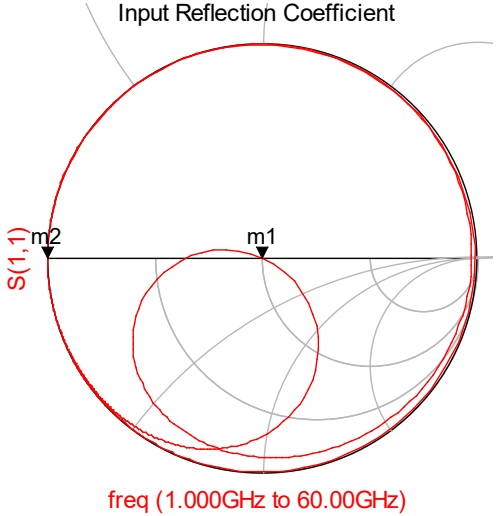


Before Matching



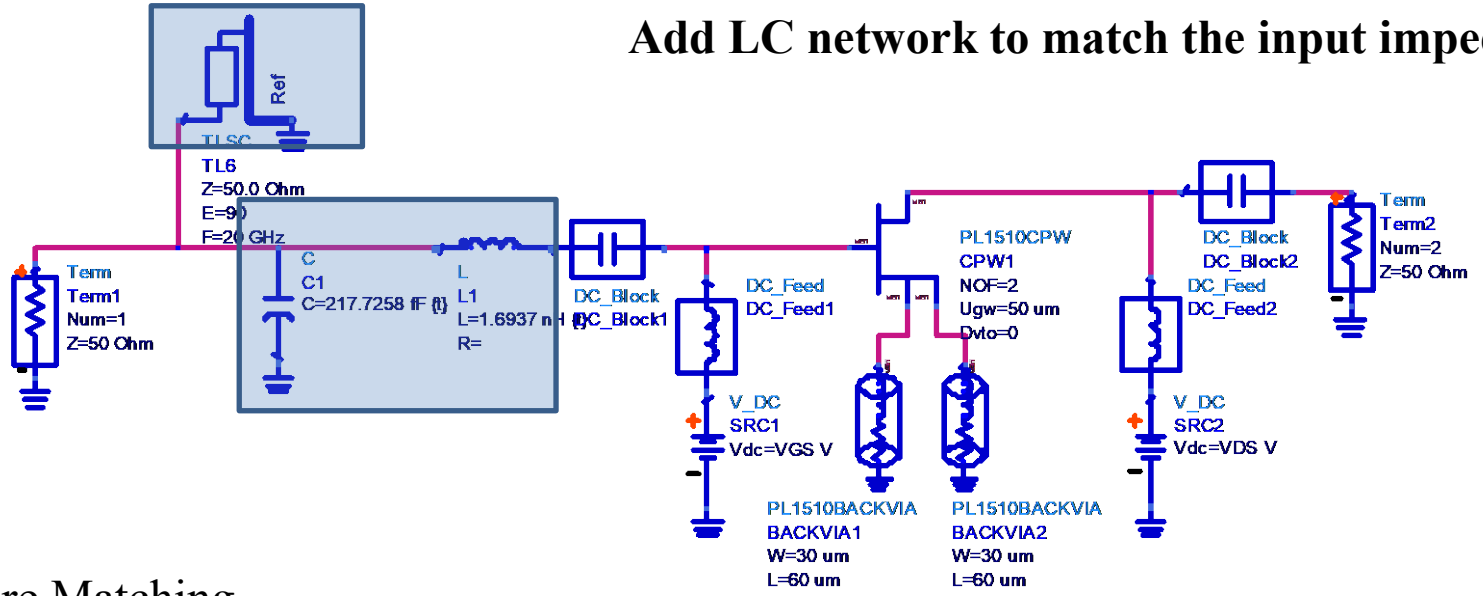
m1	m2
freq=20.00GHz S(1,1)=0.956 / -29.411 impedance = 17.413 - j189.015	freq=40.00GHz S(1,1)=0.861 / -55.369 impedance = 16.945 - j92.888

After Matching



m1	m2
freq=20.00GHz S(1,1)=3.324E-5 / -7.094 impedance = 50.003 - j4.105E-4	freq=40.00GHz S(1,1)=1.000 / -180.000 impedance = 2.500E-9 - j2.833E-14

Add LC network to match the input impedance to 50 Ω

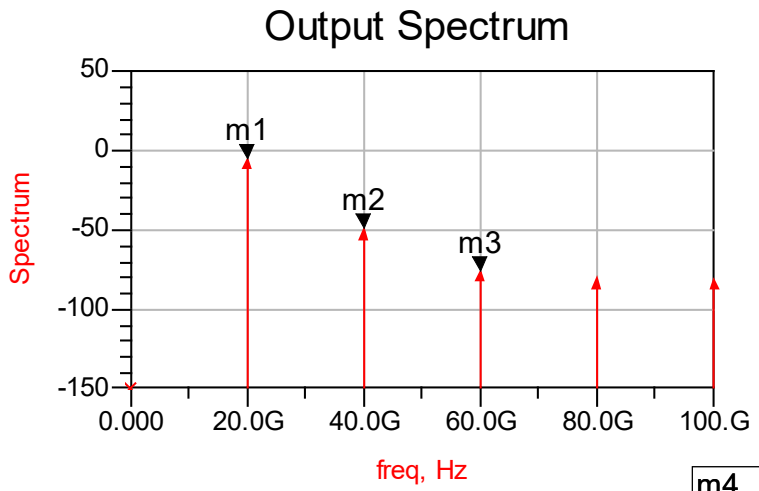


Before Matching

m1
freq=20.00GHz
Spectrum=-5.561

m2
freq=40.00GHz
Spectrum=-49.630

m3
freq=60.00GHz
Spectrum=-75.920



Output power at 2nd and 3rd harmonic has been significantly improved.

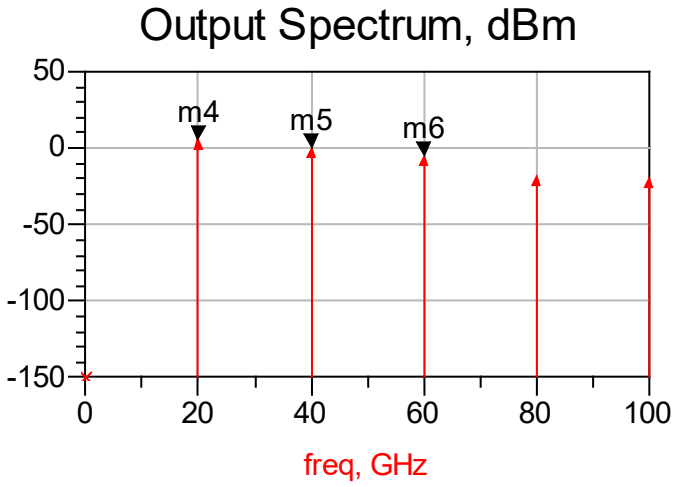
Further matching at output is needed to make the second harmonic overpowering.

After Matching

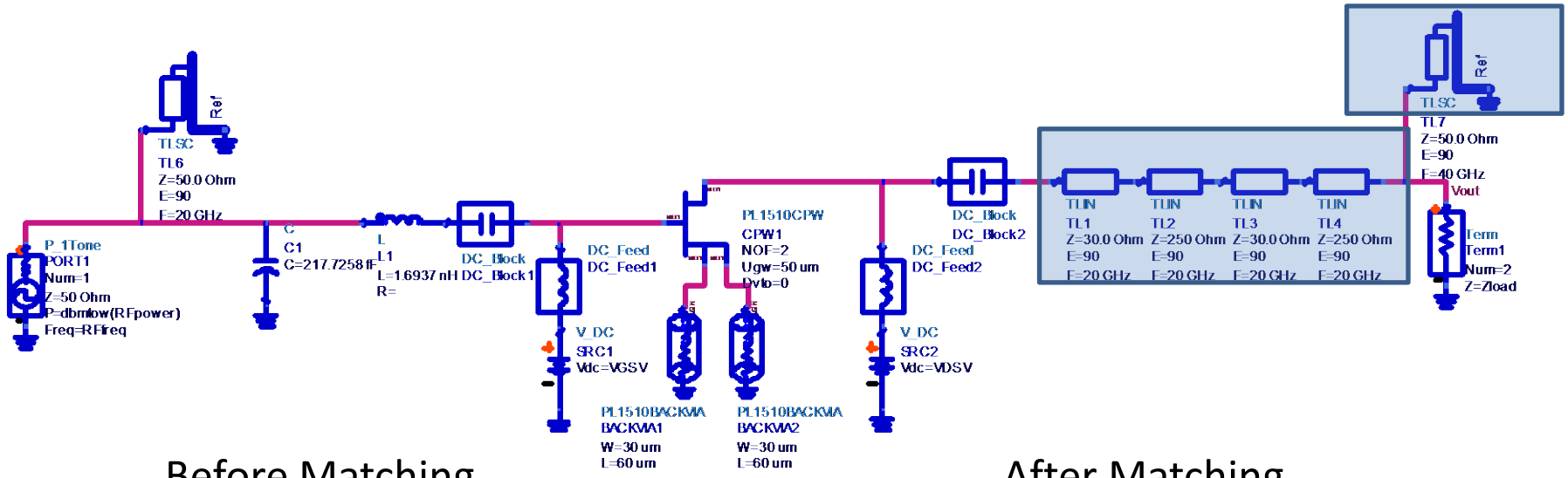
m4
freq=20.00GHz
Spectrum[m3,::]=5.744

m5
freq=40.00GHz
Spectrum[m3,::]=-0.125

m6
freq=60.00GHz
Spectrum[m3,::]=-5.426

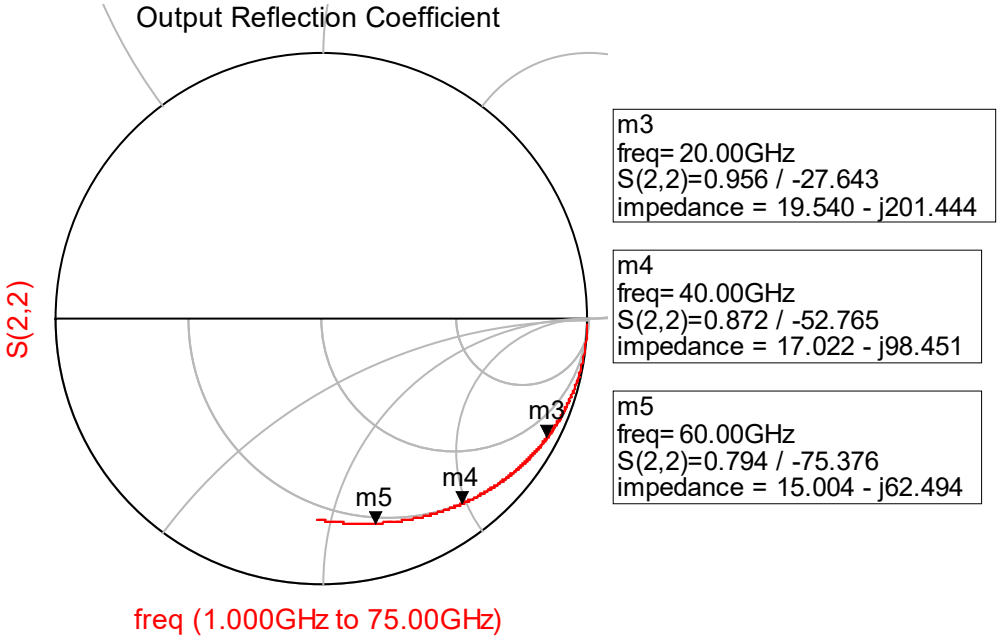


Add a series of transmission line with high and low impedance as a half wave filter at the output



Before Matching

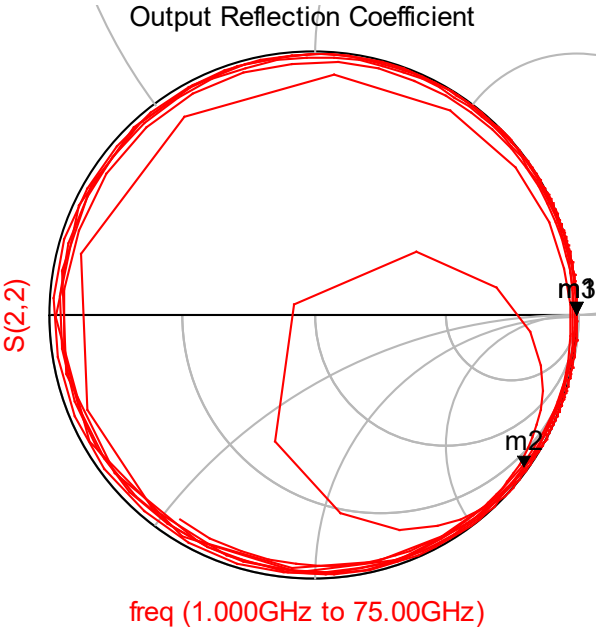
After Matching



m3
freq= 20.00GHz
S(2,2)=0.956 / -27.643
impedance = 19.540 - j201.444

m4
freq= 40.00GHz
S(2,2)=0.872 / -52.765
impedance = 17.022 - j98.451

m5
freq= 60.00GHz
S(2,2)=0.794 / -75.376
impedance = 15.004 - j62.494

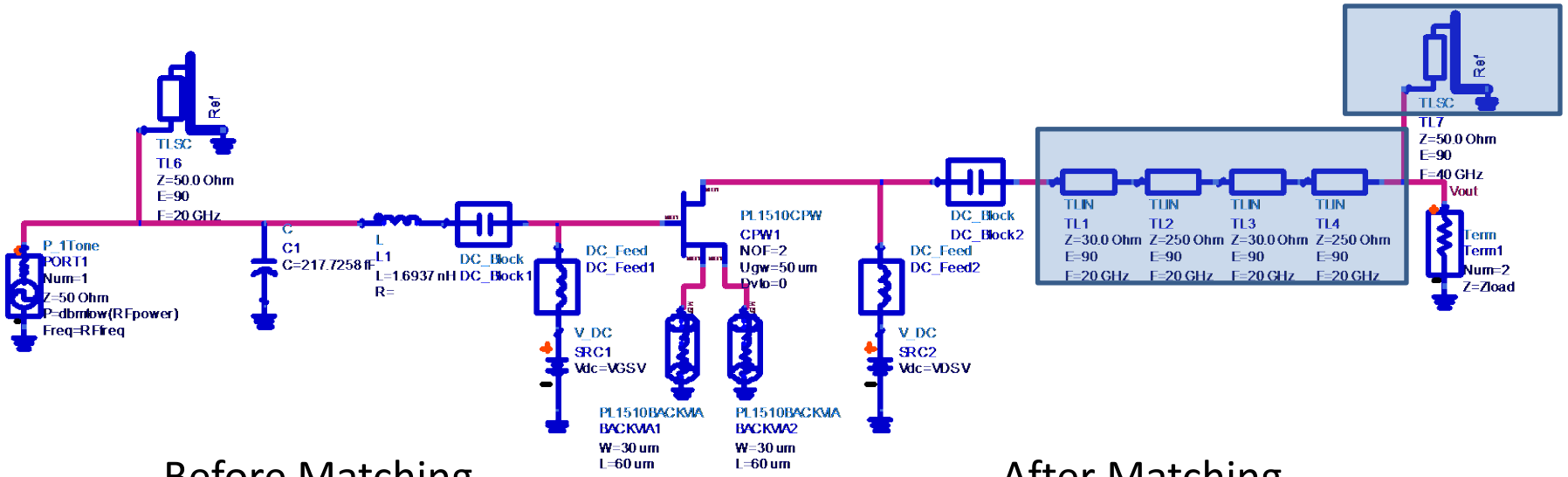


m1
freq=20.00GHz
S(2,2)=1.000 / -0.002
impedance = 3.618E5 - j5.424E4

m2
freq=40.00GHz
S(2,2)=0.986 / -36.095
impedance = 3.627 - j153.373

m3
freq=60.00GHz
S(2,2)=1.000 / -0.014
impedance = 1.243E4 - j4.200E5

Add a series of transmission line with high and low impedance as a half wave filter at the output



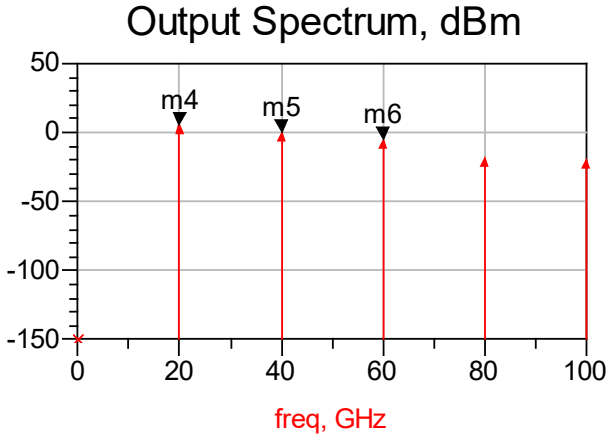
Before Matching

After Matching

m4
freq=20.00GHz
Spectrum[m3,::]=5.744

m5
freq=40.00GHz
Spectrum[m3,::]=-0.125

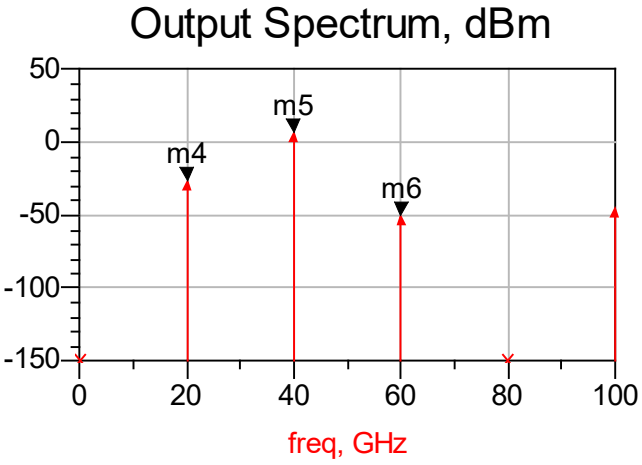
m6
freq=60.00GHz
Spectrum[m3,::]=-5.426



m4
freq=20.00GHz
Spectrum[m3,::]=-26.419

m5
freq=40.00GHz
Spectrum[m3,::]=6.521

m6
freq=60.00GHz
Spectrum[m3,::]=-50.295



Thank you !

End of Chapter 5