

Transistor Modeling Assignment

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Abstract and Background

In this document, the simulation of the EPA018 High Efficiency Hetrojunction Power FET from Excelics will be presented. The simulation engine used is ADS from Keysight. Both the small signal and large signal model of this transistor will be simulated. The results from this simulation are mixed. The small signal model and IV curves match fairly well with what is printed in the datasheet. However the large signal S parameters show some inconsistencies from what is in the datasheet. The main inconsistency being the simulated power added efficiency of 0.4% vs the datasheet value of 48%.

Academic Integrity, LLMs and Licensing

The work done in this simulation assignment was done in full by the author (Nick Cardamone) and the author takes full responsibility for the claims made in this document. The plots shown in this document were generated by scripts which were written mostly by a LLM (chat gpt). Those scripts have since been verified to be accurate. Even so, there are always errors in any piece of software and there is always a chance of errors in the scripts used in plotting for this assignment.

The scripts used in the assignment have been open sourced under an MIT license and can be found at the following github repo and at [1]. The simulation files used can also be found there as well for future reference.

<https://github.com/ncardamone10/Nonlinear-Microwave-Modeling/tree/main/Assignment>

Simulation Overview

The simulator in used to generate the data which will be presented in this document is ADS from Keysight. The general steps that have been followed for each section are as follows

1. Model circuit in ADS
2. Set up simulation settings
3. Look at simulation results in ADS, do a sanity check
4. Export results from ADS to a txt file
5. Format exported data into an excel spreadsheet with a python script
6. Manipulate and plot the data from the excel spreadsheet in python

Python scripting has been used to do plotting as it gives better plot quality than ADS and 3D plots can be helpful to understand the results obtained from the simulator. All the python scripts and data used in this document are available at [1]

Chosen Transistor

The transistor used in this simulation assignment is the EPA018A High Efficiency Hetrojunction Power FET from Excelics. The datasheet for it can be found at [2]

Note*: Excelcis has since gone out of business/ been bought by another company and it is difficult to find information on the transistor used in this simulation assignment. The datasheets have been posted to the repository in [1]

Small Signal Model

The following is the small signal model that has been used to simulate the S parameters. The datasheet giving the numerical parameters can be found in [3]. Even though it is not explicitly mentioned, it appears that this data has incorporated the bond wires used on the die to get to external pads which can be used for probing.

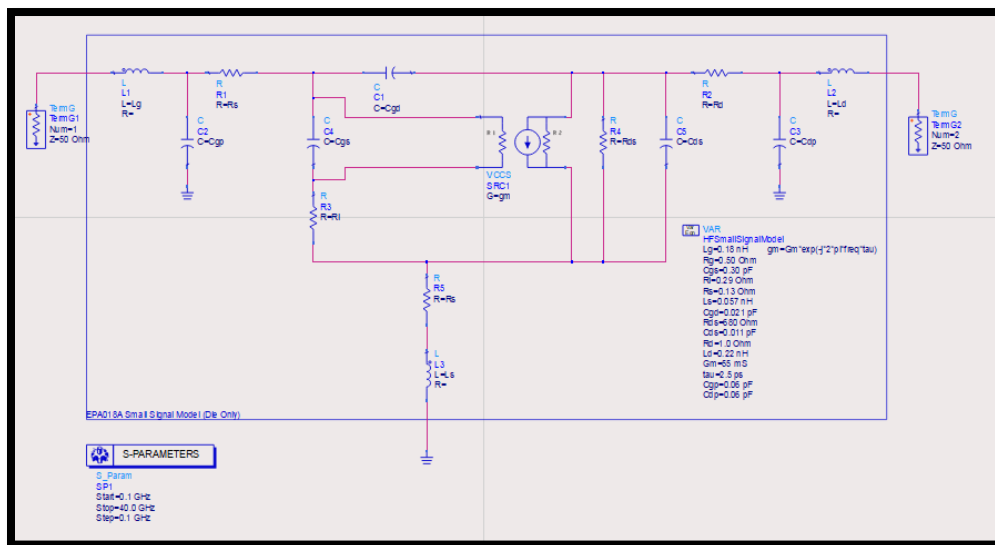


Figure 1: Small Signal Model Used in S Parameter Simulation (No Parasitics)

Small Signal Model with Packaging Parasitics

The following was used to find the S Parameters while considering the packaging parasitics. Going forward, if parasitics are mentioned, it is implied that it means the parasitics to do packing the FET. The numerical values used in this model can be found at [4]. The 70 mil package parasitics were used since that would be the typical package for this transistor if it was used in a real product. The datasheet given in [2] specifies dimensions in microns which means it isn't taking packaging into consideration. It will be seen later that the data given in the datasheet does not match up with the simulated data when parasitics are included

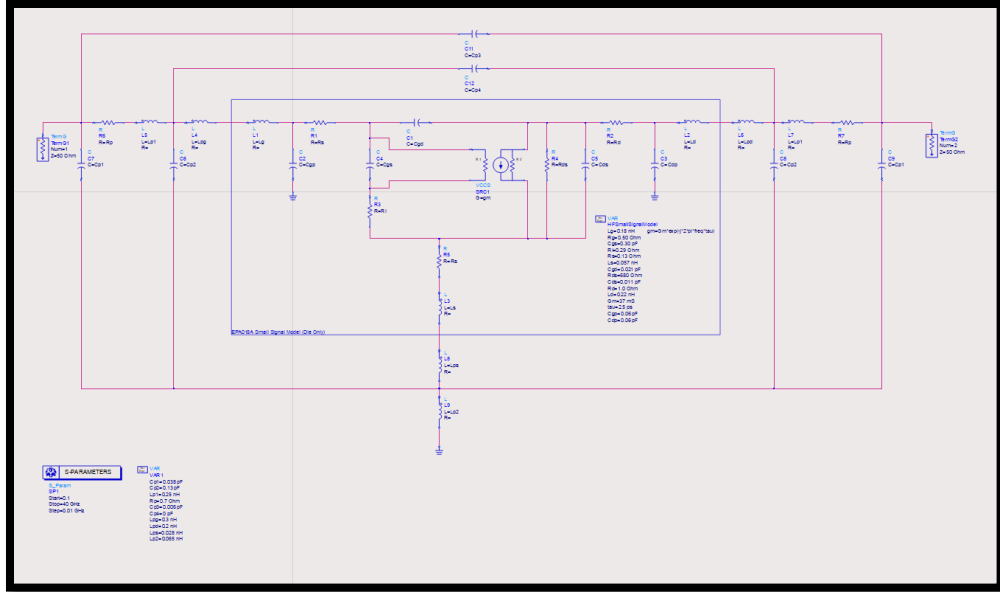


Figure 2: Small Signal Model Used In S Parameter Simulation (With Parasitics)

IV Curves + Small Signal Model

Given that IV curves are a large signal concept and the only information that could be found on google about this is at [4], this section has been skipped and the large signal IV curves have been plotted in more detail. To find the “small signal” IV curves, simply look at the large signal IV curves after the knee.

Small Signal (Low Frequency) Gain

To find the (low frequency) small signal gain (magnitude), the following was used:

$$|A_v| = g_m r_o$$

Where A_v is the small signal voltage gain, g_m is the small signal transconductance and r_o is the small signal output resistance of the transistor.

The transconductance and output resistance were computed from the IV curve data as follows

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad r_o = \frac{1}{\frac{\partial I_{DS}}{\partial V_{DS}}}$$

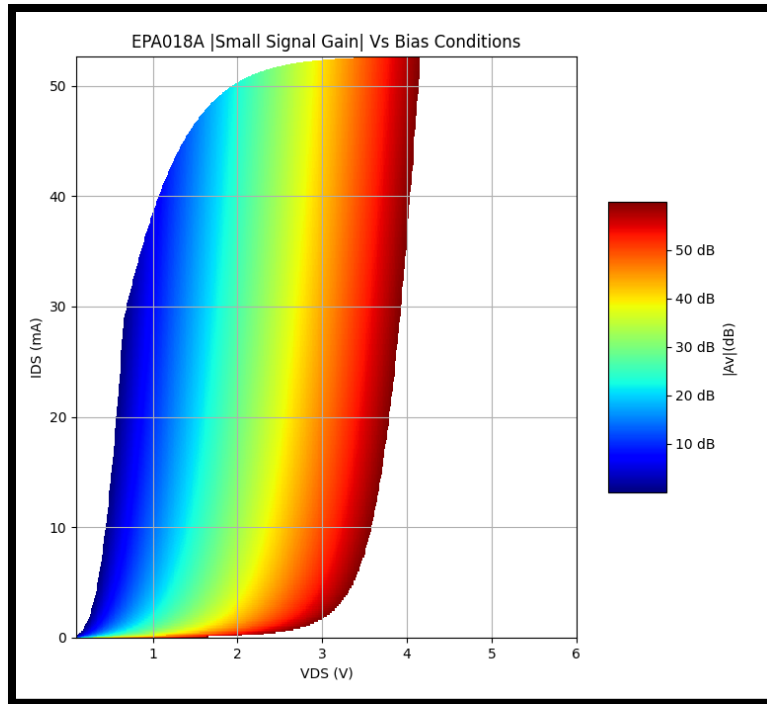


Figure 3: Low Frequency Small Signal Gain Magnitude Colour Plot

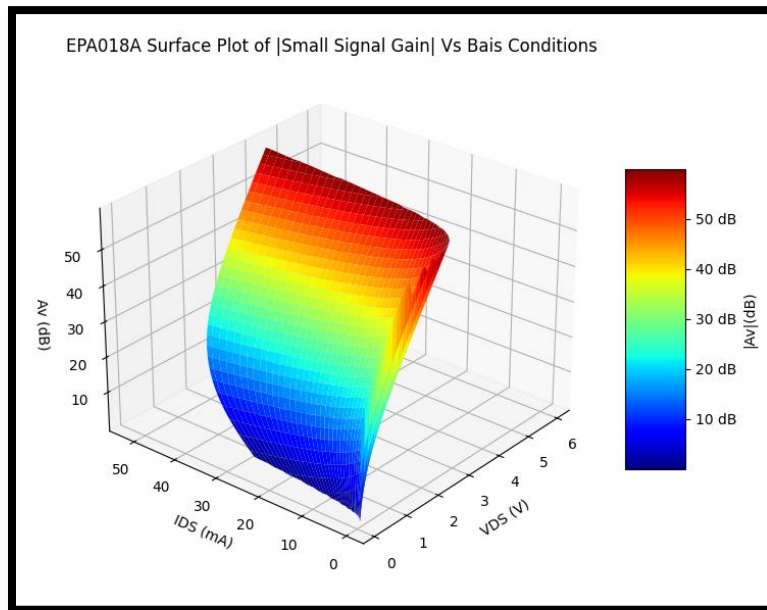


Figure 4: Magnitude of LF Small Signal Gain vs Bias Conditions

Given that the associated gain of this transistor is typically 12.5 dB at $V_{ds} = 2\text{V}$ and $I_{ds} = 15\text{mA}$ as seen in the datasheet, the value taken from this plot (about 30 dB) seems unreasonable. However, it is important to remember that these plots are for low frequencies and the gain given in the datasheet is for an operating frequency of 12 GHz. It is also worth pointing out that gain drops over frequency so a small signal gain of 30 dB at low frequencies seems reasonable.

To find the high frequency small signal gain, just look at the S21 in the next section

Small Signal S-Parameters

Since there are two different bias conditions presented in the S parameter in the datasheet, two different S parameter simulations have been run. Since bias conditions are not really part of the small signal model, “go between” must be used to account in the simulation for the bias conditions. That “go between” is the small signal transconductance which has been computed from the IV curves as seen below. The overall steps for this simulation are as follows (loop through for each bias condition):

1. From the transconductance plots, find the transconductance associated with the desired bias conditions
2. Use that value as Gm in the small signal model (figure 1 and 2)
3. Simulate the circuit and export data to python for plotting

The S parameters have been simulated with and without parasitics for comparison with the datasheet values.

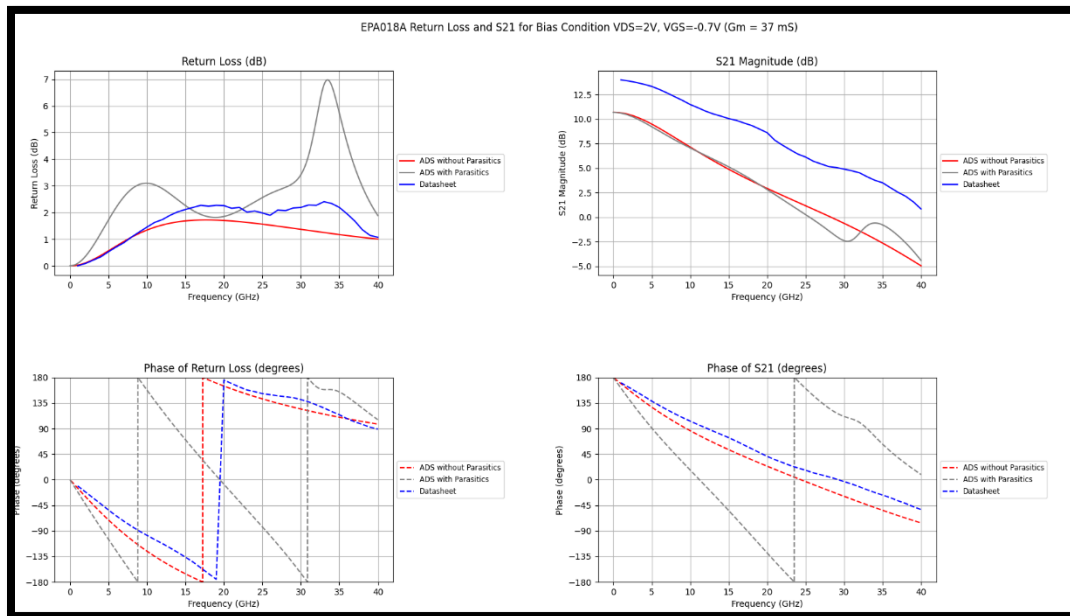


Figure 5: Return Loss and Insertion Gain for $V_{DS}=2V$ and $V_{GS}=-0.7V$ ($G_m = 37 \text{ mS}$)

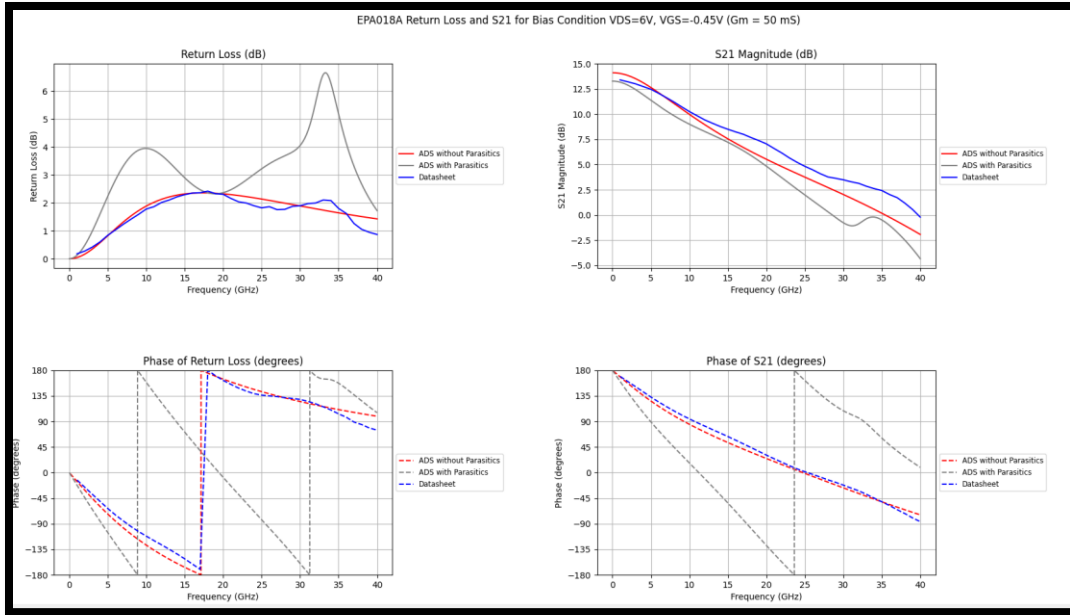


Figure 6: Return Loss and Insertion Gain for $V_{DS}=6V$ and $V_{GS}=-0.45V$ ($G_m = 50 \text{ mS}$)

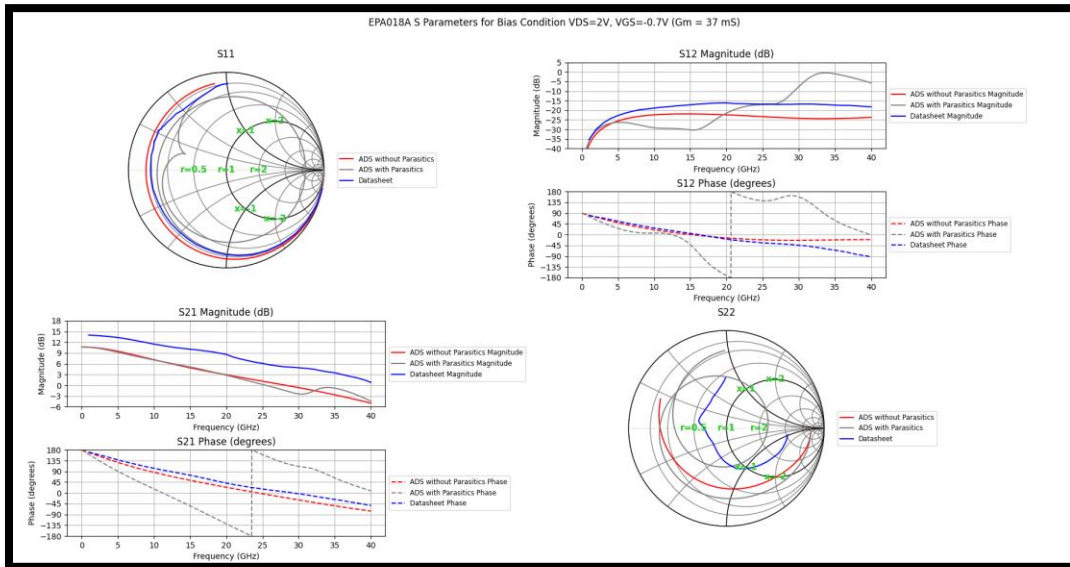


Figure 7: S Parameters for $V_{DS}=2V$ and $V_{GS}=-0.7V$ ($G_m = 37 \text{ mS}$)

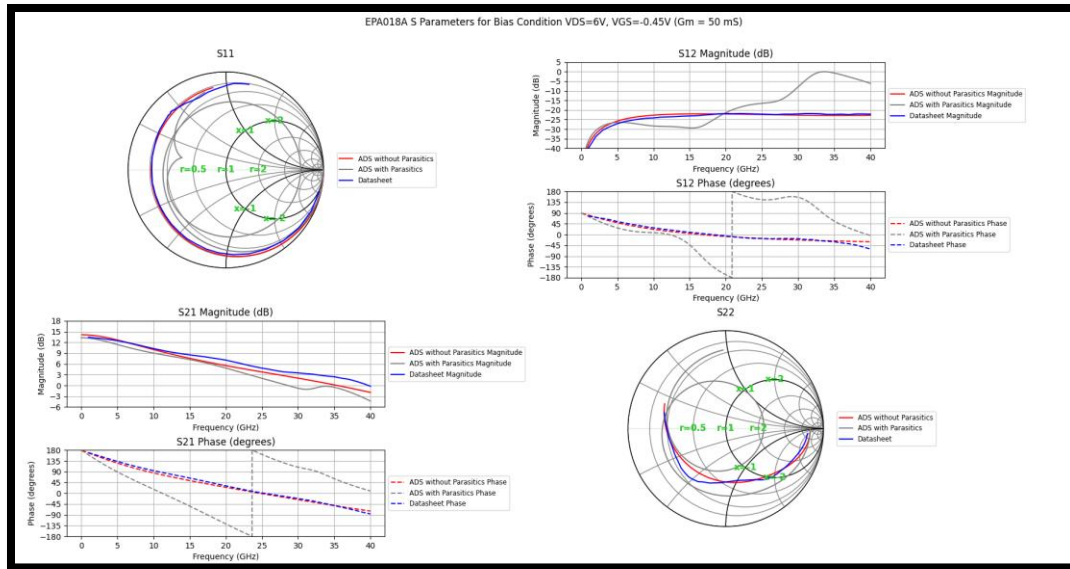


Figure 8: S Parameters for $V_{DS}=6V$ and $V_{GS}=-0.45V$ ($G_m = 50 \text{ mS}$)

As seen from figure 6, the simulated S21 and return loss is within about a dB of the datasheet value which points to this simulation being a reliable model of the real life transistor at this bias point. When running the simulation at the other lower bias point, there is a greater offset from the simulated data vs the datasheet data. This is probably due to the 37 mS transconductance not being high enough. Interestingly though, the S11 (figure 7 and 8) of both bias points agrees rather well which means the offset problem probably has something to do with the output portion of the small signal model. When comparing the simulations with parasitics to the datasheet values, they are wildly off. This further backs up the claim that the datasheet values are of the bare die transistor with a high frequency micro probe being landed on it to do these measurements. In addition to that, the datasheet parameters are taken from real world measurements which are then fitted to analytical models. There will always be some variation between the simulated values and those in the datasheet.

Large Signal Model

The following circuit has been used for the large signal modeling in this document. The specific model that has been used is the Curtice-Ettenburg model as seen in [6]. The numerical values used in this simulation can be found in [7]. In order to use the ADS Curtice3_Model, the datasheet explaining non linear device models has been consulted (see [8]). Further explanation of this model can be found at [9]

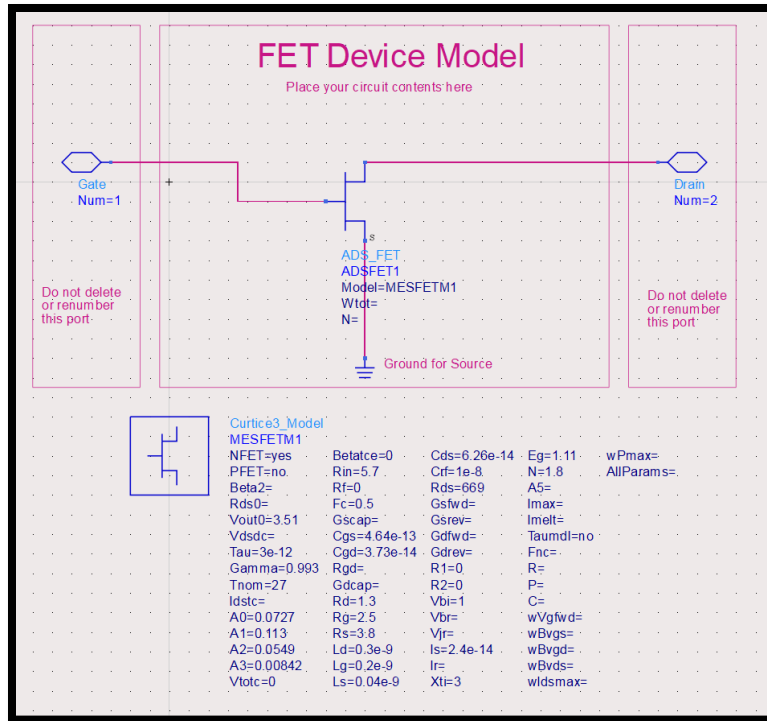


Figure 9: Large Signal (Curtice3) Model in ADS

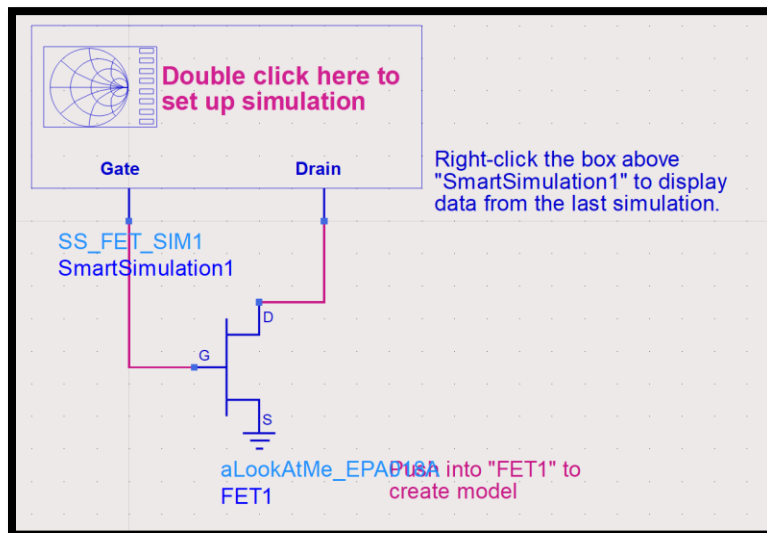


Figure 10: Simulation Wizard Controller Used In Large Signal Modelling

IV Curves + Large Signal Model (Conventional Device IV Curves)

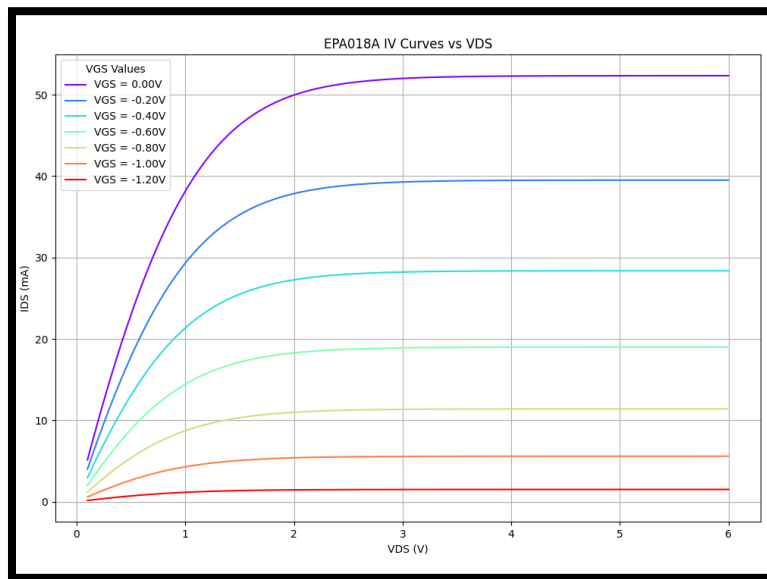


Figure 11: EPA018A IV Curves vs V_{ds}

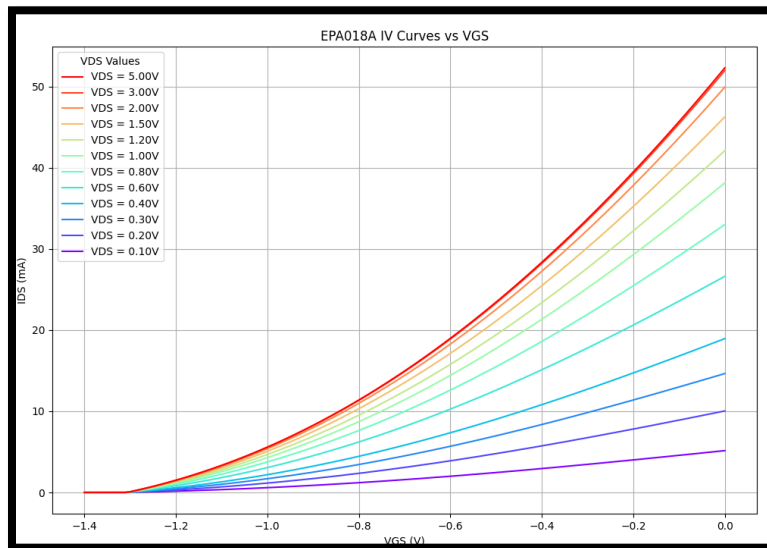


Figure 12: EPA018A IV Curves vs V_{gs}

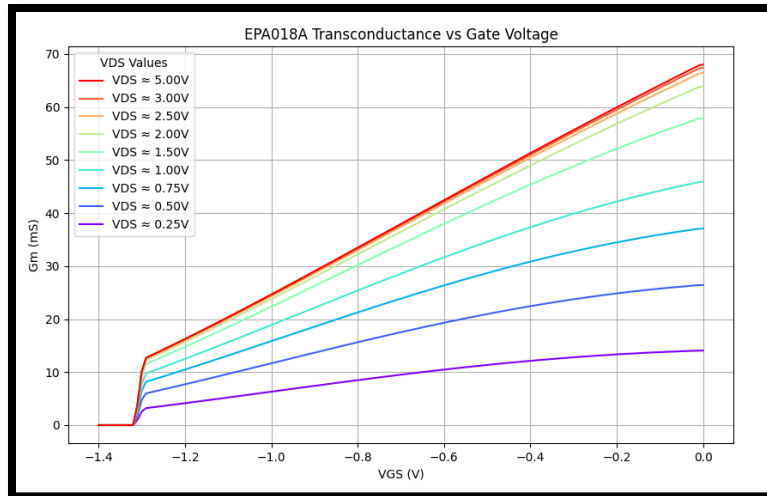


Figure 13: Transconductance Plots

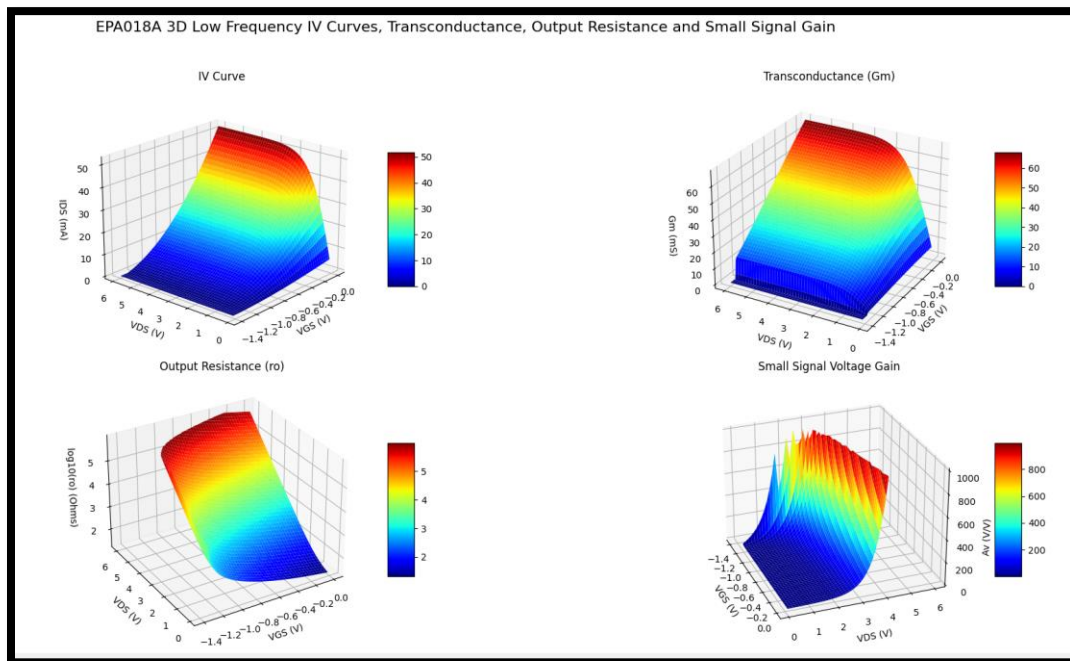


Figure 14: 3D Surface of IV Curves, Transconductance, Output Resistance, and Small Signal Gain (Magnitude)

Table 1: Comparison of DC Parameters

Parameter	Datasheet (Typical)	Simulation Result	Conditions
Idss	55 mA	52 mA	Vds=3V, Vgs=0V
Gm	60 mS	68 mS	Vds=3V, Vgs=0V
Vp	-1.0 V	-1.2 V	Vds=3V, Ids=1.0mA

As seen in table 1, the simulation results for this part does not match up with the values from the datasheet, however they are close and with in the allowable margin given in the datasheet. To get the

Figure 15: Large Signal S Parameter Simulation

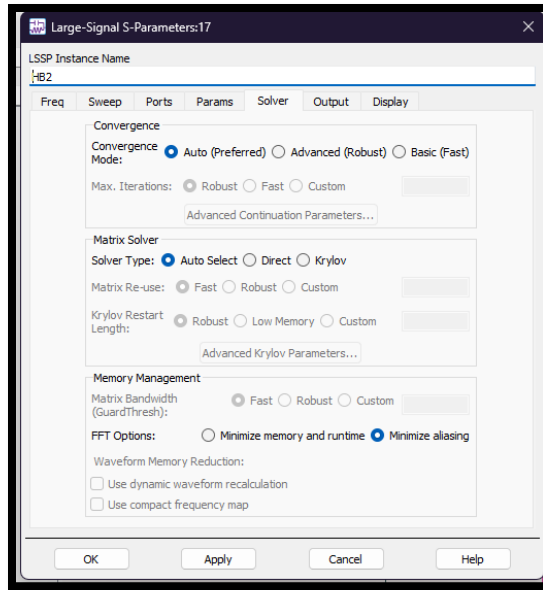
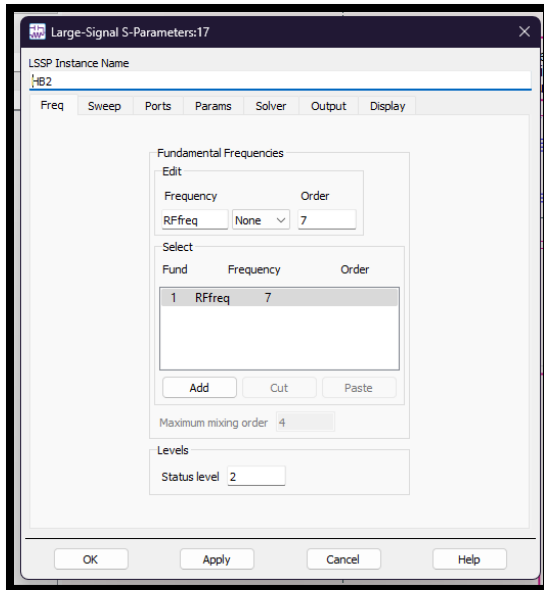


Figure 16: Large Signal S Parameter Setup, Harmonic Balance Settings, Figure 17: Large Signal S Parameter Solver Setup

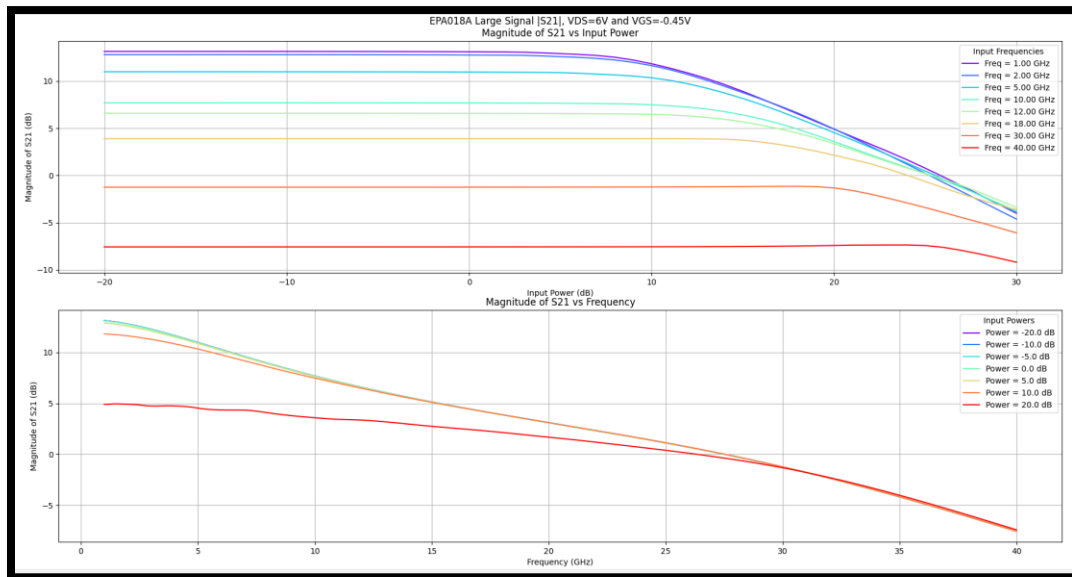


Figure 18: Large Signal $|S_{21}|$, $V_{DS}=6V$, $V_{GS}=-0.45V$

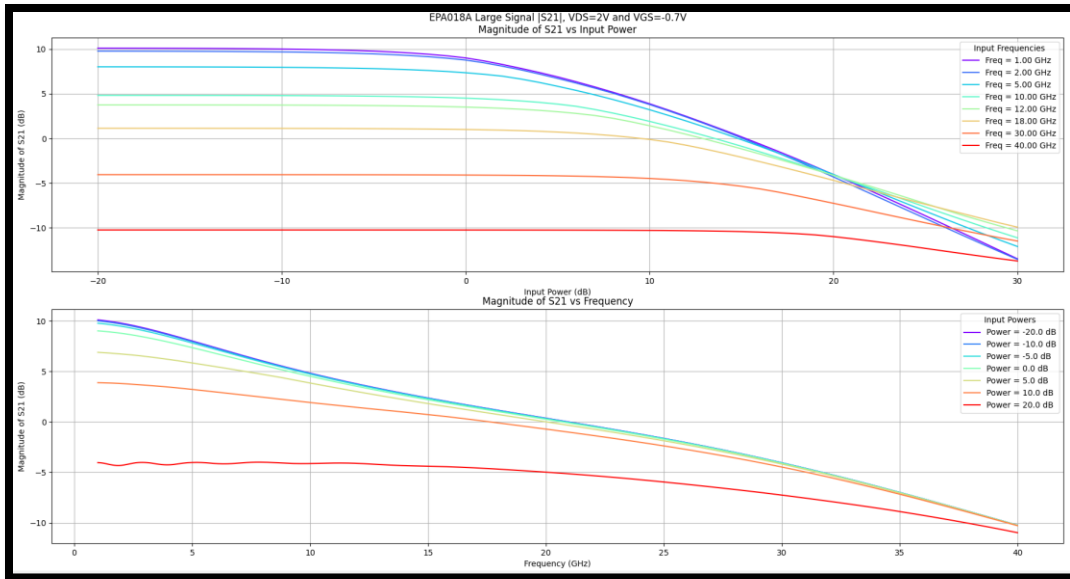


Figure 19: Large Signal $|S_{21}|$, $V_{DS}=2V$, $V_{GS}=-0.7V$

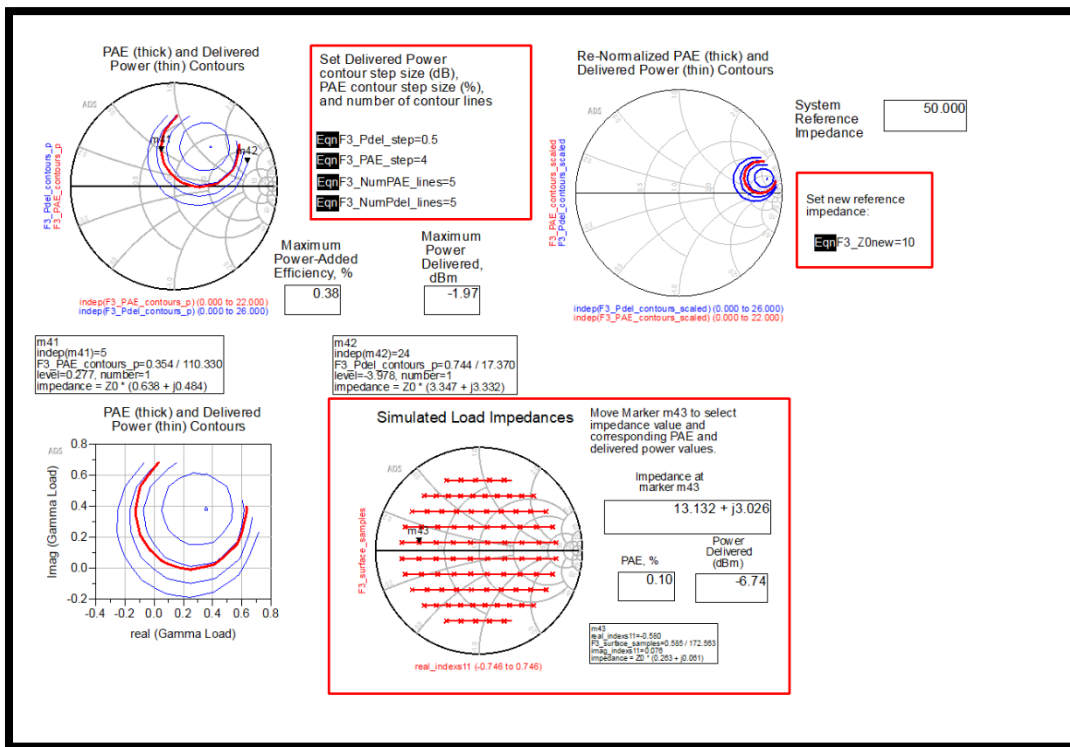
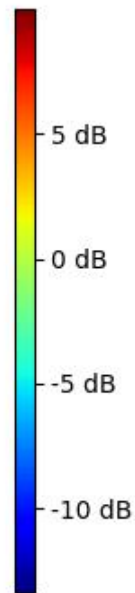
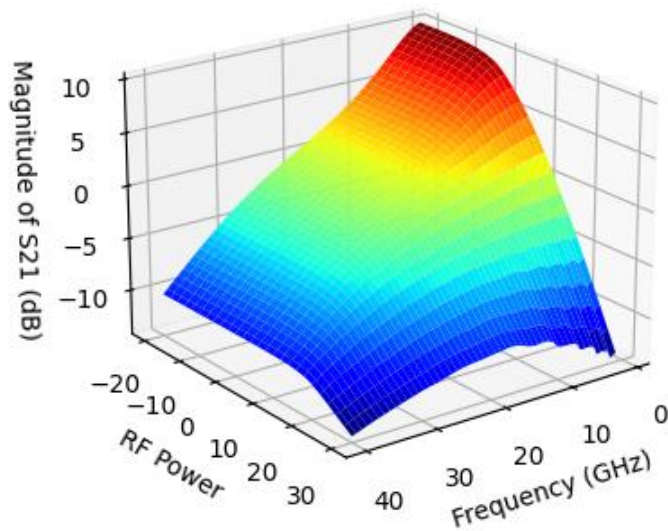


Figure 20: Load Pull Simulation from ADS at 12 GHz

EPA018A Large Signal $|S_{21}|$, $V_{DS}=2V$ and $V_{GS}=-0.7V$
 Magnitude of S_{21} (3D Surface)



Phase of S_{21} (degrees)

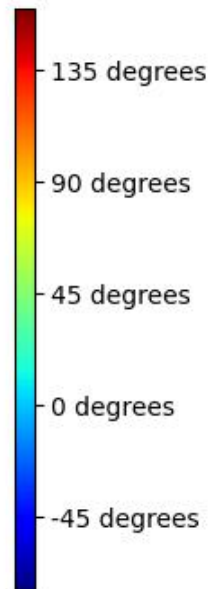
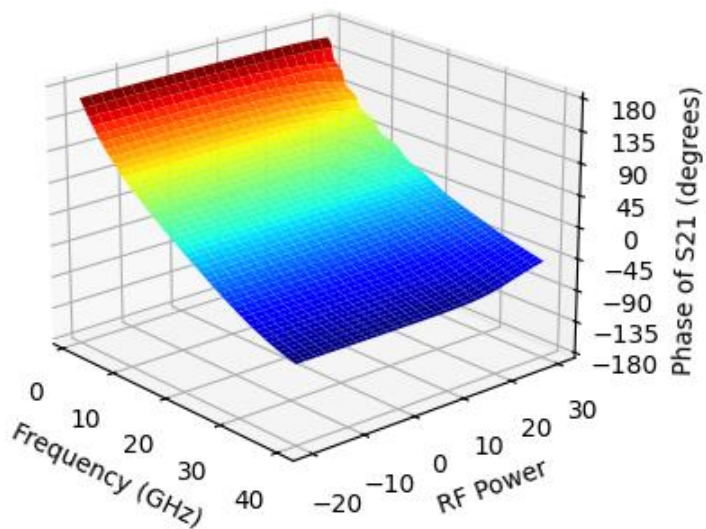
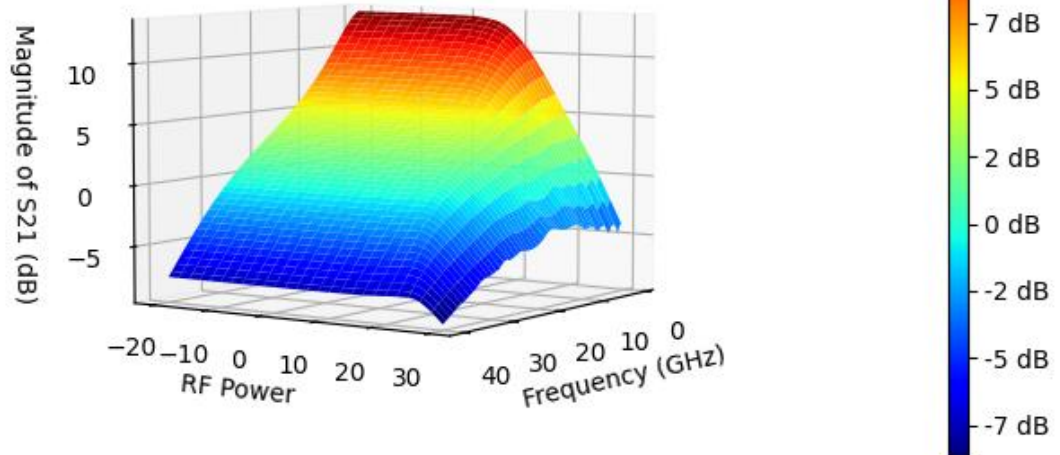


Figure 21: Large Signal $|S_{21}|$, $V_{DS}=2V$, $V_{GS}=-0.7V$ (3D)

EPA018A Large Signal $|S_{21}|$, $V_{DS}=6V$ and $V_{GS}=-0.45V$
Magnitude of S_{21} (3D Surface)



Phase of S_{21} (degrees)

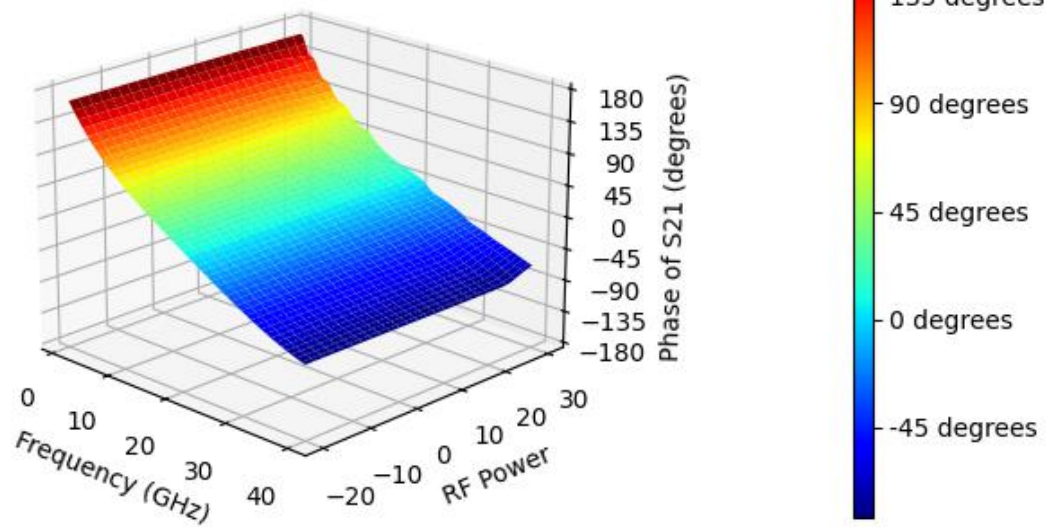
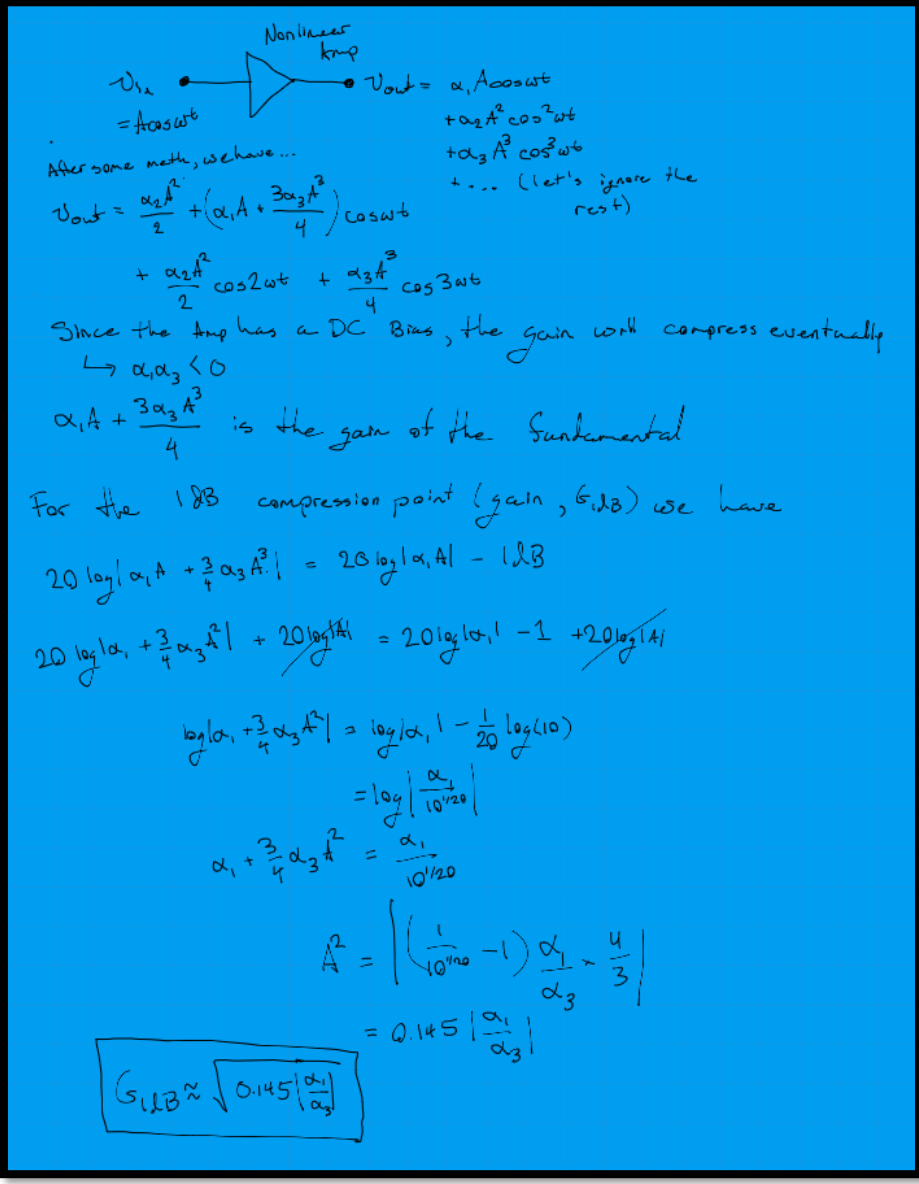


Figure 22: Large Signal $|S_{21}|$, $V_{DS}=6V$, $V_{GS}=-0.45V$

As seen in the above figures, the simulations are producing some questionable results. The shapes of the graph do look plausible, but some of the output power levels look a bit strange. For example, at 10 GHz and in input power of 20 dBm (and $V_{DS}=6V$, $V_{GS}=-0.45V$), the output power is 24 dBm which does seem a bit high given that the output power at the 1 dB compression point is 20 dBm. At the same time, there is no maximum figure on the output power at the 1 dB compression point, so these results are at least plausible. However, the maximum power added efficiency from the load pull simulation is about 0.4% which is 2 orders of magnitude off of the 48% figure in the datasheet which indicates there is definitely a problem with this large signal simulation

One dB Compression Point and Power Added Efficiency



Nonlinear kmp

$V_{in} = A \cos \omega t$

$V_{out} = \alpha_1 A \cos \omega t + \alpha_2 A^2 \cos^2 \omega t + \alpha_3 A^3 \cos^3 \omega t + \dots$ (let's ignore the rest)

After some maths, we have...

$$V_{out} = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega t + \frac{\alpha_2 A^2}{2} \cos 2\omega t + \frac{\alpha_3 A^3}{4} \cos 3\omega t$$

Since the amp has a DC Bias, the gain will compress eventually
 $\rightarrow \alpha_1, \alpha_3 < 0$

$\alpha_1 A + \frac{3\alpha_3 A^3}{4}$ is the gain of the fundamental

For the 1dB compression point (gain, G_{1dB}) we have

$$20 \log \left| \alpha_1 A + \frac{3}{4} \alpha_3 A^3 \right| = 20 \log |\alpha_1 A| - 1 \text{ dB}$$

$$20 \log \left| \alpha_1 + \frac{3}{4} \alpha_3 A^2 \right| + 20 \log |A| = 20 \log |\alpha_1| - 1 + 20 \log |A|$$

$$\log \left| \alpha_1 + \frac{3}{4} \alpha_3 A^2 \right| = \log |\alpha_1| - \frac{1}{20} \log(10)$$

$$= \log \left| \frac{\alpha_1}{10^{1/20}} \right|$$

$$\alpha_1 + \frac{3}{4} \alpha_3 A^2 = \frac{\alpha_1}{10^{1/20}}$$

$$A^2 = \left(\left(\frac{1}{10^{1/20}} - 1 \right) \frac{\alpha_1}{\alpha_3} \times \frac{4}{3} \right)$$

$$= 0.145 \left| \frac{\alpha_1}{\alpha_3} \right|$$

$$G_{1dB} \approx \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|}$$

Figure 23: 1 dB Gain Compression Point Derivation

Power Added Efficiency

$$\eta = \frac{P_{out}}{P_{DC}}$$

$$= \frac{P_{out}}{I_{DD}(V_{DD}-V_{DS})}$$



$$P_{out} = G_v^2 P_m$$

$$PAE = \frac{P_{out} - P_m}{P_{DC}}$$

$$P_{m, \text{ wave}} = \frac{A^2}{2}$$

$$v_{in} = A \cos \omega t$$

$$v_{out} = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4} \right) \cos \omega t$$

$$+ \frac{\alpha_2 A^2}{2} \cos 2\omega t$$

$$+ \frac{\alpha_3 A^3}{4} \cos 3\omega t$$

$$P_m = \frac{A^2}{2}$$

$$P_{out} = \left(\alpha_1 A \right)^2 + \left(\frac{3\alpha_3 A^3}{4} \right)^2$$

Let's just consider the fundamental, $\alpha_2 \ll 1$

$$PAE = \frac{P_{out} - P_m}{P_{DC}} = \frac{\alpha_1^2 A^2 + \frac{9}{16} \alpha_3^2 A^6}{I_{DD}(V_{DD}-V_{DS})}$$

Figure 24: Power Added Efficiency Derivation

References

- [1] N. Cardamone, "Assignment," Nonlinear Microwave Modeling, GitHub repository, 2023. [Online]. Available: <https://github.com/ncardamone10/Nonlinear-Microwave-Modeling/tree/main/Assignment>
- [2] Excelics "datasheet EPA018A," *www.digchip.com*. <https://www.digchip.com/datasheets/parts/datasheet/160/EPA018A-pdf.php> (accessed Nov. 16, 2023).
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