Simulation and Verification of Heterojunction AlGaAs/GaAs PIN Diode

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***Abstract*—A heterojunction PIN Diode in which an I-layer of GaAs is placed between P-layer of $Al_{0.11}Ga_{0.89}As$ and N-layer of GaAs is discussed. The performance of a PIN diode depends to a large extent on the semiconductor material and the geometry of the chip, particularly the intrinsic layer [1]. In this paper, the PIN switching diode model is established by Sentaurus TCAD software and the simulation of different thickness of I- layer is carried out to find the most optimal thickness of I-layer. I-V characteristics and the S-parameters of the PIN device are also measured to verify the experiments.**

***Key words*: PIN diode, Sentaurus TCAD, I-V characteristics, S-parameters**

I. Introduction

The PIN diodes offer an advantage of low insertion loss, high cut off speed, and lower turn on voltage due to its higher concentration of charge carriers reducing the RF resistance. Therefore, the PIN diode are widely used in microwave and RF switching circuit [1-2]. It is used as the switching element in the microwave and RF circuits because the PIN diodes exhibit different characteristics under forward and reverse bias conditions.

Fig. 1 shows on- and off-state equivalent circuits of a PIN diode. When PIN diode is applied with forward bias voltage, electrons and holes are injected into the intrinsic I-layer, decreasing the impedance of the layer I. With the increase of bias current, the resistance decreases gradually. It can be considered as resistance [2]:

$$R_f = \frac{W^2}{(\mu_n+\mu_p)I_0\tau} \quad (1)$$

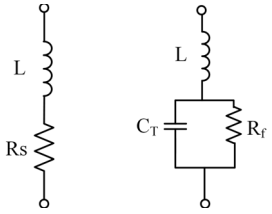
Where w is the thickness of the intrinsic layer, I_0 is the forward bias current, τ is the lifetime of lifetime, and μ_n and μ_p are the mobility of electrons and holes, respectively.

On the other hand, when the reverse voltage is biased at a PIN diode, the electrons and holes are extracted from the intrinsic layer, and the I-layer is depleted. The junction capacitance C_j of the diode tends to be constant. It functions as the capacitor [2]:

$$C_j = \frac{\varepsilon A}{W} \quad (2)$$

Where A is the junction area of PIN diode, and ε is the dielectric constant of GaAs material.

Consequently, proper I-layer thickness of the PIN diode is needed to reduce resistance and capacitance in design.



(1) On-state (2) Off -state

Fig.1. Equivalent circuits of a PIN diode

II. Simulation and Fabrication

Firstly, Sentaurus Structure Editor is used to implement AlGaAs/GaAs PIN diode structure showed in Fig.2 [4]. The first layer of the PIN structure is added for the purpose of reducing the p-ohmic contact. The heterojunction AlGaAs/GaAs structure is used for the reason that the carrier injected from the junction is limited by the bandgap discontinuity between the AlGaAs/GaAs layers. This limitation effectively reduces the resistance in the intrinsic region. The parameters of the epitaxial structure are provided in Table-I. Then, the device is simulated by Sentaurus Device. It is extremly important to choose the proper relevant physical models for realistic and accurate simulation. A proper mesh grid is also considered to achieve good numerical convergence.

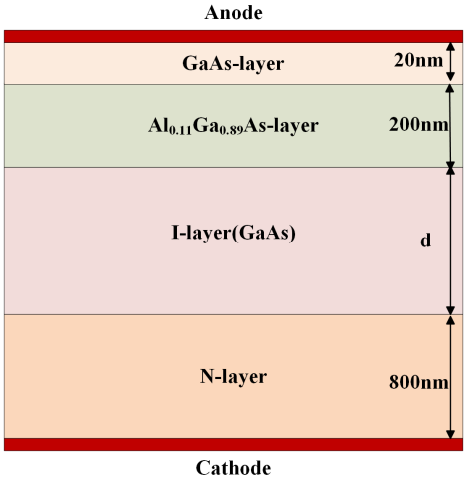


Fig.2. Structure of the PIN diode

TABLE I . PARAMETERS OF THE MATERIAL

Layer	Material	Doping(cm^{-3})	Thickness(um)
P-GaAs	GaAs	5e18	0.02
P-AlGaAs	$Al_{0.11}Ga_{0.89}As$	5e18	0.2
I	GaAs	None	w
N	GaAs	5e18	0.8

Finally, AlGaAs/GaAs PIN diode is fabricated. The vertical epitaxy is used because it has the smallest internal resistance and higher carrier injection efficiency compared with the planar structure. The P-mesa and the N-mesa are formed using the wet etching technology with the etching depth of 1.8um and 0.55um respectively. A lift-off technique is used to make n-ohmic contacts and p-ohmic contacts. BCB is used for dielectric layer of the PIN multi-layer structure [5].

III. RESULT AND ANAYSIS

The PIN device designed requires that its forward resistance be small enough and the reverse breakdown voltage be larger than 35V so it can be used as element of RF circuit. Therefore, the minimum thickness of I-layer can be set to 1.5 um due to the limitation of etching process and breakdown voltage. Meanwhile, the maximum thickness of simulated I-layer can be set to 3 um as a contact.

I-V characteristics of PIN diodes are simulated with different thickness of I layer: 1.5um, 2.0um, 2.5um, 3.0um, which are showed in Fig.3. It is seen that the thickness of I-layer has an inverse relationship with turn-on voltage. It means that the thinner the thickness of I-layer, the higher the forward current in the PIN diode.

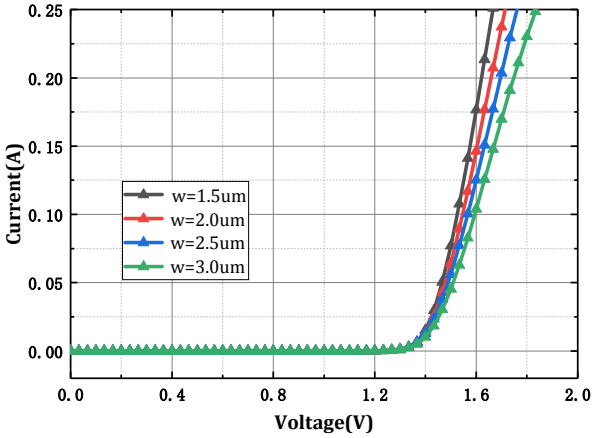


Fig.3. Simulated I-V characteristics performance of GaAs PIN diode

The measured results of I-V characteristics of PIN diode devices are shown in Fig. 4. When the current is 100μA, the PIN diode is turned on and the corresponding voltage is 1.15V. When the reverse current reaches 100μA, the diode breaks down and the breakdown voltage is greater than 20V. The measured results are in good agreement with the simulation results and the requirement of the PIN diode.

Displayed in Fig.5 is the measured insertion loss and isolation of the PIN device from 1GHz to 40GHz. It can be seen from this measured data that the isolation is around 12dB at 25GHz which is a good result while the insertion loss is 2dB which is larger than we expected. It may be because the doping concentration is not so high and the Ohmic resistivity is high.

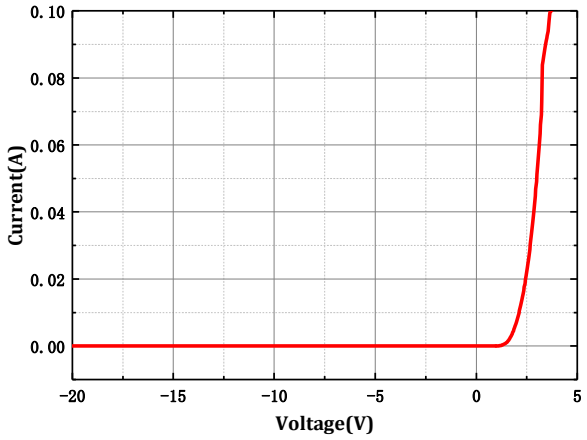


Fig.4. Measured forward I-V characteristics

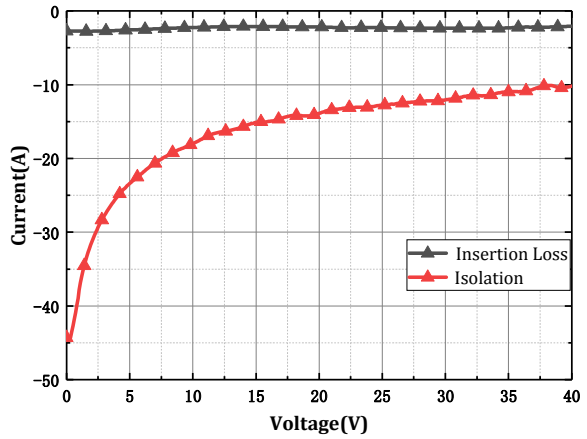


Fig.5. Measured insertion loss and isolation of PIN device

IV. CONCLUSION

In this study, AlGaAs/GaAs PIN diode with an epitaxial structure has been simulated using Sentaurus TCAD software and verified successfully. The thickness of I-layer has an inverse relationship with turn-on voltage and resistance. BCB is also used in the process of fabrication. S-parameter is also tested for the frequency range (1-40GHz) with I-layer thickness of 1.5um. It turns out that the insertion loss is larger. The insertion loss is around 2dB at 30GHz. In order to optimize the performance of a system, efforts are needed to reduce the resistance and capacitance with the aim of better characteristics.

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