

ELG 6369

NONLINEAR MICROWAVE DEVICES AND EFFECTS

CHAPTER II

**NONLINEAR MODELING OF ACTIVE
MICROWAVE DEVICES**

After a brief review on CAD, we will introduce the nonlinear models of active devices widely used in RF/microwaves.

A – ACTIVE AND PASSIVE NONLINEAR COMPONENTS

I – Two-terminal and transfer components

In nonlinear Computer-Aided Design, two concepts are used namely, the two-terminal nonlinearities and the transfer nonlinearities. Two-terminal nonlinearity is a simple passive nonlinear component, i.e., a resistance, capacitance, or inductance. Its value is function of one independent variable, the voltage or current *at its terminals* (Figure II-1-a). This variable is called control voltage or control current device.

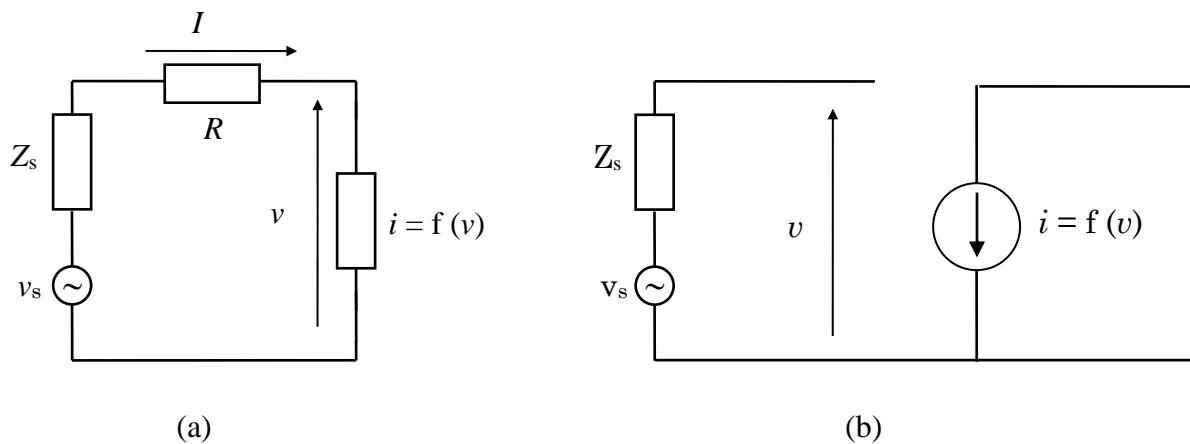


Figure II-1: Two-terminal nonlinearity (a) vs. Transfer nonlinearity (b).

In transfer nonlinearity, the control voltage or current is somewhere in the circuit *other than at the element's terminals*. Thus, it is possible for a circuit element to have more than one control variable. As one of the control variables is usually the terminal voltage or current, thus many nonlinear elements must be treated as combinations of transfer and two-terminal nonlinearities.

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A simple example of transfer nonlinearity is the nonlinear controlled current source in the equivalent electrical circuit of a transistor (Figure II-1-b).

Practical devices often include both types of nonlinearities (e.g., the gate-source capacitance C_{gs} and the drain current I_d of a FET). However, it is important to distinguish between them. Let us assume the nonlinear two-terminal in Figure II-1-a is a nonlinear resistance and the transfer nonlinearity is a nonlinear ideal transconductance amplifier. Let them be excited by a voltage source v_s with an internal real impedance Z_s . The amplifier output current is a function of the excitation voltage and the nonlinear transfer function; it can be found by simply substituting the voltage waveform into the transfer function, regardless of the nature of the input/output circuits.

In two-terminal nonlinearity, however, the excitation voltage generates current components in the resistance at few frequencies (harmonics). These components circulate in the rest of the circuit, generating voltages at those frequencies across R and therefore across the nonlinear resistance. These new voltage components generate new current components, and the process continues until current and voltage components at all possible frequencies are generated.

⇒ The two-terminal nonlinearity is more complicated to analyze analytically than the transfer nonlinearity.

These remarks show clearly *why* the transfer nonlinearities are more popular to nonlinear circuit designers than the two-terminal nonlinearities. As a consequence, nonlinear passive components are not widely used in nonlinear microwave circuits.

II – One-port active components versus passive components

The above conclusions can imply that diodes, as one-port components, are rarely used in nonlinear circuits, but the reality is exactly *the inverse*. First, diodes are active components not passive ones. Their behaviour to control voltages is completely different. Second, diodes size, reliability, and cost are often decisive criteria for microwave designers, even if transistors present a transfer function modulus greater than unity.

B – QUASI-STATIC ASSUMPTION

Inherent in the nonlinear time- or frequency-domain analyses of nonlinear circuits is the quasi-static assumption: all nonlinear elements (transconductance, capacitance, etc.) change with a change in one or more control voltages or currents. Because they are based on a fundamental assumption of linearity, impedance concepts and multi-port circuit theory cannot be used as the sole means of describing a nonlinear circuit. Accordingly, the most popular means for characterizing diodes and transistors (S - Y - or Z -parameters) cannot be used to model nonlinear solid-state devices. Instead, one should use a lumped circuit model that includes a mix of linear and nonlinear resistances, capacitances, inductors, and controlled sources.

The nonlinear elements are therefore assumed to be quasi-static up to the sub-mm range.

This assumption is also implicit in linear circuit theory; it requires, for instance, that the charge on a capacitance is a function solely of the voltage at its terminals. One advantage of the quasi-static approach is that small-signal models of devices can be converted easily to large-signal models. Small-signal devices are often described by lumped-element models as an alternative to multi-port parameters. Such models can be converted to large-signal models simply by including

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the voltage dependence of the circuit's elements or/and by making minor changes in the topologies of the models.

However, quasi-static modelling is not applicable to devices whose operation is dominated by time effects like transit-time devices such as IMPATTs and Gunn or transferred-electron devices. Such devices are so strongly nonlinear that they are rarely used in circuits that have amplitude-modulated or multiple excitations and are usually used as oscillators or amplifiers.

An obvious requirement of a good nonlinear device model is that it be sufficiently accurate over a wide frequency range because important mixing products and harmonic may span a wide range of frequencies.

But there is always a dilemma for a designer

- Assure high accuracy. This situation is possible only with the use of complex circuit topologies, which require large CPU time usage for their simulation.
- Use the simplest adequate model. However, simpler topology cannot assure high accuracy.

Another requirement is that the nonlinear characterisation of any solid-state device usually requires a number of measurements. If the number and difficulty of these measurements are excessive, the design cost of the resulting circuit is increased and accuracy may suffer.

C – NONLINEAR LUMPED ELEMENTS

I – Basic concepts

The nonlinear device models consist usually of nonlinear resistances, nonlinear capacitances, and controlled sources. The circuit elements can be described by one of two kinds of characteristics: a large signal global characteristic, or an incremental small-signal characteristic. The former describes the overall I/V or Q/V relationship and is used for modelling large-signal circuits. The latter describes the deviation of voltage and current or charge in the vicinity of a bias point, and is used for modelling small-signal, quasi-linear circuits.

Note: Since solid-state devices are not lumped circuits, such lumped equivalent circuit models are then an approximation.

Two critical concepts in the modelling of nonlinear devices are voltage and current control, and incremental quantities. Many elements are either current- or voltage-controlled and the value of a voltage-controlled element is dependent upon a voltage that may be applied to its terminals or elsewhere in the circuit. For example, we know from circuit theory that the small-signal junction conductance of a nonlinear diode can be expressed as a nonlinear exponential function of voltage or as a linear function of current. But, in the case of nonlinear elements, we should *precise* at this point what we mean exactly by *small signal resistance*. What is the difference between small-signal resistance and nonlinear resistance?

II – The substitution theorem

To emphasise that concept, the I/V characteristic of a simple linear resistance is given by the well-known Ohm's law { $V = RI$ }. But, suppose a current controlled nonlinear resistance r is used

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in an application where a small signal ac current is applied and a dc control current I_o exists. The ac component of its voltage should be given by

$$v(t) = r(I_o) i(t) \quad (\text{III-1})$$

where $v(t)$ and $i(t)$ are the small signal voltage and current, respectively (Figure II-2).

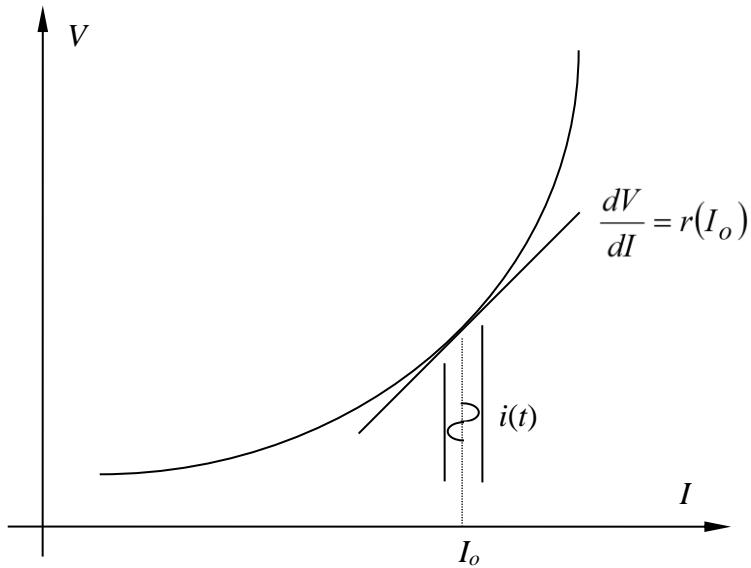


Figure II-2: Incremental small signal resistance of a nonlinear resistance.

It is clear that

$$v(t) = \left. \frac{dv}{di} \right|_{i=I_o} i(t) \quad \rightarrow \quad r(I_o) = \left. \frac{dv}{di} \right|_{i=I_o} \quad (\text{III-2})$$

This is the *incremental resistance* and is valid in small signal quasi-linear analysis. Let us consider a voltage-controlled conductance.

The small signal current i can be expended in a Taylor series around the DC bias voltage V_o as

$$i(v) = f(V_o + v) - f(V_o) = v \frac{df(v)}{dv} \Big|_{v=V_o} + \frac{1}{2} v^2 \frac{d^2 f(v)}{dv^2} \Big|_{v=V_o} + \frac{1}{6} v^3 \frac{d^3 f(v)}{dv^3} \Big|_{v=V_o} + \dots \quad (\text{II-3})$$

In the quasi-linear case, the terms of degree greater than one are neglected, and

$$i(v) = v \frac{df(v)}{dv} \Big|_{v=V_o} = g(V_o) v \quad (\text{II-4})$$

$g(V_o)$ is the *incremental resistance* at V_o . For the nonlinear case, we have

$$i(v) = g_1 v + g_2 v^2 + g_3 v^3 + \dots \quad (\text{II-5})$$

With the help of the substitution theorem, the nonlinear element can be modelled as shown in Figure II-3.

D – DIODES

A nonlinear active device modelling can be based on physics equations or equivalent electrical circuit. We have retained this approach, which is more efficient for circuit theory purposes. A large variety of diodes are available for various purposes: detection, amplification, mixing, oscillation, multiplication, etc. Usually, we should distinguish between *Transit Time Devices* or *Transferred Electron Devices* like Gunn and IMPATT diodes where the quasi-static assumption is not valid, and those where the assumption applies like Schottky, varactor and Tunnel diodes.

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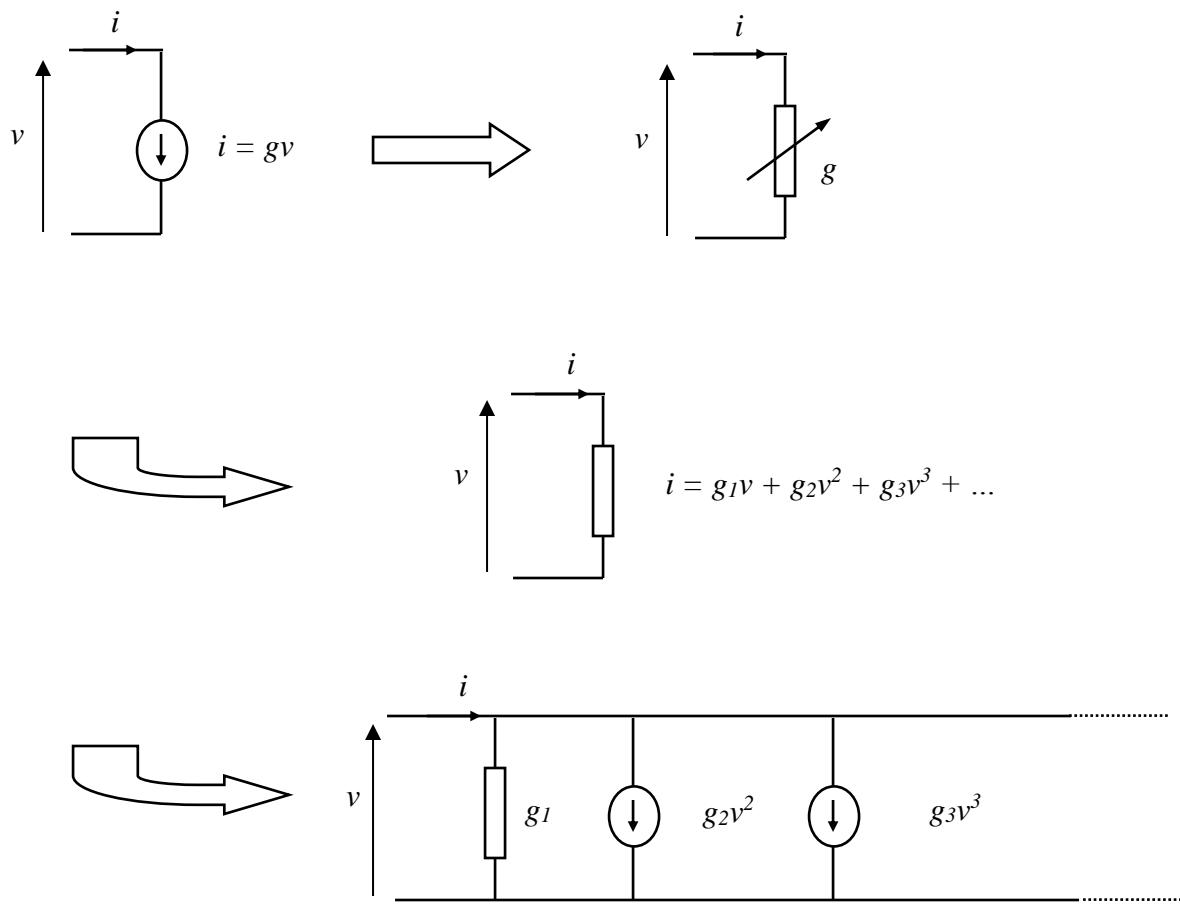


Figure II-3: The substitution theorem: A nonlinear element can be described by an equivalent circuit that includes a linear conductance G_1 and controlled current sources representing the higher-degree terms in the series.

I – Gunn Diodes

Gunn diodes are not usual diodes because there is no junction. The diode operation is based on the volume effect or Gunn effect (transfer of electrons when an electrical field is applied). Mainly used in oscillation, these diodes are constituted either as a three-layer structure N⁺-N-N⁺ or a two-

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layer structure N-N⁺ with a current-limited contact at the cathode, which control the charge injection in the active layer and thus allows a better behaviour at high frequencies.

Several large-signal diode models have been proposed but the recurrent problem is to establish a general and efficient *I/V* relationship due to the fact there is many operating modes namely the transit-time mode, the delay-domain mode, the quenched-domain mode, the accumulation-layer mode and the stable domain mode. Moreover, the voltage variation has mainly a field-dependent behaviour. One of the most used large-signal Gunn diode models is the one proposed by Chua (Figure II-4) where the elements are defined as:

$$C_1 = \frac{\varepsilon A}{L} \quad C_2 = \frac{\varepsilon A}{W} \quad (\text{II-6})$$

$$I_g = A q n_o f\left(\frac{V_1}{L}\right) = A q n_o f(E_o)$$

$$I_d = C_2 n_o \left\{ \int_{E_o}^{E_M} \left[\frac{f(E_o) - f(E)}{n_a - n_o} + \frac{f(E_o) - f(E)}{n_o - n_d} \right] dE \right\} - I \quad (\text{II-7})$$

with A the diode section, ε the dielectric constant, L the diode length, W the domain range, n_o the concentration of a carrier of charge q (uniform doping), n_a the concentration of a carrier in the accumulation region, n_d the concentration of a carrier in the depletion region, f the characteristic function describing the velocity dependence in function of the applied field E , E_o the amplitude of the constant field outside the domain mode, E_M the maximum amplitude of the field. and R a resistance, which depends on V_1 and V_2 , C_2 , n_o , and L .

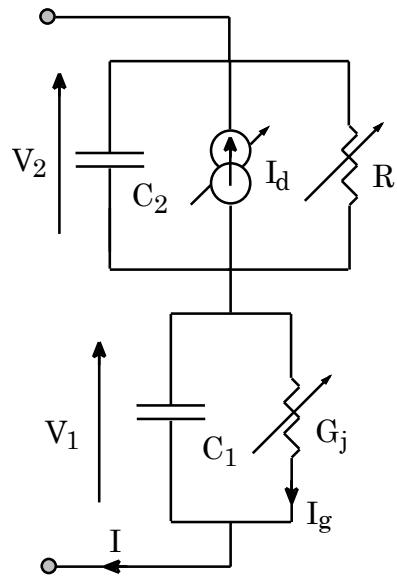


Figure II-4: The Gunn diode large-signal equivalent circuit.

II - IMPATT Diodes

IMPact ionization Avalanche Transit Time diodes or IMPATT diodes (or Read diodes) are P⁺-N-N⁺ diodes that have a large breakdown region. Their nonlinearity is related to the conduction current waveform, which is a short impulsion in the breakdown region. These diodes are used in parametric amplification, frequency multiplication and as millimetre power sources for radars (high power impulsion). They allow high-order frequency multiplication and up-conversion with high conversion rates. However, they are unstable (oscillations) and exhibit a relatively high noise figure.

The equivalent electrical circuit of an IMPATT diode is shown in Figure II-5.

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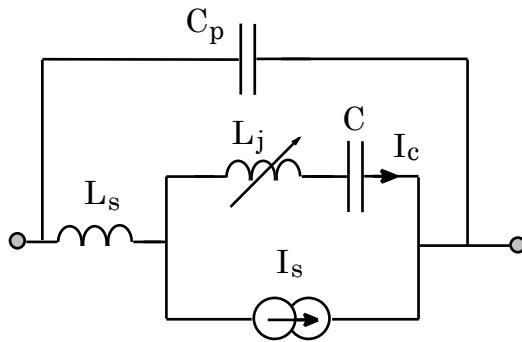


Figure II-5: Equivalent nonlinear electrical circuit of an IMPATT diode.

This equivalent circuit presents a current source I_s function of transit time τ_d

$$I_s(t) = \frac{1}{\tau_d} \int_{t-\tau_d}^t I_c(t') dt' - I_c(t) \quad (\text{II-8})$$

and a nonlinear inductance L_j function of current I_c , bias current I_{dc} , and breakdown inductance L_a

$$L_j(I_c) = \left(\frac{I_{dc}}{I_c} \right) L_a \quad (\text{II-9})$$

where L_s and C_p are parasitic elements. The voltage-current relationship is an integro-differential equation function of input signal amplitude and frequency. Similarly, to Gunn diodes, the voltage is dependent of electrical field; therefore, it is quite difficult to model the voltage-current relationships. Moreover, we have other variants like TUNNETT diodes ("TUNNEL-injection Transit Time diodes") that have better efficiency and noise figure. As diffusion effect in the transit region is avoided (due to the Gunn effect), these diodes, also called GUNNETT diodes, are mainly used in the millimetre range as oscillators.

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III - SRD Diodes

SRD diodes ("Step Recovery Diodes") are used for high-order frequency multiplication or generation of high frequency signals from low frequency harmonic oscillators. For illustration, harmonic generators with fundamental frequency of 10 MHz have generated output frequencies around 100 GHz.

The early works have modelled the diode as a perfect conductor in forward bias and a capacitance in inverse. It is possible to isolate input and output. However, the real diode exhibits a transit time, a series resistance and parasitic elements C_p and L_s (Figure II-6-a).

Relationship between the charge Q and the junction voltage V_j can be established in function of barrier voltage Φ , forward capacitance C_f , and inverse capacitance C_r (Figure II-6-b):

$$Q = \begin{cases} C_r V_j & V_j \leq 0 \\ \frac{C_f - C_r}{2\Phi} \left(V_j + \frac{C_r \Phi}{C_f - C_r} \right)^2 - \frac{C_r^2}{2(C_f - C_r)} \Phi & 0 < V_j < \Phi \\ C_f V_j - \frac{C_f - C_r}{2} \Phi & \Phi \leq V_j \end{cases} \quad (\text{II-10})$$

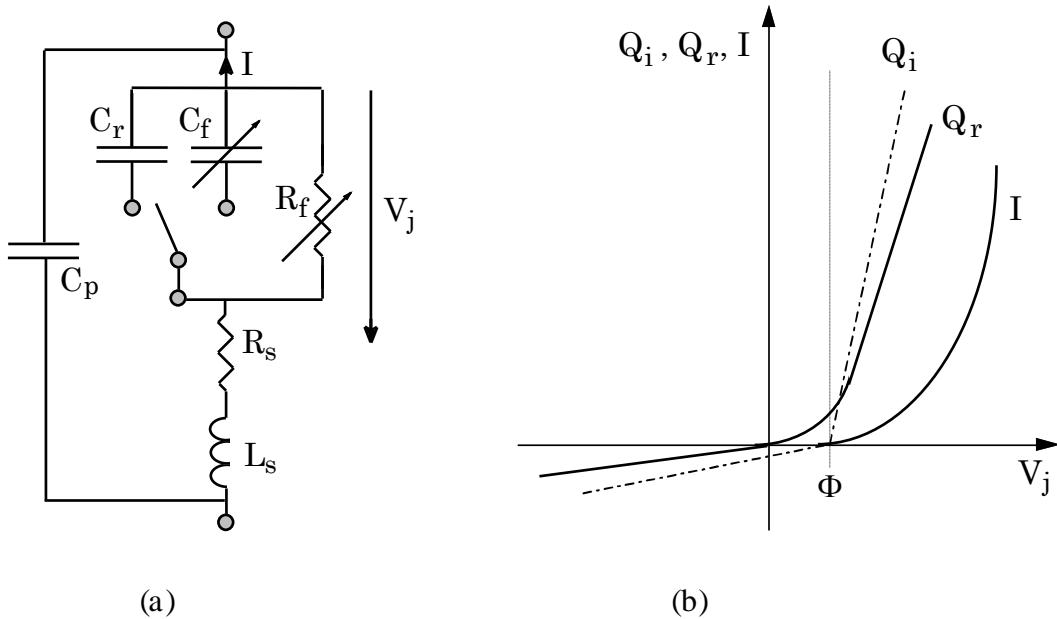


Figure II-6: SRD diodes: (a) Equivalent nonlinear electrical circuit, (b) $I(V_j)$ and $Q(V_j)$ curves
(Q_i : ideal curve; Q_r : real curve)

IV – PIN diodes

PIN diodes, used as power attenuators and limiters, exhibit a higher breakdown voltage. Also, their impedance switches from a very low value in direct bias to a very high value in inverse. Such aspect is very important because the diode is working as a reflector (a reflector is able to handle high powers, as it does not have to absorb them). Moreover, in inverse bias, as the junctions P-I and I-N are biased in inverse, the intrinsic region is fully depleted and then acts as a perfect insulator. So, when the diode reaches the breakdown region, it can generate a high-order frequency multiplication. However, if SRD diodes switch from a low forward capacitance C_f to a high inverse capacitance C_r , this kind of diodes switches from a high capacitance value to a low inductance value. Introduced in MMICs, GaAs Vertical PINs (VPINs) offer a very low on-resistance for the least amount of off-capacitance, and can handle huge power.

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V – Schottky diodes

Schottky diodes are widely used in detection, mixing, and frequency multiplication. They consist of a metal contact, thus do not have the recombination time limitations of PN junctions (due to low junction capacitance). When they are excited by a large signal, the junction conductance G_j and the junction capacitance C_j act as nonlinear elements function of the voltage V_j (Figure II-7). Parasitic effects are modelled by a series resistance R_s and an inductance L_s . A capacitance C_p can be included to take into account the embedding effects. If the diode is forward-biased, the nonlinear effect of the conductance $G_j(V_j)$ is predominant. In inverse bias, the nonlinear effect is mainly due to the capacitance $C_j(V_j)$ (Figure II-8). Resistance R_s is generally constant up to the millimetre frequency range. The total junction current I_j is the sum of the current I_c due to C_j and the current I_d due to G_j , i.e.

$$I_d(V_j) = I_s \left(e^{\frac{q}{\eta kT} V_j} - 1 \right) \quad (\text{II-11})$$

and

$$I_c(V_j) = C_j(V_j) \frac{dV_j(t)}{dt} + V_j \frac{dC_j(V_j)}{dV_j} \frac{dV_j}{dt} \quad (\text{II-12})$$

leading to

$$C_j(V_j) = C_{jo} \left\{ 1 - \frac{V_j(t)}{\Phi} \right\}^{-\gamma} \quad (\text{II-13})$$

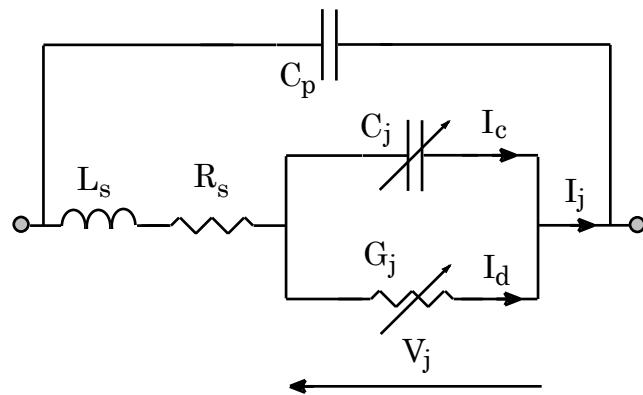


Figure II-7: Equivalent circuit of a Schottky diode.

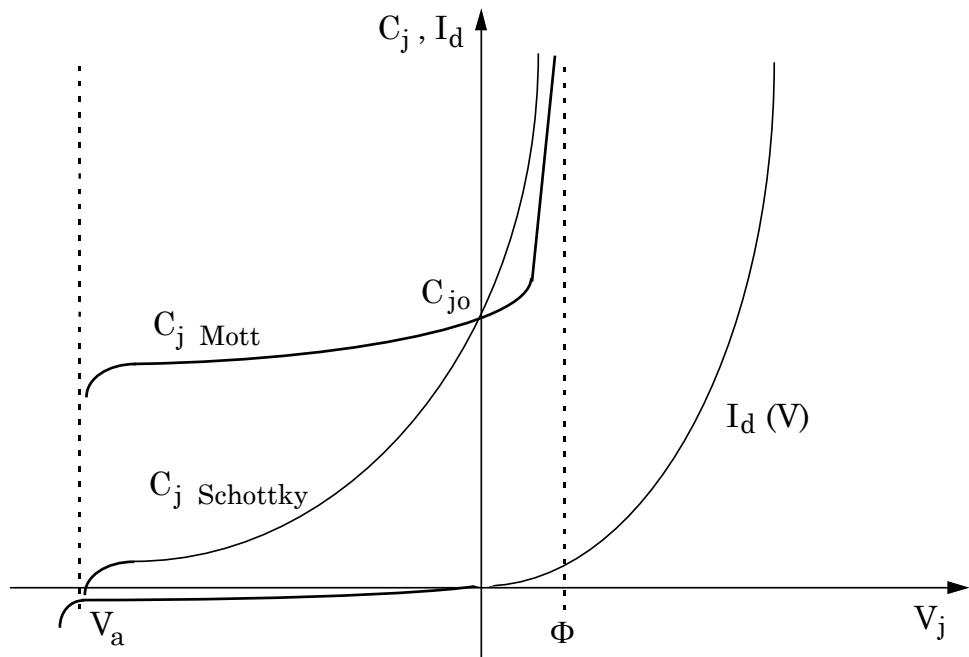


Figure II-8: Characteristic of conductance current I_d of Schottky diode and capacitance C_j of Schottky and Mott diodes.

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with,

C_{jo} : zero-bias junction capacitance,

Φ : Barrier voltage,

γ : Exponent dependent of doping (uniform: $\gamma=0.5$, gradual: $\gamma=0.33$, Marinos: $\gamma=1$),

I_s : Reverse saturation current,

q : Electron charge,

k : Boltzmann's constant ($1.37 \cdot 10^{-23} \text{ J/K}$),

T : Absolute temperature,

η : Ideality factor (usually between 1.1 and 1.2).

For a non-uniform doping, the exponent γ value changes. For example, a linearly graded junction, wherein the epitaxial-layer doping increases linearly with distance from the junction, has $\gamma=1/3$. For a strongly graded junction, the above relation is replaced by an empirical relation as for Mott diodes. In such diodes, the active region is very thin (lightly doped epitaxial layer) and then fully depleted at zero bias. Then, this kind of diodes exhibits a relatively weak capacitance variation with voltage that can be used to achieve good conversion loss and noise temperature in mixers at low local oscillator levels and/or low temperatures. Their opposite are varactor diodes.

"Super Schottky" diodes or Josephson diodes are superconductor-semiconductor tunnel junctions. They are mainly used for detection in the millimetre and near infrared frequency range.

VI – Varactor diodes

Varactor diodes use exclusively the capacitance-voltage characteristic (inverse bias). Their equivalent circuit is similar to that of Schottky diodes.

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As their capacitance-voltage characteristic nonlinearity is more accentuated, they are used in frequency multiplication and as voltage controlled tuning elements.

Hyperabrupt varactor diodes exhibit a γ coefficient equal to 1.5 or even 2.0 at least part of their reverse voltage ranges. The series resistance R_s value is high, which excludes their use in frequency multiplication. They are most useful in tuning applications (e.g., in voltage controlled oscillators) where the strong controlled nonlinearity can be used to achieve a wide and nearly linear frequency-voltage characteristic. Other varactor diodes such as SBV, QWD, BNN, bbBNN, and HEMV diodes can be used in millimetre and sub-millimetre frequency ranges but their models are perfectible due to their very small physical dimensions.

VII – Tunnel diodes

Esaki or tunnel diode current-voltage characteristic has the particularity to exhibit negative resistance, which is useful for oscillation (Figure II-9). However, due to its poor performance, the tunnel effect has been neglected in oscillation until its use in millimetre range was underlined.

Such diodes, called RTD ("Resonant Tunnelling Diodes"), have emerged in the millimetre range because they exhibit a lower capacitance value and allow more control of the peak-valley current-voltage values. Moreover, they are mainly used for odd-order frequency multiplication (the current-voltage characteristic is symmetric and then has the properties of an odd function). They are also used for detection and mixing and by opposition to passive detectors, RTD diodes can operate without power absorption (the negative resistance compensates the real positive part of the diode impedance and then let the component purely reactive).

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The main limitation of RTD diodes in millimetre and sub millimetre oscillators is their low output power. One option is to combine them in series or in parallel. However, the designer has to deal with instabilities in bias circuits, which create additional undesirable output noise.

The equivalent circuit of a RTD is similar to the one of Schottky diode and total current is the sum of capacitance current I_c (for which equation (II-13) can be used) and conductance current I_d .

For this last current, several equations have been proposed, but the polynomial approximation proposed by Narud and Meyer seems to be the most appropriate to model the current voltage relationship

$$I_d(V) = \frac{(I_{pd} - I_{vd})(V(t) - V_{vd})^4}{(V_{vd} - V_{pd})^5} \{5(V(t) - V_{pd}) - (V(t) - V_{vd})\} + I_{vd} \quad (\text{II-14})$$

where the indexes "pd" and "vd" represent the peak and the valley value respectively.

Note: For most commercial microwave circuit simulators, active components should exhibit continuously derivable current-voltage relationships. So, even if transit-time or electron-transfer device current-voltage relationships are strongly nonlinear, they are not easy to express and then to model. Thus, the quasi-static approximation is the most convenient for microwave designers.

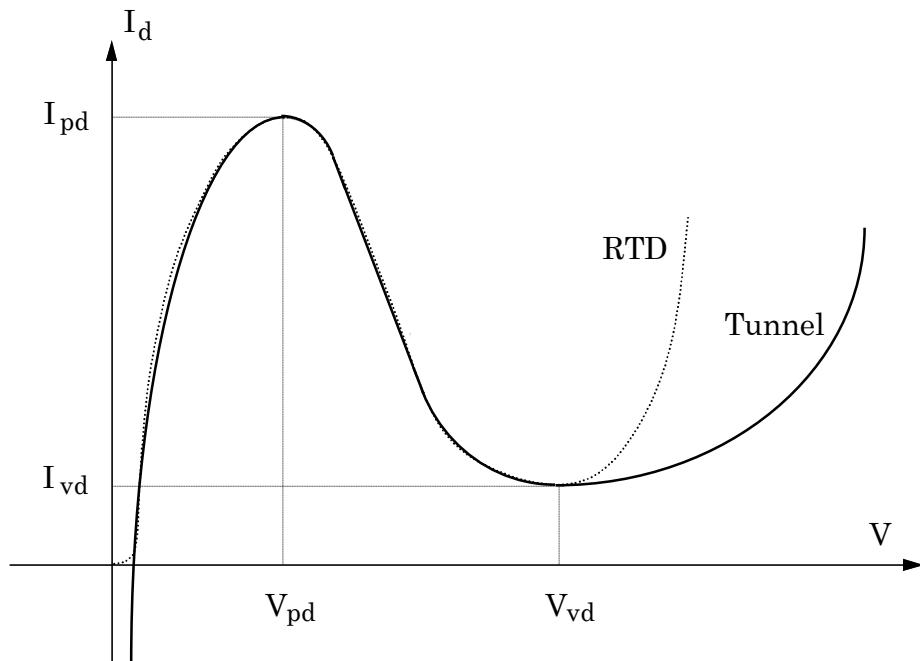


Figure II-9: Conductance current I_d of Tunnel and RTD diodes.

E – TRANSISTORS

Hybrid or monolithic transistor-based circuits and systems are widely used in communication systems. Thus, a circuit designer should have access to a large range of reliable models to use in any CAD process. To be reliable and efficient, this model has to meet two opposite goals: speed and accuracy. A complete transistor model is very precise but very slow, as it can include more than 70 parameters and use complex equations to fit the measured data over a large range of frequency and Q points. On the other side, a simpler model can be faster, but it will present lower accuracy and performance. The designer has then to deal between these two extreme cases.

Gallium arsenide (GaAs) transistors are widely used in the microwave area but research about silicon and Gallium Nitride (GaN) transistors is growing up. For more performance, complex

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hereto-structure transistors like HEMTs/HBTs of AsAlGa/AsGa, SiGe/Si, InAsGa/InP ... can be built with new technologies ionic implantation, molecular beam, metal organic vapor phase (MOCVD), and/or new process like electronic lithography, photolithography,

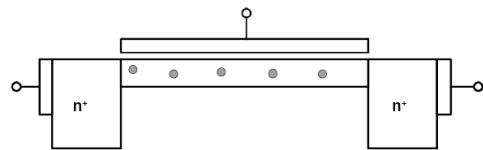
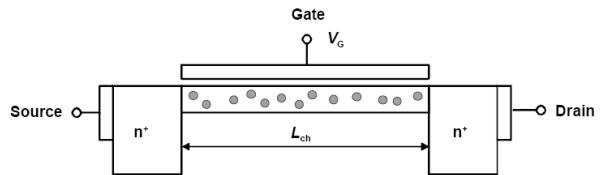
Some major issues have to be taken into account to make a transistor suitable for RF/microwave applications (i.e., reacts as fast as possible to the excitation):

- the physical parameters and the material used to fabricate the transistor,
- the cutoff and maximum frequencies (f_T and f_{max} respectively), etc.

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How to Make an FET Fast ?



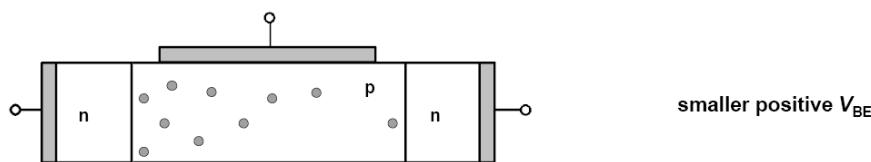
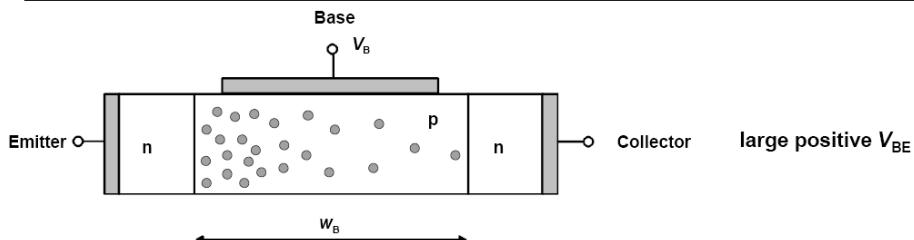
Design:

- short channel (small L_{ch})
- fast carriers (n-channel)

Material:

- fast carriers
(high mobility, high velocity)

How to Make a Bipolar Transistor Fast ?



Design:

- narrow base (small w_B)
- fast carriers (npn)

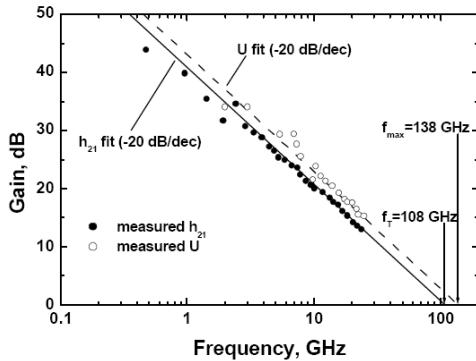
Material:

- fast carriers
 - high mobility
 - high velocity
- high diffusivity

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To characterize the device speediness, we often refer to f_T (Transition frequency or unity-current-gain frequency for which the gain falls to unity) and f_{max} (the maximum oscillation frequency or the frequency at which the power gain drops to unity). We should understand their meaning <http://www.univ-lille1.fr/anodegroup/>

The Characteristic Frequencies f_T and f_{max}



Measured h_{21} and U of a GaAs MESFET
After K. Onodera et al., IEEE Trans. ED 38, p. 429.

h_{21} and U roll off at higher frequencies at a slope of -20 dB/dec.

Cutoff Frequency f_T

Frequency, at which the magnitude of the short circuit current gain h_{21} rolls off to 1 (0 dB).

Maximum Frequency of Oscillation f_{max}
Frequency, at which the unilateral power gain U rolls off to 1 (0 dB).

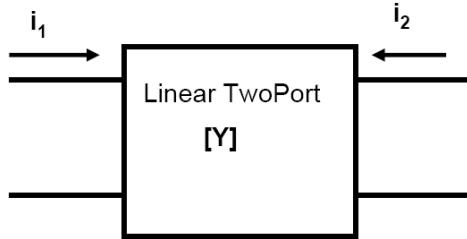
Attention: Frequently f_{max} is NOT extrapolated from measured U , but from measured MAG or MSG !

Check before working with published f_{max} values !

23

Cutoff (transit) frequencies f_t, f_{max}

Current Gain, f_t

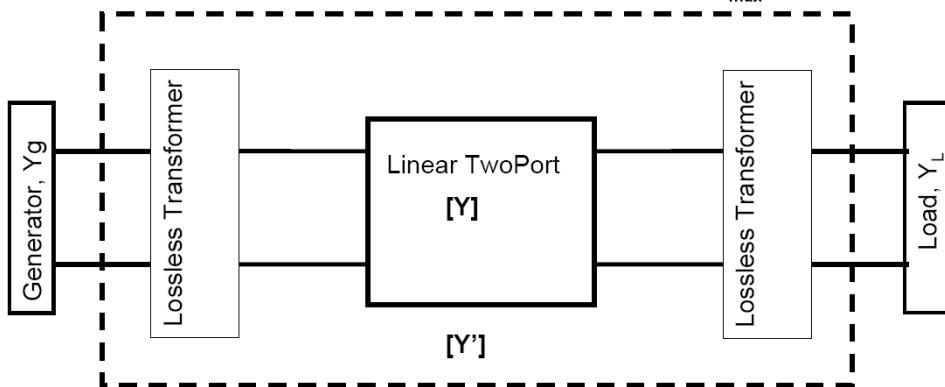


$$|H_{21}|^2(dB) = 10 \log_{10} \left(\left| \frac{Y_{21}}{Y_{11}} \right|^2 \right)$$

The transit frequency corresponding to $|H_{21}|^2$ (dB) = 0 dB is called f_t

Cutoff (transit) frequencies f_t, f_{max}

Maximum Available (or power) Gain (MAG), Mason's Gain, f_{max}

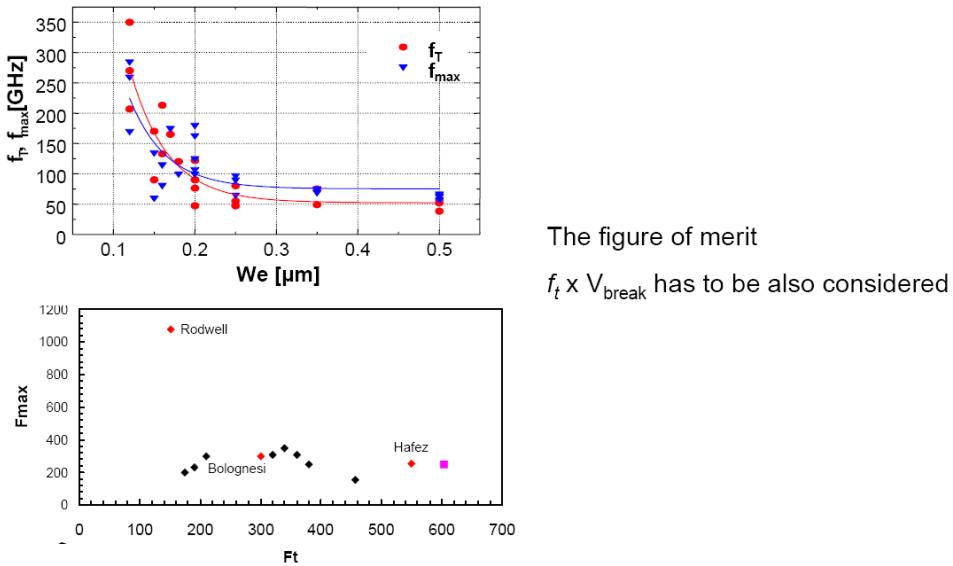


If $Y_{11}' = Y_g^*$ and $Y_{22}' = Y_L^*$

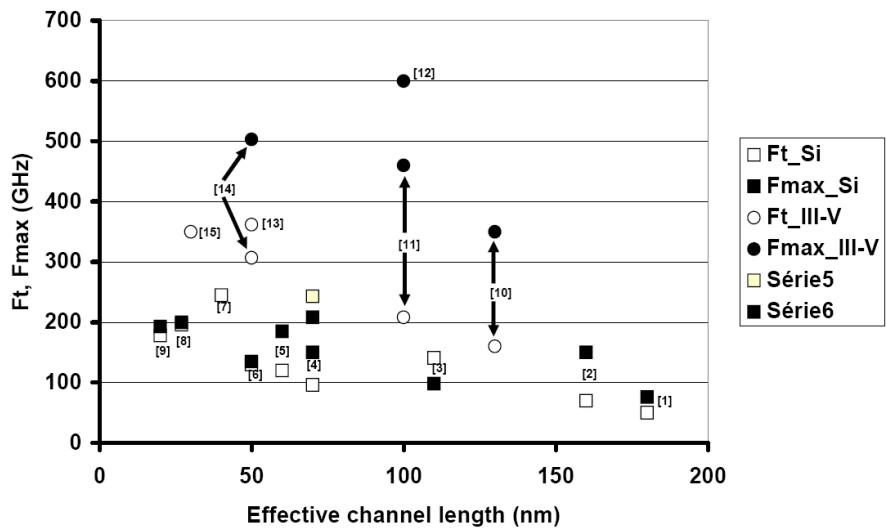
$$MAG = \left| \frac{Y_{21}}{Y_{12}} \right| (k - \sqrt{k^2 - 1}) \quad \text{avec} \quad k = \frac{2 \operatorname{Re}(Y_{11})\operatorname{Re}(Y_{22}) - \operatorname{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}$$

The transit frequency corresponding to MAG (dB) = 0 dB is called f_{max}

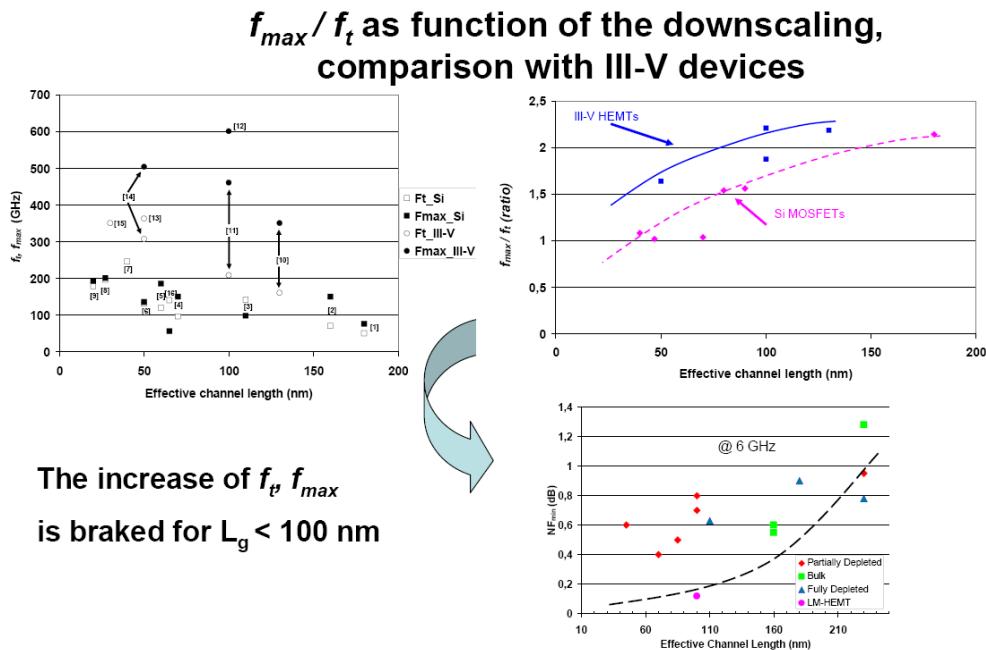
HF Performance of SiGe & III-V HBTs



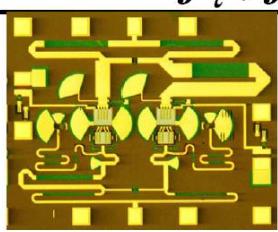
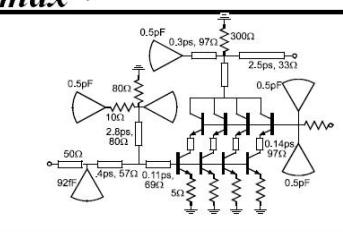
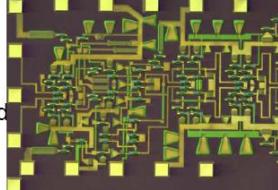
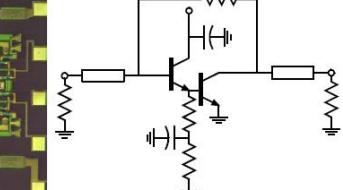
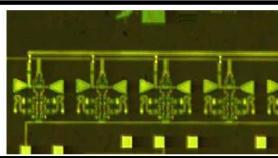
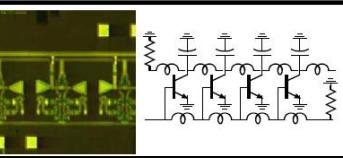
HF Performance of Si (MOSFETs) & III-V FET (HEMTs)



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What do we need: f_τ , f_{max} , or ... ?

<p>Tuned ICs (MIMICs, RF): f_{max} sets gain, & max frequency, not f_t.</p> <p>...low f_t/f_{max} ratio makes tuning design hard (high Q)</p>	 
<p>Lumped analog circuits need high & comparable f_t and f_{max}. (1.5:1 f_{max}/f_t ratio often cited as good...)</p>	 
<p>Distributed Amplifiers in principle, f_{max}-limited, f_t not relevant.... (low f_t makes design hard)</p>	 

M. Rodwell, UCSB

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FOMs – f_T and f_{\max} vs f_{op}

Rule of thumb

$$f_T \sim n \times f_{\text{op}}, f_T \sim f_{\max}$$

- Low-noise transistors: $n \sim 10$ (conservative), i.e., f_T should be around $10 \times$ the operating frequency f_{op} of the RF system in which the transistor is to be used.
- Power transistors: $n \sim 5$.

What does this mean?

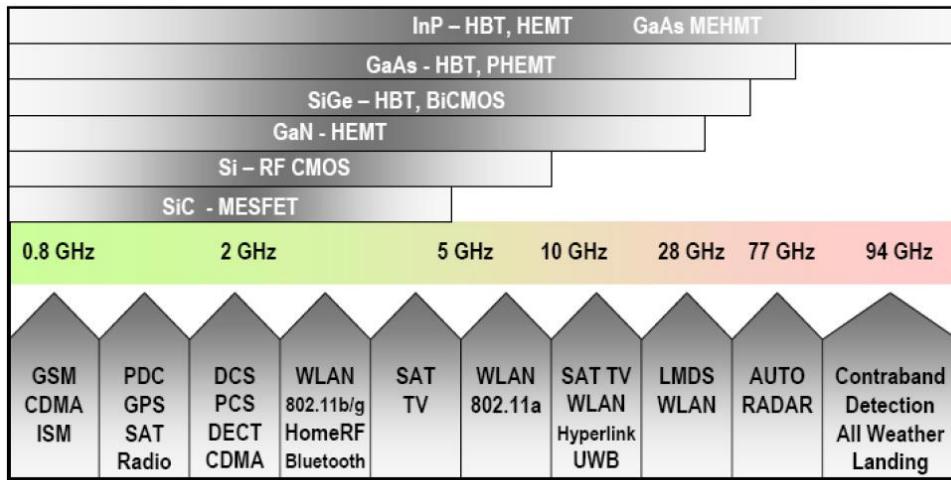
If $n = 10$ and $f_T = f_{\max}$, we have 20 dB unilateral power gain U at f_{op} . Note that U is the upper limit for the power gain a transistor can achieve. The actual gain in a realistic circuit environment, e.g. G_a for minimum noise, will be several dB lower.

Examples:

GaAs MESFET: $f_{\max} = 70$ GHz	$U @ 12$ GHz = 15.3 dB, $G_a @ 12$ GHz = 11 dB
AlGaAs/GaAs HEMT: $f_{\max} = 50$ GHz	$U @ 12$ GHz = 12.4 dB, $G_a @ 12$ GHz = 9 dB
AlGaAs/GaAs HEMT: $f_{\max} = 120$ GHz	$U @ 18$ GHz = 16.5 dB, $G_a @ 18$ GHz = 11.6 dB

As for the applications of RF/microwave transistors, refer to
<http://www.teknik.uu.se/fte/courses/asd/>

RF Electronics – Applications



Taken from: ITRS 2003 Edition.
Chapter Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications

RF Electronics – Acronyms

- **GSM** Global System for Mobile Communications
- **CDMA** Code-Division Multiple Access
- **ISM** Industrial, Scientific and Medical (frequency bands)
- **PDC** Personal digital cellular
- **GPS** Global Positioning System (Satellite)
- **DCS** Digital Communication System
- **PCS** Personal Communications system
- **DECT** Digital European Cordless Telephone/Telecommunications
- **WLAN** Wireless Local Areal Network
- **UWB** Ultra-Wideband

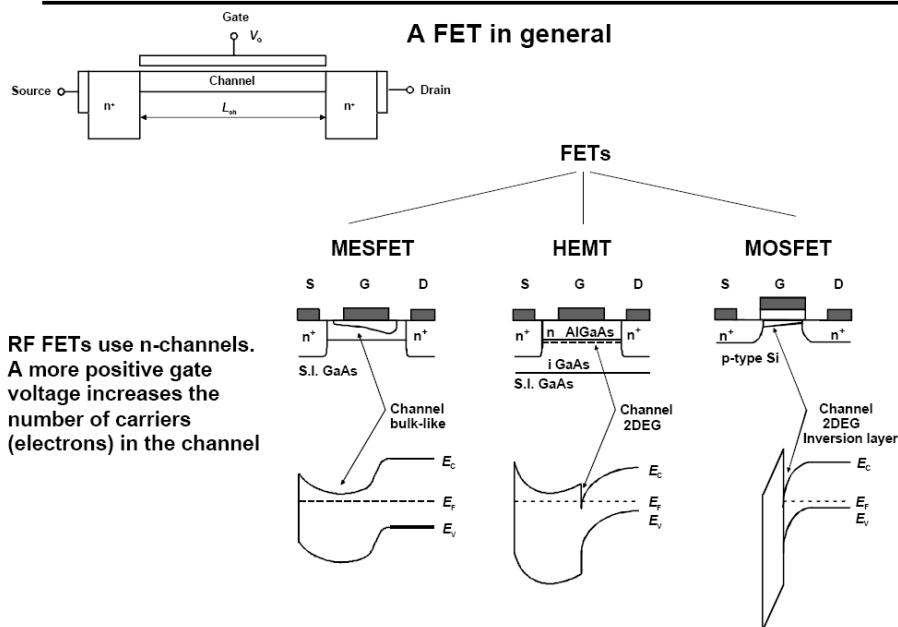
A comprehensive compilation of acronyms related to RF electronics can be found in:
F. Bashore, Acronyms Used by the RF/Microwave Industry
Pt. I: Microwave Journal, Feb. 1997, pp. 110-115
Pt. II: Microwave Journal, Feb. 1997, pp. 114-122

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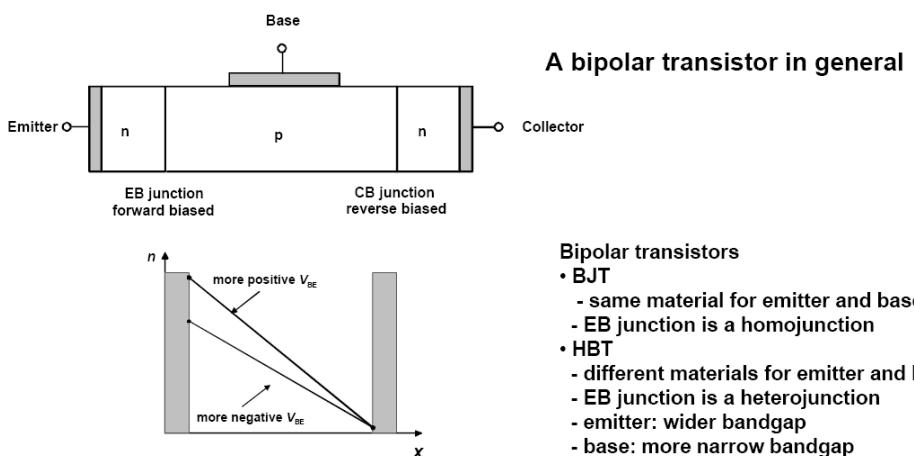
I – Transistor concepts

The following slides are taken from <http://www.teknik.uu.se/fte/courses/asd/>. A more exhaustive comparison between microwave transistor performances is given in Appendix II-1.

Transistor Concepts I - FETs



Transistor Concepts I - Bipolars



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II – Equivalent circuit parameter extraction

It exists several experimental techniques for transistor characterization. Selecting the appropriate measurement type depends on the application. For example, load-pull measurements can be selected if large-signal transistor characterization is required. However, the availability of such equipment severely limits the type of measurement selected. Load-pull setups are usually very expensive and other measurement strategies might be used as a substitute to a more desirable measurement method.

1 – Direct current-voltage measurements

The dc I-V measurement is the most fundamental of all device measurement methods. In this type of measurement, the most significant current component of the device is plotted against its corresponding device terminal voltage with respect to the common terminal; such dc device measurement has the advantage of being easy to perform even in simple laboratories and yet provides relatively good estimates for many device parameters.

For instance, microwave MESFETs are typically employed in the common source configuration: the drain current I_{ds} is plotted against the drain-source voltage V_{ds} while the gate-source V_{gs} voltage is held at a fixed value. A dc I-V family of curves can be generated by changing the V_{gs} values.

Modern laboratory equipment made it a fairly easy task to measure the dc I-V for a given device. With existing computer interfaces, such as the *General Purpose Interface Bus* (GPIB), many power supplies and multimeters can be programmed to automatically measure the device I-V curves. For such automated measurements to be performed reliably, chip and discrete components should be

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mounted on a well-designed test fixture to provide a 50Ω environment and hence prevent device oscillation.

On wafer devices, on the other hand, are mounted on microwave probe stations for dc and other high-frequency measurements. Those stations use coplanar transmission line probes, which bring 50Ω lines directly to the device terminals on the wafer. Coplanar lines exhibit less losses than the popular microstrip lines.

2 - Parameter measurements

The dc measurements alone are not sufficient for microwave device characterization. In fact, many small-signal model element values cannot be determined from dc measurements and can only be determined from RF measurements.

Scattering parameter measurements are the most popular RF device measurement technique. It is to be noted that S-parameter values depend on the DC bias condition of the device. In other words, if the bias point of the device changes, a new set of S-parameters will be required to characterize the device at the new bias point.

Automatic S-parameter measurement setups are readily available in most microwave laboratories. The measurement setup consists of computer controlled power supplies, multimeters, and most importantly the network analyzer. All the devices are connected to a computer through a general purpose interface and can be pre-programmed with a user friendly interface. Commercially available instrumentation software (e.g., LabView) can provide excellent environment for automated measurement. The device should be mounted on a suitably designed test fixture (for discrete or chip devices) with the accompanying calibration kit.

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The microwave S-parameter measurements can be very accurate even up to frequencies as high as 110 GHz (the Agilent 8510 Network Analyzer system).

The accuracy of the measurements depends mostly on the calibration and the ability to de-embed the test fixture. The two most common calibration techniques are the through-reflect-line (TRL) and the short-open-load through (SOLT).

3 - Pulsed I-V measurements

Although dc I-V measurements are easy to perform, device parameters, such as the transconductance and the output conductance, extracted from dc measurements are different from their RF counterparts. The dc parameter values can only be used as first approximations when seeking the device RF models. This is due to the low frequency dispersion characteristics of these parameters. Moreover, the dc measurements of the output current are not performed under isothermal conditions. For high currents in particular, the device temperature rises. For instance, as a consequence, the drain current of a FET decreases when the channel temperature rises.

Pulsed I-V measurements are preferred over the dc ones. They have the advantage that the transistor parameter values extracted from them are very close to the RF values. Under pulsed measurements, the DC output current of the device is constant and therefore the device is measured under isothermal conditions. Pulsed I-V measurements of FET/BJT are performed by applying pulsed voltage to either of the gate/base, the drain/collector, or both of them while dc biasing the device in the cut-off region. The pulse serves to drive the device into saturation for a very brief period of time that is short enough that the device does not heat-up. The pulsed drain/collector current is then measured by a current probe or any other measurement device. A schematic of a pulse measurement setup for the FET is shown in Figure II-10.

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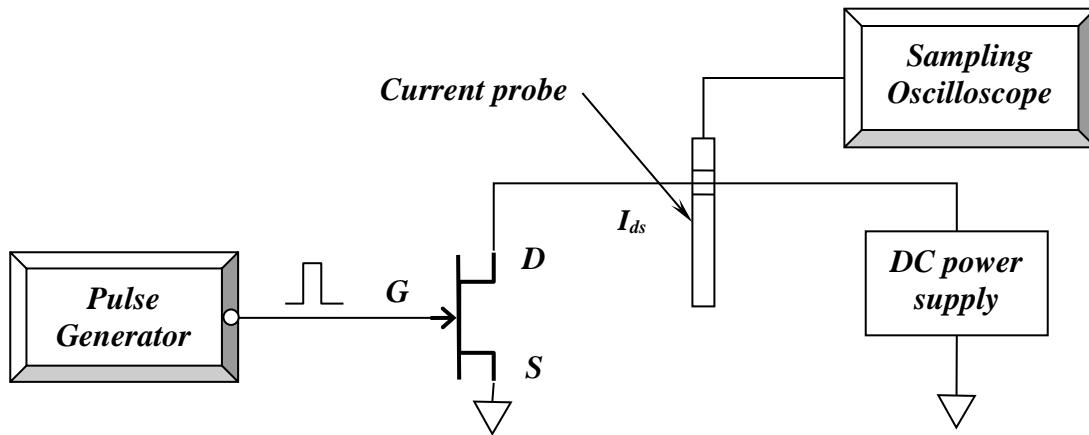


Figure II-10. Pulsed I-V measurement equipment configuration for the dual-gate FET.

4 – Load-pull measurements

In large-signal transistor circuits, such as power amplifiers and oscillators, small-signal RF characterization techniques (e.g. S-parameters) are not suitable. Due to the high power levels of these applications, the device behaves as a nonlinear element and linear characterization techniques render inaccurate results. Alternatively, large-signal measurement techniques have been developed. The most popular of them is the load-pull measurement.

Load pull measurements involve embedding the device to be tested into measurement circuitry that can be impedance tuned. The measurement system simultaneously monitors the tuned impedance of the characterization circuitry and the performance of the device. Device response is then recorded under the variable load conditions. The resulting loci of impedances required to obtain a constant performance parameter (i.e. output power or power added efficiency) are displayed on a smith chart in the form of closed contours. The load-pull contours are determined one frequency at a time. Also the load-pull contours apply to only one incident power level used in the measurement.

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Load-pull equipment configurations can be classified into two general categories. *Traditional* and *active-load* pull systems. Traditional load-pull systems utilize mechanical adjustments to change the circuit impedance. These include slide-screw tuners, dielectric slug tuned air lines, and microstrip tuning. Figure II-11 illustrates an equipment configuration that can be used for load pull measurements. Active-load pull measurement systems overcome many of the problems associated with traditional load-pull systems. In this method, two phase- and amplitude-controlled RF signals are applied to the device. No physical impedance tuner is required. The major advantage of this system is that the load reflection coefficient obtained is not limited in magnitude. By independently adjusting the input attenuators, virtually any reflection coefficient can be synthesized.

5 – Other measurement techniques

There exist several other large-signal measurement techniques for transistor characterization. These techniques are not widely used due to the expensive measurement equipment.

A list of some of them is given below:

1. Pulsed S-parameter measurements. Rather than using continuous wave (CW) S-parameter measurements dc bias conditions, Pulsed S-parameters under pulsed DC bias conditions can be a better alternative. Pulsed Bias/S-parameter measurements do not cause the device to overheat and therefore present better models under isothermal conditions.
 2. Multi-bias S-parameter measurement. In this technique, small-signal S-parameter measurements are done at many bias conditions to generate large-signal models.
 3. Two-tone harmonic content measurement. This technique is used to measure the nonlinear device behavior. In this technique, the output spectral content of the device is recorded while two input signals, closely spaced in the frequency and of equal magnitudes, are applied to the input of the device. The measurement is made for increasing input power levels.
-

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4. X-parameters measurements.

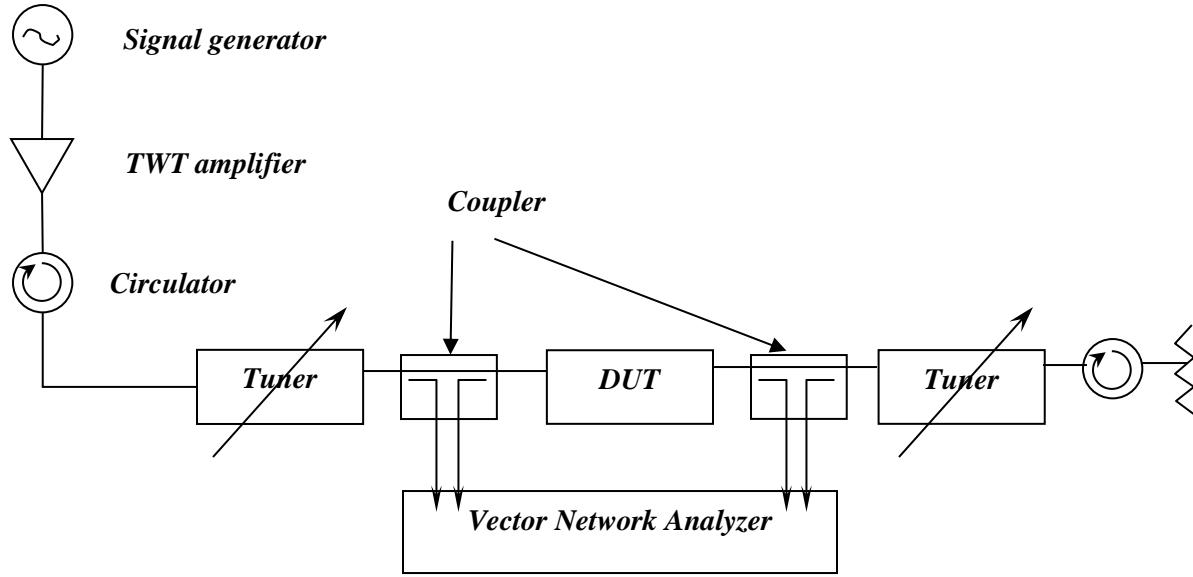


Figure II-11. Typical test equipment configuration for traditional large-signal load-pull measurements.

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III – Field effect transistors

For an exhaustive introduction to FETs, please refer to Appendix II-2.

1 – MESFET

MESFET ("MEtal Semiconductor Field Effect Transistor") is now one of the most used transistors in the upper part of the centimeter range and the lower part of the millimeter range. The MESFET modeling took several directions: physic-, electromagnetic-, and electric-based modeling (Figure II-12). As the two first require huge CPU time and memory, we will focus on the equivalent electrical circuit of a MESFET.

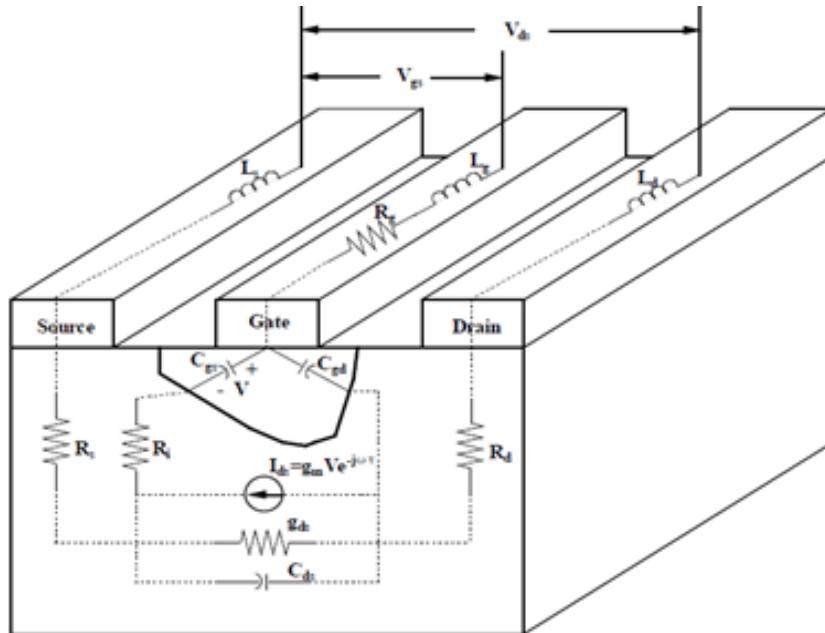


Figure II-12. Typical FET structure.

In this last area, the researchers privilege two directions:

- Parameter extraction with predefined topology and current-voltage equations. These last are often coupled with optimization and/or statistical techniques. The procedure follows one of these two options:
 - Get the S-parameters from measurements at different bias. Then, extraction programs allow obtaining the values of all linear and nonlinear equivalent circuit elements as function of bias voltages. As this experimental approach did not include heat dissipation and breakdown effects, the model is mainly a small signal model.
 - Measure the S-parameters at a given bias point in order to extract the linear element values and then perform pulsed measurements to evaluate the nonlinear elements of the equivalent electrical circuit of the transistor as function of the applied voltages. However, pulsed measurements cannot give the accurate values of differential elements like g_m and g_d which are very important, for example when one computes the intermodulation products. Moreover, the nonlinear resistive elements are not well characterized. These limitations can be significantly reduced if pulsed voltages are superposed to bias voltages to perform pulsed measurements.
- The second research axis uses various measurements: dc, small and large signal excitation, ... and is based on two major points:
 - Construct a topology for the equivalent electrical circuit that best fit the measurements for all frequency and Q point ranges.
 - Determine the relations between the elements and the applied voltages.

In the centimeter range, the most used equivalent circuit is the one shown in Figure II-13 where the two diodes D_a and D_g represent respectively the gate-drain breakdown effect (diode D_a) and the junction gate-channel current. On the other hand, the circuit shown in Figure II-14 is more efficient in the millimeter range.

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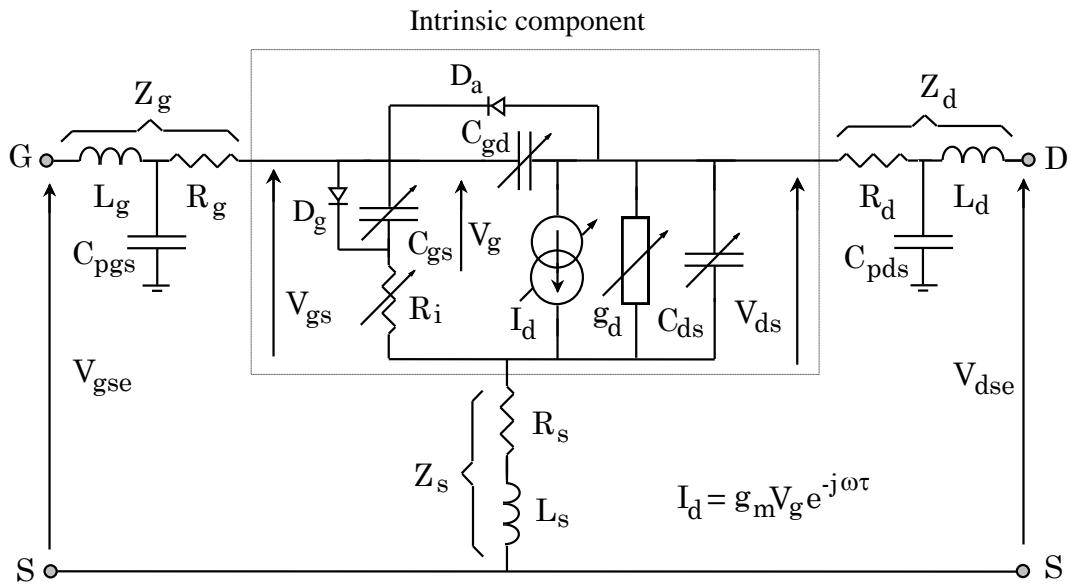


Figure II-13: MESFET equivalent electrical circuit for the centimeter range.

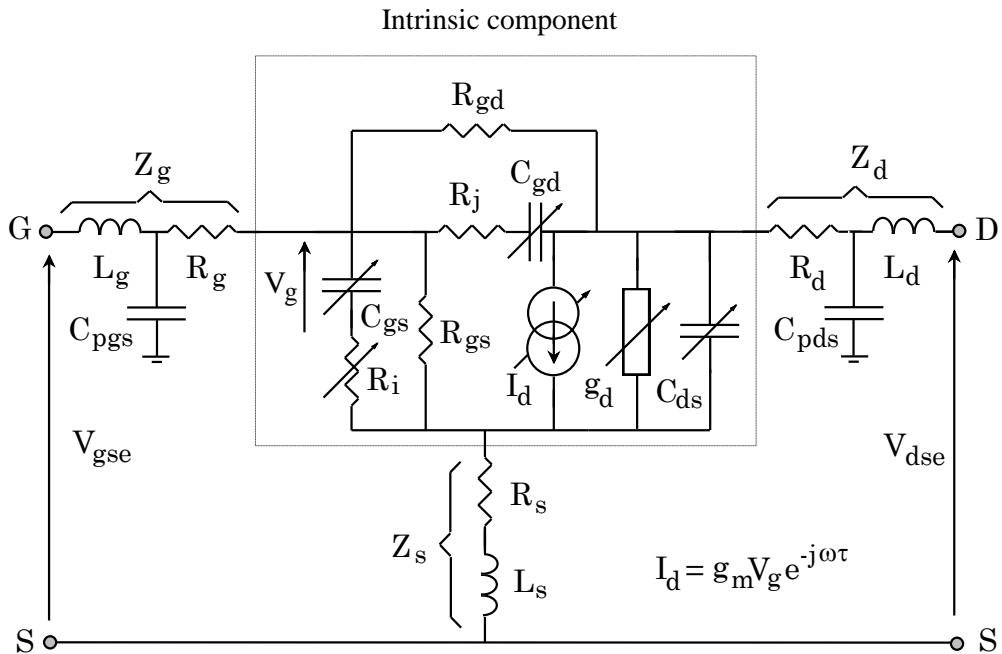


Figure II-14: MESFET equivalent electrical circuit for the millimeter range.

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Under large signal excitation, the main nonlinear elements in a decreasing scale order are:

- The drain current source I_d ,
- The gate-source capacitance C_{gs} ,
- The gate-drain capacitance C_{gd} .
- The output conductance g_d (or the equivalent output resistance R_{ds}),
- The drain-source capacitance C_{ds} ,
- The gate resistance R_i

a – Drain current source

If the dependence of the gate current in function of the gate-source voltage V_{gs} and drain-source voltage V_{ds} is relatively easy to model, the drain current source I_d is the most predominant nonlinear element in the circuit and then the most complex one to model. Many research works has been done in this field to approximate this current-voltage relationship (Figure II-15).

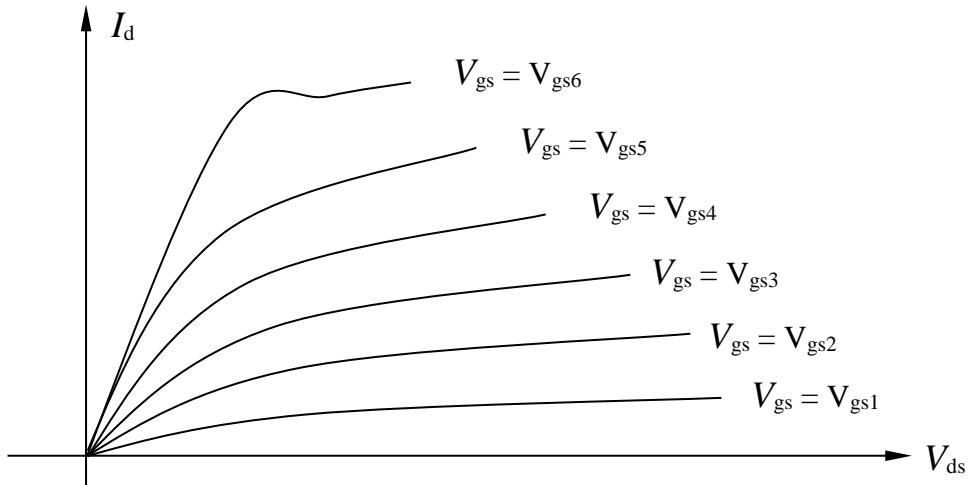


Figure II-15. DC characteristics of the drain current source $I_d(V_{gs}, V_{ds})$.

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To illustrate the huge amount of papers published and the complexity of these relationships, we can resume below some of the most important relationships, with the following notes

- We used the same notations as in the original papers,
- Variables like $a, b, \dots, a_j, \dots, k, m, q, \dots, \alpha, \beta, \gamma, w \dots$ are usually empirical parameters used to model the current-voltage behavior,
- I_{dss} is the saturation drain current for the bias point $\{ V_{gs} = 0, V_{ds} = V_{dss} \}$,
- I_{sr} is the inverse saturation current for the gate-drain junction,
- I_{dsp} is the current I_d when the transconductance g_m reached its maximum value,
- V_{bi} is the built-in voltage
- V_{po} is the pinch-off voltage. V_p is related to V_{po} using an empirical parameter α such as $V_p = V_{po} + \alpha V_{ds}$
- Other voltages like V_{dso}, V_{dsp}, \dots are used either to indicate the V_{ds} voltage value for which some empirical parameters are determined or as model parameters to improve sub-threshold and pinch-off regions (e.g., V_M).

Shockley (1952):

$$I_d = \beta(V_{gs} - V_{po})^n$$

Shichman-Hodges (1968):

$$\text{Ohmic region: } I_d = \beta V_{ds} (2(V_{gs} - V_{po}) - V_{ds})(1 + \lambda V_{ds})$$

$$\text{Saturation region: } I_d = \beta(V_{gs} - V_{po})(1 + \lambda V_{ds})$$

Taki (1978):

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_p - \sigma V_{ds}} \right)^2 \tanh \left(\alpha \left| \frac{V_{ds}}{V_p - \sigma V_{ds} - V_{gs}} \right| \right)$$

Curtice (1980):

$$I_d = \beta (V_{gs} - V_{po})^2 (1 + \lambda V_{ds}) \tanh (\alpha V_{ds})$$

Tajima 1 (1981):

$$I_d = I_{d1} \cdot I_{d2}$$

$$I_{d1} = 1 + \frac{V_{gs} - V_{bi}}{V_{po} + p V_{ds} + V_{bi}} - \frac{1}{m} + \frac{1}{m} \exp \left\{ -m \left(\frac{V_{gs} - V_{bi}}{V_{po} + p V_{ds} + V_{bi}} \right) \right\}$$

$$I_{d2} = \frac{I_{dsp} m}{m - [1 - \exp(-m)]} \left\{ 1 - \exp \left[-\frac{V_{ds}}{V_{dss}} - a \left(\frac{V_{ds}}{V_{dss}} \right)^2 - b \left(\frac{V_{ds}}{V_{dss}} \right)^3 \right] \right\}$$

Materka 1 (1983):

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_{po} + \gamma V_{ds}} \right)^2 \tanh \left(\frac{\alpha V_{ds}}{V_{gs} - V_p} \right)$$

Tajima 2 (1984):

$$I_d = I_{dss} \cdot F_g F_d + G_{d0} V_{ds}$$

$$F_g = \frac{1}{k} \left[1 + \frac{V_{gs}}{V_p} - \frac{1}{m} \left\{ 1 - \exp \left(-m \left(1 + \frac{V_{gs}}{V_p} \right) \right) \right\} \right] \quad G_{d0} = g_d \Big|_{v_{ds}=0}$$

$$F_d = 1 - \exp \left(-V_{dsn} - aV_{dsn}^2 - bV_{dsn}^3 \right) \quad V_{dsn} = \frac{V_{ds}}{V_{dsp} \left(1 + W \frac{V_{gs}}{V_p} \right)}$$

Materka 2 (1985):

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_{po} + \gamma V_{ds}} \right)^2 \left(1 + \frac{\eta V_{ds}}{I_{dss}} \right) \tanh \left(\frac{\alpha V_{ds}}{I_{dss} (1 - \lambda V_{gs})} \right)$$

Curtice-Ettenberg (1985):

$$I_d = (a_o + a_1 V + a_2 V^2 + a_3 V^3) \tanh (\alpha V_{ds})$$

$$V = V_{gs} \left(1 + \beta (V_{dso} - V_{ds}) \right)$$

Statz-Pucel "Raytheon model" (1987):

$$I_d = \begin{cases} \frac{\beta (V_{gs} - V_{po})^2}{1 + b (V_{gs} - V_{po})} (1 + \lambda V_{ds}) \left[1 - \left(1 - \alpha \frac{V_{ds}}{3} \right)^3 \right] & 0 < V_{ds} < \frac{3}{\alpha} \\ \frac{\beta (V_{gs} - V_{po})^2}{1 + b (V_{gs} - V_{po})} (1 + \lambda V_{ds}). & V_{ds} \geq \frac{3}{\alpha} \end{cases}$$

Hwang (1987):

$$I_d = \begin{cases} I_{dss} \left(1 - \frac{V_{gs}}{V_p} \right)^2 \tanh \left(\frac{\alpha V_{ds}}{V_{gs} - V_p} \right) & V_{ds} < V_{sat} \\ I_{dss} \left(1 - \frac{V_{gs}}{V_p} \right)^2 \tanh \left(\frac{\alpha V_{ds}}{V_{gs} - V_p} \right) - \frac{g_o V_{ds}}{(A - V_{gs})^q} & V_{ds} \geq V_{sat} \end{cases}$$

Vincent (1987):

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_p} \right)^2 \tanh \left(\frac{\alpha V_{ds}}{V_{gs} - V_p} \right) + F(V_{gs}, V_{ds})$$

and

$$F(V_{gs}, V_{ds}) = \begin{cases} 0 & V_{ds} < V_{sat} \\ -V_{ds} \cdot g_o [V_s - V_{gs}]^{-q} + I_{sr} \exp \{ \beta [V_{ds} - V_{gs}] \} & V_{ds} \geq V_{sat} \end{cases}$$

Plessey (1990):

$$\begin{aligned} I_d = I_{dss} \cdot \frac{(V_{gs} - V_{po})^2}{1 + b(V_{gs} - V_p)} (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \\ + \left(1 + \frac{V_{ds}}{V_p (1 - \beta V_{ds})} \right) g_{dp} V_{ds} \cdot \tanh(\alpha V_{ds}) \end{aligned}$$

Hu (1990):

$$I_d = \frac{\beta(V_{gs} - V_{po})^2}{1 + b(V_{gs} - V_{po})} (1 + \mu V_{gs} \exp\{\sigma V_{gs} V_{ds}\} + \lambda V_{gs} V_{ds}) \tanh(\alpha V_{ds})$$

TOM "TriQuint's Own Model" (1990):

$$I_d = \begin{cases} \frac{\beta(V_{gs} - V_p)^\varrho}{1 + \delta \beta V_{ds} (V_{gs} - V_p)^\varrho} \left[1 - \left(1 - \alpha \frac{V_{ds}}{3} \right)^3 \right] & 0 < V_{ds} < \frac{3}{\alpha} \\ \frac{\beta(V_{gs} - V_p)^\varrho}{1 + \delta \beta V_{ds} (V_{gs} - V_p)^\varrho} & V_{ds} \geq \frac{3}{\alpha} \end{cases}$$

Brazil (1991):

$$I_d = I_{dss} \left[1 + \tanh \left\{ 1 - \exp \left(\mu - \frac{\alpha (V_{gs} - V_{bi})}{V_{ds}^2 + V_{bi}} \right) \right\} \right] \tanh [\sigma V_{ds}]$$

Angelov (1992):

$$I_d = I_p \left(1 + \tanh \left[\sum \alpha_i (V_{gs} - V_{po} - \gamma V_{ds}) \right] [1 + \lambda V_{ds}] \tanh [\sigma V_{ds}] \right)$$

Rodriguez (1992):

$$I_d = \beta (V_{gs} - V_{po} + \gamma V_{ds})^2 (1 + \lambda V_{ds}) \tanh (\alpha V_{ds})$$

Teyssier (1994):

$$I_d = I_{dss} \cdot a \left\{ 1 + \beta (V_{ds} - V_{dm}) \left(1 + \tanh \left\{ \alpha (V_{gs} - V_{gm}) \right\} \right) \right\}$$

Fernández (1996):

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_{po} + \gamma V_{ds}} \right)^{\mu + \beta V_{gs}} \cdot (1 + \eta V_{ds}) \tanh \left(\frac{\alpha V_{ds}}{I_{dss}} \right)$$

Ooi (2002):

$$I_d = b_1 V_{ds} V_{eff}^3 + \frac{b_4 V_{ds} (b_2 + b_3 V_{ds}) V_{eff}^2}{\sqrt{(1 + g V_{gst})^2 + V_{ds}^2} (b_2 + b_3 V_{ds})^2} + \frac{b_5 V_{ds} (b_2 + b_3 V_{ds}) V_{eff}}{\sqrt{(1 + g V_{gst})^2 + V_{ds}^2} (b_2 + b_3 V_{ds})^2}$$

$$V_{gst} = V_{gs} - V_{bi} + \gamma V_{ds}$$

$$V_{eff3} = 0.5 \left(V_{gst} (1 + c) + \sqrt{V_{gst}^2 + V_M^2} (1 - c) \right)$$

$$V_{eff} = V_M (1 + M V_{ds}) \ln \left(1 + \exp \left(\frac{V_{eff3}}{V_M (1 + M V_{ds})} \right) \right)$$

Angelov (2005):

$$I_d = 0.5 (I_{dsp} - I_{dsn})$$

$$I_{dsp} = I_{pk0} \left[1 + [\tanh(\psi_p)]^* [\tanh(\alpha_p V_{ds})]^* [1 + \lambda_p V_{ds} + L_{SB0} \exp(V_{dg} - V_{tr})] \right]$$

$$I_{dsn} = I_{pk0} [1 + [\tanh(\psi_n)] * [1 - \tanh(\alpha_n V_{ds})] * [1 + \lambda_n V_{ds}]]$$

$$\psi_p = \sum_{i=1}^3 P_{im} (V_{gs} - V_{pk})^i \quad \psi_n = \sum_{i=1}^3 P_{im} (V_{gd} - V_{pk})^i$$

...

From this huge number of models, how to select the most suitable model?

The choice is based not only on the desired device performance, but also on the transistor size, the Q point variations, the temperature behaviour, the gain, the input/output power range, For example, Materka's model is very efficient in the linear region of the current-voltage curves. On the other hand, Curtice and Statz models are preferred for small transistors and Rodriguez's model presents many advantages in the knee region.

Some other researchers have concentrated their efforts to the generation of more general expressions in the form of analytical or semi analytical relations like Madjar (1988):

$$I_d = \alpha (1 + mV_{ds}) \tanh\left(\frac{V_{ds}}{V_a(V_{gs})}\right) + G_1(V_{gs}) \left(\frac{dV_{gs}(t-\tau)}{dt} \right) + G_2(V_{ds}) \left(\frac{dV_{ds}}{dt} \right)$$

These relations are certainly more accurate and general than the empirical ones, but they use physical transistor parameters, which are not available to all users and designers.

In practice, the most used models in circuit simulators like Cadence®, Spice®, Libra®, Compact®, MDS®, Touchstone®, Serenade®, ADS® ... are Materka, TOM, Angelov, Statz-Pucel, and cubic Curtice models.

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b – Nonlinear capacitances

Similarly, several nonlinear capacitance equations have been published by different authors to model the C_{gs} and C_{gd} behaviors. For example, Statz and Pucel (1987) proposed the following relations:

$$C_{gs} = \frac{C_{gso}(1+K_1)(1+K_2)}{4} \left(1 - \frac{V_1}{V_{bi}}\right)^{-\frac{1}{2}} + \frac{C_{gdo}(1-K_2)}{2} \quad (\text{II-15-a})$$

$$C_{gd} = \frac{C_{gdo}(1+K_1)(1-K_2)}{4} \left(1 - \frac{V_1}{V_{bi}}\right)^{-\frac{1}{2}} + \frac{C_{gso}(1+K_2)}{2} \quad (\text{II-15-b})$$

with

$$V_e = \frac{1}{2} \left(V_{gs} + V_{gd} + \sqrt{(V_{gs} - V_{gd})^2 + \delta^2} \right) \quad V_n = \frac{1}{2} \left(V_e + V_t + \sqrt{(V_e - V_t)^2 + \delta^2} \right)$$

$$K_1 = \frac{V_e - V_t}{\sqrt{(V_e - V_t)^2 + \delta^2}} \quad K_2 = \frac{V_{gs} - V_{gd}}{\sqrt{(V_{gs} - V_{gd})^2 + \left(\frac{1}{\alpha}\right)^2}}$$

where C_{gso} and C_{gdo} are the respective values of C_{gs} and C_{gd} at zero voltage and δ is the transition width voltage. Since these relations are also very complex to manipulate, many designers have opted for the classical equation of a junction capacitance:

$$C_{gs} = C_{gso} \left(1 - \frac{V_{gs}}{V_{bi}} \right)^{-\gamma} \quad C_{gd} = C_{gdo} \left(1 - \frac{V_{gd}}{V_{bi}} \right)^{-\gamma} \quad (\text{II-16})$$

2 – HEMT

In the recent years, High Electron Mobility Transistor (HEMT) emerged as a promising transistor with its smaller noise figure and higher cut-off frequency compared to MESFET. The most popular is the pseudomorphic HEMT or pHEMT. Moreover, it exhibits a better mobility, which implies higher transconductance and less effect of parasitic capacitances. The drain current modeling has also been the subject of many papers as:

Mahon "Core model" (1992):

$$I_d = \begin{cases} 0 & V_{ds} < 0 \\ \left(1 - \left(1 - \frac{V_{ds}}{V_{dss}}\right)^2\right) I_{dss} & 0 \leq V_{ds} \leq V_{dss} \\ I_{dss} & V_{dss} < V_{ds} \end{cases}$$

Chen (1995):

$$I_d = I_{dss} \tanh \left[\left(10^{\sum_{k=0}^4 a_k V_{gs}^k} - 1 \right) V_{ds} - \left(10^{\sum_{k=0}^4 b_k V_{gs}^k} - 1 \right) V_{ds}^2 \left(10^{\sum_{k=0}^4 c_k V_{gs}^k} - 1 \right) V_{ds}^3 \right]$$

Shirakawa (1996):

$$I_d = V_o e^{V_g} \left(\delta \left(1 + \alpha \tan^{-1} \beta (V_{gs} - V_{go}) - V_{g1} \right) V_{ds} + \tanh(\lambda V_{ds}) \right)$$

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Tanimoto (1996):

$$I_d = \left(\frac{a_o e^{a_1 V_{gs}}}{1 + a_o a_2 e^{a_1 V_{gs}}} \right) + (\beta [1 + \lambda V_{ds}] \tanh [\alpha V_{ds}])$$

$$\beta = \frac{\beta_1 V_{gs}^2}{1 + \beta_2 V_{gs} + \beta_3 V_{gs}^2 + \beta_4 V_{gs}^3 + \beta_5 V_{gs}^4}$$

$$\alpha = \alpha_o + \alpha_1 \exp \left(- \left(\frac{V_{gs} - \alpha_2}{\alpha_3} \right)^2 \right)$$

Other variants of these transistors are MODFET ("MOdulation-Doped Field Effect Transistor"), SDHT ("Selectively Doped Heterostructure Transistor"), TEGFET ("Two-dimensional Electron Gas FET"), PHFET ("Pseudomorphic Heterostructure FET") or non-doped transistors like SISFET, MISFET, HIGFET,

If the equations are not similar to those used for MESFET, HEMT equivalent electrical circuits are practically identical to MESFET circuits. Moreover, the same remarks for MESFET capacitances can be applied to HEMT capacitances. For example, Tanimoto proposed the following complex relation for both C_{gs} and C_{gd} :

$$C = (1 - \tanh [\alpha V_{ds}]) \beta_o + \tanh [\alpha V_{ds}] (\beta_1 + \beta_2 V_{gs} + \beta_3 \tanh \{\beta_4 (V_{gs} - \eta)\}) \quad (\text{II-17})$$

3 – Dual-gate FET

Presented first by Turner, dual-gate FET transistors have two parallel gates that are electrically independent, Figure II-16. For common use, the configuration is common-source with the excitation signal applied to the first gate while the second one is grounded.

If the second gate is positively biased, the gain will significantly increase *without* changing the *gain*Bandwidth* product; the circuit is equivalent to a cascode circuit common source + common gate as shown in Figure II-17.

Compared to a simple FET, the unilateral parameter S_{12} of a dual-gate transistor is much smaller and its gain and noise figure can be significantly improved if the pinch-off voltage of the second gate is greater than the one of the first gate.

These FETs are used efficiently in mixing and modulation (because of the natural isolation between signals). Other applications as switches and logic ports are reported in the literature. However, their use is limited by the complexity of their models.

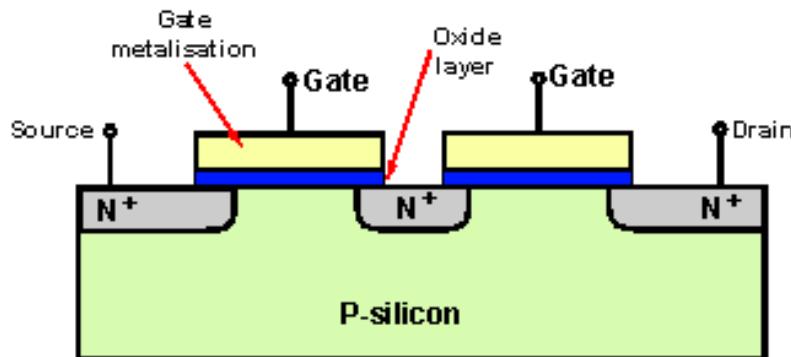


Figure II-16. Typical dual-gate FET structure (from radio-electronics.com)

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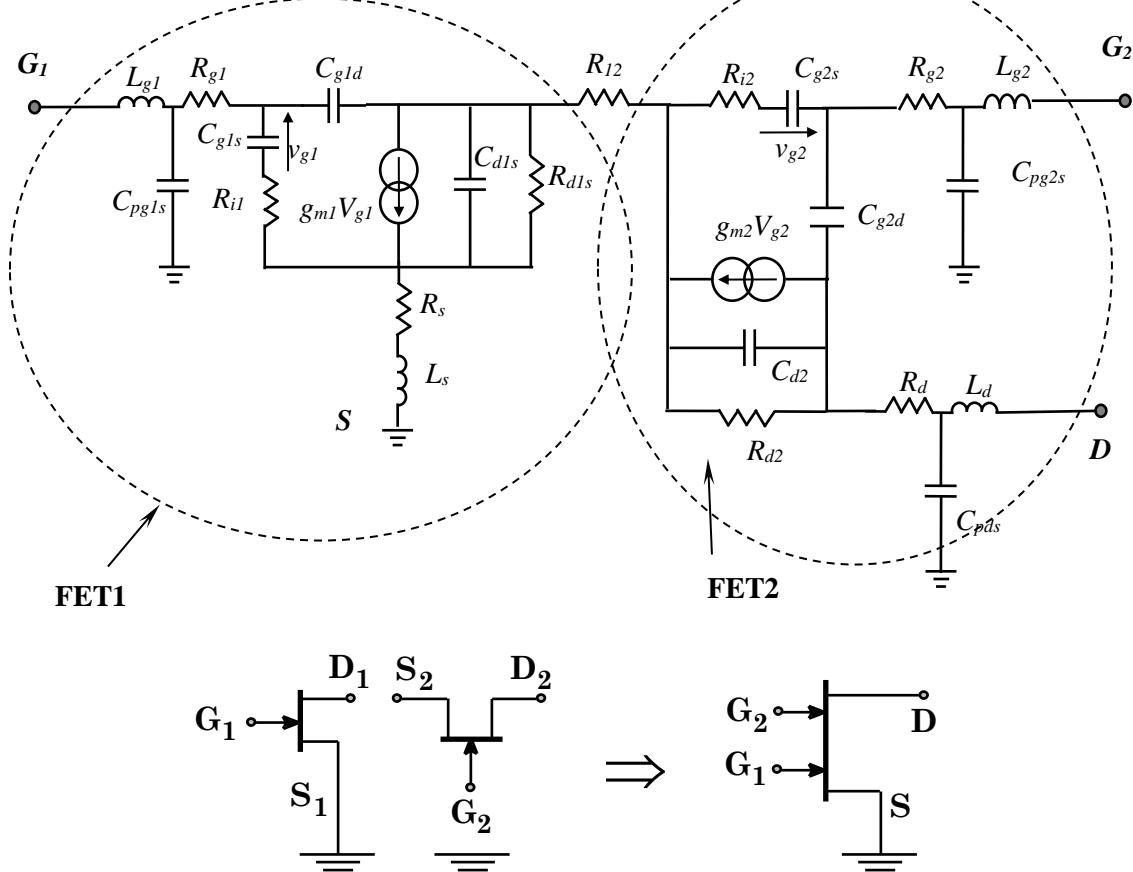


Figure II-17. Dual-gate transistor configuration as two transistors in cascode.

4 – FET intrinsic admittance matrix

According to the π topology, the admittance matrix can easily describe the equivalent circuit of MESFET or HEMT.

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Centimeter range: [Y^C]

$$Y_{11}^C = \frac{R_i C_{gs}^2 \omega^2}{1 + \omega^2 C_{gs}^2 R_i^2} + j\omega \left(\frac{C_{gs}}{1 + \omega^2 C_{gs}^2 R_i^2} + C_{gd} \right) \quad (\text{II-18-a})$$

$$Y_{12}^C = -j\omega C_{gd} \quad (\text{II-18-b})$$

$$Y_{21}^C = \frac{g_m \exp(-j\omega\tau)}{1 + jR_i C_{gs} \omega} - j\omega C_{gd} \quad (\text{II-18-c})$$

$$Y_{22}^C = g_d + j\omega (C_{ds} + C_{gd}) \quad (\text{II-18-d})$$

Millimeter range: [Y^M]

$$\begin{aligned} Y_{11}^M &= \frac{R_i C_{gs}^2 \omega^2}{1 + \omega^2 C_{gs}^2 R_i^2} + \frac{R_j C_{gd}^2 \omega^2}{1 + \omega^2 C_{gd}^2 R_j^2} \\ &\quad + \frac{1}{R_{gs}} + \frac{1}{R_{gd}} + j\omega \left(\frac{C_{gs}}{1 + \omega^2 C_{gs}^2 R_i^2} + \frac{C_{gd}}{1 + \omega^2 C_{gd}^2 R_j^2} \right) \end{aligned} \quad (\text{II-19-a})$$

$$Y_{12}^M = -\frac{R_j C_{gd}^2 \omega^2}{1 + R_j^2 C_{gd}^2 \omega^2} - \frac{1}{R_{gd}} - \frac{j\omega C_{gd}}{1 + R_j^2 C_{gd}^2 \omega^2} \quad (\text{II-19-b})$$

$$Y_{21}^M = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega R_i C_{gs}} - \frac{R_j C_{gd}^2 \omega^2}{1 + R_j^2 C_{gd}^2 \omega^2} - \frac{1}{R_{gd}} - \frac{j\omega C_{gd}}{1 + R_j^2 C_{gd}^2 \omega^2} \quad (\text{II-19-c})$$

$$Y_{22}^M = g_d + \frac{R_j C_{gd}^2 \omega^2}{1 + R_j^2 C_{gd}^2 \omega^2} + \frac{1}{R_{gd}} + j\omega \left(C_{ds} + \frac{C_{gd}}{1 + R_j^2 C_{gd}^2 \omega^2} \right) \quad (\text{II-19-d})$$

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IV – Bipolar transistors

1 – Equivalent circuit model

Due to their junction capacitance limitations (commutation time), bipolar junction transistors are replaced by HBTs (Heterojunction Bipolar Transistors) in the high microwave frequency range. In fact, HBTs have many advantages. A low doping of emitter and collector can reduce the transit capacitances and a high doping of base can increase significantly the power gain (by reducing the base resistance). For its modeling, several models have been proposed. The “T” scheme is one of the most popular ones (Figure II-18).

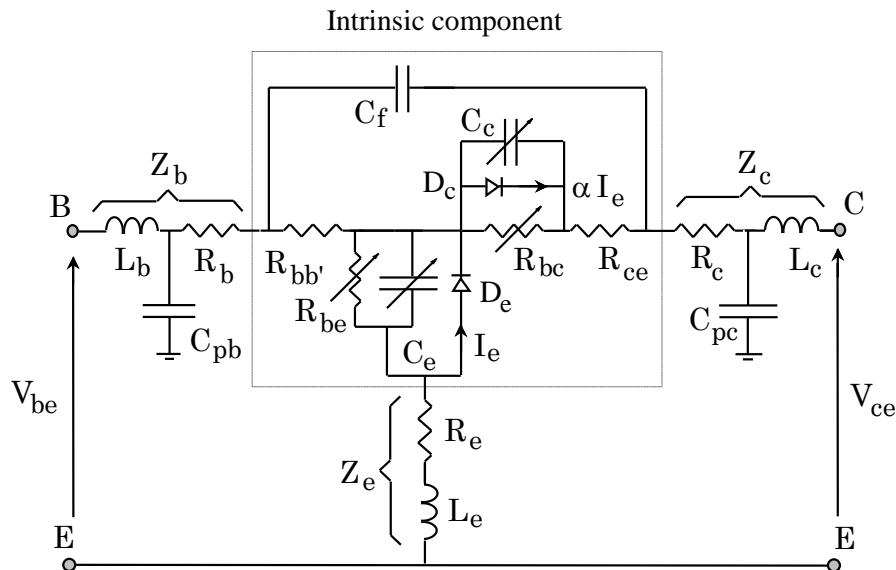


Figure II-18. Equivalent circuit of HBT.

The main nonlinear elements are the capacitances C_c and C_e , the resistances R_{be} and R_{bc} , and the emitter current I_e (in the relation, α is the transport factor, function of the operating frequency, transit time, ...). Two models proposed by Ebers-Moll and Gummel-Poon can model this source.

Ebers-Moll model: the current I_e is coupled to the collector current I_c

$$I_e = I_{es} \left(\exp\left(\frac{V_{eb}}{V_t}\right) - 1 \right) - \alpha_r I_{cs} \left(\exp\left(\frac{V_{cb}}{V_t}\right) - 1 \right) \quad (\text{II-20-a})$$

$$I_c = -\alpha_f I_{es} \left(\exp\left(\frac{V_{eb}}{V_t}\right) - 1 \right) + I_{cs} \left(\exp\left(\frac{V_{cb}}{V_t}\right) - 1 \right) \quad (\text{II-20-b})$$

V_t is the threshold voltage and "e, b, c" state for respectively the emitter, the base and the collector.

Gummel-Poon model: the current I_e is function of the base-emitter current I_{ee} and the base-collector current I_{cc}

$$I_e = \beta_f I_{ee} - \beta_r I_{cc} \quad (\text{II-21})$$

where β_f and β_r are respectively the current gains for forward and inverse bias.

2 – Intrinsic admittance matrix

The intrinsic admittance matrix of HBT is given by

$$Y_{11} = \frac{Z_e + R_c + Z_q - \alpha Z_q}{D} + j\omega C_f \quad (\text{II-22-a})$$

$$Y_{12} = \frac{-Z_e}{D} - j\omega C_f \quad (\text{II-22-b})$$

$$Y_{21} = \frac{-Z_e + \alpha Z_q}{D} - j\omega C_f \quad (\text{II-22-c})$$

$$Y_{22} = \frac{Z_e + R_{bb'}}{D} + j\omega C_f \quad (\text{II-22-d})$$

with

$$Z_q = 1/(R_{cb}^{-1} + j\omega C_c) \quad Z_e = 1/(R_{be}^{-1} + j\omega C_e)$$

$$D = \det \begin{bmatrix} Z_e + R_{bb'} & Z_e \\ Z_e - \alpha Z_q & Z_e + R_c + Z_q - \alpha Z_q \end{bmatrix}$$

V – Determination of the overall [S] matrix

To determine the overall S-matrix of HBTs and FETs, some manipulations are required. These transformations are very useful if one wants to extract or characterize these transistors. Let us define the intrinsic admittance matrix as $[\mathbf{Y}_{\text{int}}]$. Figure II-19 summarizes the process. If we can neglect the parasitic capacitances C_1 , C_2 and C_3 , the overall impedance matrix is

$$[\mathbf{Z}_T] = \begin{bmatrix} (R_1 + R_3) + j\omega(L_1 + L_3) & R_3 + j\omega L_3 \\ R_3 + j\omega L_3 & (R_2 + R_3) + j\omega(L_2 + L_3) \end{bmatrix} + [\mathbf{Y}_{\text{int}}]^{-1} \quad (\text{II-23})$$

F – TRANSISTORS: COMPARISON

I – Hetero-structures versus classical structures

The following slides are taken from <http://www.teknik.uu.se/fte/courses/asd/>

Heterostructures

Heterostructures

- are semiconductor structures consisting of at least two different semiconductors
- are uncommon in mainstream electronics
- are frequently used in RF transistors
 - FETs: HEMTs
 - Bipolars: HBTs
- The RF transistors showing
 - the highest f_T and f_{max}
 - the highest output power densities
 - the lowest noiseare heterostructure transistors.

Therefore it is useful to discuss some aspects of heterostructures in the following.

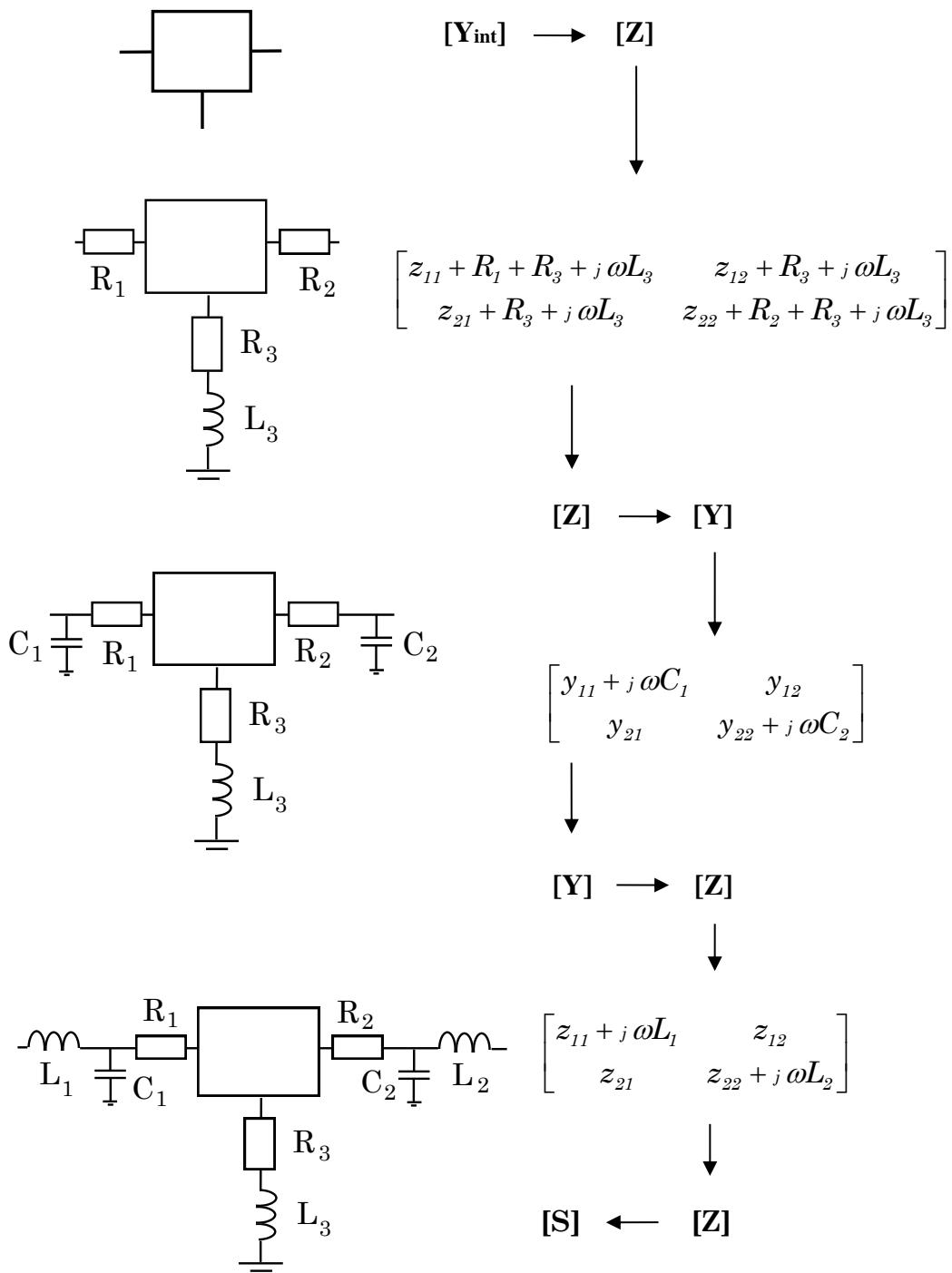


Figure II-19. Overall $[S]$ matrix determination from the intrinsic admittance matrix $[Y_{int}]$.

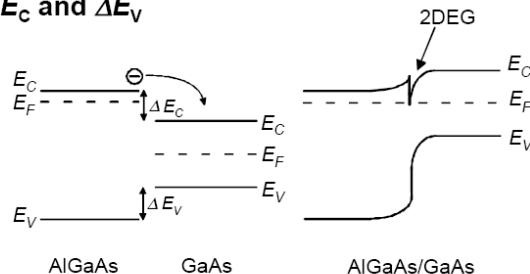
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Heterostructures

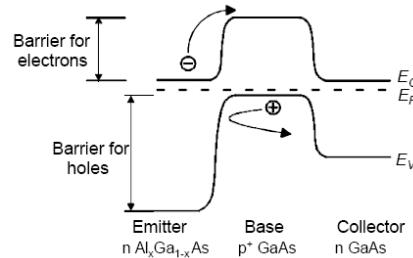
The physics exploited in RF heterostructure transistors

Most important: band offsets ΔE_C and ΔE_V

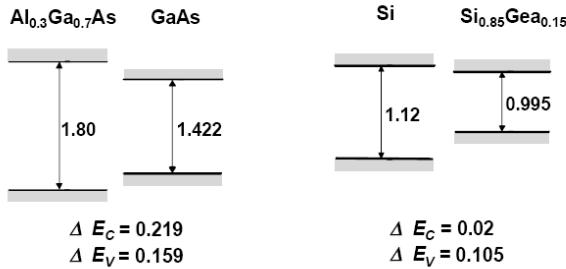
HEMTs
(here: AlGaAs/GaAs HEMT)



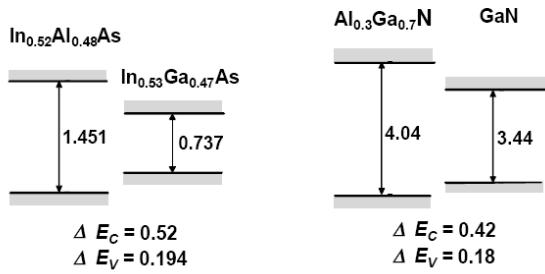
HBTs
(here: AlGaAs/GaAs HBT)



Heterostructures



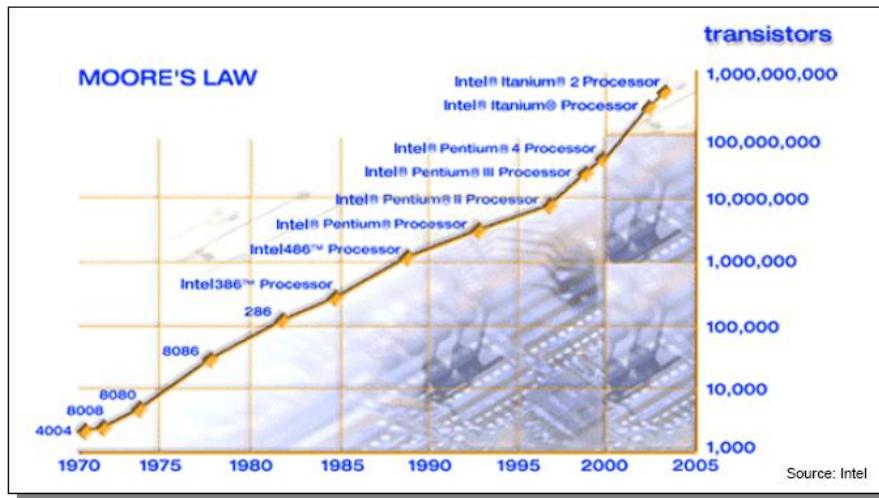
Semiconductor pairs
frequently used in
heterostructures



II – Evolution of Si technology

Even if hetero-structures are more and more used in RF/microwave applications, silicon transistors are encountered an enormous development in the last few years as shown in the following slide from www.target-org.net

Enormous development of silicon technology



Silicon for RF (applications)

Microwave applications:

- Cell phones (0.85-2.6 GHz)
- GPS (1.8 GHz)
- WLAN (2.4 GHz)
- Bluetooth (2.4 GHz)
- WLAN (5 GHz)
- DBS (12 GHz)
- HiperLink (17 GHz)
- LMDS (27-35 GHz)
- MVDS (44 GHz)
- CAR (77 GHz)
- Radio astronomy (>100 GHz)

Silicon dominates up to around 3-5 GHz.

This is also the field for the real mass markets.

Note: Microprocessors today operates above 3 GHz!

G – TRANSISTORS: FUTURES PERSPECTIVES

The desire for manufacturability-driven design and time-to-market in the microwave industry demands powerful and efficient computer-aided design (CAD) tools. With shrinking design margins and desire for first pass success, statistical analysis and yield optimization taking into account process variations and manufacturing tolerances in electronic devices and packages become necessary. This trend leads to massive and highly repetitive computational tasks during simulation, statistical design and optimization. However, combining large-scale circuit simulation and electromagnetic analysis inside an optimization and statistical design loop is extremely computationally challenging using conventional methods, so that fast and accurate models are required. This tendency, accentuated by the rapid grow of mobiles, satellite links, ..., has engendered a huge demand of models. As every one has his own advantages and disadvantages, the main problem for a designer is often to make the right decision regarding the model choice.

Depending on applications, it is preferable that devices have some of the following features:

- maximum gain,
- minimum noise figure and/or low 1/f noise,
- maximum conversion gain,
- low intermodulation products,
- maximum power-added efficiency,
- low thermal resistance,
- high temperature of operation and reliability,
- low on-resistance/high-off resistance,
- high linearity or nonlinearity,
- low power dissipation,
- low leakage current under cut-off operation,

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- low single power supply,
- semi-insulating substrate,
- mature technology, and low cost.

Table II-1 (from early 2000) shows that comparatively to D-mode FETs ("depletion-mode"), E-mode FETs ("Enhancement-mode") avoid the need of a second bias network than can save significant space for monolithic circuits.

On the other side, they exhibit a poor linearity for digital systems (SD) due to their low power added efficiency η (PAE) defined as

$$\eta = \frac{P_{output} - P_{input}}{P_{bias}} \quad (\text{II-24})$$

Other aspects should be also highlighted to predict the future of RF/microwave active device technology.

Scaling of active devices is, for instance, one of the major challenges in the RF/microwave area. As mentioned in www.target-org.net, "in 1965 Gordon Moore predicted an exponential growth of the semiconductor industry driven by market expectations –and it is still going on."

Table II-1. Comparison of various semiconductor device technologies.

Capability	D-Mode		E-Mode		GaAs HBT	SiGe		
	FET	HEMT	FET	HEMT		HBT	Si BJT	Si MOSFET
Linearity	+	+	0	0	++	0	-	-
Noise figure	+	++	+	++	-	0	-	-
Power	++	++	+	+	++	++	++	++
PAE	++	++	0	0	+	+	+	+
Control circuits	++	++	+	+	0	+	-	-
Mixers/oscillators								
Passive components	+	+	+	+	+	-	-	-
Integration on a single chip	++	+	-	-	0	0	0	0
Single polarity supply	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Turn-on voltage control	0	0	0	0	++	++	++	+
Multiple thresholds	++	-	+	-	N/A	N/A	N/A	++
Low-voltage operation	++	++	+	+	+	0	0	-
Maximum operating temperature	++	++	++	++	+	0	0	0
T _j (max) (°C)	150	150	150	150	125	125	125	125
Wafer size (mm)	100	100	100	100	100	200	200	200
Technology maturity	+	0	+	0	+	-	++	++
Cost	Moderate	High	Moderate	High	Moderate-High	Low	Low	Low
Maximum frequency of operation	+	++	+	++	+	+	0	0

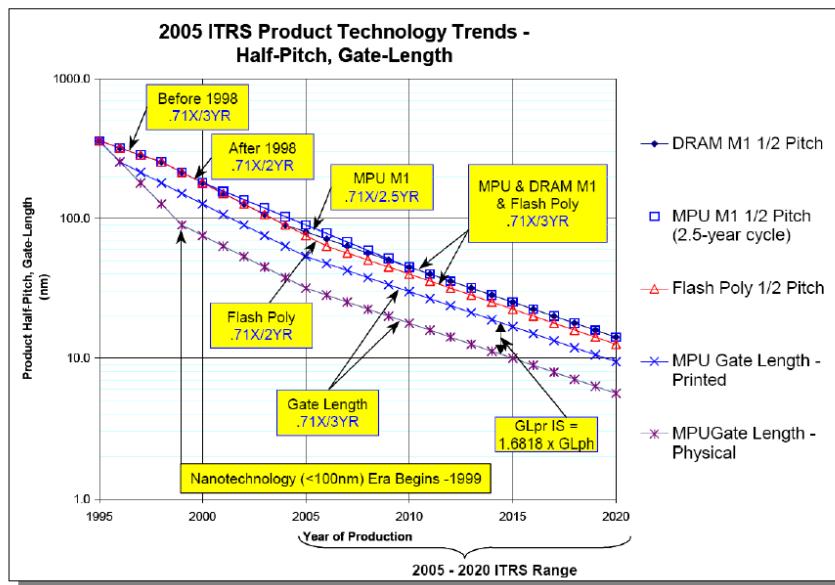
++, Excellent; +, Good; 0, Fair; -, Poor

In fact, Dimensions of MOSFETs have continuously been decreased, implying:

- Faster transistors;
- More transistors per chip;
- More chip per wafer;
- Technological solutions have been invented;
- Self-alignment;
- Silicidation;
- Amazing development of manufacturing equipment, etc

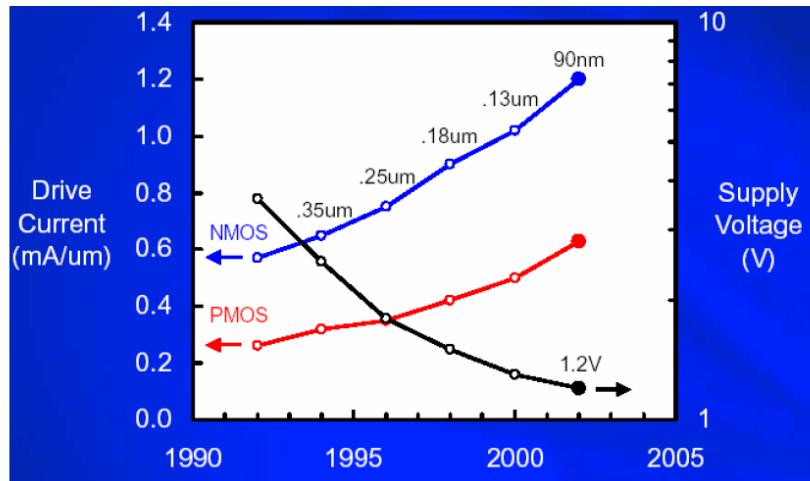
ITRS (International Roadmap for Semiconductors) describes the necessary and expected development (slides from www.target-org.net)

Example: scaling trend of gate length Lg



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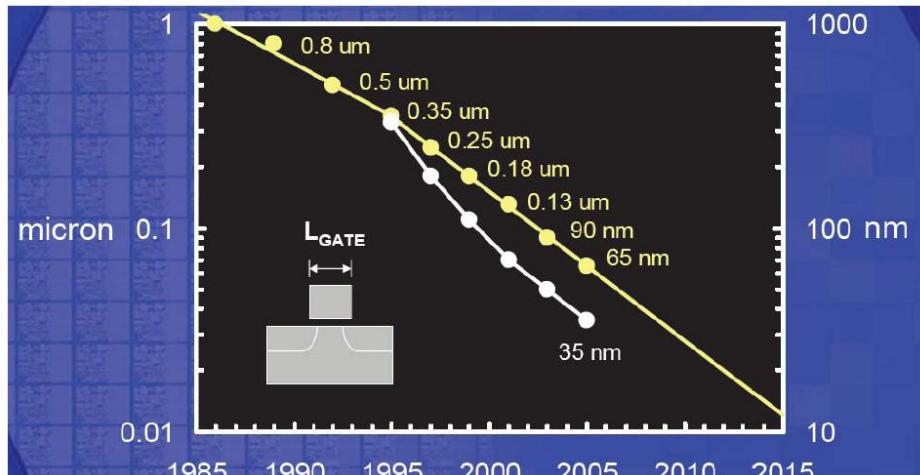
Result of scaling



Source: Intel

Aggressive scaling of L_G

Faster gate length scaling to maintain transistor performance

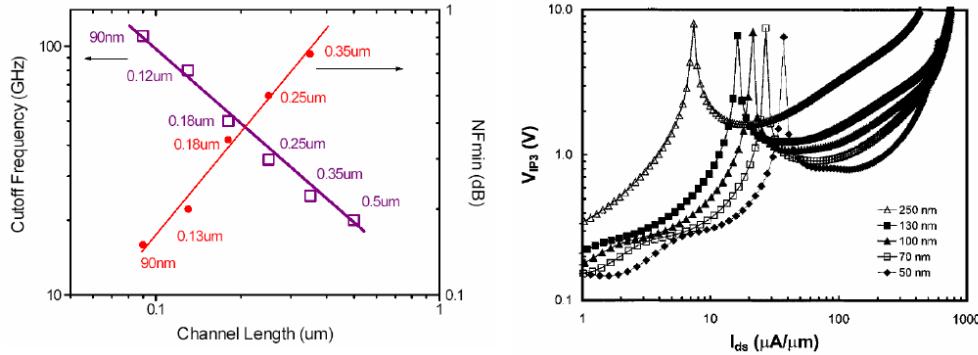


Source: Intel

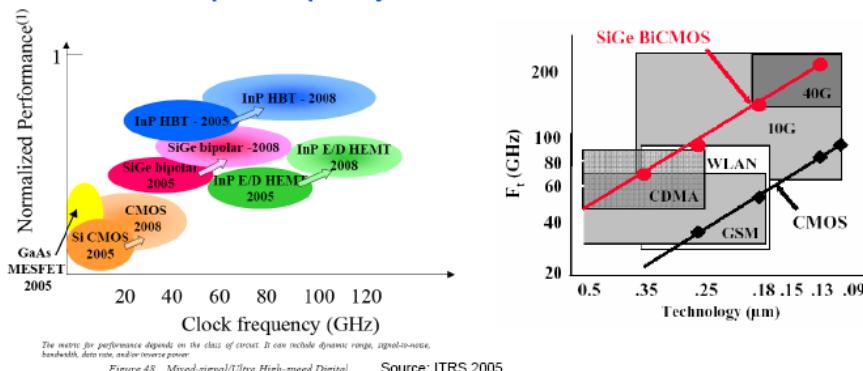
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RF performance vs. scaling

- In general RF-CMOS performance increases strongly with transistor scaling
- Linearity performance may be a problem – alternative scaling methodology can reduce the problem



- RF-CMOS is today a well established technology and has found many applications up to around 5 GHz
- Further scaling of CMOS predicts even better RF-performance and extends up in frequency

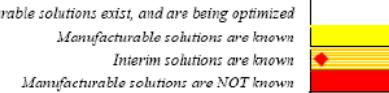


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Table 40a High-Performance Logic Technology Requirements—Near-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM $\frac{1}{2}$ Pitch (nm) (contacted)	80	70	63	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) $\frac{1}{2}$ Pitch (nm) (contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
L_g : Physical Gate length for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
<i>EOT: Equivalent Oxide Thickness</i> [2]									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
<i>Gate Poly Depletion and Inversion-Layer Thickness</i> [3]									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
<i>EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion</i> [4]									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
$J_{g,limit}$: Maximum gate leakage current density [5]									
Extended Planar Bulk (A/cm ²)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm ²)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm ²)							6.25E+02	7.86E+02	8.46E+02
V_{dd} : Power Supply Voltage (V) [6]	1.1	1.1	1.1	1	1	1	1	0.9	0.9
$V_{t,sat}$: Saturation Threshold Voltage [7]									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185



Source: ITRS 2005

H – SUMMARY

A summary of uses and characteristics of solid-state devices described in this chapter is presented in Table II-2.

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Table II-2. Uses and characteristics of solid-state devices described in this chapter
 (the frequency range is as of date 2001. These ranges change yearly).

Device	Frequency Range	Uses and Characteristics
Schottky-barrier Diode	From RF to sub-millimeter range	Mixers, modulators, and detectors. Occasionally used for frequency multipliers and switches.
PN-Junction Varactor	Up to 60GHz	Frequency multipliers, voltage controlled oscillators.
Schottky Varactor	To several hundred GHz	Frequency multipliers, voltage controlled oscillators.
SRD	Up to 30GHz	Frequency multipliers with fast pulses and high-order frequency multiplication.
BJT	Usually X-band and below. Mm-wave BJTs have been made	Small-signal amplifiers with moderate noise. Fast digital circuits. Good power devices. Low 1/f noise makes them ideal for low-noise oscillators.
HBT	Although some HBTs may have gain at 80GHz, practical limits are around 60GHz.	Power amplifiers, low-noise oscillators. Fast analog circuits. Lower 1/f noise than MESFETs and HEMTs. Preferred for oscillators.
JFET	Up to the VHF/UHF range	Low-cost. Moderately low-noise applications in amplifiers, mixers, oscillators, and switches.
Device	Frequency Range	Uses and Characteristics

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MESFET	Up to 40GHz. Can go higher, but HEMTs are usually preferred.	Amplifiers, oscillators, mixers, modulators, frequency multipliers, control components, etc. Much better noise figure than HBTs but higher 1/f noise.
HEMT	Highest frequency device available. Over 200GHz	Much the same as MESFETs. Best suited for small-signal, low-noise uses, but power devices are possible. Much better noise figure than HBTs but higher 1/f noise.
MOSFET	Up to 6 GHz for advanced technologies. 2-3 GHZ more common.	Analog, digital, and RF Si IC applications. MESFETs and HEMTs have much lower noise figures at microwave frequencies.

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APPENDIX II-1

DIODES - SUMMARY

<http://www.radio-electronics.com/info/data/semicond/diodes/types-of-diodes.php>

There are many different types of diodes that are available for use in electronics design. Different semiconductor diode types can be used to perform different functions as a result of the properties of these different diode types.

Semiconductor diodes can be used for many applications. The basic application is obviously to rectify waveforms. This can be used within power supplies or within radio detectors. Signal diodes can also be used for many other functions within circuits where the "one way" effect of a diode may be required.

Diodes are not just used as rectifiers, as various other types of diode can be used in many other applications. Some other different types of diodes include: light emitting diodes, photo-diodes, laser diodes and more as detailed below.

Many of the different types of diodes mentioned below have further pages providing in-depth information about them including their structures, method of operation, how they may be used in circuits, and precautions and tips for using them in electronics design.

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It is sometimes useful to summarize the different types of diode that are available. Some of the categories may overlap, but the various definitions may help to narrow the field down and provide an overview of the different diode types that are available.

- **Backward diode:** This type of diode is sometimes also called the back diode. Although not widely used, it is a form of PN junction diode that is very similar to the tunnel diode in its operation. It finds a few specialist applications where its particular properties can be used.
Read more about the [Backward diode](#)
- **BARITT diode:** This form of diode gains its name from the words Barrier Injection Transit Time diode. It is used in microwave applications and bears many similarities to the more widely used IMPATT diode. *Read more about the [Baritt diode](#)*
- **Gunn Diode:** Although not a diode in the form of a PN junction, this type of diode is a semiconductor device that has two terminals. It is generally used for generating microwave signals. *Read more about the [Gunn diode](#)*
- **Laser diode:** This type of diode is not the same as the ordinary light emitting diode because it produces coherent light. Laser diodes are widely used in many applications from DVD and CD drives to laser light pointers for presentations. Although laser diodes are much cheaper than other forms of laser generator, they are considerably more expensive than LEDs. They also have a limited life. *Read more about the [laser diode](#)*
- **Light emitting diodes:** The light emitting diode or LED is one of the most popular types of diode. When forward biased with current flowing through the junction, light is produced. The diodes use component semiconductors, and can produce a variety of colours, although the original colour was red. There are also very many new LED developments that are changing the way displays can be used and manufactured. High output LEDs and OLEDs are two examples. *Read more about the [light emitting diode](#)*
- **Photodiode:** The photo-diode is used for detecting light. It is found that when light strikes a PN junction it can create electrons and holes. Typically photo-diodes are operated under

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reverse bias conditions where even small amounts of current flow resulting from the light can be easily detected. Photo-diodes can also be used to generate electricity. For some applications, PIN diodes work very well as photodetectors. [**Read more about the photo-diode**](#)

- **PIN diode:** This type of diode is typified by its construction. It has the standard P type and N-type areas, but between them there is an area of Intrinsic semiconductor which has no doping. The area of the intrinsic semiconductor has the effect of increasing the area of the depletion region which can be useful for switching applications as well as for use in photodiodes, etc. [**Read more about the PIN diode**](#)
- **PN Junction:** The standard PN junction may be thought of as the normal or standard type of diode in use today. These diodes can come as small signal types for use in radio frequency, or other low current applications which may be termed as signal diodes. Other types may be intended for high current and high voltage applications and are normally termed rectifier diodes. [**Read more about the diode**](#)
- **Schottky diodes:** This type of diode has a lower forward voltage drop than ordinary silicon PN junction diodes. At low currents the drop may be somewhere between 0.15 and 0.4 volts as opposed to 0.6 volts for a silicon diode. To achieve this performance they are constructed in a different way to normal diodes having a metal to semiconductor contact. They are widely used as clamping diodes, in RF applications, and also for rectifier applications. [**Read more about the Schottky diode**](#)
- **Step recovery diode:** A form of microwave diode used for generating and shaping pulses at very high frequencies. These diodes rely on a very fast turn off characteristic of the diode for their operation. [**Read more about the Step recovery diode**](#)
- **Tunnel diode:** Although not widely used today, the tunnel diode was used for microwave applications where its performance exceeded that of other devices of the day. [**Read more about the Tunnel diode**](#)
- **Varactor diode or varicap diode:** This type of diode is used in many radio frequency (RF) applications. The diode has a reverse bias placed upon it and this varies the width of the

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depletion layer according to the voltage placed across the diode. In this configuration the varactor or varicap diode acts like a capacitor with the depletion region being the insulating dielectric and the capacitor plates formed by the extent of the conduction regions. The capacitance can be varied by changing the bias on the diode as this will vary the width of the depletion region which will accordingly change the capacitance. [**Read more about the varactor diode**](#)

- **Zener diode:** The Zener diode is a very useful type of diode as it provides a stable reference voltage. As a result it is used in vast quantities. It is run under reverse bias conditions and it is found that when a certain voltage is reached it breaks down. If the current is limited through a resistor, it enables a stable voltage to be produced. This type of diode is therefore widely used to provide a reference voltage in power supplies. Two types of reverse breakdown are apparent in these diodes: Zener breakdown and Impact Ionisation. However the name Zener diode is used for the reference diodes regardless of the form of breakdown that is employed.

[**Read more about the Zener / voltage reference diode**](#)

Semiconductor diodes are widely used throughout all areas of the electronics industry from electronics design through to production and repair. The semiconductor diode is very versatile, and there are very many variants and different types of diode that enable all the variety of different applications to be met.

The different diode types of types of diodes include those for small signal applications, high current and voltage as well as different types of diodes for light emission and detection as well as types for low forward voltage drops, and types to give variable capacitance. In addition to this there are a number of diode types that are used for microwave applications.

Understanding Diode Specifications & Parameters

Diode datasheets provide a large amount of data - diode specifications and parameters about the diodes. The exact explanations of what these diode specifications and parameters are may not always be available. The list below provides a summary of some of the more widely used diode specifications, parameters and limits detailing their meanings.

- **Semiconductor material:** The semiconductor material used in the PN junction diode is of paramount importance because the material used affects many of the major diode characteristics and properties. Silicon is the most widely used material as it offers high levels of performance for most applications and it offers low manufacturing costs. The other material that is used is germanium. Other materials are generally reserved for more specialist diodes. The semiconductor material choice is of particular importance as it governs the turn on voltage for the diode - around 0.6volts for silicon and 0.3 volts for germanium, etc..
- **Forward voltage drop (V_f):** Any electronics device passing current will develop a resulting voltage across it and this diode characteristic is of great importance, especially for power rectification where power losses will be higher for a high forward voltage drop. Also RF diodes often need a small forward voltage drop as signals may be small but still need to overcome it. The voltage across a PN junction diode arise for two reasons. The first of the nature of the semiconductor PN junction and results from the turn-on voltage mentioned above. This voltage enables the depletion layer to be overcome and for current to flow. The second arises from the normal resistive losses in the device. As a result a figure for the forward voltage drop at a specified current level will be given. This figure is particularly important for rectifier diodes where significant levels of current may be passed.
- **Peak Inverse Voltage (PIV):** This diode characteristic is the maximum voltage a diode can withstand in the reverse direction. This voltage must not be exceeded otherwise the device may fail. This voltage is not simply the RMS voltage of the incoming waveform. Each circuit

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needs to be considered on its own merits, but for a simple single diode half wave rectifier with some form of smoothing capacitor afterwards, it should be remembered that the capacitor will hold a voltage equal to the peak of the incoming voltage waveform. The diode will then also see the peak of the incoming waveform in the reverse direction and therefore under these circumstances it will see a peak inverse voltage equal to the peak to peak value of the waveform.

- **Maximum forward current:** When designing a circuit that passes any levels of current it is necessary to ensure that the maximum current levels for the diode are not exceeded. As the current levels rise, so additional heat is dissipated and this needs to be removed.
- **Leakage current:** If a perfect diode were available, then no current would flow when it was reverse biased. It is found that for a real PN junction diode, a very small amount of current flow in the reverse direction as a result of the minority carriers in the semiconductor. The level of leakage current is dependent upon three main factors. The reverse voltage is obviously significant. It is also temperature dependent, rising appreciably with temperature. It is also found that it is very dependent upon the type of semiconductor material used - silicon is very much better than germanium. The leakage current characteristic or specification for a PN junction diode is specified at a certain reverse voltage and particular temperature. The specification is normally defined in terms of in microamps, μA or picoamps, pA .
- **Junction capacitance:** All PN junction diodes exhibit a junction capacitance. The depletion region is the dielectric spacing between the two plates which are effectively formed at the edge of the depletion region and the area with majority carriers. The actual value of capacitance being dependent upon the reverse voltage which causes the depletion region to change (increasing reverse voltage increases the size of the depletion region and hence decreases the capacitance). This fact is used in varactor or varicap diodes to good effect, but for many other applications, especially RF applications this needs to be minimised. As the capacitance is of importance it is specified. The parameter is normally detailed as a given

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capacitance (in pF) at a given voltage or voltages. Also special low capacitance diodes are available for many RF applications.

- **Package type:** Diodes can be mounted in a variety of packages according to their applications, and in some circumstances, especially RF applications, the package is a key element in defining the overall RF diode characteristics. Also for power applications where heat dissipation is important, the package can define many of the overall diode parameters because high power diodes may require packages that can be bolted to heatsinks, whereas small signal diodes may be available in leaded formats or as surface mount devices.

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APPENDIX II-2

TRANSISTOR TRADEOFFS

From <http://www.microwaves101.com/encyclopedia/MMICsemi.cfm>

GaAs MESFET

Gallium arsenide MESFET was the original answer to "how can we make amplifiers at microwave frequencies?" The first GaAs MMICs demonstrated in the 1970s. Including HEMT and HBT technologies, literally billions of dollars have been spent extending f_{max} of GaAs products up into 100s of GHz.

The semi-insulating properties of GaAs substrates and the 12.9 dielectric constant make it an excellent media for microstrip or CPW design. It operates reliably up to 150C channel temperature. GaAs substrates are available up to six inches (150 mm) in diameter, which has been a long development since the first 2-inch wafers were available in the late 1970s. Sadly, GaAs MESFET MMICs will never be cheaper than silicon, due to the starting material cost (\$100s of dollars). GaAs parts are more fragile than silicon, and the thermal dissipation factor is not that good. GaAs MESFETs may be extinct in five years, because it doesn't cost much more to fabricate PHEMT or MHEMT on GaAs, and these technologies offer higher performance.

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Advantages:	Disadvantages
<ul style="list-style-type: none"> • Mature technology • Optical gates (usually) means low cost • Great microwave substrate (ϵ_r of 12.9, low loss tangent, high bulk resistivity) • Six inch wafers available • Photonic properties • 16-20 volt breakdown possible • Relatively cheap to produce (but always more than silicon) • Channel temperatures up to 150C possible 	<ul style="list-style-type: none"> • Limited to Ku-band or lower • Noise figure and power performance not as good as GaAs PHEMT • Positive and negative voltage typically needed (V_{GS} and V_{DS}).

GaAs PHEMT

GaAs PHEMT was the second MMIC technology to be perfected, in the 1990s. Breakdown voltages of PHEMT up to 16 volts make high-power/high efficiency amplifiers possible, and noise figure of tenths of a dB at X-band means great LNAs. PHEMT stands for pseudomorphic high electron mobility transistor. "Pseudomorphic" implies that the semiconductor is not just GaAs (e.g., AlGaAs/InGaAs/GaAs).

Actually, "pseudomorphic" means that the hetero layers are thin enough not to keep their own crystal lattice structure, but assume the structure (lattice constants especially) of surrounding material (lots of stress is involved). If you look at a two dimensional cross section of the layer, you'll see that while it assumes the lattice constant of the bulk structure in the X direction, it tries to keep its original lattice constant in the vertical direction.

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This layer is indeed strained. For a GaAs pHEMT, indium is added to improve mobility and form a quantum well. Indium wants to grow the lattice and the typical range for useful thicknesses would be 10-25% on GaAs. You can also do strain compensation with the Schottky or cap layer.

Advantages:	Disadvantages
<ul style="list-style-type: none">• Useful through Q-band, especially if thinned to 2 mils and individual source vias are used• Excellent power and efficiency (greater than 60% PAE)• Breakdown 12 volts at best, typical operate at 5-6 volts• Channel temperatures up to 150C possible.	<ul style="list-style-type: none">• E-beam gates (increases cost)• Positive and negative voltage typically needed (V_{GS} and V_{DS})

GaAs MHEMT

Recent work on metamorphic MHEMT has made premium InP HEMT performance possible (amplifiers up to 100 GHz) at the same price as "regular" GaAs PHEMT. You can get noise figure and f_{max} equal to indium phosphide by using MHEMT, if you use a reputable foundry and indium content is high.

You can actually exceed InP RF performance with indium content greater than 55% ! The down side to all that indium is reduced operating voltage.

MHEMT stands for metamorphic high-electron mobility transistor. The channel material is InGaAs. "Metamorphic" implies that the lattice structure of GaAs is buffered using epitaxial layers to gradually transform the lattice constant so it lines up with InGaAs. InGaAs is normally grown

on InP, which is expensive and fragile compared to GaAs. "Metamorphic" is changing the lattice constant by bond breaking as opposed to "pseudomorphic".

Advantages:	Disadvantages
<ul style="list-style-type: none">• Extremely low noise figure• Incredibly high f_{max} (more than 100 GHz)• Extremely low on-resistance, makes great switches, but not as good as PIN diodes.• Channel temperatures up to 150C possible.	<ul style="list-style-type: none">• Breakdown voltage much lower than PHEMT• Low operating voltage (1 to 2 volts)• Positive and negative voltage typically needed (V_{GS} and V_{DS})

GaAs HBT

The heterojunction bipolar transistor (HBT) is a new development, and can decrease the cost of GaAs amplifier products because the emitters are formed optically. GaAs HBT devices operate vertically, compared to the horizontal operation of FETs. However, for very high frequency, the emitter size must be made quite small, and the InGaAs layer is thick and is a thermal insulator, so these devices tend to run HOT. Typical HBT amplifiers are "gain blocks", used in the UHF to C-band frequency ranges.

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Advantages:	Disadvantages
<ul style="list-style-type: none"> • Single power supply polarity • All-optical process 	<ul style="list-style-type: none"> • Heat dissipation can be problem at small emitter size • Typically, reverse isolation is not as high as with PHEMT amplifiers, leading to poor amplifier directivity. • Collector resistors are required to stabilize amplifiers. These cut into your power efficiency.

Indium phosphide (InP) HEMT

Indium phosphide HEMT has broken all of the upper frequency records, on the way to terahertz devices. However, there are serious drawbacks to this technology, not the least of which is its high cost. For this reason, InP is more regarded as a lab curiosity rather than a production process. The actual semiconductor that is doing the work in so-called InP is actually InGaAs. Indium phosphide is merely the substrate that it is grown onto. The reason for this is that InGaAs shares the same lattice constant with InP, 5.87 angstroms. InP substrates are small (3" typical, 4" are also available). Permittivity of 12.4, close to that of GaAs. A huge drawback of indium phosphide technology is that InP wafers are extremely brittle compared to other semiconductors. Try shipping an InP wafer sometime. Silicon is the least brittle, and GaAs is somewhere in the middle.

Advantages:	Disadvantages
<ul style="list-style-type: none"> • Extremely low noise figure • Useful through W-band and beyond 	<ul style="list-style-type: none"> • More expensive than GaAs due to starting material costs, small size of wafers. • Extremely fragile. • Low breakdown voltage (power is low)

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Indium phosphide (InP) HBT

Some people think that InP will have a second chance to become the most ubiquitous power amplifier technology for cell phones when new higher power density/lower voltage lithium ion batteries become available, as suggested in the December 2006 paper by Michael Gaynor (at the end of this chapter). InP has superior low voltage performance compared to GaAs HBT.

Silicon CMOS

Silicon is very economical. It comes in 12 inch (300 mm) and bigger wafers. Processing is also low-cost. But it is not a good media for microstrip (lossy). Silicon by itself doesn't make very good amplifiers above maybe X-band. Noise figure, power, are all second class to any of the compound semiconductors. It can only operate reliably up to 110C, but silicon is an pretty good heat dissipater.

Silicon carbide LDMOS

Laterally-diffused metal oxide semiconductor technology, used to make power amplifiers. Can withstand 200C channel temperatures.

Silicon germanium HBT

SiGe is a new development (in the last years), and was originally predicted to put all forms of GaAs into the history books. SiGe can make very cheap parts, with performance maybe into millimeterwave, and processing on eight-inch (200 mm) diameters wafers. But the devices are not as high-performance as GaAs, in terms of noise figure and power. The setup charge at IBM to make a mask set is enormous, because 200 mm contact masks are needed (GaAs usually uses a 10X wafer stepper, these glass reticles are relatively cheap).

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The poor insulating properties of a silicon substrate means it's not a good media for microstrip, so you have two choices. You can make transmission lines in the backend of line (BEOL) SiO₂ and metal layers. The SiO₂ dielectric layers are thin, which means high metal losses. Or you can send your wafers to a third party for post-processing to put a lower dielectric metal system on top of it, such as benzo-cyclo-butene (BCB) and gold. Every time the upper frequency of SiGe extended, the breakdown voltage is reduced. Some of that stuff has to operate at 1.0 volts.

Advantages:	Disadvantages
<ul style="list-style-type: none"> • Eight inch silicon wafers mean low production cost in high volume • All-optical process (also low cost) • Possible to add scads of logic onto RF chip (BiCMOS logic) 	<ul style="list-style-type: none"> • Low V_{br}, as bad as 1.5 volts for IBM "9HP" • Electrically, Si is not a great insulator • Thermal runaway? • 110C max junction temperature • Not radiation hard • No equivalent of a switch FET, so phase shifters and attenuators are a problem • Not many foundries do SiGe • High setup charges due to expensive mask set

IBM's SiGe HBT BiCMOS Technology Generations:

- 1st Generation (IBM 5HP – 50 GHz HBT + 0.35μm CMOS)
- 2nd Generation (IBM 6HP – 50 GHz HBT + 0.25μm CMOS)
- 3rd Generation (IBM 7HP – 120 GHz HBT + 0.18μm CMOS)
- 4th Generation (IBM 8T – 200 GHz HBT)
- 5th Generation (IBM 9T – 350 GHz HBT)

Gallium nitride (GaN)

This is the future of microwave power amplifiers. GaAs has probably exceeded its half-life. More expensive in terms of dollars per die, GaN offers a path to much higher power densities and therefore cheaper dollars per Watt. Breakdown voltages of 100 Volts are possible! GaN is still a relatively immature process, reliability has been a huge problem that is just being overcome. Ancillary stuff like higher-voltage capacitors and resistors, and backside processes need to be redeveloped at MMIC foundries in order to participate in this new technology.

DARPA (Defense Advanced Research Projects Agency) is pumping millions of dollars into GaN so that the US will maintain technological superiority in military programs for the next decade or two. The big DARPA program is called WBGS-II (for Wide BandGap Semiconductor), and the three teams are TriQuint/Lockheed, Raytheon/Cree and Northrop Grumman.

Substrates for GaN are either silicon carbide, sapphire, or silicon (Nitronix uses this approach). "Native" GaN wafers are impractical, so a lot of expensive alchemy is needed to align the GaN crystal onto mismatched substrates. Four-inch SiC substrates are just becoming available, for GaN-on-silicon, four inch wafers are also available. SiC is an excellent heat sink, and GaN can operate up to greater than 150C channel temperature. Below 2 GHz, expect to see GaN used in base station applications, competing with silicon carbide technology. Higher frequency GaN products will be fielded by the military, HRL reports power amplifiers even up at millimeterwave!

Silicon is not such a great heat sink as silicon carbide (40 versus 350 W/m-K), so lower-cost of GaN on-silicon-may be outweighed by the ability to dissipate higher power (and thereby achieve greater power density) on SiC Normally, silicon's conductivity makes it lossy as an RF substrate, Nitronix could fix that using high-resistivity silicon.

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Advantages:	Disadvantages
<ul style="list-style-type: none">• Up to 10X the power density of GaAs PHEMT has been demonstrated.• Higher operating voltage, less current.• Excellent efficiency possible.• SiC substrates are great heat spreaders.• Can operate hotter than GaAs, Si or SiGe.	<ul style="list-style-type: none">• Expensive as heck!• Reliability not established yet• You have to deal with a huge heat flux.

Antimonide-based compound semiconductors

At the other end of the power spectrum is ABCs. Here's a technology that can operate at only one tenth of a volt! It is possible to create low noise amplifiers that dissipate only one milliwatt using ABCs. The market? Space-based arrays, where power is limited to solar cells, and the received power from earth is pretty-well attenuated to next to nothing. Don't look for ABCs applications where high linearity is a priority.

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APPENDIX II-3

FET BASICS

From <http://www.microwaves101.com/encyclopedia/FETs.cfm>

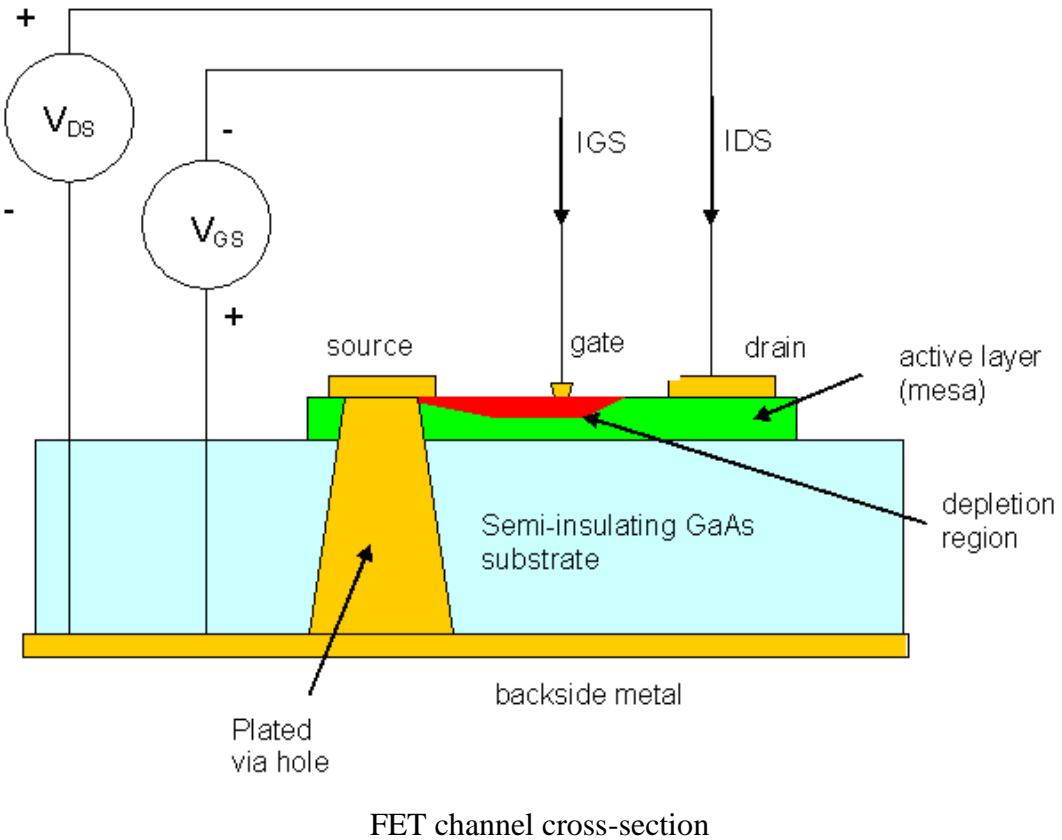
What's a FET?

In microwaves we are almost always referring to a MESFET, which stands for metal-semiconductor field effect transistor. A FET is a three terminal device capable of both microwave amplification and switching. The FET's three terminals are denoted as gate, source and drain. With respect to a bipolar transistor (BJT), the gate of a FET corresponds to the base of a BJT, the drain corresponds to the collector and the source corresponds to the emitter terminal.

Used as an amplifier, the gate is most often configured as the input terminal, the source is grounded and the drain is the output. The output current (I_{DS}) is controlled by the input voltage (V_{GS}). This configuration is called common source since the source is common to the input and output ground connections. It is also possible (but unusual) to ground the gate and create a common-gate amplifier. Such an amplifier does not provide the voltage gain of the common-source amplifier, but it has the interesting property of being easier to impedance match than a "normal" common-source amplifier.

The figure below shows a cross-section of the channel of a field-effect transistor and explains some FET terminology.

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The drain and source are connected by the FET channel, which is formed by creating a mesa of N-type semiconductor (for an N-channel FET) on top of a semi-insulating substrate (typically GaAs). In microwaves we are almost often dealing with N-channel FETs. P-channel FETs are possible but are never used at microwave frequencies, because they would have far worse performance compared to N-channel FETs (due to the electron mobility of the device).

The drain and source contacts are connected to the channel with ohmic metal contacts that form low-resistance connections to these terminals. The gate connection to the channel is formed between the drain and source by a Schottky metal contact to the channel.

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The rectifying property of the gate contact means that when it is reverse biased with respect to the channel it conducts almost zero DC current (I_{GS}) to the channel, but its electric field can be used to effectively displace the electrons within the channel. Thus an AC voltage incident on the gate terminal causes a variable resistance between the source and drain of the FET. When the gate reaches pinch-off voltage the electrons below the gate are depleted to the point where essentially no current can flow from drain to source.

The source connection is the "source" of electrons in the channel, and the drain is where they are "drained off". Remember that we are talking about electrons flowing here, and you will see that the direction of current flow is positive from drain to source.

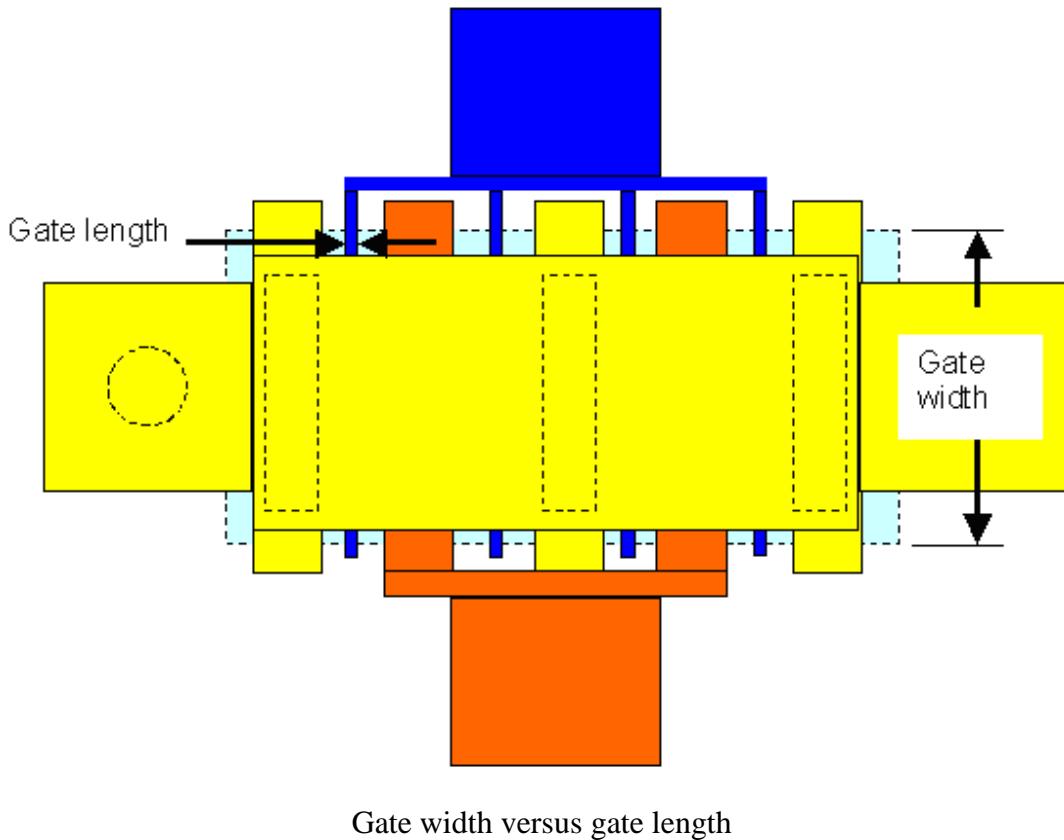
FET geometry

FET geometry refers to the physical dimensions of a FET. FET dimensions are always described in microns or millimeters, never in mils, with the exception that overall chip dimensions (length, width and thickness) are often given in mils as well as microns. This is because the next higher assembly (artwork for a thin-film network for example) is often dimensioned in inches.

Gate length is often confused with *gate width*. Just remember when you look at a gate finger, gate length is the short dimension and gate width is the long dimension. This is illustrated in the figure below. Gate length has a major effect on maximum frequency of operation: one-micron gates are fine up to C-band, half-micron gates are good through X-band, quarter-micron gates are good into Ka-band, and 0.15 micron gates can work up through W-band. What is the limit on gate length? Some companies are experimenting with 50 to 100 nanometer gates!

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Gate width refers to the unit width of the gate as it passes between the source and drain across the mesa (the semiconducting area of a FET). Wider gates mean more DC and RF current, and therefore more power capability. Gate width must be sized appropriate to frequency: if the gate width starts to become an appreciable fraction of a wavelength, the RF performance of the FET starts to suffer. At X-band, power FETs often have 150 um wide gates. At Ka band the gate width is typically 75 micron maximum. At W-band perhaps 40 micron fingers is the upper limit.



A *gate finger* refers to a single gate structure. *Gate periphery* is the total size of a FET. Most FETs have multiple gate fingers, so the periphery is equal to the number of gate fingers times the unit gate width. In the above figure there are four gate fingers. Many of the FET parameters can be

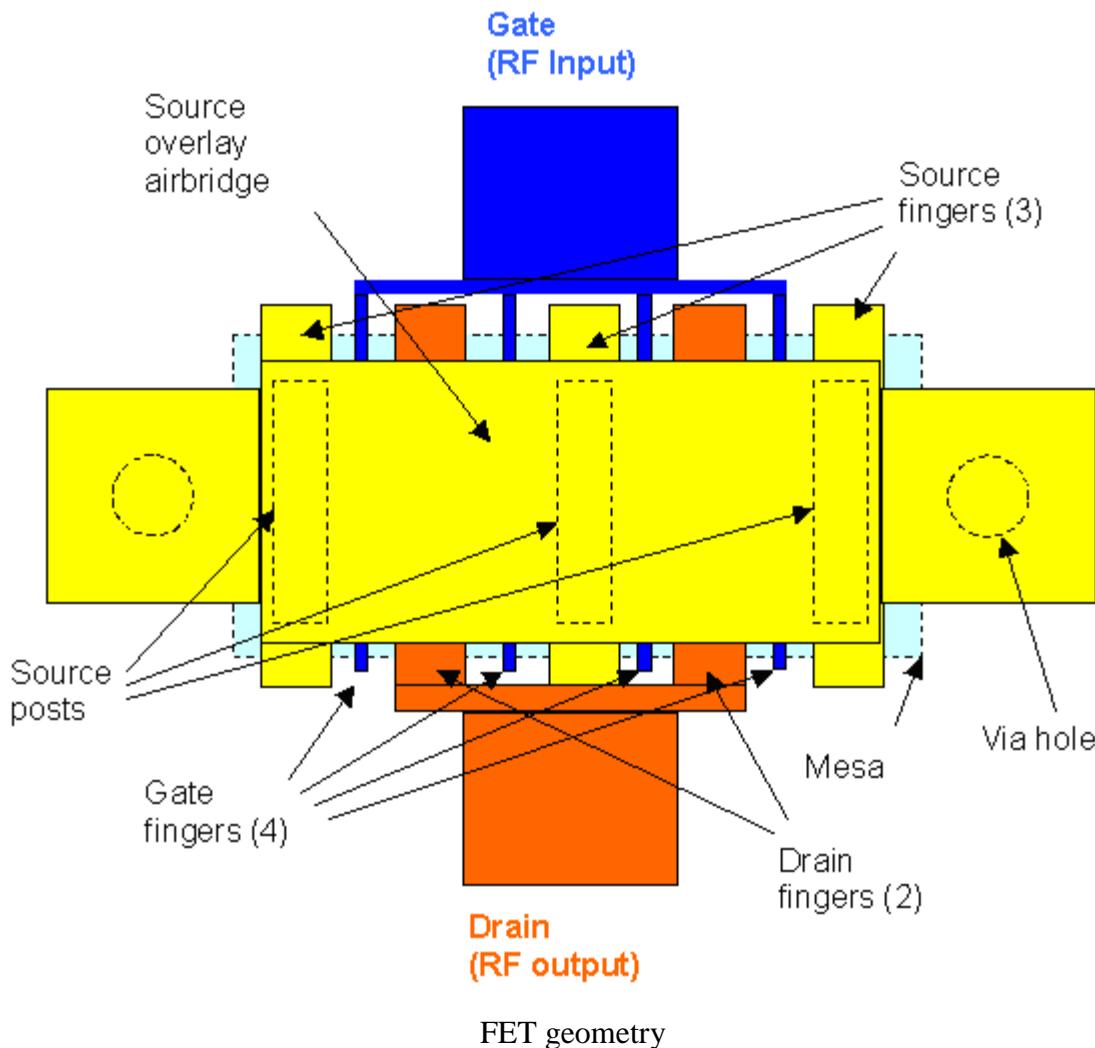
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directly scaled with gate periphery, for example the saturated drain current is proportional to gate periphery.

The *gate bus-bar* is the electrical contact that is used to connect all of the multiple gate fingers together. The *drain bus bar* serves a similar purpose.

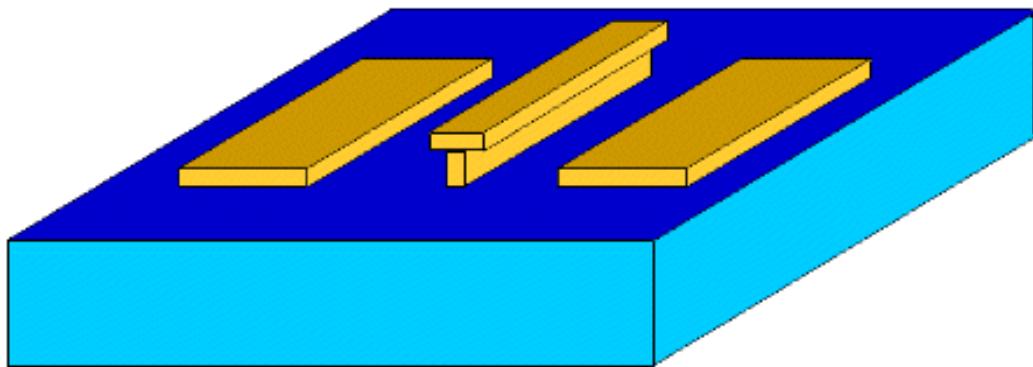
Via holes are what connect the source (or individual sources) to the chip backside metal, which is considered RF and DC ground. When individual sources are grounded with separate via holes, these vias are referred to as ISVs which stands for Individual Source Vias. ISVs are only used on very thin FETs, perhaps with two mils (50 microns) maximum thickness. ISVs provide very low-inductance grounding to the source connection, providing the most gain and efficiency for power amplifiers, which becomes more important for power FETs operating at millimeter-wave frequencies. On four-mil GaAs and thicker, ISVs are not usually possible, because the source contact pad is typically smaller than the minimum diameter of an etched via hole.

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Mushroom gate or tee gate refers to a technique of providing very short effective gate length, while providing low gate resistance. Gate resistance is a parasitic element that affects the maximum available gain of a FET, and is inversely proportional to the cross-sectional area of metal along the gate finger. A picture of a tee-gate is shown below. This type of structure involves extra process steps and is therefore used only in higher-frequency applications where short gates are required, such as X-band through millimeter-waves.

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A tee gate

Why use GaAs?

The FET is built on top of a semi-insulating substrate, most often GaAs. When we say "semi-insulating" this is perhaps misleading. In its pure form, GaAs is remarkable insulator, which is what makes monolithic microwave integrated circuits (MMICs) practical. Here is one advantage GaAs has over silicon. Pure silicon is a better conductor than pure GaAs, so it tends to dissipate electrical fields that are needed to support transmission modes and hence needs some "help" to be used as a MMIC.

What's a compound semiconductor?

GaAs is referred to as a "compound semiconductor", because it is a crystal of more than one element.

Silicon is a semiconductor all by itself. GaAs wafers are available in up to six inch diameter, but more often FET and MMIC manufacturers use four-inch material.

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What does III-V semiconductor refer to?

Three-five material refers to compound semiconductors made from one element from Group III on the periodic chart (arsenic in the case of GaAs) and one from Group V (gallium in the case of GaAs). Other three-five (or III-V in Roman numerals) semiconductors include indium phosphide and gallium nitride. TriQuint Semiconductor derived their name from the III-V material that their business is based on (GaAs)

What does “bandgap” refer to?

Bandgap is a material property that takes some knowledge of semiconductor physics to understand. The higher the bandgap, the higher the breakdown voltage the material can support. High breakdown is a huge advantage for power amplifiers, remember Ohm's law and you will see that voltage swing is proportional to power. GaAs is a medium bandgap technology at 1.5 electron-volts, you could get 20 volts breakdown with a GaAs MESFET. InP is a low-bandgap device at 0.75 electron-volts, it only supports a few volts breakdown. The “great white hope” of microwave semiconductors is gallium nitride, which is a wide bandgap semiconductor at greater than 3 electron-volts bandgap energy. GaN FETs have exhibited over 100 volts breakdown voltage. DARPA is a big fan of GaN technology and is spending tens of millions of taxpayer dollars trying to develop this technology beyond a laboratory curiosity that blows up in a few hours of operation into the "next big thing" for solid-state microwave power.

What is the difference between Schottky and Ohmic contacts?

Ohmic metal on a FET is often called "source-drain metal". This is because it forms the contacts for these two terminals of the FET. The drain and source contacts are considered “ohmic” because they behave resistively, that is, they pass current in either direction, obeying Ohm's law where

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current is proportional to voltage. Ohmic metal is usually the first layer of metal applied when a FET or a MMIC is fabricated. It is alloyed at high temperature. The Schottky contact is a diode junction formed between certain metals and semiconductors. Metals that form Schottky contacts to N-type GaAs include aluminum, gold, silver, titanium and platinum. Often a layered structure of metals is used in FETs, such as Ti/Pt/Au. Gold reacts with GaAs so it is a bad Schottky metal. Platinum keeps the gold away from the GaAs (it acts as a barrier metal in this case). Titanium is what makes the gate "stick" to the GaAs.

What does semiconductor refer to?

Based on differences in bulk resistivity, five classes of materials are in common usage, namely conductors, semiconductors, semi-insulators, insulators and superconductors. GaAs bulk resistivity can be tailored over a huge range, 10^6 to 10^{22} , so that GaAs can be anywhere from a conductor to an insulator. By doping Chrome is usually added to the melt to raise resistivity, but this trick has its limitations (it does not stay stable through wafer processing steps). High purity, undoped GaAs can be 10^7 to 10^8 ohm-cm.

Intrinsic versus extrinsic GaAs: intrinsic refers to the pure crystal, extrinsic refers to the doped material where conduction is due to donor or acceptors.

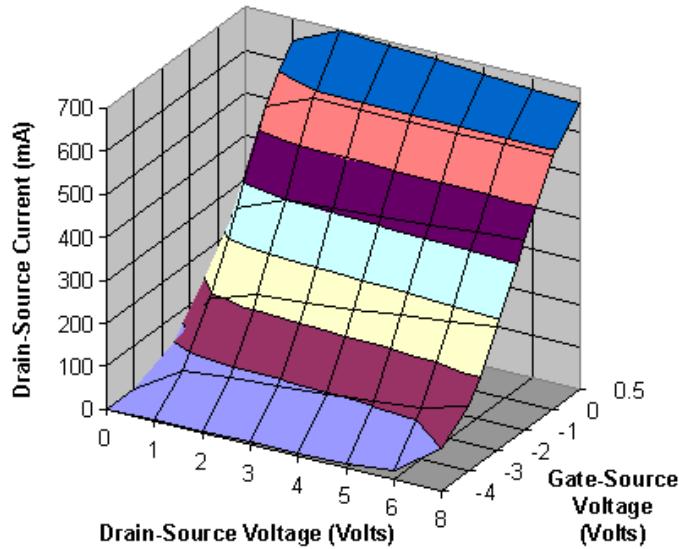
Thermal conductivity of FETs

The thermal conductivity (TC) of GaAs varies at $1/T$ (T in Kelvin). It is approximately 0.55 W/cm-C at room temperature.

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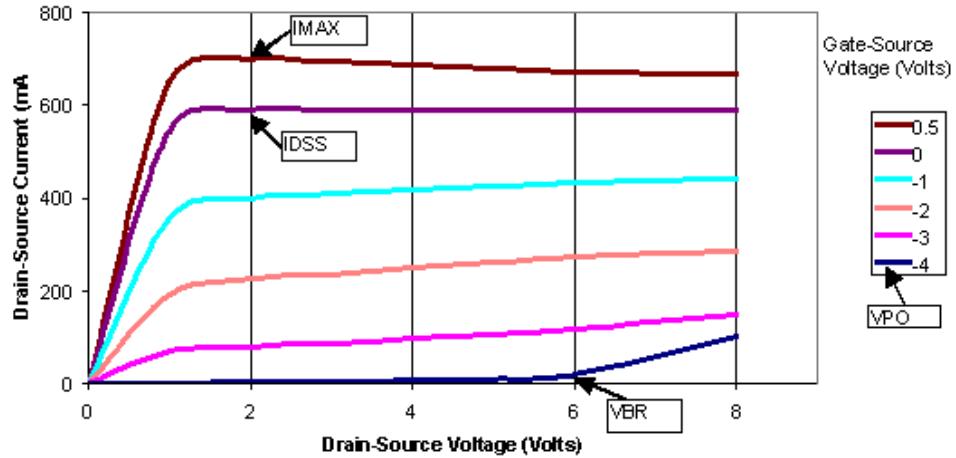
FET I-V and Transfer Curves

The operation of any three-terminal device is well described on a three dimensional surface plot as shown below. For an FET, the output characteristics V_{DS} and I_{DS} are shown to be a function of the input voltage V_{GS} . A typical FET response is shown below.



Three-dimensional FET I-V characteristics

The three-dimensional characteristics are most often collapsed onto 2-D plots of IV curves:



FET I-V characteristics and definitions

Here the output drain current/voltage relationship is plotted at discrete gate voltages. Depicted on this plot are some definitions:

I_{MAX} : the drain-source current when the gate is forward biased for maximum channel current. This is typically measured at up to 1.0 volts on the gate (higher potentials will conduct tons of current across the gate Schottky contact which tends to destroy the FET) and perhaps 1.5 or 2 Volts drain-to-source. To get to I_{MAX} the gate must be raised to its Schottky barrier height (voltage), which is approximately 0.7 volts. This is the intrinsic gate bias. The other 0.3 volts will drop across the intrinsic source resistance R_s . Still, you might want to limit the measurement current with a current-limiting resistor.

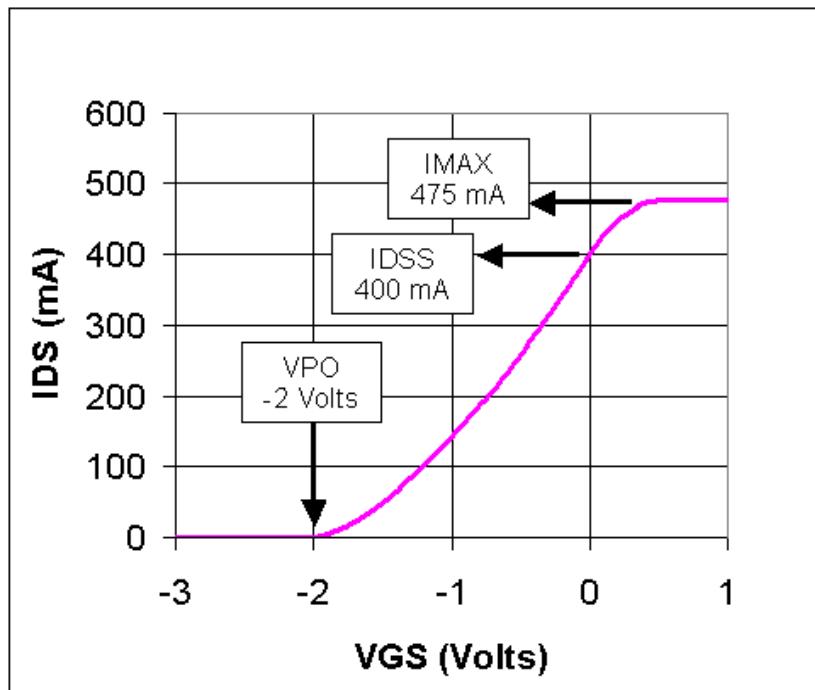
I_{DSS} : the saturated drain-source current when the gate is biased at zero volts (grounded to the source). This is typically measured at 1.5 or 2 Volts drain-to-source.

V_{PO} : pinch-off voltage. This is where the drain-source terminals start to look like an open circuit, and no appreciable current flows even at high drain-source potentials. In practice there is always some residual current and the actual V_{PO} measurement must make an allowance for this. For example, the pinch-off voltage could be measured at 2.5% of I_{DSS} and $V_{DS} = 2$ volts.

V_{BR} : the gate-drain breakdown voltage, which is indirectly measured on the IV curves. At high drain-source potential and near pinch-off, the IV curves tend to bend up. As shown in the picture the breakdown voltage V_{DS} is approximately 10 volts ($V_{GS} = -4$ volts and $V_{DS} = 6$ volts combined). Stay away from this bias region if you want your FET to be safe!

Knee voltage: the voltage at which the curves transition from "linear" to "saturation". In the linear region, I_{DS} depends on both V_{GS} and V_{DS} (from $V_{DS} = 0$ Volts to approximately $V_{DS} = 2$ Volts). In the saturation region, I_{DS} depends mainly on V_{GS} and not V_{DS} . This is the right side of the curve, beyond $V_{DS} = 2$ volts..

Another very useful plot of the FET's characteristics is called the FET transfer characteristic. Here we see the variation in drain current due to variation in gate voltage, at some fixed drain voltage in the saturation region (beyond $V_{DS} = 2$ Volts). This is analogous to looking at a cut in the Y-Z plane in the surface plot above. Plotted below is the transfer characteristic of a FET. This type of plot is extremely useful in designing self-biasing networks which are described below. Here we see why a FET is an effective amplifier: for a quiescent point of -1 Volts, a peak-to-peak voltage swing of +/-0.5 Volts on the gate terminal provides a variation in drain current from 50 to 250 mA.



FET transfer characteristics

Types of microwave FETs

With respect to their intended operation, FETs can be divided into three categories: low noise, power and switch FETs. Low noise FETs are optimized to provide the lowest possible noise figure at very low voltage and power (perhaps 1.5 volts and 10 mA). Power FETs possess higher breakdown voltage than low noise FETs and can therefore operate at higher voltages, and are much larger in periphery than low noise FETs.

Switch FETs are intended to operate passively (no drain current and no gain); the gate voltage is merely used to switch the device from a resistive element to a small capacitive element. Switch FETs can be configured in series with a transmission line (drain and source act as input or output),

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or in shunt, with the source grounded. One beautiful thing about switch FETs is that you don't really care how high the gate feed resistance is, because the RF signal doesn't traverse the gate terminal. This opens up many possibilities when you design the gate structure. One type of switch FET is called a "meandered gate" FET. This means that multiple FET gates are hooked up in series, rather than through a single bus-bar.

Depletion and enhancement modes

A “depletion mode” FET is one where the gate is mainly used to reduce the current within the channel (most common microwave FETs are depletion mode). An “enhancement mode” FET does not conduct drain-to-source until the gate is slightly forward biased. Think of this as a depletion-mode FET with a zero-volt pinch-off voltage. There is a big limitation to enhancement-mode FETs: you can't exceed the turn-on voltage of the Schottky contact, which is typically 0.7 volts, so the gate etching process has to be well-controlled to produce a FET with pinch-off of zero volts or perhaps a few tenths of a positive volt. Etch too far and you will end up with no FET at all, just a capacitor between drain and source!

FET bias networks

Bias networks are what are used to put a FET at the intended quiescent operating point or Q point. For example, you might want to operate a FET in a power amplifier at 6 volts V_{DS} and at 50% of the saturated drain current ($I_{DSS}/2$). This is the quiescent point.

FET DC characteristics, such as I_{DSS} and V_{PO} vary from lot to lot, and even within a wafer. This complicates the life of the amplifier designer, since V_{GS} needs to be set to achieve either a fixed fraction of the saturated drain current, or a fixed current. One amplifier might need V_{GS} to be - 1.05 volts, another might need $V_{GS} = - 2.1$ volts to perform as designed.

What's a designer to do?

There are at least three ways to bias up a FET amplifier to get to the intended quiescent operating point. The most obvious is to have separate DC power supplies for the gate and drain connections, with the gate supply being adjustable, and ground the source.

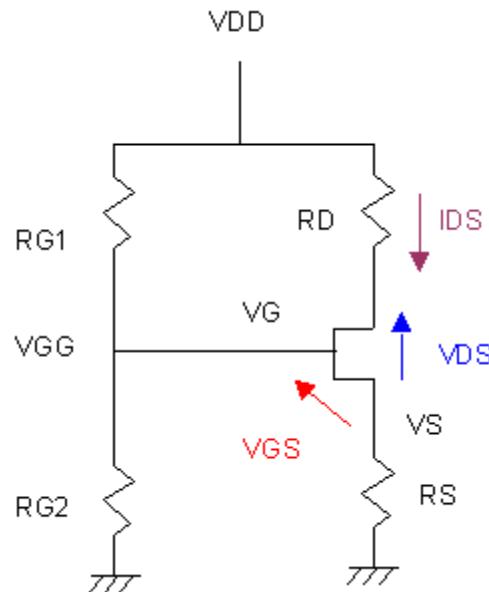
Grounding the source directly will provide the most gain from the FET, which is why this is a good idea if efficiency is a concern. In practice, the “adjustable” gate bias supply is often a fixed supply of perhaps –5 Volts, with an adjustable resistor-divider network being employed to supply the needed gate voltage.

Another method of biasing a FET is with an *active bias* network. This is an analog circuit that attempts to eliminate any manual adjustments to the FET Q-point, by using a small FET to “calculate” the required gate bias for the FET in the circuit and supply it to the larger FET which is the active device in the amplifier. Such a circuit is often called a “current mirror”. An active bias network, if designed properly, does not reduce the overall efficiency of a power amplifier by much. However, a negative supply voltage is still required, although it need only be at a fixed voltage such as –5 Volts.

The third way to bias a FET is to employ a “self-biasing” network, in which a resistor of a strategic value is placed between the source connection and ground. The resistor is bypassed with a capacitor so that the FET source connection sees a zero-Ohm connection to ground at the operating frequency. When drain current flows through the FET and then through the source resistor, the source voltage rises above ground. The gate voltage is either held at a fixed voltage or grounded, resulting in a fixed negative gate-source voltage, which is (hopefully) the intended Q-point. For example, if the gate was grounded, and the FET was drawing 200 mA of drain current through a 10-ohm source resistor, the gate-source bias would be –2 volts. The major advantage of

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the self-bias scheme over other bias schemes is that only a single positive voltage supply is needed to power up the amplifier. The downsides to using self-bias schemes are that amplifier efficiency is lost due to the voltage drop of the source resistor. Also, the FET cannot be RF grounded at all frequencies as well as if it was DC grounded with via holes, so gain and efficiency can be degraded as a result. Self-bias networks are often used in LNAs, but not power amplifiers, for these two reasons.



Self-bias network with raised gate voltage

Self-biasing secrets

The self-bias network is used to eliminate the need for a negative voltage to a FET-based amplifier. One of the ways to make a design less susceptible to normal variations in FET transfer characteristics (the gate voltage needed to induce a fixed drain current) is to raise the gate bias above ground. Such designs are often called “raised gate bias” designs.

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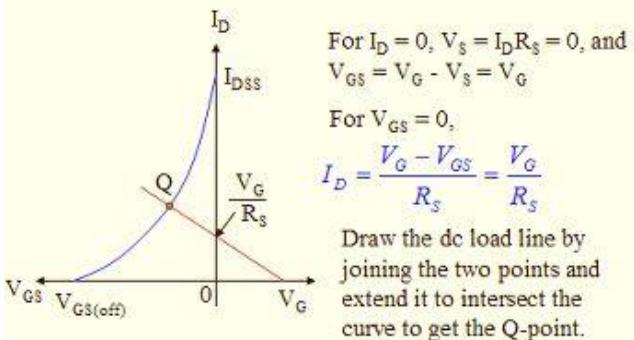
Below is an example from <http://ee.stlcc.info/132/fetbias.htm>

The bias equations for depletion-mode field-effect transistors are repeated in many books - for example, to find the drain current:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

This equation is easy to use if the right input parameters are known. However, FET self-bias circuits generate the required negative gate-source voltage by inserting a source resistor in series with the source terminal of the transistor. The resulting positive source voltage results in a negative gate-to-source bias.

Graphical Analysis of Voltage-Divider Biased JFET



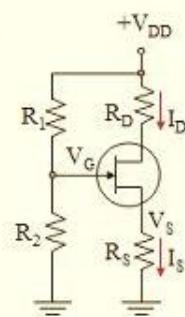
To keep the gate-source junction reverse-biased, $V_S > V_G$

$$V_S = I_D R_S$$

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

$$V_S = V_G - V_{GS}$$

$$I_D = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}$$



Since the drain current depends on gate bias, but the gate bias now depends on drain current, it is soon seen that the solution will require finding the roots of a quadratic equation. The actual solution will yield two roots, of course, but only the one representing the smaller drain current will be valid - the gate-source bias associated with the larger root will actually place the transistor beyond cutoff. That root is mathematically correct but physically meaningless.

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The importance of gate inductance cannot be over-emphasized for mm wave operation. In most cases the gate finger inductance will limit finger width to small fractions of a wavelength. It is controlling the gate inductance, too, which is the primary driver for the use of tee gates.

All FETs run up against a simple geometrical constraint: the channel has to scale down at least in proportion to the gate length, or gate control of the current is lost. This makes it hard to get power densities out of short gate devices.

InP actually has a bandgap of around 1.35 eV, but most InP based FETs have InGaAs based channels, which do have bandgaps around 0.75eV.

Most contacts (ohmic or Schottky) to compound semiconductors are far from perfectly stable over time. Some Schottky contacts might not be stable in the presence of hydrogen from, say, plated packages.

REFERENCES

(In this list, pioneer papers are privileged)

General references

- [1] S.A. Maas, *Nonlinear microwave circuits*, Norwood MA: Artech House, 1988.
 - [2] M.E. Hines, "The virtues of nonlinearity - detection, frequency conversion, parametric amplification and harmonic generation," *IEEE Trans. Microwave Theory Tech.*, Vol. 32, 1097-1104, Sept. 1984.
 - [3] F.T. Ulaby, *Fundamentals of applied electromagnetics*, Upper Saddle River NJ: Prentice Hall, 2007.
 - [4] S.M. Wentworth, *Fundamentals of electromagnetics with engineering applications*, John Wiley and Sons, 2005.
 - [5] R. Ludwig, P. Bretchko, *RF Circuit Design: Theory and Applications*, Upper Saddle River NJ: Prentice Hall, 2000.
 - [6] K. Chang, I. Bahl, V. Nair, *RF and Microwave Circuit and Component Design for Wireless Systems*, New York NY: Wiley, 2002.
 - [7] S. M. Sze, *Modern Semiconductor Device Physics*, New York NY: Wiley, 1997.
 - [8] I.E. Getreu, *Modeling the bipolar transistor*, Amsterdam: Elsevier, 1978.
 - [9] J.M. Golio, *Microwave MESFETs and HEMTs*, Norwood MA: Artech House, 1991.
 - [10] D.J. Roulston, *An introduction to the physics of semiconductor devices*, New York NY: Oxford University Press, 1999.
 - [11] C.M. Snowden, R.E. Miles, *Compound semiconductor device modelling*, London: Springer-Verlag, 1993.
 - [12] T.R. Turlington, *Behavioral modeling of nonlinear RF and microwave devices*, Norwood MA: Artech House, 2000.
 - [13] F. Ali, A. Gupta, *HEMTs and HBTs: devices, fabrication and circuits*, Norwood MA: Artech House, 1991.
-

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- [14] P.J. Bulman, G.S. Hobson, B.C. Taylor, *Transferred electron devices*, New York NY: Academic Press, 1972.
- [15] W.F. Chow, *Principles of tunnel diode circuits*, New York NY: Wiley, 1964.
- [16] C.M. Lee, R.J. Lomax, G.I. Haddad, "Semiconductor device simulation," *IEEE Trans. Microwave Theory Tech.*, Vol 22, 160-177, Mar. 1974.
- [17] N.T. Linh, "Two dimensional electron gas FET's: microwave applications," in *Semiconductors & semimetals*, Willardson R.K. and Beer A.C., Eds, Vol 24, New-York: Academic Press, 1985.
- [18] R.S. Pengelly, *Microwave field effect transistors-theory, design and applications*, Chichester England: Research studies, 1982.
- [19] J.O. Scanlan, *Analysis and synthesis of tunnel diode circuits*, Aberdeen U.K.: Wiley/University Press, 1966.
- [20] C.M. Snowden, "Microwave and millimeter-wave device and circuit design based on physical modelling," *Int. J. Microwave and Millimeter-Wave Computer-Aided Eng.*, Vol 1, 4-21, Jan. 1991.
- [21] P. Ladbrooke, *MMIC design: GaAs FETs and HEMTs*, Norwood MA: Artech House, 1989.

Diodes

- [22] H.A. Watson, *Microwave semiconductor devices and their circuit applications*, New York: Mc Graw Hill, 1969.
 - [23] S.M. Sze, *Physics of semiconductor devices*, 2nd Ed., New-York: Wiley, 1981.
 - [24] P.J. Bulman, G.S. Hobson, B.C. Taylor, *Transferred electron devices*, New York: Academic Press, 1972.
 - [25] C.M. Snowden, R.E. Miles, *Compound semiconductor device modelling*, London: Springer-Verlag, 1993.
 - [26] J.B. Gunn, "Microwave oscillations of current in III-V semiconductors," *Solid state Commun.*, Vol 1 (4), 88-91, 1963.
-

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- [27] R.L. Gunshor, A.C. Kak, "Lumped-circuit representation of Gunn diodes in domain mode," *IEEE Trans. on Electron Devices*, Vol 19, 765-770, June 1972.
 - [28] L.O. Chua, Y.W. Sing, "A generalized nonlinear lumped circuit model for Gunn diodes which includes field-dependent diffusion effects," *Electronics Research Lab.*, University of California, Berkeley, Memo ERL-M77-15, May 1977.
 - [29] L.O. Chua, Y.W. Sing, "A new nonlinear lumped circuit model for Gunn diodes," in Proc. *CAD of Electronic and Microwave Circuits and Syst. Conf.*, University of Hull, England, 1977.
 - [30] W.H. Haydl, "Fundamental and harmonic operation of millimeter-wave Gunn diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 31, 879-889, Nov. 1983.
 - [31] W.T. Read, Jr., "A proposed high frequency negative resistance diode," *Bell Syst. Tech. J.*, Vol 37, 401-444, 1958.
 - [32] G.I. Haddad, P.T. Greiling, W.E. Schroeder, "Basic principles and properties of avalanche transit-time devices," *IEEE Trans. Microwave Theory Tech.*, Vol 18, 752-772, Nov. 1970.
 - [33] S.M. Sze, R.M. Ryder, "Microwave avalanche diodes," *IEEE Proc.*, Vol 59, 1140-1154, Aug. 1971.
 - [34] H.C. Bowers, "IMPATT diodes start competing as microwave system amplifiers," *Electronics*, Vol 45, 82-88, Aug. 1972.
 - [35] P.A. Rolland, Vaterkowski J.L., Constant E., Salmer G., "New modes of operation for avalanche diodes : frequency multiplication and upconversion," *IEEE Trans. Microwave Theory Tech.*, Vol 24, 768-775, Nov. 1976.
 - [36] M.S. Gupta, "A nonlinear equivalent circuit for IMPATT diodes," *Solid State Electron.*, Vol 19, 23-26, Jan. 1976.
 - [37] L.H. Holway, Jr., S.L.G. Chu, "Theory and measurement of back bias voltage in IMPATT diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 31, 916-922, Nov. 1983.
 - [38] R. Pierzina, J. Freyer, "Power increase of pulsed millimeter-wave IMPATT diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 33, 1228-1231, Nov. 1985.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [39] C. Dalle, P.A. Rolland, "Drift-diffusion versus energy model for millimeter wave IMPATT diodes modeling," *Int. J. Numerical Modeling: Electronic Networks, Devices and Fields*, Vol 2 (1), 61-73, 1989.
 - [40] W. Behr, J.F. Luy, "High-power operation mode of pulsed IMPATT diodes," *IEEE Electron Device Letters*, Vol 11, 206-208, May 1990.
 - [41] U.C. Ray, A.K. Gupta, "Intrapulse frequency variation in a W-band pulsed IMPATT diode," *Microwave J.*, Vol 37, 238-244, April 1994.
 - [42] R. Judaschke, K. Schünemann, "Design and optimization of millimeter-wave IMPATT oscillators," in *IEEE Int. Microwave Symp. Dig.*, San Francisco, 939-942, 1996.
 - [43] J.I. Nishizawa, Y. Watanabe, "High frequency properties of the avalanching negative resistance diode," *Sci. Rep. Res. Inst. Tohoku Univ.*, Vol 10 (2), 91-108, 1958.
 - [44] Y. Hirachi, K. Kobayashi, K. Ogasawara, T. Hisatsugu, Y. Toyama, "A new operation mode 'surfing mode' in high-low-type GaAs IMPATT's," in Proc. *Int. Electron Device Meeting*, 102-105, 1976.
 - [45] J.I. Nishizawa, K. Motoya, Y. Okuno, "GaAs TUNNETT diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 26, 1029-1035, Dec. 1978.
 - [46] K.L. Kotzebue, "A circuit model of the step recovery diode," *Proc. IEEE*, Vol 53, 2119-2120, Dec. 1965.
 - [47] J. Zhang, A.V. Räisänen, "A survey on step recovery diode and its applications," *Report S 208, Radio Lab.*, Helsinki Univ., Sept. 1994.
 - [48] A.N. Pergande, "One Watt W-band transmitter," in *IEEE Int. Microwave Symp. Dig.*, San Diego, 305-308, 1994.
 - [49] J. Zhang, A.V. Räisänen, "Computer-aided design of step recovery diode frequency multipliers," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 2612-2616, Dec. 1996.
 - [50] P.L. Ntake, D.R. Conn, "Frequency multiplication by a P-I-N diode when driven into avalanche breakdown," *IEEE Trans. Microwave Theory Tech.*, Vol 23, 477-485, June 1975.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [51] R. Caverly, G. Hiller, "The small-signal AC impedance of GaAs and silicon PIN diodes," *Solid State Electron.*, Vol 33, 1255-1263, Oct. 1990.
 - [52] R. Caverly, N. Jain, "Modeling GaAs PIN diodes for microwave and millimeter wave applications," in Proc. *24th Eur. Microwave Conf.*, Cannes, 1622-1627, 1994.
 - [53] J. Harari, G.H. Jin, F. Journet, J. Vandecasteele, J.P. Vilcot, C. Dalle, M.R. Friscourt, D. Decoster, "Modeling of microwave top illuminated PIN photodetector under very high optical power," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 1484-1487, Aug. 1996.
 - [54] W. Schottky, "Spontaneous current fluctuations in electron streams," *Ann. Physik*, Vol 57, 541-567, Dec. 1918.
 - [55] B.J. Clifton, "Schottky-barrier diodes for submillimeter heterodyne detection," *IEEE Trans. Microwave Theory Tech.*, Vol 22, 270-275, Mar. 1974.
 - [56] G.T. Wrixon, "Schottky diode realization for low-noise mixing at millimeter wavelengths," *IEEE Trans. Microwave Theory Tech.*, Vol 24, 702-706, Nov. 1976.
 - [57] B.J. Clifton, "Schottky-barrier diodes for submillimeter heterodyne detection," *IEEE Trans. Microwave Theory Tech.*, Vol 25, 457-467, June 1977.
 - [58] K.S. Champlin, G. Eisenstein, "Cutoff frequency of submillimeter Schottky-barrier diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 26, 31-34, Jan. 1978.
 - [59] R.J. Mattauch, T.W. Crowe, W.L. Bishop, "Frequency and noise limits of Schottky barrier mixer diodes," *Microwave J.*, Vol 28, 101-116, Mar. 1985.
 - [60] W.L. Bishop, T.W. Crowe, R.J. Mattauch, H. Dossal, "Planar GaAs diodes for THz frequency mixing applications," in Proc. *Int. Symp. Space THz Technol.*, Ann Arbor MI, 1992.
 - [61] F.L. Vernon, Jr., M.F. Millea, M.F. Bottjer, A.H. Silver, R.J. Pedersen, M. McColl, "The super Schottky diode," *IEEE Trans. Microwave Theory Tech.*, Vol 25, 286-294, April 1977.
 - [62] R.L. Dickman, W.J. Wilson, G.G. Berry, "Super-Schottky mixer performance at 92 GHz," *IEEE Trans. Microwave Theory Tech.*, Vol 29, 788-793, Aug. 1981.
 - [63] P. Penfield, R.P. Rafuse, *Varactor applications*, Cambridge MA: M.I.T. Press, 1962.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [64] P. Philippe, W. El-Kamali, V. Pauker, "Physical equivalent circuit model for planar Schottky varactor diode," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 250-255, Feb. 1988.
 - [65] M.A. Frerking, J.R. East, "Novel heterojunction varactors," *Proc. IEEE*, Vol 80, 1853-1860, 1992.
 - [66] B.J. Rizzi, J.L. Hesler, H. Dossal, T.W. Crowe, "Varactor diode for millimeter and submillimeter wavelengths," in *Proc. 3rd Int. Symp. Space Terahertz Technol.*, Ann Arbor MI, 73-92, 1992.
 - [67] J.T. Louhi, A.V. Räisänen, "On the modeling and optimization of Schottky varactor frequency multipliers at submillimeter wavelengths," *IEEE Trans. Microwave Theory Tech.*, Vol 43, 922-926, April 1995.
 - [68] R.N. Hall, "Tunnel diodes," *IRE Trans. on Electron Devices*, Vol 7, 1-7, Jan. 1960.
 - [69] G. Dermit, "High-frequency power in Tunnel diodes," *Proc. IRE*, Vol 49, 1033-1042, June 1961.
 - [70] C.A. Burrus, "Gallium arsenide Esaki diodes for high frequency applications," *J. Appl. Phys.*, Vol 32, 1031-1036, June 1961.
 - [71] C.S. Kim, "Tunnel-diode converter analysis," *IEEE Trans. Electron Devices*, Vol 8, 394-405, Sept. 1961.
 - [72] J.A. Narud, S.S. Meyer, "A polynomial approximation for the tunnel diode characteristic," *IEEE Trans. on Circuit Theory*, Vol 10, 526-530, Dec. 1963.
 - [73] W.F. Chow, *Principles of tunnel diode circuits*, New York: Wiley, 1964.
 - [74] J.O. Scanlan, *Analysis and synthesis of tunnel diode circuits*, Aberdeen U.K.: Wiley/University Press, 1966.
 - [75] M.E. Hines, "Negative-resistance diode power amplification," *IEEE Trans. Electron Devices*, Vol 17, 1-8, Jan. 1970.
 - [76] R. Tsu, L. Esaki, "Tunneling in a finite superlattice," *Appl. Phys. Lett.*, Vol 22, 562-564, June 1973.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [77] I.E. Campisi, W.O. Hamilton, "Experimental properties of three-cavity tunnel diode RF oscillators," *IEEE Trans. Microwave Theory Tech.*, Vol 31, 905-910, Nov. 1983.
- [78] J.M. Gering, T.J. Rudnick, P.D. Coleman, "Microwave detection using the resonant tunneling diode," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 1145-1150, July 1988.
- [79] C. Kidner, I. Mehdi, J.R. East, G.I. Haddad, "Power and stability limitations of resonant tunneling diodes," *IEEE Trans. Microwave Theory Tech.*, Vol 38, 864-872, July 1990.
- [80] C.C. Yang, D.S. Pan, "Theoretical investigations of a proposed series integration of resonant tunneling diodes for millimeter-wave power generation," *IEEE Trans. Microwave Theory Tech.*, Vol 40, 434-441, Mar. 1992.
- [81] O.B. Lubecke, D.S. Pan, T. Itoh, "RF excitation of an oscillator with several tunneling devices in series," *IEEE Microwave and Guided Wave lett.*, Vol 4, 364-366, Nov. 1994.
- [82] O.B. Lubecke, D.S. Pan, T. Itoh, "Fundamental and subharmonic excitation for an oscillator with several tunneling diodes in series," *IEEE Trans. Microwave Theory Tech.*, Vol 43, 969-976, April 1995.

Transistors

- [82] I.E. Getreu, *Modeling the bipolar transistor*, Amsterdam: Elsevier, 1978.
- [83] R.S. Pengelly, *Microwave field effect transistors-theory, design and applications*, Chichester England: Research studies, 1982.
- [84] R. Soares, J. Graffeuil, J.J. Obregon, *Application des transistors à effet de champ en arsénure de gallium*, Paris: Eyrolles, 1984.
- [85] P. Ladbrooke, *MMIC design: GaAs FETs and HEMTs*, Norwood MA: Artech House, 1989.
- [86] J.M. Golio, *Microwave MESFETs and HEMTs*, Norwood MA: Artech House, 1991.
- [87] E.F. Crabbe, J.H. Comfort, J.D. Cressler, J.Y.C. Sun, J.M.C. Stork, "High-low polysilicon-emitter SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, Vol 14, 478-480, Oct. 1993.

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [88] J.D. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," *IEEE Trans. Microwave Theory Tech.*, Vol 46, 572-589, May 1998.
 - [89] P. Russer, "Si and SiGe millimeter-wave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, Vol 46, 590-603, May 1998.
 - [90] S.M.S. Imtiaz, S.M. El-Ghazaly, "Performance of MODFET and MESFET: a comparative study including equivalent circuits using combined electromagnetic and solid-state simulator," *IEEE Trans. Microwave Theory Tech.*, Vol 46, 923-931, July 1998.
 - [91] G. Ghione, C.U. Naldi, F. Filicori, "Physical modeling of GaAs MESFET's in an integrated CAD environment: from device technology to microwave circuit performance," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 457-468, Mar. 1989.
 - [92] C.M. Snowden, R.R. Pantoja, "GaAs MESFET physical models for process-oriented design," *IEEE Trans. Microwave Theory Tech.*, Vol 40, 1401-1409, July 1992.
 - [93] M.A. Alsunaidi, S.M.S. Imtiaz, S.M. El-Ghazali, "Electromagnetic wave effects on microwave transistors using a full-wave time-domain method," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 799-808, June 1996.
 - [94] H.A. Willing, C. Rauscher, P. De Santis, "A technique for predicting large-signal performance of a GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 26, 1017-1023, Dec. 1978.
 - [95] G. Halkias, H. Gerard, Y. Crosnier, G. Salmer, "A new approach to the RF power operation of MESFET's," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 817-825, May 1989.
 - [96] J.E. Purviance, M.C. Petzold, C. Potratz, "A linear statistical FET model using principal component analysis," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 1389-1394, Sept. 1989.
 - [97] J.F. Vidalou, J.F. Grossier, M. Chaumas, M. Camiade, P. Roux, J.J. Obregon, "Accurate nonlinear transistor modeling using pulsed S parameters measurements under pulsed bias conditions," in *IEEE Int. Microwave Symp. Dig.*, Boston, 95-98, 1991.
 - [98] S.A. Maas, D. Neilson, "Modeling GaAs MESFET's for intermodulation analysis," *Microwave J.*, Vol 34, 295-300, May 1991.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [99] K. Nagatomo, Y. Daido, M. Shimizu, N. Okubo, "GaAs MESFET characterization using least squares approximation by rational functions," *IEEE Trans. Microwave Theory Tech.*, Vol 41, 199-205, Feb. 1993.
 - [100] D.A. Patterson, V.F. Fusco, J.J. McKeown, J.A.C. Stewart, "A systematic optimization strategy for microwave device modeling," *IEEE Trans. Microwave Theory Tech.*, Vol 41, 395-405, Mar. 1993.
 - [101] T.A. Winslow, R.J. Trew, "Principles of large-signal MESFET operation," *IEEE Trans. Microwave Theory Tech.*, Vol 42, 935-942, June 1994.
 - [102] J. Bandler, R. Biernacki, Q. Cal, S.H. Chen, "Device statistical modelling and verification," *Microwave Eng. Europe*, 35-41, May 1995.
 - [103] J. Carroll, K. Whelan, S. Prichett, D.R. Bridges, "FET statistical modeling using parameter orthogonalization," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 47-54, Jan. 1996.
 - [104] J.A. Reynoso-hernandez, F.E. Rangel-Patino, J. Perdomo, "Full RF characterization for extracting the small-signal equivalent circuit in microwave FET's," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 2625-2633, Dec. 1996.
 - [105] M. Berroth, R. Bosch, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, Vol 38, 891-895, July 1990.
 - [106] M. Berroth, R. Bosch, "High frequency equivalent circuit of GaAs FET's for large-signal applications," *IEEE Trans. Microwave Theory Tech.*, Vol 39, 224-229, Feb. 1991.
 - [107] W. Shockley, "An unipolar 'field-effect' transistor," *Proc. IRE*, Vol 40, 1365-1376, Nov. 1952.
 - [108] H. Schichman, D.A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE J. Solid-State Circuits*, Vol 3, 285-289, Sept. 1968.
 - [109] T. Taki, "Approximation of junction field-effect transistor characteristics by a hyperbolic function," *IEEE J. Solid-State Circuits*, Vol 13, 724-726, Oct. 1978.
 - [110] H. Fukui, "Determinations of the basic parameters of a GaAs MESFET," *Bell Syst. Tech. J.*, Vol 58, 771-797, Mar. 1979.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [111] W.R. Curtice, "A MESFET model for use in the design of GaAs integrated circuits," *IEEE Trans. Microwave Theory Tech.*, Vol 28, 448-456, May 1980.
 - [112] Y. Tajima, B. Wrona, K. Mishima, "GaAs FET large-signal model and its application to circuit designs," *IEEE Trans. Electron Devices*, Vol 28, 171-175, Feb. 1981.
 - [113] T. Kacprzak, A. Materka, "Compact DC model of GaAs FET's for large-signal computer calculation," *IEEE J. Solid-State Circuits*, Vol 18, 211-213, April 1983.
 - [114] Y. Tajima, P.D. Miller, "Design of broad-band power GaAs FET amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol 32, 261-267, Mar. 1984.
 - [115] A. Materka, T. Kacprzak, "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. Microwave Theory Tech.*, Vol 33, 129-135, Feb. 1985.
 - [116] W.R. Curtice, M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, Vol 33, 1383-1393, Dec. 1985.
 - [117] H. Statz, P Newman., I.W. Smith, R.A. Pucel, H.A. Haus, "GaAs FET device and circuit simulation in SPICE," *IEEE Trans. Electron Devices*, Vol 34, 160-169, Feb. 1987.
 - [118] V.D. Hwang, T. Itoh, "An efficient approach for large-signal modeling and analysis of the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 35, 396-402, April 1987.
 - [119] W.R. Curtice, "GaAs MESFET modeling and nonlinear CAD," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 220-230, Feb. 1988.
 - [120] D.H. Huang, *Modeling GaAs field effect transistors*, Ph.D. dissertation, Maryland University, 1989.
 - [121] Z.R. Hu, J.J. McKeown, T. Brazil, J.A.C. Stewart, "Comparison of GaAs MESFET DC models," in *IEEE Int. Microwave Symp. Dig.*, 311-314, Dallas, 1990.
 - [122] R.J. Trew, "MESFET models for microwave computer-aided design," *Microwave J.*, Vol 33, 115-130, May 1990.
 - [123] A. McCamant, G. McCormack, D. Smith, "An improved GaAs MESFET model for SPICE," *IEEE Trans. Microwave Theory Tech.*, Vol 38, 822-824, June 1990.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [124] T.J. Brazil, "A universal large-signal equivalent circuit model for the GaAs MESFET," in *Proc. 21st European Microwave Conf.*, 921-926, 1991.
 - [125] T.J. Rodriguez, K.A. Mezher, O.M. Conde Portilla, J.C. Luengo Patronio, "A new highly accurate microwave nonlinear MESFET model," *Microwave J.*, Vol 36, 280-285, May 1993.
 - [126] J.P Teyssier., L.P. Viaud, R. Quere, "A new nonlinear I(V) model for FET devices including breakdown effects," *IEEE Microwave and guided Wave Lett.*, Vol 4, 104-107, April 1994.
 - [127] T. Fernández, Y. Newport, J.M. Zamanillo, A. Tazon, A. Mediavilla, "Extracting a bias-dependent large-signal MESFET model from pulsed I/V measurements," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 372-378, Mar. 1996.
 - [128] I. Angelov, *Chamlers nonlinear HEMT and MESFET model - extraction procedure*, Chamlers Univ., Report N°26, Nov. 1996.
 - [129] I. Angelov, V. Desmaris, K. Dynefors, P.A. Nilsson, N. Rorsman, H. Zirath, "On the large-signal modelling of AlGaN/GaN HEMTs and SiC MESFETs," *European Symp. on Gallium Arsenide and Other Semiconductor Application*, Oct. 3-4, 309-312, 2005.
 - [130] I. Angelov, L. Bengtsson, M. Garcia, "Extensions of the Chalmers nonlinear HEMT and MESFET model," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 1664-1674, Oct. 1996.
 - [131] G. Rafael-Valdivia, R. Brady, T.J. Brazil, "New drain current model for MESFET/HEMT devices based on pulsed measurements," *European Microwave Integrated Circuits Conf.*, Sept. 10-13, 289-291, 2006.
 - [132] Optotek Ltd, "Large-signal modeling of MESFETs and HEMTs," *Microwave J.*, Vol 40, 162-166, Nov. 1997.
 - [133] T.J. Rodriguez, M. Al-Daas, K.A. Mezher, "Comparison of nonlinear MESFET models for wideband circuit design," , " *IEEE Trans. Microwave Theory Tech.*, Vol 41, 288-293, Mar. 1994.
 - [134] M. Miller, M. Golio, B. Beckwith, E. Arnold, D. Halchin, S. Ageno, S. Dorn, "Choosing an optimum large-signal model for GaAs," in *IEEE Int. Microwave Symp. Dig.*, 1279-1282, Dallas, 1990.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [135] A. Madjar, F.J. Rosenbaum, "A practical AC large signal model for GaAs microwave MESFET," in *IEEE Int. Microwave Symp. Dig.*, Orlando, 399-401, 1979.
 - [136] A. Madjar, F.J. Rosenbaum, "A large signal model for the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 29, 781-788, Aug. 1981.
 - [137] D.L. Peterson, A.M. Pavio Jr., B. Kim, "A GaAs FET model for large signal applications," *IEEE Trans. Microwave Theory Tech.*, Vol 32, 276-281, Mar. 1984.
 - [138] M.S. Shur, "Analytical models of GaAs FET's," *IEEE Trans. Electron Devices*, Vol 32, 70-72, Jan. 1985.
 - [139] M.A. Khatibzadeh, R.J. Trew, "A large signal, analytic model for the GaAs MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 231-238, Feb. 1988.
 - [140] A. Madjar, "A fully analytical AC large-signal model for the GaAs MESFET for nonlinear network analysis and design," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 61-67, Jan. 1988.
 - [141] I. Corbella, J.M. Legido, G. Naval, "Instantaneous model of a MESFET for use in linear and nonlinear circuit simulations," *IEEE Trans. Microwave Theory Tech.*, Vol 40, 1410-1421, July 1992.
 - [142] L. Fujiang, G. Kompa, "FET model parameter extraction based on optimization with multiplane data-fitting and bidirectional search - a new concept," *IEEE Trans. Microwave Theory Tech.*, Vol 42, 1114-1121, 1994.
 - [143] G. Dambrine, A. Cappy, F. Heliodore, E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, Vol 36, 1151-1159, 1998.
 - [144] P.J. Tasker, M. Fernandez-Barciela, "HBT small signal T and π model extraction using a simple, robust and fully analytical procedure," *IEEE Int. MTT-Symp.*, Seattle, WA, USA, June 2-7, 2129–2132, 2002.
 - [145] M. Fernandez-Barciela, P.J. Tasker, Y. Campos-Roca, M. Demmler, H. Massler, E. Sanchez, M.C. Curras-Francos, M. Schlechtweg, "A simplified broad-band large-signal nonquasi-
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- static table-based FET model," *IEEE Trans. Microwave Theory Tech.*, Vol 48, 395-405, 2000.
- [146] R. Menozzi, A. Piazzini, F. Contini, "Small-signal modeling for microwave FET linear circuits based on a genetic algorithm," *IEEE Trans. Circuits Systems*, Vol 43, 839-847, 1996.
- [147] N.T. Linh, "Two dimensional electron gas FET's: microwave applications," in *Semiconductors & semimetals*, Willardson R.K. and Beer A.C., Eds, Vol 24, New-York: Academic Press, 1985.
- [148] M. Sholley, S. Maas, B. Allen, R. Sawires, A. Nichols, J. Abell, "HEMTs mm-wave amplifiers, mixers and oscillators," *Microwave J.*, Vol 28, 121-130, Aug. 1985.
- [149] P.M. Smith, A.W. Swanson, "HEMTs- low noise and power transistors for 1 to 100 GHz," *Applied Microwave*, 63-72, May 1989.
- [150] U.K. Mishra, A.S. Brown, M.J. Delaney, P.T. Greiling, C.F. Krumm, "The AlInAs-GaInAs HEMT for microwave and millimeter wave applications," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 1279-1287, Sept. 1989.
- [151] T.H. Chen, K.W. Chang, S.B.T. Bui, L.C.T. Liu, G.S. Dow, S. Pak, "Broadband single-and double-balanced resistive HEMT monolithic mixers," *IEEE Trans. Microwave Theory Tech.*, Vol 43, 477-484, Mar. 1995.
- [152] G. Zhang, R.D. Pollard, C.M. Snowden, "A novel technique for HEMT tripler design," in *IEEE Int. Microwave Symp. Dig.*, San-Fransisco, 663-666, 1996.
- [153] M.J. Bailey, "PHEMT devices offer high power density and efficiency," *Microwaves & RF*, Vol 36, 61-70, Feb. 1997.
- [154] C.E. Bilber, M.L. Schmatz, T. Morf, U. Lott, E. Morifuji, W. Bachtold, "Technology independent degradation of minimum noise figure due to pad parasitics," in *IEEE Int. Microwave Symp. Dig.*, Baltimore, 145-148, 1998.
- [155] H.R. Yeager, R.W. Dutton, "Circuit simulation models for the high electron mobility transistor," *IEEE Trans. Electron Devices*, Vol 33, 682-692, May 1986.

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [156] G.W. Wang, L.F. Eastman, "An analytical model for I-V and small-signal characteristics of planar-doped HEMT's," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 1395-1400, Sept. 1989.
 - [157] S.J. Mahon, D.J. Skellern, F. Green, "A technique for modelling S-parameters for HEMT structures as a function of gate bias," *IEEE Trans. Microwave Theory Tech.*, Vol 40, 1430-1440, July 1992.
 - [158] U. Gütlich, "Microstrip DROs: MESFET, PMHEMT, and HBT compared as active oscillator devices," in Proc. *Microwave and Optronics Conf.*, 341-344, Sindelfingen, 1995.
 - [159] K. Shirakawa, H. Oikawa, T. Shimura, Y. Kawasaki, Y. Ohashi, T. Saito, Y. Daido, "An approach to determining an equivalent circuit of HEMT's," *IEEE Trans. Microwave Theory Tech.*, Vol 43, 499-503, Mar. 1995.
 - [160] K. Shirakawa, M. Shimizu, Y. Kawasaki, Y. Ohashi, N. Okubo, "A new empirical large-signal HEMT model," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 622-624, April 1996.
 - [161] T. Tanimoto, "Analytical nonlinear HEMT model for large-signal circuit simulation," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 1584-1586, Sept. 1996.
 - [162] A. Miras, E. Legros, "Very high frequency small-signal equivalent circuit for short gate-length InP HEMT's," *IEEE Trans. Microwave Theory Tech.*, Vol 45, 1018-1026, July 1997.
 - [163] A. Ghazinour, R.H. Jansen, "Robust, model-independent generation of intrinsic characteristic and multi-bias parameter extraction for MESFETs/HEMTs," in *IEEE Int. Microwave Symp. Dig.*, Baltimore, 149-152, 1998.
 - [164] J.A. Turner, A.J. Waller, E. Kelley, D. Parker, "Dual-gate gallium arsenide microwave field-effect transistor," *Electron. Lett.*, Vol 7, 661-662, Nov. 1971.
 - [165] S. Asai, F. Murai, H. Kodera, "GaAs dual gate Schottky barrier FET's for microwave frequencies," *IEEE Trans. Electron Devices*, Vol 22, 897-904, Oct. 1975.
 - [166] T. Furutsuka, M. Ogawa, N. Kawamura, "GaAs dual gate MESFET's," *IEEE Trans. Electron Devices*, Vol 25, 580-586, June 1978.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [167] P.T. Chen, C.T. Li, P.H. Wang, "Performance of a dual-gate GaAs MESFET as a frequency multiplier at Ku-band," *IEEE Trans. Microwave Theory Tech.*, Vol 27, 411-415, May 1979.
 - [168] C. Tsironis, R. Meierer, "Microwave wide-band model of GaAs dual gate MESFET's," *IEEE Trans. Microwave Theory Tech.*, Vol 30, 243-251, Mar. 1982.
 - [169] J.R. Scott, R.A. Minasian, "A simplified microwave model of the GaAs dual-gate MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 32, 243-248, Mar. 1984.
 - [170] C. Tsironis, R. Meierer, R. Stahlmann, "Dual gate MESFET mixers," *IEEE Trans. Microwave Theory Tech.*, Vol 32, 248-255, Mar. 1984.
 - [171] B. Kim, H.Q. Tserng, P. Saunier, "GaAs dual-gate FET for operation up to K-band," *IEEE Trans. Microwave Theory Tech.*, Vol 32, 256-261, Mar. 1984.
 - [172] T. Sugiura, K. Honjo, T. Tsuji, "12-GHz-band GaAs dual gate MESFET monolithic mixers," *IEEE Trans. Microwave Theory Tech.*, Vol 33, 105-110, Feb. 1985.
 - [173] R.B. Darling, "Distributed numerical modeling of dual gate GaAs MESFET's," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 1351-1360, Sept. 1989.
 - [174] M. Schöön, "A novel, bias-dependent, small-signal model of the dual gate MESFET," *IEEE Trans. Microwave Theory Tech.*, Vol 42, 212-216, Feb. 1994.
 - [175] K. Hartmann, M.J.O. Strutt, "Computer simulation of small-signal and noise behavior of microwave bipolar transistors up to 12 GHz," *IEEE Trans. Microwave Theory Tech.*, Vol 22, 178-183, Mar. 1974.
 - [176] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proc. IEEE*, Vol 70, 13, 1982.
 - [177] H. Ito, T. Ishibashi, T. Sugeta, "Fabrication and characterization of AlGaAs/GaAs heterojunction bipolar transistor," *IEEE Trans. Electron Devices*, Vol 34, 224-229, Feb. 1987.
 - [178] M.E. Kim, A.K. Oki, G.M. Gorman, D.K. Umemoto, J.B. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications," *IEEE Trans. Microwave Theory Tech.*, Vol 37, 1395-1400, Sept. 1989.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [179] H. Asano, S. Hara, S. Komai, "A 900 MHz HBT power amplifier MMICs with 55 % efficiency at 3.3V operation," in *IEEE Int. Microwave Symp. Dig.*, Baltimore, 205-208, 1998.
 - [180] D. Costa, W. Liu, J.S. Harris, Jr., "A new direct method for determining the heterojunction bipolar transistor equivalent circuit model," in Proc. *IEEE Bipolar Circuits and Tech. Meeting*, 118-121, 1990.
 - [181] D.A. Teeter, J.R. East, R.K. Mains, G.I. Haddad, "large-signal numerical and analytical HBT models," *IEEE Trans. Electron Devices*, Vol 40, 837-845, May 1993.
 - [182] U. Schaper, B. Holzapfl, "Analytical parameter extraction of the HBT equivalent circuit with T-like topology from measured S-parameters," *IEEE Trans. Microwave Theory Tech.*, Vol 43, 493-498, Mar. 1995.
 - [183] R. Hajji, A.B. Kouki, S.E. Rabaie, F.M. Ghannouchi, "Systematic dc/small-signal/large-signal analysis of heterojunction bipolar transistors using a new consistent nonlinear model," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 233-240, Feb. 1996.
 - [184] S. Lee, "Fast and efficient extraction of HBT model parameters using multibias S-parameter sets," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 1499-1502, Aug. 1996.
 - [185] K. Yang, A.L. Gutierrez-Aitken, X. Zhang, P. Bhattacharya, G.I. Haddad, "An HSPICE HBT model for InP-based single HBT's," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 1470-1472, Sept. 1996.
 - [186] Q.M. Zhang, H. Hu, J. Sitch, R.K. Surridge, J.M. Xu, "A new large signal HBT model," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 2001-2009, Nov. 1996.
 - [187] C.J. Wei, J.C.M. Hwang, W.J. Ho, J.A. Higgins, "Large-signal modeling of self-heating, collector transit-time, and RF-breakdown effects in power HBT's," *IEEE Trans. Microwave Theory Tech.*, Vol 44, 2641-2647, Dec. 1996.
 - [188] J.M.M. Rios, L.M. Lunardi, S. Chandrasekhar, Y. Miyamoto, "A self-consistent method for complete small-signal parameter extraction of InP-based heterojunction bipolar transistors (HBT's)," *IEEE Trans. Microwave Theory Tech.*, Vol 45, 39-44, Jan. 1997.
-

The materials you receive for this course are protected by copyright and to be used for this course only. You do not have permission to upload the course materials, including any lecture recordings you may have, to any website. If you require clarification, please consult your professor.

- [189] A. Samelis, D. Pavlidis, "DC to high-frequency HBT-model parameter evaluation using impedance block conditioned optimization," *IEEE Trans. Microwave Theory Tech.*, Vol 45, 886-897, June 1997.
- [190] S. Searles, D.L. Pulfrey, T.C. Kleckner, "Analytical expressions for the tunnel current at abrupt semiconductor- semiconductor heterojunctions," *IEEE Trans. Microwave Theory Tech.*, Vol 45, 1851-1856, Nov. 1997.
- [191] M. Rudolph, R. Doerner, P. Heymann, "Direct extraction of HBT equivalent circuit elements," *IEEE Trans. Microwave Theory Tech.*, Vol 47, 82-84, Jan. 1999.
- [192] J.J. Ebers, J.L Moll., "Large-signal behavior of junction transistors," *Proc. IRE*, Vol 42, 1954.
- [193] H.K. Gummel, "Computer device modeling," in Proc. *European Sem. Develop. Res. Conf.*, Munich, 1969.
- [194] H.C. Poon, H.K. Gummel, "Modeling of emitter capacitance," *Proc. IEEE*, Vol 57, 2181-2182, 1969.
- [195] H.K. Gummel, H.C. Poon, "An integral charge control model of bipolar transistors," *Bell Syst. Tech. J.*, Vol 49, 827, 1970.
- [196] J.M.M. Rios, L.M. Lunardi, S. Chandrasekhar, Y. Miyamoto, "A self-consistent method for complete small-signal parameter extraction of InP-based heterojunction bipolar transistors," *IEEE Trans. Microwave Theory Tech.*, Vol 45, 39-45, 1997.
- [197] B. Sheinman, E. Wasige, M. Rudolph, R. Doerner, V. Sidorov, S. Cohen, D. Ritter, "A peeling algorithm for extraction of the HBT small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, Vol 50, 2804-2810, 2002.
- [198] T.H. Teo, Y.Z. Xiong, J.S. Fu, H. Liao, J. Shi, M. Yu, W. Li, "Systematic direct parameter extraction with substrate network of SiGe HBT," *Radio Frequency Integrated Circuit Symp.*, Fort Worth, TX, USA, June 6-8, 603-606, 2004.

Perspectives

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- [199] D. Halchin, M. Golio, "Trends for portable wireless applications," *Microwave J.*, Vol 40, 62-78, Jan. 1997.
 - [200] "Focus on MMICs, RFICs & circuit technology," *Microwave Eng. Europe*, 17-25, Feb. 1998.
 - [201] T. Edwards, "Countdown to the microwave millenium," *Microwave J.*, Vol 41, 70-81, June 1998.
 - [202] D. Friday, "Microwave technology : directions and measurement requirements for the 21th century," *Microwave J.*, Vol 41, 110-114, June 1998.
 - [203] J. Del Alamo, M. Somerville, R. Blanchard, "Millimeter wave power InP HEMTs : challenges and prospects," *Microwave Eng. Europe*, 49-52, Mar. 1999.
 - [204] R.R. Tummala, M. Swaminathan, M.M. Tentzeris, J. Laskar, G.-K. Chang, S. Sitaraman, D. Keezer, D. Guidotti, Z. Huang, K. Lim, L. Wan, S.K. Bhattacharya, V. Sundaram, F. Liu, P. M. Raj, "The SOP for miniaturized, mixed-signal computing, communication, and consumer systems of the next decade," *IEEE Trans. Advanced Packaging*, Vol 27, 250-267, 2004.
 - [205] K. Uchida, "Single-electron transistors and circuits for future ubiquitous computing applications," *European Solid-State Device Research Conf.*, Montreux, Switzerland, Sept. 18-22, 17-20, 2006.
 - [206] V.G. Mashkantsev, S.V. Kalinin, "The perspective structures for microwave heterotransistors for communication techniques," *Int. Workshop on Electron Devices and Materials*, Novosibirsk, Russia, July 1-5, 24-26, 2006.
 - [207] B. Razavi, "Design considerations for future RF circuits," *IEEE Int. CAS-Symp.*, New Orleans, LA, USA, May 27-30, 741-744, 2007.
 - [208] P. Phokharatkul, S. Phaiboon, "Mobile propagation path loss models for suburban areas using type-2 fuzzy logic approximation," *Int. Conf. on Microwave and Millimeter Wave Technology*, Beijing, China, Aug. 18-21, 158-162, 2004.
 - [209] E.L. Piner, S. Singhal, P. Rajagopal, R. Therrien, J.C. Roberts, T. Li, A.W. Hanson, J.W. Johnson, I.C. Kizilyalli, K.J. Linthicum, "Device degradation phenomena in GaN HFET
-

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- technology: status, mechanisms, and opportunities,” *Int. Electron Devices Meeting*, San Francisco, CA, USA, Dec. 11-13, 2006, 1-4.
- [210] R. Chau, “Challenges and opportunities of emerging nanotechnology for VLSI nanoelectronics,” *Int. Semiconductor Device Research Symp.*, Maryland, MD, USA, Dec. 12-14, 2007.
- [211] Y. Sun, L.F. Eastman, “Trade-offs and challenges of short channel design on millimetre-wave power performance of GaN HFETs,” *Electronics Letters*, Vol 41, 854-855, 2005.
- [212] B. Bosco, R. Emrick, S. Franson, J. Holmes, S. Rockwell, “Emerging commercial applications using the 60 GHz unlicensed band: opportunities and challenges,” *IEEE Annual Wireless and Microwave Technology Conf.*, Clearwater, FL, USA, Dec. 4-5, 2006.

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APPENDIX II-1

DIODES - SUMMARY

<http://www.radio-electronics.com/info/data/semicond/diodes/types-of-diodes.php>

There are many different types of diodes that are available for use in electronics design. Different semiconductor diode types can be used to perform different functions as a result of the properties of these different diode types.

Semiconductor diodes can be used for many applications. The basic application is obviously to rectify waveforms. This can be used within power supplies or within radio detectors. Signal diodes can also be used for many other functions within circuits where the "one way" effect of a diode may be required.

Diodes are not just used as rectifiers, as various other types of diode can be used in many other applications. Some other different types of diodes include: light emitting diodes, photo-diodes, laser diodes and more as detailed below.

Many of the different types of diodes mentioned below have further pages providing in-depth information about them including their structures, method of operation, how they may be used in circuits, and precautions and tips for using them in electronics design.

It is sometimes useful to summarize the different types of diode that are available. Some of the categories may overlap, but the various definitions may help to narrow the field down and provide an overview of the different diode types that are available.

- **Backward diode:** This type of diode is sometimes also called the back diode. Although not widely used, it is a form of PN junction diode that is very similar to the tunnel diode in its operation. It finds a few specialist applications where its particular properties can be used.
Read more about the [Backward diode](#)
- **BARITT diode:** This form of diode gains its name from the words Barrier Injection Transit Time diode. It is used in microwave applications and bears many similarities to the more widely used IMPATT diode. *Read more about the [Baritt diode](#)*
- **Gunn Diode:** Although not a diode in the form of a PN junction, this type of diode is a semiconductor device that has two terminals. It is generally used for generating microwave signals. *Read more about the [Gunn diode](#)*
- **Laser diode:** This type of diode is not the same as the ordinary light emitting diode because it produces coherent light. Laser diodes are widely used in many applications from DVD and CD drives to laser light pointers for presentations. Although laser diodes are much cheaper than other forms of laser generator, they are considerably more expensive than LEDs. They also have a limited life. *Read more about the [laser diode](#)*
- **Light emitting diodes:** The light emitting diode or LED is one of the most popular types of diode. When forward biased with current flowing through the junction, light is produced. The diodes use component semiconductors, and can produce a variety of colours, although the original colour was red. There are also very many new LED developments that are changing the way displays can be used and manufactured. High output LEDs and OLEDs are two examples. *Read more about the [light emitting diode](#)*
- **Photodiode:** The photo-diode is used for detecting light. It is found that when light strikes a PN junction it can create electrons and holes. Typically photo-diodes are operated under reverse bias conditions where even small amounts of current flow resulting from the light can be easily detected. Photo-diodes can also be used to generate electricity. For some

applications, PIN diodes work very well as photodetectors. [**Read more about the photodiode**](#)

- **PIN diode:** This type of diode is typified by its construction. It has the standard P type and N-type areas, but between them there is an area of Intrinsic semiconductor which has no doping. The area of the intrinsic semiconductor has the effect of increasing the area of the depletion region which can be useful for switching applications as well as for use in photodiodes, etc. [**Read more about the PIN diode**](#)
- **PN Junction:** The standard PN junction may be thought of as the normal or standard type of diode in use today. These diodes can come as small signal types for use in radio frequency, or other low current applications which may be termed as signal diodes. Other types may be intended for high current and high voltage applications and are normally termed rectifier diodes. [**Read more about the diode**](#)
- **Schottky diodes:** This type of diode has a lower forward voltage drop than ordinary silicon PN junction diodes. At low currents the drop may be somewhere between 0.15 and 0.4 volts as opposed to 0.6 volts for a silicon diode. To achieve this performance they are constructed in a different way to normal diodes having a metal to semiconductor contact. They are widely used as clamping diodes, in RF applications, and also for rectifier applications. [**Read more about the Schottky diode**](#)
- **Step recovery diode:** A form of microwave diode used for generating and shaping pulses at very high frequencies. These diodes rely on a very fast turn off characteristic of the diode for their operation. [**Read more about the Step recovery diode**](#)
- **Tunnel diode:** Although not widely used today, the tunnel diode was used for microwave applications where its performance exceeded that of other devices of the day. [**Read more about the Tunnel diode**](#)
- **Varactor diode or varicap diode:** This type of diode is used in many radio frequency (RF) applications. The diode has a reverse bias placed upon it and this varies the width of the depletion layer according to the voltage placed across the diode. In this configuration the varactor or varicap diode acts like a capacitor with the depletion region being the insulating dielectric and the capacitor plates formed by the extent of the conduction regions. The

capacitance can be varied by changing the bias on the diode as this will vary the width of the depletion region which will accordingly change the capacitance. [**Read more about the varactor diode**](#)

- **Zener diode:** The Zener diode is a very useful type of diode as it provides a stable reference voltage. As a result it is used in vast quantities. It is run under reverse bias conditions and it is found that when a certain voltage is reached it breaks down. If the current is limited through a resistor, it enables a stable voltage to be produced. This type of diode is therefore widely used to provide a reference voltage in power supplies. Two types of reverse breakdown are apparent in these diodes: Zener breakdown and Impact Ionisation. However the name Zener diode is used for the reference diodes regardless of the form of breakdown that is employed. [**Read more about the Zener / voltage reference diode**](#)

Semiconductor diodes are widely used throughout all areas of the electronics industry from electronics design through to production and repair. The semiconductor diode is very versatile, and there are very many variants and different types of diode that enable all the variety of different applications to be met.

The different diode types of types of diodes include those for small signal applications, high current and voltage as well as different types of diodes for light emission and detection as well as types for low forward voltage drops, and types to give variable capacitance. In addition to this there are a number of diode types that are used for microwave applications.

Understanding Diode Specifications & Parameters

Diode datasheets provide a large amount of data - diode specifications and parameters about the diodes. The exact explanations of what these diode specifications and parameters are may not always be available. The list below provides a summary of some of the more widely used diode specifications, parameters and limits detailing their meanings.

- **Semiconductor material:** The semiconductor material used in the PN junction diode is of paramount importance because the material used affects many of the major diode characteristics and properties. Silicon is the most widely used material as it offers high levels of performance for most applications and it offers low manufacturing costs. The other material that is used is germanium. Other materials are generally reserved for more specialist diodes. The semiconductor material choice is of particular importance as it governs the turn on voltage for the diode - around 0.6volts for silicon and 0.3 volts for germanium, etc..
- **Forward voltage drop (V_f):** Any electronics device passing current will develop a resulting voltage across it and this diode characteristic is of great importance, especially for power rectification where power losses will be higher for a high forward voltage drop. Also RF diodes often need a small forward voltage drop as signals may be small but still need to overcome it. The voltage across a PN junction diode arise for two reasons. The first of the nature of the semiconductor PN junction and results from the turn-on voltage mentioned above. This voltage enables the depletion layer to be overcome and for current to flow. The second arises from the normal resistive losses in the device. As a result a figure for the forward voltage drop at a specified current level will be given. This figure is particularly important for rectifier diodes where significant levels of current may be passed.
- **Peak Inverse Voltage (PIV):** This diode characteristic is the maximum voltage a diode can withstand in the reverse direction. This voltage must not be exceeded otherwise the device may fail. This voltage is not simply the RMS voltage of the incoming waveform. Each circuit needs to be considered on its own merits, but for a simple single diode half wave rectifier with some form of smoothing capacitor afterwards, it should be remembered that the capacitor will hold a voltage equal to the peak of the incoming voltage waveform. The diode will then also see the peak of the incoming waveform in the reverse direction and therefore under these circumstances it will see a peak inverse voltage equal to the peak to peak value of the waveform.

- **Maximum forward current:** When designing a circuit that passes any levels of current it is necessary to ensure that the maximum current levels for the diode are not exceeded. As the current levels rise, so additional heat is dissipated and this needs to be removed.
- **Leakage current:** If a perfect diode were available, then no current would flow when it was reverse biased. It is found that for a real PN junction diode, a very small amount of current flows in the reverse direction as a result of the minority carriers in the semiconductor. The level of leakage current is dependent upon three main factors. The reverse voltage is obviously significant. It is also temperature dependent, rising appreciably with temperature. It is also found that it is very dependent upon the type of semiconductor material used - silicon is very much better than germanium. The leakage current characteristic or specification for a PN junction diode is specified at a certain reverse voltage and particular temperature. The specification is normally defined in terms of microamps, μA or picoamps, pA .
- **Junction capacitance:** All PN junction diodes exhibit a junction capacitance. The depletion region is the dielectric spacing between the two plates which are effectively formed at the edge of the depletion region and the area with majority carriers. The actual value of capacitance being dependent upon the reverse voltage which causes the depletion region to change (increasing reverse voltage increases the size of the depletion region and hence decreases the capacitance). This fact is used in varactor or varicap diodes to good effect, but for many other applications, especially RF applications this needs to be minimised. As the capacitance is of importance it is specified. The parameter is normally detailed as a given capacitance (in pF) at a given voltage or voltages. Also special low capacitance diodes are available for many RF applications.
- **Package type:** Diodes can be mounted in a variety of packages according to their applications, and in some circumstances, especially RF applications, the package is a key element in defining the overall RF diode characteristics. Also for power applications where heat dissipation is important, the package can define many of the overall diode parameters because high power diodes may require packages that can be bolted to heatsinks, whereas small signal diodes may be available in leaded formats or as surface mount devices.

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1 DESCRIPTION

The Gunn diode is the best known and most readily available device in the family of transferred electron devices (TED). They are employed as DC to microwave converters using the negative resistance characteristics of bulk Gallium Arsenide (GaAs) and only require a standard, low impedance, constant voltage power supply, thereby eliminating complex circuitry.

The DC1200 series of GaAs Gunn diodes is designed for operation at fixed frequency (determined by the oscillator cavity) within a specified band under CW or pulsed conditions. Both conventional and hot electron injected (graded-gap) Gunn diode designs are available (see Section 2). All devices feature low FM and AM noise characteristics and their wideband negative resistance enables them to be used in voltage controlled and mechanically tuned oscillators. The hot electron injected Gunn diodes offer the additional advantages of:

- higher fundamental frequency operation,
- increased efficiency,
- improved temperature stability,
- improved turn-on characteristic and
- reduced FM sideband noise.

Devices are available in either polarity, but are generally supplied as negative heat sink.

1.1 Package Styles

Several standard package styles are offered covering the frequency range 4 to 110 GHz and designed to suit different applications (see Fig. 1.1). Custom packaging requirements will also be considered upon request.

The following package limitations need to be taken into consideration:

Thermal Resistance

The lowest thermal resistance is offered by the screw-based packages (outlines 40, 86 and 106). For high volume, lower power applications where oscillator assembly time is more important, non-threaded packages such as outline 00 will be preferred (refer to Mounting and Heat Sink Considerations - Section 3.3).

Frequency Range

The equivalent circuit diagram of a packaged Gunn diode is shown in Fig. 1.2. The magnitude of the parasitic impedances attributed to the package element reduces with the package size (00 > 86 > 106). Consequently, the larger, more robust package styles are normally specified for operation at lower frequencies and the smaller, low parasitic impedance packages are recommended for the higher frequency applications.

Magnetically Tuned Circuits

For applications involving magnetically (YIG) tuned oscillators, Gunn diodes can be supplied in Kovar-free packages.

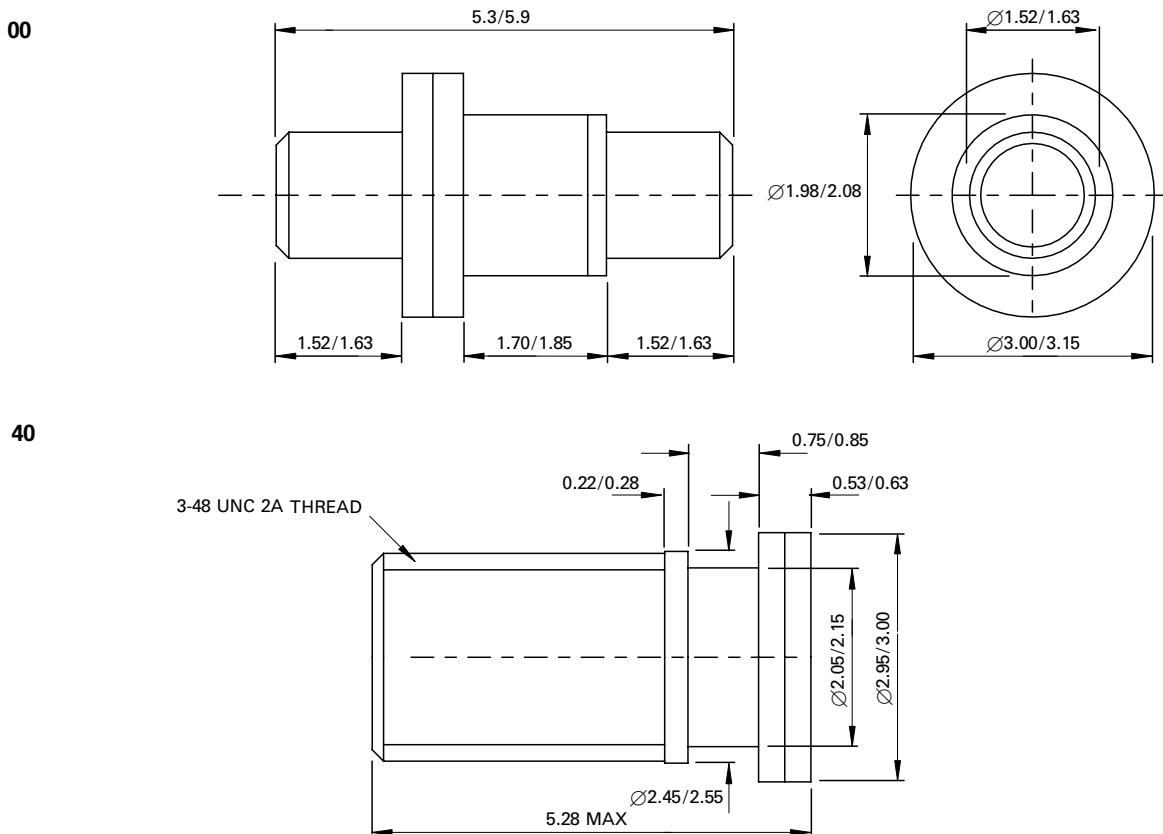
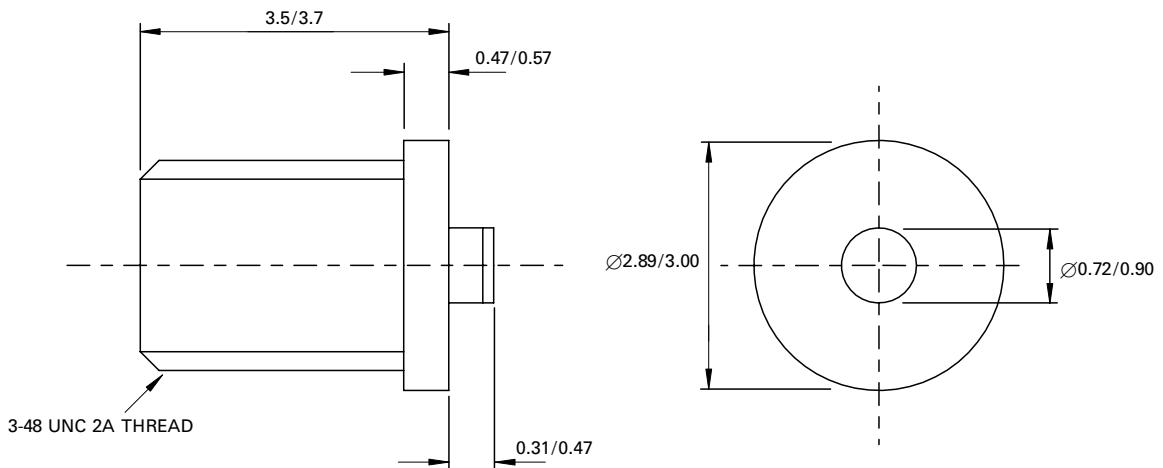
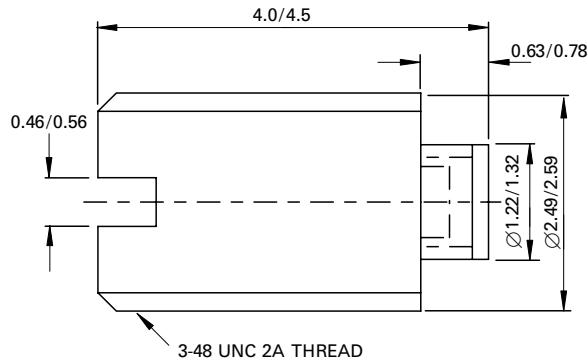
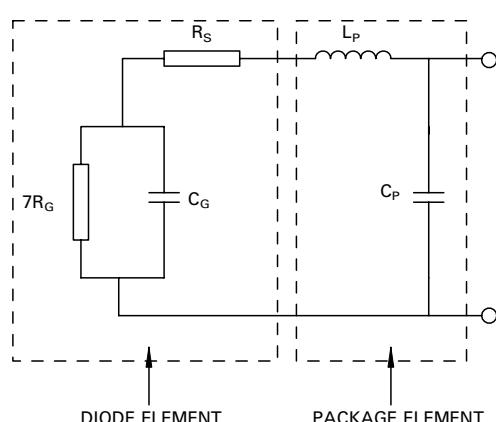


Fig. 1.1 Standard Gunn Diode Package Outlines (continued on page 3)



1.2 Gunn Oscillators

E2V Technologies designs and manufactures a range of oscillator products using E2V Gunn diodes. Standard products include a range of fixed frequency and mechanically or electronically tuned oscillators. Enquiries are welcomed for oscillator products that are not in the standard range.



C_P = PACKAGE CAPACITANCE
 L_P = BOND LEAD INDUCTANCE
 R_S = SERIES RESISTANCE
 7R_G = GUNN DIODE RESISTANCE
 C_G = GUNN DIODE CAPACITANCE

Fig. 1.2 Simple Equivalent Circuit for a Packaged Gunn Diode

2 PRINCIPLE OF OPERATION

2.1 Gunn Diode Theory

In order to understand the nature of the transferred electron effect exhibited by Gunn diodes, it is necessary to consider the electron drift velocity versus electric field (or current versus voltage) relationship for GaAs (see Fig. 2.1).

Below the threshold field, E_{th} , of approximately $0.32 \text{ V}/\mu\text{m}$, the device acts as a passive resistance. However, above E_{th} the electron velocity (current) decreases as the field (voltage) increases producing a region of negative differential mobility, NDM (resistance, NDR). This is the essential feature that leads to current instabilities and Gunn oscillations in an active device and is due to the special conductance band structure of direct band gap semiconductors such as Gallium Arsenide (see Fig. 2.2).

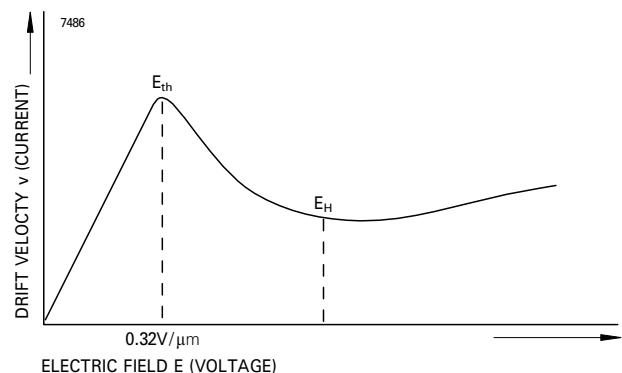


Fig. 2.1 The Electric Field Dependent Average Drift Velocity for N-type GaAs

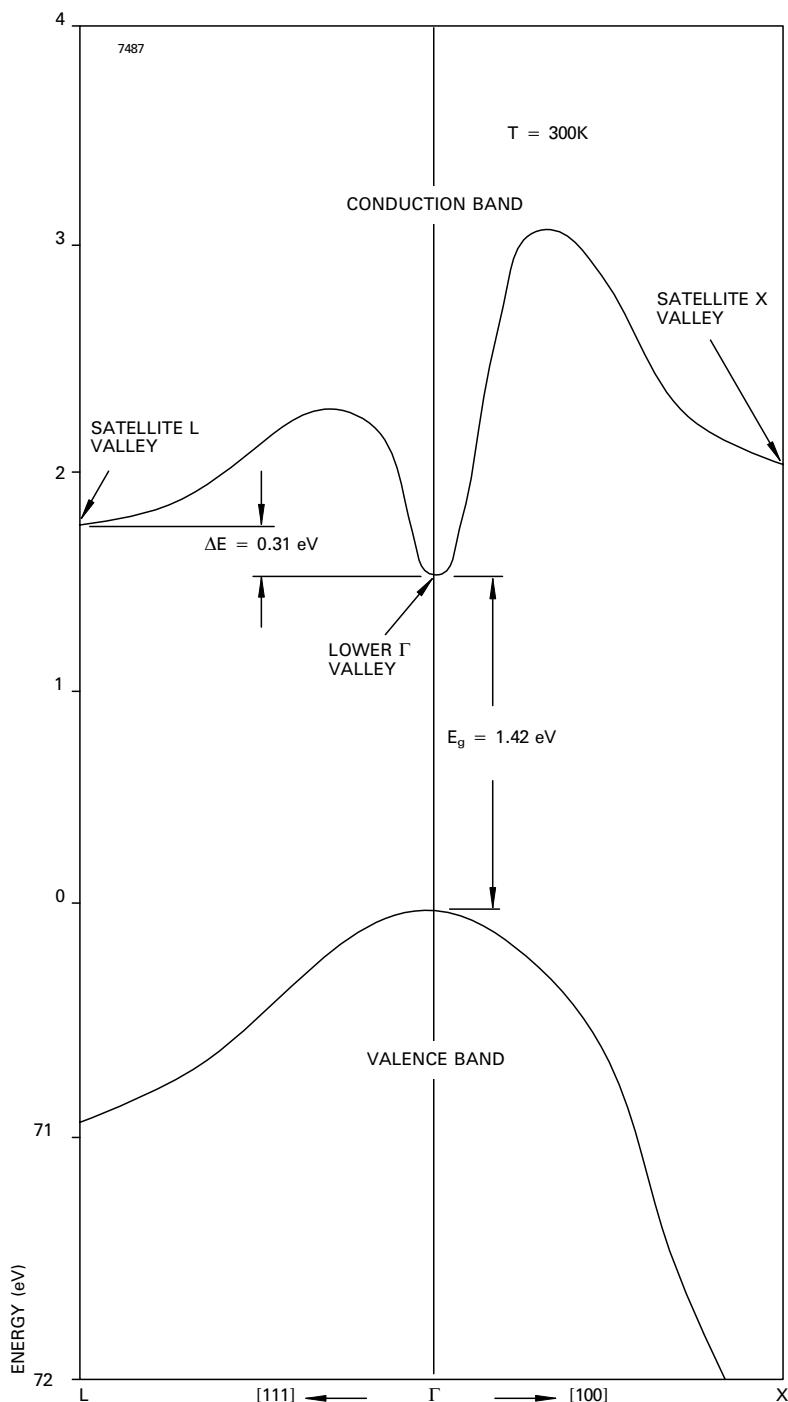


Fig. 2.2 The Band Structure of GaAs at 300 K

The energy-momentum relationship contains two conduction band energy levels, Γ and L (also known as valleys) with the following properties:

- In the lower Γ valley, electrons exhibit a small effective mass and very high mobility, μ_1 .
- In the satellite L valley, electrons exhibit a large effective mass and very low mobility, μ_2 .
- The two valleys are separated by a small energy gap, ΔE , of approximately 0.31 eV.

In equilibrium at room temperature most electrons reside near the bottom of the lower Γ valley. Because of their high mobility ($\sim 8000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$), they can readily be accelerated in a strong electric field to energies in the order of the Γ -L

intervalley separation, ΔE . Electrons are then able to scatter into the satellite L valley, resulting in a decrease in the average electron mobility, μ , as given below:

$$\mu = (n_1 \cdot \mu_1 + n_2 \cdot \mu_2) / (n_1 + n_2)$$

where n_1 = electron density in Γ valley
 n_2 = electron density in L valley

Above the high field, E_H , most electrons reside in the L valley and the device behaves as a passive resistance (of greater magnitude) once again.

In a practical Gunn diode, electrons are accelerated from the cathode by the prevailing electric field. When they have acquired sufficient energy, they begin to scatter into the low mobility satellite valley and slow down. This charge fluctuation

results in a localised increase in the electric field and a corresponding decrease (to below the threshold value) elsewhere within the sample. Electrons ahead of the region still exhibit high mobility and move away from the charge fluctuation causing a depletion of carriers. Electrons behind the charge fluctuation, are also moving faster and accumulate behind the depleted region causing a dipole (or high field) domain (see Fig. 2.3), which grows in amplitude.

A fall in current is associated with the domain growth due to its reduced mobility. The domain propagates through the sample at a constant velocity ($\sim 1 \times 10^7 \text{ cm.s}^{-1}$ for GaAs) until it reaches the anode where it collapses. As the domain collapses, the electric field outside the domain rises and the current in the external circuit increases until the threshold field is reached again and a new domain is formed.

For a given doping density there will be a minimum device length that will support a domain due to the finite time required for domain growth. If this time is longer than that required for the domain to traverse the sample, then domain formation will not occur. Similarly, if the doping density is too high, then the current (and hence the temperature) in the semiconductor becomes too great and the life expectancy of the device is reduced. In practice, the product of doping density, n , and device length, l , is maintained between the following limits:

$$1 \times 10^{12} \text{ cm}^{-2} \leq n.l \leq 2 \times 10^{12} \text{ cm}^{-2}$$

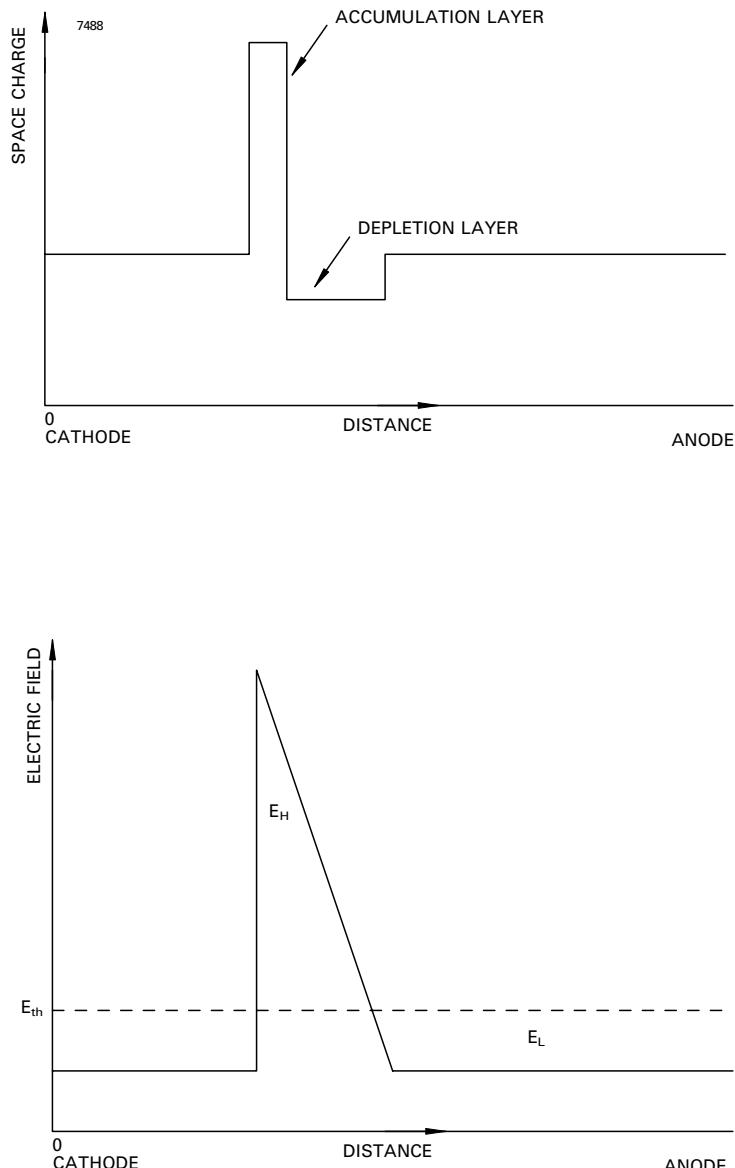


Fig. 2.3 The Band Structure of GaAs at 300 K

2.2 Modes of Oscillation

2.2.1 Transit Time Mode

This is the basic diode oscillation mode and is independent of the external circuit. Current peaks are obtained when a domain is quenched at the anode, after which another is nucleated near the cathode. The frequency is determined by the domain transit time, T_t :

$$T_t = l/v_D$$

where l = length of device

v_D = domain velocity ($\sim 1 \times 10^7 \text{ cm.s}^{-1}$)

so frequency, f_t :

$$f_t = 1/T_t = v_D/l$$

This mode of operation was first reported by (and is named after) J. B. Gunn in 1963. Its main characteristics are (see Fig. 2.4):

- The total electric field across the device at any time is above the threshold value.
- The current waveform consists of narrow spikes, indicating a high harmonic content and low efficiency at fundamental frequency.
- The RF field across the device is small, indicating low impedance.
- The transit time frequency is a strong function of operating voltage and temperature.

Therefore the transit time mode has poor stability and efficiency.

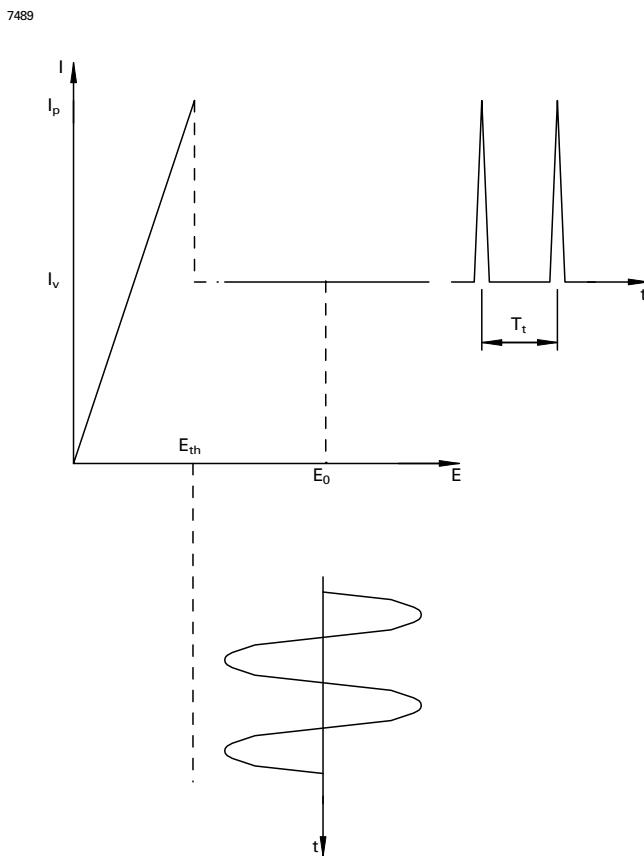


Fig. 2.4 Current and Field Waveforms for Transit Time Mode

2.2.2 Delayed Domain Mode

Fig. 2.5 shows the basic voltage and current waveforms for this mode of operation. Unlike the transit time mode, the total electric field across the device drops below the threshold value, E_{th} , during part of the RF cycle, such that nucleation of a new domain is delayed.

As soon as the field rises above E_{th} , a domain nucleates at the cathode and travels across the device. As the field swings below E_{th} , the domain arrives at the anode and decays its charge. A new domain cannot form at the cathode until the field rises above E_{th} again. This delay time between extinction and creation of domains modifies the operating frequency, f_d , to:

$$f_d = 1/(T_t + T_d)$$

where T_t = transit time

T_d = delay time

The transit time is a fixed quantity for a given device, but the delay time is a function of the RF voltage, which is determined by an external circuit. It follows that the operating frequency is always below the transit time frequency.

The important characteristics of this mode of operation are:

- The total electric field across the device is below the threshold field, E_{th} , over a part of the RF cycle.
- The current waveform consists of broad spikes, indicating a low harmonic content and higher efficiency at fundamental frequency.
- The RF field across the device is large, indicating high impedance.
- The operating frequency is determined mainly by the resonant frequency of the external circuit and can be made very stable. A device can also be used over a much broader bandwidth below the transit time frequency.

This mode of operation is therefore most commonly used in the majority of commercial applications.

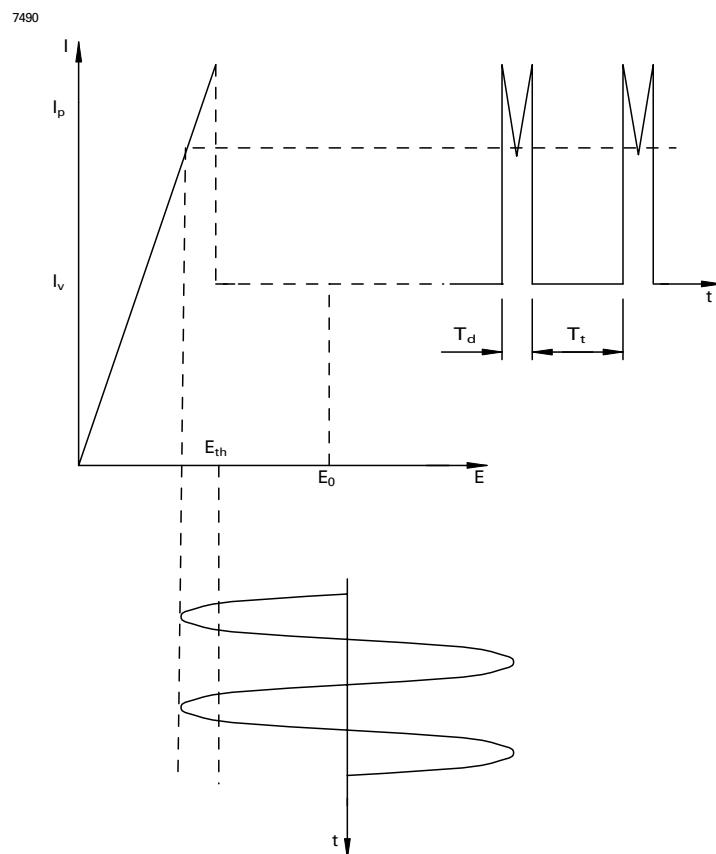


Fig. 2.5 Current and Field Waveforms for Delayed Domain Mode

2.3 Conventional Gunn Diode

A conventional Gunn diode generally consists of three layers; a relatively low doped transit region sandwiched between two highly doped contact regions, forming an n^{++} - n^- n^+ structure (see Fig. 2.6). The device is defined basically by five parameters:

- n The doping concentration in the transit region of the Gallium Arsenide.
- I The thickness of the transit region.
- R_0 The low field resistance of the diode measured close to the origin.
- I_{th} Threshold current. This is the maximum current through the device and can exceed the operating current by as much as 50%.
- NB. The power supply must be capable of passing through this point.
- V_{th} Threshold voltage. The voltage at the current maximum.

The ratio $-R_G / R_0$ is an important circuit design parameter. V_{th} and I_{th} are independent of the external circuit and may be measured with the diode in any good heat sink. Because V_{th} is measured on the flat part of the curve, the measuring technique must be carefully specified to avoid error.

The frequency of the Gunn diode is determined primarily by the transit region length, I. However, a portion of this region is used to accelerate the electrons from the cathode until they have sufficient energy to enter the low mobility state and does not support domain formation. This 'dead zone' may be as much as $0.25 \mu\text{m}$ in a transit region length of $1.5 \mu\text{m}$ (for a millimetric diode) and, because it acts as a parasitic resistance, results in reduced efficiency. For conventional Gunn diodes there is a rapid fall-off in power at frequencies above 60 GHz, where the less efficient second harmonic component of the power has to be utilised.

The starting voltage must be well below the required operating voltage (typically $V_{op} = 3 \times V_{th}$), particularly when low temperature operation is required, as the starting voltage rises with falling temperature. This can be controlled to some extent by the correct choice of n and I, but severely restricts the use of conventional Gunn diodes at temperatures below about -25°C . The turn-on voltage, V_{on} (the voltage above threshold at which coherent RF power is obtained), increases to the point where it equals the peak power voltage V_{pk} (see Fig. 2.7a). This forces the diode to be operated at a higher voltage with corresponding loss in power, reduced efficiency, poor FM sideband noise and the increased possibility of device failure.

2.4 Graded-gap Gunn Diode

The limitations of the conventional Gunn diode (described earlier) can be overcome by injecting high energy, 'hot electrons', into the transit region. The concept is to introduce electrons into a region so that the temperature, which describes their energy distribution, is much greater than that of the semiconductor lattice. In the graded-gap Gunn diode, electrons are injected into the transit region with an energy equal to that of the Γ -L intervalley separation so that stable domains will form very near to the cathode and move across the transit region as soon as the field is high enough to sustain accumulation and propagation. The dead zone is effectively eliminated and the transit length is fixed and independent of bias. Therefore, coherent power can be generated over a wide range of operating voltages (see Fig. 2.7b).

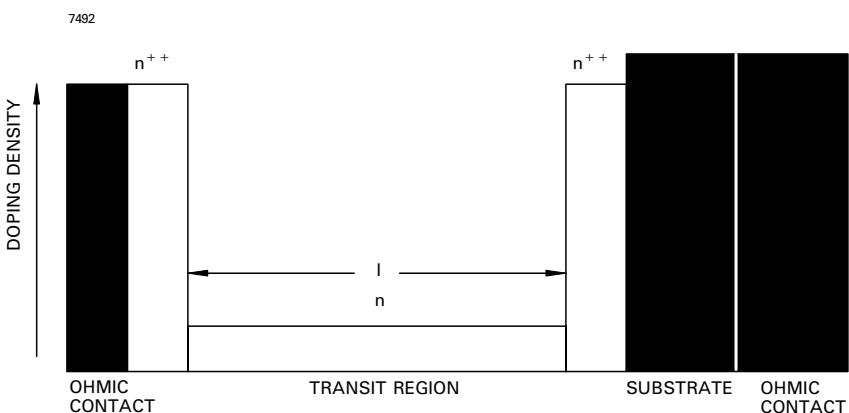
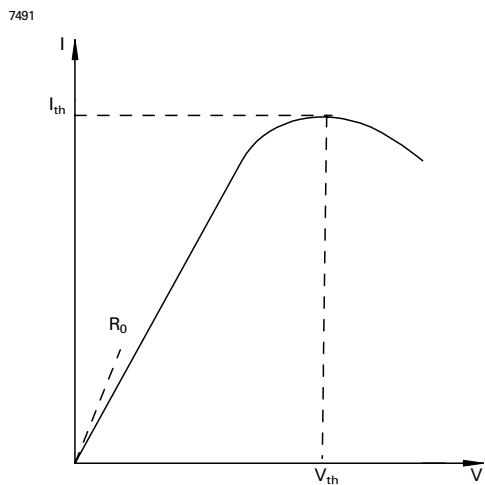


Fig. 2.6 Structural Schematic and Current-Voltage Relationship for a Conventional Gunn Diode

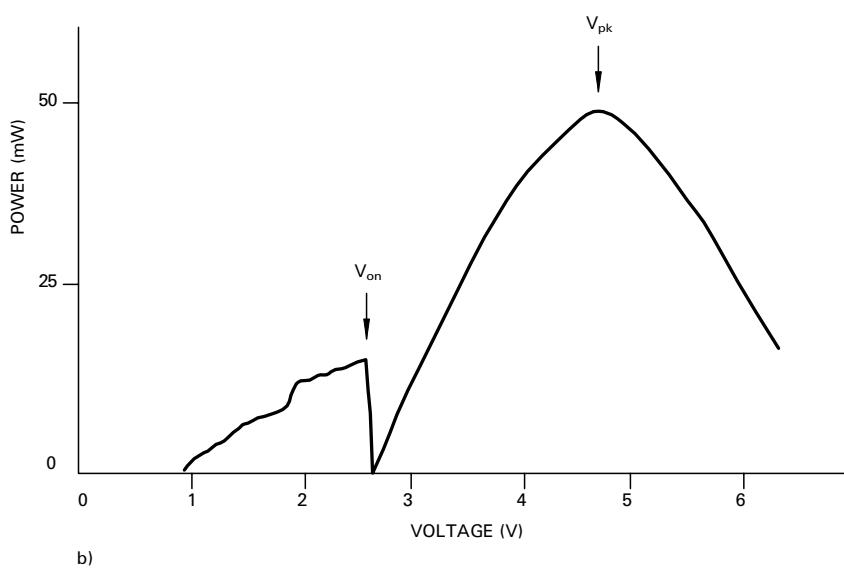
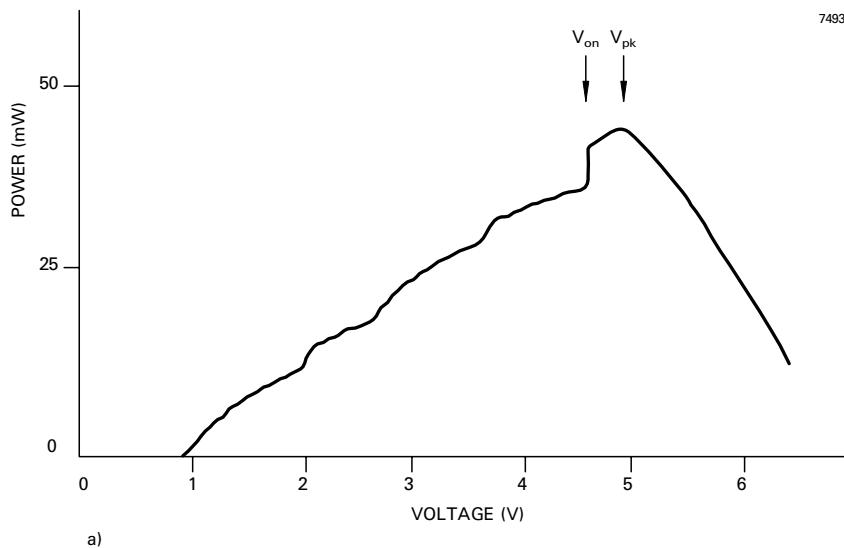


Fig. 2.7 Typical Turn-on Characteristic of: a) Conventional Gunn Diode and b) Graded-gap Gunn Diode

There are a variety of possible structures which can be used for hot electron injection. To produce microwave power with as little bias dependence as possible, the optimum injector shape has a slowly increasing potential with an abrupt drop back to the transit region value. This is best realised with a graded-gap injector (see Fig. 2.8). Simulations have shown that a thin n^+ layer between the injector and the transit region is critical for controlling the electric field, while retaining the hot electron properties. Fig. 2.8b shows the n^+ spike depleted giving an injection energy of ΔE .

An additional benefit from using a graded-gap Gunn diode is the much improved temperature stability. This is due to the electron temperature being set by the injection energy, typically equivalent to 2000 K. Changes in the substrate temperature in the 130 °C range usually required for military specifications, etc, are relatively small in comparison.

The structural schematic and current-voltage relationship for a graded-gap Gunn diode are shown in Fig. 2.9. Under forward bias, the peak current is much less defined due to the action of the cathode injector (i.e. significant numbers of electrons already reside in the upper valley when entering the transit region) and the gradient of the curve beyond threshold is shallower.

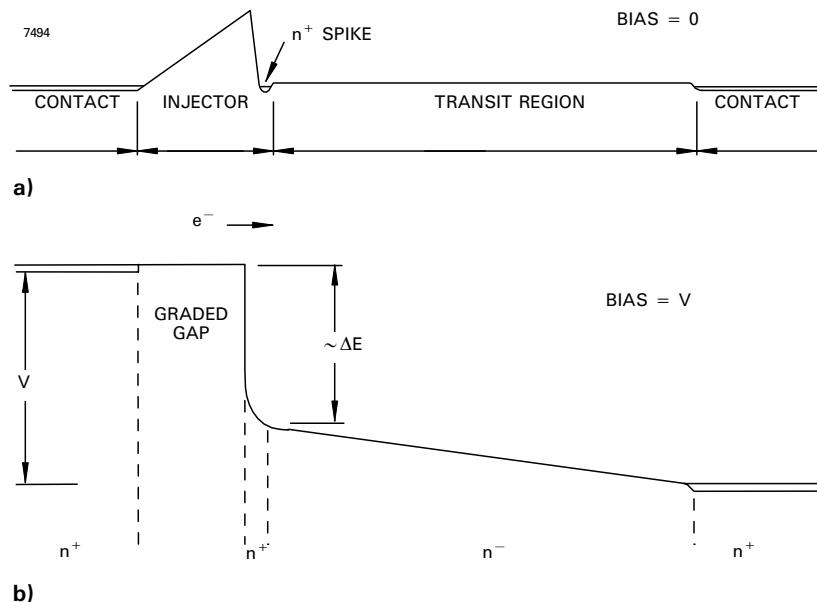


Fig. 2.8 A Schematic Diagram of a Hot Electron Injector Gunn Diode under a) Zero Bias, and b) Forward Bias *V*.

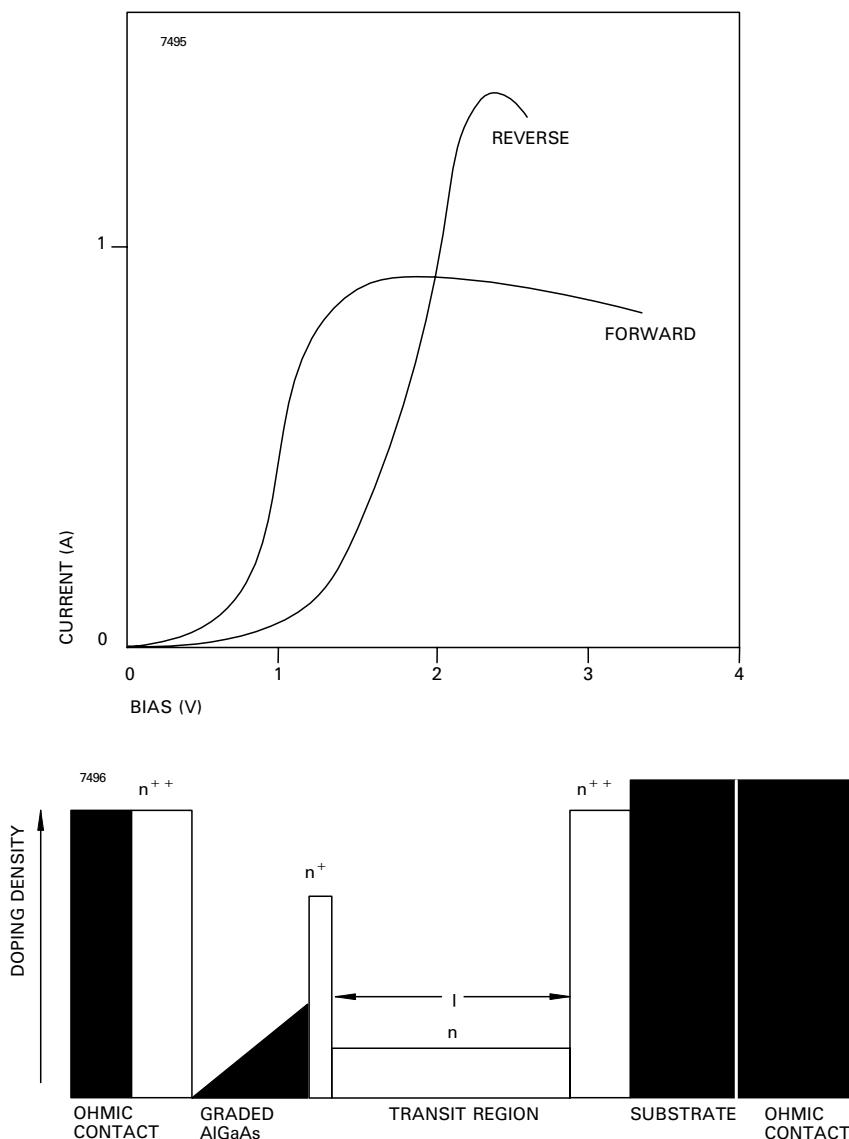


Fig. 2.9 Structural Schematic and Current-Voltage Relationship for a Graded-gap Gunn Diode

Graded-gap Gunn diodes have demonstrated room temperature performance of up to 80 mW and 2.4% efficiency at 90 GHz; the best results achieved for mm-wave GaAs devices at this frequency. 50 - 60 mW at 94 GHz, with efficiencies of 1.6%, is reproducibly achieved (see Table 2.1). FM sideband noise is better than -80 dBc/Hz, 100 kHz from carrier, equal to that obtained from the best conventional devices. Significantly these devices exhibit a turn-on voltage very close to threshold (see Figure 2.7b), which allows coherent oscillations around peak power over the full military specification temperature range. Further evidence of the improved temperature stability can be seen from the power, frequency and peak power variations across this temperature range, generally a factor of two or more below that exhibited by devices without hot electron injection. This is an added bonus for VCO designers who can then utilise a larger bandwidth, because there is no longer need to compensate for frequency drift with temperature.

Freq (GHz)	Temp (°C)	V_{on} (V)	V_{op} (V)	I_{op} (mA)	Power (mW)	Eff (%)	Noise * (dBc/Hz)
90	-40	3.9	4.9	680	58	1.75	
90	+25	3.2	4.7	660	50	1.6	-86
90	+80	3.1	4.8	640	42	1.4	
94	+25	3.0	4.5	600	60	2.0	-88
60	+25	3.0	4.5	600	120	5.0	-90
35	+25	3.0	4.5	1300	350	5.5	-95

* 100kHz offset frequency

Table 2.1 Typical Performance of Graded-gap GaAs Gunn Diodes

3 APPLICATIONS

Gunn diodes are reliable, relatively easy to install and the lower output power levels fall well below the safety exposure limits. They are ideally suited for use in low noise sources such as local oscillators, locking oscillators, low and medium power transmitter applications and motion detection systems. Higher power varieties can be used in phase-locked oscillators or as reflection amplifiers in point-to-point communication links and telemetry systems.

Microwave sources have the advantages over ultrasonic detectors of size and beamwidth, and over optical systems of working in dusty and adverse environments. The low voltage requirements of Gunn oscillators mean that battery or regulated mains supplies may be used, (battery drain can be reduced by using low current devices or by operation in a pulsed mode). However, microwaves are reflected from metal surfaces and partially reflected from many others e.g. brick, Tarmac and concrete, and they are attenuated by oxygen, water or water vapour. Figure 3.1 shows attenuation effects in the frequency range of interest.

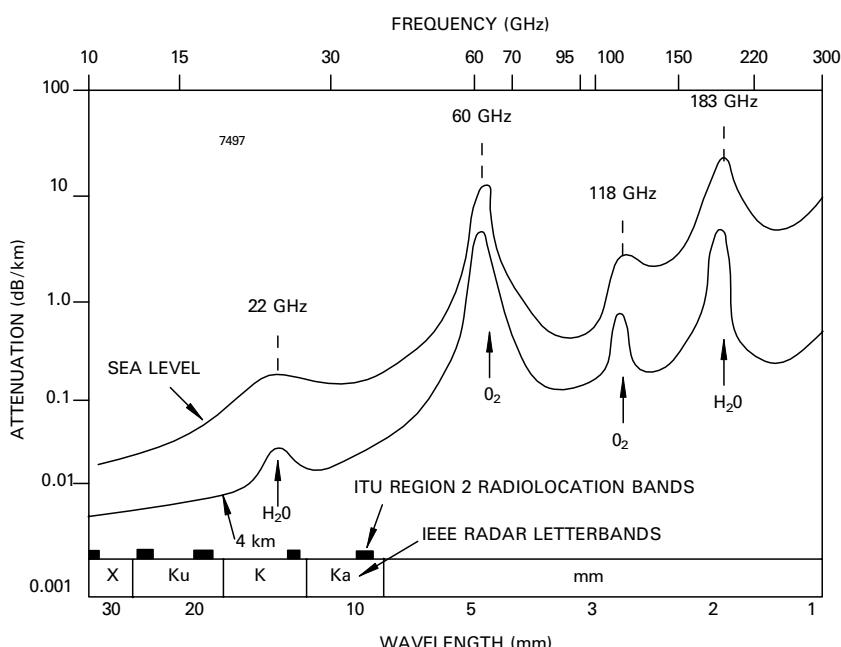


Fig. 3.1 Atmospheric attenuation at millimetre wavelengths with IEEE radar letterbands and ITU radiolocation bands for region 2 (after Altshuler *et al*)

The range of application of Gunn sensors for industrial and commercial use is extensive and the following is only a brief list:

- Collision avoidance radar
- Vehicle ABS
- Traffic analyser sensors
- 'Blind spot' car radar
- Pedestrian safety systems
- Elapsed distance meters
- Automatic identification
- Presence/absence indicators
- Movement sensors
- Distance measurements
- Slow-speed sensors
- Level sensors

- Traffic signal actuators
- Proximity movement detectors
- Door opening sensors
- Barrier operation
- Process control devices (object counting)
- Intruder/burglar alarms
- Perimeter protection
- Train derailment sensors
- Contactless vibration transducers
- Rotational speed tachometers
- Linear distance indicators
- Moisture content measurement

Table 3.1 indicates the most commonly used Gunn diode types by application.

APPLICATION	Fixed Frequency CW			Broadband CW	Pulsed		
	Low Power	High Power					
		Low Frequency	High Frequency				
Local Oscillators: Radar Fast tunable ECM Diode noise measurement		●		●			
Telecommunications: Transmitters Low noise oscillators Point-to-point links		● ●	●				
Control devices: Railway crossings Traffic control Vehicle ABS Door openers	● ● ● ●				●		
Motion detectors: Speed control Radar detectors Intruder alarms Shoreline navigation	● ● ● ●				●		
Transmitters: Radar transponders Missile beacons					● ●		
Radio link excitors		●					
Injection locked amplifiers		●					
Paramp pump sources			●				
Instrumentation				●			

Table 3.1 Gunn Diode Selection Chart

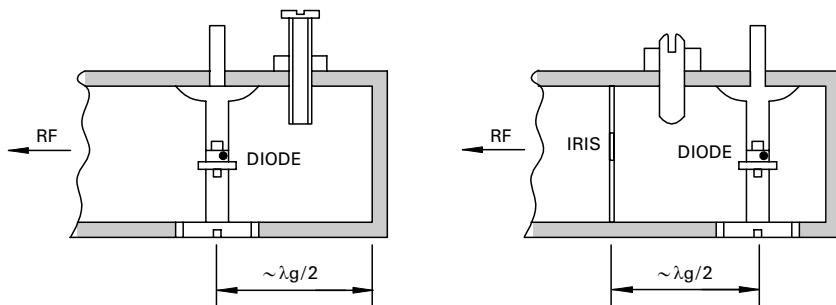


Fig. 3.2 Basic Microwave Cavity Design

3.1 Oscillator Design

The natural frequency of oscillation of the Gunn diode can be altered to some extent by the external circuit. The formation or premature collapse of a domain within a cycle can be controlled, and hence the power, frequency and efficiency adjusted. Control of the frequency by external means rather than by device parameters only is essential for a stable oscillator. The external cavity used to resonate the device negative impedance can be coaxial, waveguide, microstrip, YIG crystal, etc, depending on the required application.

Generally, coaxial and microstrip circuits offer low Q values with poor noise and stability performance, resulting in the frequency of oscillation changing with load and environmental variations. YIG crystal tuned circuits are usually too expensive for commercial and industrial applications and therefore the most common cavity is waveguide. Usually the Gunn diode is mounted on a post structure between the waveguide walls, either $\lambda g/2$ from an iris or $\lambda g/2$ from a short circuit (see Fig. 3.2). Some alteration is necessary to set the exact frequency to allow for diode and package parasitics and manufacturing tolerances. Tuning screws of either metal or dielectric are used to modify the cavity resonant frequency. Power output variations are achieved by adjusting the coupling between diode and load using variations in post size or tuning screws. A more detailed schematic of a packaged Gunn diode mounted in a radial disc, microwave cavity and its equivalent circuit diagram are given in Figs. 3.3 and 3.4.

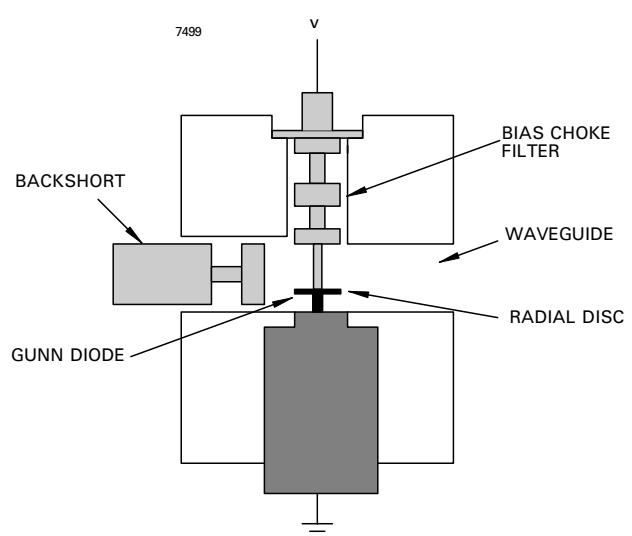


Fig. 3.3 The Packaged Gunn Diode Mounted in a Microwave Cavity (approximately half scale).

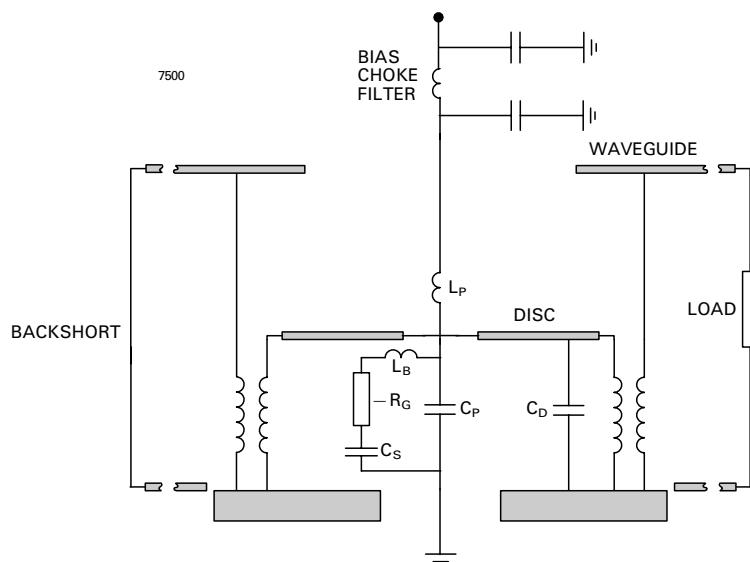


Fig. 3.4 An Equivalent Circuit Diagram for the Gunn Diode, Package, Disc and Cavity

Most simple Gunn oscillators are designed empirically using a few ground rules and a lot of experience. The designs have to tolerate batch to batch variations in diode parameters and have the required stability. They must not present the diode with an RF impedance such that the device takes DC power but produces no RF output, thus leading to a possible turn-on or switch-on failure.

A recommended Gunn diode driver circuit is shown in Fig. 3.5

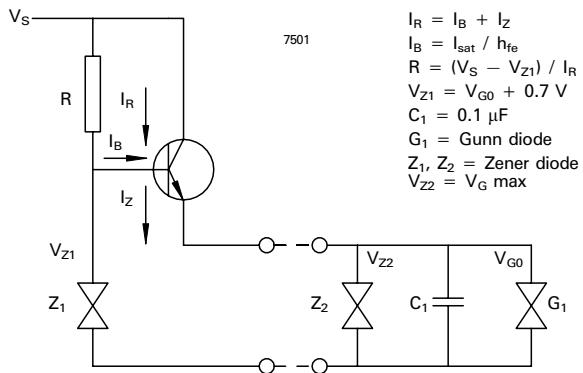


Fig. 3.5 A Recommended Gunn Diode Drive Circuit

3.2 Performance Considerations

3.2.1 Matching

The Gunn diode is a current generator and needs matching into the circuit for optimum output power, noise, smooth tuning and power-temperature variation. Small differences may exist even between cavities which are nominally identical. Testing in the customer's own cavity design is always the preferred solution.

The impedance matching problem becomes increasingly critical as the cavity Q goes up. The impedance of the diode is determined to the first order by the thickness, doping and operating voltage. However, second order trimming can be obtained by varying the voltage to alter the domain width, and therefore the domain capacitance, by field control. The voltage at which maximum power is obtained is cavity dependent. If the diode is not well matched to the cavity, there may be a conflict between the voltage for correct match and the voltage at which the diode would want to operate in a low Q cavity. Trimming the diode parameters, therefore, becomes more critical as Q increases and the tolerances on device specifications become correspondingly tighter. It follows that it is more difficult to design a diode to work in a high Q cavity without having access to the cavity.

3.2.2 Starting Voltage

The conventional Gunn diode is a broadband negative resistance device and random noise is required to start it. Starting becomes more difficult at low temperature and in high Q cavities. High Q operation also means higher voltage operation for reliable starting. These limitations can be overcome (at higher frequencies) by the use of a graded-gap, current injected Gunn diode.

3.2.3 Operating Current

Increasing the operating current increases the output power. However, the maximum safe operating current for an encapsulated device is limited by the corresponding increase in the transit region temperature ($\lesssim 250^\circ\text{C}$). This, in turn, is determined by the thermal resistance of the diode itself and by the effectiveness of the package heat sink (see Section 3.3). The lower limit of current is more difficult to define because the series resistance of the ohmic contact increases non-linearly as the diode area decreases.

3.2.4 Output Power

The output power is determined primarily by the diode area and the doping level. The highest power/efficiency is achieved using an integral heat sink (IHS) construction. This has the advantage of a thick, gold plated heat sink formed directly onto the epitaxial region and a minimal thickness of remaining substrate, thereby reducing the parasitic resistance. Further improvement in output power can be obtained at higher frequencies by the use of a graded-gap, current injected Gunn diode.

The upper limit on power handling is mainly determined by the dissipation of DC power through the package heat sink and the fact that the diode impedance becomes low and is difficult to match.

3.2.5 FM Noise and dF/dT

FM noise measurements are given as noise to carrier ratios (N/C) versus carrier offset modulation frequency, f_m . The frequency deviation, Δf , is calculated from:

$$N/C = 20 \log (\Delta f \sqrt{2} / f_m)$$

where values of (N/C) are given in dBc/Hz.

In the graded-gap Gunn diode, the variation in position at which domain formation occurs is much less than in a conventional device. Associated with this is a reduction in the variance of the first intervalley scattering effect for electrons entering the cathode region and hence a reduction in noise.

The factors controlling FM noise and the frequency-temperature coefficient are complex and are resolved by work involving both the diode and oscillator design. The equivalent circuit of both the diode and the cavity form a total circuit concept and there is a trade-off between the parameters in each component. Oscillators and diodes need to be designed together to achieve given second order aspects of the specification.

Second order effects such as noise, chirp, dF/dT , etc., bear no direct relationship to the primary characteristics of frequency and power. The secondary parameters can show wide variation between diodes, which in all other primary respects are identical.

3.2.6 Pulse Diodes

These diodes are even more cavity dependent than CW diodes. Whereas a conventional CW diode requires as low a series resistance as possible, this is not true in pulse diodes. The constant re-nucleation of domains at the start of each pulse requires closer control of the electric field at the cathode. Various methods of achieving this are available, including adding series resistance with a disc or by partially alloying the contacts to provide some non-ohmic behaviour. Alternatively, a graded-gap, current injected Gunn device may be used.

Frequency change during the pulse (chirp) is also affected by these measures as is the dF/dT with which it correlates.

Pulse diode noise is normally defined as the degradation in the Fourier sin(x)/x display of the RF power pulse from the ideal rectangular pulse values. The factors that control pulse noise and chirp are complex and the solution in any particular case is arrived at by modifications both to the diode processing and oscillator design.

3.2.7 Special Operating Conditions

In all cases where the optimum unique frequency and power design parameters have to be modified to achieve some special condition of low or high temperature operation, restricted voltage or current consumption, or broadband tuning, then some loss of optimum performance results. There is always a trade-off to be made to meet a special operating condition.

3.2.8 Low Harmonic Diodes

Diodes can be designed to meet low harmonic generation limits (if required by local regulations) by modifying the material specification. The extent to which the harmonics can be reduced, however, is limited by the cavity design and depends on the measurement technique.

3.2.9 Broadband Operation

Diodes can be specially designed by modifying the material properties and controlling the encapsulation parasitics to give a broadband tuning performance in a carefully defined cavity. This is achieved at the expense of output power and efficiency.

3.2.10 High Temperature Operation

E2V Technologies' standard range of Gunn diodes can be used up to heat sink temperatures of 85 °C. At higher temperatures it is necessary to reduce the transit region doping level in order to ensure long life. This means that for the same current flowing through the device a larger die is used and greater cooling is achieved by the increased area of contact with the heat sink and the larger surface area for radiation. This affects other properties of the diode and may require further modifications to be made to the specification.

3.3 Mounting and Heat Sink Considerations

The increase in temperature between the diode heat sink and the semiconductor transit region is defined by:

$$\Delta T = R_\theta (P_{in} - P_{out})$$

The thermal drop between the ambient and the diode heat sink must also be taken into account to avoid exceeding the maximum transit region temperature of ~250 °C. The transit region temperature may be computed as follows:

$$T_{tr} = T_{amb} + \Delta T_{case} + \Delta T$$

$$= T_{amb} + \Delta T_{case} + R_\theta (P_{in} - P_{out})$$

where: T_{tr} = transit region temperature (≤ 250 °C).

T_{amb} = ambient temperature.

ΔT_{case} = temperature difference between the diode heat sink and ambient at the operating power.

R_θ = diode thermal resistance.

In well designed packages, the temperature difference, ΔT_{case} , is usually less than 30 °C for an input power of about 15 W.

4 PERFORMANCE CHARACTERISTICS

4.1 Limiting Conditions of Use

Temperature:

operating (for standard types) −40 to +85 °C

storage −55 to +150 °C

Operating voltage each type is individually rated.

Application of a bias voltage in excess of this value may lead to degradation in performance.

4.2 Typical Performance Curves

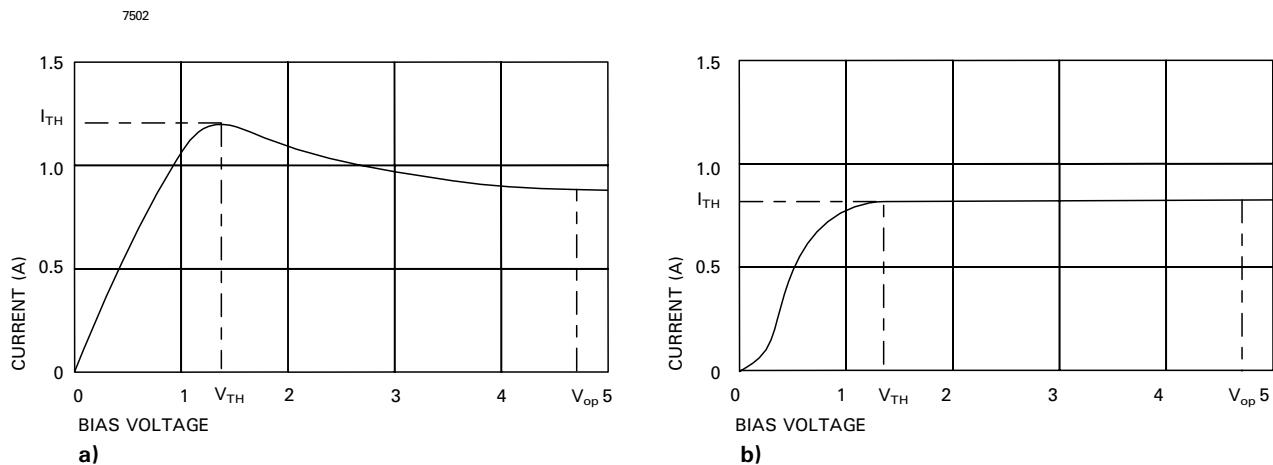


Fig. 4.1 Typical DC Characteristic a) Standard Gunn Diode, b) Graded-gap Gunn Diode

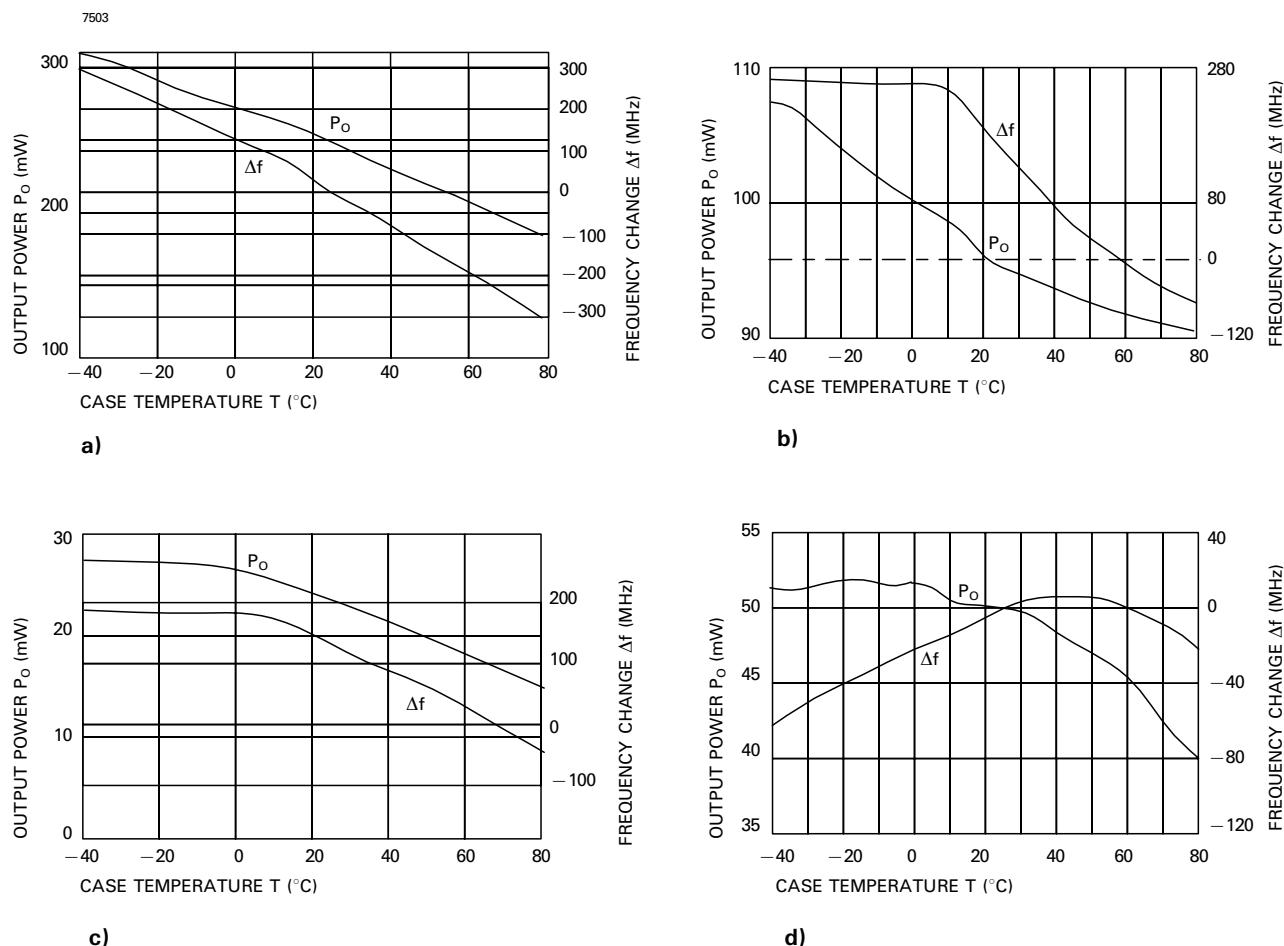


Fig. 4.2 Variation of Power and Frequency with Temperature for:
 a) DC1276H operating in the fundamental mode;
 b) DC1277G-T operating in the fundamental mode;
 c) DC1279D operating in the second harmonic mode;
 d) DC1279F-T operating in the second harmonic mode

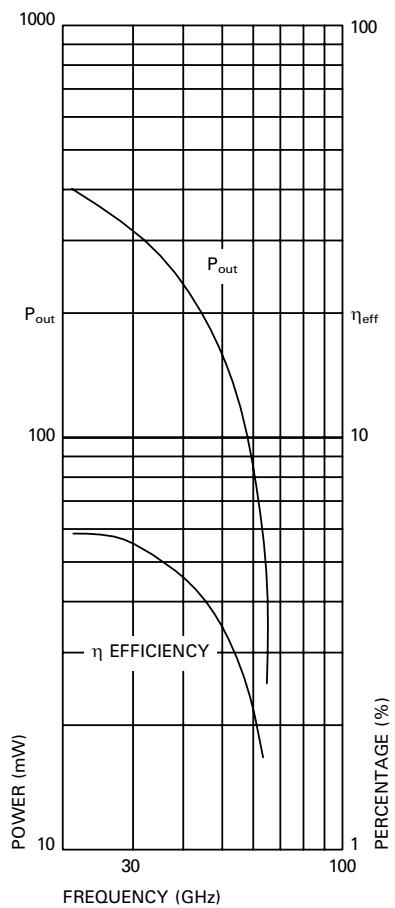


Fig. 4.3 Variation of power and frequency with temperature for DC1276 and DC1277 series.

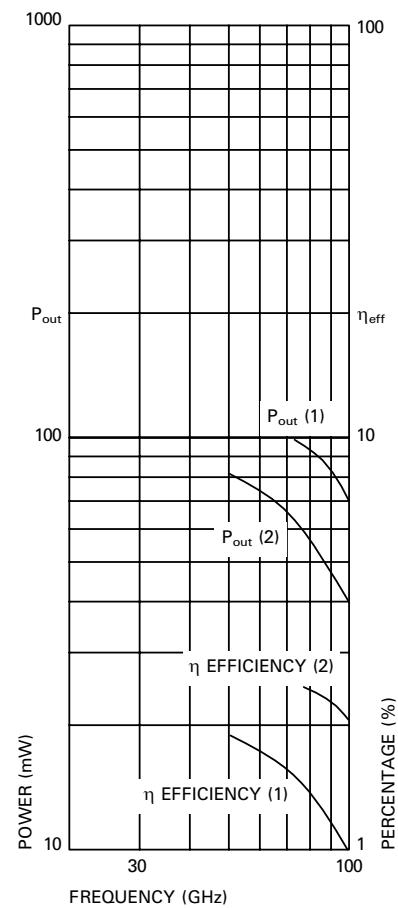


Fig. 4.4 Variation of power and efficiency for: 1) DC1278 and DC1279 series; 2) DC1279F-T series

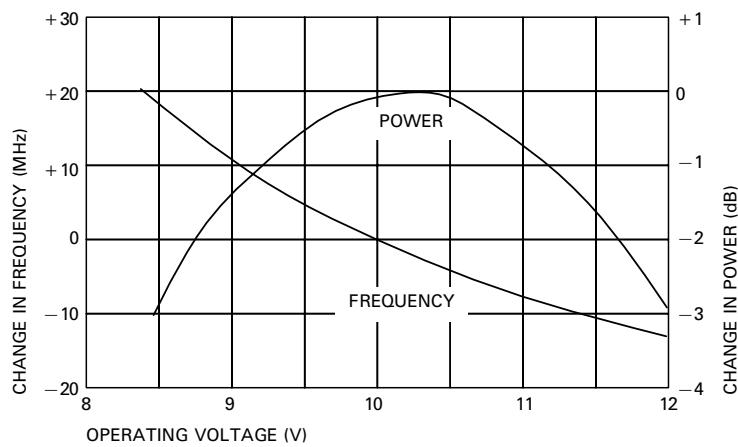


Fig. 4.5 Variation of output power and frequency with operating voltage

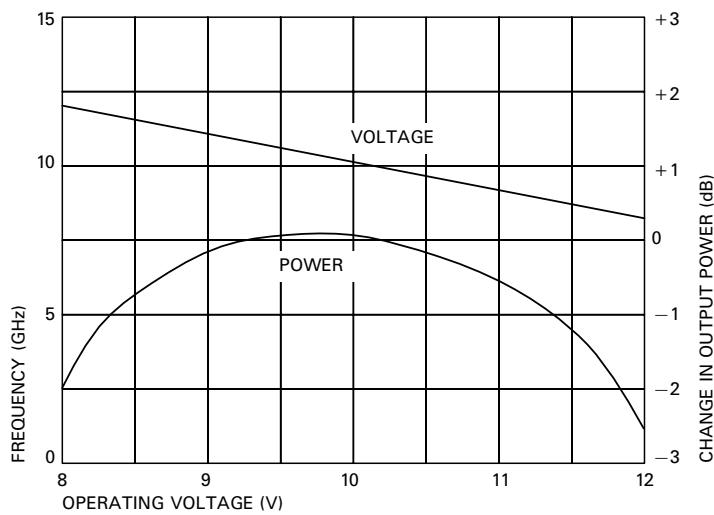


Fig. 4.6 Effect of voltage tracking on the variation of output power with frequency on a wideband tunable waveguide oscillator.

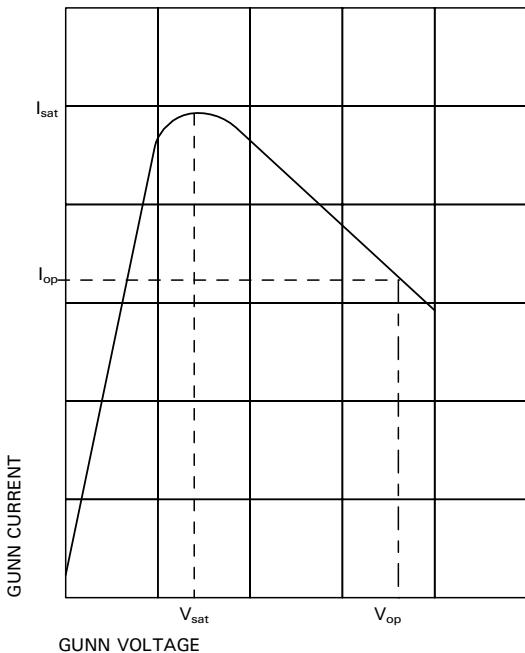


Fig. 4.7 DC Gunn characteristics

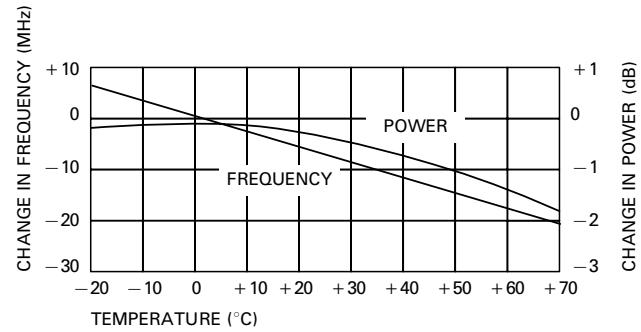


Fig. 4.8 Variation of frequency and power with temperature.

5 BIBLIOGRAPHY

Microwave Oscillation of Current in III-V Semiconductors.

Gunn J.B.

Solid State Commun., 1, 88 (1963).

Theory of the Gunn Effect.

Kroemer H.

Proc. IEEE, 52, 1736 (1964).

The Gunn Effect.

Hobson G.S.

Clarendon, Oxford, 1974.

Theory of Stable Domain Propagation in the Gunn Effect.

Butcher P.N.

Phys. Lett., 19, 546 (1965).

Transferred Electron Amplifiers and Oscillators for Microwave Application.

Sterzer F.

Proc. IEEE, 59, 1155 (1971).

Hot Electron Microwave Generators.

Carroll J.E.

Arnold, 1970.

Fundamental Mode graded-gap Gunn Diode Operation at 77 and 84 GHz.

Dale I., Stephens J.R.P., Bird J.

Conf. Proc. Microwaves '94, .

Advances in Hot Electron Injector Gunn diodes.

Spooner H., Couch N.R.

GEC J. of Res., 7, 34 (1989).

Hot Electron Injection by Graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$.

Long A.P., Beton P.H., Kelly M.J., Kerr T.M.

Electronics Letters, 22, 130 (1986).

Hot Electron Injection : Concept to Product.

Couch N.R., Kelly M.J.

Physics World, 2, 37 (1989).

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APPENDIX II-2

TRANSISTOR GUIDE

Performance Guides Transistor Selection

Jack Browne

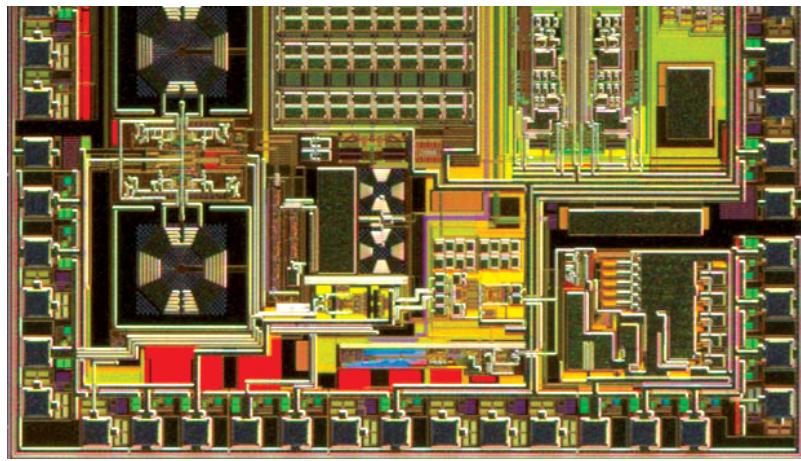
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With such a large number of RF/microwave transistor technologies currently available, basic requirements like output power at a given frequency can speed the selection process.

Transistors for RF/microwave applications are based on several different elements and compounds, with each substrate material bringing its own strengths and weaknesses. Not long ago, the choice for a microwave transistor was essentially between silicon and gallium arsenide (GaAs). But the last few decades have seen the emergence and growth of additional high-frequency semiconductor substrates, including indium phosphide (InP); silicon carbide (SiC); silicon germanium (SiGe); gallium nitride (GaN); and even combinations of the materials, such as GaN on SiC. Transistors fabricated on these semiconductor materials offer a wide range of performance capabilities, from low noise figures to high output powers, from the high-frequency (HF) range through millimeter-wave frequencies.

The comparison of silicon bipolar-junction-transistor (BJT) devices to GaAs transistors, such as metal-epitaxial-semiconductor field-effect transistors (MESFETs), has long been simply the differentiation of the two technologies' operating frequency ranges. In addition to using different substrate materials, silicon bipolar transistors and GaAs MESFETs differ in structure, although both are three-terminal semiconductor devices. The terminals in a silicon bipolar transistor are the base, collector, and emitter; a small current at the base terminal can switch or control a much larger current between the collector and emitter terminals.

Bipolar transistors are formed of two junction diodes on semiconductor material with two polarities. These transistors are fabricated on positive (p) and negative (n) layers of semiconductor material: either a positive layer between two negative layers (an npn transistor) or a negative layer between two positive layers (a pnp transistor). Bipolar transistors conduct both majority and minority carriers.



1. This highly integrated circuit demonstrates the silicon CMOS heritage of this SiGe device technology. (Photo courtesy of [IBM](#).)

In contrast, an FET's terminals are the gate, source, and drain—a voltage at the gate can control a current between source and drain. A FET is also known as a unipolar transistor because it uses only one form of conductor, electrons, or holes. Current flows from the drain to the source, with the conductivity varied by the electric field that is produced when a voltage is applied between the gate and source terminals. The current that flows between the drain

and the source is controlled by the voltage between the gate and the source. FETs, in both silicon and GaAs forms, can be used as switches (as they often function in digital circuits or power supplies) or as amplifiers (providing gain to a circuit).

Silicon metal-oxide-semiconductor FETs (MOSFETs) are capable of high power-handling capabilities at lower (such as audio) frequencies and in switching power supplies. GaAs FETs—although not capable of the high power levels of silicon MOSFETs—can operate through microwave and millimeter-wave frequencies, typically in solid-state low-noise or power amplifiers. FETs can provide current gain, voltage gain, or both.

In addition to serving for many years as the substrate of choice for many high-power silicon bipolar transistors at sub-microwave frequencies, silicon has also been the basis for many high-frequency CMOS integrated-circuit (IC) devices. When fabricated with sufficiently small dimensions, such as with 90-nm processes, silicon CMOS transistors are capable of low-power, high-gain operation at frequencies to 60 GHz and beyond. While such devices have long been associated with digital and computer applications, their low cost and capabilities for millimeter-wave operation make them attractive candidates for use in higher-frequency consumer applications. These include point-to-point backhaul radios at 60 GHz and automotive radar systems at 77 GHz.

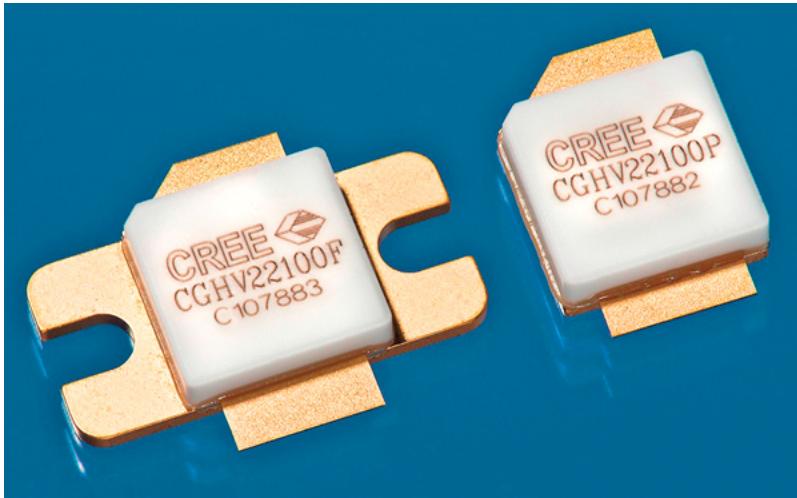
As part of efforts to develop higher-frequency, higher-power transistors, silicon has also worked with other elements as part of compound materials substrates, including silicon germanium (SiGe) and silicon carbide (SiC). SiGe substrates have held great promise for higher-frequency applications while silicon-carbide (SiC) materials offer much potential for higher power levels, whether as the main semiconductor substrate or as a base for other types of semiconductors.

[IBM](#) has done a great deal of work on high-frequency SiGe BiCMOS devices, offering foundry services for customers needing high-frequency analog and mixed-signal ICs. IBM's SiGe technology is based on 130-nm silicon CMOS foundations, and is suitable for applications at 60 GHz and higher frequencies (**Fig. 1**). The firm offers what are known as “multi-project wafers,” with a number of different customers having their designs fabricated on the same wafer so that one customer is not required to field the expenses for an entire process run (for more, [click here](#)).

Last year, [Renesas Electronics](#) announced its work using a blend of SiGe and carbon, resulting in its model NESG7030Mo4 SiGe:C heterojunction bipolar transistor (HBT) for low-noise applications. Developed for 5-GHz wireless-local-area-network (WLAN) applications, this transistor features a noise figure of only 0.75 dB with about 14-dB gain in the 5.8-GHz band. This performance represents a significant improvement in noise-figure performance over the company's earlier SiGe HBT devices. The firm explains that the addition of carbon has made it possible to optimize the device's collector-base profile, increasing the range of supply voltages that can be used.

In terms of SiC, these discrete devices and modules are capable of high-voltage, high-power operation through lower microwave frequencies. An early developer of the technology, [Cree](#), offers SiC MOSFET die and packaged devices at voltages to 1200 V, such as the low-frequency model CMF10120D. Suitable for motor drives and switched-mode power supplies, it draws 24 A at +1200 VDC.

Over a decade ago, the firm introduced its model CRF-22010, a SiC MESFET capable of 10 W output power and 12-dB gain at 2.2 GHz. The Class A linear transistor is designed for a +48-VDC supply. But the company is also heavily involved in GaN device development, recently introducing 50-V GaN HEMTs for commercial cellular communications applications, including model CGHV22100 with 100 W output power from 1800 to 2200 MHz for Long-Term-Evolution (LTE) cellular base stations. The GaN HEMT (**Fig. 2**) features 20-dB gain with as much as 35% power-added efficiency across its frequency range.



2. These packaged 50-V GaN HEMTs are capable of 100 W output power from 1800 to 2200 MHz for use in cellular communications networks. (Photo courtesy of [Cree](#).)

Many companies are finding the electrical capabilities of GaN and the thermal capabilities of SiC to be a powerful combination, fabricating GaN-on-SiC transistors with excellent high-power, high-frequency capabilities. The model T1G4005528-FS transistor from [TriQuint Semiconductor](#) is a discrete GaN-on-SiC HEMT that is usable from DC to 3.5 GHz. It provides 15-dB linear gain at 3.5 GHz with 55-W output power at that frequency when operating from a +28-VDC supply. It is built with the firm's 0.25- μ m production GaN process and supplied in a metal-ceramic flange package. It is suitable for commercial and military applications in radios, radar, and avionics systems. The company's highest-power discrete GaN-on-SiC HEMT is model TGF2023-20, with 100 W output power from DC to 18 GHz. It offers maximum power-added efficiency of 52%, with 17.5-dB power gain at 3 GHz.

Just what kind of output-power levels are in store for GaN devices? Military organizations such as [DARPA](#) foresee GaN amplifiers as compact solid-state replacements for vacuum-tube electronics in radar systems. As an example, the [Beverly Microwave Division of Communications and Power Industries](#) developed their model VSS3607 GaN amplifier for S-band radar transmitters. It yields 1.3 W saturated output power from 2.7 to 2.9 GHz when operating with pulse widths from 1 to 100 μ s at 10% duty cycle. The GaN amplifier draws 13 A at +30.5 VDC and provides 62-dB small-signal gain. It measures 9.5 x 15.5 x 1.75 in. and weighs 11 lbs. When 12 of these units are power combined as the model VSS3605 amplifier, however, they achieve 13 kW output power from 2.7 to 2.9 GHz with 71-dB small-signal gain. Of course, with so many amplifiers, the package size is somewhat larger, at 19.0 x 25.5 x 23.5 in. and 230 lbs.

Researchers pursuing higher-frequency uses for semiconductor devices have considered the various types of transistors and semiconductor devices used for microwave and millimeter-wave applications; they have generally compared GaAs versus GaN devices, or even InP devices. [Last year, NASA's [Jet Propulsion Laboratory \(JPL\)](#) reported InP ICs operating to frequencies as high as 670 GHz.] For example, emerging applications in the terahertz (THz) region, which typically includes frequencies just below the infrared region, from 100 GHz to 10 THz, show a great deal of promise for imaging radar, and broadband communications systems.

The thermal conductivity of GaN is much higher than that of GaAs, about 170 W/m-K for GaN versus about 50 W/m-K for GaAs, which allows for much higher power levels for GaN devices compared to GaAs transistors. GaN also offers more than twice the bandgap energy of InP and GaAs. Quite simply, GaAs and InP transistors are limited in output power at higher frequencies, especially compared to GaN, making GaN an attractive semiconductor material for potential THz applications.

In addition, DARPA has invested in InP device technology for higher frequencies as part of its THz Electronics program. The organization's efforts have resulted in improvements in InP HBTs and HEMTs, making possible a

670-GHz LNA based on InP active devices, as compact, lower-power replacements for vacuum-electronics devices. Major defense contractors, such as [Northrop Grumman](#), have long applied InP HEMT MMIC technology for fabrication of amplifiers and other components operating in the millimeter-wave range, at frequencies past 200 GHz, for passive imaging and other satellite-communications (satcom) applications.

Source URL: <http://mwrf.com/analog-semiconductors/performance-guides-transistor-selection>

APPENDIX II-3

TRANSISTOR TRADEOFFS

From <http://www.microwaves101.com/encyclopedia/MMICsemi.cfm>

GaAs MESFET

Gallium arsenide MESFET was the original answer to "how can we make amplifiers at microwave frequencies?" The first GaAs MMICs demonstrated in the 1970s. Including HEMT and HBT technologies, literally billions of dollars have been spent extending f_{max} of GaAs products up into 100s of GHz.

The semi-insulating properties of GaAs substrates and the 12.9 dielectric constant make it an excellent media for microstrip or CPW design. It operates reliably up to 150C channel temperature. GaAs substrates are available up to six inches (150 mm) in diameter, which has been a long development since the first 2-inch wafers were available in the late 1970s. Sadly, GaAs MESFET MMICs will never be cheaper than silicon, due to the starting material cost (\$100s of dollars). GaAs parts are more fragile than silicon, and the thermal dissipation factor is not that good. GaAs MESFETs may be extinct in five years, because it doesn't cost much more to fabricate PHEMT or MHEMT on GaAs, and these technologies offer higher performance.

Advantages:	Disadvantages
<ul style="list-style-type: none"> • Mature technology • Optical gates (usually) means low cost • Great microwave substrate (ϵ_r of 12.9, low loss tangent, high bulk resistivity) • Six inch wafers available • Photonic properties • 16-20 volt breakdown possible • Relatively cheap to produce (but always more than silicon) • Channel temperatures up to 150C possible 	<ul style="list-style-type: none"> • Limited to Ku-band or lower • Noise figure and power performance not as good as GaAs PHEMT • Positive and negative voltage typically needed (V_{GS} and V_{DS}).

GaAs PHEMT

GaAs PHEMT was the second MMIC technology to be perfected, in the 1990s. Breakdown voltages of PHEMT up to 16 volts make high-power/high efficiency amplifiers possible, and noise figure of tenths of a dB at X-band means great LNAs. PHEMT stands for pseudomorphic high electron mobility transistor. "Pseudomorphic" implies that the semiconductor is not just GaAs (e.g., AlGaAs/InGaAs/GaAs).

Actually, "pseudomorphic" means that the hetero layers are thin enough not to keep their own crystal lattice structure, but assume the structure (lattice constants especially) of surrounding material (lots of stress is involved). If you look at a two dimensional cross section of the layer, you'll see that while it assumes the lattice constant of the bulk structure in the X direction, it tries to keep its original lattice constant in the vertical direction.

This layer is indeed strained. For a GaAs pHEMT, indium is added to improve mobility and form a quantum well. Indium wants to growth the lattice and the typical range for useful thicknesses would be 10-25% on GaAs. You can also do strain compensation with the Schottky or cap layer.

Advantages:	Disadvantages
<ul style="list-style-type: none"> • Useful through Q-band, especially if thinned to 2 mils and individual source vias are used • Excellent power and efficiency (greater than 60% PAE) • Breakdown 12 volts at best, typical operate at 5-6 volts • Channel temperatures up to 150C possible. 	<ul style="list-style-type: none"> • E-beam gates (increases cost) • Positive and negative voltage typically needed (V_{GS} and V_{DS})

GaAs MHEMT

Recent work on metamorphic MHEMT has made premium InP HEMT performance possible (amplifiers up at 100 GHz) at the same price as "regular" GaAs PHEMT. You can get noise figure and f_{max} equal to indium phosphide by using MHEMT, if you use a reputable foundry and indium content is high.

You can actually exceed InP RF performance with indium content greater than 55%! The down side to all that indium is reduced operating voltage.

MHEMT stands for metamorphic high-electron mobility transistor. The channel material is InGaAs. "Metamorphic" implies that the lattice structure of GaAs is buffered using epitaxial layers to gradually transform the lattice constant so it lines up with InGaAs. InGaAs is normally grown on InP, which is expensive and fragile compared to GaAs. "Metamorphic" is changing the lattice constant by bond breaking as opposed to "pseudomorphic".

Advantages:	Disadvantages
<ul style="list-style-type: none"> Extremely low noise figure Incredibly high f_{max} (more than 100 GHz) Extremely low on-resistance, makes great switches, but not as good as PIN diodes. Channel temperatures up to 150C possible. 	<ul style="list-style-type: none"> Breakdown voltage much lower than PHEMT Low operating voltage (1 to 2 volts) Positive and negative voltage typically needed (V_{GS} and V_{DS})

GaAs HBT

The heterojunction bipolar transistor (HBT) is a new development, and can decrease the cost of GaAs amplifier products because the emitters are formed optically. GaAs HBT devices operate vertically, compared to the horizontal operation of FETs. However, for very high frequency, the emitter size must be made quite small, and the InGaAs layer is thick and is a thermal insulator, so these devices tend to run HOT. Typical HBT amplifiers are "gain blocks", used in the UHF to C-band frequency ranges.

Advantages:	Disadvantages
<ul style="list-style-type: none"> Single power supply polarity All-optical process 	<ul style="list-style-type: none"> Heat dissipation can be problem at small emitter size Typically, reverse isolation is not as high as with PHEMT amplifiers, leading to poor amplifier directivity. Collector resistors are required to stabilize amplifiers. These cut into your power efficiency.

Indium phosphide (InP) HEMT

Indium phosphide HEMT has broken all of the upper frequency records, on the way to terahertz devices. However, there are serious drawbacks to this technology, not the least of which is its high cost. For this reason, InP is more regarded as a lab curiosity rather than a production process. The actual semiconductor that is doing the work in so-called InP is actually InGaAs. Indium phosphide is merely the substrate that it is grown onto. The reason for this is that InGaAs shares the same lattice constant with InP, 5.87 angstroms.

InP substrates are small (3" typical, 4" are also available). Permittivity of 12.4, close to that of GaAs. A huge drawback of indium phosphide technology is that InP wafers are extremely brittle compared to other semiconductors. Try shipping an InP wafer sometime. Silicon is the least brittle, and GaAs is somewhere in the middle.

Advantages:	Disadvantages
<ul style="list-style-type: none">• Extremely low noise figure• Useful through W-band and beyond	<ul style="list-style-type: none">• More expensive than GaAs due to starting material costs, small size of wafers.• Extremely fragile.• Low breakdown voltage (power is low)

Indium phosphide (InP) HBT

Some people think that InP will have a second chance to become the most ubiquitous power amplifier technology for cell phones when new higher power density/lower voltage lithium ion batteries become available, as suggested in the December 2006 paper by Michael Gaynor (at the end of this chapter). InP has superior low voltage performance compared to GaAs HBT.

Silicon CMOS

Silicon is very economical. It comes in 12 inch (300 mm) and bigger wafers. Processing is also low-cost. But it is not a good media for microstrip (lossy). Silicon by itself doesn't make very good amplifiers above maybe X-band. Noise figure, power, are all second class to any of the compound semiconductors. It can only operate reliably up to 110C, but silicon is an pretty good heat dissipater.

Silicon carbide LDMOS

Laterally-diffused metal oxide semiconductor technology, used to make power amplifiers. Can withstand 200C channel temperatures.

Silicon germanium HBT

SiGe is a new development (in the last years), and was originally predicted to put all forms of GaAs into the history books. SiGe can make very cheap parts, with performance maybe into millimeterwave, and processing on eight-inch (200 mm) diameters wafers. But the devices are not as high-performance as GaAs, in terms of noise figure and power. The setup charge at IBM to make a mask set is enormous, because 200 mm contact masks are needed (GaAs usually uses a 10X wafer stepper, these glass reticles are relatively cheap).

The poor insulating properties of a silicon substrate means it's not a good media for microstrip, so you have two choices. You can make transmission lines in the backend of line (BEOL) SiO_2 and metal layers. The SiO_2 dielectric layers are thin, which means high metal losses. Or you can send your wafers to a third party for post-processing to put a lower dielectric metal system on top of it, such as benzo-cyclo-butene (BCB) and gold.

Every time the upper frequency of SiGe extended, the breakdown voltage is reduced. Some of that stuff has to operate at 1.0 volts.

Advantages:	Disadvantages
<ul style="list-style-type: none"> • Eight inch silicon wafers mean low production cost in high volume • All-optical process (also low cost) • Possible to add stacks of logic onto RF chip (BiCMOS logic) 	<ul style="list-style-type: none"> • Low V_{br}, as bad as 1.5 volts for IBM "9HP" • Electrically, Si is not a great insulator • Thermal runaway? • 110C max junction temperature • Not radiation hard • No equivalent of a switch FET, so phase shifters and attenuators are a problem • Not many foundries do SiGe • High setup charges due to expensive mask set

IBM's SiGe HBT BiCMOS Technology Generations:

- 1st Generation (IBM 5HP – 50 GHz HBT + 0.35μm CMOS)
- 2nd Generation (IBM 6HP – 50 GHz HBT + 0.25μm CMOS)
- 3rd Generation (IBM 7HP – 120 GHz HBT + 0.18μm CMOS)
- 4th Generation (IBM 8T – 200 GHz HBT)
- 5th Generation (IBM 9T – 350 GHz HBT)

Gallium nitride (GaN)

This is the future of microwave power amplifiers. GaAs has probably exceeded its half-life. More expensive in terms of dollars per die, GaN offers a path to much higher power densities and therefore cheaper dollars per Watt. Breakdown voltages of 100 Volts are possible! GaN is still a relatively immature process, reliability has been a huge problem that is just being overcome. Ancillary stuff like higher-voltage capacitors and resistors, and backside processes need to be redeveloped at MMIC foundries in order to participate in this new technology.

DARPA (Defense Advanced Research Projects Agency) is pumping millions of dollars into GaN so that the US will maintain technological superiority in military programs for the next decade or two. The big DARPA program is called WBGS-II (for Wide BandGap Semiconductor), and the three teams are TriQuint/Lockheed, Raytheon/Cree and Northrop Grumman.

Substrates for GaN are either silicon carbide, sapphire, or silicon (Nitronix uses this approach). "Native" GaN wafers are impractical, so a lot of expensive alchemy is needed to align the GaN crystal onto mismatched substrates. Four-inch SiC substrates are just becoming available, for GaN-on-silicon, four inch wafers are also available. SiC is an excellent heat sink, and GaN can operate up to greater than 150C channel temperature. Below 2 GHz, expect to see GaN used in base station applications, competing with silicon carbide technology. Higher frequency GaN products will be fielded by the military, HRL reports power amplifiers even up at millimeterwave!

Silicon is not such a great heat sink as silicon carbide (40 versus 350 W/m-K), so lower-cost of GaN on-silicon-may be outweighed by the ability to dissipate higher power (and thereby achieve greater power density) on SiC. Normally, silicon's conductivity makes it lossy as an RF substrate, Nitronix could fix that using high-resistivity silicon.

Advantages:	Disadvantages
<ul style="list-style-type: none">• Up to 10X the power density of GaAs PHEMT has been demonstrated.• Higher operating voltage, less current.• Excellent efficiency possible.• SiC substrates are great heat spreaders.• Can operate hotter than GaAs, Si or SiGe.	<ul style="list-style-type: none">• Expensive as heck!• Reliability not established yet• You have to deal with a huge heat flux.

Antimonide-based compound semiconductors

At the other end of the power spectrum is ABCs. Here's a technology that can operate at only one tenth of a volt! It is possible to create low noise amplifiers that dissipate only one milliwatt using ABCs. The market? Space-based arrays, where power is limited to solar cells, and the received power from earth is pretty-well attenuated to next to nothing. Don't look for ABCs applications where high linearity is a priority.

Microwave Transistor-Parameter Trade-offs in Circuit Design: Part 1

John G. Tatum

Wed, 2013-11-06 10:20

September, 1967

The rapid advance in transistor technology into the microwave-frequency region makes this article on microwave transistor trade-offs especially timely. Designers of microwave circuits using transistors should find the information presented here very helpful in their work. It will also bring other readers up to date on a subject of vital importance to the microwave industry.

Part 1 deals with basic considerations and evaluates the effect of dc parameters on microwave-circuit performance.

Part 2 will relate rf parameters to circuit performance and discuss transistor characteristics for power amplifier applications.

Part 3 will cover microwave-transistor thermal effects and VSWR considerations and will interrelate the dc-rf circuit parameters to microwave circuits. E.T.E.

Part 1: Basic Considerations

Rf power transistors have recently moved rapidly into microwave applications both at sub-harmonic and direct-operating frequencies. The state-of-the-art should continue to advance, especially the maximum operating frequency, reliability, packaging and for transistors tailored to specific design applications. At present, both general purpose and tailored transistors for specific microwave applications are available. It is important, therefore, for the circuit designer to have an insight into the trade-offs involved to better understand the design problems and achievable circuit performance.

For a given transistor type and its processing, there are definite differences in high-frequency performance and interaction with the circuit. These differences can be related to the basic dc and rf parameters of the transistor. Knowing these relationships, it is then possible for the circuit designer to better understand the differences between transistors and for the equipment designer to better tailor transistor parameters to meet specific performance criteria.

The bipolar transistor now offers reliable power outputs up to 50 W at 150 Mc and 15 to 20 W at 400 Mc. The power-frequency state-of-the-art at present is shown in Fig. 1. This is primarily for Class C, cw power output. Most microwave power generation uses Class C amplifiers at lower frequencies with multiplication, or direct Class C amplification at the planned output frequency.

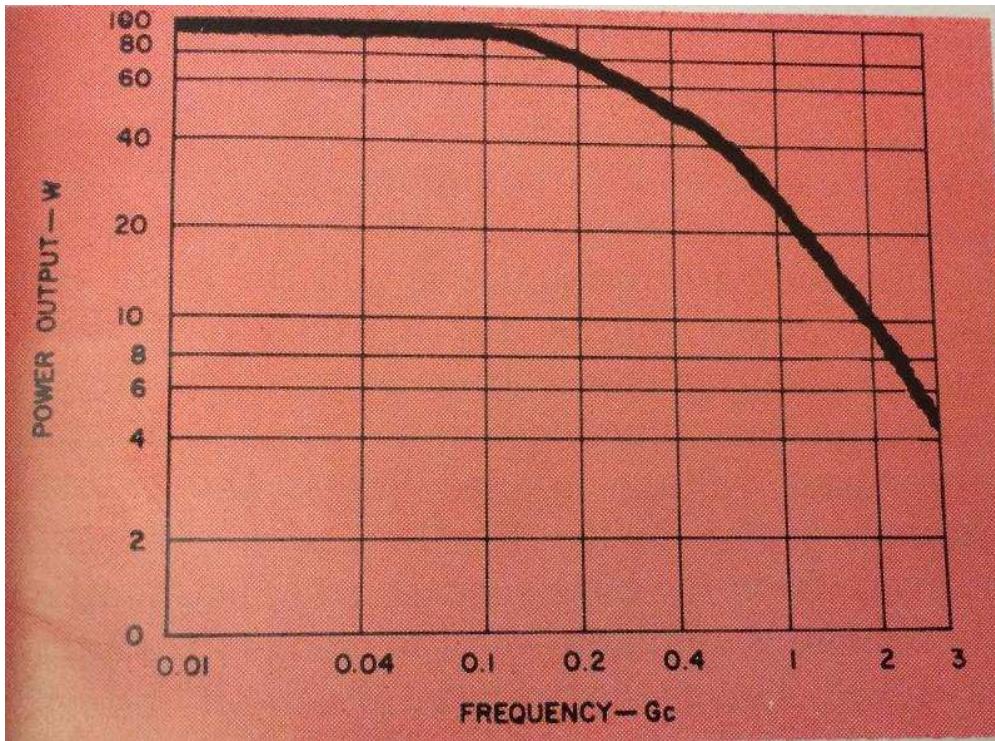


Fig. 1. Power-frequency state-of-the-art for transistors operating cw Class C.

Selecting a transistor

Some basic guidelines for the circuit designer in selecting a transistor are:

- Do not introduce a transistor to a circuit that is not compatible. Understand the characteristics of the semiconductor device before designing circuits around it.
- Exercise caution in package selection. Requiring more than is needed is costly; requiring less than needed causes trouble.
- Selecting a semiconductor device on cost alone becomes a costly mistake if needed performance is sacrificed.
- Select a device which is both available and will do the proper circuit job.
- Stay within the recommended limits set by the manufacturer on its data-sheets. This requires a complete understanding of the data-sheet parameters and their interrelated use.
- Don't overspecify the semiconductor device. Give the widest possible tolerances to save cost and improve delivery of the device from the vendor.
- Understand maximum device ratings and how to apply them in combination. Not all information on possible combinations of maximum ratings can always be included on the data sheets.
- Evaluate both the device and the circuit operation thoroughly, including all of the stress levels. Stress levels often dictate the semi-conductor device to use. How stress levels can be applied to the transistor requires a complete knowledge of its parameters and capabilities.
- Obtain assistance from the applications engineering department of the semiconductor manufacturer. It is less costly to ask a question early in the circuit design than after all of the devices have been destroyed!

Microwave transistors- how they're built

To understand the characteristics of power amplifier transistors, and how parameters affect each other in combination with circuit trade-offs, the circuit designer should have a basic concept of device construction. The

semiconductor die, resistor stabilization when applicable, and the packaging of the device are all very important at microwave frequencies. It is important to qualitatively relate device construction to parameters and circuit performance. Thus, one can intelligently evaluate different devices and the differences between devices of the same transistor family.

The currently most popular type of transistor construction will be described—planar epitaxial diffused junction. This type is used by all semiconductor manufacturers at present in the processing of high-frequency, power-amplifier transistors. The geometries may vary, but the concepts described here are qualitatively independent of the geometries employed. Parameters are affected by geometry, but the relationships are similar for all types.

Basic transistor construction

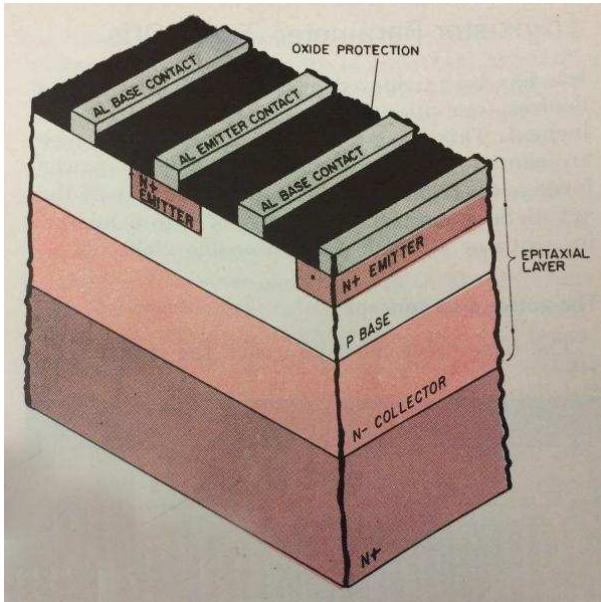


Fig. 2. Planar transistor construction. The basic elements are indicated.

The NPN planar transistor is constructed as shown in Fig. 2. Fig. 3 is a typical top view showing interdigitated (comb structure) connections for the emitter and base areas; which is one type of connection pattern.

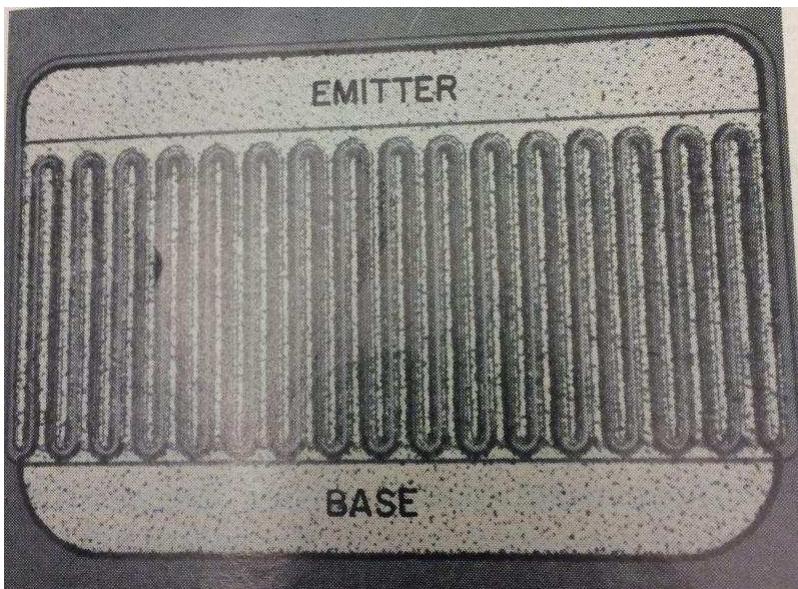


Fig. 3. Top view of typical planar transistor showing interdigitated comb-like structure. This is one popular connection pattern.

Transistors for higher frequencies and higher power outputs in a given physical chip area must have increased active-to-physical-area ratio. To accomplish this, a finer geometrical structure for the emitter is necessary to increase the emitter-base periphery for a given physical area. This requires smaller emitters spaced closer together. This, in turn, requires tighter mask tolerances, creating more yield problems and requiring more careful processing; thus, a more expensive device is created. Emitter geometry definition of one micron or less has been achieved in small-signal, low-power devices (one micron = 10^{-6} meters or 3.95×10^{-5} inches). This mask-tolerance requirement, however, cannot yet be attained in very high power, large-area transistors. The present state-of-the-art dictates emitter geometries of 3 to 5 microns in width or site side for reasonable yields.

The active area concept

The base drive must approach the emitter-base junction from the side as visualized from the basic construction model. This base current has to go through the region under the emitter. The narrower the base width, the higher the lateral sheet resistance of the structure will be, or the higher the effective base resistance is and the more voltage drop there will be for a given base drive. Thus, the emitter-base voltage even at the edge of the emitter-base junction will not be as high as the emitter-base voltage applied across the external terminals of the device. Further, under the emitter, away from the base-contact area, less emitter-base voltage is available and the current turn-on is less as well. This is the “current pinch-off” effect.

Current pinch-off is a function of dc beta (h_{FE}) since beta is a function of the base width. As the transistor is driven harder, the pinch-off effect becomes worse and the active area of the device (the emitter-area-carrying current) increases less rapidly than at lower current levels. What the active area looks like is roughly shown in Fig. 4. Basically, this is a three-dimensional series resistance with a shunt capacitance. As frequency increases, this built-in low-pass filter allows less base-emitter junction drive. The active area decreases as the frequency increases. This, to the circuit designer, means that the transistor is shrinking in useful size or area. Unfortunately, the impedance levels are not changing as rapidly and the output capacitance is only slightly affected.

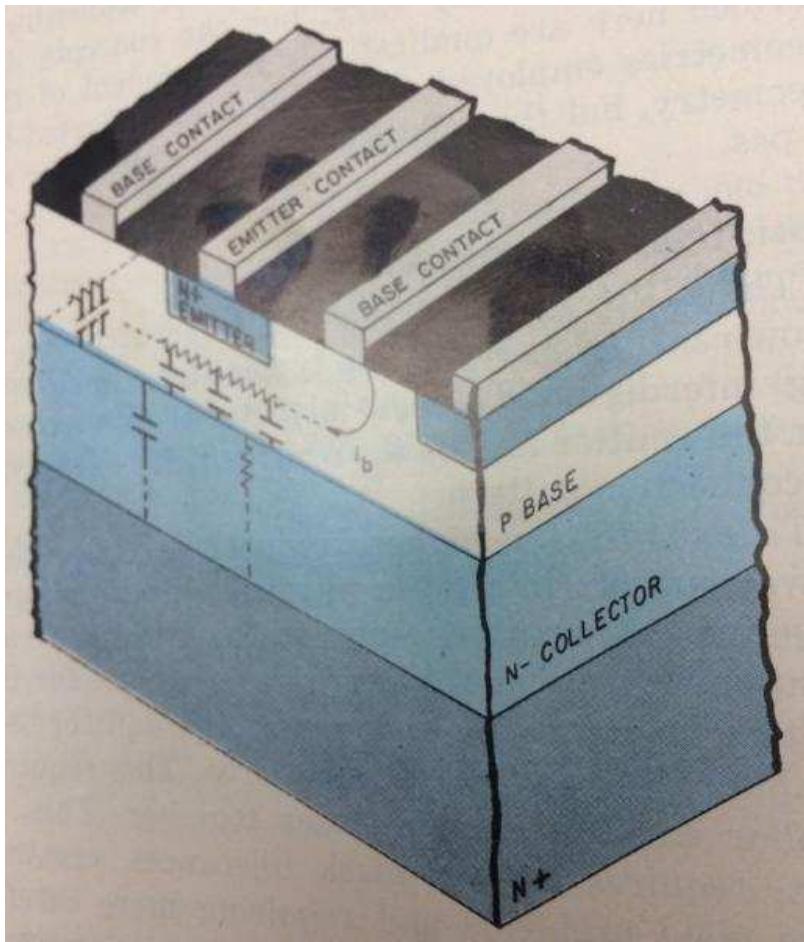


Fig. 4. Impedance representation in transistor model. The effect is a low-pass filter.

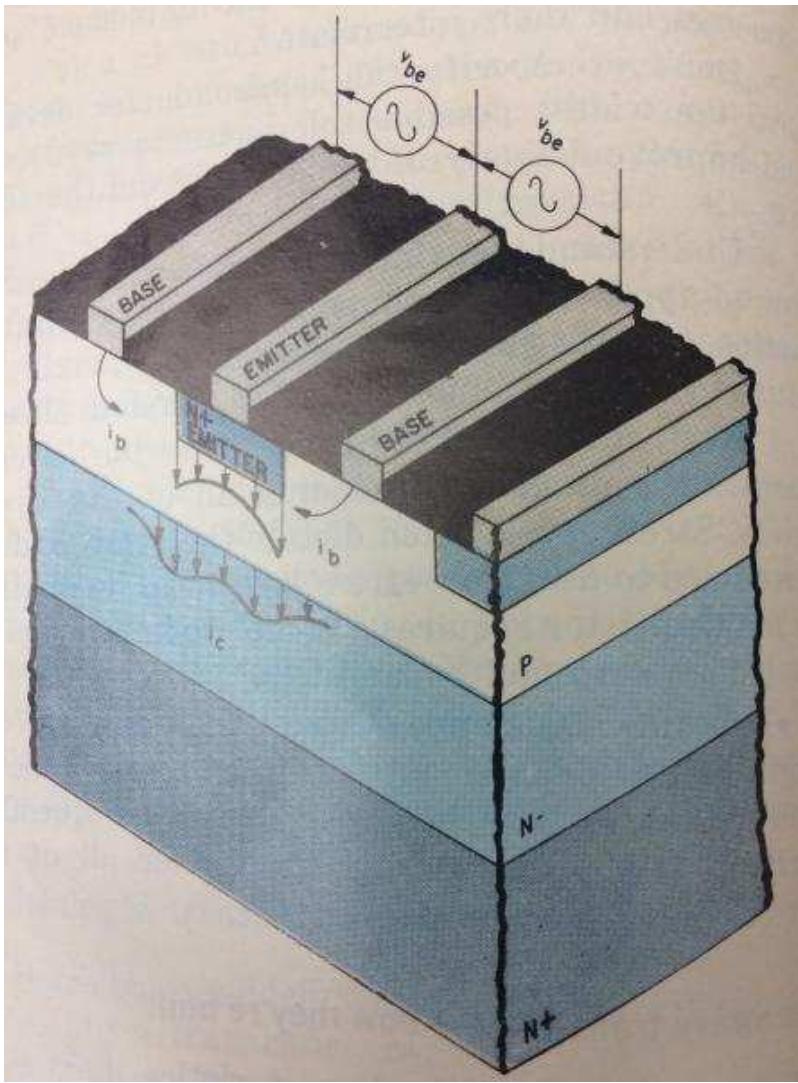


Fig. 5. Transistor current distribution for a simple transistor model.

How the current distribution looks at one frequency for a simple transistor model, is shown in Fig. 5. From this sketch, it can be seen how a higher-frequency transistor (a transistor with a higher active-to-physical area ratio) would require a finer geometry. By example, Fig. 6a shows a coarse geometry compared to Fig. 6b. For the same drive at the same frequency, the current distributions would be as shown. For a given physical area, there is much more active area in the transistor of Fig. 6b because of the finer geometry. This makes the transistor more useful at this frequency. The greater active area gives more power gain for reasons that will be discussed. The transistor of Fig. 6b, however, has problems involving the safe-operating area and uniformity of operation, over the area for which something must be done to give it equivalent safe-operating performance. This also will be discussed.

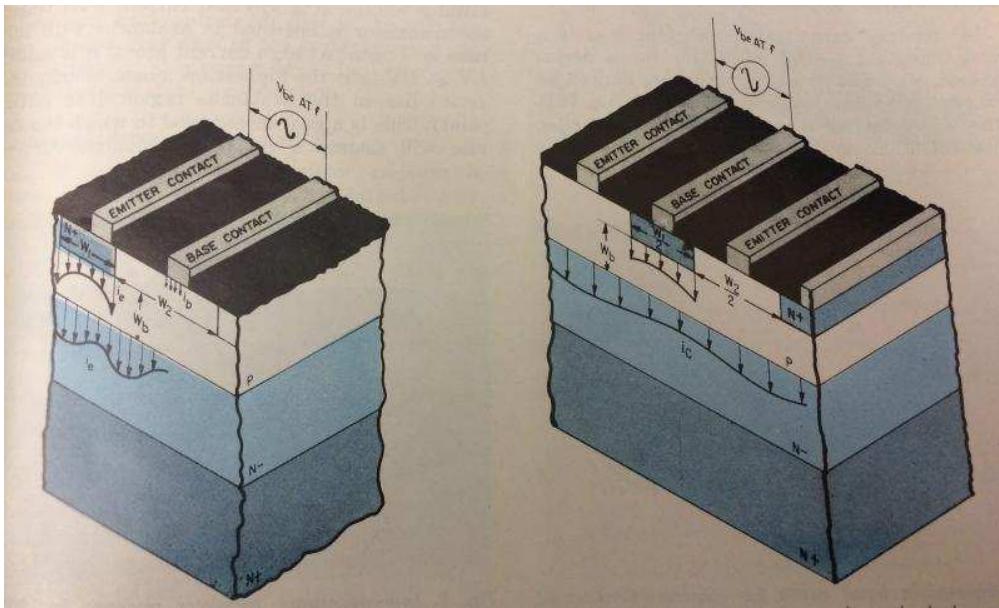


Fig. 6. How finer geometry increases active area. At *a* is a relatively course geometry. For a given physical area, *b* has a more active area because of its finer geometry.

Transistor packaging

Many currently-available transistors are more limited by their packaging than by the basic capability of the chip itself. This is especially so for high-frequency power devices which have relatively-low input and output impedances. The package impedances can easily be as large. Thus, a revolution is taking place in transistor packaging, especially for devices in the microwave-frequency ranges above 400 Mc.

Package inductances and resistive losses have significant effects on circuit performance—more specifically, on bandwidth, stability, power gain and phase delay. Bandwidth is important in many communications circuits, and wide bandwidth is harder to achieve with high-power transistors than for small-signal devices.

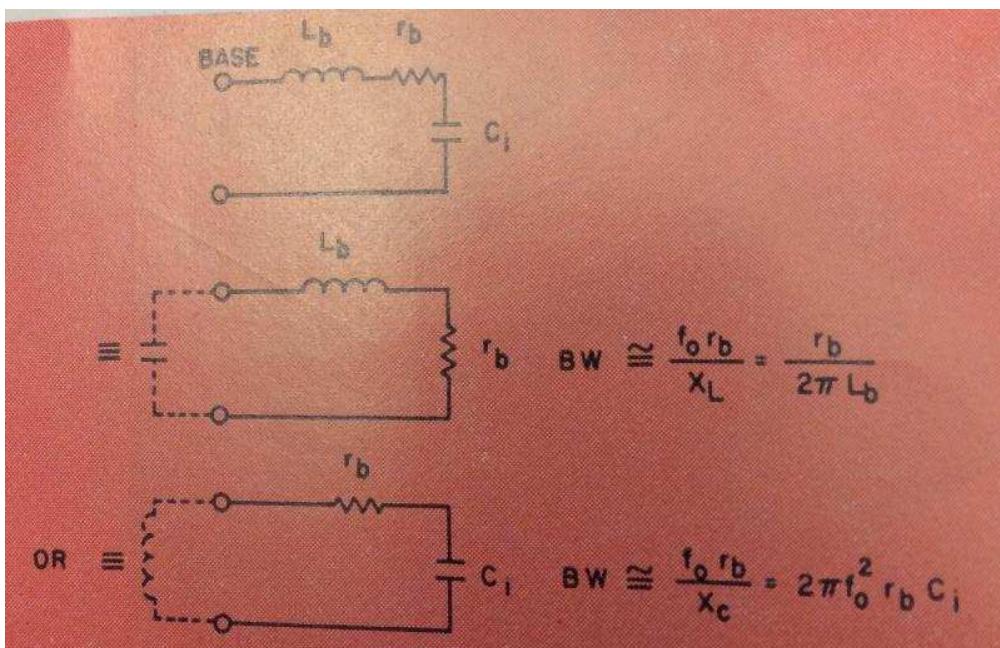


Fig. 7. Equivalent input circuit for common-emitter configuration, showing small-signal relationships between frequency, bandwidth, base resistance and input reactance.

A simple representation of a common-emitter equivalent transistor input circuit is shown in Fig. 7, demonstrating the small-signal relationships between bandwidth, base resistance and input reactance. The large-signal r_b and C_i are different from the small-signal values, and an exact quantitative analysis is impossible. However, the large-signal bandwidth at the transistor input circuit will be considerably smaller than that predicted from small-signal parameter measurements. This is primarily because the effective large-signal base resistance, r_b , is lower.

The emitter package inductance, L_e , reduces power gain as shown in the following approximate equation.

$$(1) \quad \frac{P_{0E}}{P_{1E}} = \frac{\omega_T}{\omega^2 C_c (4r_b + 2\omega_T L_e)}$$

L_e also reflects an impedance into the input circuit of a common-emitter configuration (this is the most widely used configuration and the one of primary concern here). The input impedance given by small-signal analysis is (See Appendix A):

$$(2) \quad Z_{in} \approx r_b + r_e + \omega_t L_e + j[\omega L_e - (\omega t/\omega)r_e]$$

where r_e is the combination of transistor emitter resistance and any external emitter resistance.

Low-inductance packaging improves both bandwidth and stability and thus ease of power matching to the transistor. A lower-inductance lower-Q circuit means less change of phase vs tuning and a wider range of stability with respect to internal feedback. An improved low-inductance package, incorporating wide-ribbon leads for the collector and base and with the emitter connected to the case for low and consistent emitter inductance, is shown in Fig. 8. This is a new concept in high-frequency packaging for transistors above 300 Mc. Still further improvement can be expected in the future.



Fig. 8. Low-inductance transistor package for 300 Mc and above. Wide ribbon leads are used for the collector and base, resulting in better stability over a wider range.

Dc parameters

If one knows a transistor's dc parameters, he can determine what to expect of the rf parameters and of circuit performance. It is very useful to the circuit designer to understand the relationships between dc and rf parameters.

The EIA requirements for registering an rf power transistor for a 2N number are quite loose, allowing a wide latitude in parameters. All manufacturers use as wide a latitude as they can; yet, to ship good products the parameters must be controlled more closely than typical EIA registration requires. Often the parameters of distribution is tightened merely by selection of units to meet the requirements of a specific application.

Common emitter h_{FE} and beta

DC forward current transfer ratio, h_{FE} , is a most important control parameter for a device process. Many different rf parameters as well as circuit performance, correlate directly to h_{FE} . It is typically measured at a low voltage and under pulse conditions so that power dissipation has no effect on it. Typically, h_{FE} increases with junction temperature.

Dc beta is usually specified at both a low-current and a high-current level. Usually a minimum and maximum is specified at low-current levels; a minimum value is certainly most necessary at high-current levels. This goes back to the concept of active area and the fact that at high-current levels the current pinch-off effect occurs. At high current levels, dc beta will decrease quite rapidly when the current density has reached a high level. Therefore, low h_{FE} devices, which have a wider base width and lower lateral sheet resistance in the base structure under the emitter of a transistor, will have more linear or constant h_{FE} vs collector current. A high h_{FE} device will have more radical percentage variations in h_{FE} vs collector current. And as h_{FE} increases, the device will reach a peak at a lower current level.

Typical relationships between h_{FE} and collector current for different levels of h_{FE} are shown in Fig. 9 for two different 400 Mc transistors. The curves are more linear for low h_{FE} devices and this should significantly affect the saturation level at high frequencies and the power-output and modulation linearity. Many of the basic rf parameters also correlate directly to the h_{FE} level of a given transistor for a given process.

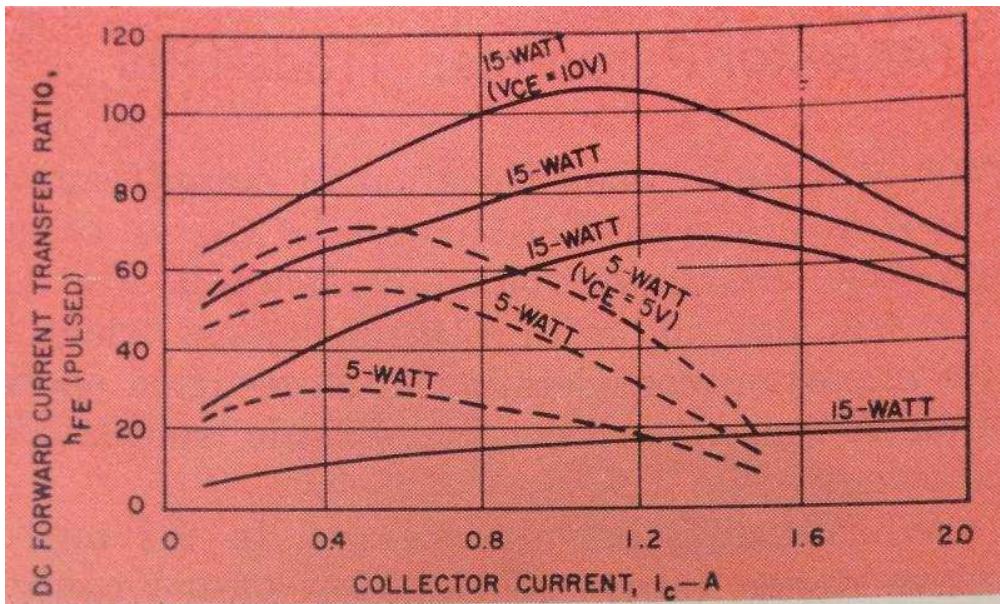


Fig. 9. Relationship of h_{FE} to I_c for two transistors at different h_{FE} levels. The 5-W unit is designated ITT 2N3375; the 15-W transistor, ITT 3TE440.

Breakdown voltages

The dc or pulse-current breakdown voltages typically specified on data sheets are:

- **$BV_{CEO(SUS)}$** -- This is the collector-to-emitter sustaining voltage at a specified current level when the transistor is operated in avalanche with the base lead open. At high current levels, it is called LV_{CEO} . BV_{CEO} is the highest open-base voltage the device has in the avalanche region (the initial point). This is a guaranteed level to which the device will sustain a collector avalanche current without secondary breakdown or complete collapse of the device voltage. It is always measured in a pulse condition. Sometimes a specified quantity of energy is applied by pulsing the transistor from an inductance which has a predetermined amount of stored energy.
- **$BV_{CER(SUS)}$** -- This is the breakdown voltage from the collector to the emitter, with a resistor connected from the base to the emitter. The measurement is made as for $BV_{CEO(SUS)}$. A more common designation is LV_{CER} , or LV_{CES} , when $R_{BE} = 0$.
- **BV_{CBO}** -- This is the breakdown voltage from the collector to the base and thus is the avalanche voltage of the collector-base junction. It is an important parameter because both rf parameters and circuit operation parameters correlate to this breakdown voltage. A fairly broad range of collector-base breakdown voltage is possible for a given process depending on the resistivity variation of the silicon material used.

Typical breakdown-voltage curves for a low-resistivity thin epitaxial transistor and for a high-resistivity and thick-epitaxial device are shown in Fig. 10. Note that significantly different curve

shapes are obtained by different transistor designs. The VSWR capabilities of the transistor are dependent on the sustaining region and these breakdown voltages.

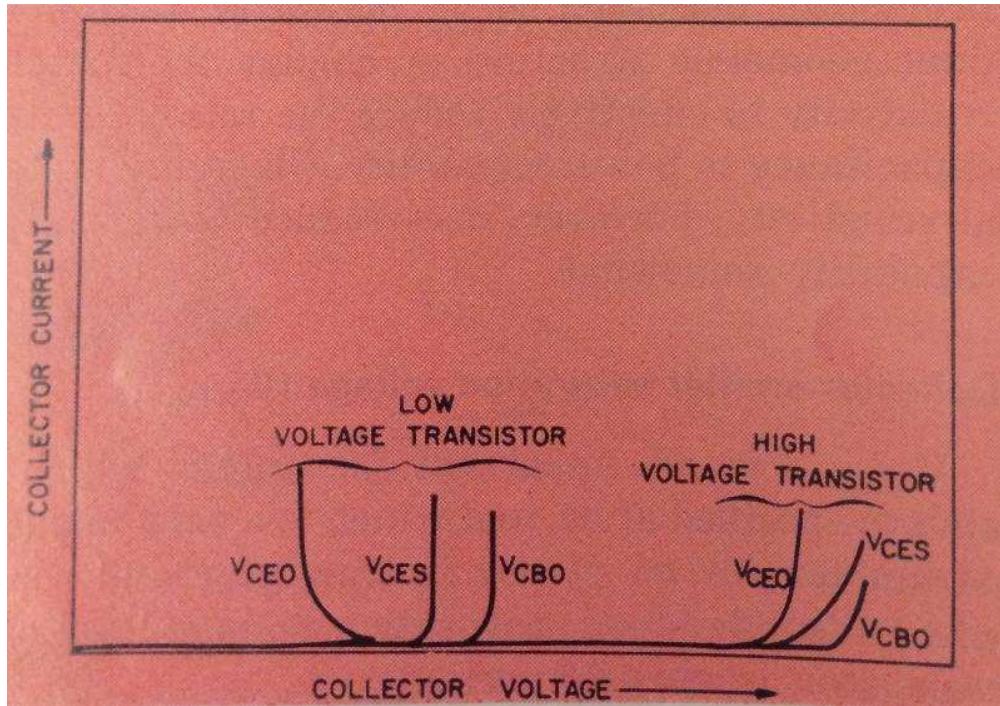


Fig. 10. Breakdown voltage characteristics—typical transistors. Curves at left are for a low-resistivity thin epitaxial layer; at right, for a high-resistivity relatively thick epitaxial device.

- **BV_{EBO}** -- This is the emitter-base breakdown voltage and is also specified at a given current level in the avalanche breakdown region. It is of secondary concern to the circuit designer where the transistor is to be operated at very high frequencies, because the stored charged rather than the external field controls the field in the emitter-base junction over most of the cycle. However, at low frequencies, this parameter is important and should be taken into consideration.

Output capacitance, common-base (C_{ob})

C_{ob} is an important parameter because it affects the circuit tuning and the output-impedance level of the transistor. It also relates to some of the other dc parameters. In a common-emitter circuit, C_{ob} is essentially the output capacitance, too. This is because the impedance levels at the base are quite low relative to the impedance level at the transistor output. However, the high-frequency value must definitely be considered and also the large-signal value (which can be as much as twice the small signal value).

The output capacitance of a transistor represents effectively its junction capacitance in series with a resistance. If the collector resistivity is increased, the effective output capacitance is decreased as seen from the external terminals. Also, if the resistivity is increased, the collector-base breakdown voltage, BV_{CBO} , is also increased. Junction and epitaxial-thickness variation will cause some variation in output capacitance, too. A typical distribution of C_{OB} vs. collector-base breakdown voltage is shown in Fig. 11. C_{OB} will also vary with collector voltage, which is an important consideration in large-signal operation. A typical variation in a 400-Mc transistor is shown in Fig. 12.

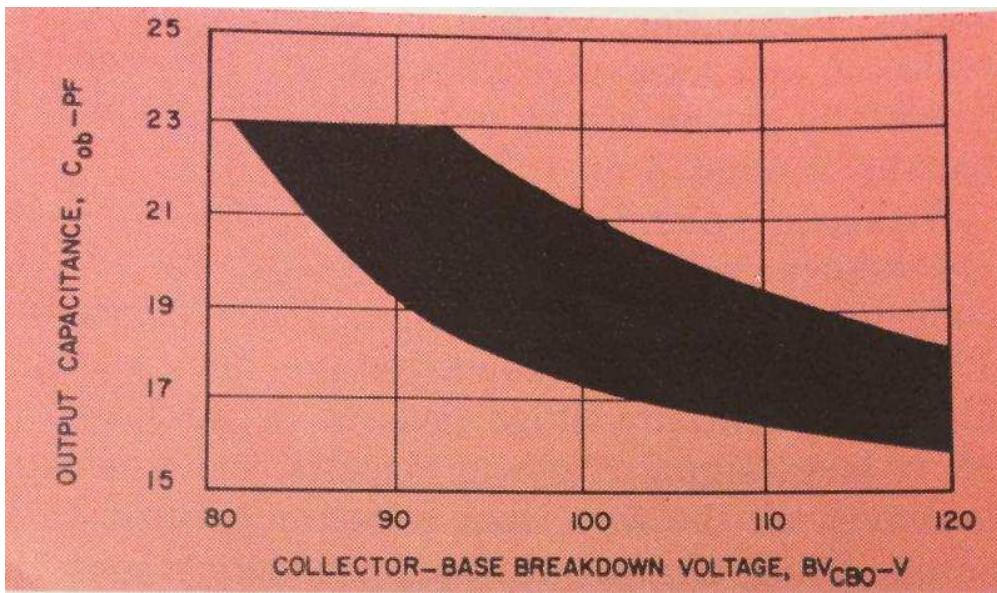


Fig. 11. Typical C_{ob} - BV_{CBO} distribution. This was obtained on a type ITT 3TE440 transistor at $f \approx 1$ Mc and $V_{CB} = 28$ V.

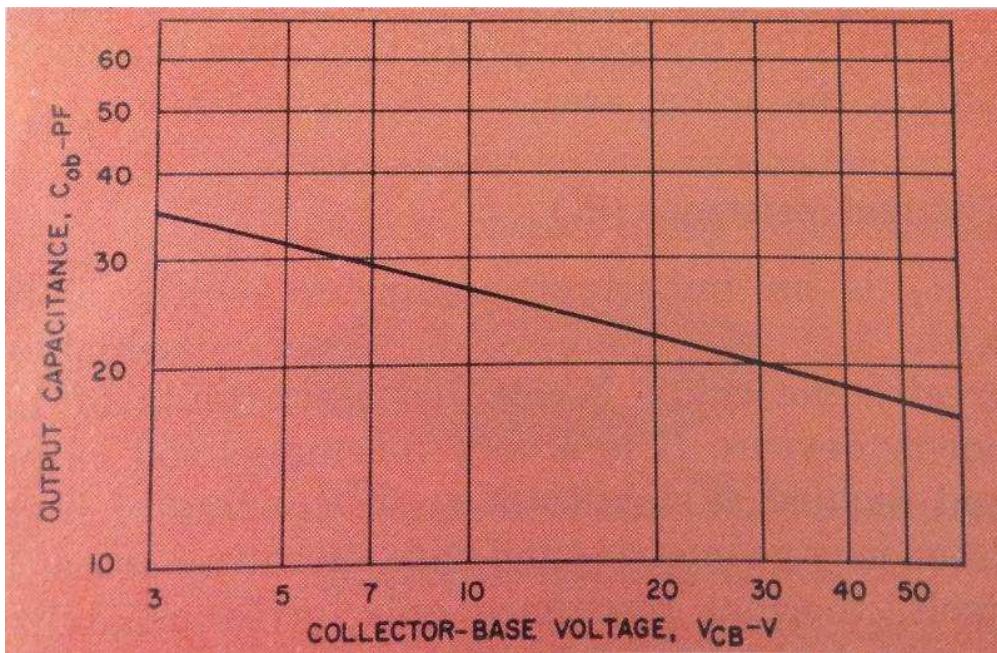


Fig. 12. Typical C_{ob} - V_{cb} curve for a 400-Mc transistor, type ITT 3TE440. This variation is important in large-signal operation.

When transistors are operated in the microwave region (above 300 Mc) low output capacitance is important for good gain and high circuit impedance. Based on the "active area" concept previously discussed, it is necessary to build a finer geometric or change the material resistivity to effectively reduce the ratio of output capacitance to power capability. Changing material resistivity, however, does reduce power-output capability somewhat.

Collector-emitter saturation voltage ($V_{CE(SAT)}$)

$V_{CE(SAT)}$ is an important parameter which is always specified at dc, and which is a very misused parameter for

an rf power transistor and somewhat misunderstood. Saturation voltage is specified at given collector and base currents, thus at a forced h_{FE} (typically at the lowest guaranteed h_{FE} , which is usually around 8 or 10).

$V_{CE(SAT)}$ correlates to the collector-base breakdown voltage; i.e., the resistivity of the collector epitaxial material in the transistor. Thus, a higher breakdown-voltage device has a higher saturation-voltage level at dc, and also at rf. In large-signal rf power circuits, the transistor is driven all the way from collector saturation to cutoff. Thus, the saturation level determines the extent of the voltage swing. The relationship between dc saturation and rf saturation is partly controlled by the geometry of the device because it affects the same area.

Thermal resistance (R_T)

R_T is an important parameter which, along with maximum-rated power dissipation, creates the actual dissipation level limits of the power devices. It is a very misunderstood rating and requires a significant understanding of high-frequency geometries and safe operating areas. In itself, thermal resistance only gives capability, provided the transistor is operated at certain collector voltages and currents as they are translated to junction temperatures and voltage fields.

Appendix

Thermal resistance is not an absolute constant of the transistor because it can be different, depending on the measurement conditions.

The approximate effect of L_e and r_e can easily be shown considering the simplified T-equivalent circuit of Fig. A.

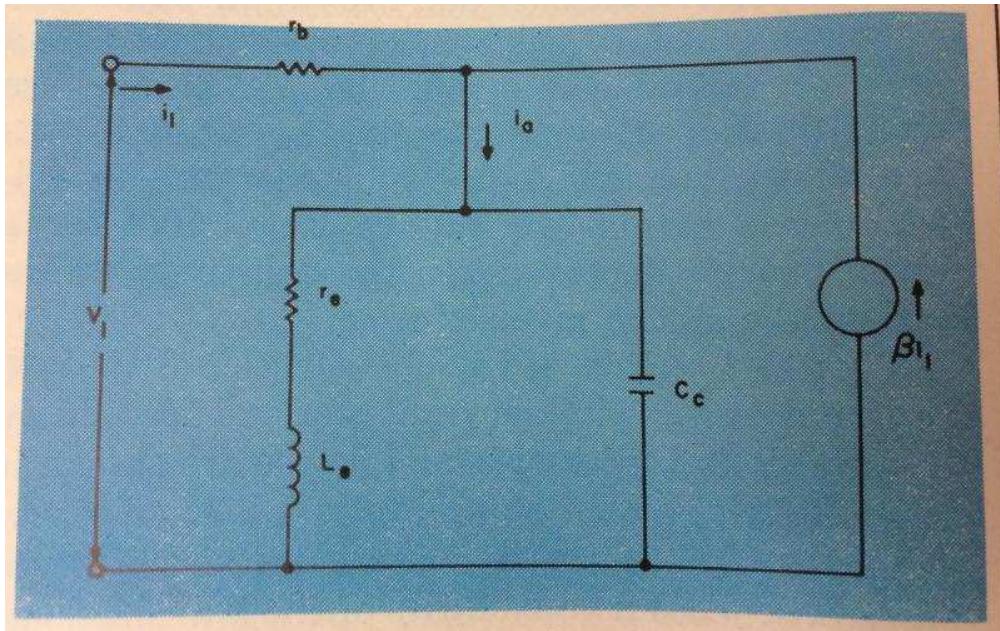


Fig. A. T-equivalent circuit with output shorted.

At high frequencies, it is convenient to represent β by the equation:

$$(1) \beta(\omega) = \frac{\omega_t}{j\omega}$$

From Fig. A2,

$$(2) i_a = i_1(1 + \beta)$$

Writing the voltage-loop equation for the input circuit, using relations (1) and (2), results in the equation:

$$(3) V_1 = i_1 r_b + i_1 \left(1 + \frac{\omega_t}{\omega}\right) \frac{r_e + j\omega L_e}{1 - \omega^2 L_e C_c + j\omega C_c r_e}$$

which results in an input impedance of:

$$(4) Z_{in} = \frac{V_1}{i_1} = r_b + \left(1 - j \frac{\omega_t}{\omega}\right) \frac{r_e + j\omega L_e}{1 - \omega^2 L_e C_c + j\omega C_c r_e}$$

At normal frequencies of interest for normal rf power transistors,

$$(5) \omega^2 L_e C_c \ll 1,$$

and

$$(6) \omega C_c r_e \ll 1.$$

Eq. 4 is then simplified to the final result:

$$(7) Z_{in} = r_b + r_e + \omega_t L_e + j \left(\omega L_e - \frac{\omega_t}{\omega} r_e \right).$$

Read the next part in this series [here](#).

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Microwave Transistor-Parameter Trade-offs in Circuit Design: Part 2

John G. Tatum

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October, 1967

Although dc parameters, as covered in Part 1 of this series, give a great deal of information about a transistor for use at microwave frequencies, rf parameters are important, too. The parameters to be considered are h_{fe} , G_{PE} , η , rf BV_{CEO} , and $V_{CE(SAT)}$. Each will be defined and discussed in turn.

Hf forward-current transfer ratio (h_{fe})

The high-frequency common-emitter forward-current transfer ratio of a transistor is the ratio of the short-circuit output current divided by the input current. This is the high-frequency Beta of the device. The theoretical curve of current gain vs frequency is shown in Fig. 1 and is very closely approached in practice.

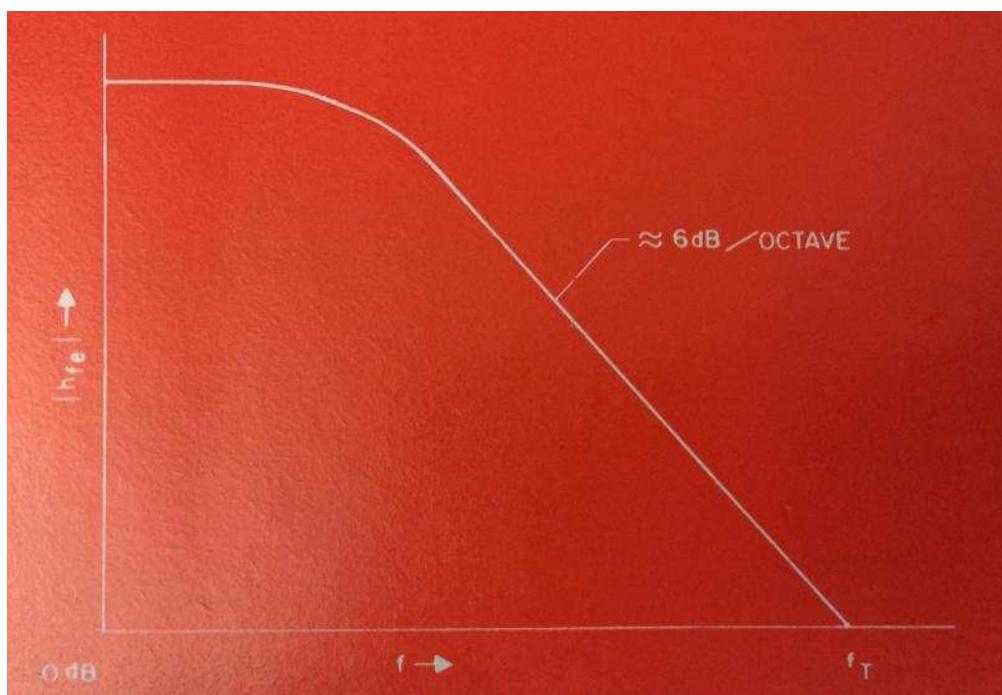


Fig. 1. Theoretical curve— h_{fe} vs f . In practice, the high-frequency current transfer ratio varies with frequency in a manner closely approximating the theoretical curve shown.

The frequency at which h_{fe} is 1 (or 0 dB) is usually considered as being f_T , the current-gain times bandwidth of the transistor. Parameter f_T is usually estimated by multiplying h_{fe} by the frequency of measurement. In practice, however, measured h_{fe} times frequency of measurement does not give f_T – especially for high-power rf transistors. The external h_{fe} is not necessarily that of the internal structure and thus is not always an exact

measurement or estimate of f_T . The difference is cause by the division of input current between the input resistance depends upon the emitter inductance and whether there is resistor stabilization in the emitter structure. Thus, the measured h_{fe} may not be the actual internal gain of the structure. Although external current gain is important, in estimating power gain it is the internal current gain that should be used. This is especially so if emitter inductance is to be neglected or if any emitter resistance will otherwise be used in the power gain formula. All transistor manufacturers' data sheets specify h_{fe} as the external measurement. However, the internal (current) gain-bandwidth product can be somewhat higher depending upon device type and packaging.

Parameter h_{fe} determines many circuit capabilities as well as some of the dc transistor parameters. It is not a measure of power gain, because base resistance (which can be established somewhat independently of h_{fe} or f_T) also enters into determination of power gain.

Input and output admittances

To design adequately a high-frequency power-transistor circuit, the approximate impedances to which the input and output must be matched need to be known. In effect, it is the large-signal impedances that are important. These are difficult to determine with available measuring equipment, but accurate measurement techniques have been established. At present, mostly small signal parameters are specified. These place the circuit design in the right ball park for the large-signal impedance values, which are now being specified on some manufacturers' data sheets.

Common-emitter admittances are normally given in the transistor specifications such as input admittance y_{11e} (the input admittance with output short-circuited) and output admittance y_{22e} . Typical forward-bias curves for these small-signal values are shown in Fig. 2. The large-signal input resistance will be less than the small-signal value. Thus, the circuit designer must compensate for this. The large-signal output admittance will be closer to the small-signal value if the latter is measured at less than the large-signal circuit operating voltage.

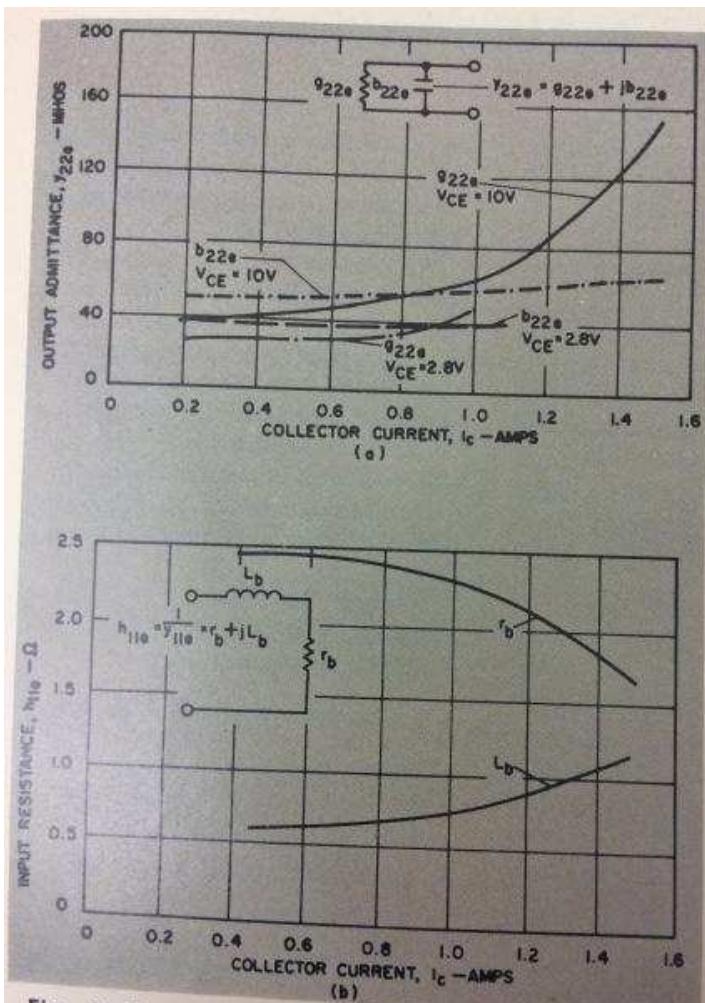


Fig. 2. Typical forward-bias curves for small-signal values of common-emitter admittance and large-signal input resistance. Curves were obtained on a type ITT-3TE440 transistor at 400 Mc.

Typically, the small-signal measurement of y_{22} at 10 V will agree closely with the large-signal value at around 28 V. Sometimes, the equivalent series circuit input resistance and reactance are given rather than the shunt values.

Common-emitter power gain (G_{PE})

The large-signal common-emitter power gain, G_{PE} , is the ratio of the output power, P_{OE} , to the input power, P_{IE} , in a common-emitter power-gain circuit. Most specifications give the P_{IE} range for a given P_{OE} and supply voltage. Power gain typically decreases as the temperature of the transistor increases at high frequencies. The reverse may be true using a high-frequency transistor at low frequency. It is also a function of the power-output level and the transistor's dc parameters. A typical dependence of power gain on power output is shown in Fig. 3. The closer the power output design center is to the transistor's saturated power output, the greater the fall-off in power gain with increased drive, and the greater the variation from transistor to transistor.

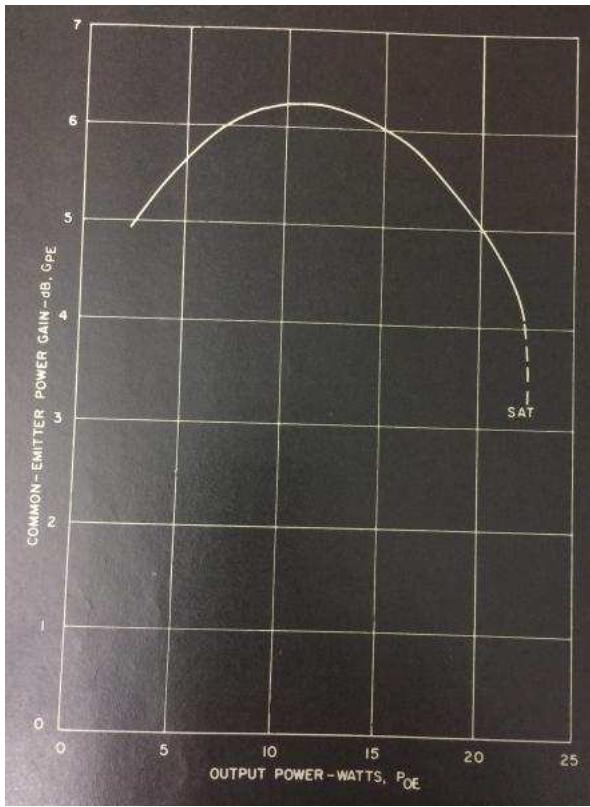


Fig. 3. Typical dependence of power gain on output power from microwave transistors.

Power gain is normally measured with the input and output simultaneously matched for maximum power gain. Occasionally, some mismatch is allowed to improve efficiency. Power gain is typically specified in a narrow-band tuned circuit. Broader bandwidth power gain would be somewhat lower.

Power gain theoretically decreases with increased frequency at 6 dB per octave. In practice, it decreases slightly faster than this. How power gain typically varies with frequency is shown in Fig. 4. Theoretically, the power gain is 1 (0 dB) at f_{max} (maximum frequency of oscillation). At this point, all of the output power would have to be fed back to the input of the device to sustain oscillation. In good present-day devices, f_{max} can be considerably higher than f_T , and thus significant power gain can be obtained at a frequency above f_T . This is because power gain is proportional to f_T/r_b . Base resistance is consequently a major factor in high-frequency performance.

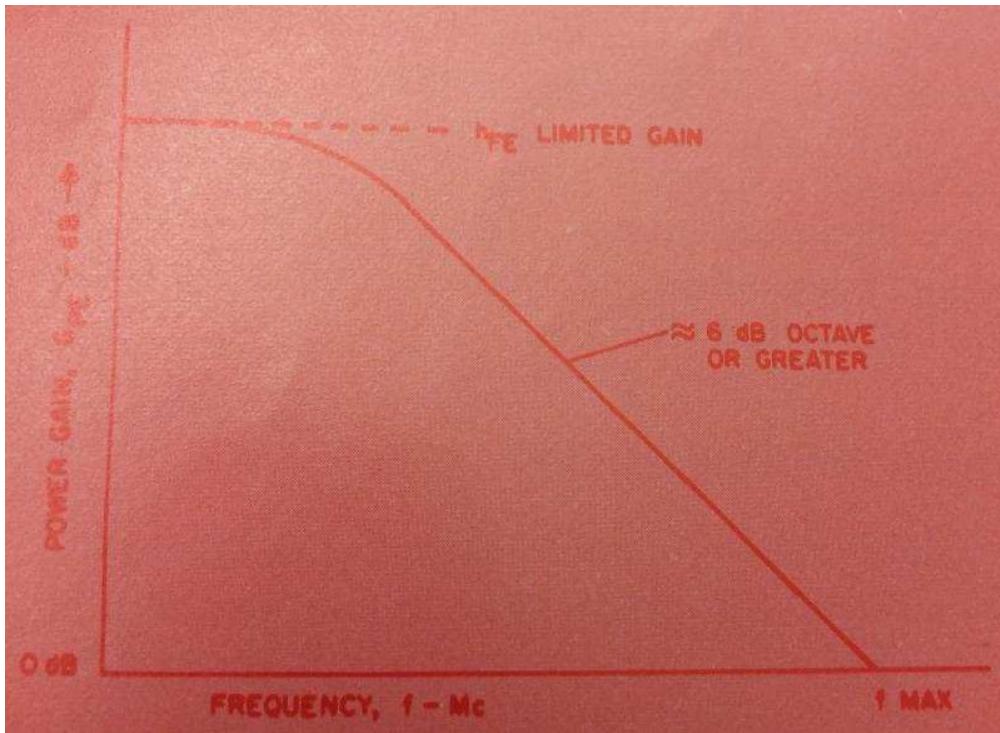


Fig. 4. How power gain decreases with frequency—a theoretical curve.

Collector-circuit efficiency (η)

Collector-circuit efficiency is an important parameter because it involves the power consumption of the power amplifier. Collector deficiency is defined by:

$$\eta_C = \frac{P_{OE}}{P_{DC}} \times 100 \text{ percent.}$$

Assuming that the amplifier stage has reasonably high-power gain, the collector-circuit efficiency is then very nearly the over-all efficiency which is defined:

$$\eta = \frac{P_{OE}}{P_{IE} + P_{DC}} \times 100 \text{ percent.}$$

For a given tuned circuit, η varies with power output as illustrated in Fig. 5. Collector efficiency can very much be a function of the circuit design, but it also relates to some transistor parameters.

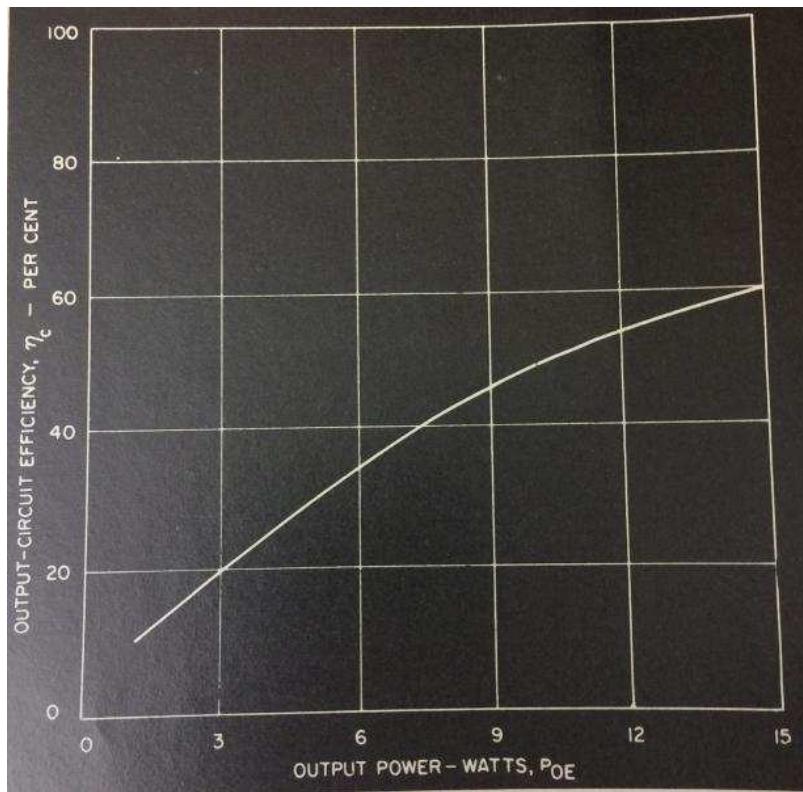


Fig. 5. Collector-circuit efficiency as a function of output power for a typical microwave transistor (ITT3TE440) at 400 Mc. $V_{cc} = 40$ V.

Rf breakdown voltage

Initial studies by James Janky, at ITT Semiconductors Applications Engineering Department in September, 1966, show that the rf breakdown voltage of a transistor is higher than its dc value (in a CEO or CEX mode) and can approach its BV_{CBO} value at high frequencies. Attempts to measure this value may be accomplished by applying rf directly to the collector and measuring the result. The result is very dependent on the circuit in the base and the capacitive current through C_{OB} . A circuit, which leaves the base open at rf, tends to approximate the typical condition of an amplifier circuit but will give much lower breakdown values than if the C_{ob} current is shorted at the base (BV_{CES}) which will measure closer to BV_{CBO} at rf.

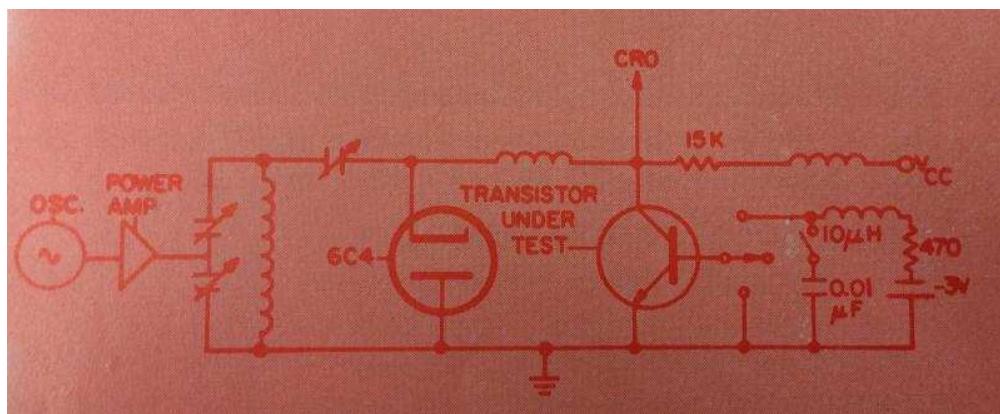


Fig. 6. Rf breakdown test circuit.

A simple, straightforward rf breakdown test circuit is shown in Fig. 6. The transistor is normally in the OFF condition; a reverse bias is applied to the collector; and rf peak voltages are applied to the unit until breakdown occurs.

The BV_{CEO} of the 2N3375 with 40 V bias is shown in Fig. 7. Only a 10 percent increase is apparent here. BV_{CES} will be considerably higher.

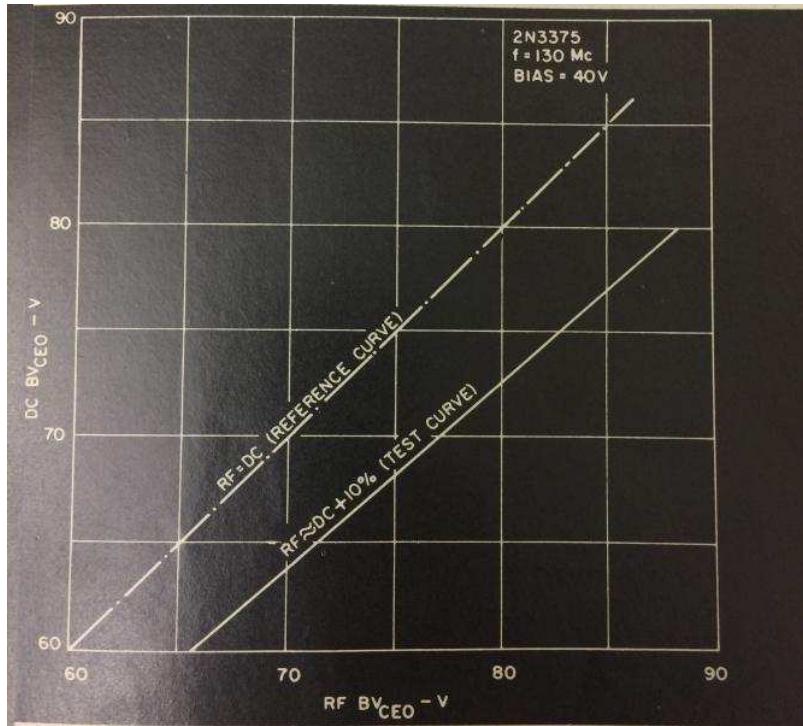


Fig. 7. Dc vs rf breakdown voltage for transistor 2N3375 operating at 130 Mc with 40-V bias.

Transistor epitaxial thickness and basewidth are important factors because these affect the avalanche multiplication factor. Table 1 gives the range for other device types.

Table 1: Dc and rf breakdown-voltage comparison for typical microwave transistors

Transistor type	DC BV_{CEO} (Volts)	RF BV_{CEO} @100 Mc (Volts)
2N3866	34	50
2N3632	50	92
3TE160	75	96
3TE250	100	130

Much work must yet be done to determine how the actual operating-circuit breakdown varies. This is because the foregoing fails to account for an rf base drive and the fact that the transistor is going through a transition—from a charge-controlled (ON) to an (OFF) state where the charge-storage time may be a considerable portion of an rf cycle.

Saturation Voltage (rf $V_{CE(SAT)}$)

At higher frequencies, saturation voltage is significantly greater than the dc value. This is because the high-frequency active area is less than at dc. Typically, a high-breakdown-voltage device utilizing high-resistivity materials will have higher saturation voltage levels than low-breakdown-voltage device. The rf saturation voltage will thus have a great effect on the saturated power output of a transistor operated at too low a supply voltage. It is not advisable, therefore, to use a high-breakdown-voltage device for a low-voltage application. For a given power level, a much larger-area device is necessary if the saturation voltage is a significant percentage of the supply voltage.

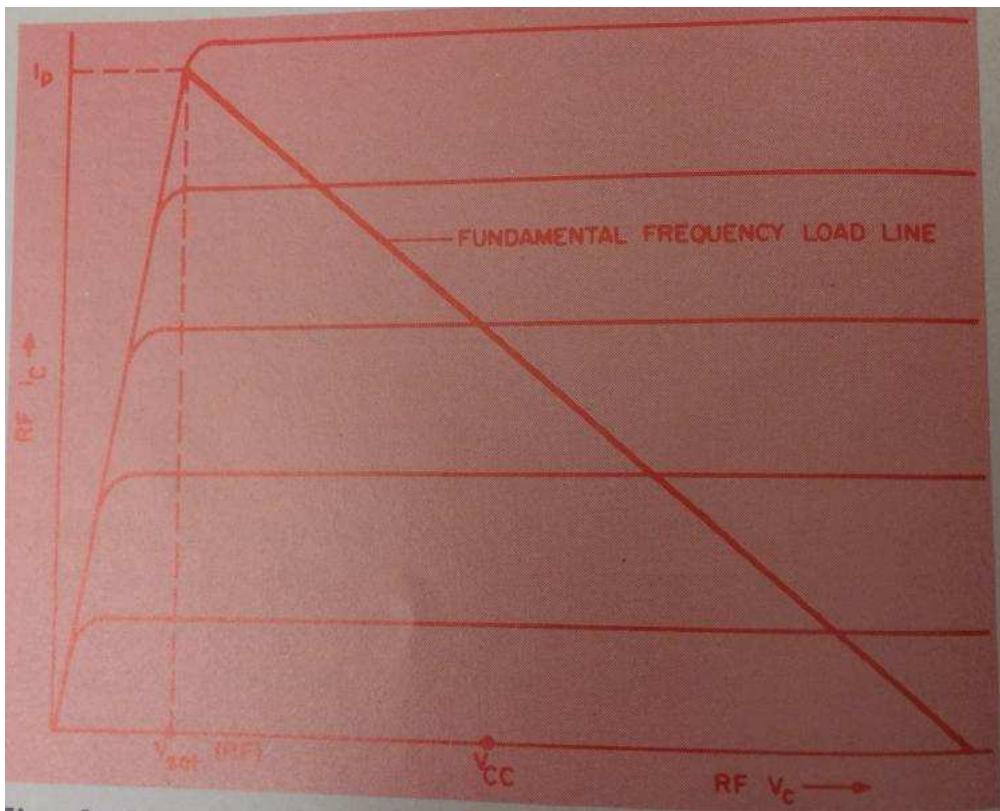


Fig. 8. Ideal Class-B load line for microwave transistors.

The ideal Class-B collector load line is shown in Fig. 8, where V_{SAT} is the rf saturation voltage—higher than the dc value. The relation between power output, V_{SAT} , and supply voltage is given by the equation:

$$P_{OE} = \frac{(V_{cc} - V_{SAT})^2}{2R_L (\text{Fundamental})}.$$

From this equation, the effects of V_{SAT} vs V_{cc} are shown in Fig. 9. It can be seen that V_{SAT} has a significant effect on the maximum power output capability of a transistor. Thus, this is an important parameter from the standpoint of both circuit design and device design and must be taken into account when calculating the required load line to achieve a given power output.

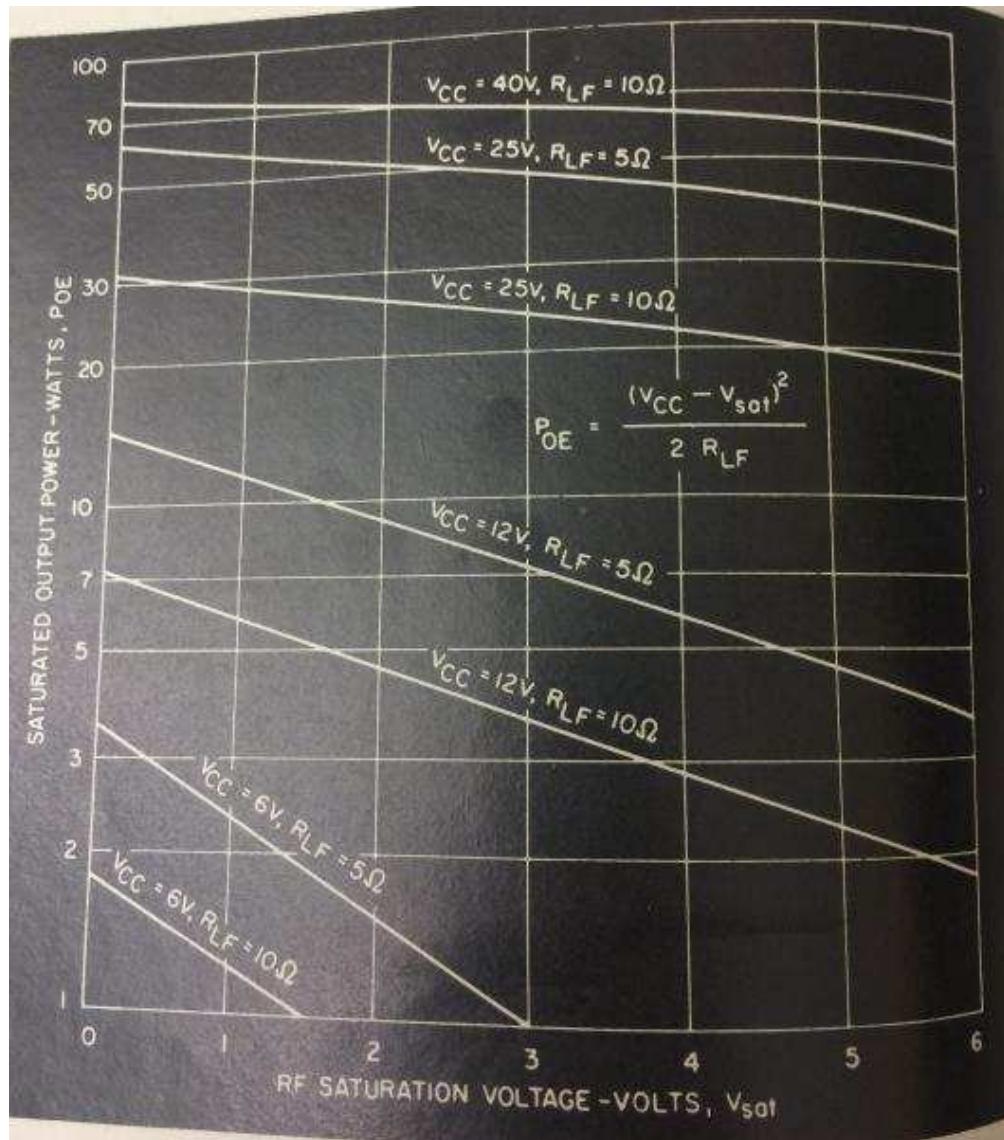


Fig. 9. How saturated output power varies with rf saturation voltage with typical microwave transistors.

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Microwave Transistor-Parameter Trade-offs in Circuit Design: Part 3

John G. Tatum

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November, 1967

For a specific transistor process and family, a very strong relationship exists between the dc beta, h_{FE} , and the high-frequency common-emitter current transfer ratio, h_{fe} . This is primarily because of a basic difference between a high- and a low-beta transistor in a given process with fixed doping levels: The base width is narrower in a high-beta device; i.e., the emitter diffusion time is longer or the epitaxial thickness is less. A high-dc-beta device will also have a greater high-frequency current gain.

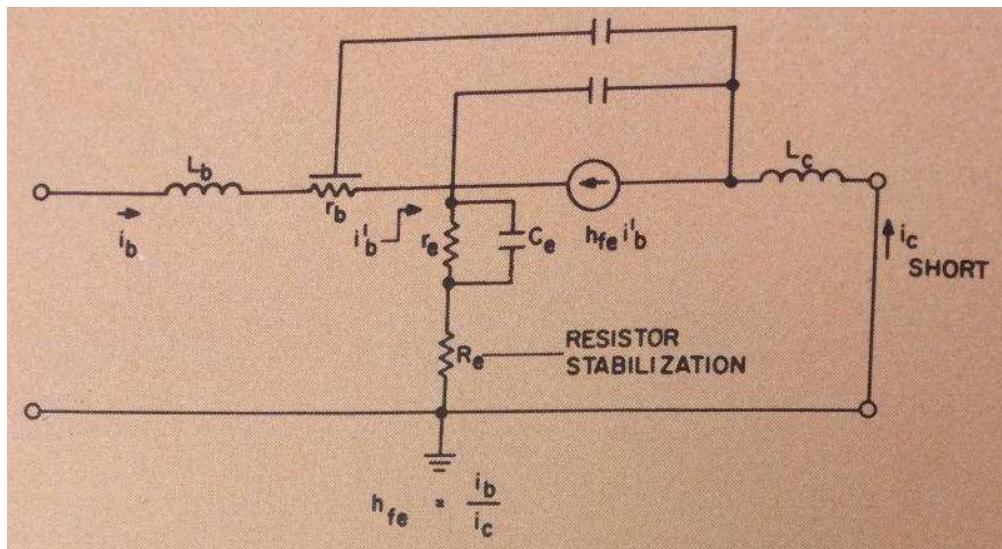


Fig. 1. Transistor-package circuit. This representation clearly shows that packaging has a significant effect on the performance of a transistor at microwave frequencies.

The external h_{fe} measurement is not necessarily the current gain of the internal device, since the measurement is made on the device in the package. A simplified model of the packaged transistor is shown in Fig. 1. Note that the capacitance distributed along the base resistance together with the other external capacitances will affect the short-circuit current gain of the device in the package. The package inductances and the resistance in the emitter structure will also affect the short-circuit current gain. Thus, the current gain of the package is not necessarily a good measure of the f_T or h_{fe} of the chip unless the reverse transfer admittance and other admittances are also measured and taken into account. This is an important consideration if the device is to be used for radiation resistance. Here a narrow base width is important rather than the effects of the package on the measurement of f_T , which is used as an indication of base width.

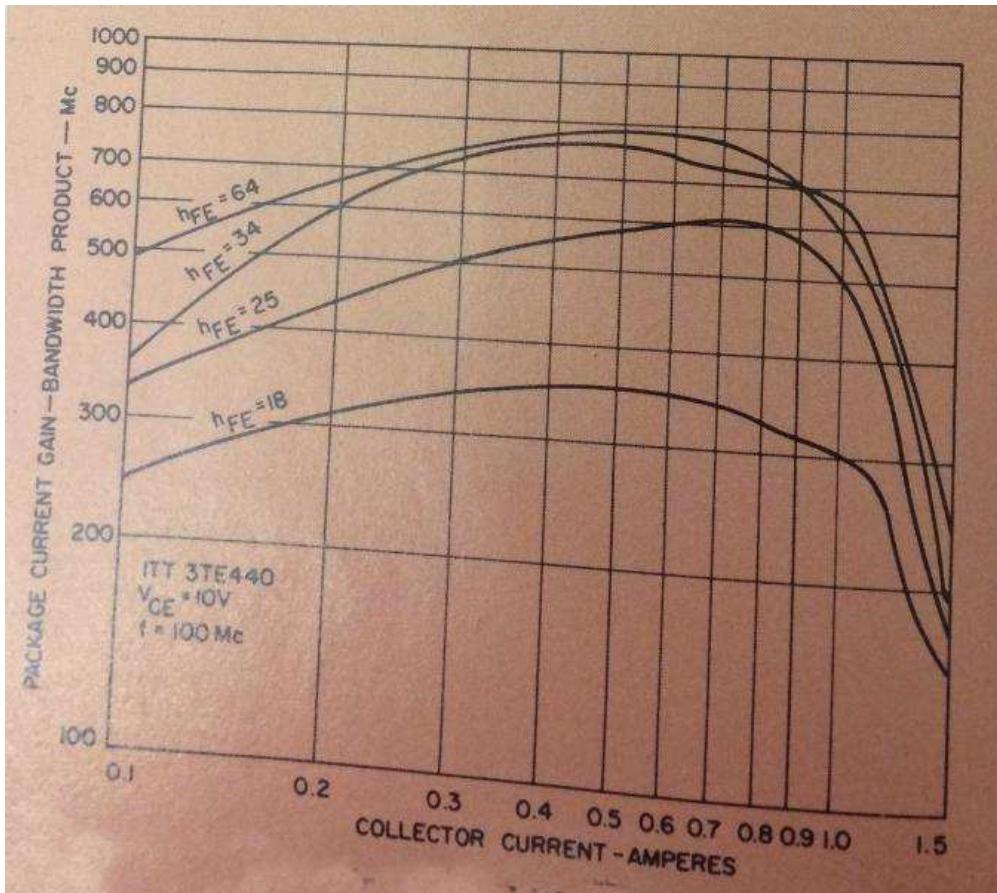


Fig. 2. Package gain-bandwidth vs collector current for various dc betas. A high-beta transistor with a low narrow base will exhibit current crowding at low current levels.

A high-beta transistor with a narrow base will exhibit current crowding at low current levels. The relationship between current gain-bandwidth product and collector current for different h_{FE} levels (for a resistor-stabilized device) is shown in Fig. 2. The current gain of the packaged device is considerably less than the current gain of the device itself. This is because of degeneration caused by the resistance introduced into the emitter structure. At a current level of about 1.1 A a sharp dropoff exists in hf current gain (as was true of dc current gain) and this is a result of current crowding. The maximum current rating of a transistor is specified in an area where the hf and lf current gains are still useful. This explains the 1.5-A max collector current rating for this transistor.

To keep within the most linear portion of the transistor characteristics, the average current within the device should be held no greater than 1 A. It can be seen that a low- h_{fe} device has less percentage change in hf current gain-bandwidth product than a high- h_{fe} device. This is also true for h_{FE} (or dc beta). The other variables which affect h_{fe} are primarily resistors introduced into the emitter circuits of resistor-stabilized transistors, and current distribution for equivalent betas. The transistors represented in Fig. 2 have been chosen for equivalent emitter resistance to eliminate this effect on measurement. Other important correlations to h_{FE} further validate the concept of what is happening in the base under the emitter.

Output admittance (y_{oe}) to h_{FE} relationship

Generally, a high- h_{fe} transistor and one of high-output capacitance have low real-output impedance. Actually, the output resistance at high frequencies in a small-signal analysis (simplified) approaches $1/(w_t C_o)$, where C_o is

nearly C_{ob} . Thus, it is expected that where current crowding and current distribution have little effect, a high-dc-beta device will have the lowest output impedance. This is so in Fig. 3, where the parallel-output resistance is lower at low currents for a high-beta device than for one of low-beta. The difference, nevertheless, is rather small; and at high current levels, variations in distribution of the current and current pinch-off effect will probably mask this tendency as it does for these curves.

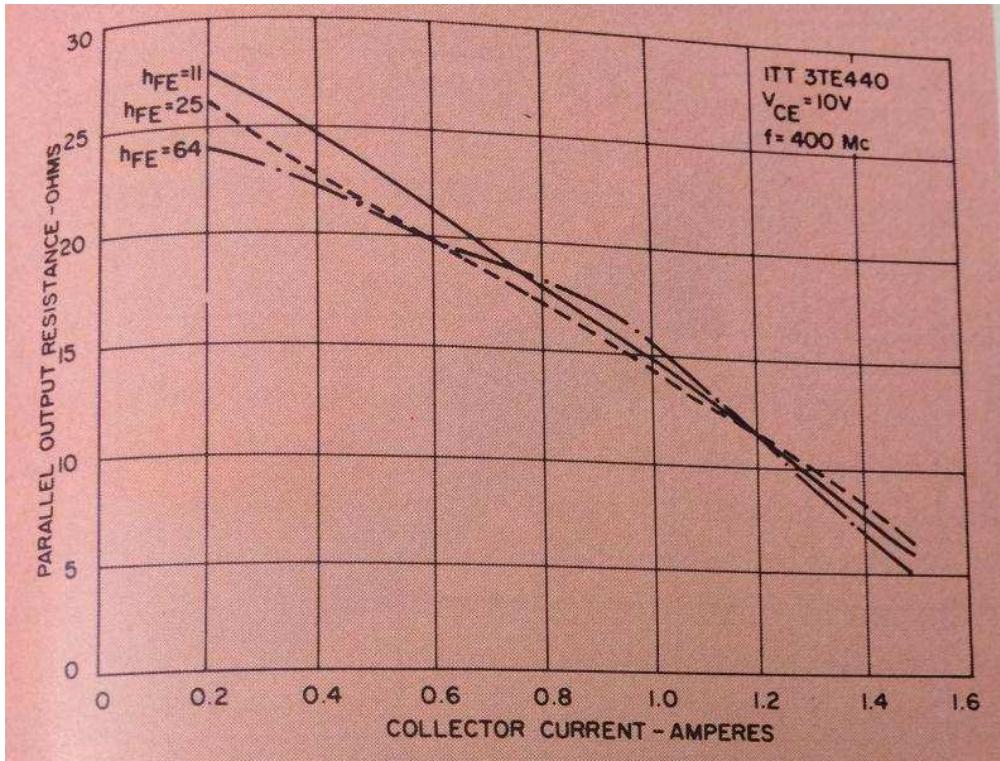


Fig. 3. Output impedance vs collector current curves show that the higher the dc beta the lower the output impedance, particularly at low values of collector current. The effect is not great, however.

It is important to note on these curves (which represent small-signal measurements of parallel output resistance) that output resistance decreases significantly as the collector current is increased. This provides a clue that the output resistance will be significantly lower in a large-signal circuit of an rf power amplifier than for the small-signal case or where the transistor drive level is low. Thus, the harder a transistor is driven, the lower the output impedance will become. Measurements of large-signal output impedance should bear this out. Output capacitance is fairly constant with current swing but not with voltage.

Collector breakdown-voltage differences will also affect the output impedance. For a single-type transistor, one with a higher BV_{CBO} than another (and thus a higher resistivity) will have a lower output capacitance and subsequently a somewhat higher output impedance. The trade-off, however, is that the higher the collector-base breakdown voltage (and thus the resistivity of the silicon material) the lower the saturated power-output capability of the transistor. This condition increases the saturation voltage level and reduces efficiency as a transistor multiplier.

Input impedance (Z_{in}) to h_{FE} relationship

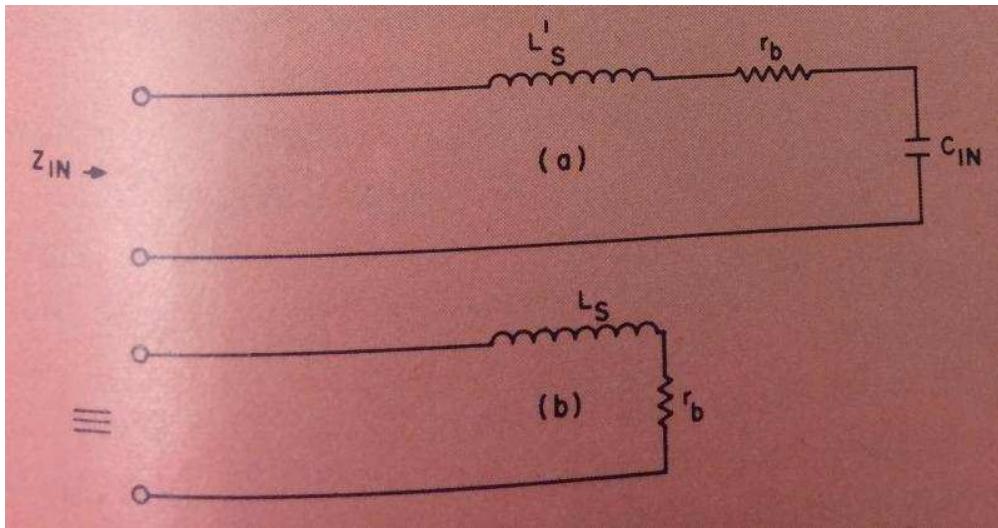


Fig. 4. Input circuit representations. Where the input capacitance is large, as for high-power transistors, the general circuit (a) can be simplified to that at (b).

The input impedance of a transistor at high frequencies can be represented by the simple circuit in Fig. 4a. Assuming the input capacitance is large, as for a high-power rf transistor, the circuit can be reduced to that of a series inductance and a base resistance shown at b. The input capacitance decreases as the dc beta of the device is increased as shown in Fig. 5. Therefore, the hf input inductance becomes effectively smaller as the dc beta becomes greater. This is because the capacitive reactance will be larger and cancel out more of the package and circuit inductance. This is shown in Fig. 6 where the effective small-signal series inductance decreases as the dc beta increases. The large-signal value will also be different from the small-signal value. The inductance due to the package itself is of fixed value.

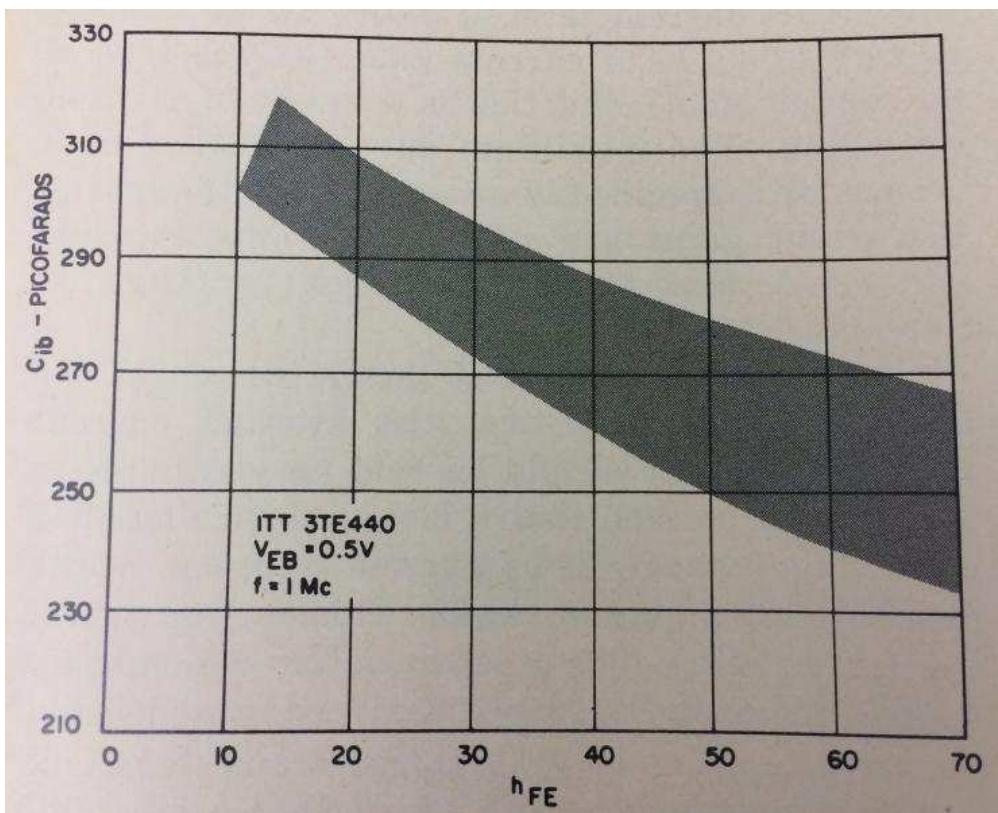


Fig. 5. Input capacitance vs dc beta. The capacitance decreases with increased beta, which means that the hf input inductance (Fig. 4b) becomes less as dc beta increases.

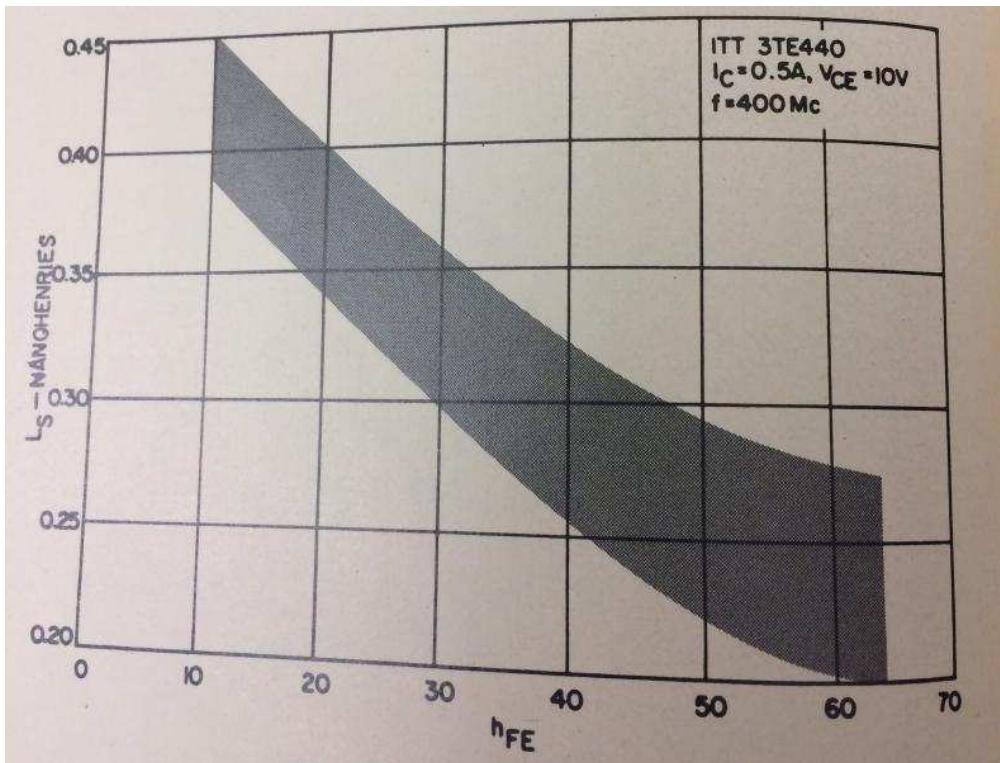


Fig. 6. Series input inductance vs dc beta (small signal). This phenomenon follows from the effect shown in Fig. 5 for input capacitance vs dc beta.

A high-dc-beta unit would be expected to have a higher base resistance since the lateral sheet resistance of the base under the emitter would be higher. The effect is fairly pronounced as shown in Fig. 7. The base resistance can increase by as much as 25 percent over the beta range of any transistor type. This is a small-signal base resistance and is lower in a large-signal condition.

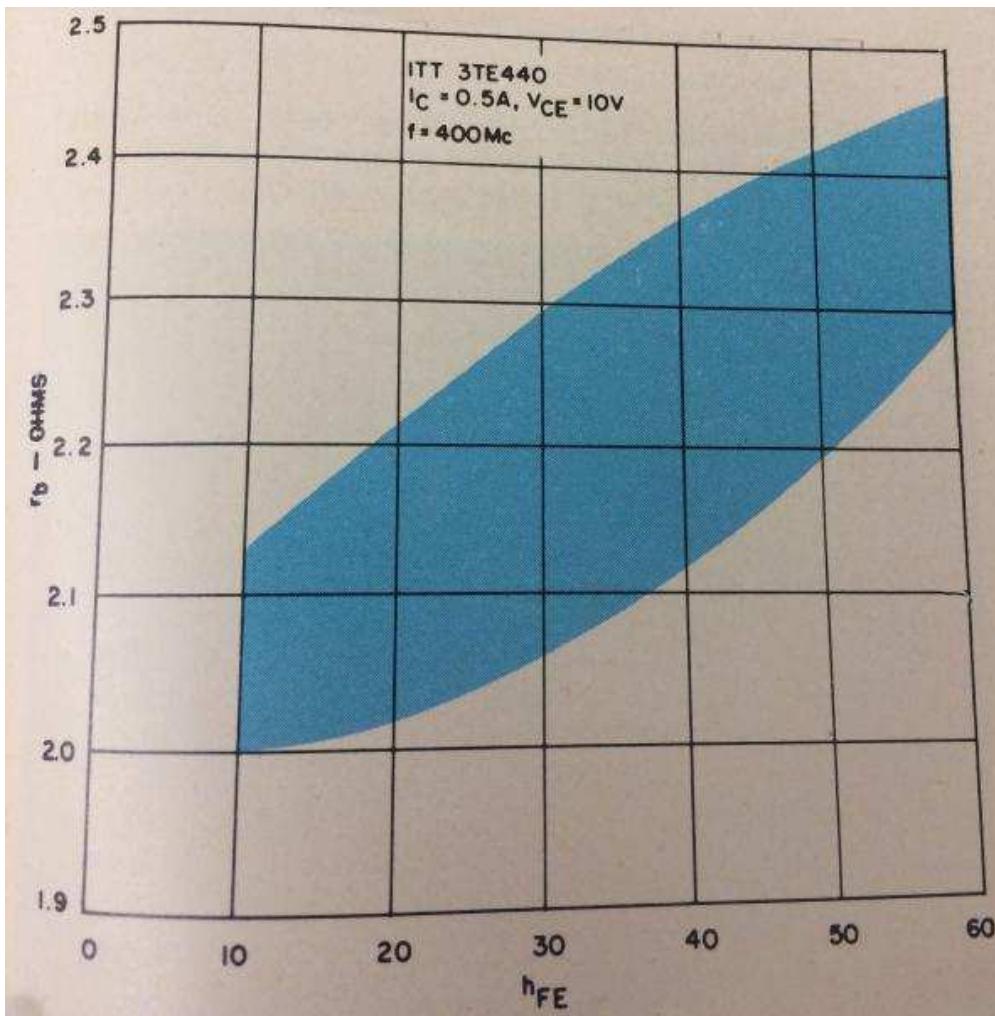


Fig. 7. Base resistance vs dc beta. The lateral sheet resistance of the base under the emitter increases with dc beta.

Trade-offs

From the curves it is assumed that a transistor with a high dc beta (and thus a high h_{FE}) is relatively easy to match since it has a high input resistance and a low input inductance. But, matching is a significant problem because high-power, hf transistors have a large-signal real input impedance in the order of 0.2-0.7 ohm for a 20-50-W device. The trade-offs involved with high dc beta are:

- A high-beta transistor has greater tendency to oscillate and at lower frequencies.
- It is more difficult to maintain a constant bandwidth as a function of a circuit layout.
- It will have lower saturated-power output, although it will have higher power gain at most frequencies.
- It will be a less linear device and thus will have higher intermodulation distortion and less dc bias stability for single-sideband circuits.

Input-impedance to collector-current relationships

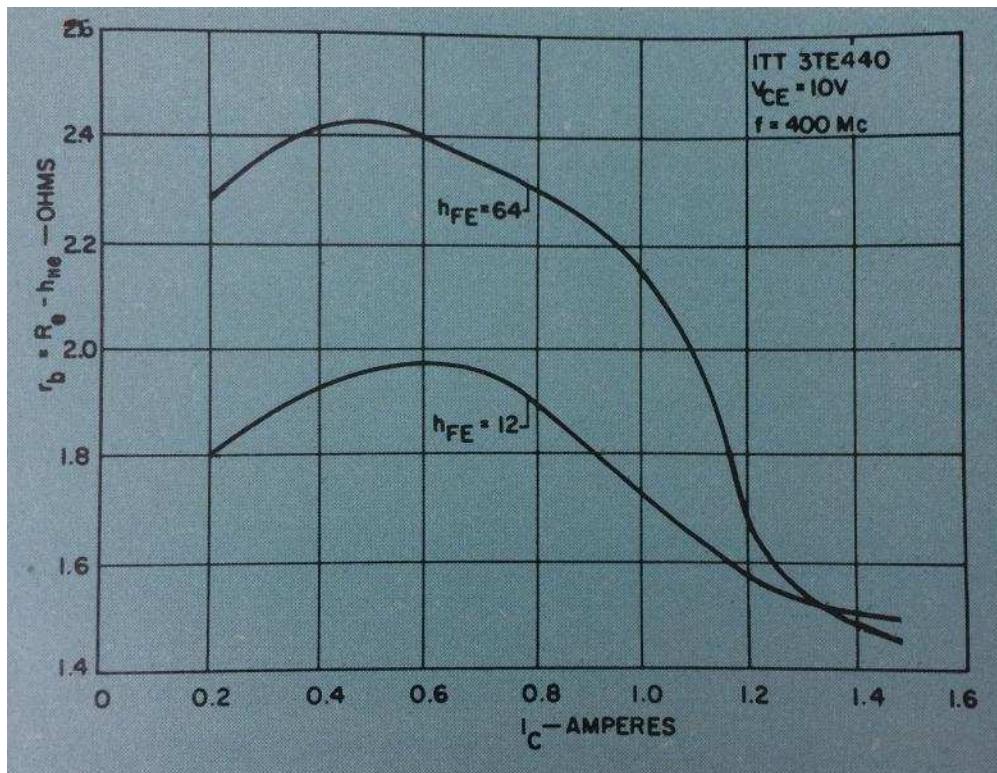


Fig. 8. Series base resistance vs input current. Note that lower dc-beta transistors have less variation in input resistance with current.

The input impedance should have less variation with collector current (or emitter current) if the device has a low dc beta. In Fig. 8 the series base resistance, r_b , (or real part of h_{11e}) has less variation with current for a low h_{FE} transistor. A definite similarity of the impedance-vs-current curve to the h_{fe} -vs-current curve exists. The same rapid change in resistance is observed in the same current region, as for dc beta and for h_{fe} . It is also apparent from these curves that the large-signal impedance will be much lower than the small-signal value. This impedance in a tuned circuit is also affected by the stored charge and how the charge is drawn out of the device in the "off" part of the drive cycle. This would have the effect of lowering the input impedance still further. These curves show that the harder a transistor is driven (such that the average and peak currents become higher), the lower the input resistance. Large-signal impedance measurements show this to be true.

The series inductance, L_s , would also be expected to show variations with collector current, since the input capacitance changes with current. Typically, the input capacitance of a transistor increases as the collector current increases. The input capacitance would also be affected by the current pinch-off effect. Also, one would expect a more rapid input-capacitance change in the same areas where there are rapid changes in the input resistance, h_{FE} , and h_{fe} . Since capacitance increases with current level, the effective series inductance would be expected to increase likewise. This is because there will be less capacitive reactance to subtract from the package inductance. The theory is borne out in practice as shown in Fig. 9, where a larger change in input inductance occurs for a high- h_{FE} device than one of low h_{FE} . Both curves show a tendency to have rapid changes in series inductance above 1.1 A where this correlates with the same rapid changes in other parameters and in h_{FE} itself. Inductance also increases with current. This corresponds with an increase in input capacitance with current. One must examine the combined effect of L_s and r_b to see how the input circuit Q and package bandwidth are affected by current and h_{FE} . Again, it should be noted that the large-signal input inductance will depend on the stored charge of the transistor and the class of operation. Thus, these curves can only give an indication of

which way the values will go. Typically, the large-signal values of these curves will be somewhat different from the high-current values.

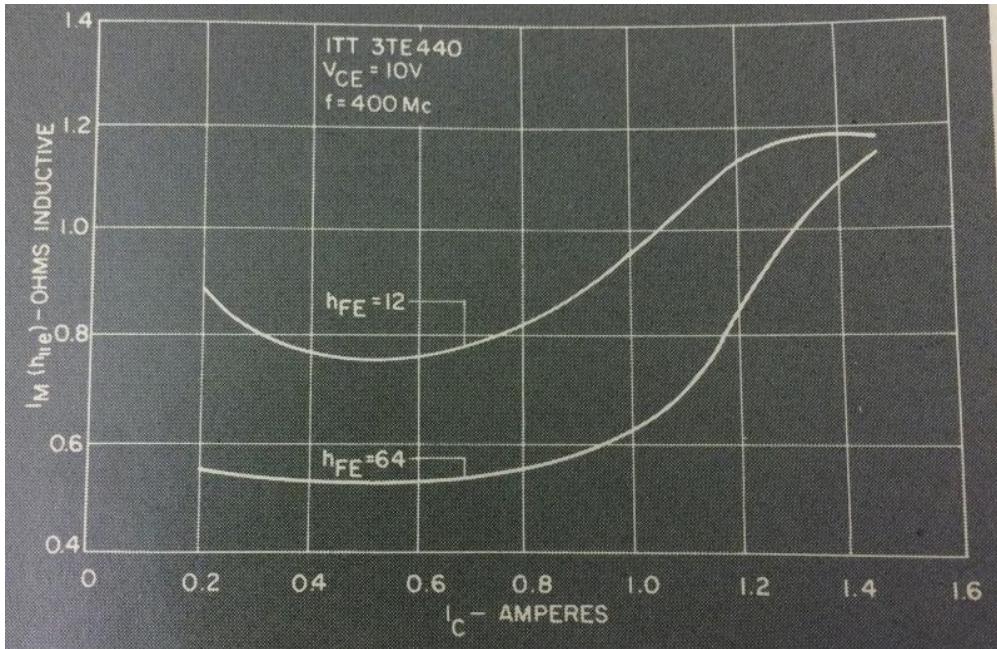


Fig. 9. Input inductive reactance vs collector current for low- and high-dc beta transistors. The low-beta transistor has less over-all reactance variation than the one with a high beta.

Package Q and sensitivity to series lead inductance

Bandwidth capability of the transistor, and thus package Q, are an important consideration and not only for those applications where bandwidth is important. A low-Q input to a transistor (a low reactive part relative to the real part) is important for ease of matching to the transistor; it also improves circuit stability. The package input Q doesn't determine the circuit bandwidth in itself. Other factors are the feedback effects of the load on the collector circuit and the degree of difficulty in matching to the low value of the input resistance. The higher the ratio of the source impedance to the real part of the transistor input impedance, the narrower the bandwidth; also, the more difficult it is to maintain the bandwidth when designing and cascading networks. A low package-input Q is of utmost importance as the first step in providing a good transistor for broadband applications and for ease in circuit design.

The circuit designer must connect the last element of the input matching network at some point external to the transistor package. This can't be done without some finite package lead length and added inductance beyond what appears at the input to the package.

To maintain the low package Q, it is necessary to have a shunt capacitance to ground from the package input or from a point near it. Thus, it is quite important for good circuit design that the input-Q sensitivity to a change in the added series inductance external to the package be rather small. The small-signal bandwidth is:

$$(1) BW = \frac{f_o}{Q} = \frac{r_b}{2\pi L_S}$$

The bandwidth sensitivity factor is defined as:

$$(2) S_B = \frac{d(BW)}{dL_S} = -\frac{r_b}{2\pi L_S^2} \text{ cycles/Henry}$$

This sensitivity factor gives a relative measure of the bandwidth lost when a series inductance is added using the small-signal short-circuit impedance measurements as the criteria. It can only be a relative factor, because bandwidth is also significantly affected by changes in input impedance caused by the load on the collector.

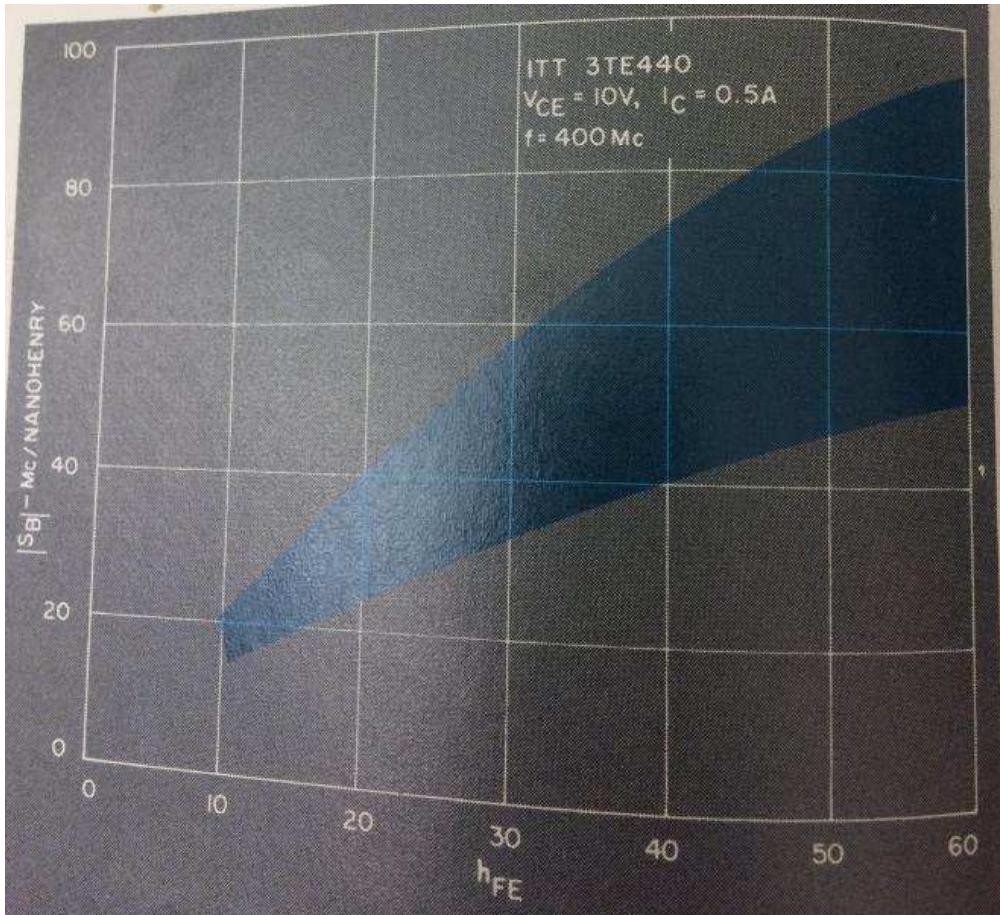


Fig. 10. Bandwidth sensitivity vs dc beta. One would choose a high-beta transistor for a high-input impedance for ease in matching and for lowest input Q.

Because the input impedance is a function of the transistor's dc beta, it is possible to plot a range of values for the sensitivity factor S_B vs h_{FE} , using the measured values of the small-signal input parameters. This plot is shown in Fig. 10. Over the normal beta range for a given device type, the sensitivity factor can vary all the way from 15 Mc/nH to 90 Mc/nH at the high-beta end. There is a significant trade-off here. One would like to choose a high-beta device for a high-input impedance for ease of matching and for lowest input Q.

This creates a problem in that the bandwidth sensitivity is a maximum for a change in series inductance brought on by packaging or placement of components. A middle-of-the-road compromise is to choose a mid-range beta. More work will be required with actual broadband loads and large-signal input-impedance and bandwidth measurements to determine what the actual sensitivity factor is in a direct circuit operating mode. But the small-signal analysis indicates the direction of the tradeoffs. The small signal package Q is:

$$(3) \text{ Package } Q = \frac{2\pi f_o L_s}{r_b}$$

Package Q is dependent upon the h_{FE} of the device. A typical median-range plot (Fig. 11) of many device measurements shows the approximate variation in package Q with h_{FE} . Because of differences in resistor stabilization values, transistor resistivity, and uniformity of current and power distribution over the device, package Q can vary over quite a broad range either side of this median curve for a given h_{FE} .

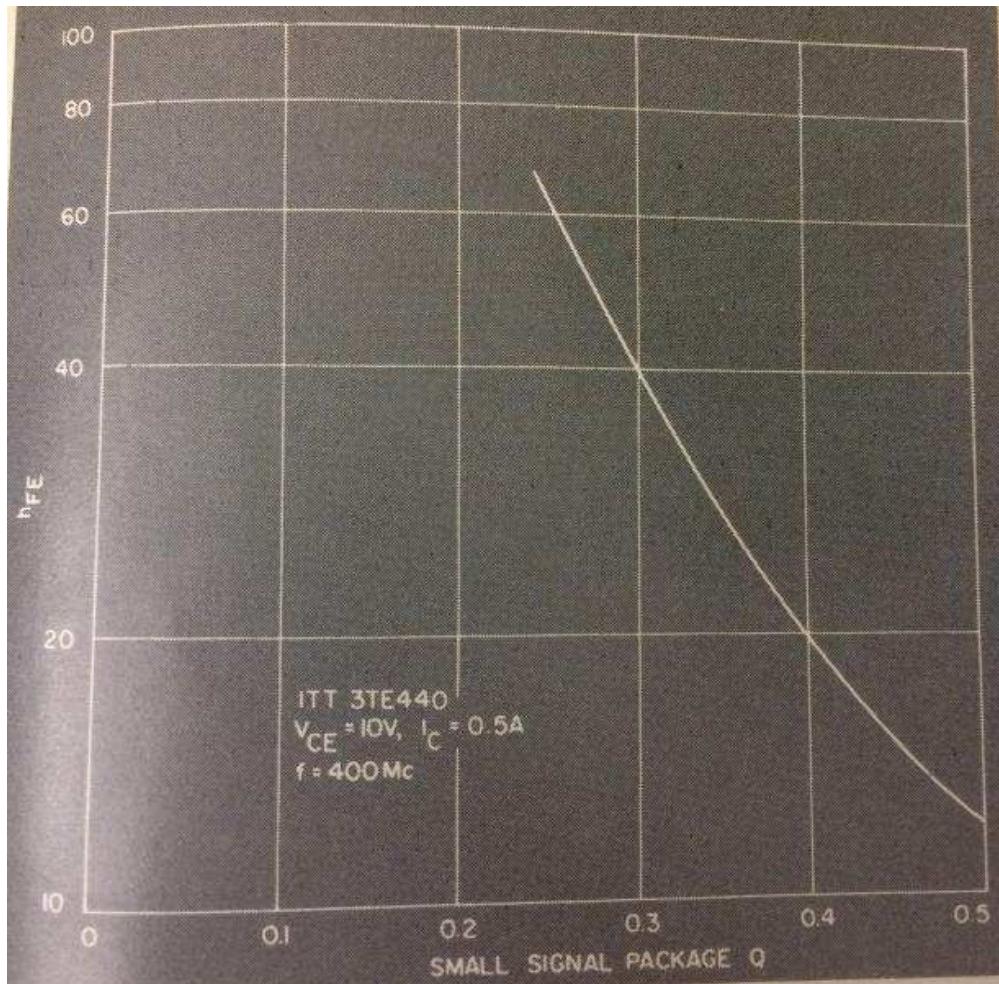


Fig. 11. How package Q varies with dc beta. Factors that affect this curve are resistor stabilization values, transistor resistivity and uniformity of current and power distribution over the device.

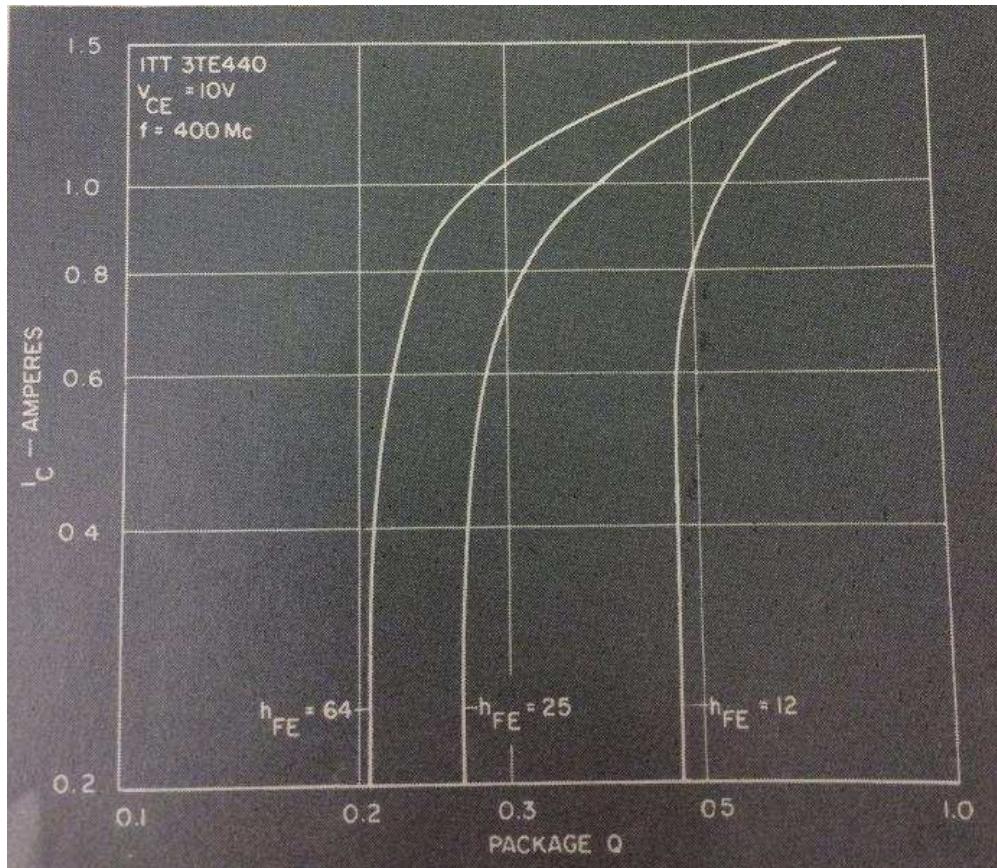


Fig. 12. Variation of package Q with collector current. Note rapid change in Q above the 1.1-A level.

Package Q is also a function of the collector current as shown in Fig. 12, and one would expect it to change even more rapidly as other parameters change at the same time.

Not the sharp change in package Q above the 1.1-A level for a 3TE440 transistor.

Large-signal input impedance measurements

When one compares the small-signal data so far plotted with large-signal measurements in an operating circuit, good correlation is observed. A setup for a 400-Mc large-signal input-impedance measurement, with a tuned and matched collector circuit load, is shown in Fig. 13. Test results are shown in Fig. 14. The slope of the r_b curve is sensitive to the heat sink employed. If a smaller heat sink were used, r_b would increase with P_{IE} . The large-signal r_b is seen to be lower in Fig. 14 than for the small-signal condition shown in Fig. 14 than for the small-signal condition shown in Fig. 8 as would be expected. The input reactance is less than the small-signal value due primarily to the effects of the feedback from the collector load. But the package Q is 3.4 – much higher than the small-signal value.

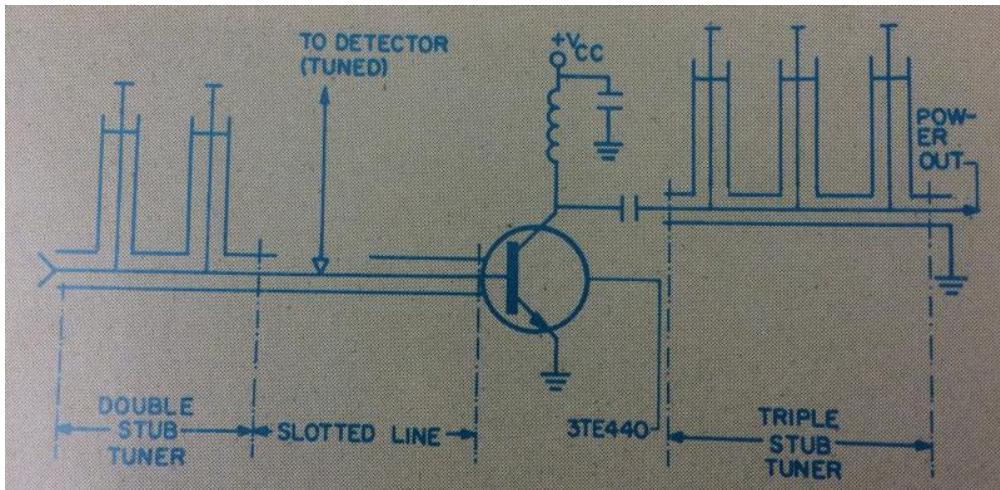


Fig. 13. Large-signal input-impedance test setup for 400-Mc measurement. Test results are shown in Fig. 14.

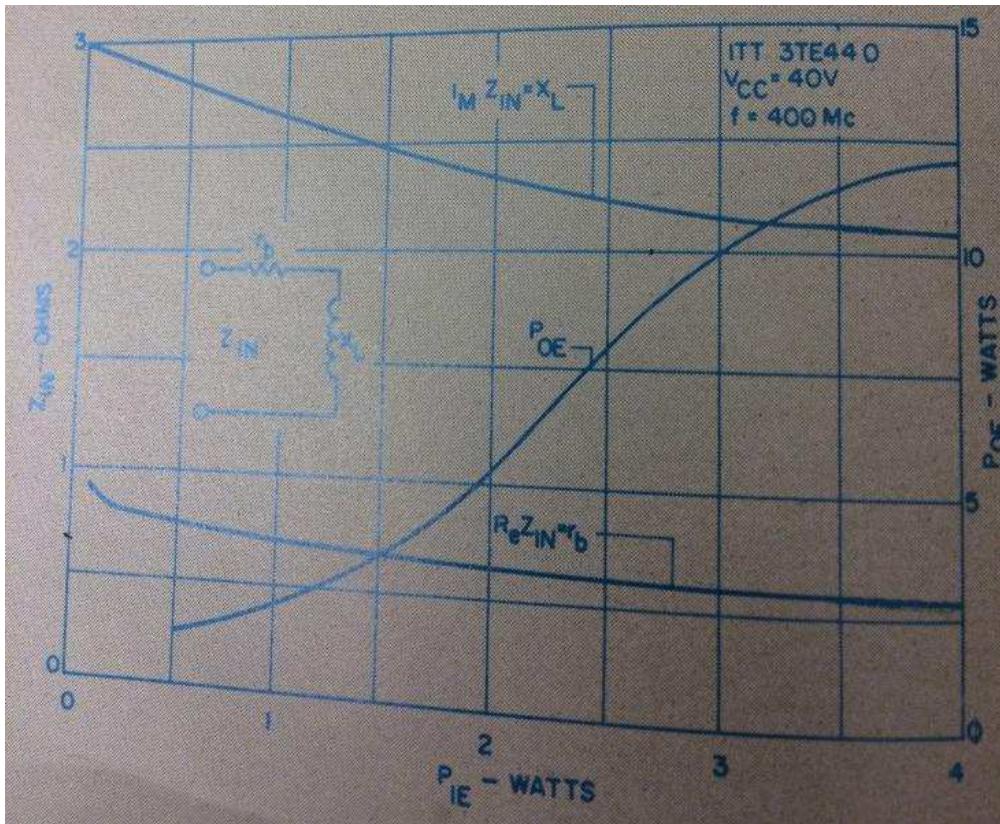


Fig. 14. Large-signal input-impedance curves. Note that the large-signal r_b shown here is considerably lower than for the small-signal case shown in Fig. 8.

Power gain as a function of transistor parameters

A significant trade-off between power gain and the other required transistor parameters exists for each particular circuit operation. Power gain is a function of frequency, and at high frequencies approximates 6 dB/octave roll off. The lower the frequency where a transistor is used, the greater the sensitivity of power gain to h_{FE} . At quite low frequencies, as expected, power gain is controlled more by the h_{FE} of a transistor than by other basic parameters. A 400-Mc transistor, for instance, demonstrates this phenomenon as shown in Fig. 15, when operating at the lower frequency of 250 Mc. A large lot sampling of the devices at this frequency gives the

distribution shown. Obviously, low-beta transistors have significantly lower gain than those with high beta. The range is roughly from 6 to 10 dB for the normal h_{FE} range of a device family. Thus, there is a significant trade-off between the power gain that can be expected and the other required device parameters which correlate to h_{FE} .

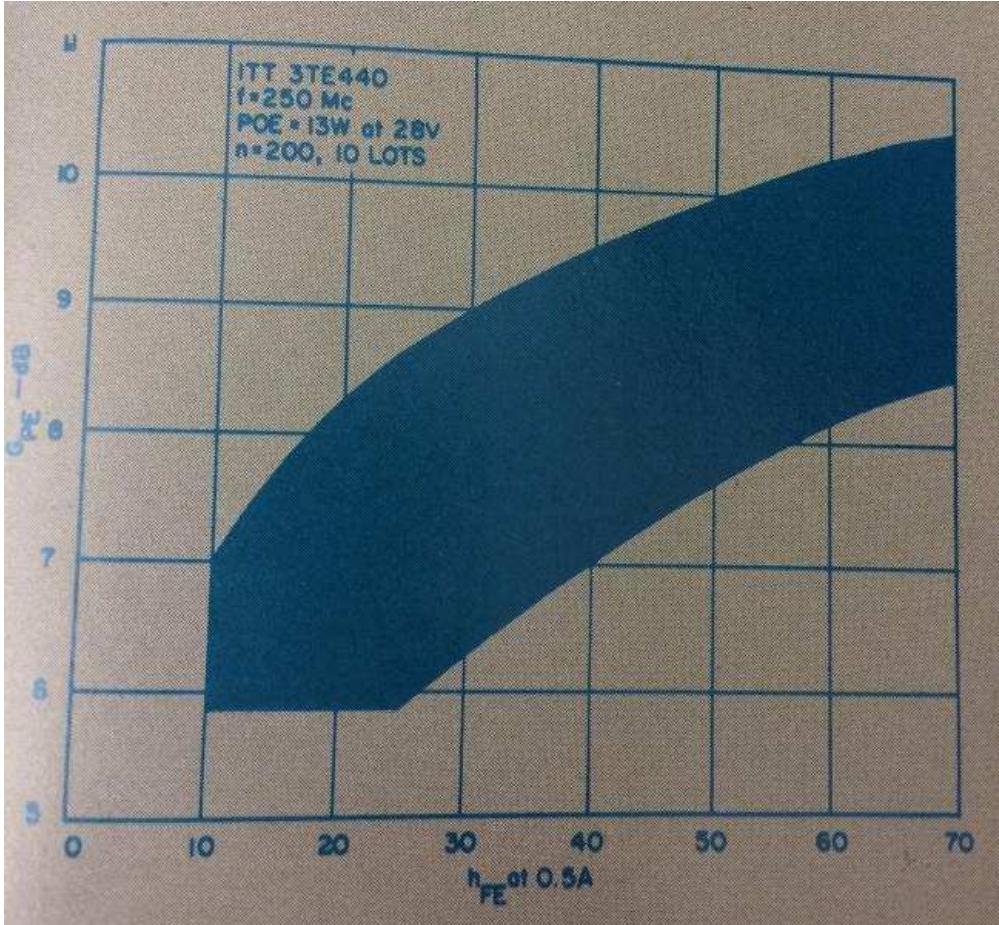


Fig. 15. Power gain vs dc beta. At lower microwave frequencies, the power gain is controlled more by h_{FE} than by other parameters.

In addition to correlation of power gain to h_{FE} , it would also correlate to $V_{CE(SAT)}$. This is especially true where high $V_{CE(SAT)}$ devices are caused by either non-uniform current distribution or (for resistor stabilized devices) higher value resistors in the emitter.

Saturated power output trade-offs

Saturated-power output capability is a significant and often overlooked characteristic of a power transistor. Among those presently marketed by many manufacturers, there is a wide range between the saturated-power-output capability and the specified power-output capability. Many designers tend to design around the saturated-power output if they can obtain this saturated power output without exceeding the dissipation limits of the transistor. In addition, the power a transistor dissipates under a high VSWR load condition is partially a function of saturated-power output capability. A significant trade-off exists between saturated power output capability and h_{FE} . This is because of the current pinch-off effect under the emitter as previously described, where current peaks are more difficult to obtain with a high h_{FE} .

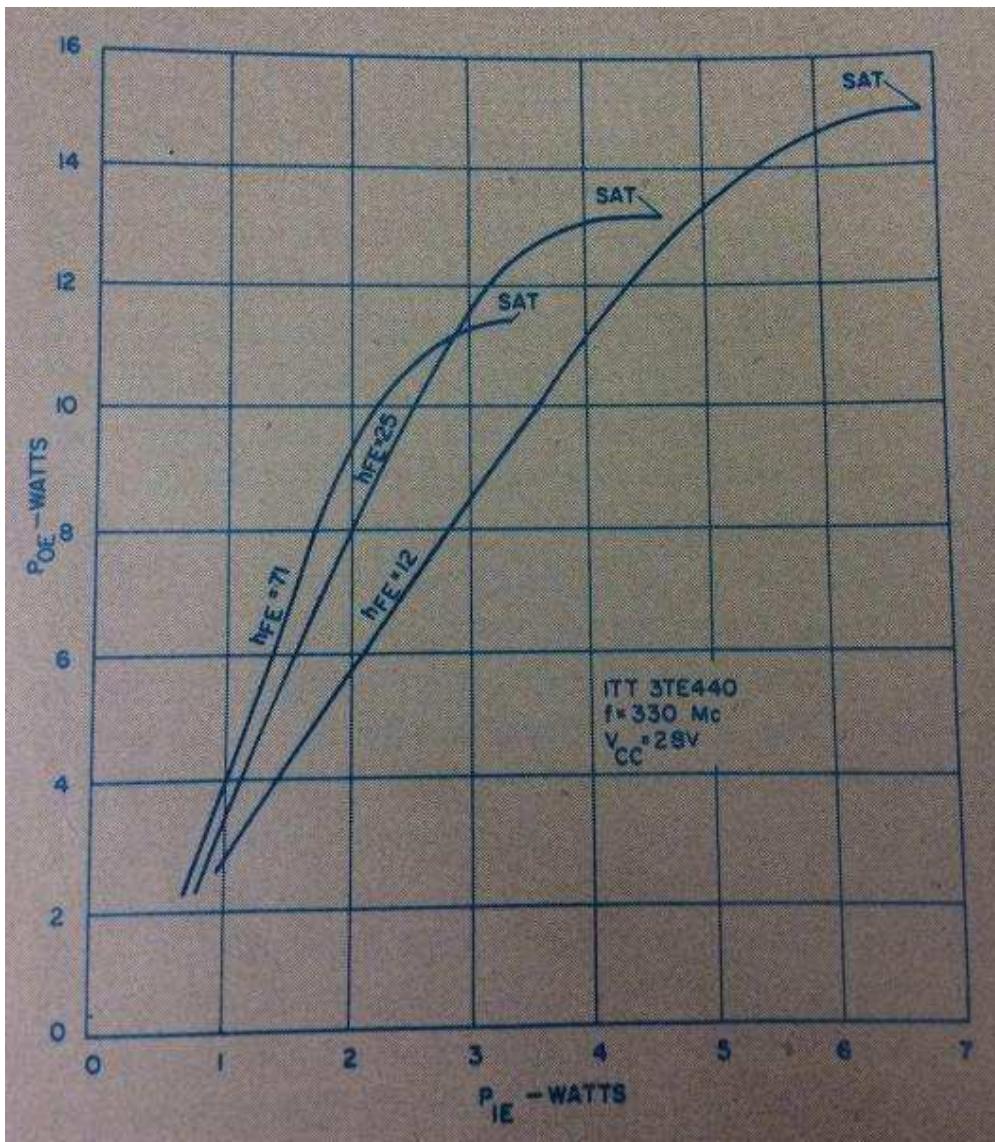


Fig. 16. Gain saturation curves at 330 Mc. The lower dc beta transistors show significantly higher power gain.

Thus, device saturation would be expected at a lower level. Measurements of a device family, selected such that other parameters which affect saturated power output are equivalent in all devices at 330 Mc, are shown in Fig. 16. Here, a low h_{FE} device has a significantly higher output level than one having high h_{FE} . Also, note the differences in power gain as a function of h_{FE} .

Another trade-off in the saturated-power output is with $V_{CE(SAT)}$. The higher the V_{SAT} the lower the saturated-power output for a similar h_{FE} . Table 1 shows roughly the trade-off between $V_{CE(SAT)}$ measured at dc and at saturated P_{OE} (the rf V_{SAT} will be considerably higher but will also correlate). This is done on a high h_{FE} unit to emphasize the correlation. A lower h_{FE} device would not be quite as sensitive to the trade-off.

Table 1. Correlation of $V_{CE(SAT)}$ to $P_{OE(SAT)}$ (For $h_{FE} = 60-65$ units)

Unit	$V_{CE(SAT)}$ (V)	$P_{OE(SAT)}$ (W)

1	0.70	13.5
2	0.70	13.5
3	0.72	13.4
4	0.75	13
5	0.75	12.8
6	0.75	12.5
7	0.85	12.5
8	1.0	10.5

Saturated-power output would also correlate to the BV_{CEO} transistor breakdown voltage because a high BV_{CEO} would indicate a high resistivity collector. This, in turn, would indicate a higher V_{SAT} or a lower saturated-power output. However, as previously noted, a high BV_{CEO} unit would have less C_{OB} and more power gain. The trade-off between all of these parameters becomes somewhat complex.

Thermal effects, resistor stabilization and trade-offs

The concept of resistor stabilization was introduced over two years ago for the express purpose of making a large-area hf silicon transistor operate uniformly and maintain a safe operating area. The concept that a high-power, hf transistor is nothing more than many small-signal transistors in parallel is a good premise to begin from. If this is true, and if differences exist in thermal dissipation of the device area plus differences in base width (and thus gain of some small transistors), a significant non-uniform distribution of current and power density over the large area of the high-power device exists. This is accentuated by the fact that a hf device has a high density of small transistors in parallel.

It is a well-known fact that if a bipolar transistor is heated up its gain will increase. Thus, the chip area that carries the most current will tend to heat up more than the surrounding areas and carry more of the load until it will blow itself out in that small area or “hot spot.” An obvious and direct method to equalize the current uniformity and power density is to put a small emitter resistor in series with each transistor. Such a large-area “resistor-stabilized” device operates more uniformly.

An increasing number of resistor-stabilized transistors are being introduced by semiconductor manufacturers. Thus, it is important to understand the trade-offs involved between resistor stabilization, thermal capability and

operating characteristics of such devices. Since resistor stabilization is a form of emitter degeneration, power gain is degenerated as well. This is one of the more important trade-offs between thermal capability, safe-operating area and power gain. The higher the resistor stabilization, the lower the power gain. Thus, for a given power density and area, it sometimes is necessary to put a higher-gain device in for the same amount of resistor stabilization to maintain a useful over-all power gain. The more resistor stabilization is introduced, the higher the $V_{CE(SAT)}$ will be and the lower the saturated power output. This is a trade-off which is controlled by the manufacturer rather than the circuit designer, but it is an important one for the circuit designer to understand.

If device thermal resistances are compared, it is found that for a similar device type those with lower resistor stabilization will have a higher thermal resistance and less thermal dissipation capability. The significant trade-off here is one which relates power gain to saturated power output and VSWR capability (improved by resistor stabilization). Future devices will have improved forms of resistor stabilization structures built in, making these trade-offs less critical than at present.

Another plus feature of resistor stabilization is improved dc bias capability. This is combined with improved intermodulation distortion in single-sideband applications.

Thermal resistance and how to measure it

Contrary to the normal circuit-design concept, there is no such thing as a fixed thermal resistance for a transistor. Thermal resistance is normally defined as the temperature rise between the junction and the case per watt of dissipation. Because current uniformity (and thus power density) is a function of the current level as well as the collector supply voltage (or thus the power level in the transistor), one would expect thermal resistance to be a nonlinear function of these circuit parameters. Typically, current distribution is more uniform at low-current levels and is also more uniform at lower voltages. Thus, for a given transistor type, the low-voltage, low-current area will give the lowest value of thermal resistance. It is also to be expected that where one small area of the device tends to go into thermal runaway (i.e., has a negative slope of the base-emitter voltage vs collector current for a fixed collector voltage), that runaway will cause current from one area to suddenly shift to the area which is trying to carry more of the load. At this point, the active area of the transistor is effectively reduced resulting in high thermal resistance. This shows up as a sudden shift in a thermal resistance plot, as shown in Fig. 17. This plot of thermal resistance vs collector current as a function of dc collector-emitter voltage, is for a microwave transistor, type 2N3375. It substantiates that thermal resistance is a nonlinear function of these parameters, is much lower at low-current, low-voltage levels, and has discontinuities associated with sudden shifting of current and power density in the device. These effects, which are measured at dc, correlate reasonably well with the rf-power capabilities as well. Thus, it is important that the circuit designer be aware that thermal resistance is a function of the measurement conditions under which it is specified. Unfortunately, the conditions are very seldom specified on data sheet.

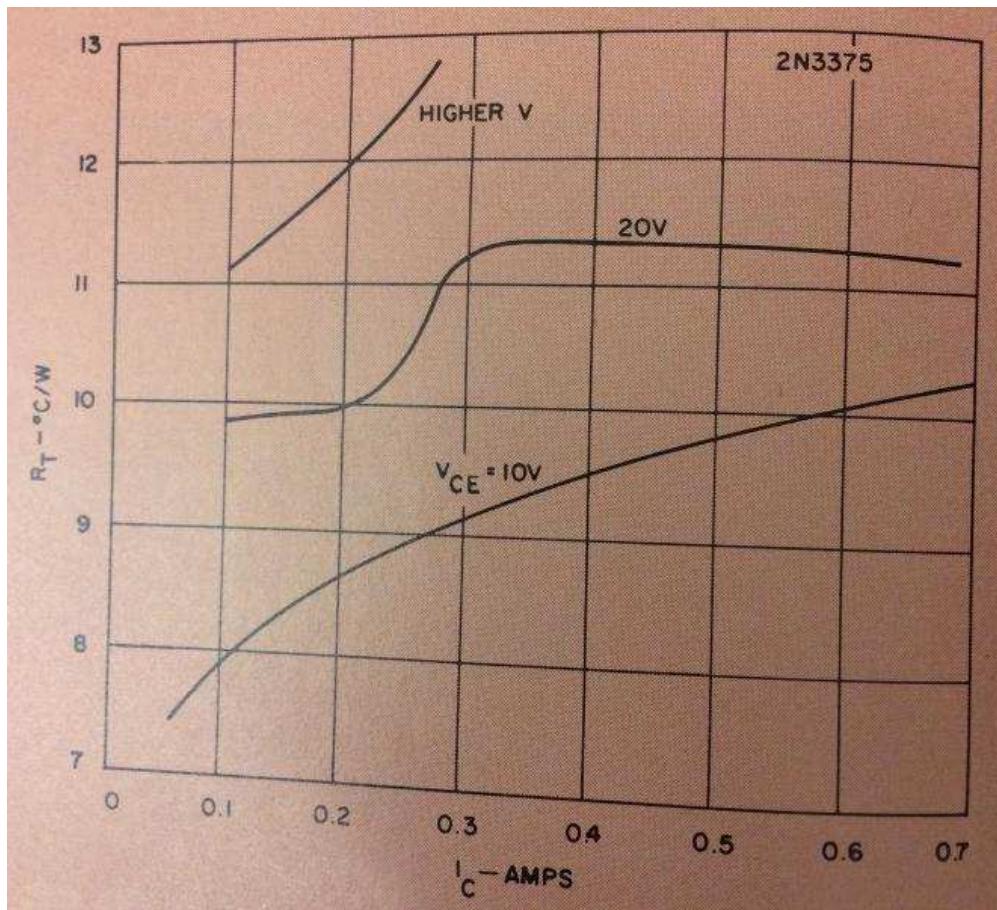


Fig. 17. How thermal resistance varies with collector current. The effect is nonlinear and much lower at low-current, low-voltage levels.

Because thermal resistance is a function of V_{CE} and I_C , it would be expected that the safe operating area under pulsed conditions would be a function of these parameters as well as the thermal time-constant of the device itself. If the safe-operating area under pulsed conditions is defined as that point at which some part of the junction area of the transistor reaches 200°C and pulsed measurements are then taken, safe operating curves are shown in Fig. 18, result.

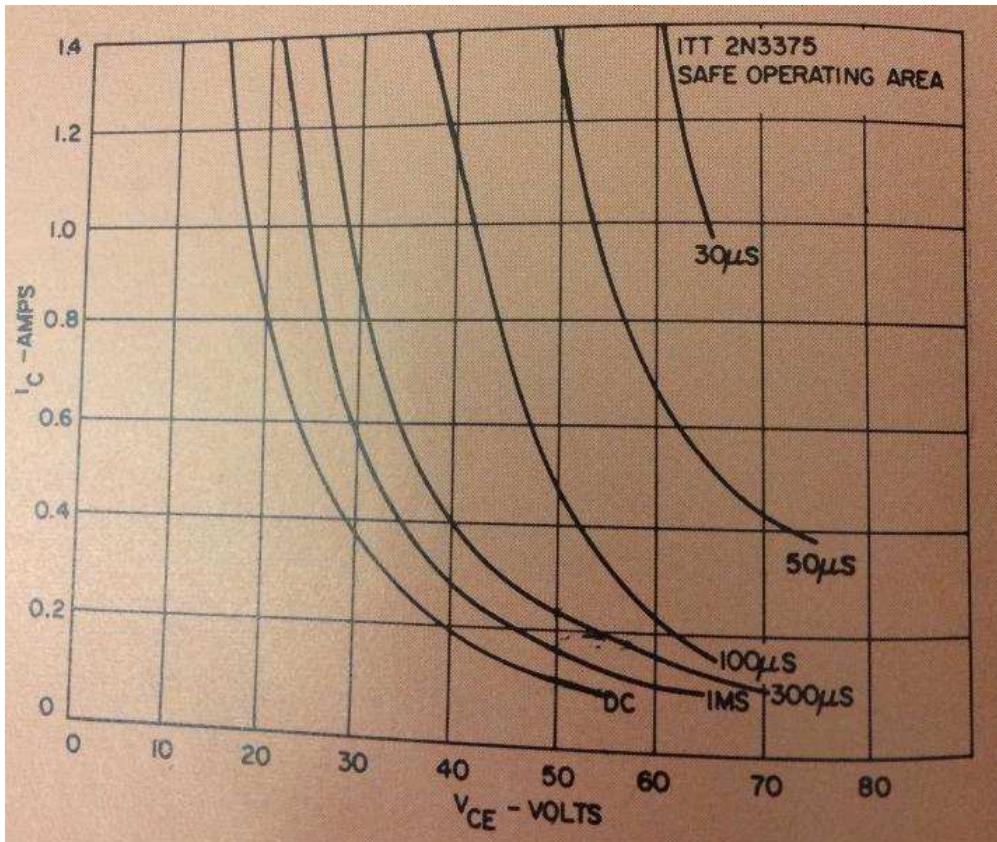


Fig. 18. Safe-operating pulse conditions for a typical microwave transistor. These curves are based on the transistor junction area not exceeding $200^\circ C$.

VSWR capability, or the ability of a transistor to withstand a high VSWR load (i.e., approaching or equal to an open- or short-circuit condition) is an important consideration and correlates to some of the other transistor parameters. High-VSWR capability can relate closely to a transistor's dissipation capability. Through part of the VSWR phase angle, the transistor must dissipate more power than in matched condition. Thus, a resistor-stabilized device, or one with a higher safe-operating area, can withstand this VSWR load better. The other trade-offs to obtain this capability are already apparent. Also, a device with a lower saturated-power output tends to limit its peak current more. Thus its total power dissipation is somewhat less. This is another direct trade-off between VSWR capability and the device itself. In the other phase of VSWR, a high-voltage, low-current condition exists on the collector. Here, a high-voltage break-down requirement and a sustained-high-current capability in avalanche are important. The trade-offs of high-voltage capability have already been discussed. However, high-avalanche sustaining-current capability has been difficult to relate directly to other basic device parameters that a circuit designer measures. It must be designed into the transistor.

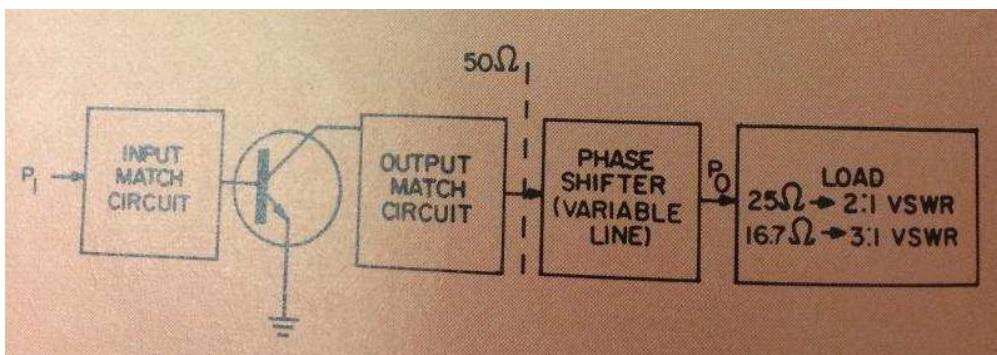


Fig. 19. Basic VSWR test circuit. Using this test setup one can measure the variation in transistor power dissipating, power output and collector current as a function of phase length between output circuit and load.

A typical variation in transistor power dissipation, power output, and collector current as a function of phase length between the transistor-output circuit and the load can be measured as shown in Fig. 19, with results as shown in Fig. 20 when adjusted for line losses. These curves illustrate how the phase between the output circuit and the VSWR load is important in determining what is happening at the transistor.

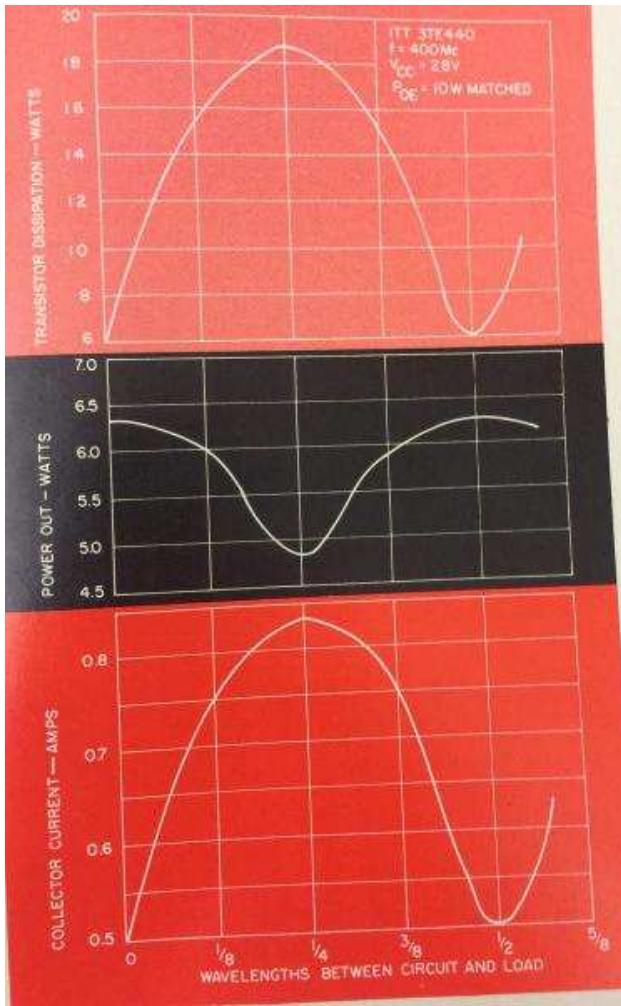


Fig. 20. Test results from setup of Fig. 19 show how the phase between output circuit and load is important in determining events at the transistor itself.

Summary

It is important for the circuit designer to have a basic understanding of what is happening inside the semiconductor device to better understand its performance and the significance of circuit measurements. Much correlation exists between basic device parameters, which are easily measured prior to rf testing, and the characteristic performance of a device in its rf power-test circuit. With a reasonable knowledge of the basic relationships, the designer can estimate the performance of a given circuit for a distribution of device parameters. Much more work needs to be done to further characterize device parameters as related to circuit performance especially as it involves large-signal impedance measurements and hf breakdown characteristics as well as safe-operating area in an rf circuit. An attempt has been made in these three articles to show the relationships and trade-offs as they are understood today. The general ideas presented hold true for any device

of the planar epitaxial type of construction regardless of the geometry or type.

References

Part 1:

John Tatum, "RF Large-Signal Transistor Power Amplifiers: Part I- Theoretical Considerations," *EDN, Cahners Publishing Co.*, (May, 1965).

Part 3:

E.O. Johnson, "Physical Limitations of Frequencies and Power Parameters of Transistors," *RCA Review*, Vol. XXVI, No. 2, (June, 1965), pp. 163-173.

D.M. Smith and G.D. Vendelin, "High Frequency Silicon Power Transistors: Characteristics and Applications," Texas Instruments Seminar Bulletin.

John Tatum, "RF Large-Signal Transistor Power Amplifiers: Parts I, II, III," *Electrical Design News*, (May, June, and July, 1965).

John Tatum, "Circuit Improvements Utilizing the New Resistor Stabilized VHF Transistors," *Proceedings of the National Electronics Conference*, Vol. XXI, (1965).

John Tatum, "UHF/SHF High Power Solid State Device Improvements," *Proceedings of the Southwestern IEEE Conference*, (1965).

C.R. Turner, "Interpretation of Voltage Readings for Transistors," *RCA Application Note SM A-2*, RCA Electronic Components and Devices.

H.E. Schauwecker, "Understanding Transistor Voltage Breakdown," *Electronic Design*, (July 22, 1959), pp. 28-30.

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APPENDIX II-4

TRANSISTOR BASICS

High-Frequency Transistor Primer

Part I

Silicon Bipolar Electrical Characteristics

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Preface

Transistors have been used at frequencies above 1 GHz since about 1960. The technology has increased such that both circuit and project engineers look to transistors for new system requirements at frequencies up to millimeter wave. The purpose of this primer series is to introduce microwave designers to the terminology used in describing the characteristics of high-frequency transistors. An understanding of the capabilities and limitations of these transistors should result in better performing, more reliable circuits.

This volume, Part I, covers general device electrical characteristics for silicon bipolar transistors. Volume II covers general noise and S-parameter characterization. Part III covers device thermal properties and Part IV covers GaAs FET device parameters and measurements.

Introduction

This primer is a short glossary and brief explanation of transistor terms commonly used in Agilent Technologies transistor data sheets, advertisements and other technical communications. Some of these terms are simple, virtually self-explanatory and are included here primarily for the sake of completeness. Others are more specialized and potentially ambiguous due to a lack of terminology standardization in the high-frequency transistor area. These latter types receive more treatment here.

I. Transistor Structure Types

All current Agilent Technologies silicon transistors are of the bipolar NPN planar epitaxial type. Briefly, the significance of each of these terms is as follows:

A. Bipolar

In its broadest sense it is the basic structure shown schematically in Figure 1, i.e., the familiar three semiconductor-region structure. Bipolar specifically means that the charge carriers of both negative (electrons) and positive (holes) polarities are involved in the

transistor action. In way of contrast, unipolar types include the junction-gate and insulated-gate field-effect transistors which are basically one- or two-semiconductor-region structures in which carriers of a single polarity dominate.

B. NPN

An abbreviation for *negative-positive-negative* which identifies the regions of the structure as to polarity of the dominant or majority carrier in each region. The other polarity type is PNP. (See Figure 1.)

C. Silicon

Silicon is one of two elements from the fourth column of the periodic table which are in widespread use for transistor fabrication (the other is germanium). Other materials used include the compound gallium arsenide. Silicon is in predominant use because it results in the most favorable compromise among high-frequency, high-temperature, high-reliability and ease of use attributes of the usable semiconductor materials.

D. Planar

A term which denotes that both emitter-base and base-collector junctions of the transistor intersect the device surface in a common plane (hence, a better term might be co-planar). However, the real significance of the so-called planar structure is that the technique of diffusing dopants through an oxide mask, used in fabricating such a structure, results in junctions being formed beneath a protective oxide layer. These protected junctions are less prone to surface problems sometimes associated with other types of structures, such as the mesa.

E. Epitaxial

This term, as it is commonly used, is actually a shortening of the term epitaxial-collector. That is, the collector region of the transistor is formed by the epitaxial technique rather than by diffusion which is commonly used to form the base and emitter regions. The epitaxial layer is formed by condensing a single-crystal film of semiconductor material upon a wafer or substrate which is usually of the same material. Thus, an epitaxial (collector) transistor is one in

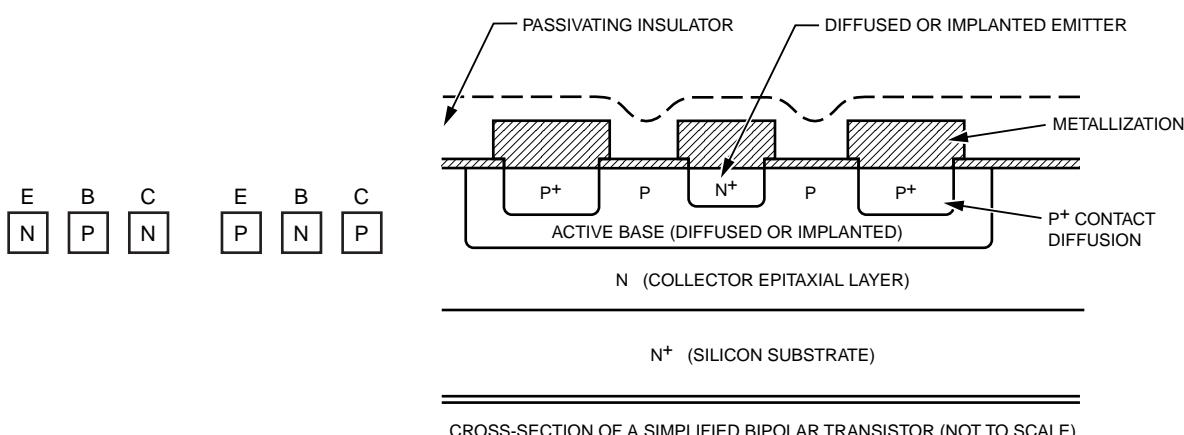


Figure 1. Transistor Structure Schematics

which the collector region is formed upon a low-resistivity silicon substrate. Subsequently, the base and emitter regions are diffused into the "epi" layer. The epitaxial technique lends itself to precise tailoring of collector-region thickness and resistivity with consequent improved device performance and uniformity.

II. Maximum Ratings

Maximum ratings may be defined as limiting values of externally applied stresses (voltage, current, temperature, etc.) normally under control of the user which if exceeded may result in irreversible damage to the device. The user who exceeds the maximum ratings does so necessarily at his own risk. These ratings are set by the manufacturer on the basis of many considerations such as life tests, breakdown voltages, etc., in order to define to the user certain operating conditions which are safe for each and every transistor of a given type.

Unfortunately, due to the cost of establishing certain ratings (which must eventually be reflected in product prices) the ratings given do not always encompass all conceivable operating conditions. For example, device dissipation ratings typically are complete only for the case of continuous dissipation (as opposed to peak dissipation in pulse applications). In practice, the ratings given should be sufficient for the majority of applications of a particular device. In certain applications, more information must be obtained by the user himself and/or through applications assistance from the manufacturer. The following ratings typically appear on Agilent Technologies transistor data sheets and provide adequate

information for most applications of these devices.

A. Voltage Ratings

These ratings are usually derived from and usually coincide with the minimum device breakdown voltages. However, since this coincidence does not necessarily occur, it has become common practice to include both maximum voltage ratings and minimum breakdown voltages on data sheets.

It can be argued that such practice erodes the meaning of maximum ratings. Since, strictly speaking, maximum ratings should not be exceeded under any circumstances, strict adherence to voltage ratings would preclude measurement of breakdown voltage of any but marginal devices. In practice, voltage ratings are usually maximum operating voltages and no damage results if they are exceeded only to measure the breakdown voltages provided that care is taken to ensure that the specified low currents for these measurements are not exceeded.

B. Current Ratings

Maximum current ratings are arrived at from various considerations such as bonding-wire current-carrying ability, overall transistor performance degradation, etc. Maximum ratings are usually given only for collector current (except, in some cases for switching devices) since safely limiting collector current usually ensures that base and emitter currents are also safely limited.

C. Dissipation Ratings

In addition to the individual ratings on voltage and current discussed above, there is also a

limit to the voltage-current products which can be safely handled by a transistor. That is, there is a power dissipation rating which must also be adhered to. Since the dissipation capabilities of a device are a function of the temperature of the external environment, this rating is a function of that temperature. For the DC case, this temperature dependence is usually the only significant functional dependence of this rating. In the AC case, that is when device dissipation varies significantly with time, dissipation capabilities become a generally complex function of waveshape. In the latter case, in addition to an average dissipation rating (which coincides with the DC rating) there exists a peak dissipation rating which is a function of waveshape (e.g., a function of pulse width and pulse period in the case of rectangular waveforms). Due to the complexity of the general AC case, transistors are seldom characterized completely enough to include complete AC rating information. Most transistors are rated only in terms of maximum continuous dissipation (i.e., the maximum DC and the maximum average dissipation). This rating is typically specified in terms of a maximum continuous dissipation at or below some stated reference temperature (usually 25°C) and a linear derating factor to be applied at higher temperatures. These two quantities define the maximum continuous dissipation rating curve shown graphically in Figure 2, or expressed analytically as shown in Equation 1.

Equation 1:

$$P_{T(\max)} T_X = P_{T(\max)} T_{XI}; T_X \leq T_{XI}$$

$$P_{T(\max)} T_X = P_{T(\max)} T_{XI} - K_{JX} \Delta T_X; T_{XI} < T_X < T_{X(\max)}$$

Where

T_X = Temperature of the external reference point

$P_{T(\max)}$ = Maximum Total Dissipation, a function of T_X

T_{XI} = Reference temperature below which $P_{T(\max)}$ is constant

K_{JX} = Linear Derating Factor

$T_{X(\max)}$ = Maximum Junction Temperature

ΔT_X = $T_X - T_{XI}$

Two external temperature reference points are commonly used:

1. Air ambient, T_A (or free-air; i.e., no forced air cooling), which is the air temperature in proximity to the transistor case as mounted in its "normal" manner and,

2. Case ambient, T_C , which is the temperature at the point on the transistor package at which it is most effective to heat sink the transistor.

Which reference point is used depends on the application.

In summary, the continuous dissipation rating (usually based on a $V \times I$ product), and the collector voltage and current ratings define a DC safe operating area as sketched in Figure 3.

D. Junction Temperature Rating

Another temperature reference point implicit in the above discussion of dissipation ratings is transistor junction temperature. The maximum external reference-temperature, $T_{X(\max)}$, corresponds to the maximum internal junction

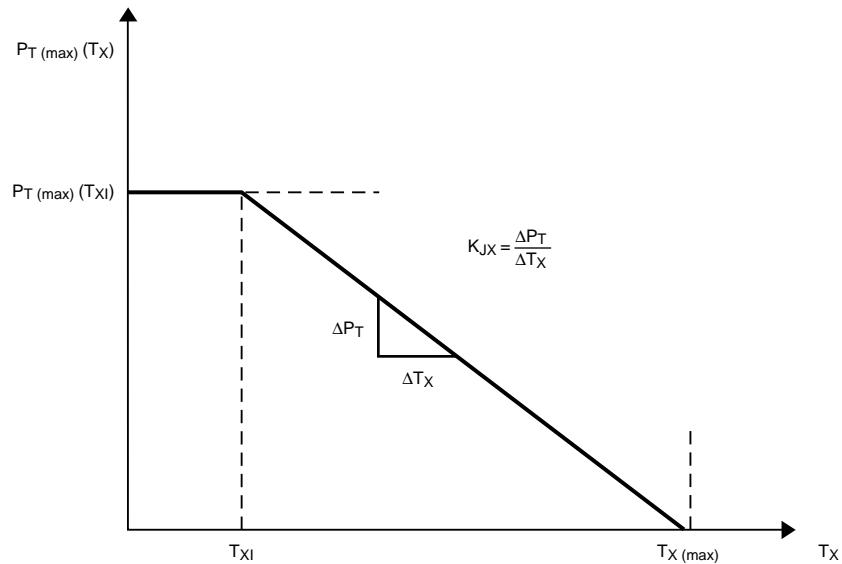


Figure 2. Continuous Dissipation Rating Curve

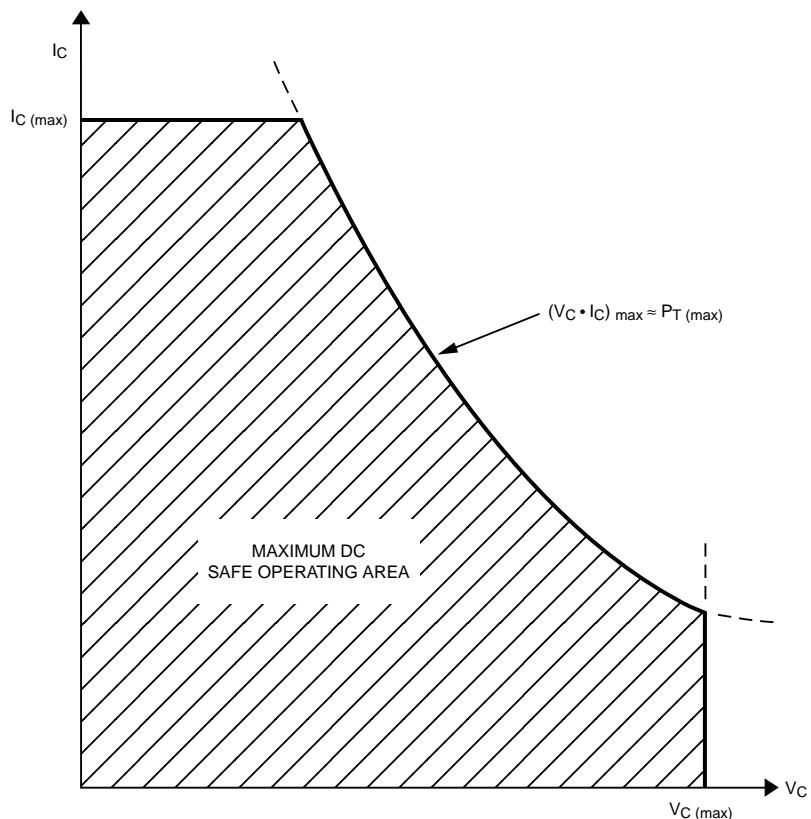


Figure 3. Maximum DC Safe Operating Area

temperature, since at $T_{X(\max)}$ the power dissipation must be derated to zero. Strictly speaking, junction temperature does not properly classify as a maximum rating since it is not an external stress under direct control of the user (as opposed to power dissipation and external operating temperature which are). Thus, a more appropriate terminology for this rating would be maximum operating temperature. However, since it is a limiting factor in transistor dissipation capabilities and its use simplifies time-varying thermal analysis, the rating still appears on many transistor data sheets as a junction temperature rating.

E. Storage Temperature Rating

This rating defines the range of temperature over which the transistor may be stored (in the non-operating state) without damage. Because of possible electrical-temperature interactions, storage temperature range and operating temperature range do not necessarily coincide. However, in practice, they usually do coincide and in the absence of stated restrictions on operating range, storage temperature range may be taken as operating range also.

III. Electrical and Performance Characteristics

Electrical characteristics may be described as uniquely defined, measurable electrical properties of the transistor which are not a function of the measuring circuit or apparatus (except insofar as standard terminations and measurement accuracy are concerned). Performance, or operating characteristics are also electrical properties but they are,

in general, not unique because their values depend upon the measuring circuit (in particular, the source and load impedance, which may be arbitrary). As might be expected, the terms are often used somewhat loosely (and sometimes interchangeably), especially in some cases where there are only subtle differences involved. The terms are generally used on transistor data sheets to segregate (for emphasis) under performance or operating characteristics those properties most directly applicable for the primary intended application.

A. Performance (Operating) Characteristics

Of the numerous performance characteristics which can be specified for high-frequency transistors, perhaps the most fundamental and pertinent characteristics are:

1. Power gain and noise figure, for small-signal applications;
2. Power gain, power output and efficiency, for large signal applications.

All of these characteristics are, of course, functions of frequency, bias temperature, etc., and to completely characterize a transistor over its full frequency, bias, and temperature ranges would be prohibitively costly. Consequently, characterization data is given only for restricted ranges of these variables. This data should portray sufficiently the capabilities of a particular device for its intended applications. As in the case of maximum ratings, some applications may require additional characterization by the user himself or through applications assistance from the manufacturer.

1. Power Gain

a. G_{max}

Of the various definitions for the measure of power flow in an active two-port device, such as a transistor, two are unique enough to allow specification without recourse to specifying the complete measuring circuit in detail. One of these definitions is termed Maximum Available Gain, G_{max} , and is the power gain obtained when the input and output ports are simultaneously conjugately matched to source and load impedances, respectively. Implicit in this definition is the assumption that the two-port is unconditionally stable, i.e., no combinations of input/output tuning can result in increasing gain to the point of oscillation.

b. $|S_{21}|^2$

The other unique power gain is the gain realized when the transistor is inserted between a source and a load with identical impedances (in practice usually $50 + j0$ ohms). This particular insertion or transducer gain happens to coincide with the usual definition of the two-port forward scattering parameter, S_{21} . More precisely, it is equal to the magnitude squared of this parameter and is therefore often identified by the symbol

$|S_{21}|^2$.

For wideband applications,

$|S_{21}|^2$ is important since wideband terminations "not-too-different" from 50 ohms are more easily realized than are wideband transforming networks which provide the matching required for G_{max} .

2. Noise Figure

A common measure of the noise generated by an active two-port device, noise which sets a lower limit on amplifier sensitivity, is the noise factor, F . This is defined as:

$$F = \frac{\text{Input signal-noise ratio}}{\text{Output signal-noise ratio}} \quad (2)$$

or more generally as:

$$F = \frac{\text{Total output noise power}}{\text{Output noise power due to source resistance}} \quad (3)$$

At high frequencies, spot noise factor or noise factor for a small fractional bandwidth (say 1%) is used and is usually expressed as noise figure, NF , in decibels, i.e.,

$$NF = 10 \log F$$

As already discussed, noise figure is a function of source impedance (as well as functions of frequency, bias, etc.) and hence, there is an infinity of noise figures associated with a given device corresponding to the infinity of possible impedances which may be presented to the device input. The only unique one, in the sense that it does not involve arbitrary source impedances, is NF_{min} , the minimum noise figure obtained (at given bias and frequency) when the input is tuned to optimize this parameter. It is this noise figure which is usually given on Agilent Technologies data sheets.

In practical amplifiers, involving more than one stage, overall noise factor F_O is given by:

$$F_O = F_1 + \frac{F_2 - 1}{G_1} + \dots + \frac{F_n - 1}{G_{(n-1)}} \quad (4)$$

where

- n = number of stages
- G_n = gain of the n th stage
- F_n = noise factor of the n th stage.

This expression emphasizes the important fact that for low noise amplifiers, the first stage must be designed for the lowest noise figure and highest gain possible. (Note that the noise contribution of the second stage is divided [reduced] by the gain of the first stage). Since the optimum source impedance and bias currents for optimum gain and noise figure do not often coincide, very careful circuit design is required to minimize overall noise figure.

3. Power Output

This characteristic is important for both amplifier and oscillator transistors. In both cases, it is extremely circuit sensitive. For amplifiers, maximum useful output is often limited to that power output level at which gain has compressed 1 dB, an indicator of the upper limit on the linearity range. For oscillators, it is merely a quantitative measure of RF power for a given DC input power.

4. Efficiency

In the most general sense, this characteristic expresses as a percentage, the ratio of RF power output to the total circuit input power, both DC and RF. That expression is total efficiency, η_t , defined as:

$$\eta_t = \frac{P_O}{P_i + P_{DC}} \times 100 \quad (5)$$

where

- P_O = RF output power
- P_i = RF input power
- P_{DC} = total DC power input

Power transistors are often characterized in terms of power added efficiency, η_{add} , defined as:

$$\eta_{add} = \frac{P_O - P_i}{P_{DC}} \times 100 \quad (6)$$

Since for oscillator transistors there is no RF power input, and for amplifier transistors the maximum input RF power is calculable from the power gain and power output specifications, the inclusion of P_i in efficiency is redundant. Moreover, since the major portion of the DC power is dissipated by the transistor collector, a more restricted definition of efficiency is pertinent. This parameter, termed collector efficiency, η_c , is given by:

$$\eta_c = \frac{P_O}{P_{CC}} \times 100 \quad (7)$$

where

- P_{CC} = $V_{CC} \times I_{CC}$
- V_{CC} = collector supply voltage
- I_{CC} = collector supply current

B. Electrical Characteristics

Electrical characteristics may be conveniently classified into two main types, DC and AC.

1. DC Characteristics

The importance of DC characteristics of high frequency transistors lies primarily in biasing and reliability considerations. However, certain DC characteristics are also directly related to high-frequency performance. For example, high-frequency noise figure is affected by the DC current gain. The DC characteristics which are discussed here are those usually found on high frequency transistor data sheets.

a. $V_{(BR)CBO}$, I_{CBO}

These two parameters serve to characterize the reverse-biased collector-base p-n junction and are defined as follows (with the aid of Figure 4a). The collector-base breakdown voltage, $V_{(BR)CBO}$, identifies the voltage at which collector current tends to increase without limit, usually due to the high electric field developed across the junction. This voltage sets a limit on the maximum transistor operating voltage and, as mentioned before under maximum ratings, usually is the basis for the collector-base maximum voltage rating. $V_{(BR)CBO}$ should be specified at a value of $I_C = I_{C1}$ in the figure, which is within the avalanche (or high slope) region of the reverse characteristic. Typical values of I_{C1} are in the $1 - 10 \mu\text{A}$ region for high frequency transistors.

To further define the quality of the reverse V-I characteristic a specification is usually placed on collector cutoff current, I_{CBO} , measured at some value of collector-base voltage less than $V_{(BR)CBO}$. For a good quality silicon junction ("sharp" instead of soft, see Figure 4a), I_{CBO} is in the nano-ampere range.

b. $V_{(BR)EBO}$, I_{EBO}

These two parameters characterize the reverse-biased emitter-base p-n junction in an analogous manner to the collector-base junction parameters $V_{(BR)CBO}$, and I_{CBO} , given above and are shown in Figure 4b. No further discussion will be given here.

c. $V_{(BR)CEO}$, I_{CEO}

The collector-emitter breakdown voltage and cutoff current are somewhat more complex in nature than either the collector-base or emitter-base parameters. In the

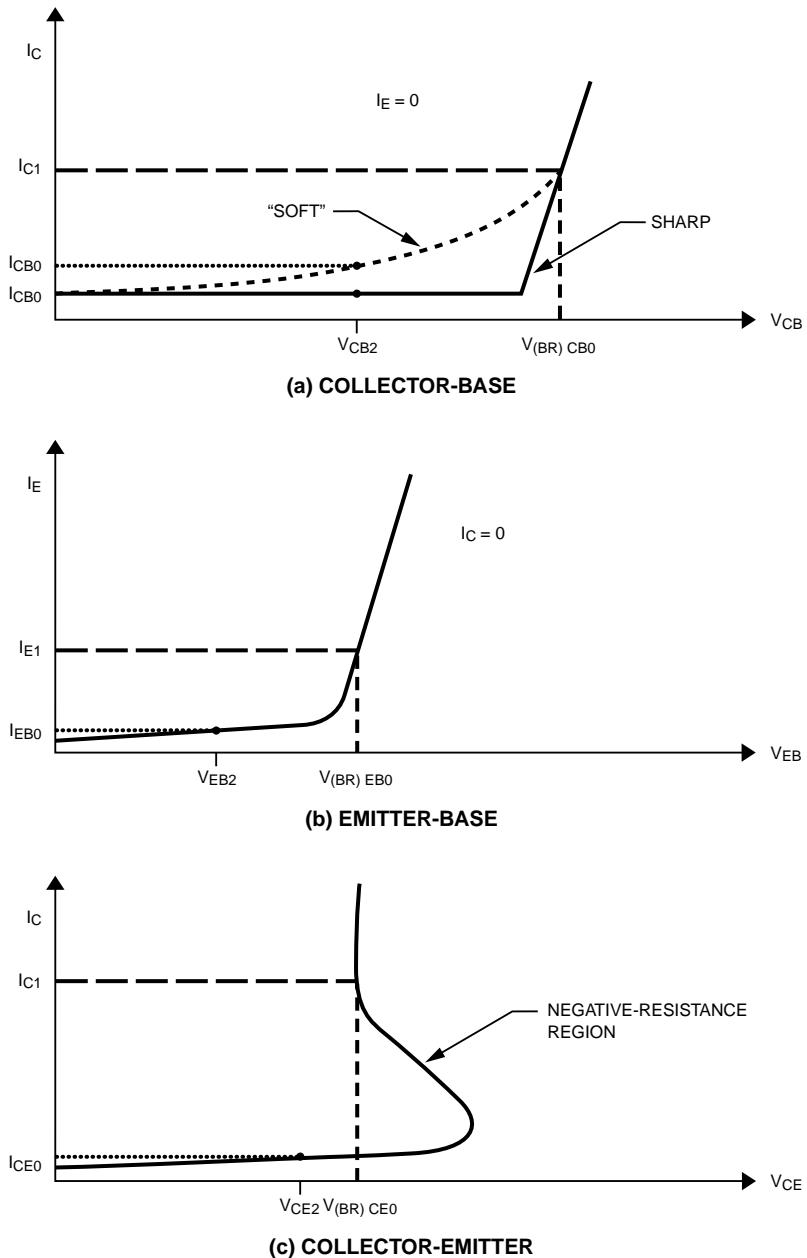


Figure 4. Transistor Reverse V-I Characteristics

latter two, only a single p-n diode is involved. In the collector-emitter case, two diodes are involved. Moreover, each is influenced by the other through transistor action, since the reverse current of the collector-base diode flows through the emitter-base junction as forward current. Thus the collector-base reverse current is amplified by the DC current gain of the transistor resulting in:

- 1) I_{CEO} being greater than I_{CBO} (for a given voltage).
- 2) Typically the familiar negative-resistance region in the V-I characteristic as shown in Figure 4c.

Consequently, $V_{(BR)CEO}$ is typically specified at collector currents one to three orders of magnitude higher than in the case of $V_{(BR)CBO}$ and $V_{(BR)EBO}$ in order to establish the minimum value of this characteristic.

d. h_{FE}

This parameter is simply the DC common-emitter current gain; i.e., the ratio of collector current to base current at some specified collector voltage and current.

2. AC Characteristics

Of the numerous AC characteristics which are defined for transistors, only relatively few are commonly used in characterizing high-frequency transistors. Some of the more pertinent parameters are briefly covered here.

a. S-Parameters

By far the most useful and conveniently measured set of two-port parameters for transistor high frequency (roughly 100 MHz and above) characterization is the S-parameter or scattering-matrix set. These parameters completely

and uniquely define the small-signal gain and input/output immittance properties of any linear "black box". (By definition, a transistor or any active device is linear under small-signal conditions). However, these parameters reveal nothing (except possibly indirectly and approximately) about large-signal behavior or about noise behavior. Simply interpreted (more general definitions and other interpretations abound in the technical literature), the S-parameters are merely insertion gains, forward and reverse; and reflection coefficients, input and output, with driven and non-driven ports both terminated in equal impedances, usually 50 ohms, real. Such an interpretation tends to make S-parameters very attractive, once some familiarity is gained, at high (especially microwave) frequencies, since the power flow or gain and reflection-coefficient concepts are more intuitively meaningful than voltage and current conceptual schemes. It should also be mentioned that S-parameters can be converted through straight-forward matrix transformations to other two-port parameter sets; e.g., h-, y-, or z-parameters.

Proceeding with more specific definitions, the S-parameters are defined analytically by:

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2 \end{aligned} \quad (8)$$

or, in matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11}S_{12} \\ S_{21}S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (9)$$

where, referring to Figure 5:

$$a_1 = (\text{incoming power at port 1})^{1/2}$$

$$b_1 = (\text{outgoing power at port 1})^{1/2}$$

$$a_2 = (\text{incoming power at port 2})^{1/2}$$

$$b_2 = (\text{outgoing power at port 2})^{1/2}$$

$$E_1, E_2 = \text{Electrical stimuli at port 1, port 2}$$

From the figure and defining linear equations, for $E_2 = 0$, then $a_2 = 0$, and (skipping numerous rigorous steps) refer to Equation 10 below.

Equation 10 :

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1} = \left[\frac{\text{Outgoing Input Power}}{\text{Incoming Input Power}} \right]^{1/2} \\ &= \frac{\text{Reflected Voltage}}{\text{Incident Voltage}} = \text{Input Reflection Coefficient} \\ S_{21} &= \frac{b_2}{a_1} = \left[\frac{\text{Outgoing Output Power}}{\text{Incoming Input Power}} \right]^{1/2} \\ &= \left[\frac{\text{Output Power}}{\text{Available Input Power}} \right]^{1/2} = [\text{Forward Transducer Gain}]^{1/2} \end{aligned}$$

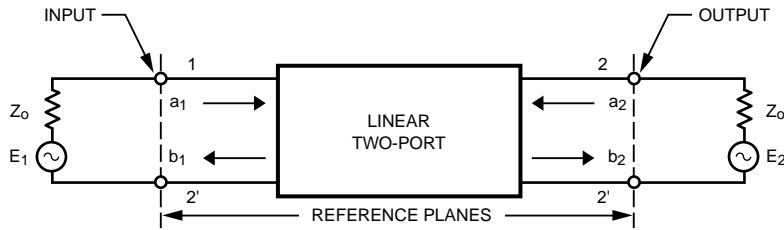


Figure 5. Two-port S-parameter Definition Schematic

or more precisely in the case of S_{21} :

Equation 11:

$$\text{Forward Transducer Gain} = G_{TF} = |S_{21}|^2$$

$$Z_i = Z_o$$

Similarly at Port 2 for $E_1 = 0$, then $a_1 = 0$, and

Equation 12:

$$S_{22} = \frac{b_2}{a_2} = \text{Output Reflection Coefficient}$$

$$S_{12} = \frac{b_1}{a_2} = \text{Reverse Transducer Gain}^{1/2}$$

$$G_{TR} = |S_{12}|^2$$

Since many measurement systems actually “read out” the magnitude of S-parameters in decibels, the following relationships are particularly useful:

Equation 13:

$$|S_{11}|_{\text{db}} = 10 \log |S_{11}|^2$$

$$= 20 \log |S_{11}|$$

$$|S_{22}|_{\text{db}} = 20 \log |S_{22}|$$

$$|S_{21}|_{\text{db}} = 10 \log |S_{21}|^2$$

$$= 20 \log |S_{21}|$$

$$= 10 \log |G_{TF}| = |G_{TF}|_{\text{db}}$$

$$|S_{12}|_{\text{db}} = 10 \log |S_{12}|^2$$

$$= 20 \log |S_{12}|$$

$$= 10 \log |G_{TR}| = |G_{TR}|_{\text{db}}$$

b. Transition Frequency

One of the better known, but perhaps least understood, figures-of-merit for high-frequency transistors is the so-called transition frequency, f_T . Part of the misunderstanding which appears to exist is due to the use of a misleading (but common, for historical reasons) terminology of “short-circuit gain-bandwidth product” for this parameter.

By definition, f_T is that characteristic frequency described by the equation:

$$f_T = h_{fe} \times f_{\text{meas}} \quad (14)$$

where

h_{fe} = magnitude of small-signal common-emitter short-circuit current gain, h_{fe}

f_{meas} = Frequency of measurement, chosen such that:

$$2 \leq h_{fe} \leq \frac{h_{feo}}{2} \quad (15)$$

h_{fe} = the low frequency value of h_{fe}

To varying degrees of approximation, depending on transistor type, f_T is the frequency at which h_{fe} approximates unity. It is not, in general, the frequency at which h_{fe} is precisely equal to unity. To clarify these points further, consider the plot of h_{fe} against frequency sketched in Figure 6.

At low frequencies, $f < f_B$, h_{fe} is constant and equal to h_{feo} .

At f_B , h_{fe} has decreased to 0.707 h_{feo} ; i.e., f_B is the 3 dB cutoff frequency for common-emitter short-circuit current gain, h_{fe} .

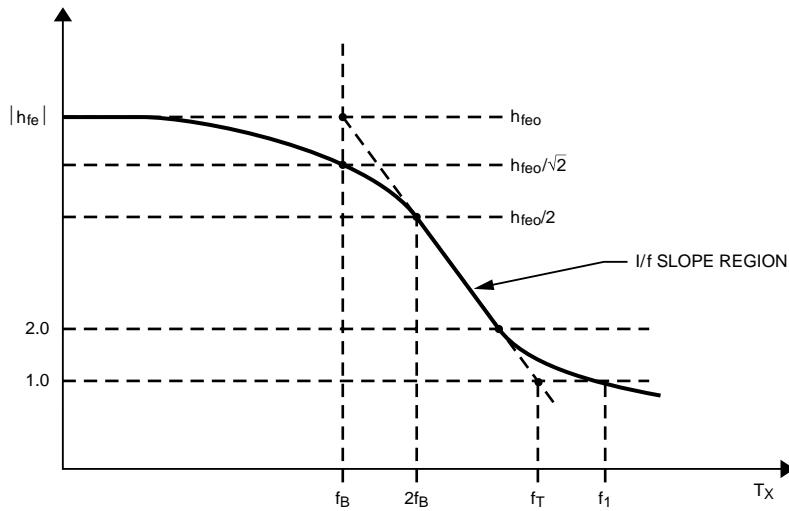


Figure 6. $|h_{fe}|$ Frequency Characteristics

For frequencies such that

$$2f_B < f < f_T$$

h_{fe} varies inversely proportional to frequency. That is, the f_T defining relationship holds:

$$h_{fe} \times f_{meas} = \text{constant} = f_T \quad (16)$$

At frequencies approaching f_T , other parameters, especially package parasitics, can cause $|h_{fe}|$ to depart significantly from this $1/f$ variation. Therefore, the frequency, f_1 , at which $|h_{fe}|$ actually equals unity can be somewhat different from f_T .

Applying this frequency-gain characteristic to common-emitter wide-band, low-pass amplifiers gives rise to the terminology of f_T being a “gain-bandwidth product”. However, this is an optimistic approximation at best, since the product of low frequency circuit gain and the 3 dB cutoff frequency is reduced from f_T by an amount depending on circuit impedances.

The real significance of f_T lies in the fact that it is a measure of certain internal transistor parameters which do, in fact, affect high-frequency performance; for example, gain (though not in the convenient quantitative manner implied by the gain-bandwidth product terminology). In particular, good high-frequency noise performance requires that f_T be high. Thus, f_T is included on transistor data sheets as a figure of merit primarily, not as a parameter to be used directly in design.

c. Collector-Base Time Constant, $r_b'C_c$

This is an internal device parameter which relates only indirectly to high frequency performance. It is primarily a measure of internal feedback within the transistor. It also relates to transistor high-frequency impedance. As the name says (in symbols), it is a measure of transistor base resistance and collector capacitance in combination; however, except for certain low-frequency transistors, it cannot be considered the simple two-element lumped R-C time

constant implied by the terminology. (In high frequency transistors, both base resistance and collector capacitance must be considered distributed when considered in detail). As a figure of merit, it is included on transistor data sheets to indicate how well base resistance and collector capacitance have been minimized. It also allows the estimation of certain gain properties of the transistor (see f_{max} parameter, following).

d. Collector-Base Capacitance, C_{cb}

This parameter is simply the total collector-base p-n junction capacitance measured at a low frequency (typically, 1 MHz) where it can be considered a single lumped element. For high-frequency transistors it is, of course, desirable that C_{cb} be small from bandwidth and stability considerations as well as from gain considerations alone.

e. Maximum frequency of Oscillation, f_{max}

This is another figure-of-merit parameter, as opposed to measurable parameters directly usable in the applications of transistors. Its importance stems from the following approximate relationships (which will not be derived here):

$$f_{max} \approx \left(\frac{f_T}{8\pi r_b C_c} \right)^{1/2} \quad (17)$$

$$G_{max} \approx \left(\frac{f_{max}}{f_{oper}} \right)^2 \quad (18)$$

These expressions illustrate in a quantitative way the importance and the interrelationship between high f_T and low $r_b'C_c$ insofar as high frequency gain is concerned. However, since they are approximations and since their derivation

involves several assumptions not always valid, they must be interpreted with caution. For example, the expression for G_{max} is obviously not applicable at low frequencies since as $f \rightarrow 0$, $G_{max} \rightarrow \infty$, according to this expression. As a rule of thumb, the G_{max} expression is a reasonable approximation for frequencies such that,

$$5 > \frac{f_{max}}{f_{oper}} > 1 \quad (19)$$

For accurate analysis of transistor gain and stability, a complete set of two-port parameters must be employed in exact expressions, such as those from which the approximations shown above were derived.

IV. Glossary of Microwave Transistor Terminology

$V_{(BR)CBO}$

Breakdown voltage of a reverse biased collector-base junction measured with the emitter open.

$V_{(BR)EBO}$

Breakdown voltage of a reverse biased emitter-base junction measured with the collector open.

$V_{(BR)CBO}$

Breakdown voltage between the collector and emitter terminals measured with the base open.

I_{CBO}

Leakage current of a reverse biased collector-base junction measured with the emitter open.

I_{EBO}

Leakage current of a reverse biased emitter-base junction measured with the collector open.

h_{fe}

DC common-emitter current gain.

C_{cb}

Collector-base junction capacitance measured with the emitter connected to the guarded terminal

of a three terminal measurement system.

f_T

Transition Frequency. The frequency at which the magnitude of the small-signal common-emitter short-circuit current gain approximates unity.

$r_b' C_c$

The collector-base time constant.

f_{max}

Maximum frequency of oscillation. The frequency at which G_{max} approaches unity.

$P_{T(max)}$

Maximum continuous power dissipation below a reference temperature (usually 25°C).

$T_{J(max)}$

Maximum allowable transistor junction temperature.

$I_{C(max)}$

Maximum allowable collector current without destruction or degradation of the transistor.

NF

A measure of the noise generated by the transistor.

G_{max}

The maximum available power gain (MAG) when the transistor is unconditionally stable and input and output ports are simultaneously conjugately matched.

S_{11}

Input reflection coefficient.

S_{12}

Reverse transfer coefficient.

S_{21}

Forward transfer coefficient.

S_{22}

Output reflection coefficient.

P_O

Amplifier – The power output at the one (1) db gain compression point.

Oscillator – A measure of the RF power output.

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High-Frequency Transistor Primer

Part IV

GaAs FET Characteristics

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Introduction

This primer (number four in a series) offers a brief explanation of the terms commonly used in Agilent Technologies GaAs FET data sheets, advertisements and other technical communications. Some of these terms are virtually self-explanatory and are included here primarily for the sake of completeness. Others are more specialized and potentially ambiguous due to a lack of terminology standardization among manufacturers and users of high-frequency transistors – the latter receive more thorough treatment here.

I. Basic Terminology

The last section of this primer is a comprehensive glossary of the important terms associated with GaAs FETs. To make it easier for the reader with little familiarity with GaAs FETs, however, a few of the most basic terms are presented here.

GaAs: Gallium Arsenide. A semiconductor compound.

FET: Field Effect Transistor. A type of transistor in which the current is controlled by the application of a varying electric field.

GaAs FET: A field effect transistor made from gallium arsenide.

Source, Drain and Gate: The three basic elements of an FET. Their functions will be explained in the text.

Epi layer: A very thin (*epitaxial*) layer of semiconducting GaAs grown on an insulating GaAs wafer.

Dopant: A material added to GaAs to make it semiconducting.

Schottky Barrier: A diode formed by a rectifying metal-semiconductor junction in which majority carriers carry the current flow. Used as the gate contact in GaAs FETs.

II. Transistor Structure

A. What Is a GaAs FET?

A basic depletion mode field effect transistor (FET) is a three port device in which the gate controls the flow of current from the source to the drain by varying the electric field and thus a depleted carrier region in the semiconducting epitaxial layer, beneath the gate (See Figure 1). A GaAs FET (or GaAs MESFET for Metal Semiconductor) is simply an FET with a diode gate structure (similar to a junction FET, but a surface device) made from gallium arsenide (GaAs) which is a compound, as opposed to silicon, which is an element.

A FET is a semiconductor analog to a triode vacuum tube. The gate acts as the control element as does the grid in the triode. The source acts as the cathode and the drain as the plate (anode). The conductivity of the epi layer under the gate, and thus the flow of current, is varied by applying a

voltage to the *gate* which is of negative polarity with respect to the *source*, while in a triode vacuum tube the *grid* is biased negative with respect to the *cathode*. The *drain* terminal of the FET is biased positive with respect to the *source*, just as the *plate* of a triode is biased positive with respect to the *cathode*.

B. Active Layer Fabrication

There are several ways to fabricate the semiconducting active layer of GaAs FETs. The two main approaches are: *Epitaxial growth* where the active layer of doping impurities is grown on the top of the substrate crystal by the liquid-phase, vapor-phase or molecular beam process; and *Ion implantation* where the doping impurities are injected directly into the crystal lattice of the substrate material (which may have an undoped epitaxial layer already fabricated – or implanted – on it by the vapor-phase process).

Agilent Technologies presently uses two approaches for GaAs FET active layer growth: Vapor phase epitaxy (VPE) and ion-implantation (I²). The DC and RF performance of devices produced by the two approaches is virtually the same.

C. Metallization Systems

The combination of metals used to make contact to the three GaAs FET device elements (source, gate and drain) is crucial to both the reliability and performance of the device. The source and drain contacts, through which *all* of the drain current flows, must be of *very low* resistance and high stability to insure optimum device performance. Agilent Technologies presently uses a proven alloyed gold-germanium-nickel

contact (Au-Ge-Ni) for contacts to GaAs FET source and drain elements.

Several different metal systems have been used by transistor manufacturers to make the Schottky-barrier diode gate contact; the two main approaches being aluminum and gold-based systems.

Aluminum creates a good Schottky barrier on GaAs, and aluminum atoms do not diffuse easily into the GaAs – such diffusion would change the device characteristics. However, aluminum is an active element and can form intermetallic compounds, particularly at the Au-Al interface, and is relatively susceptible to damage from electrostatic discharge and high RF energy levels. Gold, on the other hand, is the element which is most stable in the presence of oxidants, and is less susceptible to electrostatic or RF damage. It does, however, diffuse quickly into GaAs and, therefore, in order for gold to be used as a gate metal, barrier metals must be introduced between the gold and the GaAs. Agilent Technologies uses titanium (Ti) and tungsten (W) as barrier metals in its gold-based gate metal system. This metallization has proven to provide both high reliability and excellent mechanical and electrical performance.

D. FET Dimensions Affecting Microwave Performance

The important dimensions in FETs are the spacing from the source to the gate, and from the gate to the drain. For microwave operations, the most critical dimension is the “length” of the gate along the carrier (electron) path. The shorter the gate length, the

higher becomes the signal frequency which can be controlled by the depletion layer set up in the active channel beneath the gate. The spacing between the gate electrode and the source, and gate and drain introduces capacitance. If the FET is to handle larger amounts of signal current, the gate width must be increased appropriately. Viewing the FET pictorially (Figure 1) helps to understand that the "width" dimension is perpendicular to the carrier flow along the length of the channel from source to drain. RF power handling capability is proportional to this gate width. In general, the transconductance (g_m) – the influence of gate voltage on drain current – and the capacitances increase proportionally with increasing gate width while the resistances vary inversely with the width. Doubling the gate width doubles the transconductance and the feedback capacitance and halves the resistance.

E. Why a GaAs FET Instead of a GaAs Bipolar or Silicon Transistor?

The advantage of GaAs over silicon is that with GaAs the carriers (electrons, or electrons and holes) can reach about twice the limiting

velocity with one third the applied bias voltage. Therefore, for a given geometry, a given current gain can be reached at more than twice the frequency as with silicon. However, because of the more difficult physical chemical properties of GaAs, the variously doped layers of the bipolar structure (emitter, base and collector), would be difficult to form in GaAs (GaAs bipolar transistors would also be undesirable because of the low mobility of P-type GaAs material).

The structure used for GaAs FET fabrication, while somewhat similar to that of the silicon junction field-effect transistor – with a reverse-biased diode acting as the gate, and operation in the depletion mode – is totally a surface structure. There are no vertically diffused elements, such as the "buried" base layer between the emitter and collector which is used in a silicon bipolar transistor, or the "buried" channel in a silicon JFET. This is the only technique which can tap the advantages offered by GaAs with present fabrication technology. The FET surface structure can be used with GaAs and the necessary FET half-micron geometry for microwave frequency operation

can be fabricated routinely with the present state of the art in optical photolithography techniques.

There is one theoretical advantage of an FET structure as an amplifier, unrelated to the semiconductor material: the potential for low distortion. The FET is a square-law device, with its drain current proportional to the square of the ratio of the gate voltage to the pinchoff voltage.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(OFF)}} \right)^2$$

$$V_{GS(OFF)} = V_P =$$

$$\text{Pinchoff Voltage} \quad (1)$$

This means that it generates little odd-order distortion, and that the small amount of even-order distortion that it does generate can easily be suppressed with a balanced-stage circuit design. An FET looks like a biased capacitor in a circuit, while a bipolar transistor looks like a forward-biased diode junction.

III. How Does the FET Work?

Gain in an FET is proportional to the channel conductivity (the "channel" being that area within the epi material under the gate). In a depletion mode FET (of which the GaAs FET is an example), as the gate is biased more negatively, the actual conducting channel cross-section is reduced, and the drain current is also reduced. A small negative voltage applied to the gate starts to "deplete" the channel of carriers, beginning immediately adjacent to the gate electrode at the top of the channel. As the gate voltage is made increasingly negative, the

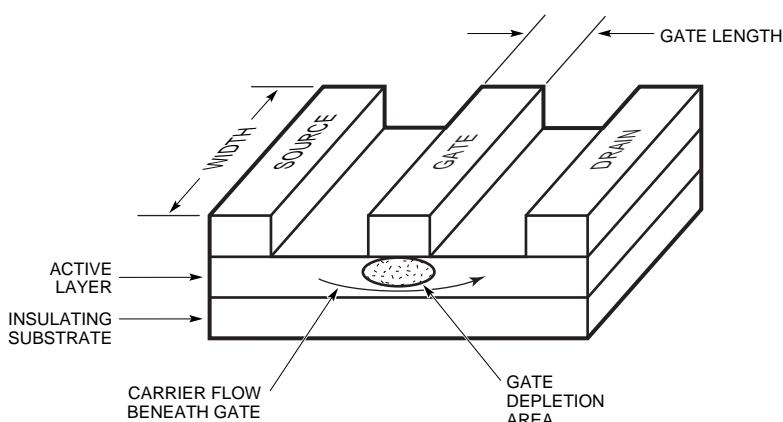


Figure 1. Basic GaAs FET Structure

gate depletion layer is extended further into the channel until it reaches the semi-insulating GaAs substrate. When the gate is made sufficiently negative, the channel is closed, or "pinched off", and no current flows. The gate voltage at which drain current is stopped is called the *pinchoff voltage* (V_p).

Drain current will be highest, and the gain of the GaAs FET will be highest when the gate voltage is zero with respect to the source -- that is, with the gate connected directly to the source. This is the "saturated" drain-to-source current condition or I_{DSS} .

IV. Electrical and Performance Characteristics

Electrical characteristics may be described as uniquely defined, measurable electrical properties of the transistor which are not a function of the measuring circuit of apparatus (except insofar as standard terminations and measurement accuracy are concerned). Performance or operating characteristics are also electrical properties, but they are, in general, not unique because their values depend upon the measuring circuit (in particular, the source and load impedance, which may be arbitrary). As might be expected, these terms are often used somewhat loosely (and sometimes interchangeably), especially in cases where there are only subtle differences involved. The terms are generally used on transistor data sheets to segregate (for emphasis) under performance or operating characteristics those properties most directly applicable to the expected application.

A. Performance (Operating) Characteristics

The most fundamental characteristics specified for microwave GaAs FETs are:

1. Noise Figure
2. Gain at Noise Figure
3. Maximum Available Gain
4. Linear Power Output
5. Associated Small Signal Power Gain
6. Efficiency
7. Forward Transducer Gain

All of these characteristics are, of course, functions of frequency, bias, temperature, etc., and to completely characterize a transistor over its full frequency, bias and temperature ranges would be prohibitively costly. Consequently, characterization data is given only for restricted ranges of these variables. This data should portray sufficiently the capabilities of a particular device for its primary intended applications. As in the case of maximum ratings, some applications may require additional characterization by the user or applications assistance from the manufacturer.

1. Noise Figure - NF_0

Noise factor is a numerical value which is the common measure of the noise generated by an active two-port device - noise which sets a lower limit on amplifier sensitivity. This may be defined as:

$$F = \frac{\text{Input Signal-to-Noise Ratio}}{\text{Output Signal-to-Noise Ratio}} \quad (2)$$

or, more generally,

$$F = \frac{\text{Total Output Noise Power}}{\text{Output Noise Power Due To Signal Source Resistance}} \quad (3)$$

At high frequencies, the spot noise factor, or noise factor at a small bandwidth (say 1%), is used, and is usually expressed as noise figure, NF , in decibels, e.g.

$$NF = 10 \log F \quad (4)$$

As already discussed, noise figure is a function of source impedance (as well as being a function of frequency, bias, etc.), and hence there is an infinity of noise figures associated with a given device corresponding to the infinity of possible impedances which may be presented to the device output. The only unique noise figure, in the sense that it does not involve arbitrary source impedances, is NF_0 , the minimum noise figure obtained (at given bias and frequency) when the input is tuned to optimize this parameter. It is this noise figure which is usually given on Agilent Technologies data sheets.

In practical amplifiers, involving more than one stage, the overall *numeric* noise measure, F_m , is given by:

$$F_m = F_1 + \frac{F_2 - 1}{G_1} + \dots + \frac{F_n - 1}{G_{(n-1)}} \quad (5)$$

n = Number of Stages,
G = Gain of nth Stage,
 F_n = Noise Factor of
nth Stage

This expression emphasizes the important fact that for low noise

amplifiers the first stage must be designed for the lowest noise figure and highest gain possible. Note that the noise contribution of the second stage is divided (reduced) by the gain of the first stage. Since the optimum source impedances and bias currents for optimum gain and noise figure do not often coincide, very careful circuit design is required to minimize overall noise figure.

2. Associated Gain at Noise Figure – G_A

This gain is simply the small-signal gain that results from optimum noise figure tuning of the circuit in which the device is installed. Best noise matching of the input of the transistor does not necessarily coincide with conjugate input S-parameter match (S_{11}^*), and therefore gain at noise figure is usually lower than the maximum available gain.

3. Maximum Available Gain – MAG

Of the various definitions for the measure of power flow in an active two-port device, such as a transistor, two are unique enough to allow specification without recourse to specifying the complete measuring circuit in detail. One of these definitions is termed maximum available gain, MAG. It is the power gain obtained when the input and output ports are simultaneously conjugately matched to source and load impedances, respectively. Implicit in the definition is the assumption that the two-port device is unconditionally stable: i.e., no combination of input and output tuning can result in increasing the gain of the device to the point of oscillation.

The other definition of power flow is Maximum Stable Gain or MSG. This definition is used when stability is only conditional and is the maximum gain possible with stable operation.

4. Power Output

This characteristic is important for both amplifier and oscillator transistors. In both cases, it is extremely circuit sensitive. For amplifiers, the maximum useful power output is often limited to that power output level ($P_1 \text{ dB}$) at which gain has compressed 1 dB ($G_1 \text{ dB}$), an indicator of the upper limit of linearity range, or may be specified at a greater gain compression, such as 2 dB or 3 dB (P_{sat}), when output power is more important than linearity. For oscillators, power output is merely a quantitative measure of RF power output for a given DC input power.

5. Associated Small Signal Power Gain – G_P

This gain is determined by decreasing the input power to the point that the device is operating in its linear region and then measuring the gain. This gain level will be lower than MAG primarily because the output is conjugately matched for large signal conditions and some mismatch occurs when signal levels are reduced.

6. Power Added Efficiency – η_{add}

The most commonly used efficiency expression for GaAs FET power devices is the *power added efficiency* which is defined as:

$$\eta_{\text{add}} = \frac{P_O - P_{\text{IN}}}{P_{\text{dc}}} \cdot 100\% \quad (6)$$

where

$$\begin{aligned} P_O &= R_F \text{ Output Power} \\ P_{\text{IN}} &= R_F \text{ Input Power} \\ P_{\text{dc}} &= \text{Total DC Input Power} \end{aligned} \quad (7)$$

7. Forward Transducer Power Gain $|S_{21}|^2$

The other unique power gain is the gain realized when the transistor is inserted between a source and load with identical impedances (in practice usually $50 + j0$ ohms). This particular insertion or transducer gain happens to coincide with the usual definition of the two-port forward scattering parameter, S_{21} . More precisely, it is equal to the magnitude-squared of this parameter and is therefore often identified by the symbol $|S_{21}|^2$. For wideband applications, $|S_{21}|^2$ is important since wideband terminations “not-too-different” from 50 ohms are more easily realized than are wideband transforming networks which provide the precise matching required for MAG.

B. Electrical Characteristics

Electrical characteristics may be conveniently classified into two types, DC and AC.

1. DC Characteristics

The importance of DC characteristics of high frequency transistors lies primarily in biasing and reliability considerations. However, certain DC characteristics are also directly related to high frequency performance. For example, high-frequency noise figure is affected by the DC current gain. The DC characteristics which are discussed here are those usually found on high-frequency transistor data sheets.

a. Transconductance – g_m

This parameter is the DC common-source conductance; that is the incremental change in output (drain) current with a given change in input (gate) voltage. It is usually specified at either I_{DSS} (gate voltage = 0 V) or one-half I_{DSS} although any current value or specified percentage of I_{DSS} can be used as the measurement point.

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \quad (8)$$

b. Pinchoff Voltage – V_p

This parameter is the gate voltage at which the drain-to-source current is reduced to some given value (usually 1 mA for small signal FETs and 5 mA for power FETs). See point A on the curves in Figure 2.

c. Saturated Drain-to-Source Current – I_{DSS}

This current occurs when the gate-to-source voltage is held to zero and the drain-to-source voltage set to a specified (usually 3 volts) value. See point B on Figure 2 curves.

d. Low-Field Channel Resistance – R_{do}

This is the slope of the drain I-V characteristic near the origin of the curve and is an indicator of the active channel resistivity and the drain and source contact quality. See the region around point C on Figure 2 curves.

e. Breakdown Characteristics

The breakdown characteristics of the gate contact can be measured in both directions (gate-to-drain and gate-to-source). In general, since the device is close to physically symmetrical, only one of the two is needed to verify device quality. Most often the gate-to-drain characteristics are used. There are two ways of characterizing the breakdown characteristics: Specifying the gate-to-drain current and measuring the voltage at that point (BV_{gd}), or specifying the voltage and measuring the reverse current (I_{gd}). In either case they are go-no-go type tests, failing when either the reverse current exceeds the specified value or the breakdown voltage is lower than the specified value, and are non-destructive as long as the current levels are kept low (in the μ A range).

variety of sources including volumes one and two of this Primer series. That information will not be repeated here. What will be discussed is the measurement technique and fixturing utilized in Agilent Technologies' transistor S-parameter measurements.

Packaged device S-parameters are measured in 50 ohm test fixtures* using Agilent Technologies' TFP microstripline or TF coaxial test fixtures. The test fixture introduces errors which can be corrected by either a reference plane extension or a THRU/DELAY calibration¹. The most accurate data for frequencies above 6 GHz uses the THRU/DELAY calibration, which is also referred to as de-embedded S-parameter data. This is the data in the Agilent Technologies RF Semiconductor Designers Catalog.

Chip devices are measured in the 50 ohm microstripline test fixture shown in Figure 3. The S-parameter data should be de-embedded for frequencies above 6 GHz. At present, bonding wire inductances are *not* subtracted out of the chip S-parameter values. A sketch of the standard chip test carrier is shown in Figure 3.

b. f_{max}

The maximum frequency of oscillation, f_{max} , is the frequency at which a curve of unilateral power gain (U) vs. frequency intercepts zero dB gain. The gain of both bipolar and FET transistors drops at a rate of approximately 6 dB per octave in the microwave region. If gain is measured at convenient

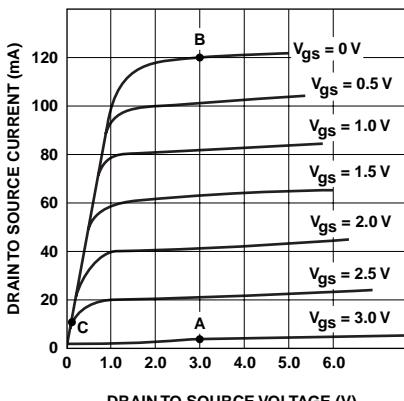


Figure 2. Typical GaAs FET DC Characteristic

2. AC Characteristics

Of the numerous AC characteristics which are defined for transistors, only relatively few are commonly used in characterizing high-frequency transistors. Some of the more pertinent parameters are briefly covered here.

a. S-Parameters

The standard definitions of S-parameters are covered in a

* TFP test fixtures and de-embedding software are available from Intercontinental Microwave, 2370B Walsh Ave., Santa Clara, CA 95051.

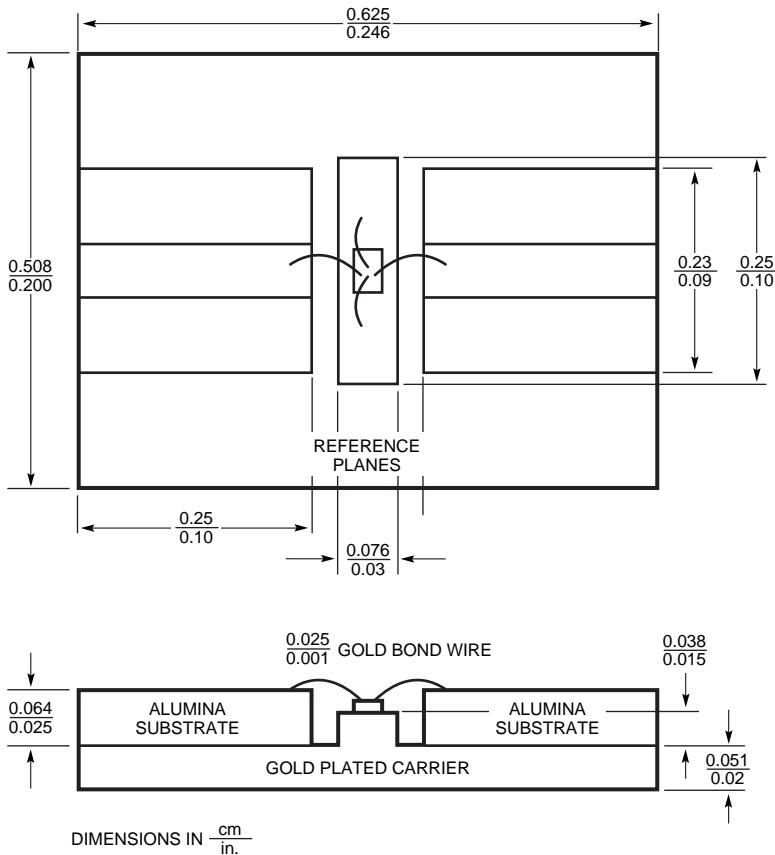


Figure 3. Test Carrier Used to Characterize Unpackaged GaAs FET Chips

frequencies between 2 and 12 GHz the points will approximately fit a straight line curve when gain in dB is plotted on a linear vertical scale against frequency plotted on a log scale horizontally. The frequency at which the unilateral power gain extrapolates to 0 dB gain is f_{\max} .

c. Gate-to-Source Capacitance – C_{gs}

This capacitance measurement is usually made at 1 MHz, and varies with the value of DC voltage applied to the gate. A zero-volt measurement is used most often to give an idea of the gate metallization area or, more precisely, the gate length. For a given device gate width, the capacitance is directly proportional to gate length. A negatively-biased gate

will result in a lower value of capacitance, because carriers have been depleted in the region under the gate. This value is more useful in estimating the gate capacitance for RF performance or device modeling.

V. Maximum Ratings

(Also refer to *Agilent Technologies High-Frequency Transistor Primer, Part I, Section II* for additional information.)

In addition to the normal maximum ratings defined for GaAs devices, which limit externally-applied stress to values below those which, if exceeded, may result in irreversible damage to the device, some manufacturers are including ratings called "recommended maximums for

continuous operation." This latter set of ratings may be interpreted as the values above which the life expectancy of the device may be shortened. Of course, in situations where the device lifetime is less important than achieving the maximum possible performance, these ratings may be intentionally exceeded through any combination of temperature, voltage or current conditions.

The following parameters normally appear on Agilent Technologies GaAs FET data sheets, and provide adequate information for most applications.

A. Voltage Ratings

GaAs FET voltage ratings are usually derived from, and usually coincide with, the minimum device breakdown voltages. However, since this is not *always* true, it has become common practice to include both maximum voltage ratings and minimum breakdown voltages on data sheets.

It can be argued that such practice erodes the meaning of maximum ratings. Since, strictly speaking, maximum ratings should not be exceeded under any circumstances, strict adherence to the voltage ratings would preclude the measurement of the breakdown voltages of any but marginal devices. In fact, drain-to-source breakdown voltage measurements may be destructive tests except when conducted using a sophisticated pulsed measurement technique. Gate-to-source and gate-to-drain breakdown voltages can be measured without damage to the device, since there is no avalanche characteristic in these breakdown phenomena.

B. Current Ratings

The maximum current ratings for GaAs FETs are derived from a number of considerations, including the current-carrying capacity of the bonding wires and the performance degradation which can be produced by excessive current causing physical changes in the active region. Maximum ratings are normally only specified for *drain* current.

C. Dissipation Ratings

Besides the individual voltage and current ratings, there is also a limit to the product of voltage and current which can be safely handled by a GaAs FET. That is, there is a power dissipation rating which must be adhered-to for any device. Since the power dissipation capability of a GaAs FET is a function of the temperature of the external environment, the power dissipation rating is specified at a specific temperature or over a stated temperature range. For the DC case, this is usually the only significant functional dependence.

In the AC case, device dissipation varies significantly with time, so that power dissipation capability becomes a generally complex function of the signal waveform. Due to the complexity of the general AC case, transistors are seldom characterized completely enough to include complete AC power dissipation rating information. Most transistors are rated only in terms of maximum continuous dissipation – the maximum DC and maximum average dissipation. This rating is typically specified in terms of a maximum continuous dissipation at or below a stated reference temperature (usually 25°C), with

a linear derating factor to be applied at higher temperatures.

Two external temperature reference points are commonly used. The one which is the more valid depends on the application. They are:

1. *Air ambient*, T_A , also known as free air temperature, since no forced-air or other "artificial" cooling is applied to the transistor. This is the air temperature in proximity to the transistor case as mounted in its normal manner.
2. *Case ambient*, T_C , which is the temperature of the point on the transistor package at which a heatsink is the most effective in reducing temperature.

D. Channel Temperature Rating

Another temperature reference point implicit in the previously-mentioned ratings, is the actual temperature at the transistor channel. The maximum internal reference temperature $T_{ch\ (max)}$ corresponds to the maximum channel temperature, since at $T_{ch\ (max)}$, the power dissipation of the transistor must be derated to zero. Strictly speaking, channel temperature is not properly classified as a *maximum* rating, since it is not an external stress under the direct control of the user – as opposed to power dissipation and external operating temperature which *are* user-controlled.

Thus, a more appropriate term for this rating would be *maximum operating temperature*. However, since it is a limiting factor in the transistor power dissipation capability, and since its use simplifies

time-varying thermal analysis, this rating still appears on many transistor data sheets.

One key factor that should be kept in mind when specifying operating bias and calculating channel temperature is that the thermal resistance of GaAs is not constant with temperature. The thermal resistance from channel to case is a function of temperature and varies directly as the thermal resistance of bulk GaAs. This temperature variation can be approximated as:

$$\begin{aligned} \theta_{jc} &= \theta_{jc}(60^\circ\text{C}) \\ \{1 &= 0.00355(T_{CH} - 60^\circ\text{C})\} \end{aligned} \quad (9)$$

where T_{CH} equals channel temperature and θ_{jc} (60°C) is the channel-to-case thermal resistance at a T_{CH} of 60°C . For a more complete discussion of thermal resistance, refer to Agilent Technologies' *High Frequency Transistor Primer Series, Part III (Thermal Properties) and Part IIIA (Thermal Resistance)*.

E. Storage Temperature Rating

This rating defines the range of temperature over which the transistor may be stored in a non-operating condition, without damage. Because of possible electrical-temperature interactions, the storage temperature range and operating temperature range do not necessarily coincide. In practice, however, they usually *do* coincide and, in the absence of stated restrictions on operating temperature range, storage temperature range may be taken to be the operating temperature range as well.

VI. Glossary of GaAs FET Terms

Active layer

The doped layer of gallium arsenide (GaAs) through which the electrons flow in a GaAs FET and upon which the source, gate and drain electrodes are placed. The region between the source and drain electrodes is known as the channel.

Avalanche breakdown

The application of excessive voltage to a semiconductor material creates an excess of high-energy (or hot) electrons. These electrons can excite additional carriers into a high-energy state, which makes the semiconductor more conductive and can, with the same voltage applied, result in a high current flow with resulting destructive breakdown of the material. Drain-to-source breakdown in a GaAs FET is an avalanche effect.

Bipolar

Refers to a transistor in which both majority and minority carriers (electrons and holes) carry current, and which is formed with PN junctions.

Breakdown voltage

The reverse bias voltage at which a rectifying junction begins to conduct a large reverse current (higher than normal reverse leakage). Reverse breakdown can be caused by avalanche breakdown (see entry) or by other electrical or thermal effects. Gate-to-source and gate-to-drain breakdown in a GaAs FET are not avalanche effects, and may take place without damage to the device so long as the reverse current is limited to a safe value.

BV_{GD}

Breakdown voltage, gate-to-drain

– The reverse breakdown characteristic of the gate-drain Schottky-barrier diode in a GaAs FET.

BV_{GD} is usually specified at some specific value of leakage current.

BV_{GS}

Breakdown voltage, gate-to-source

– The reverse breakdown characteristic of the gate-source Schottky-barrier diode. BV_{GS} is usually specified at some value of leakage current.

Depletion layer

The portion of the epitaxial layer that lies directly beneath the gate of an FET and becomes depleted of carriers (electrons) when a negative bias is applied to the gate.

Dopant

A substance added to GaAs (or silicon or other transistor base material) to make it semi-conductive.

Drain

The terminal of an FET to which electrons flow. (See also: source, gate)

C_{GS}

Capacitance, gate-to-source

– The capacitance that exists between the gate and source electrodes in a GaAs FET, and which is dependent on the Schottky diode characteristics and applied bias voltage.

Conjugate match

A transistor input or output port is conjugately matched when connected to an impedance which has the same resistance as the transistor port and a reactance of the same magnitude but opposite

sign. This means that the reactances cancel, and that maximum power transmission takes place and that there is no mismatch loss.

Epitaxial (epi) layer

A doped layer of GaAs grown on top of the substrate crystal as a continuation of the crystal lattice structure. Gallium, arsenic and other dopants are carried to the substrate surface in a variety of ways, including liquid-phase, vapor-phase and molecular beam approaches.

f_{max}

Maximum Frequency of Oscillation – The frequency at which the unilateral power gain (U) of a transistor approaches unity.

FET

Field Effect Transistor – A unipolar device in which the number of carriers available to carry current in the conducting region is controlled by the application of an electric field to the surface (in the form of a capacitor or reverse-biased diode junction) of the semiconductor. As a unipolar device, the current in an FET is carried only by the free majority carriers (in an N-channel FET, *electrons*) in the conducting channel and there is little or no current carried by the minority carriers (in an N-channel FET, *holes*). Compare this to the bipolar transistor in which both positive and negative free carriers carry approximately equal current.

GaAs

Gallium Arsenide – A type III-V (from the periodic table) compound of gallium and arsenic which has a resistivity sufficiently high to fabricate field-effect

transistors. Compared to silicon, the free carriers can reach about twice the limiting velocity with one-third the applied voltage.

GaAs FET

A field effect transistor made of gallium arsenide.

Gate

The terminal of an FET that controls the flow of current from the drain to the source. (See also: drain, source)

Gate length

The distance along which the electrons must travel when moving from source to drain. That is, length is the *shorter* of the two gate dimensions (gate width is the longer dimension). The frequency response of a GaAs FET, with all other things equal, is inversely proportional to its gate length.

Gate width

The size of the GaAs FET channel that carries current. That is, width is the longer of the two gate dimensions (gate length is the shorter dimension). The power handling capacity of a GaAs FET, with all other things equal, is directly proportional to its gate width.

G_1 db

1 dB gain compression point -- The level of gain from a device which is 1 dB less than the gain measured under small signal conditions when the device is tuned at G_1 dB. This is usually considered to be the upper limit of linear amplification. See also P_1 dB.

g_m

DC transconductance, which is the ratio of the change in the drain current to changes in gate voltage:

$$g_m = \frac{\Delta I_{ds}}{\Delta V_{gs}} \quad (10)$$

G_{NF}

Small signal gain, resulting from tuning for optimum noise figure. Also designated: G_A .

G_P

Small signal gain, resulting from tuning for optimum output power.

G_T

Transducer power gain – The insertion power gain of a transistor, with no assumptions made concerning S_{12} , S_{11} , S_{22} or the source or load impedances. The maximum value of G_T for an unconditionally stable transistor is MAG. $|S_{21}|^2 = G_T$ when the source and load impedances equal 50Ω .

G_{Tu}

Unilateral transducer power gain – Transducer power gain with S_{12} assumed equal to zero.

I_{DSS}

Saturated drain-to-source current – The current that results from a given voltage applied to the GaAs FET with the gate voltage held at zero.

I_{GD}

Gate-to-drain leakage current at a stated reverse gate-to-drain voltage.

I_{GS}

Gate-to-source leakage current at a stated reverse gate-to-source voltage.

Implanted layer

An active layer formed by the implantation of dopants directly into the substrate crystal, or an insulating layer produced by vapor-phase epitaxy.

MAG

Maximum available gain, at a frequency where the transistor is unconditionally stable and the input and output ports are simultaneously conjugately matched. Also designated: G_A (max), G_{max} .

MESFET

Metal Semiconductor Field Effect Transistor – A GaAs FET can more formally be described as a GaAs MESFET.

NF_O

A measure of the noise generated by a transistor when tuned for minimum noise figure at a given frequency. Also designated NF_{min} and $NFOpt$.

NF_{50}

Noise figure of a transistor at a given frequency, when inserted in an untuned 50Ω circuit. This figure is most often used for the calculation of noise resistance.

P_1 dB

Power output at the 1 dB gain compression point – Essentially the maximum output power available from the transistor while providing linear amplification. Also designated: P_{OUT} , P_0 -1 dB, and in numerous other ways. See also G_1 db.

P_{sat}

Saturated power output – Usually specified at some level of small signal gain compression, such as 2 dB or (most usually) 3 dB.

P_{max}

Maximum continuous power dissipation at or below a stated reference temperature (usually 25°C), or linearly derated at a higher ambient temperature.

R_{do}

Low field drain-to-source resistance – The slope of the drain I-V characteristic near the origin of the curve, and an indicator of the active channel resistivity and the drain and source contact quality.

R_N

Equivalent noise resistance, used in the GaAs FET model to predict noise figure performance.

S₁₁

S-parameter input reflection coefficient – Expresses the magnitude and phase of the input match with respect to a pure resistance of 50 ohms.

S₁₂

S-parameter reverse transfer coefficient – Expresses the reverse isolation magnitude and phase, measured with the input terminated in 50 ohms.

S₂₁

S-parameter forward transfer coefficient – Expresses the forward gain amplitude and phase, measured with the input terminated in 50 ohms.

S₂₂

S-parameter output reflection coefficient – Expresses the magnitude and phase of the output match with respect to a pure resistance of 50 ohms.

Schottky diode

A rectifying junction formed by depositing a layer of metal onto the surface of a semiconductor. This creates an electrostatic barrier which gives the metal-semiconductor interface rectifying properties, with the metal acting as the anode and the N-type semiconductor as the cathode. Since the Schottky diode is a surface device, and since its metal layer can be fabricated at the same time as ohmic (drain and source) contacts, it is used to provide the gate structure of GaAs FETs. Also designated: Schottky-barrier diode, metal-semiconductor diode, hot-carrier diode.

Source

The terminal of an FET from which electrons flow (see also: drain, gate).

T_{ch}

Channel Temperature – The measured or estimated temperature of the GaAs FET channel under operating conditions.

T_{stg}

Storage Temperature – For an unbiased transistor.

V_P

Pinchoff Voltage – The gate-to-source voltage at which the drain current is reduced to some small, specified level. Also known as V_{GS(OFF)}.

Pinchoff Voltage

See: V_P

Transconductance

See: g_m

U

Unilateral Power Gain – The power gain of a transistor amplifier when lossless feedback has been used to neutralize the reverse transfer coefficient (S₁₂) to zero; the input reflection coefficient (S₁₁) has been matched to zero with lossless circuit elements; and the output reflection coefficient has been matched to zero with lossless circuit elements. The unilateral power gain is the highest power gain which can be achieved from the transistor, and the frequency where this gain is unity (or zero dB) is f_{max}.

Γ_o***Optimum Source Reflection Coefficient***

Coefficient – The input source reflection which results in the lowest device noise figure. This value does not coincide with the S₁₁ conjugate match. Also sometimes designated Γ_{opt}.

η_{add}

Power Added Efficiency – The ratio of RF power output minus RF input power to the DC input power:

$$\eta_{\text{add}} = \frac{P_0 - P_{\text{IN}}}{P_{\text{dc}}} \cdot 100 \quad (11)$$

VII. References

1. *Measurement and Modelling of GaAs FET Chips*, Agilent Technologies Application Note ATP-1054, October, 1983.

www.semiconductor.agilent.com

Data subject to change.

Copyright © 1999 Agilent Technologies, Inc.

Obsoletes 5963-2025E

5966-0779E (11/99)



SILICON RF-DEVICES (part I)

A tutorial about CMOS

Jörgen Olsson

Uppsala University, Sweden



Outline

- **Introduction**
- **Basic function of silicon MOSFET**
- **Manufacturing of CMOS**
- **MOSFET modeling**
- **SOI-MOSFET**
- **Scaling of CMOS**
- **Future CMOS**
 - Strained-Si, SiGe, and non-classical devices
- **Summary**

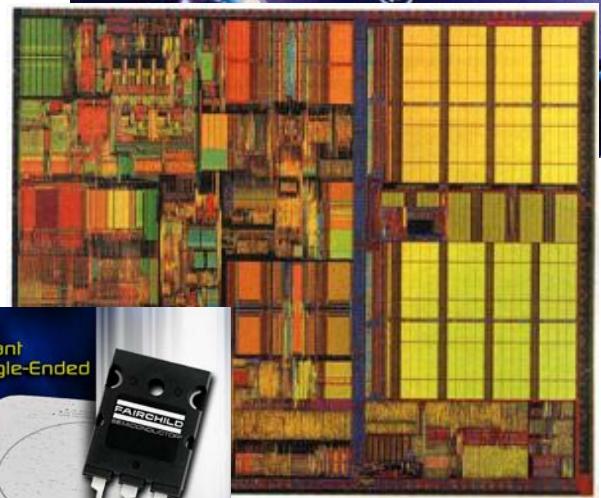


Introduction

Silicon dominates the microelectronic industry

- Microprocessors
- Memories
- Logic
- Linear circuits
- Power
- Telecommunication
- ...

Silicon also dominates for RF-applications up to around 3 GHz



Source: Fairchild

Source: IBM

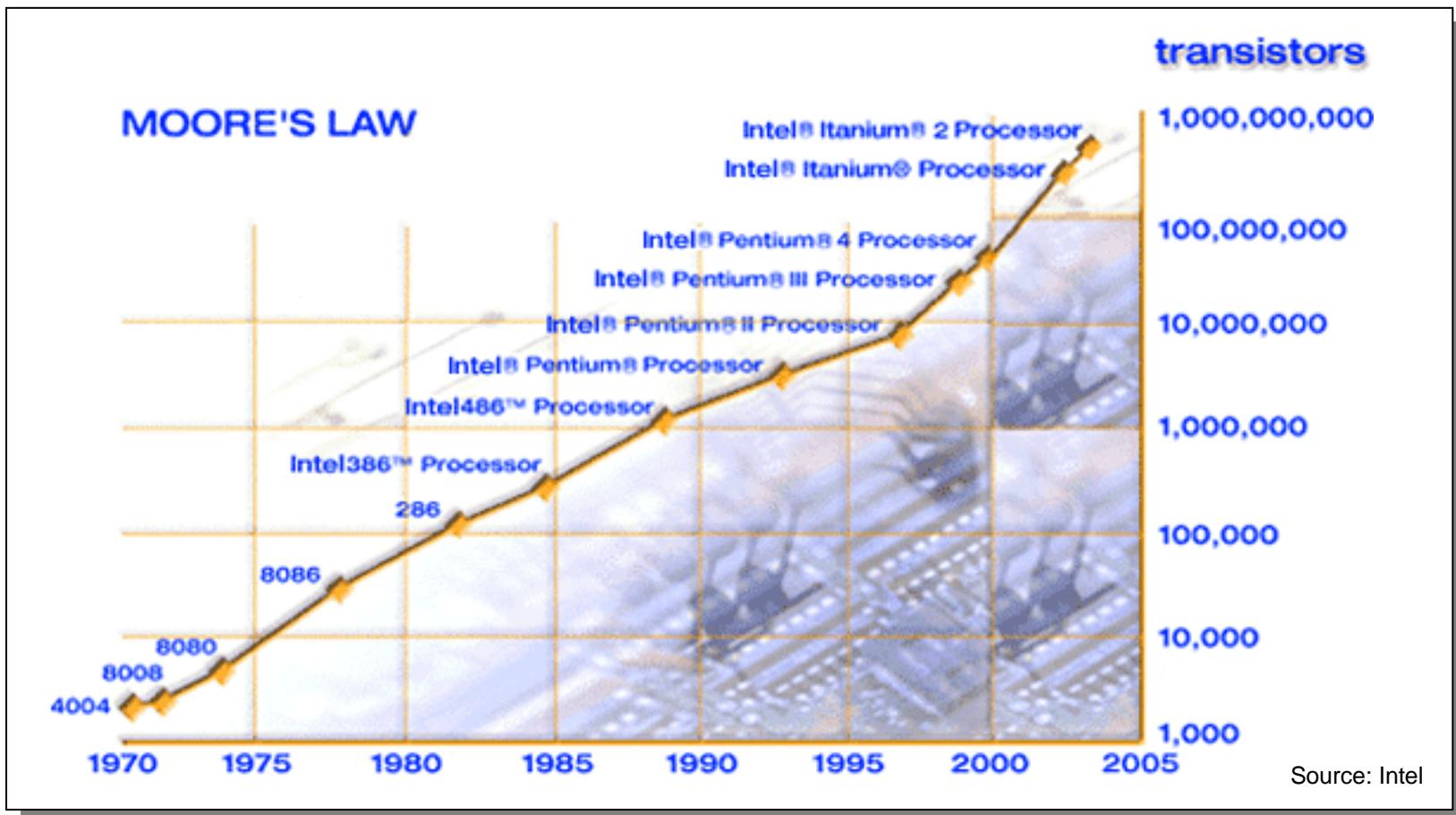


Silicon advantages

- **Many different devices**
 - MOSFET (CMOS)
 - BJT (BiCMOS)
 - IGBT
 - DMOS
 - etc...
- **Integration of a large variety of different types of devices on the same piece of silicon enables high functionality**
- **Enormous effort drives continuous development**
- **Very mature technologies – high yield**
- **Low cost!**



Enormous development of silicon technology





Silicon RF devices

- **Smaller dimensions have enabled RF-silicon technologies**
- **Low voltage / low power (RFIC)**
 - CMOS
 - Bipolar
 - BiCMOS
 - SiGe HBT
 - BiCMOS (SiGe)
- **High voltage / high power (discrete devices)**
 - LDMOS
 - SiGe HBT



Silicon for RF (applications)

Microwave applications:

- Cell phones (0.85-2.6 GHz)
- GPS (1.8 GHz)
- WLAN (2.4 GHz)
- Bluetooth (2.4 GHz)
- WLAN (5 GHz)
- DBS (12 GHz)
- HiperLink (17 GHz)
- LMDS (27-35 GHz)
- MVDS (44 GHz)
- CAR (77 GHz)
- Radio astronomy (>100 GHz)

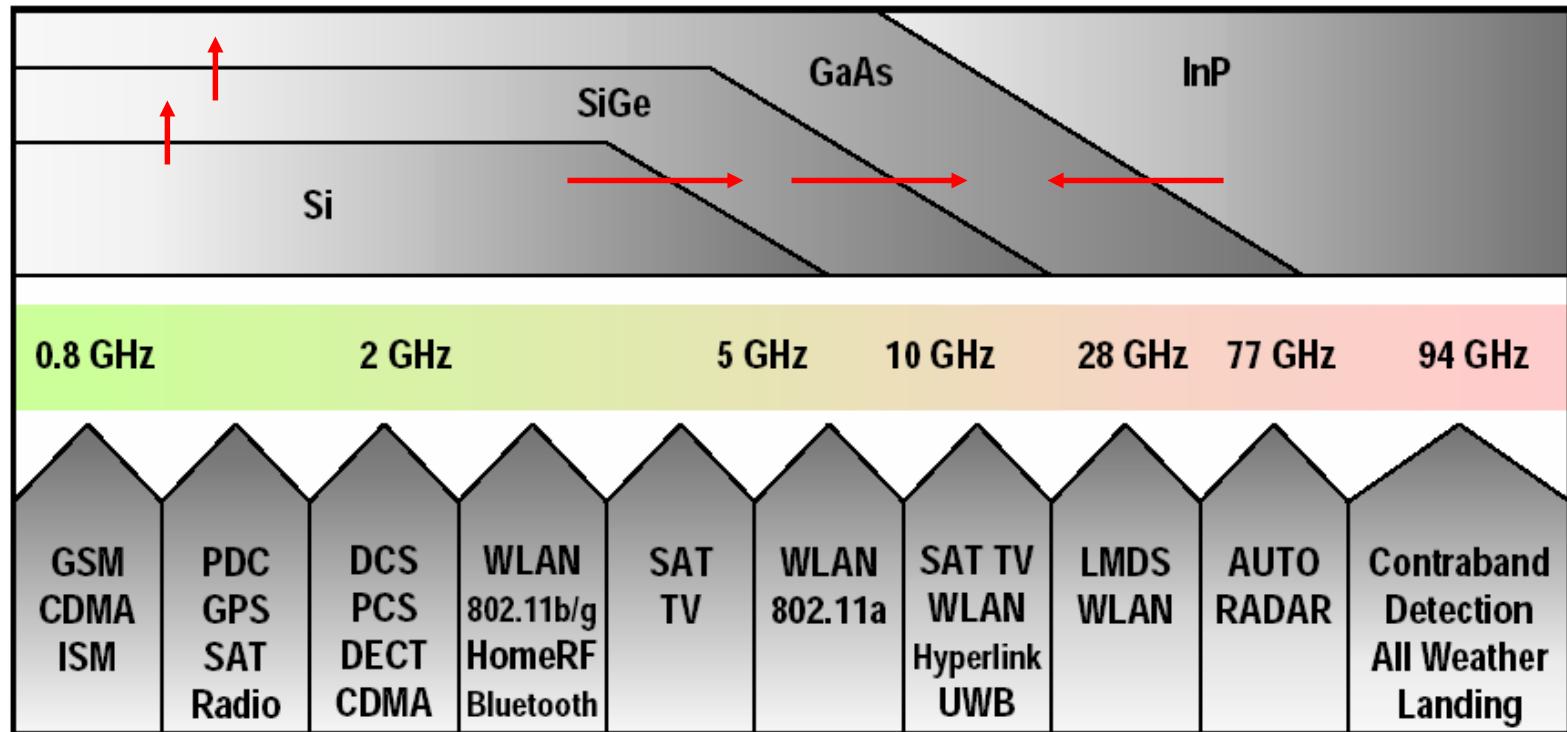
Silicon dominates up to around 3-5 GHz.

This is also the field for the real mass markets.

Note: Microprocessors today operates above 3 GHz!



RF trends: Silicon expands



Source: ITRS 2003



So what is RF CMOS?

- The term **RF-CMOS** has been around since the mid-1990s
- **CMOS is for low voltage**
- **CMOS is also integration, high yield and low cost!**
- **Circuit view**
 - CMOS implementation of already existing RF bipolar circuits
 - Develop new RF-circuit topologies with CMOS
 - Layout optimized for analog/RF circuits
- **Technology view**
 - Focus on analog/RF performance of MOSFETs
 - Modify/develop new CMOS processes optimized for RF
 - Substrate engineering for RF
 - Integration of passives



Typical RF-CMOS applications

Pure RF-CMOS chips are now in production at several companies.



CDMA2000 chipset
0.25 µm CMOS
QUALCOMM



Bluetooth transceiver
0.25 µm CMOS
GCT Semiconductor



Single-chip CMOS
GSM/GPRS transceiver
Silicon Laboratories



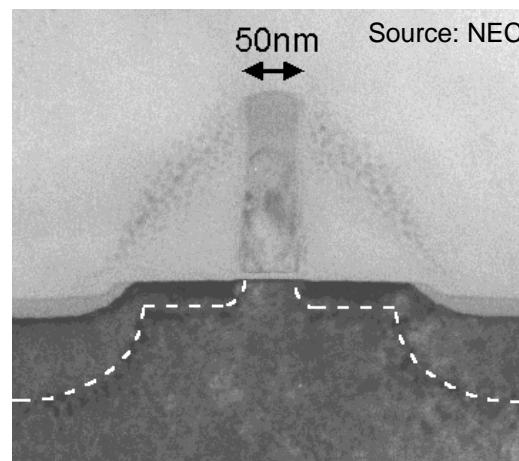
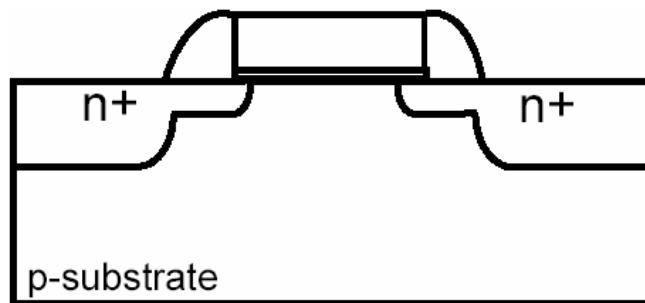
2.4-5 GHz IEEE802.11a/b/g
WLAN transceiver
0.18 µm CMOS
Spirea



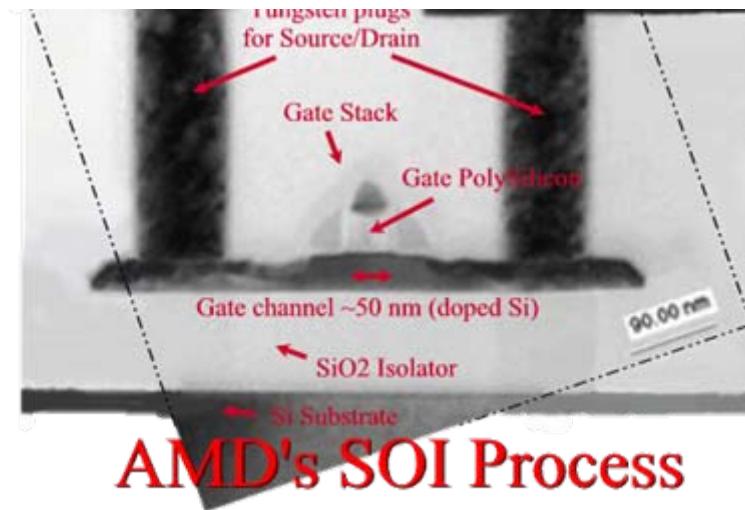
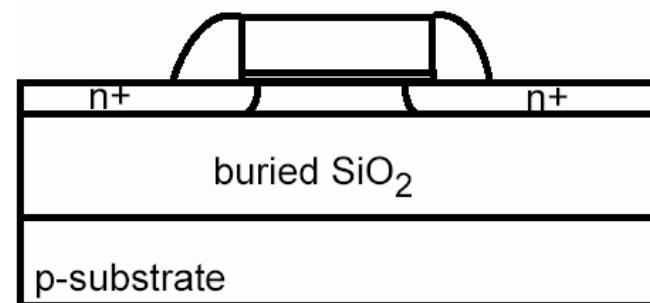
GSM/GPRS transceiver
0.13 µm CMOS
Infineon Technologies

MOSFETs in production today (90 nm node) During 2006 the 65 nm node enters production

Bulk MOSFET



SOI MOSFET





Outline

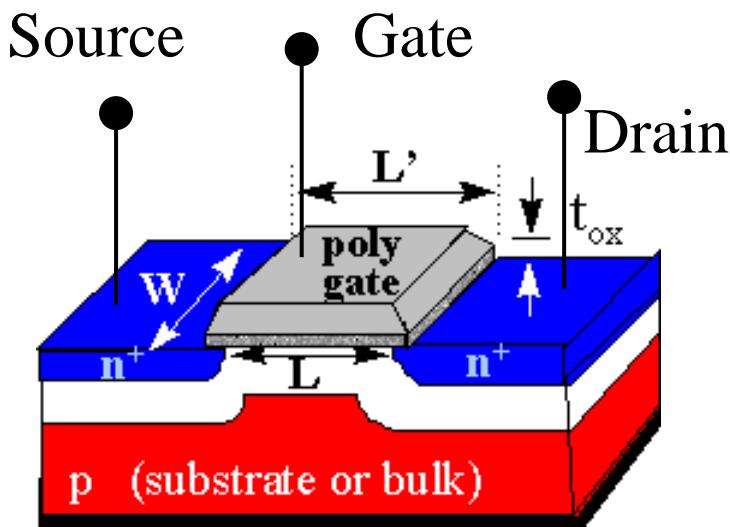


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MOSFET basic theory

MOSFET structure (NMOS)



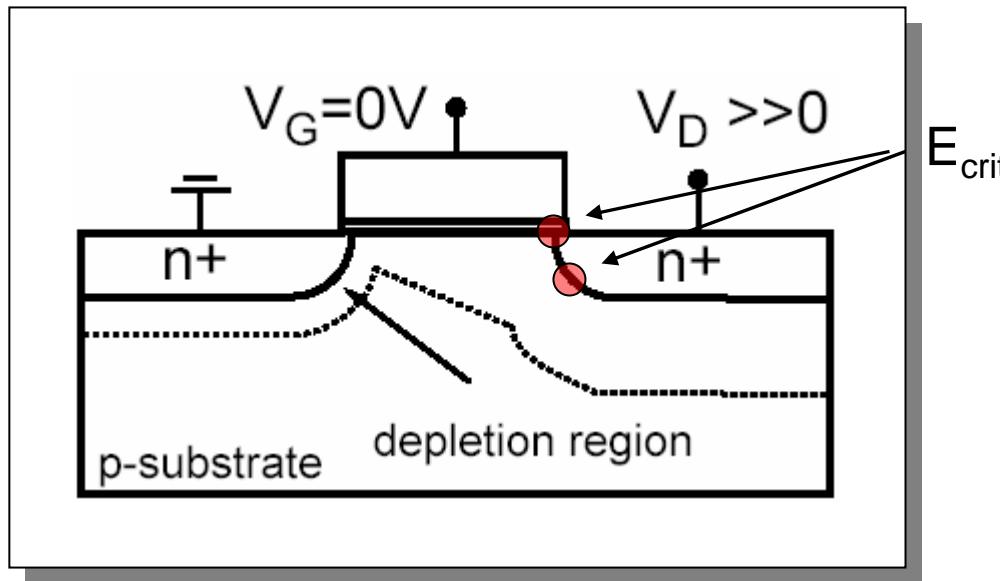
The MOSFET is a 4-terminal device: Source, Drain, Gate, Bulk

Dopant type determines the transistor type: PMOS (hole conduction) or NMOS (electron conduction)

Three basic operation regimes: Off-region, Linear (On-region), and Saturation region



MOSFET off-state



At high V_{DS} critical electrical field strength (E_{Crit}) can be reached in the semiconductor, which leads to electrical breakdown

BV =breakdown voltage

$E_{Crit}(Si) \approx 3 \times 10^5 \text{ V/cm}$

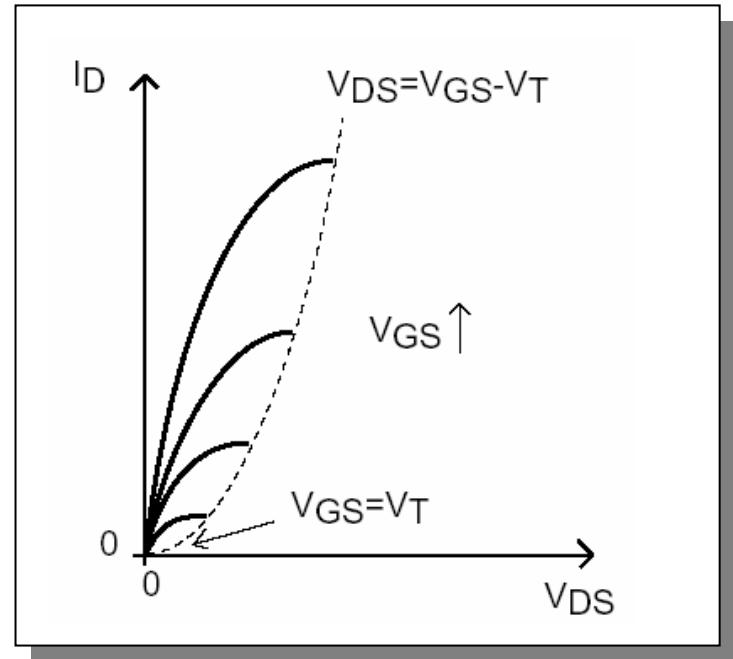
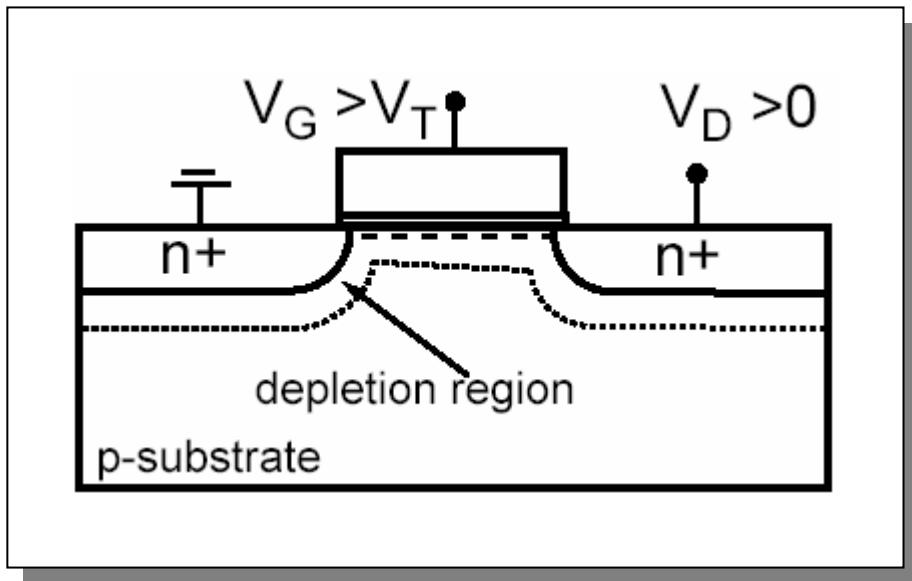
$E_{Crit}(SiO_2) \approx 1 \times 10^7 \text{ V/cm}$

30 nm channel length can support 1 V!

**No dielectric breakdown for 1 nm gate oxide @ 1 V !
(But other problems)**



MOSFET Linear region

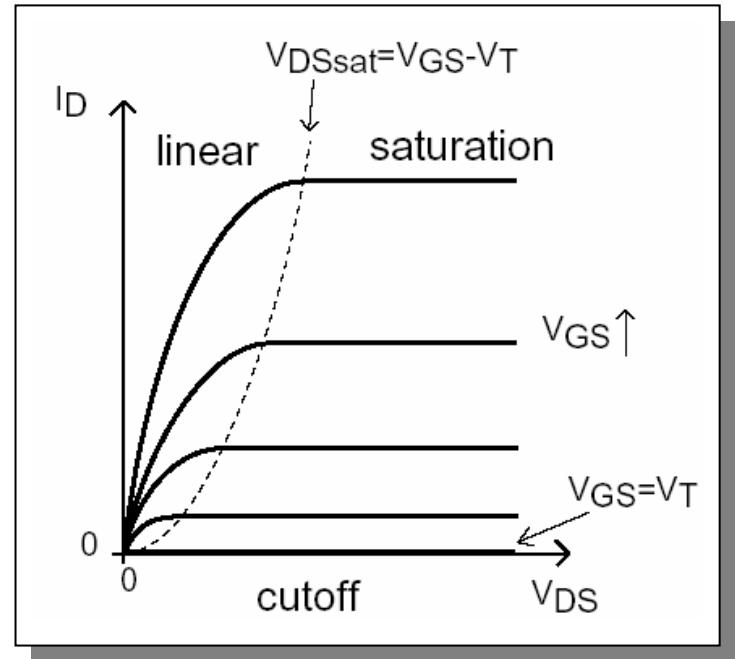
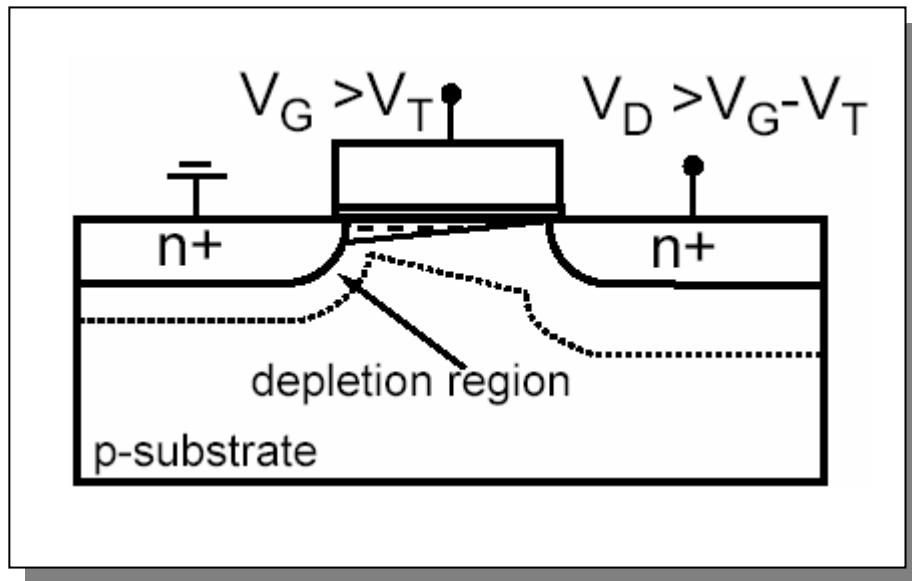


At $V_{GS} > V_T$ an inversion channel is formed underneath the gate and connects the source and drain regions

$$\text{In general: } I_D = \frac{W}{L} \mu_n C_{ox} \left(V_{GS} - \frac{V_{DS}}{2} - V_T \right) V_{DS}$$

$$\text{For small } V_{DS}: \quad I_D = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T) V_{DS}$$

MOSFET Saturation region

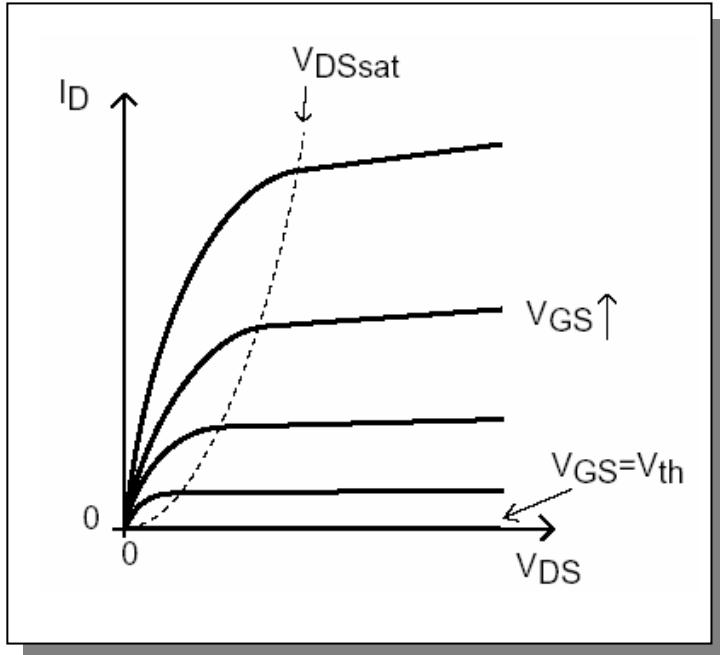


As V_{DS} is increased in the linear region ohmic drop de-biases the channel, until it is pinched-off at the drain side. The current then saturates at I_{Dsat} .

$$\text{In general: } I_{Dsat} = \frac{W}{2L} \mu_n C_{ox} (V_{GS} - V_T)^2$$



MOSFET in reality (long channel)



$$I_{Dsat} = \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T)^2 [1 + \lambda(V_{DS} - V_{DSsat})]$$

$$\frac{\Delta L}{L} = \lambda(V_{DS} - V_{DSsat})$$

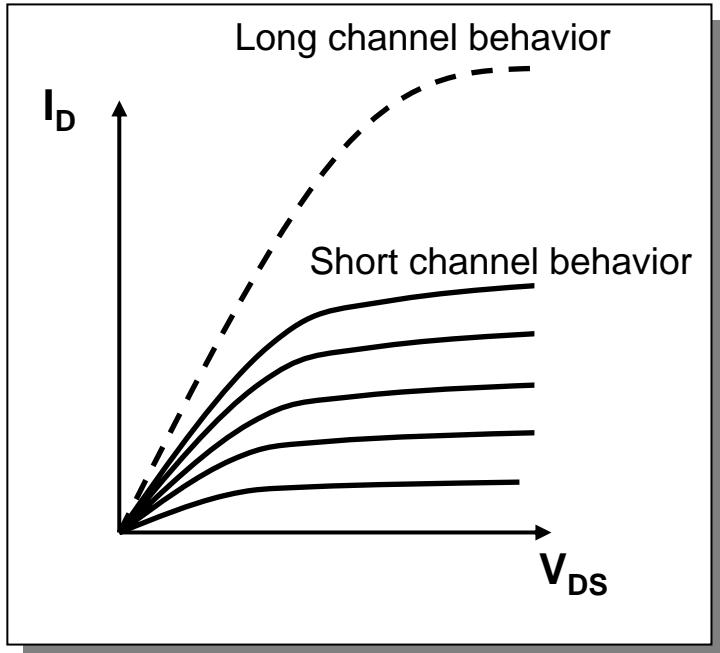
$$g_m = \frac{\partial I_D}{\partial V_G} \propto \mu_n C_{ox} \frac{W}{L}$$

$$\frac{1}{R_{out}} \approx g_{ds} = \frac{\partial I_D}{\partial V_D}$$

Due to increasing V_{DS} the electrical channel length is changes (the pinch-off point is moved towards the source)
“Channel length modulation”

Basic equations for long channel MOSFET

MOSFET in reality (short channel)



$$I_{Dsat} = C_{OX} W V_{sat} (V_{GS} - V_T)$$

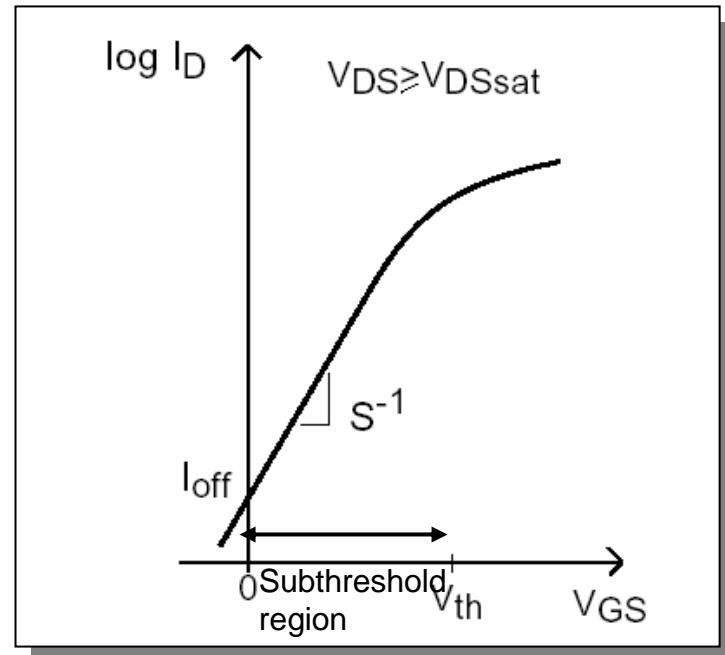
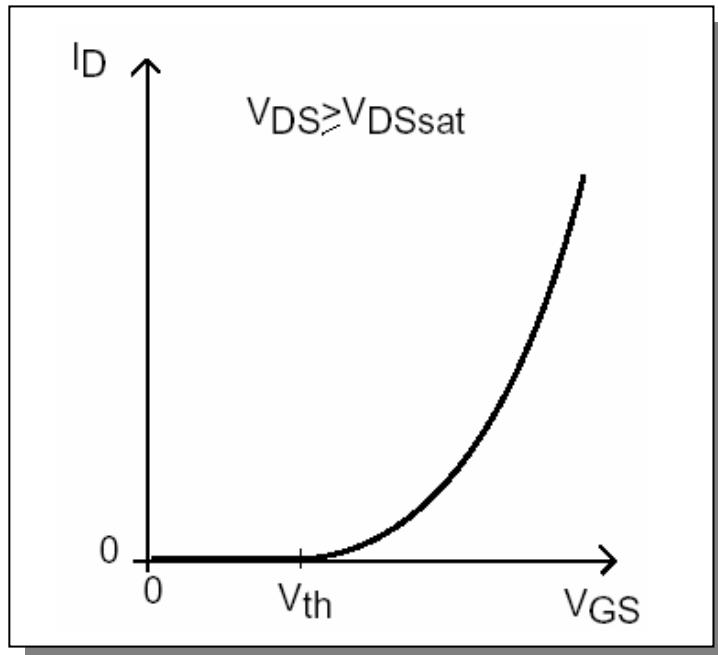
$$g_m = C_{OX} W V_{sat}$$

(Incomplete) list of MOSFET short channel effects:

- V_T variations with channel length
- Drain-induced-barrier-lowering (DIBL)
- Mobility degradation with high vertical field
- Velocity saturation – carrier mobility drops at field higher than $1 \text{ V}/\mu\text{m}$
- Hot carrier effects impact ionization

Basic equations for short channel MOSFET

MOSFET subthreshold region



$$I_D \propto \exp \frac{q(V_{GS} - V_T)}{nkT}$$

$$S = \frac{nkT}{q} \ln 10 \quad n = \left(1 + \frac{C_{dm}}{C_{ox}} \right)$$

If $n=1$, $S=60$ mV/dec ($T=300$ K)

In modern well designed devices
 $S \approx 70-90$ mV/dec



Basic MOSFET High frequency equations

Intrinsic MOSFET

$$f_T = \frac{g_m}{2\pi C_{gg}}$$

$$g_m = \frac{\partial I_D}{\partial V_G} \propto \mu_n C_{ox} \frac{W}{L}$$

$$f_{MAX} \approx f_T \sqrt{\frac{R_{out}}{R_G + R_i}}$$

$$\frac{1}{R_{out}} \approx g_{ds} = \frac{\partial I_D}{\partial V_D}$$

Extrinsic MOSFET

$$f_T = \frac{1}{2\pi} \frac{g_m}{C_{gg} + C_{gso} + C_{gdo} + C_{par}}$$

$$f_{MAX} = \frac{f_T}{2\sqrt{(R_g + R_i)(g_{ds} + 2\pi f_T C_{gdo})}}$$

$$NF_{min} = 1 + K \frac{f}{f_T} \sqrt{g_m (R_g + R_i + R_s)}$$

$$V_{IP3} \approx \sqrt{\frac{g_m}{g_{m3}}} \quad g_{m3} = \frac{\partial^3 I_{ds}}{\partial V_{gs}^3}$$



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CMOS manufacturing

Modern CMOS processes consist of several hundreds of process steps.

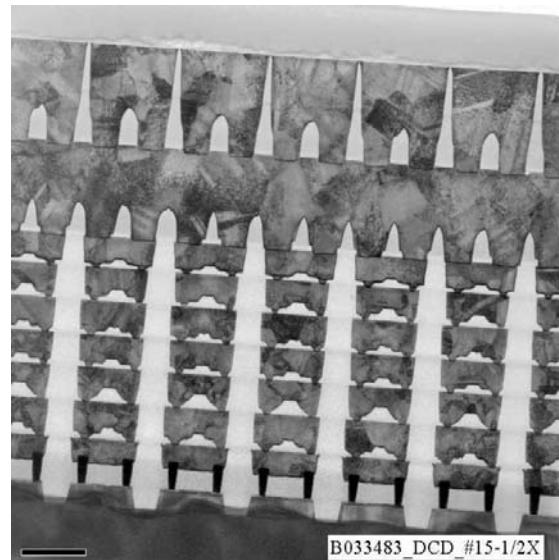
Manufacturing in very clean environment (class 1)



Fab 30
Cleanroom fab
Source: AMD

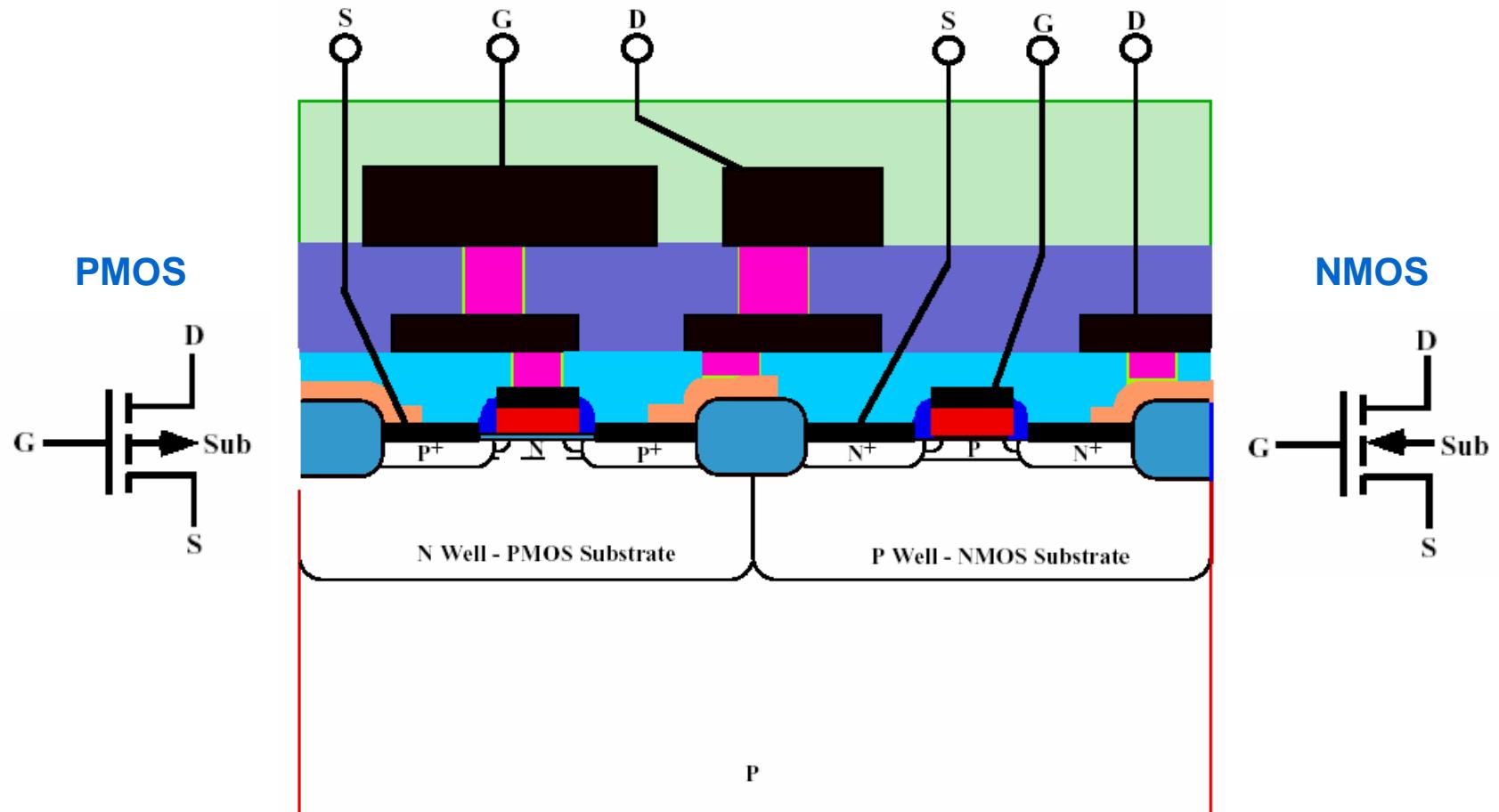
Current state-of-the-art CMOS in production is the 90/65 nm technology mode

Physical gate length less than 50 nm!



9 metal layer
interconnect
Source: TSMC

Process example: Two metal layer CMOS

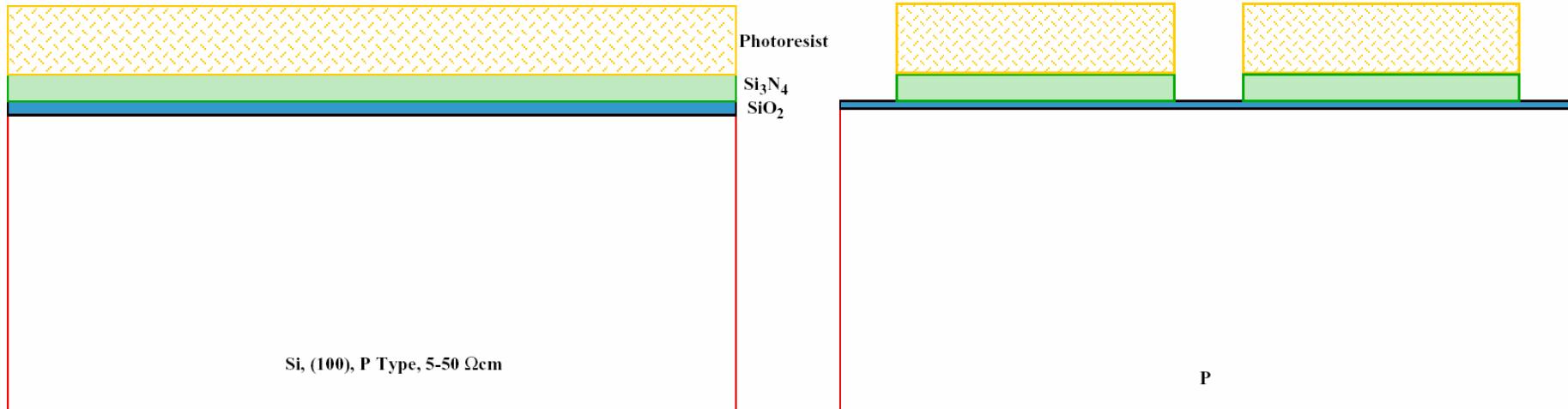


Process flow from: SILICON VLSI TECHNOLOGY
Fundamentals, Practice and Modeling
By Plummer, Deal and Griffin



Substrate: Si (100): p/p+ epi, p, or for RF High resistivity ($> 50 \Omega\text{cm}$)

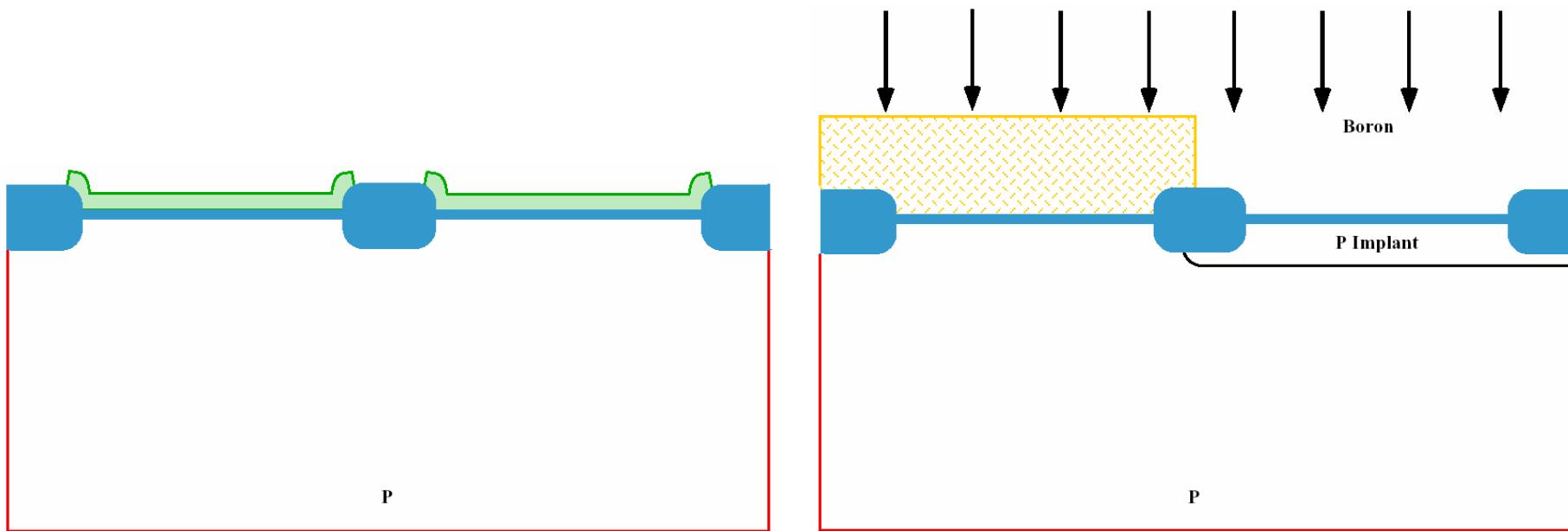
Mask #1: Dry etch to define active area





Grow field oxide ($\approx 0.5 \mu\text{m}$) with LOCOS process

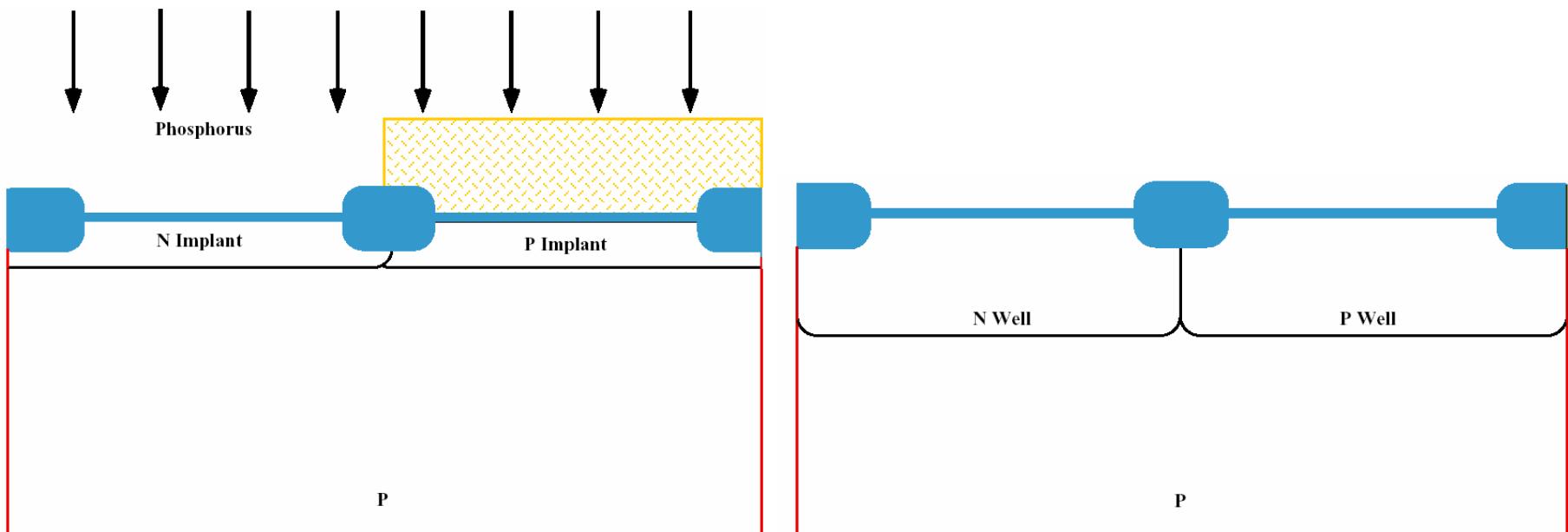
Mask #2: Boron implantation to form p-wells for NMOS devices





Mask #3: Phosphorus implantation to form n-wells for PMOS devices

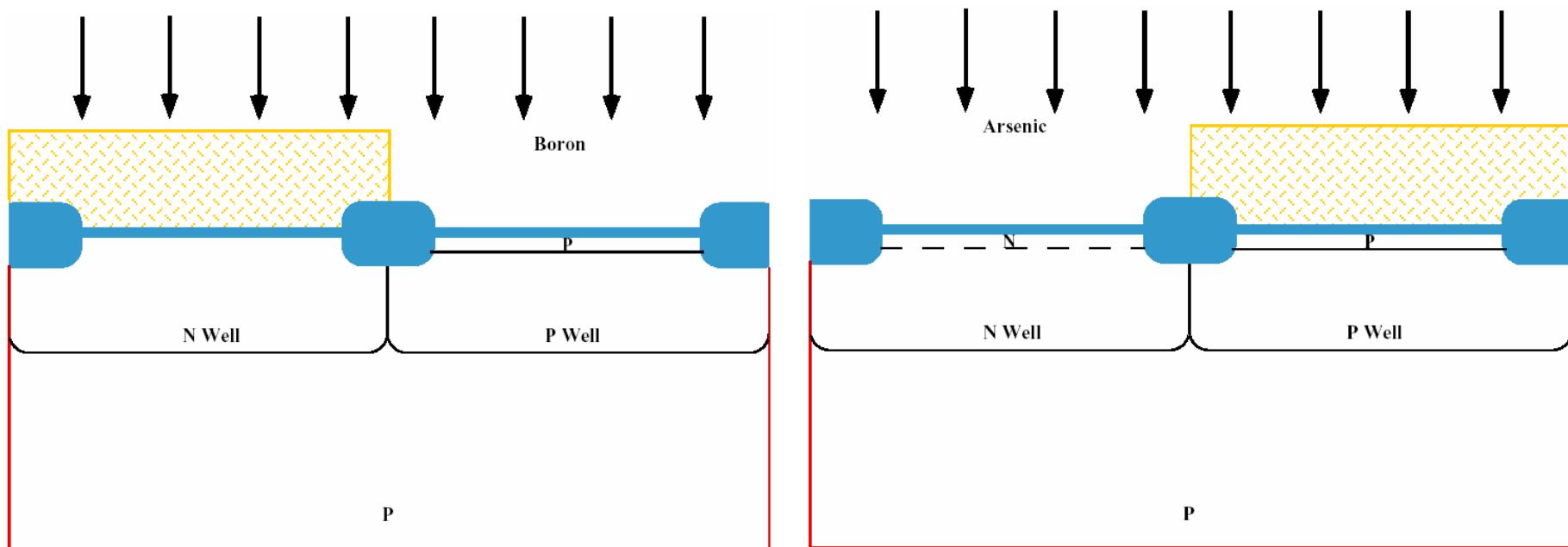
High temperature drive-in to diffuse wells





Mask #4: Adjust threshold voltage for NMOS

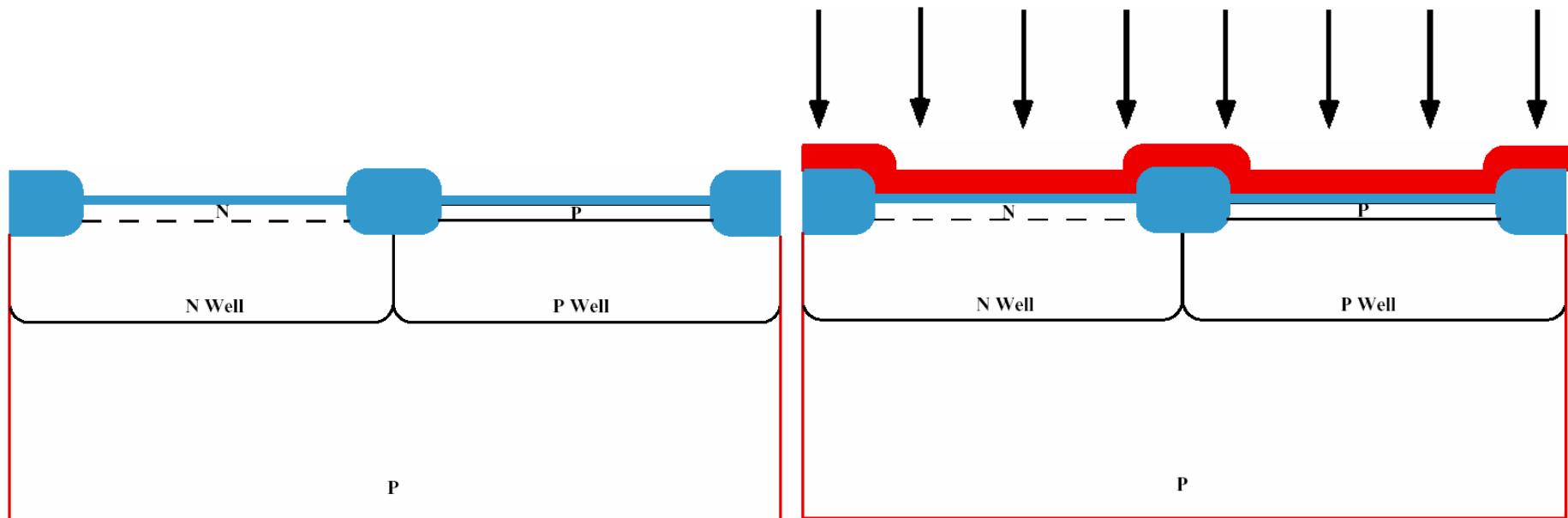
Mask #5: Adjust threshold voltage for PMOS





Strip oxide on active area and grow thin gate oxide 20-50 Å

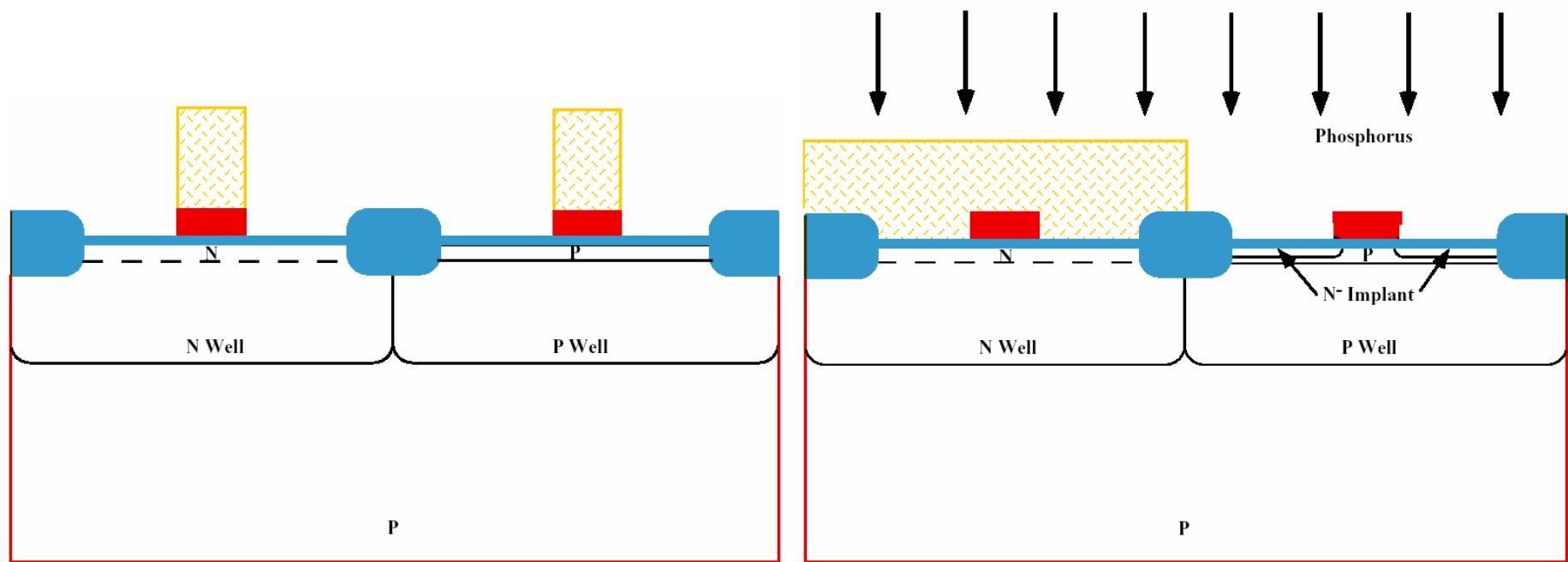
Deposit polysilicon and implant high dose As or P





Mask #6: Dry etch to form polysilicon MOS gates

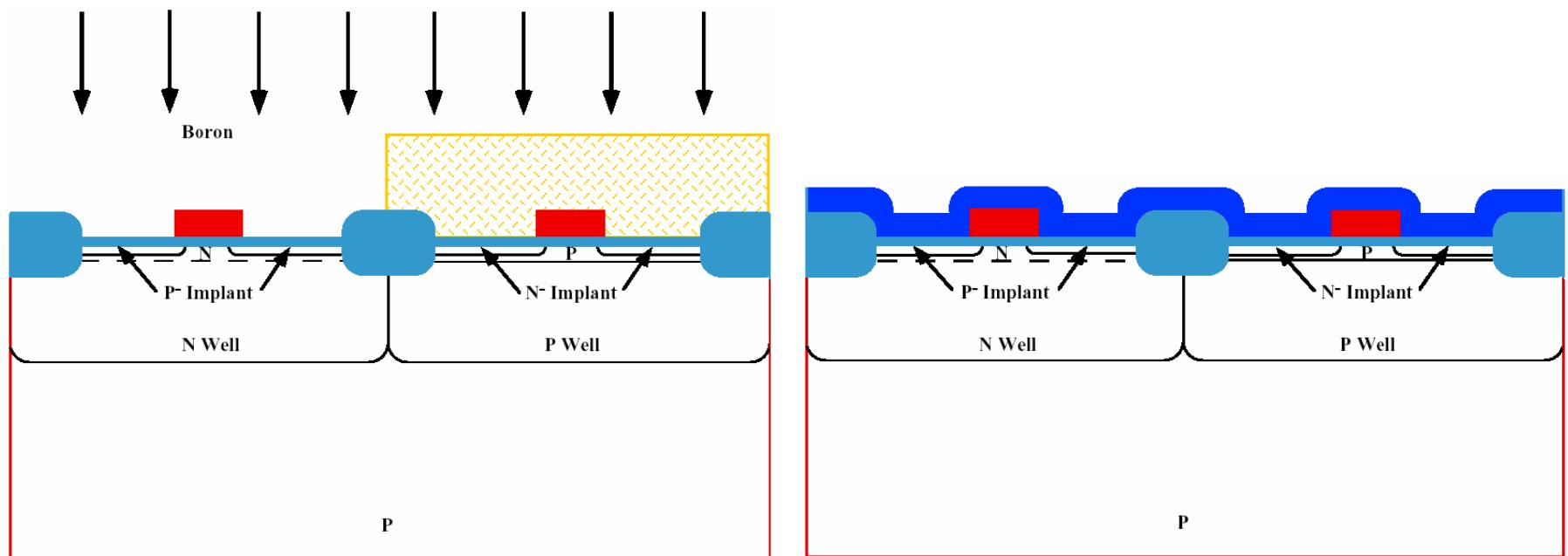
Mask #7: Implant P or As to form shallow LDD regions in the NMOS devices





Mask #8: Implant B to form shallow LDD regions in the PMOS devices

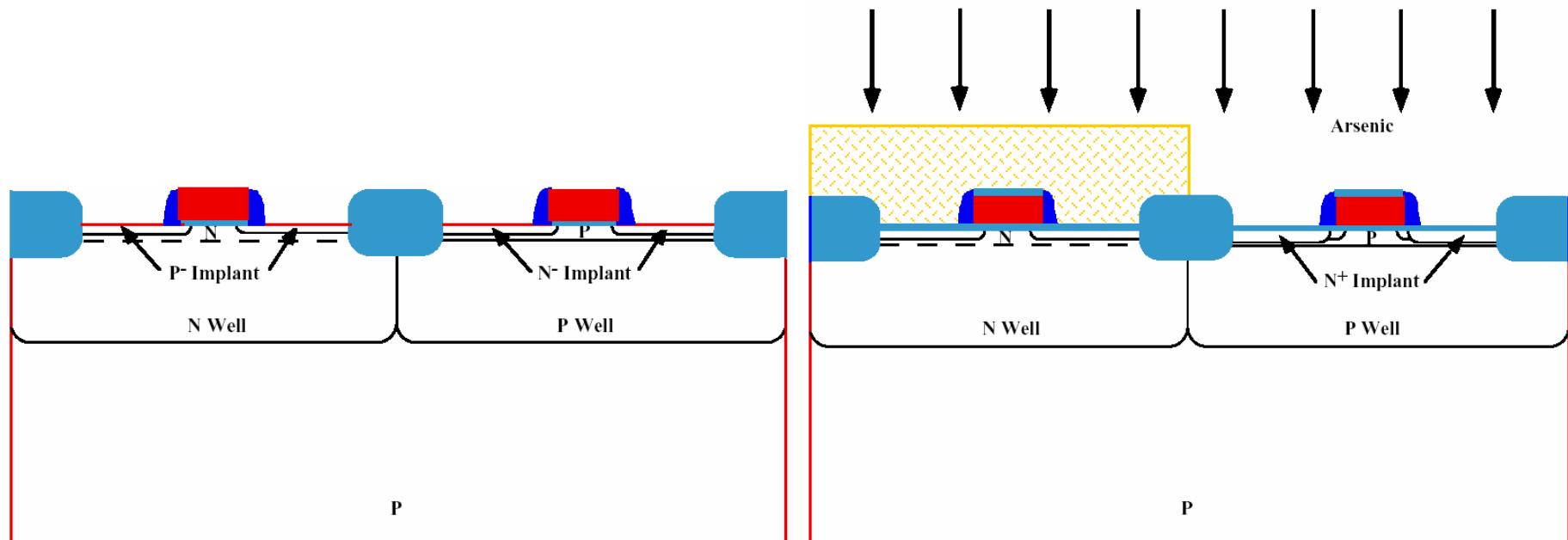
Conformal deposition of SiO_2 ($\approx 0.5 \mu\text{m}$)





Anisotropic dry etch of SiO_2 to form sidewall spacers along the edges of the gate polysilicon

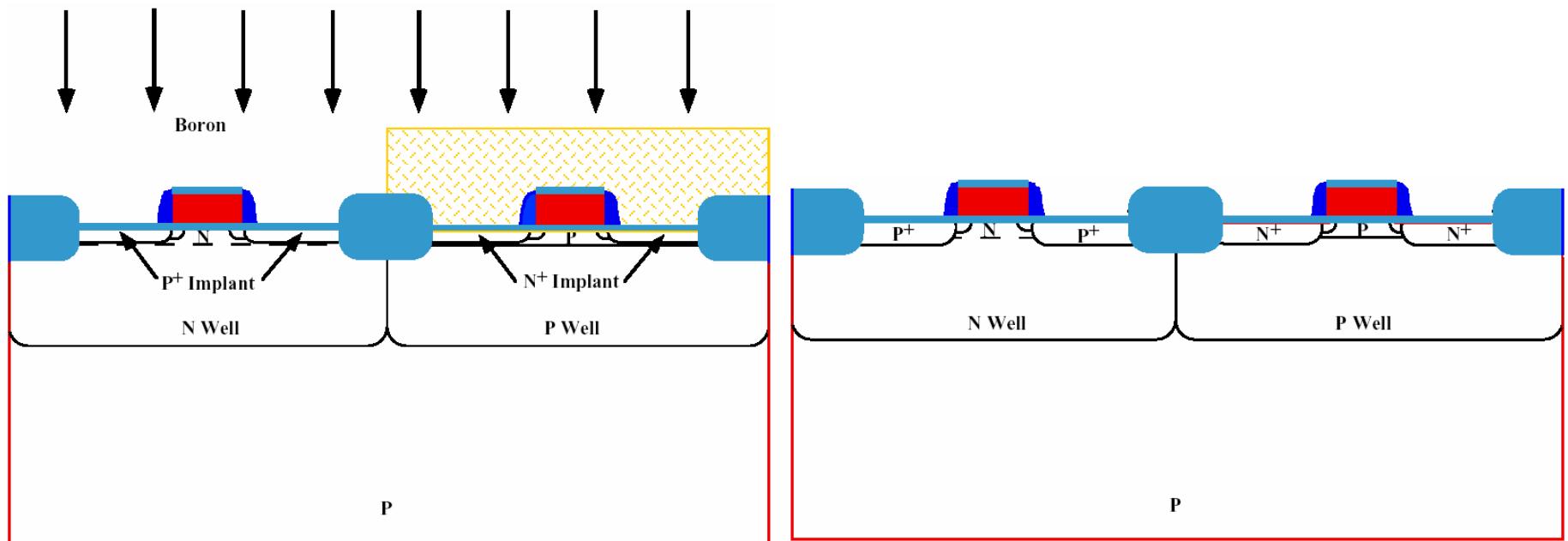
Mask #9: High dose implantation of S/D in NMOS





Mask #10: High dose implantation of S/D in PMOS

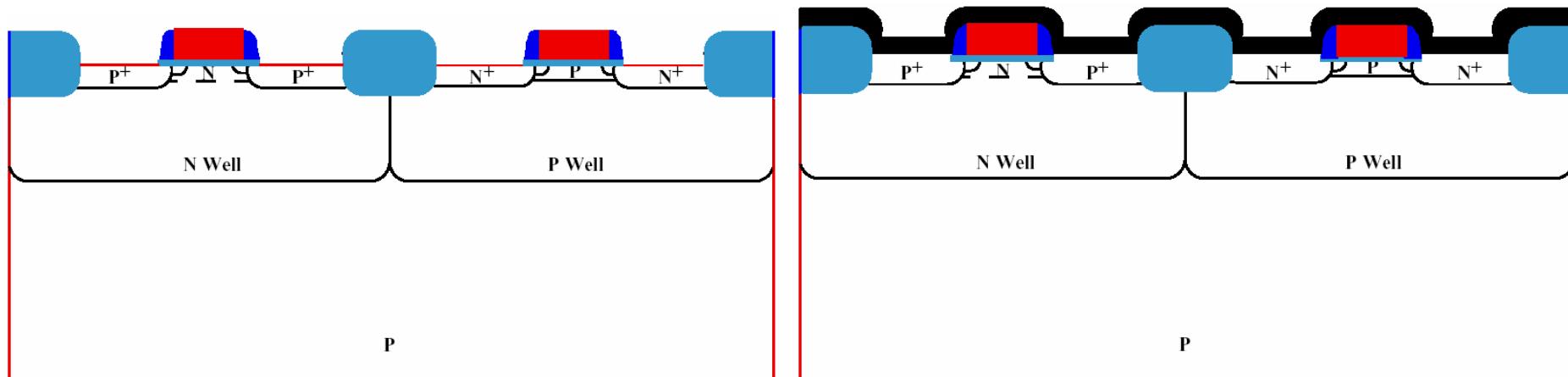
Final high temperature anneal (RTA) to activate dopants and repair implantation damage





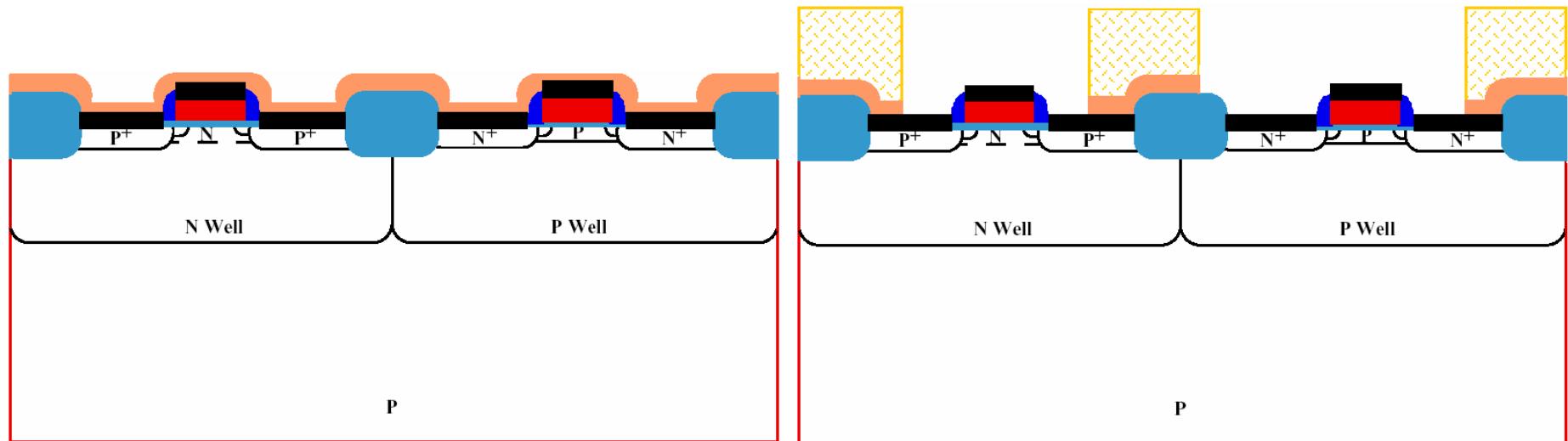
Unmasked etch of SiO_2 to expose silicon and poly in order to form contacts

Sputter deposition of about 100 nm Ti (or Co)



Anneal in N_2 ambient to form $TiSi_2$ and TiN .
Typically 1 min at 600 °C.

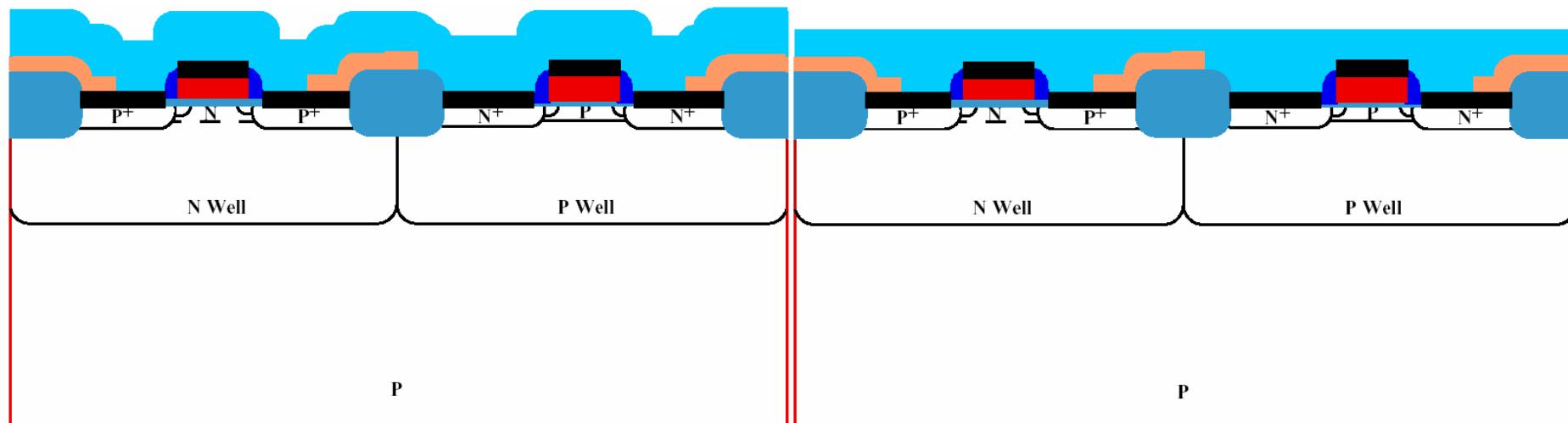
Mask #11: Etch TiN to form local interconnects





Conformal deposition of around 1 μm SiO_2

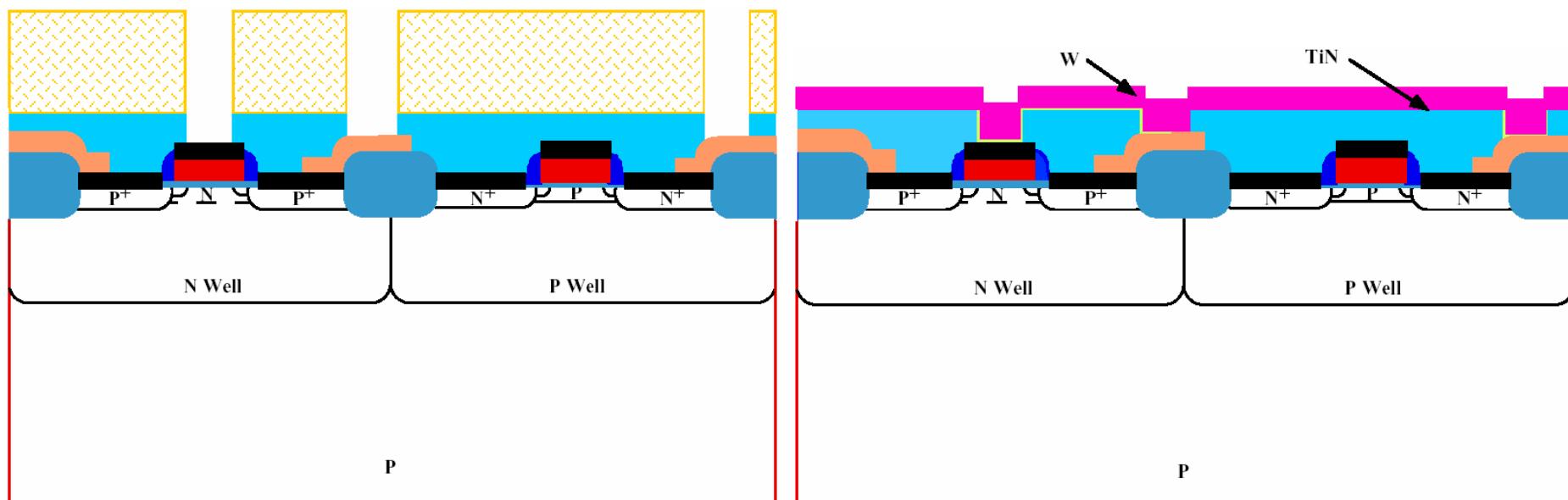
Chemical Mechanical Polishing (CMP) of the oxide to planarize the wafer surface





Mask #12: Etch oxide to form contact holes

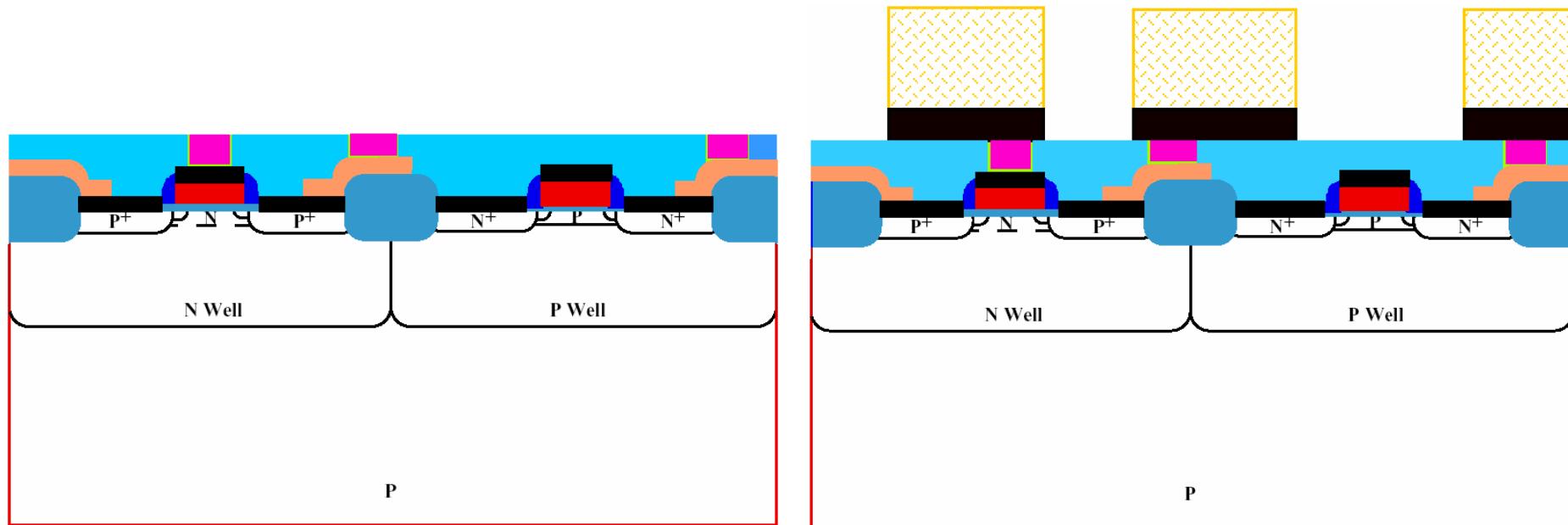
Deposition of thin (10-30 nm) TiN barrier layer
followed by CVD of W





CMP of W to planarize wafer surface

Deposition of Al followed by mask #13 to dry etch the first metal layer

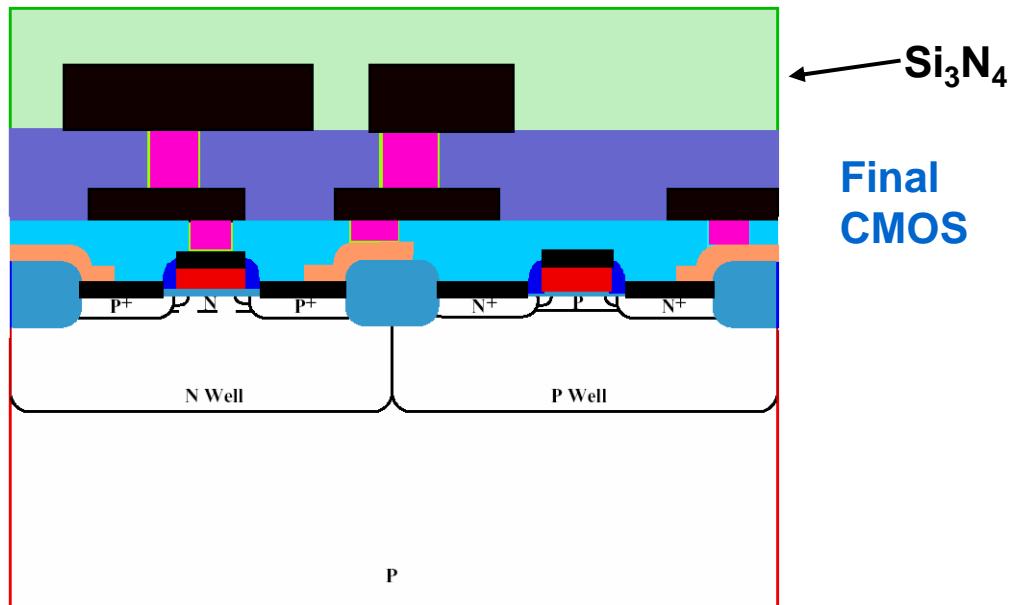




Interlevel dielectric is deposited and etched (mask #14) and the process with TiN/W and CMP is repeated.

Deposition of Al followed by mask #15 to dry etch the second metal layer.

Mask #16 is used to open the passivation layer





Outline

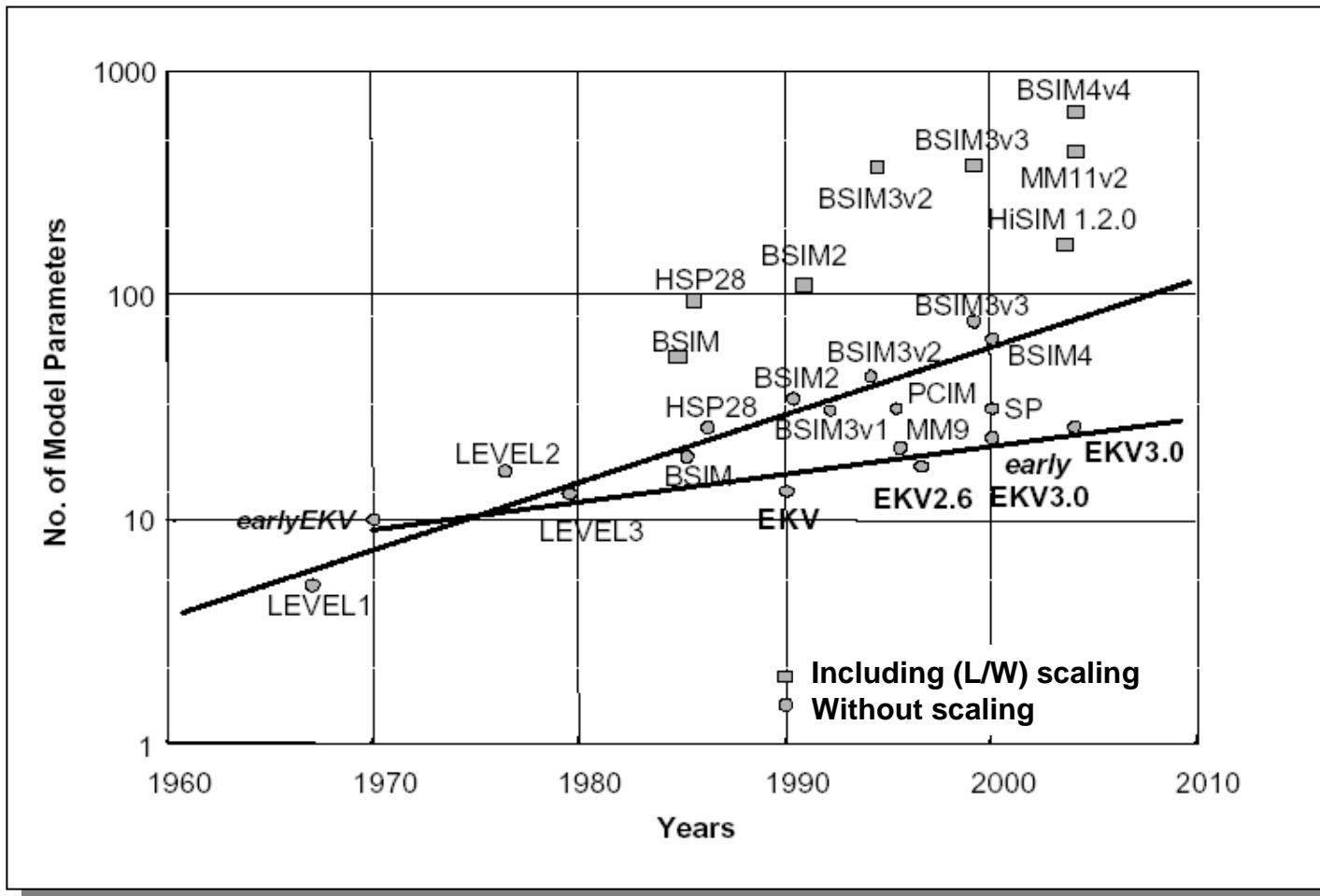
- Introduction
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MOSFET modeling

- In general CMOS circuits are simulated with a Spice based circuit simulators
- Major MOSFET Spice compact models:
 - BSIM3v3
 - BSIM4
 - EKV
 - MM11
- The models take into account small-size effects in state-of-the-art submicron MOS technology
- Models proven to work below 100 nm

Number of model parameters vs. time





Comparison

MODEL	Inversion model	Drain current	Reference	QM effects
BSIM3v3	V_T -based	Drift	Source	Yes
BSIM4	V_T -based	Drift	Source	Yes
MM9	V_T -based	Drift	Source	No
MM11	ϕ_s -based	Drift & Diff.	Bulk	Yes
EKV 3.0	Hybrid	Drift	Bulk	Yes

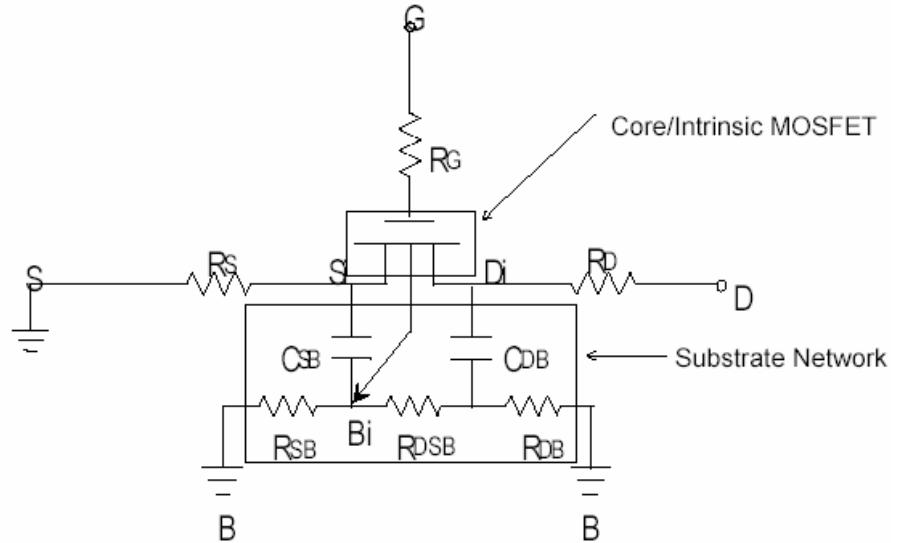


RF model with BSIM3v3

Some models do not include parasitic elements which are important for the RF ($f > 1$ GHz) performance.

A sub-circuit extension to the BSIM3v3 solves the problem

BSIM4 includes these effects, as well as, improved noise models



RG	Gate resistance
RS	Source resistance
RD	Drain resistance
RSB	Substrate resistance between source and drain
RDB	Substrate resistance between drain and bulk
RDSB	Substrate resistance between drain and source underneath the channel
CDB	Capacitance between intrinsic drain and bulk
CSB	Capacitance between intrinsic source and bulk



Recent development

- **Dec. 2005. PSP model was selected for standardization by the Compact Model Council (CMC)**
- **Effort by Penn State University and Philips**
- **Objectives of the PSP project:**
 - Merge and further develop the best features of the two most advanced Surface-Potential-Based Models: SP and MM11
 - Create the most advanced engineering MOSFET model for circuit design applications
 - Provide the modeling capabilities down to 65nm node and beyond (in the nearest future)
- **The PSP model is now being further evaluated and developed**



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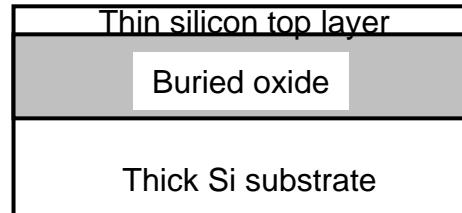


SOI MOSFET

Silicon-on-insulator as substrate material enables improved or novel device structures

Common SOI materials today with very high quality:

- B-SOI (bonded SOI)
- SIMOX
- Smart-Cut®
- Eltran®
- SOS (Silicon-on-Sapphire); is not very common, but used in a few RF-CMOS processes



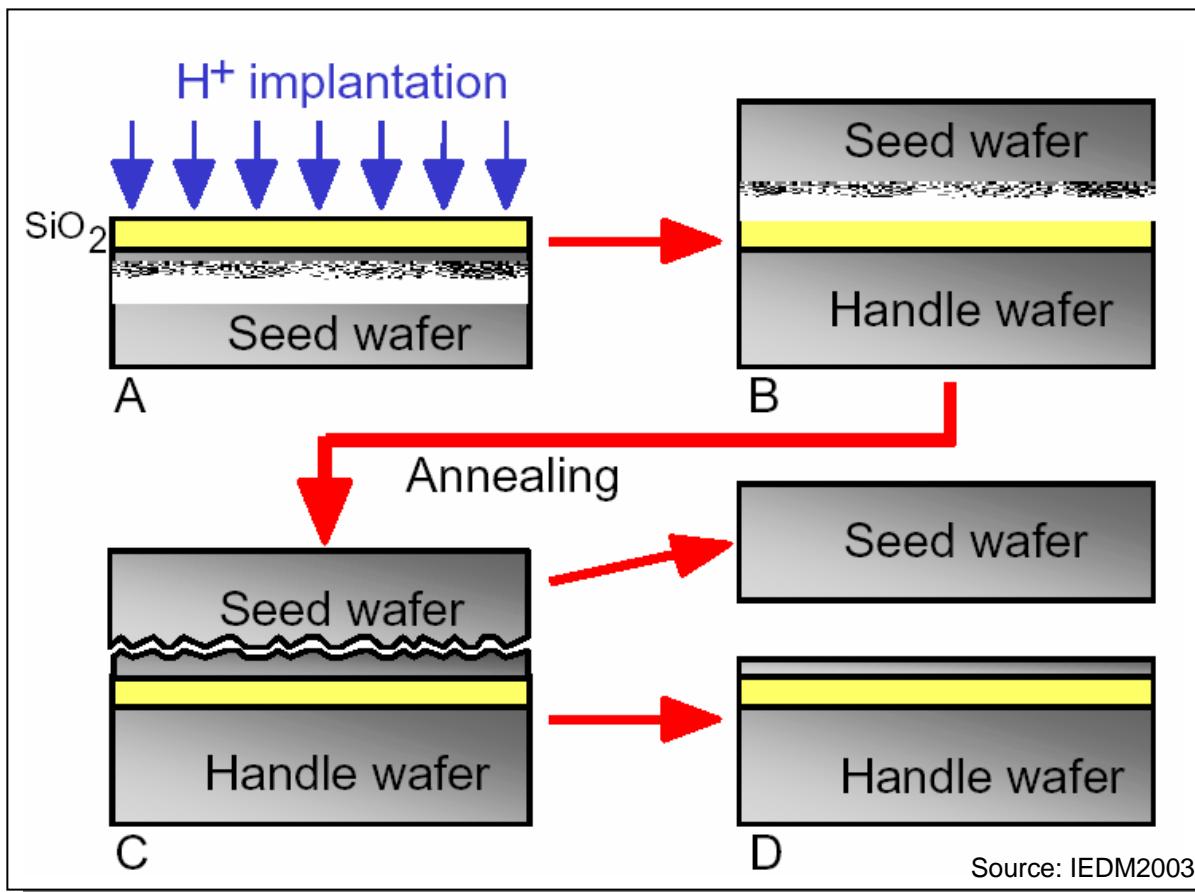
SOI advantages:

- Lower leakage currents
- Reduced process complexity
- Reduced parasitic capacitances
- Higher circuit speed
- 300 mm wafers available

SOI disadvantages:

- Availability
- Thickness uniformity
- Possible thermal problem

Smart-Cut® process



A: Hydrogen implantation

B: Wafer bonding to handle wafer

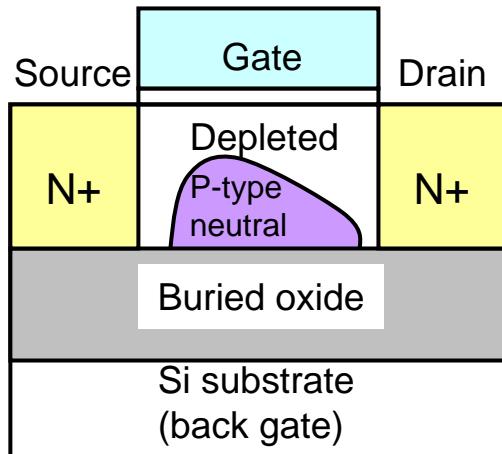
C: High temperature anneal to split the wafers

D: Polish both wafers

Wafers A to be reused as handle wafer



Types of SOI MOSFETs (I)

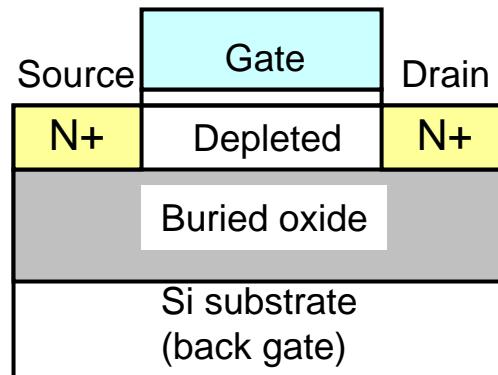


Partially depleted (PD) SOI MOSFET

Typical Si thickness: 100-340 nm

Typical BOX thickness: 100-400 nm

PD-SOI CMOS is now in mass production



Fully depleted (FD) SOI MOSFET

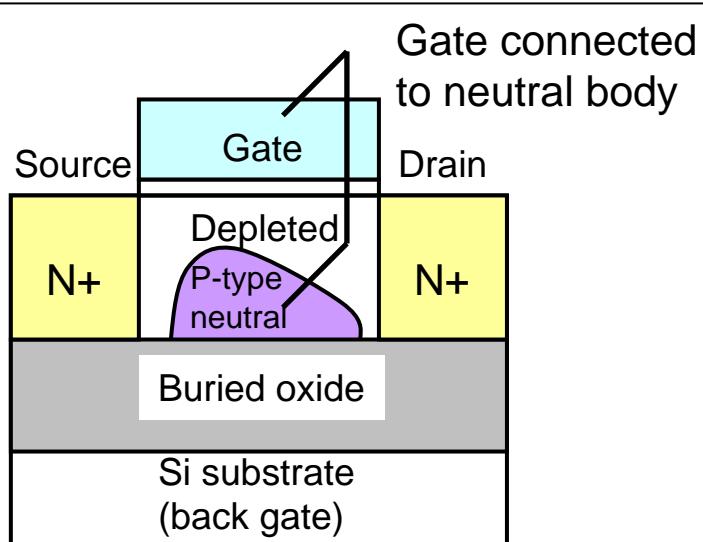
Typical Si thickness: 20-100 nm

Typical BOX thickness: 50-150 nm

FD-SOI CMOS is now in mass production



Types of SOI MOSFETs (II)



Dynamic Threshold SOI MOSFET (DTMOS)

Typical Si thickness: 100-340 nm

Typical BOX thickness: 100-400 nm

DTMOS is especially suited for ultra-low voltage operation



Basic MOSFET equations

- Linear region

$$I_D = \mu_n C_{OX} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} n V_{DS}^2 \right]$$

- Saturation region

$$I_{Dsat} = \frac{1}{2n} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_T)^2$$

- Subthreshold swing

$$S = n \frac{kT}{q} \ln 10$$

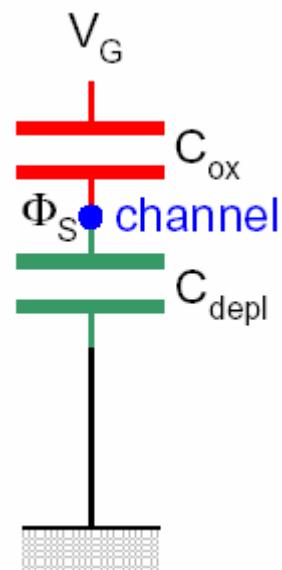
- Reduced transconductance

$$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{OX} W / L}{n I_D}}$$

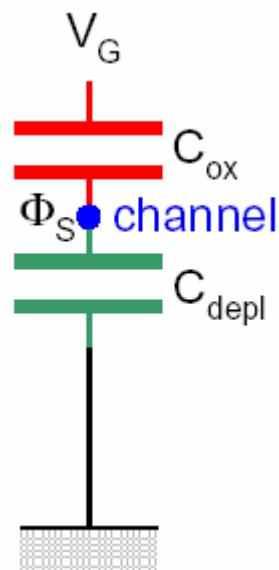
$$n = \left(1 + \frac{C_{dm}}{C_{OX}} \right)$$

- **n affects the current equations**
- **C_{dm} is the depletion capacitance**

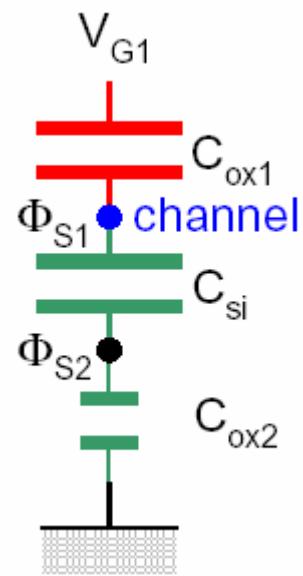
Gate-to-channel coupling and body factor



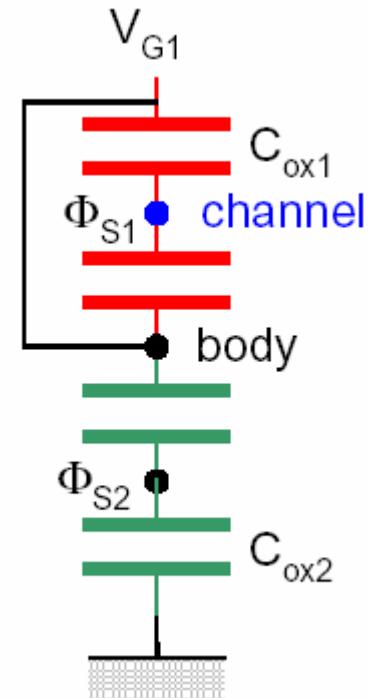
$n=1.3 \dots 1.5$



$n=1.3 \dots 1.5$

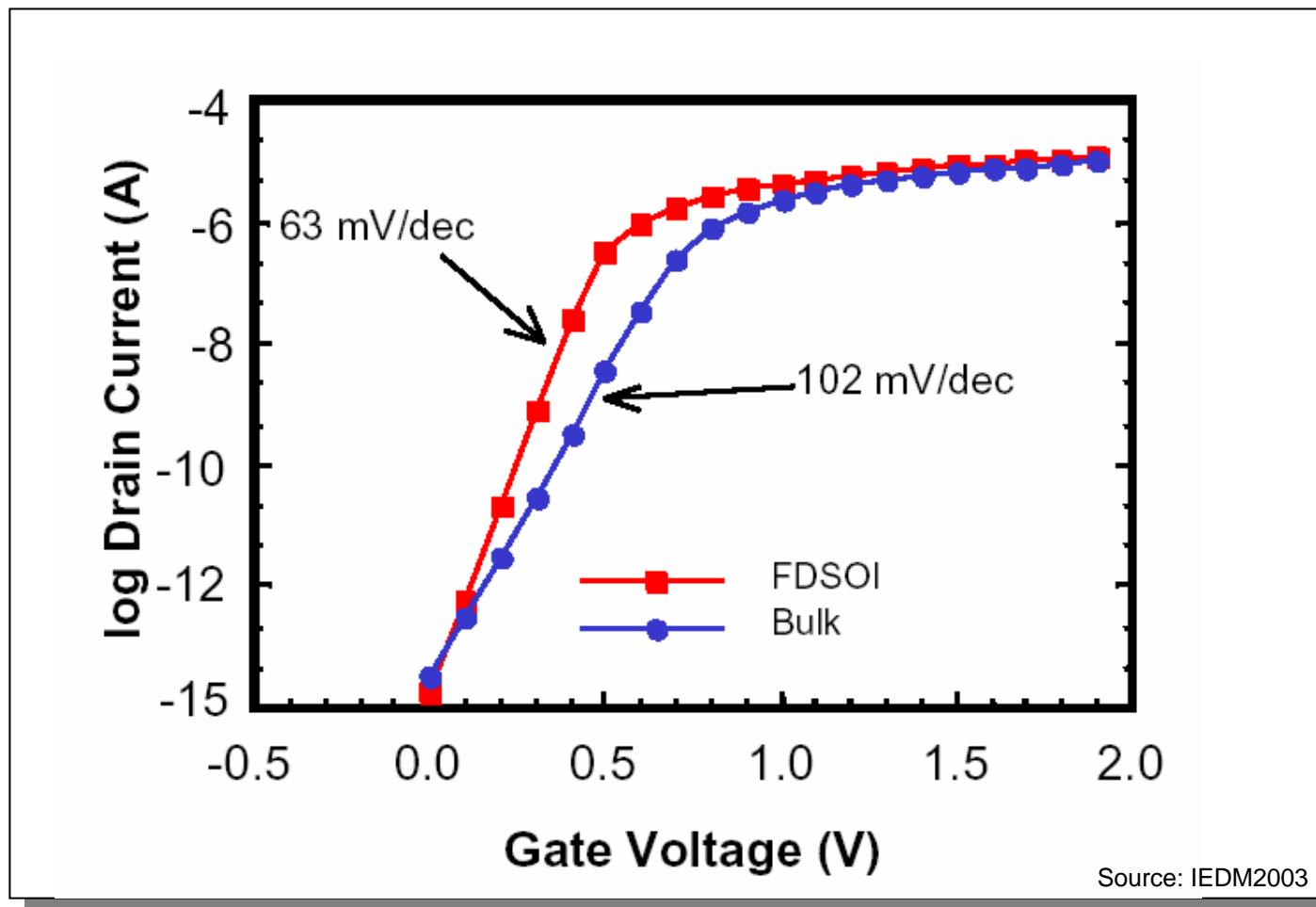


$n < 1.1$

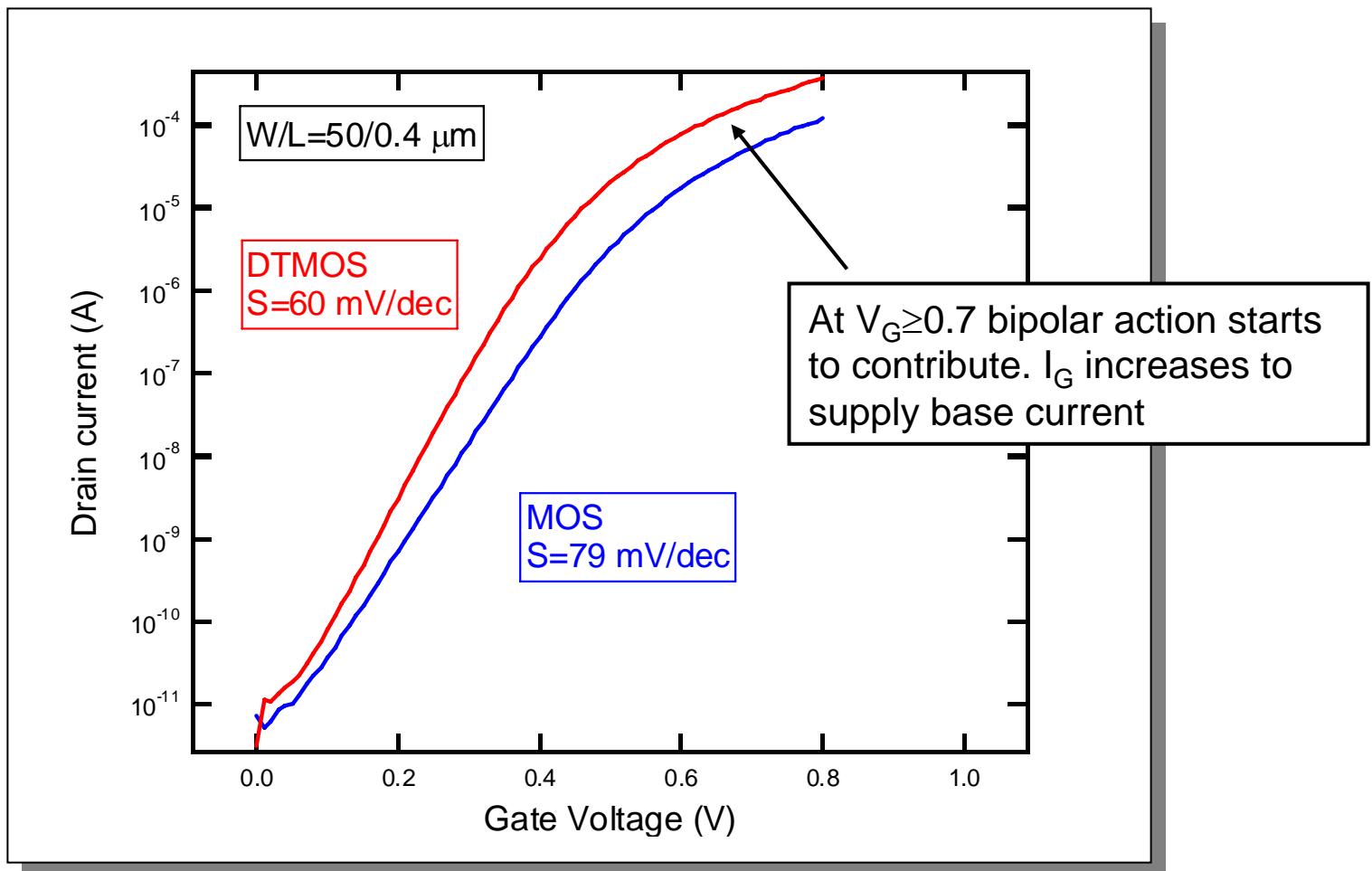


$n=1$

Example: FDSOI with lower S and higher I_{Dsat}



Example: DTMOS with lower S and higher I_{Dsat}





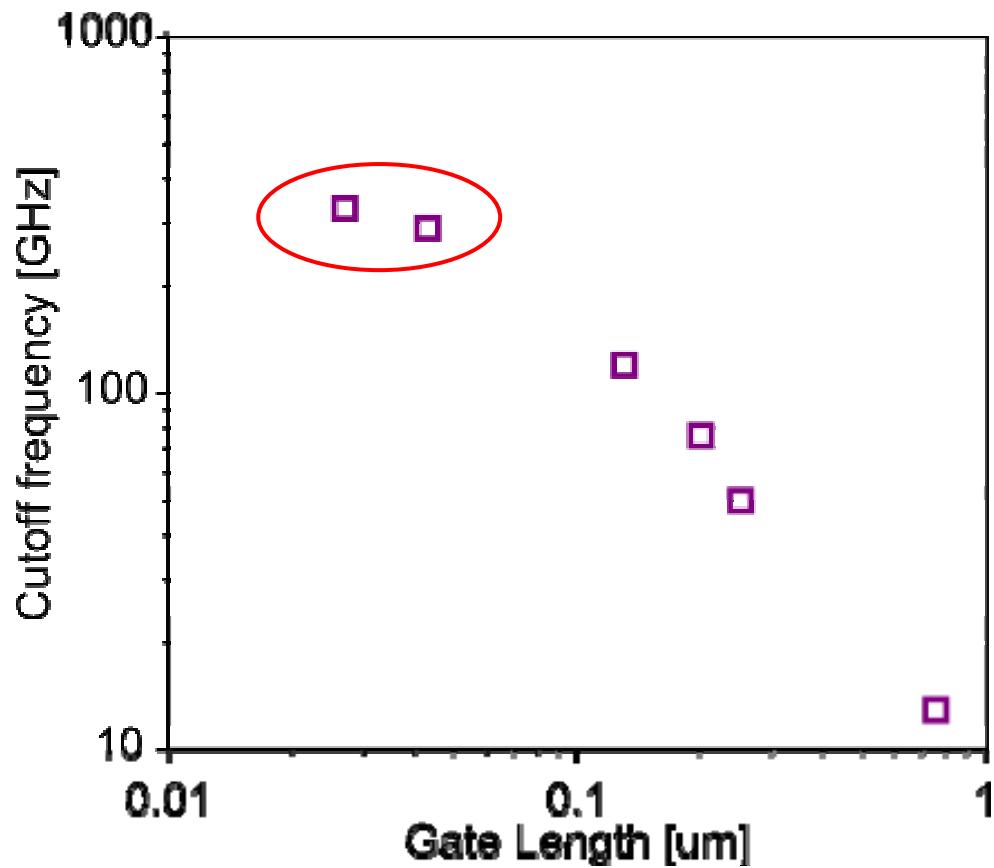
Reported SOI RF-CMOS performance

- **High-resistivity SOI substrates allows for reduced crosstalk, lower losses and higher-Q inductors**

Type	L (μm)	V _{DD} (V)	f _T (GHz)	f _{MAX} (GHz)	NF (dB)/Gain @ 2 GHz
FD	0.75	0.9	12.9	30	- / 11
PD	0.3	2	-	24	0.9 / 14
PD	0.2	2	28.4	46	1 / 15.3
DTMOS	0.25	0.6	16	33	- / -
FD	0.2	1.5	76	40	0.4 / 18
PD	0.25	1.5	50	75	- / -
PD	0.07	1.2	114	135	- / -
PD	0.07	1.2	141	98	0.5 / -
DTMOS	0.08	-	140	60	- / -
FD	0.25	1	42	70	0.8 @ 6 GHz / -
FD	0.25	1.5	30	42	0.45 / -
PD	0.13	1.2	120	150	0.8/16 @ 6 GHz

SOI state-of-the-art

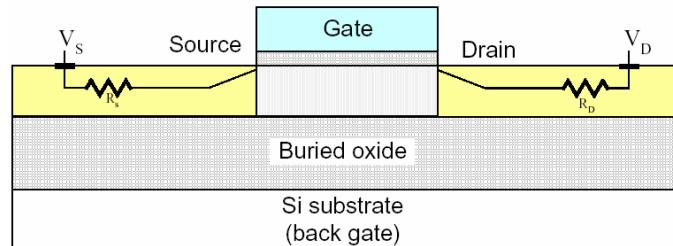
- **Lately, very high cut-off frequencies were demonstrated for SOI, with f_T of 330 GHz and f_{max} of 450 GHz [IBM, IEDM05]**
- **Lg=27 nm (65nm node)**





SOI issues

- FDSOI is sensitive for thickness uniformity, since thickness affects the threshold voltage
- Source and drain resistance get higher as the films get thinner



- SiO_2 is a poor thermal conductor, which may cause device self-heating
- Analog performance affected due to frequency dependent output conductance and transconductance
- However, SOI enables other MOSFET structures...



Outline

- Introduction
- Basic function of silicon MOSFET
- Manufacturing of CMOS
- MOSFET modeling
- SOI-MOSFET
- **Scaling of CMOS**
- Future CMOS
 - Strained-Si, SiGe, and non-classical devices
- Summary



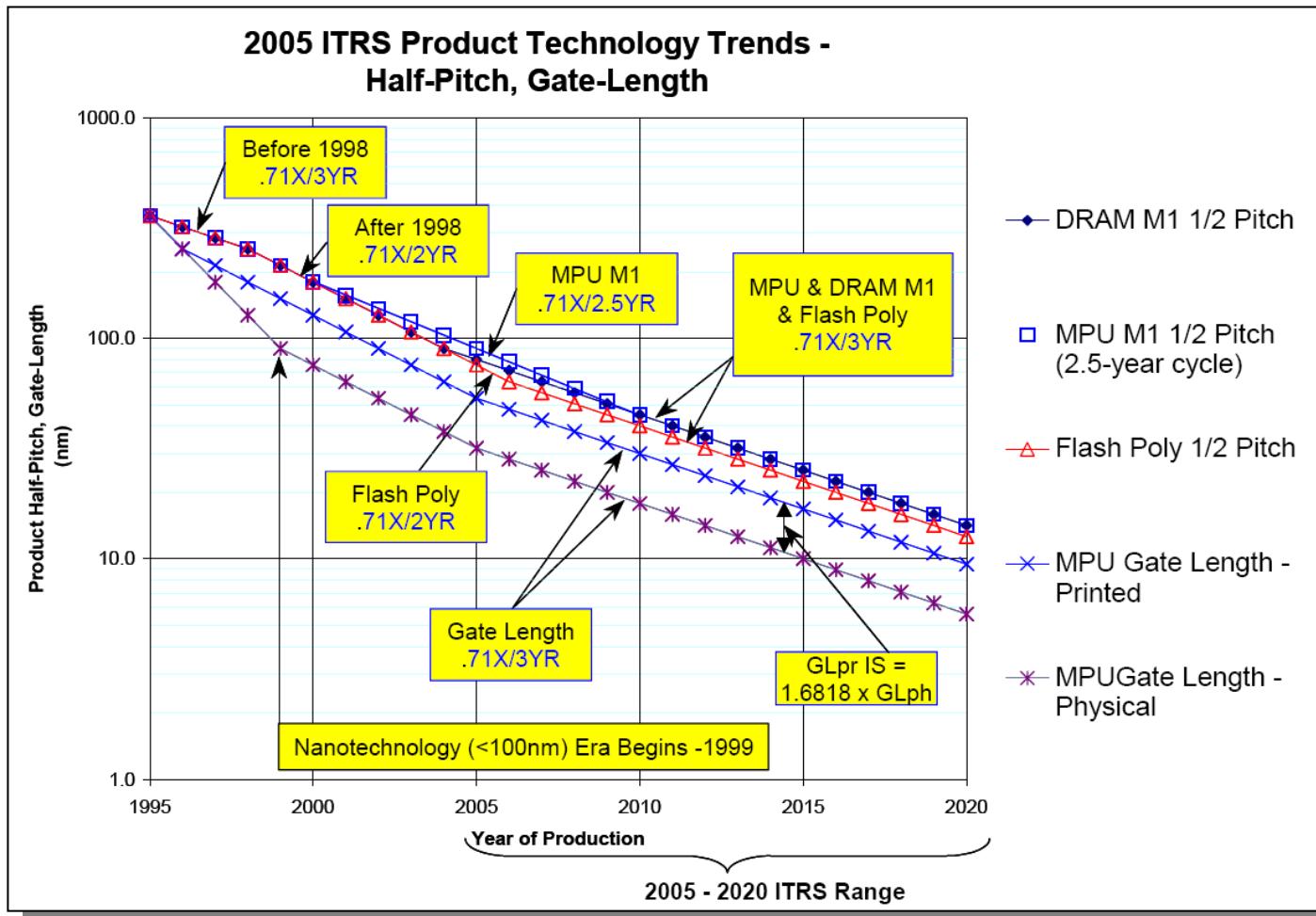


Scaling of CMOS

- Already in 1965 Gordon Moore predicted an exponential growth of the semiconductor industry driven by market expectations – and it is still going on
- Dimensions of MOSFETs have continuously been decreased
 - Faster transistors
 - More transistors per chip
 - More chip per wafer
- Technological solutions have been invented
 - Self-alignment
 - Silicidation
 - etc.
- Amazing development of manufacturing equipment
- ITRS (International Roadmap for Semiconductors) describes the necessary and expected development

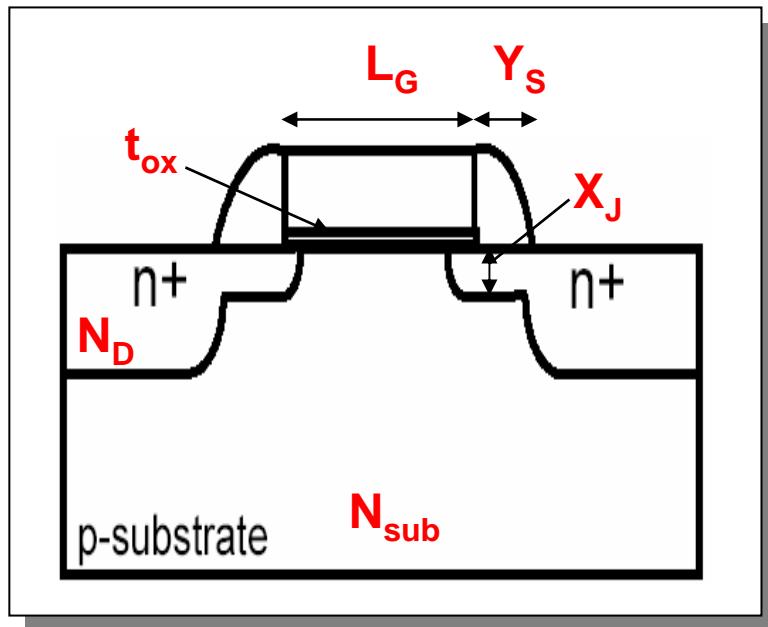


Example: scaling trend of gate length Lg





MOSFET scaling



In general the supply voltage V_{DD} has to be scaled to maintain the electrical field strength – but that is not always the case

Parameters to be scaled:

L_G – gate length ↓

- High I_{dsat} , high speed

N_{sub} – channel doping ↑

- Reduce short channel effects (SCE)

X_J – LDD junction depth ↓

- Reduce SCE

t_{ox} – gate oxide thickness ↓

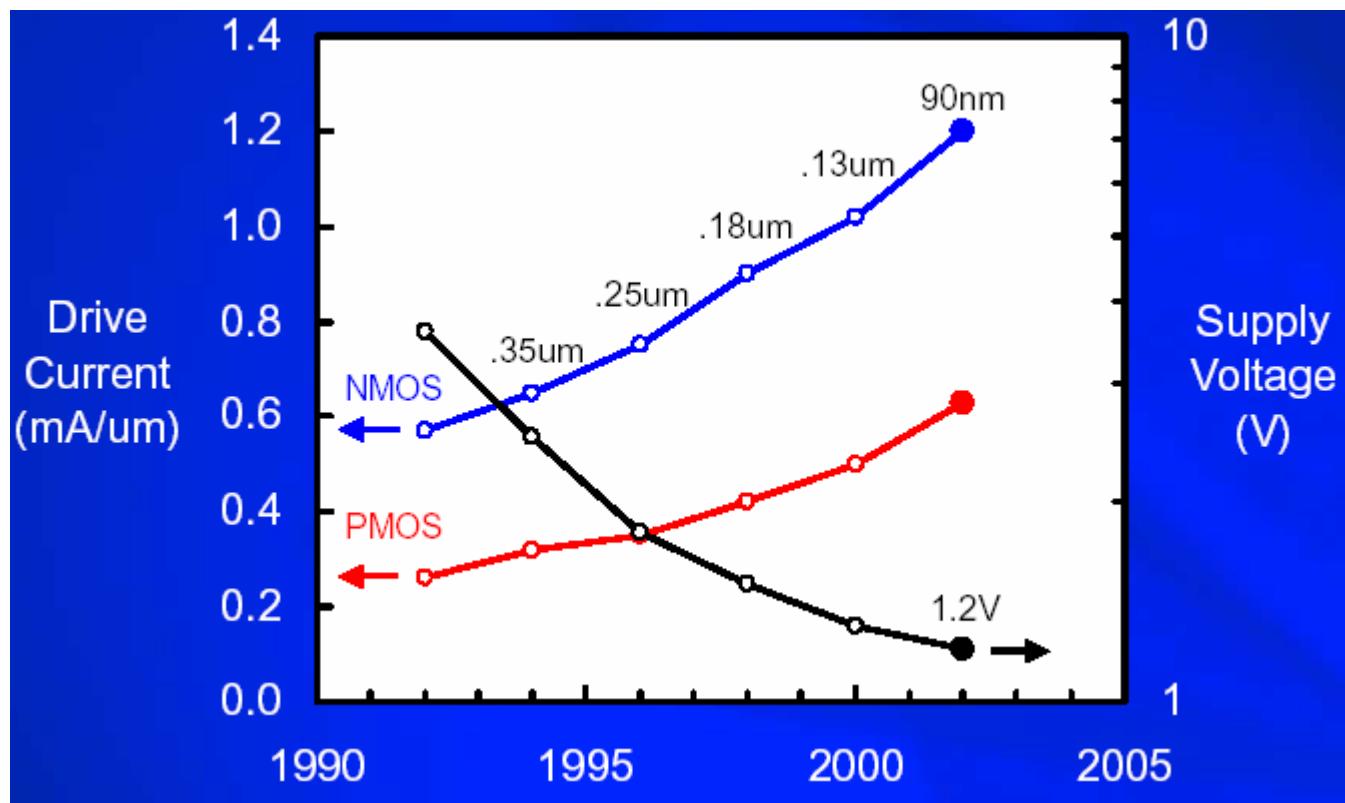
- Increase C_{OX} – channel control

Y_s – spacer width ↓

- Reduce LDD resistance

N_D – S/D doping (or resistance) ↑

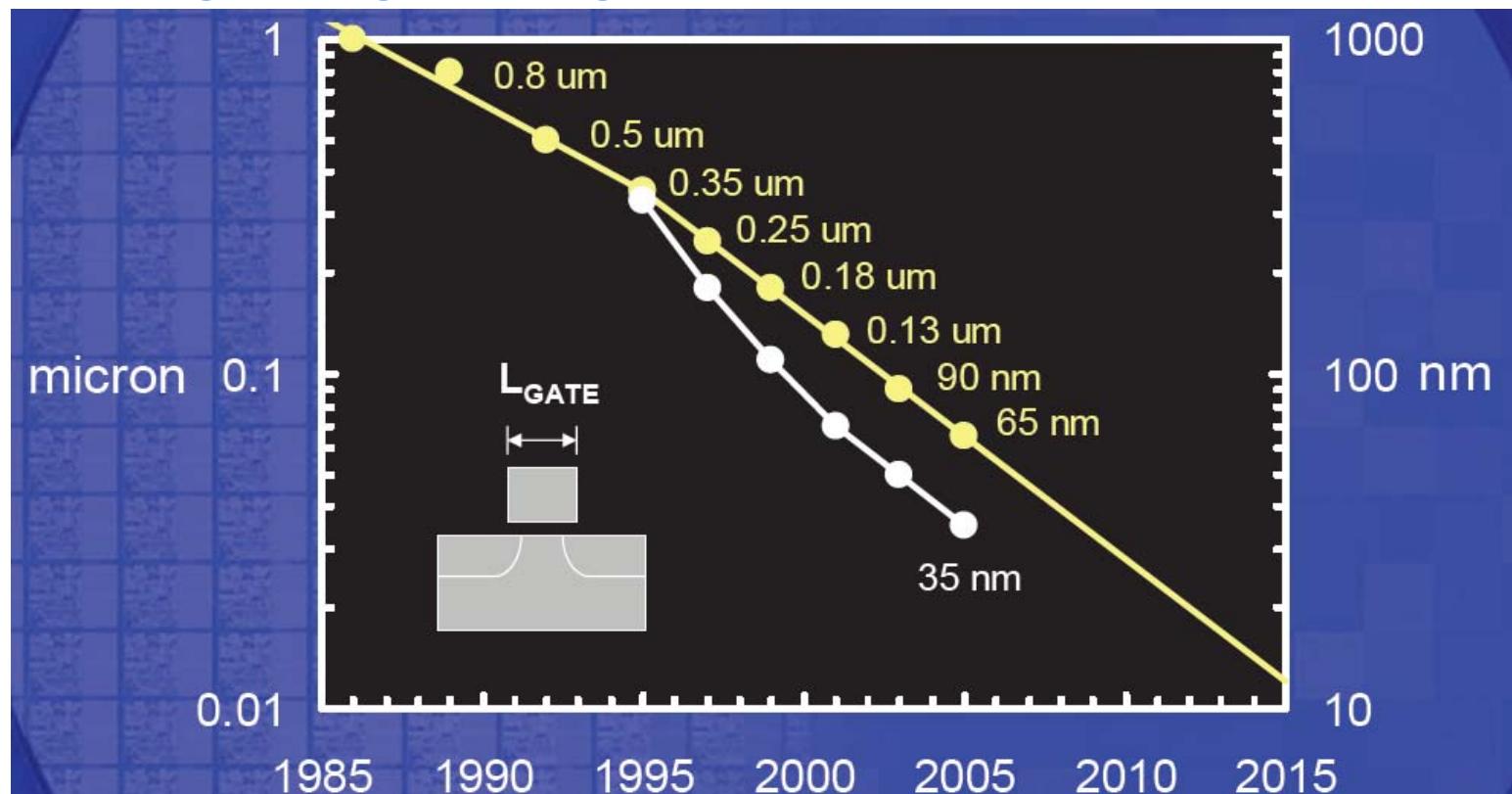
Result of scaling



Source: Intel

Aggressive scaling of L_G

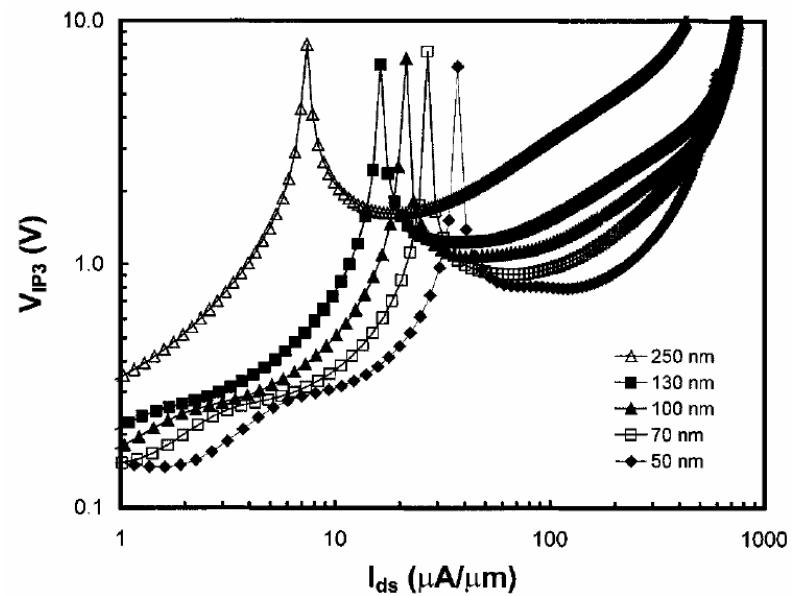
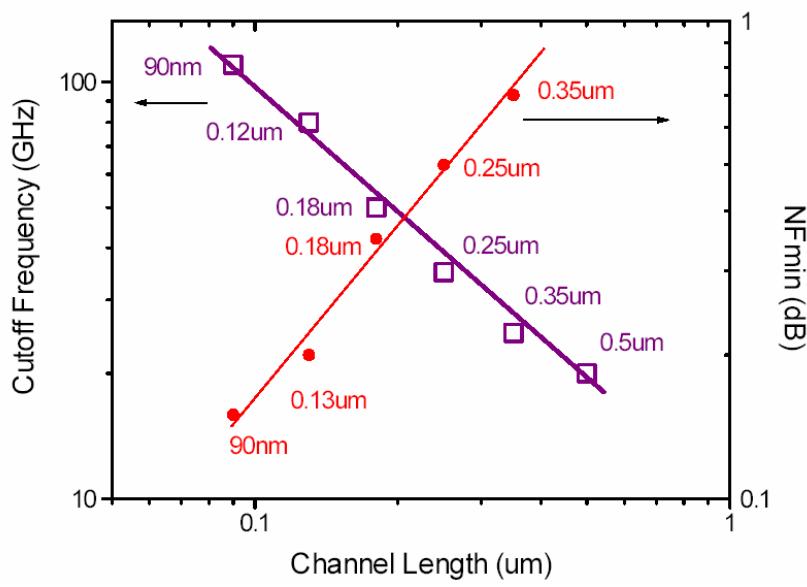
Faster gate length scaling to maintain transistor performance



Source: Intel

RF performance vs. scaling

- In general RF-CMOS performance increases strongly with transistor scaling
- Linearity performance may be a problem – alternative scaling methodology can reduce the problem





Outline

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Future CMOS

- **The current version of the ITRS predicts further scaling of the silicon technologies for at least another 15 years – but enormous efforts and new inventions are needed**
- **Scaling of the traditional planar MOSFET will be driven to its extreme – but it will involve new materials (very soon) and different process technologies**
- **Eventually other non-classical MOSFET (non-planar) structures will enter the production – but this requires even more research and development**
- **The SOI MOSFET is the first step towards alternative MOSFET structures**



Table 40a High-Performance Logic Technology Requirements—Near-term

Grey cells delineate one of two time periods: either before initial production ramp has started for ultra-thin body fully depleted (UTB FD) SOI or double-gate (DG) MOSFETs, or beyond when planar bulk or UTB FD MOSFETs have reached the limits of practical scaling (see the text and the table notes for further discussion)

Year of Production	2005	2006	2007	2008	2009	2010	2011	2012	2013
DRAM $\frac{1}{2}$ Pitch (nm) (contacted)	80	70	65	57	50	45	40	36	32
MPU/ASIC Metal 1 (M1) $\frac{1}{2}$ Pitch (nm)(contacted)	90	78	68	59	52	45	40	36	32
MPU Physical Gate Length (nm)	32	28	25	22	20	18	16	14	13
L_g : Physical L_{gate} for High Performance logic (nm) [1]	32	28	25	22	20	18	16	14	13
<i>EOT: Equivalent Oxide Thickness [2]</i>									
Extended planar bulk (Å)	12	11	11	9	7.5	6.5	5	5	
UTB FD (Å)				9	8	7	6	5	5
DG (Å)							8	7	6
<i>Gate Poly Depletion and Inversion-Layer Thickness [3]</i>									
Extended Planar Bulk (Å)	7.3	7.4	7.4	2.9	2.8	2.7	2.5	2.5	
UTB FD (Å)				4	4	4	4	4	4
DG (Å)							4	4	4
<i>EOT_{elec}: Electrical Equivalent Oxide Thickness in inversion [4]</i>									
Extended Planar Bulk (Å)	19.3	18.4	18.4	11.9	10.3	9.2	7.5	7.5	
UTB FD (Å)				13	12	11	10	9	9
DG (Å)							12	11	10
<i>J_{g,limit}: Maximum gate leakage current density [5]</i>									
Extended Planar Bulk (A/cm ²)	1.88E+02	5.36E+02	8.00E+02	9.09E+02	1.10E+03	1.56E+03	2.00E+03	2.43E+03	
FDSOI (A/cm ²)				7.73E+02	9.50E+02	1.22E+03	1.38E+03	2.07E+03	2.23E+03
DG (A/cm ²)							6.25E+02	7.86E+02	8.46E+02
<i>V_{dd}: Power Supply Voltage (V) [6]</i>									
	1.1	1.1	1.1	1	1	1	1	0.9	0.9
<i>V_{t,sat}: Saturation Threshold Voltage [7]</i>									
Extended Planar Bulk (mV)	195	168	165	160	159	151	146	148	
UTB FD (mV)				169	168	167	170	166	167
DG (mV)							181	184	185

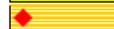
Manufacturable solutions exist, and are being optimized



Manufacturable solutions are known



Interim solutions are known



Manufacturable solutions are NOT known



Source: ITRS 2005



Major challenges: Gate oxide

- Problem: Direct gate oxide tunneling ($t_{ox} < 2 \text{ nm}$) – increased standby power
- Solution: Replace SiO_2 with thicker high-k dielectric
- Challenge: Find high-k that is stable with both silicon and gate material, and has suitable electrical behavior
- Present status: HfO_2 -based with controlled top and bottom interfacial layers, HfSiO , HfSiON etc.
- ALD (atomic layer deposition) is the most promising method

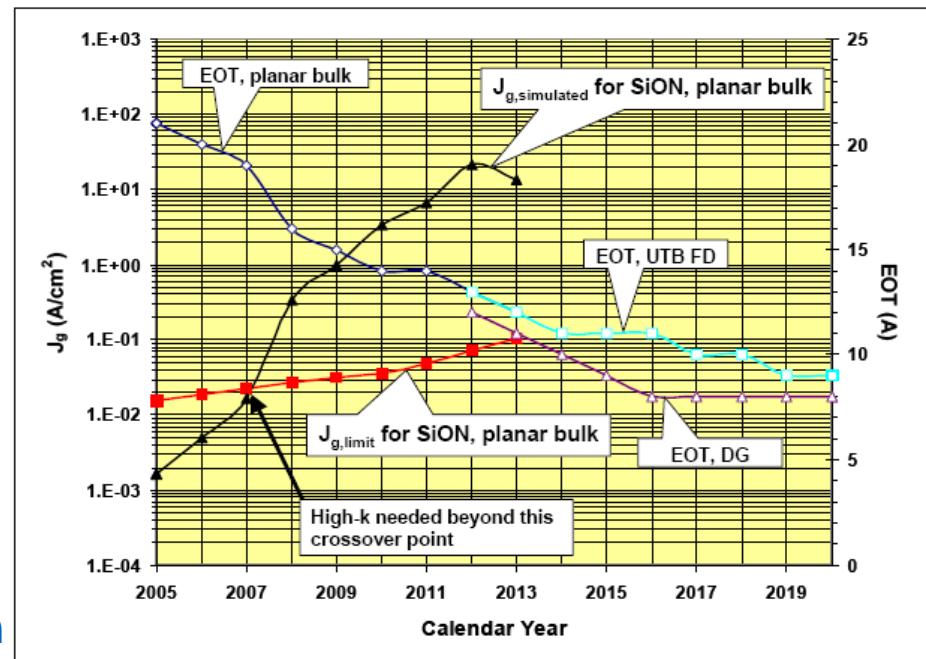
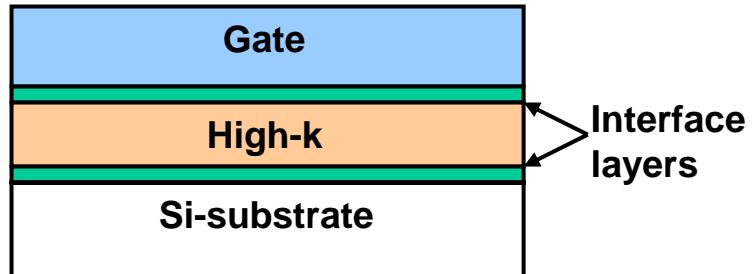


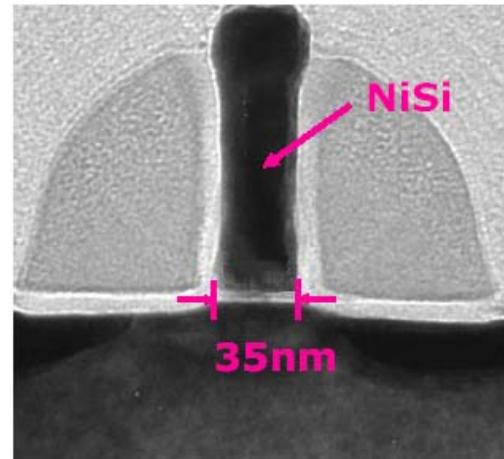
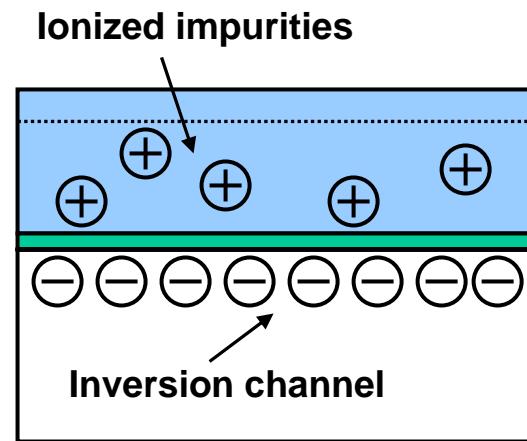
Figure 36 $J_{g,\text{limit}}$ versus $J_{g,\text{simulated}}$ for Low Standby Power





Major challenges: Gate electrode

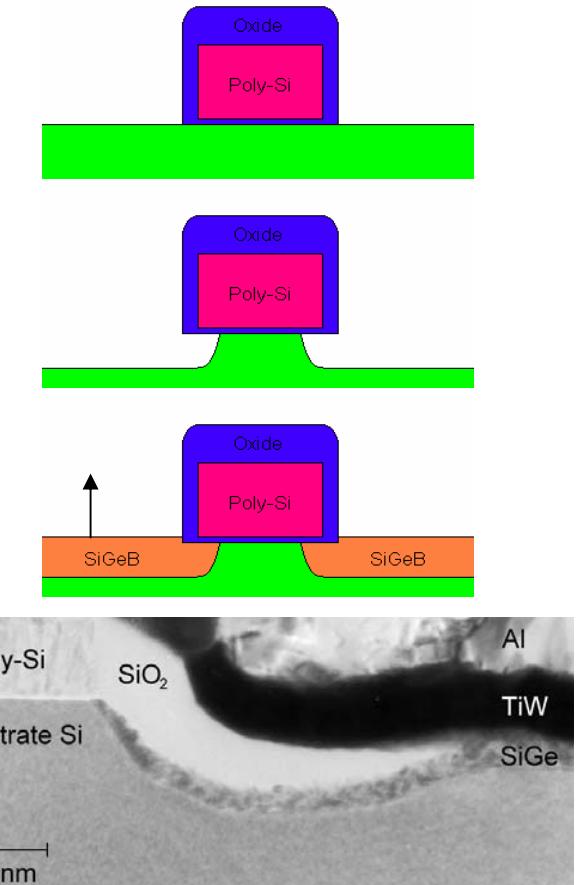
- Problem: Gate poly depletion – increased electrical EOT, lower C_{ox} , lower I_{Dsat}
- Solution: Replace polysilicon with metal gate
- Challenge: Find metal(s) stable with both silicon and gate dielectric, and suitable electrical behavior (low resistivity and complementary work-function)
- Present status: Different processing schemes have been presented. Fully Ni-silicided poly seems to be a possible solution for SiO_2 (and perhaps SiON).





Major challenges: S/D resistance

- **Problem:** Ultra shallow LDD and S/D junctions – increased series resistance
- **Solutions:** Low energy implantation, plasma doping, elevated S/D, selective Si (or SiGe) epitaxy with in-situ doping, spike or laser annealing
- **Challenges:** Find solutions which allows for ultra-shallow junctions while not increasing the process complexity (cost)
- **Present status:** Selective epitaxy is accepted in production

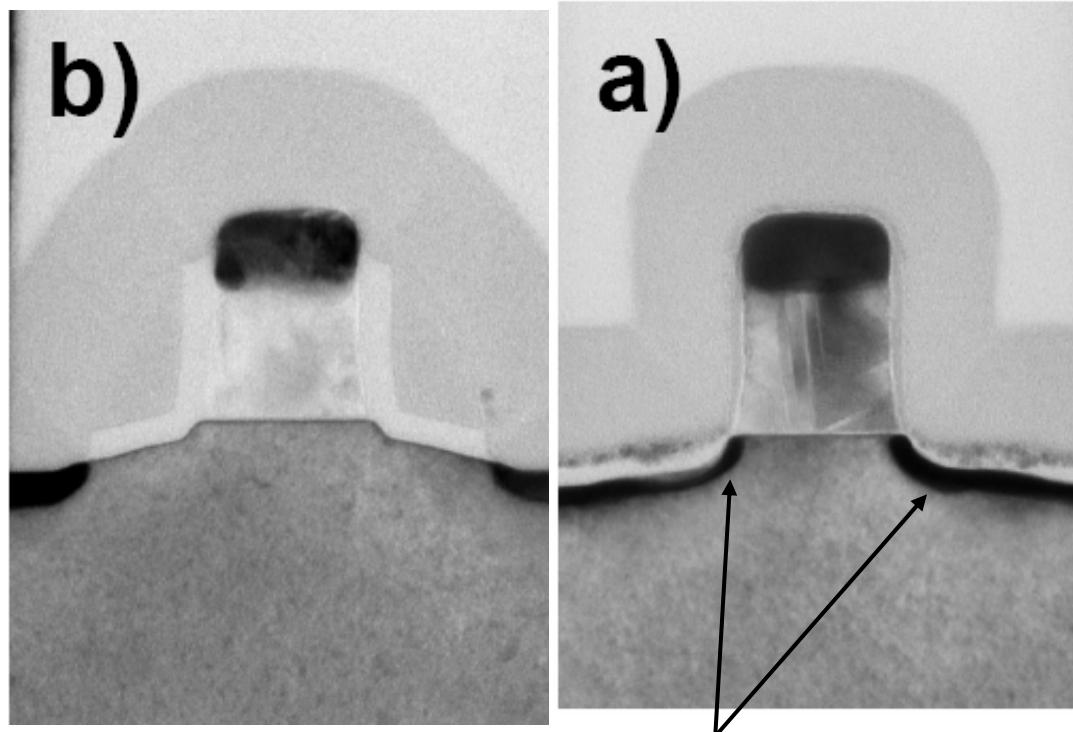


Source: KTH, Sweden



Major challenges: S/D resistance II

- Alternative solution: Use Schottky barrier metals instead of dopings
- Challenges: Find solutions which allows for controlled silicidation
- Present status: NiSi is under investigation my many groups and companies

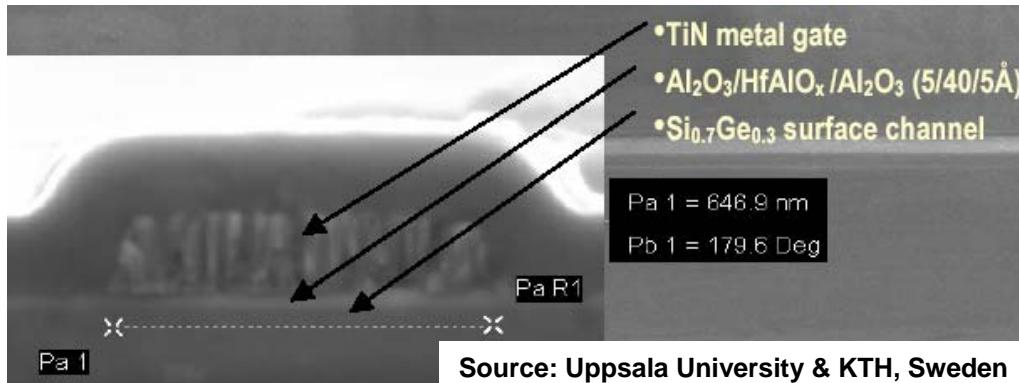


NiSi



Major challenges: Channel engineering

- **Problem:** High channel doping, high electric field (and high-k) – lower carrier mobility, lower I_{Dsat}
- **Solutions:** Un-doped channel, strained-SiGe (PMOS), strained-Si (PMOS and NMOS)
- **Challenges:** Find solutions which enhance both electron and hole mobility, while not increase the process complexity (cost)
- **Present status:** Intel already has strained-Si in production (90 nm process node and soon 65 nm)



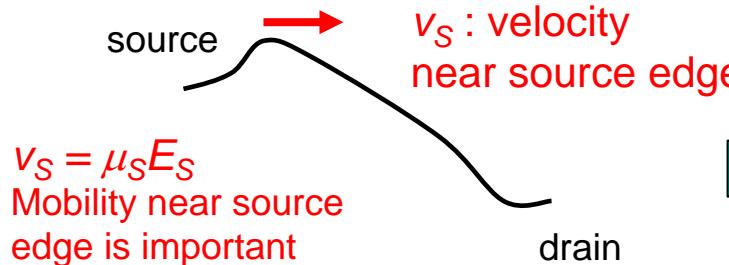
TiN metal gate, high-k and strained $\text{Si}_{1-x}\text{Ge}_x$ demonstrating increased hole mobility for PMOS



Strained Silicon for high mobility

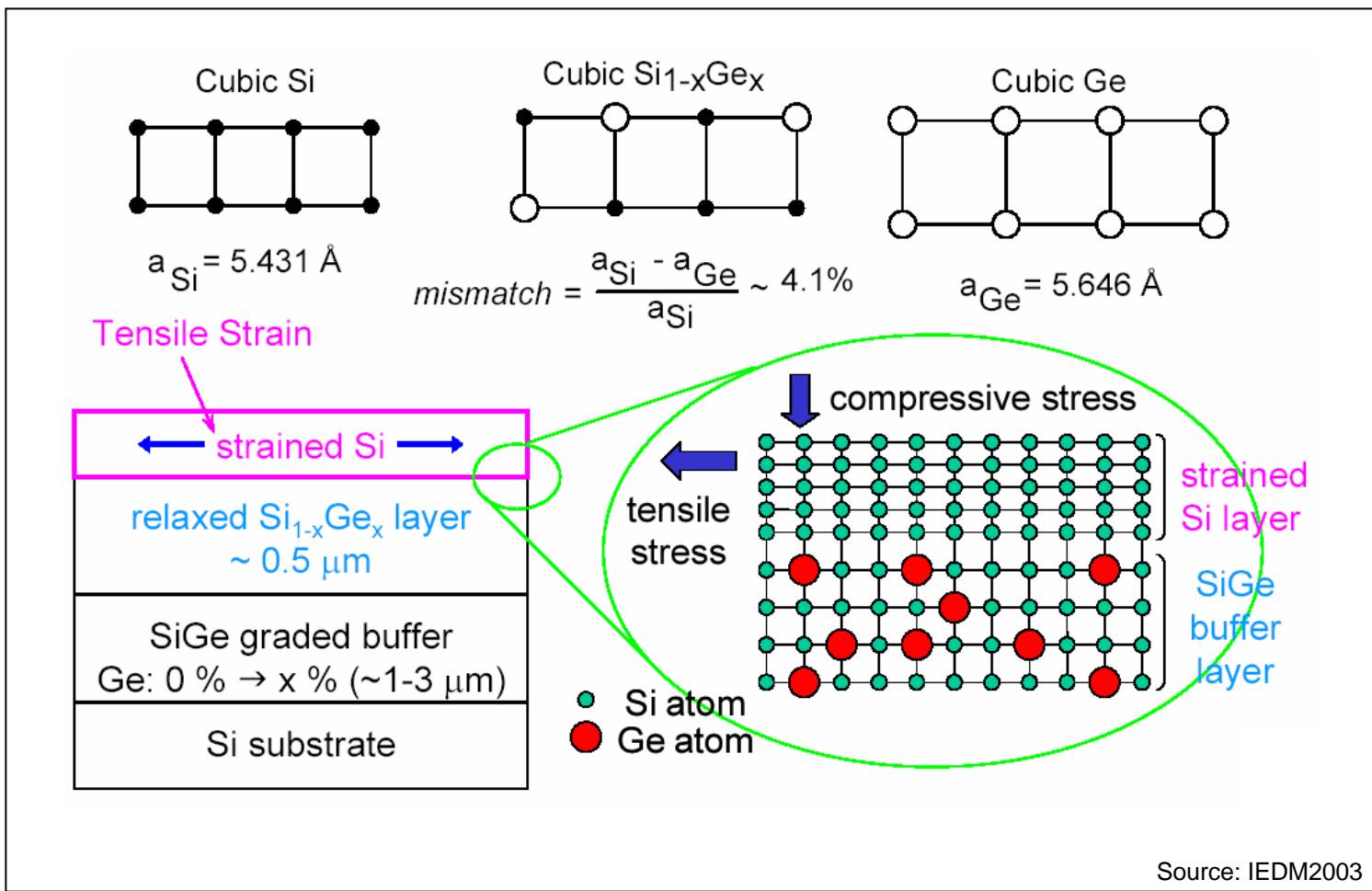
- **NMOS (high electron mobility)**
 - Strained Si on relaxed $\text{Si}_{1-x}\text{Ge}_x$
 - Pure Ge channel? (problem with MOS interface)
- **PMOS (high hole mobility)**
 - Strained Si on relaxed $\text{Si}_{1-x}\text{Ge}_x$
 - Strained $\text{Si}_{1-x}\text{Ge}_x$ on Si substrate
 - Pure Ge channel?
- **But why is mobility important for submicron MOSFETs?**

$$I_{Dsat} = C_{OX} W v_{sat} (V_{GS} - V_T)$$



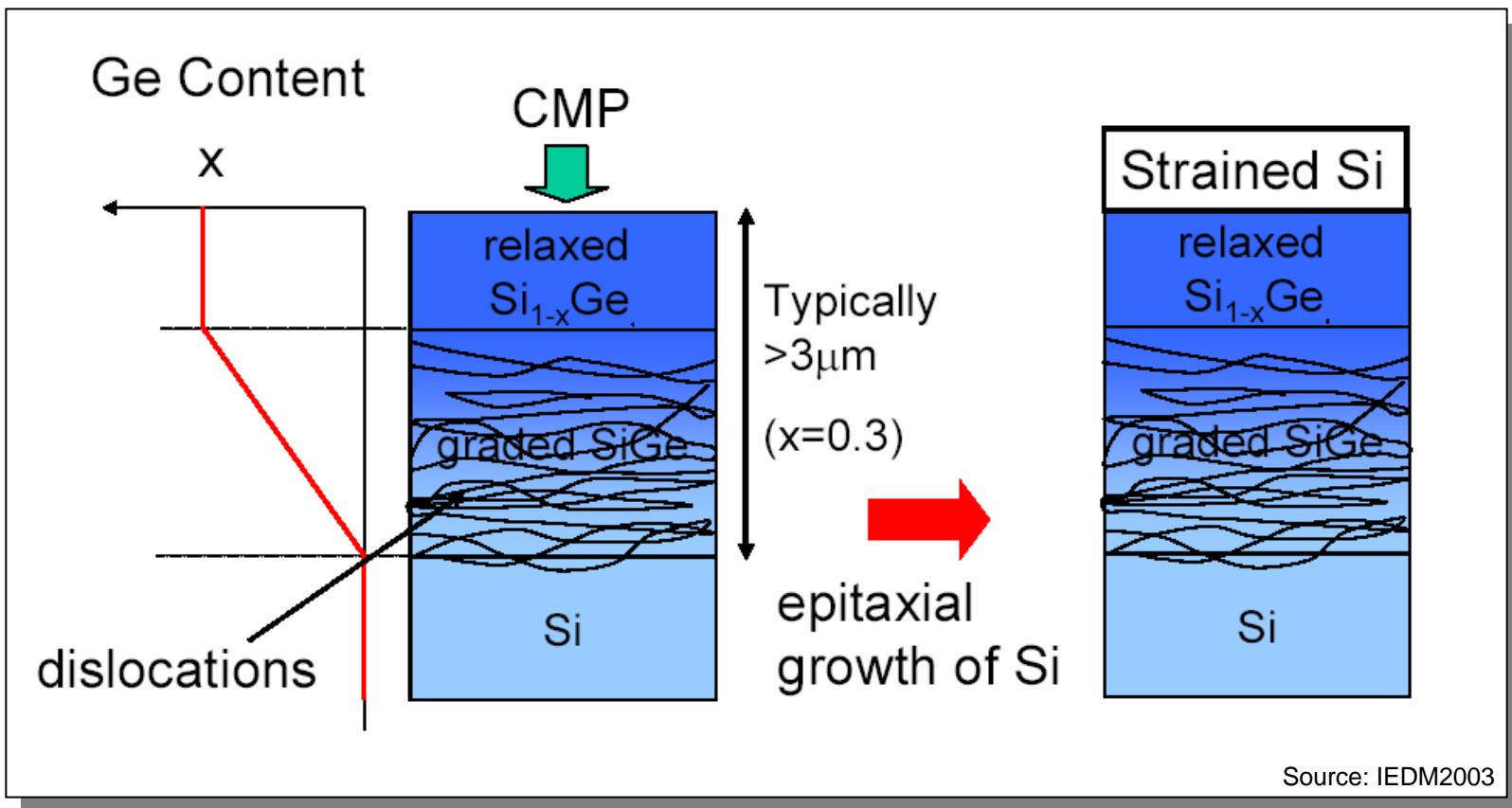
Mobility is still important for sub-100 nm MOSFET

Structure of strained silicon

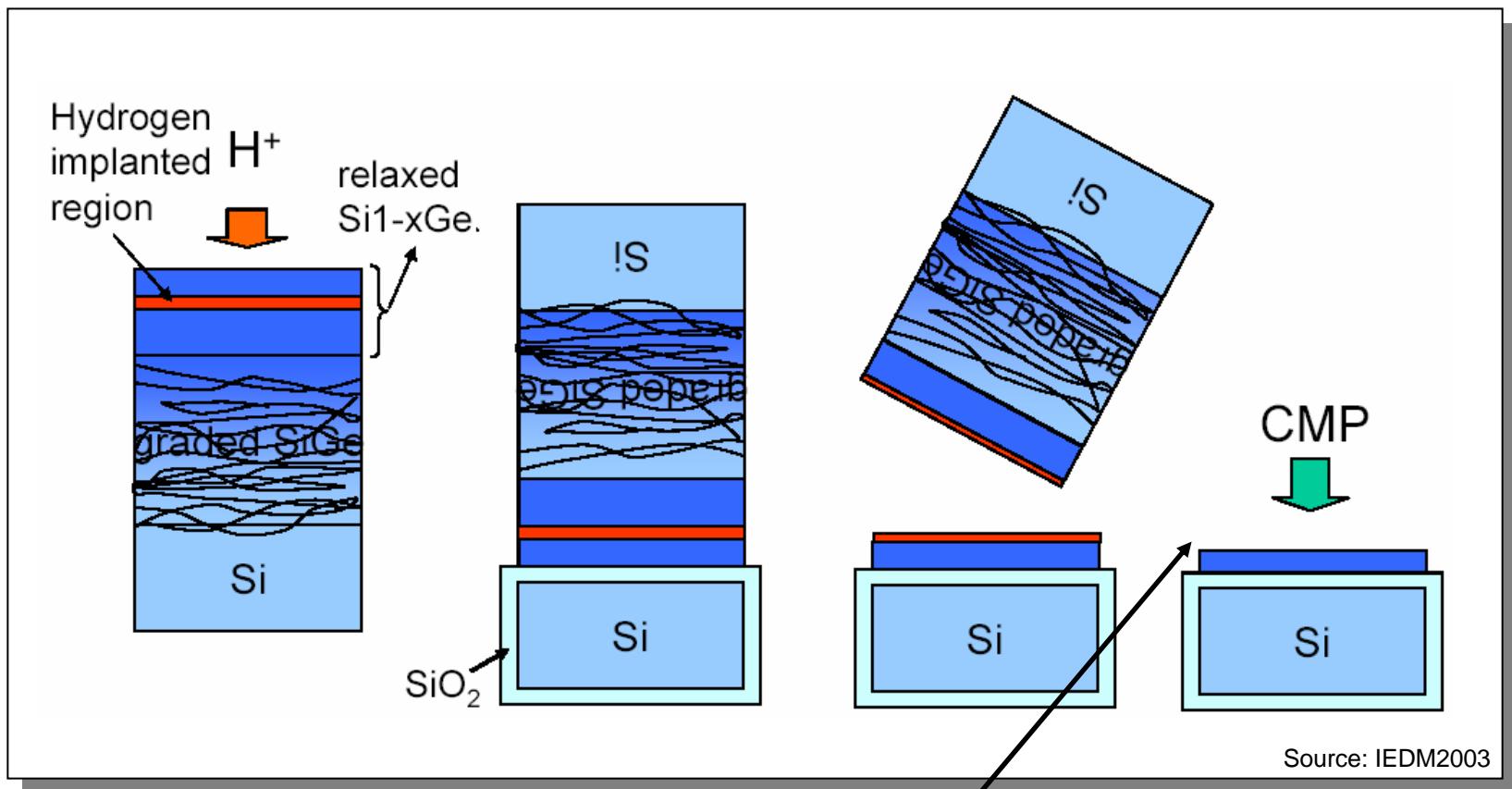




Preparing bulk Strained-Si substrates



Preparing Strained-Si-on-Insulator (SSOI)

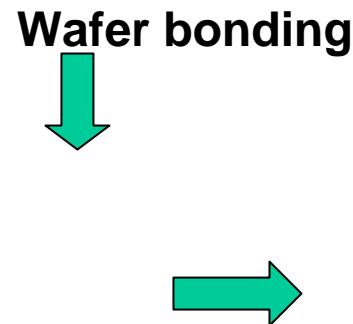


Followed by silicon-epi

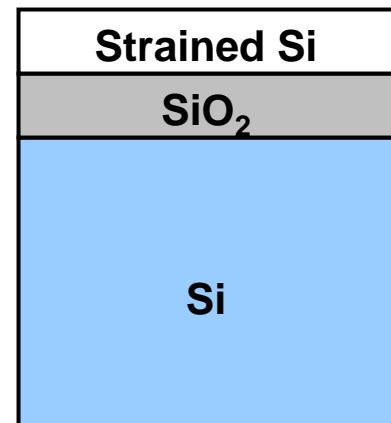
Source: IEDM2003



Preparing SSOI without relaxed SiGe



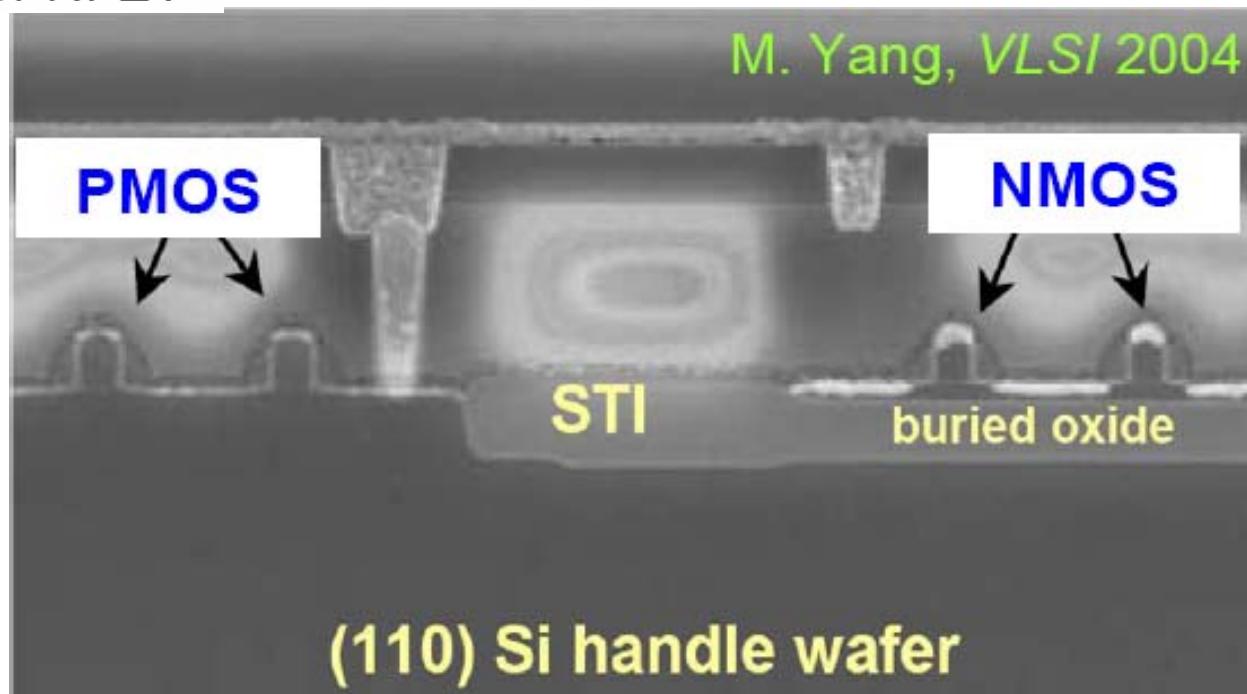
1. Silicon grinded and etched
2. Selective etch of SiGe
3. CMP of Strained-Si





IBM SOI for increased mobility

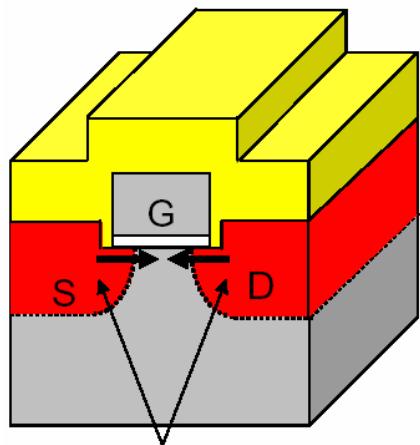
- Hybrid Orientation
 - 110 for PFET
 - 100 for NFET





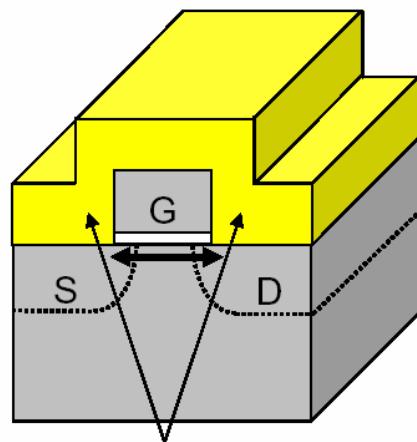
Alternative methods for Strained-Si

Intel's 90nm Technology



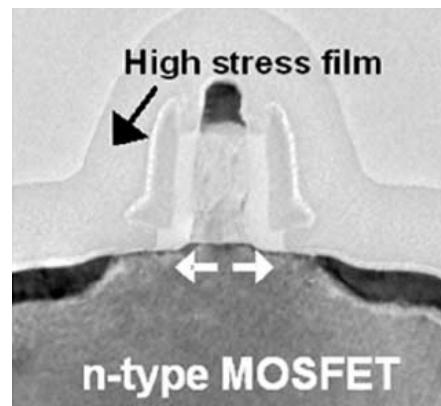
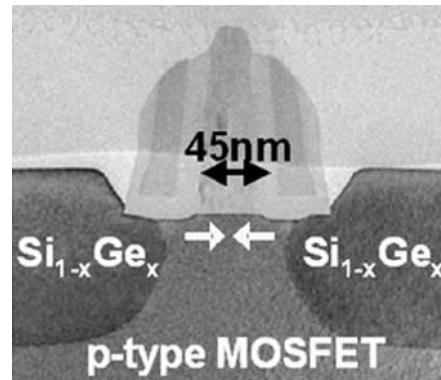
Selective SiGe S-D

Uniaxial
Compressive Strain
for PMOS



Tensile Si₃N₄ Cap

Uniaxial
Tensile Strain
for NMOS

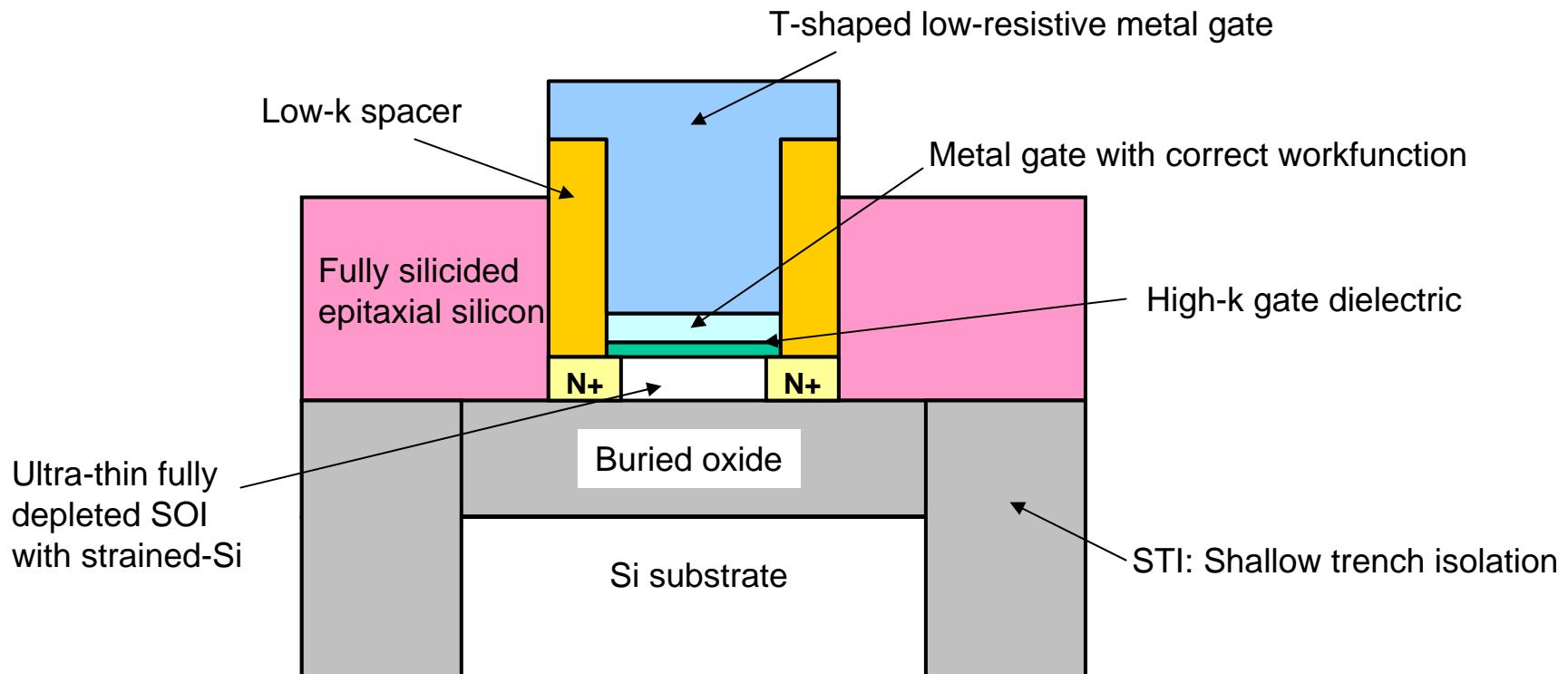




Issues with strained silicon

- No clear evidence for performance enhancement for $L_G < 30 \text{ nm}$
- Immunity for strain relaxation, uniformity of strain
- Influence from other stress sources – STI, silicidation
- Hole mobility enhancement for PMOS lower at high electrical fields
- Low heat conductivity of SiGe – self-heating problems?
- Increased junction leakage due to reduced bandgap
- Reliability and yield – cost!
- Status: Local strain engineering better than global strain!

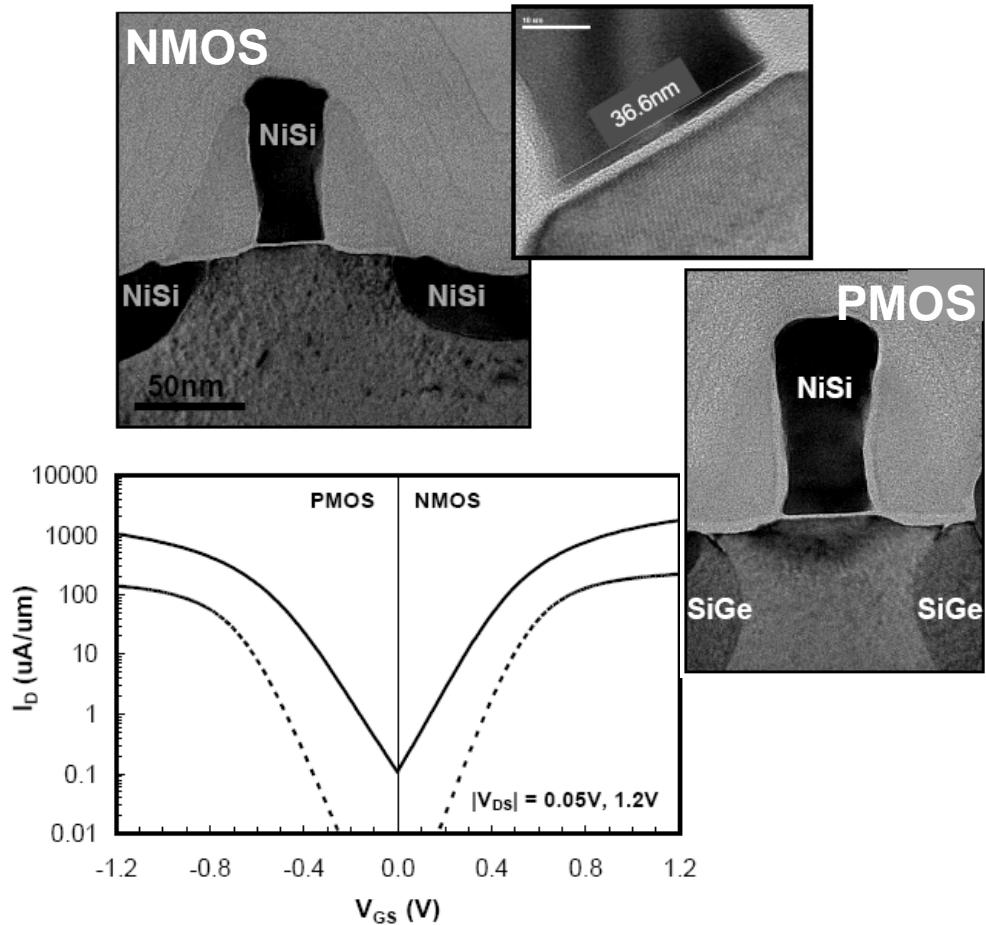
The ultimate planar MOSFET?





State-of-the-art CMOS in production: Intel 65 nm node

- 35 nm gate length
- 1.2 nm SiON
- NiSi FUSI gate
- $V_{dd}=1.2$ V
- Local strain engineering
- Record high I_{dsat}
 - 1.75 mA/ μ m (NMOS)
 - 1.06 mA/ μ m (PMOS)
- Best reported I_{dsat}/I_{off}

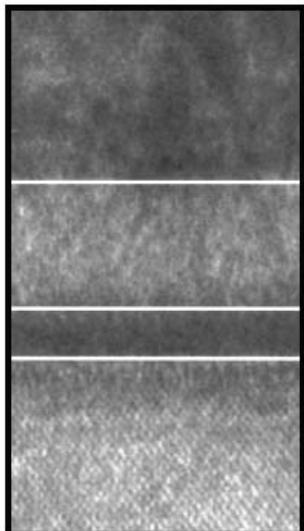


Source: IEDM 2005



State-of-the-art CMOS today: Intel 45 nm node

- Less than 28 nm gate length?
- High-k gate dielectric
- Secret metal gate
- Local strain engineering?
- Best reported I_{dsat}/I_{off} ?



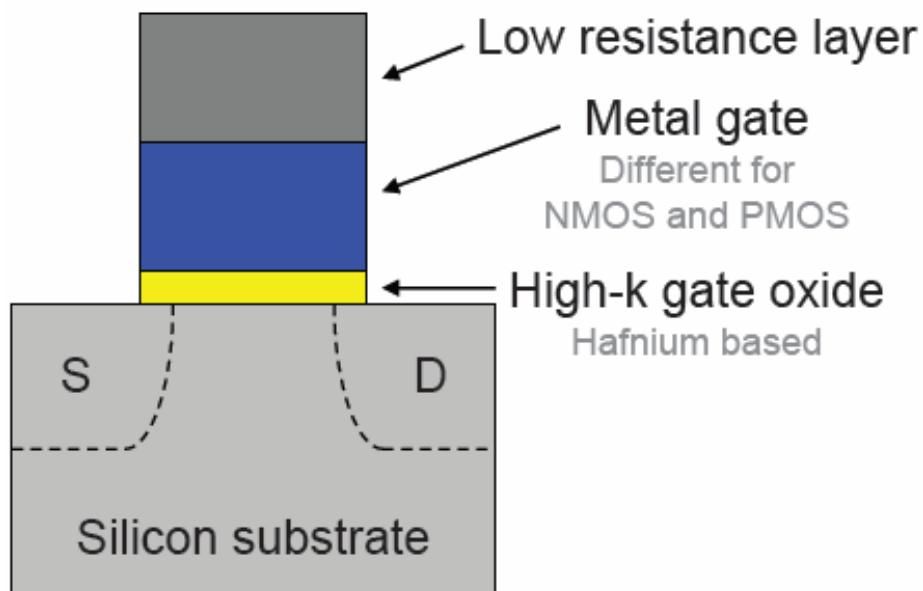
Low Resistance Layer

Work Function Metal
Different for NMOS and PMOS

High-k Dielectric
Hafnium based

Silicon Substrate

HK+MG
Transistor



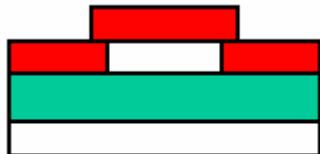
Non-classical MOSFET structures

- The conventional planar bulk single-gate MOSFET will be scaled and new materials will be used
- The absolute limit for L_G is unclear, but it seems to be realistic to produce sub-20 nm MOSFETs
- Single gate SOI-MOSFETs will probably follow the same scaling trend
- FD SOI may extend the scaling one or two generations
- Further scaling will probably result in un-controlled short-channel effect
- It is therefore necessary to introduce other MOSFET structure to control the SCE and enable further down-scaling

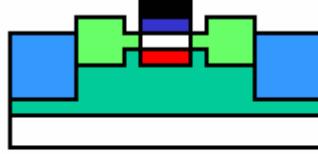


ITRS emerging devices

- The ITRS mentions possible non-classical MOSFET devices, which may emerge in the future
- Of highest priority is to control/suppress the SCE
- Multi-gate structures may be immune to SCE and also provide additional advantages, such as higher I_{Dsat}



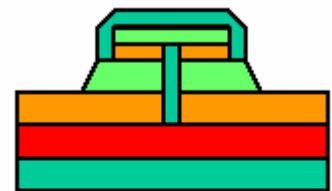
Ultra-thin
body SOI



Double-gate
transistor



FinFET



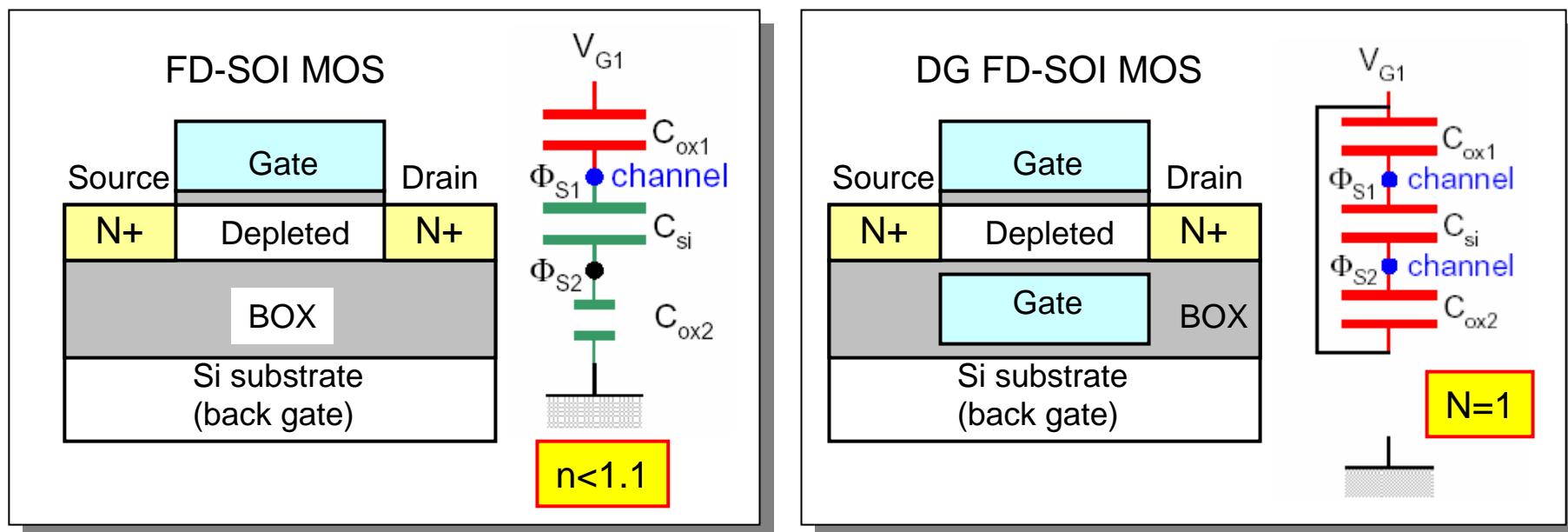
Vertical
transistor



DG SOI MOSFET

Fully depleted DG SOI-MOSFET provides:

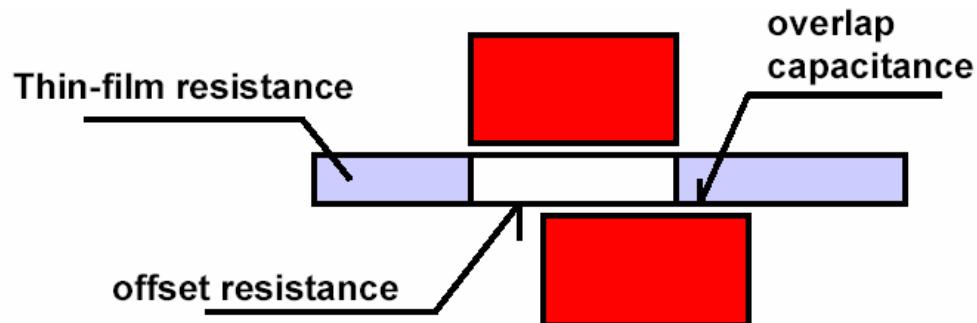
- SCE immunity (drain field does not penetrate to source)
- Higher drive current (two channels/volume inversion)
- Ideal subthreshold swing (no body effect)





Challenges for DG SOI MOSFET

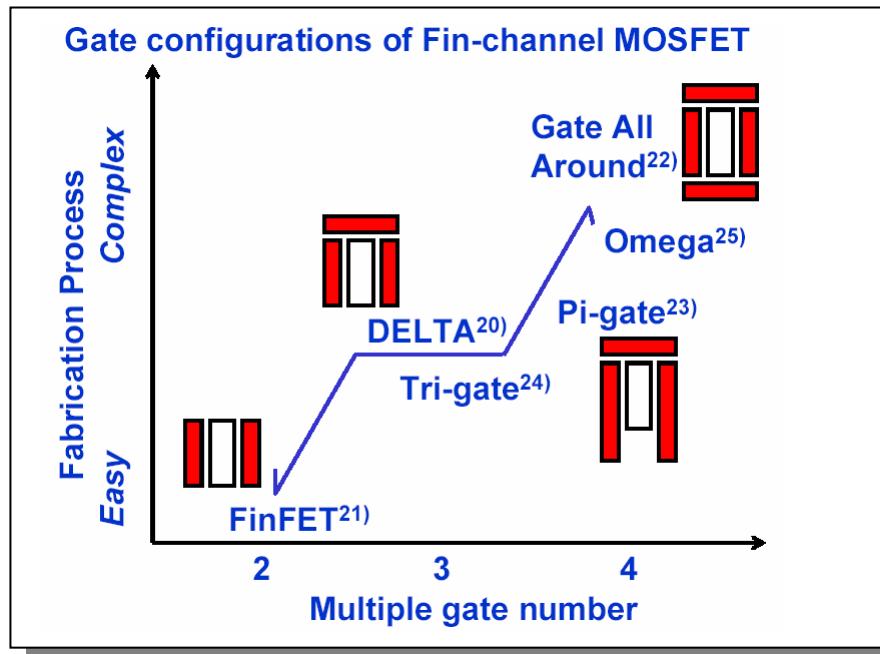
- Find process flow which provide self-alignment of top- and bottom gates
- S/D regions also have to be self-aligned
- Process complexity increases – yield and cost may be affected





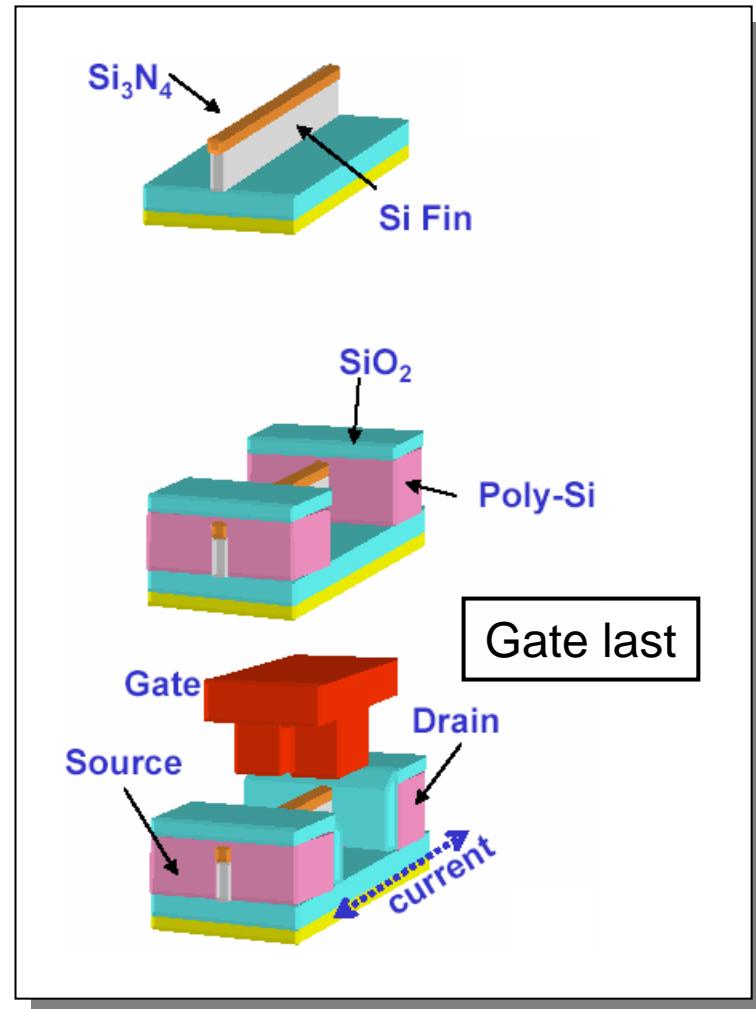
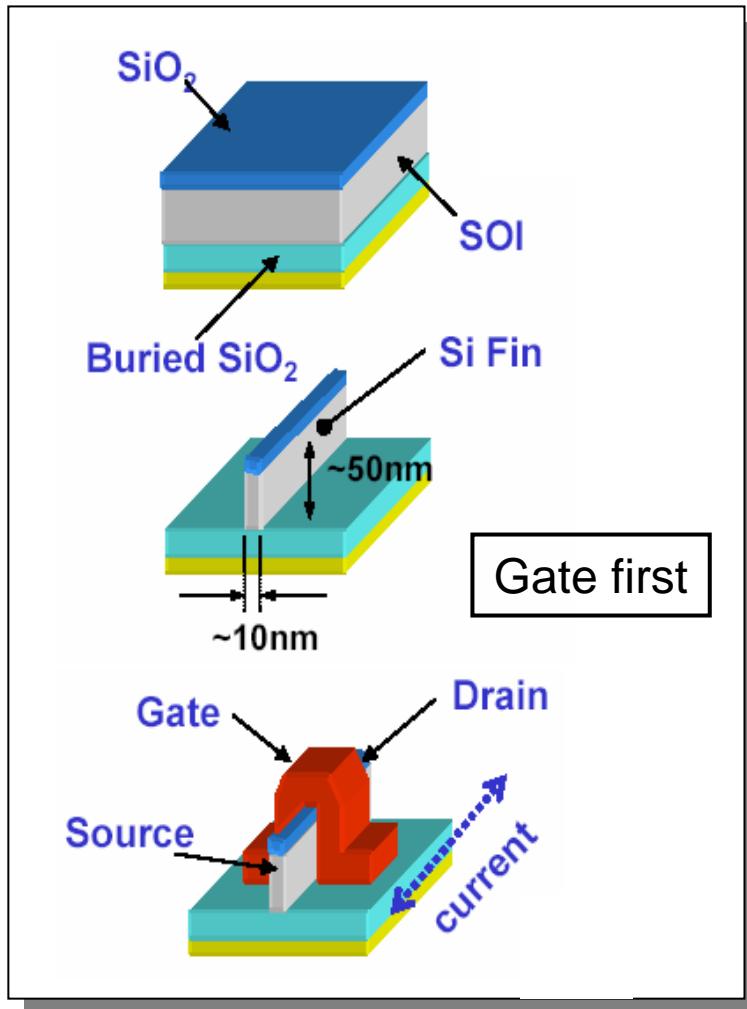
FinFET

- The FinFET is a non-planar device, which can have different gate configuration (DG, DELTA, PI, OMEGA)
- DG-FinFET process is simple, but still provide the same electrical advantages as the FD-SOI MOSFET



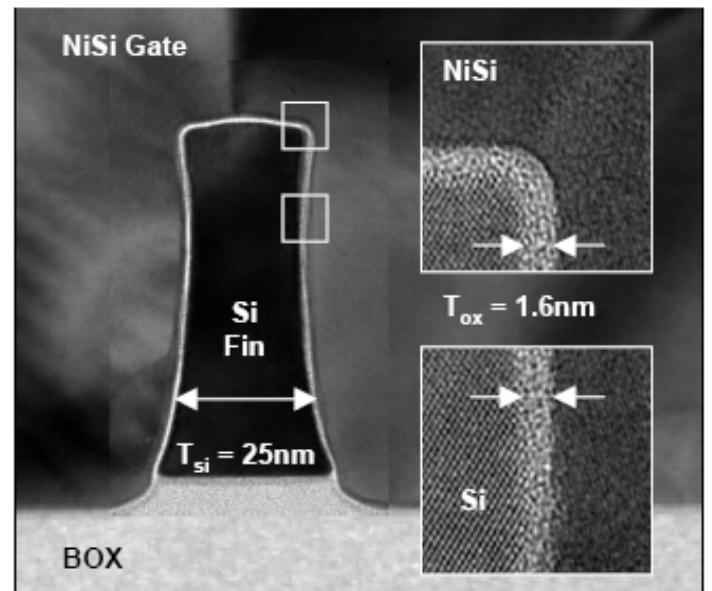
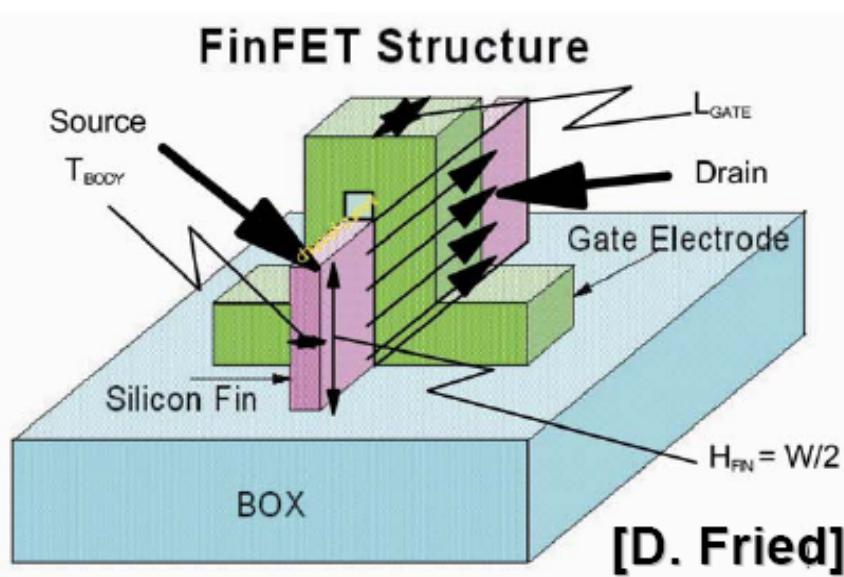


FinFET process flows





Example of FinFET



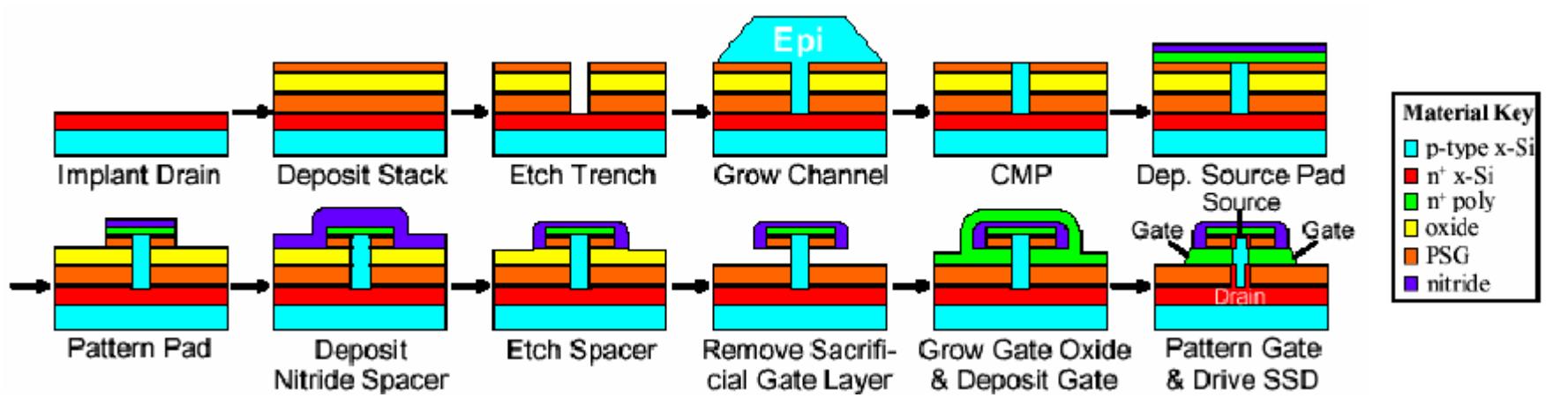
Challenges:

- **Source/Drain resistance engineering**
- **Contact formation**



VRG (Vertical Replacement Gate) MOSFET

- Several concepts for vertical MOSFETs have been demonstrated. VRG MOS seems to be the most promising
- Complex process: PMOS vs. NMOS, different LG, parasitics, circuit integration...





Summary non-classical devices

- Extensive research is on-going in exploring multi-gate structures (DG, FinFET...)
- Multi-gate MOSFETs will definitely extend the scaling horizon for CMOS
- Several issues remain to be solved, e.g. how to control Fin dimensions? – Fin thickness determined by lithography and etch
- RF-properties have to be characterized and appropriate devices models have to be developed
- Is there some unknown show-stopper?



Outline

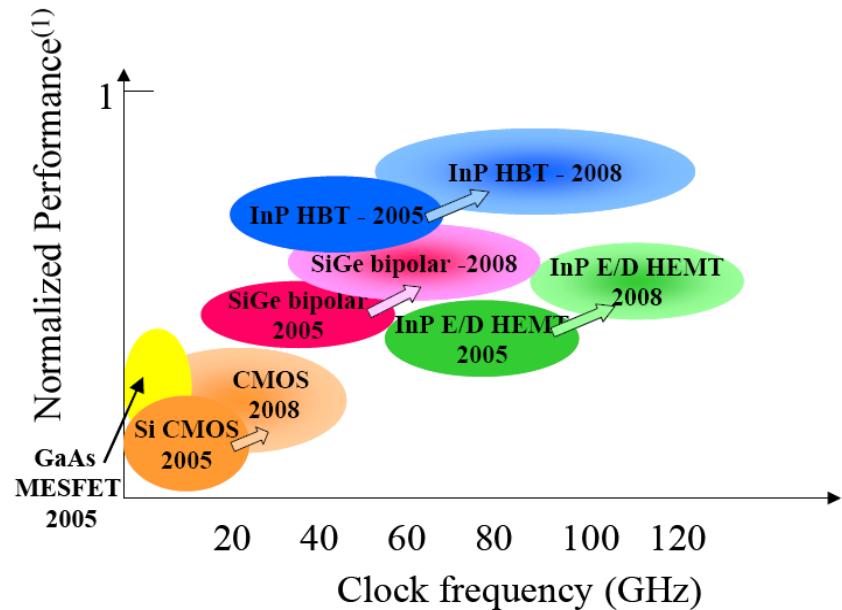
- Introduction
- Basic function of silicon MOSFET
- Manufacturing of CMOS
- MOSFET modeling
- SOI-MOSFET
- Scaling of CMOS
- Future CMOS
 - Strained-Si, SiGe, and non-classical devices
- **Summary**





Summary (I)

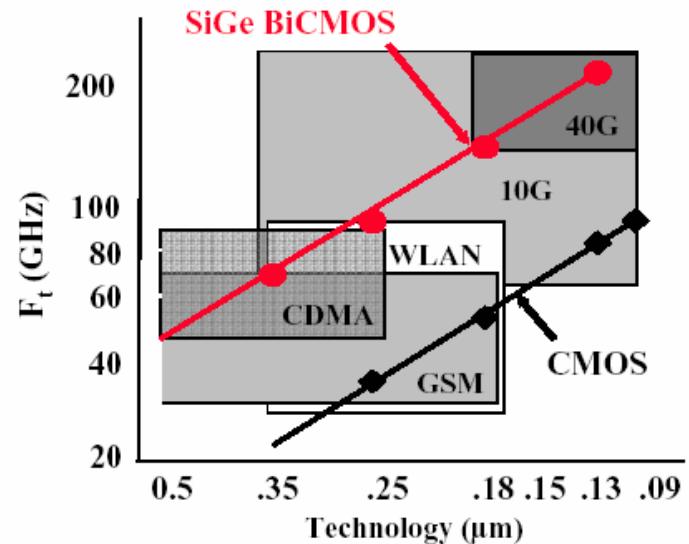
- RF-CMOS is today a well established technology and has found many applications up to around 5 GHz
- Further scaling of CMOS predicts even better RF-performance and extends up in frequency



The metric for performance depends on the class of circuit. It can include dynamic range, signal-to-noise, bandwidth, data rate, and/or inverse power.

Figure 48 Mixed-signal/Ultra High-speed Digital

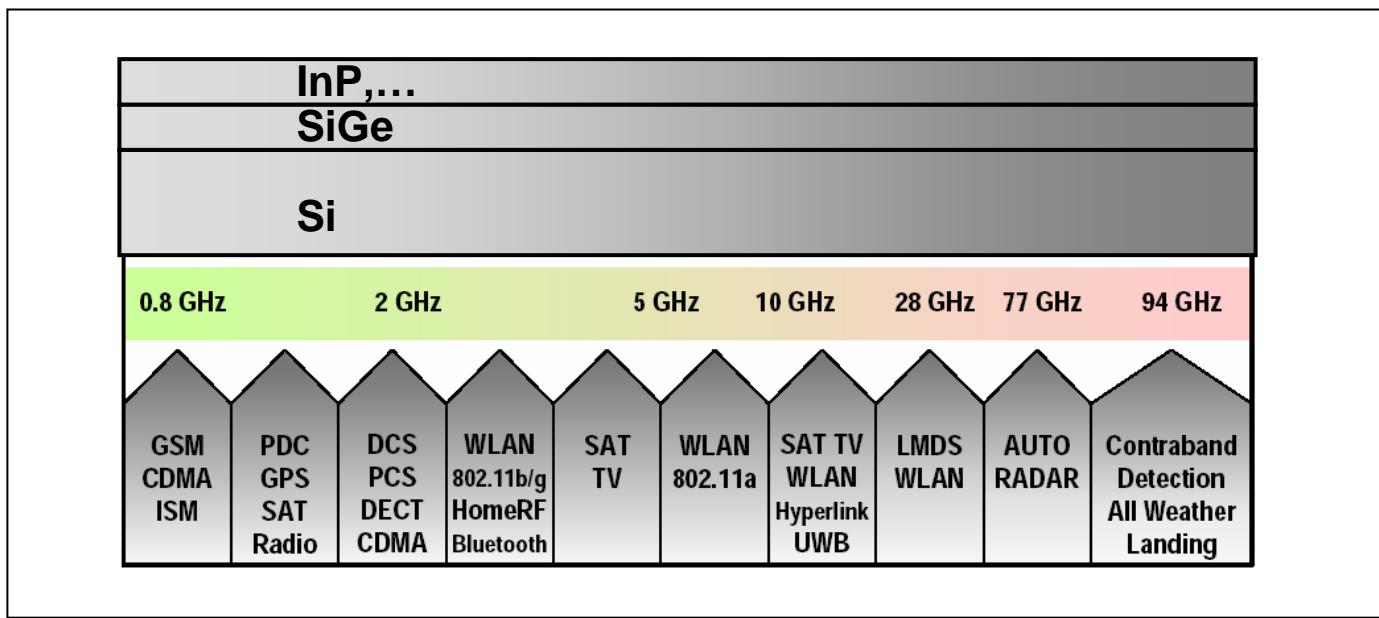
Source: ITRS 2005





Summary (II)

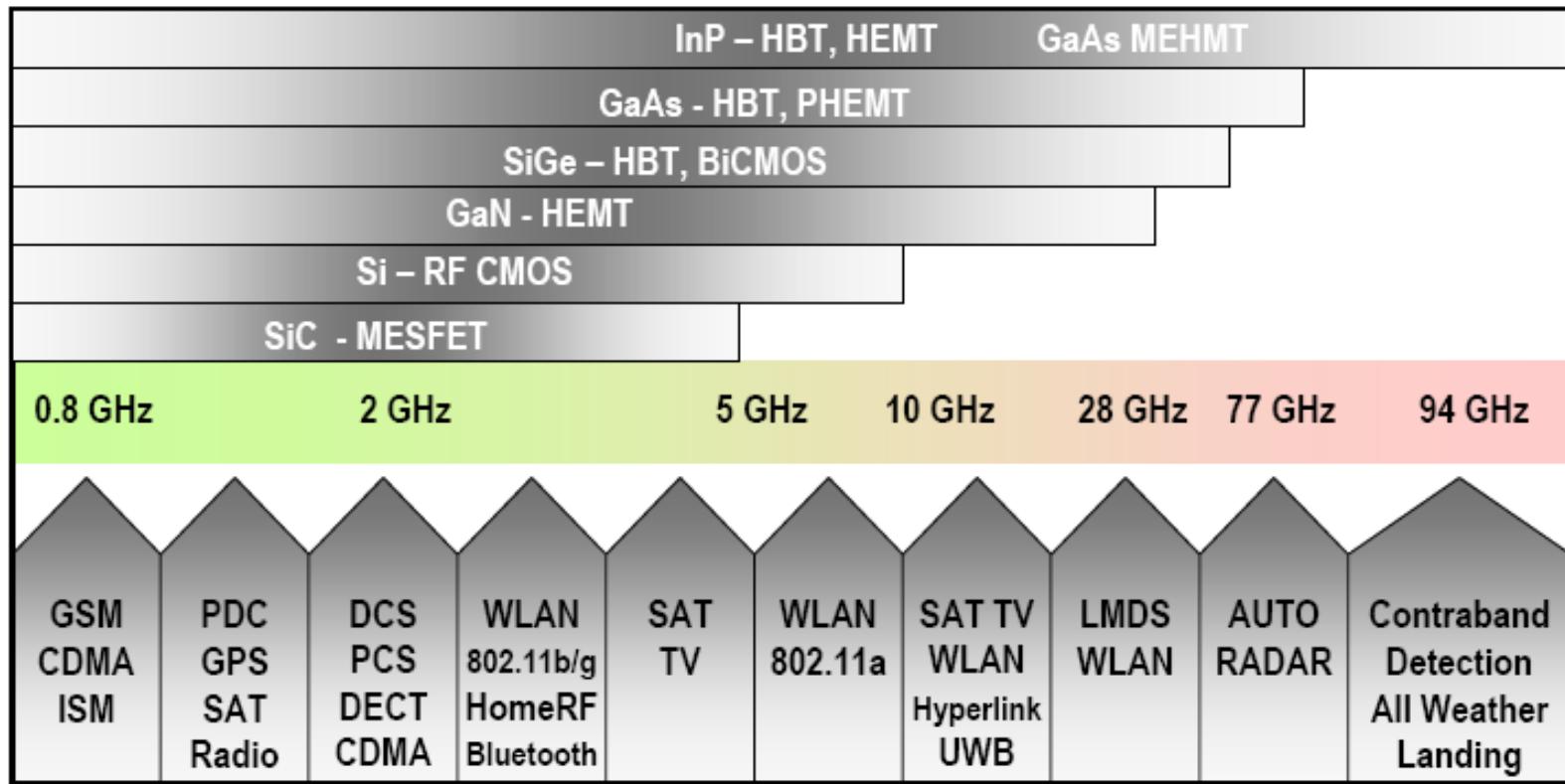
- **2003 prediction: In the future many different technologies will cover the frequency range 1-100 GHz**
- **Performance in terms of e.g. noise, efficiency, linearity, output power, and cost will determine the choice**
- **CMOS will always compete with low cost**





Summary (III)

- 2003 prediction seems to be included in ITRS 2005!





Acknowledgment

- Prof. Andrej Litwin, Infineon Technologies
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-
- The preparation of this presentation was performed in the context of the network TARGET– “Top Amplifier Research Groups in a European Team” and supported by the Information Society Technologies Programme of the EU under contract IST-1-507893-NOE, www.target-org.net



2001 IEEE GaAs IC Symposium

Basics of GaAs, InP, and SiGe RFICs

RFIC Design Examples

Stephen I. Long

**Dept. of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106**

RFIC Design Examples

- Digital: static frequency divider
- Analog: wideband transimpedance amplifier
- Emphasize design and analysis techniques
- Simulation complements but does not replace analytical techniques

Application Example #1

- 1. Digital: Static Frequency Divider
 - Why SFD?
 - Device figures of merit & equivalent circuit model
 - How to increase clock frequency
 - Delay analysis: RC delay terms
 - Device parameters, current density, scaling

Why Static Frequency Dividers?

Master-Slave Flip-Flop

MS flip-flops resynchronize data to clock

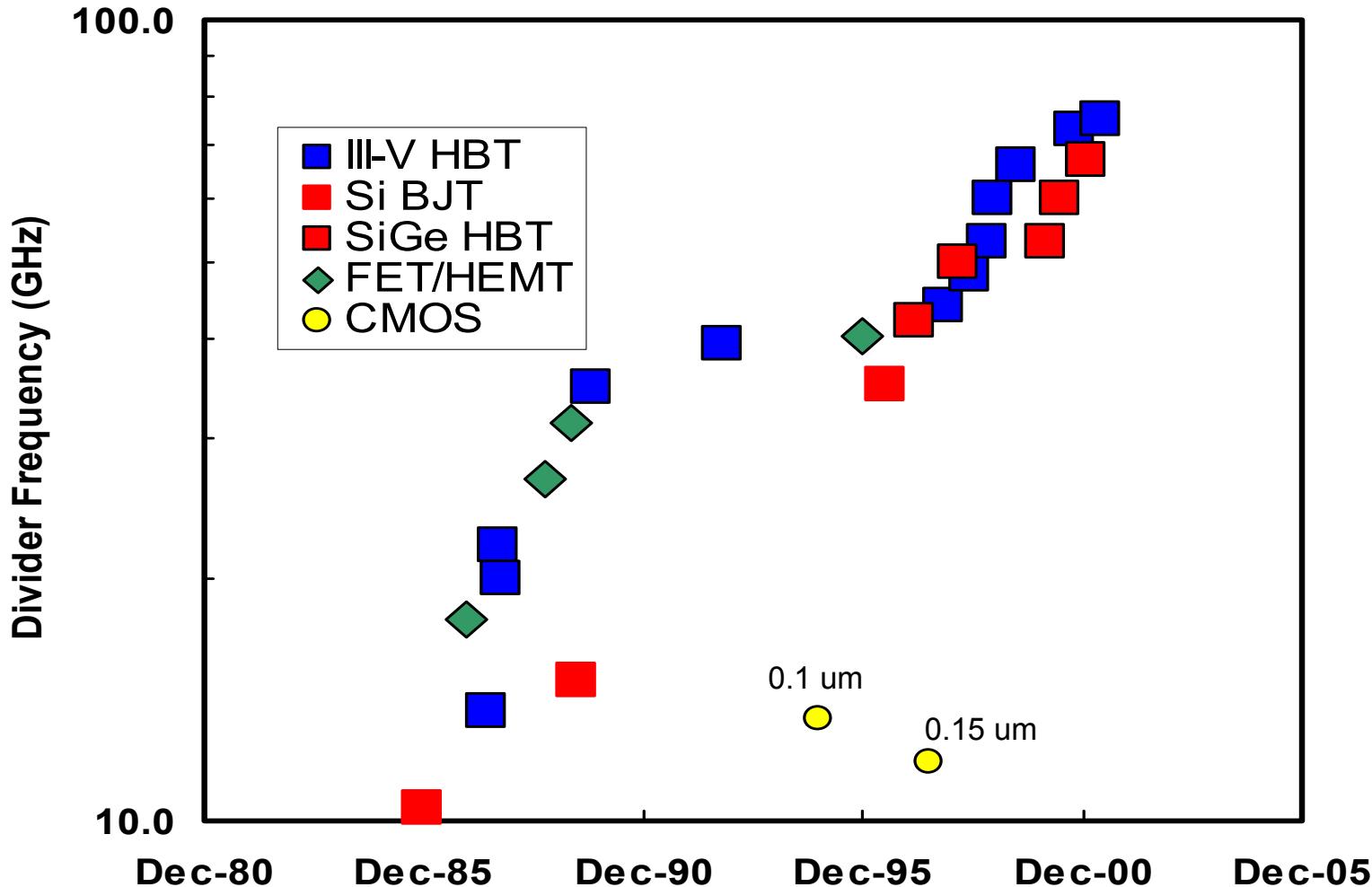
connection as 2:1 frequency divider provides simple test method.

Standard benchmark of logic speed

performance comparisons across technologies

Technology	Max freq (GHz)	Power (mW)	Ref.
Si MOSFET	16.8	3	5.2
Si BJT	30	630	5.3
AlGaAs/GaAs HBT	34.8	495	5.4
InAlAs/InGaAs PHEMT	49.2	290	5.5
SiGe HBT	67	175	5.6
InAlAs/InGaAs HBT	72.8	55	5.7
InAlAs/InGaAs TSHBT	75	800	5.8

Logic Speed: III-V vs. Silicon

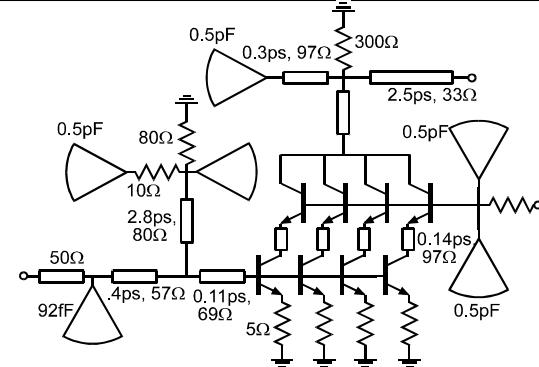
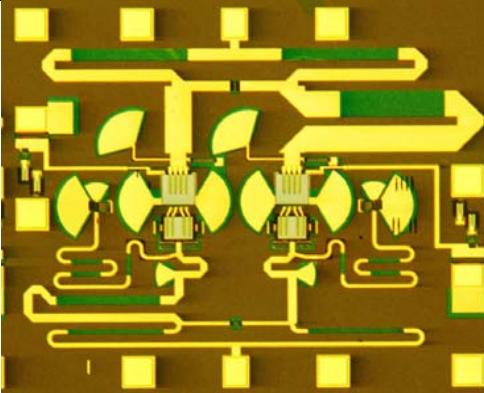


Benchmark: master-slave flip-flop configured as 2:1 **static** frequency divider

Source: M. Sokolich, HRL, M. Rodwell, UCSB

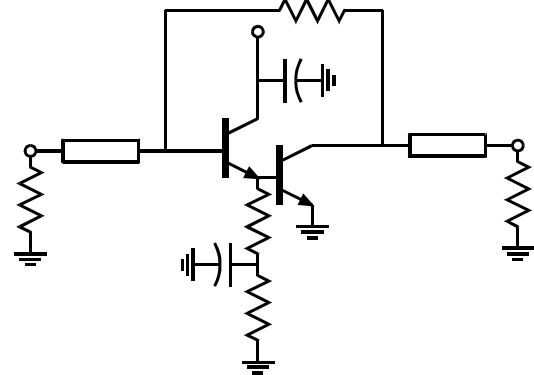
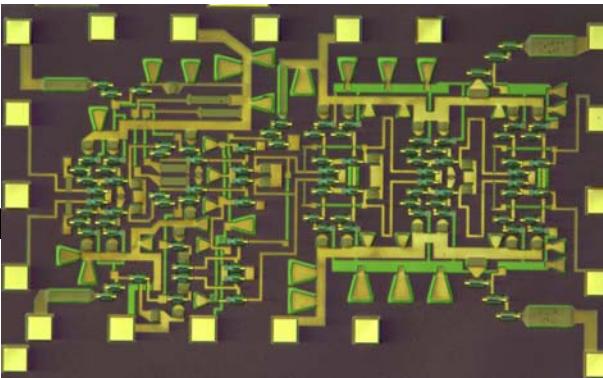
What do we need: f_τ , f_{max} , or ... ?

Tuned ICs (MIMICs, RF):
fmax sets gain,
& max frequency, not ft.

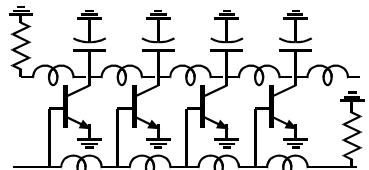
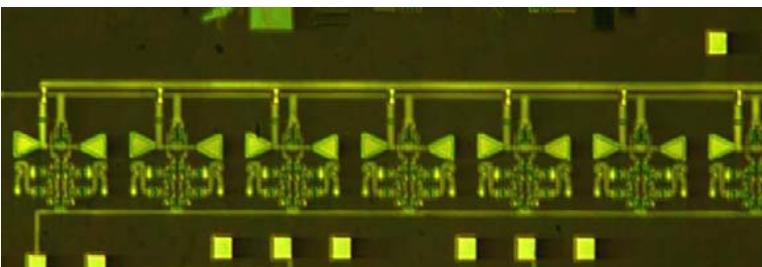


Lumped analog circuits
need high & comparable ft
and fmax.

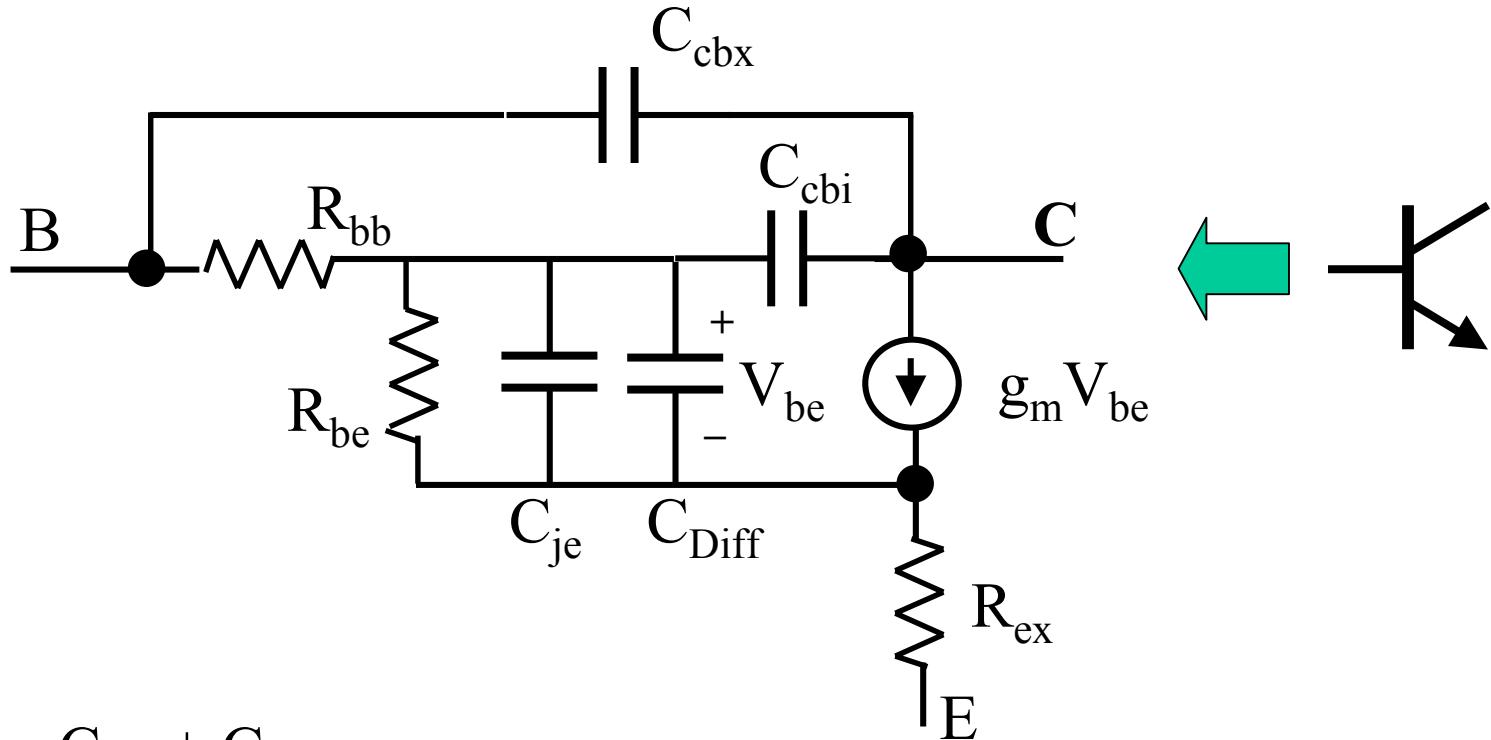
(1.5:1 fmax/ft ratio often cited
as good...)



Distributed Amplifiers
in principle, fmax-limited,
ft not relevant....
(low ft makes design hard)



Hybrid pi HBT equivalent circuit



$$C_{cb} = C_{cbi} + C_{cbx}$$

C_{cbi} is adjusted to give the correct f_{max} . Not geometrically determined

$$C_{diff} = g_m(\tau_b + \tau_c)$$

What determines digital circuit speed?

- Neither f_T nor f_{max} predict digital circuit speed

$$\frac{1}{2\pi f_T} = \tau_B + \tau_c + \frac{kT}{qI_c} (C_{je} + C_{cb}) + (R_{ex} + r_c) C_{cb}$$

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_{bb} C_{cb}}}$$

- RC time constant analysis can guide the design
- Must consider both large signal and small signal parameters as required by circuit application

Propagation Delay Estimation

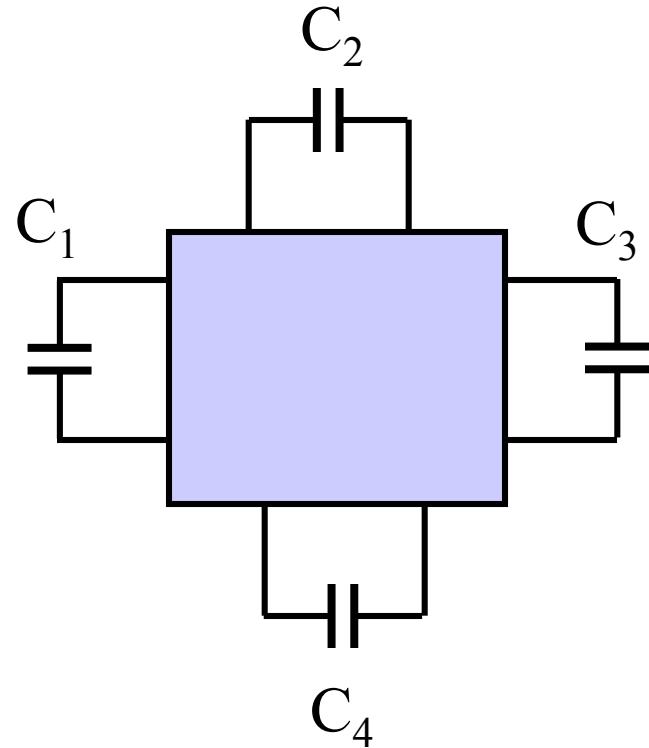
- Find t_{pd}
 - Analytical model can identify dominant time constants
 - Determine sensitivity to:
 - Device parameters
 - Bias current, voltage swing, device area
 - Wiring delays, loading due to fanout
- SPICE or ADS simulation
 - accurate as the device models
 - Estimate of t_{pd} doesn't give great insight
 - Can use for sensitivity analysis – $\Delta t_{pd}/\Delta x_i$

Analytical Delay Models

- Elmore/Ashar requires deriving $H(s)$
 - Frequency domain
 - Nasty unless circuit is small [Refs 4.1, 4.8]
- Open-Circuit Time Constants [Refs.4.3, 4.4]
 - Easy. The method decouples the circuit
 - Uses linearized equivalent device model
 - Always predicts equal rise/fall times
- Charge control analysis: $\Delta t = \Delta Q / 2I$ [Ref. 4.7]
 - Similar result to OCTC method

Open-circuit time constants

- Redraw network with all capacitors outside the box
- No inductors allowed
- OCTC method can estimate the 3 dB bandwidth and the propagation delay
- Assume first order dominant pole. Moderate error if complex conjugate poles or zeros in the network.



Ref. 4.3, 4.4

Open-circuit time constants

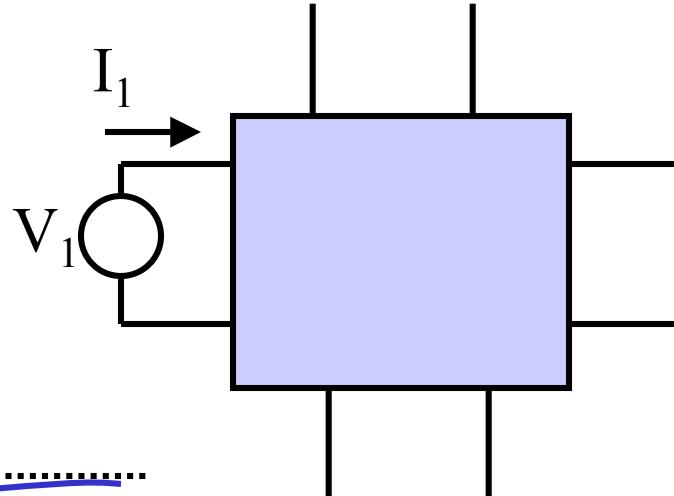
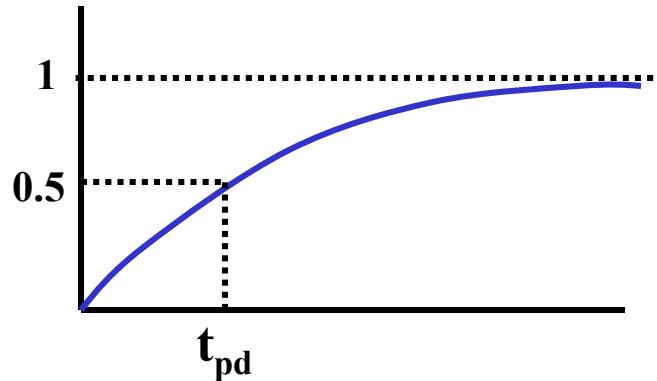
Remove all capacitors

$R_{ii}^o = V_i/I_i$ open circuit R presented to i^{th} capacitor

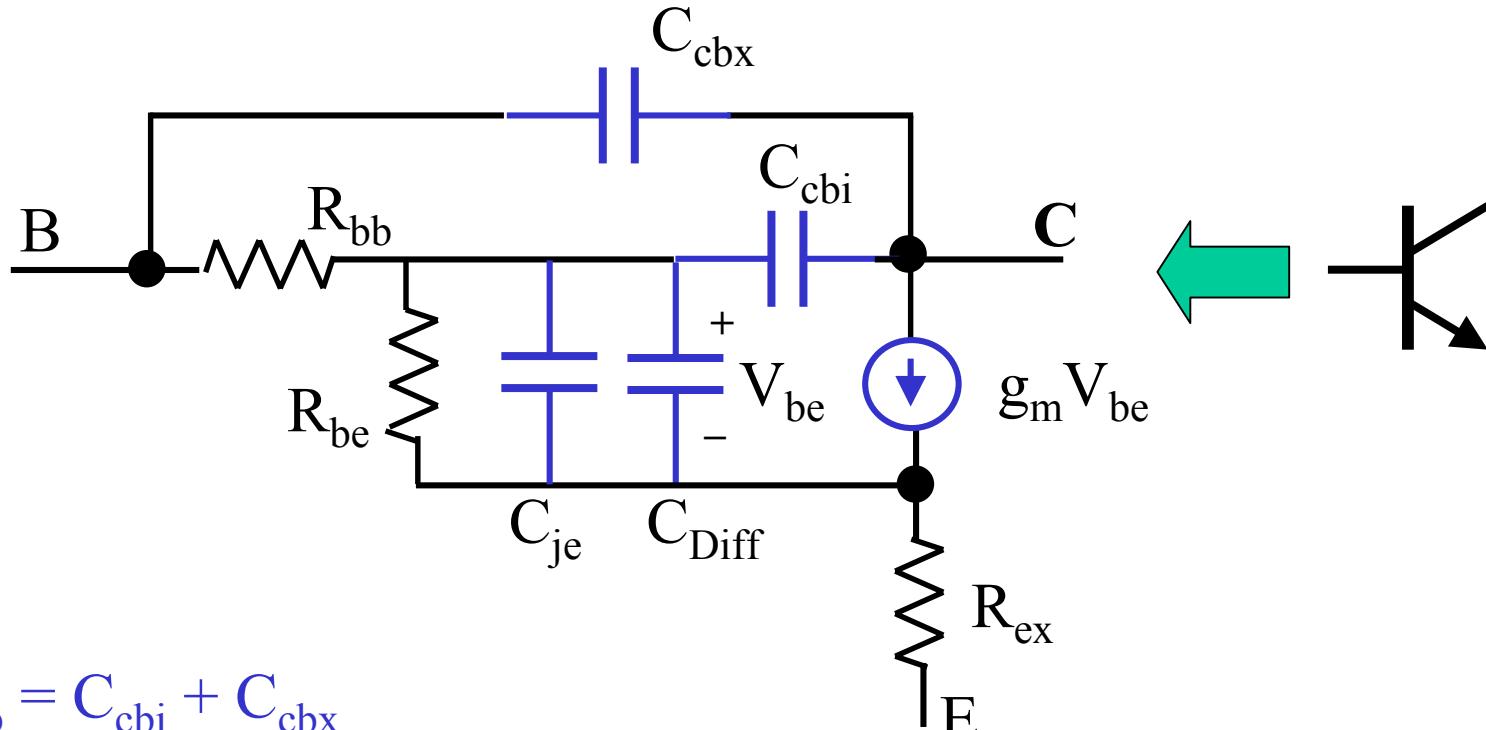
$$a_1 = \sum_{i=1}^n R_{ii}^o C_i$$

$$f_{3dB} = \frac{1}{a_1}$$

$$t_{pd} = (\ln 2) a_1$$



Hybrid pi HBT equivalent circuit



$$C_{cb} = C_{cbi} + C_{cbx}$$

C_{cbi} is adjusted to give the correct f_{max} . Not geometrically determined

$$C_{diff} = g_m(\tau_b + \tau_c)$$

Ref: 4.10

Propagation Delay Estimation

1. All nonlinear capacitances are linearized over the appropriate voltage range:

Depletion capacitances (Mainly C_{je})

$$C_{eq} = \frac{\Delta Q}{\Delta V} = \frac{Q(V_H) - Q(V_L)}{V_H - V_L} = K_{eq} C_{j0}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_H - V_L)(1-m)} \left[(\phi_0 - V_H)^{1-m} - (\phi_0 - V_L)^{1-m} \right]$$

Ref. 4.7

Propagation Delay Estimation

Diffusion Capacitance

Charge storage in base and collector regions

$$C_D = \tau_F G_M \quad \text{Large signal}$$

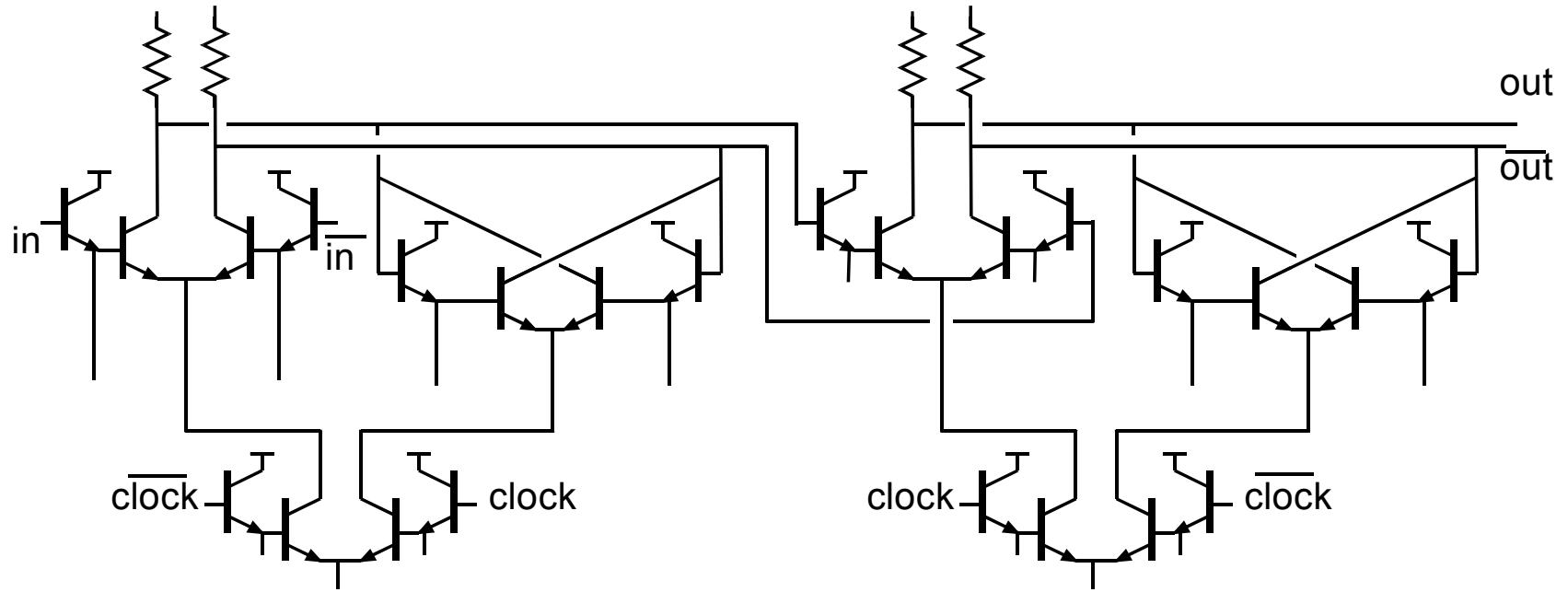
$$C_D = \tau_F g_m = \frac{\tau_F q I_C}{n k T} \quad \text{Small signal}$$

Transconductance is linearized for large signal case:

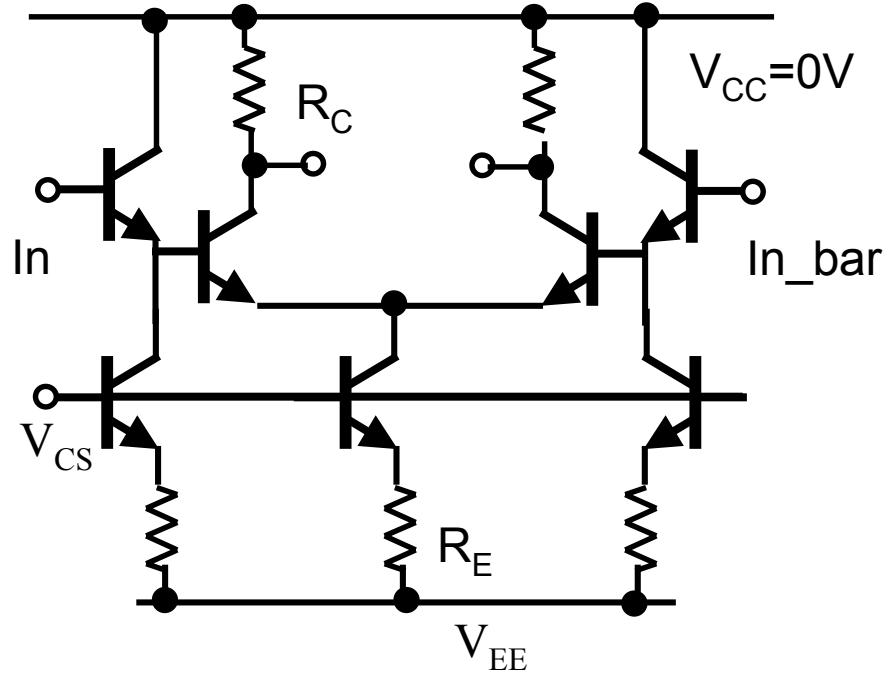
$$G_M = \frac{I_C(V_H) - I_C(V_L)}{V_H - V_L} = \frac{I_{EE}}{\Delta V_{Logic} - I_{EE} R_{ex}}$$

Ref. 4.7

Master-Slave Flip-Flop

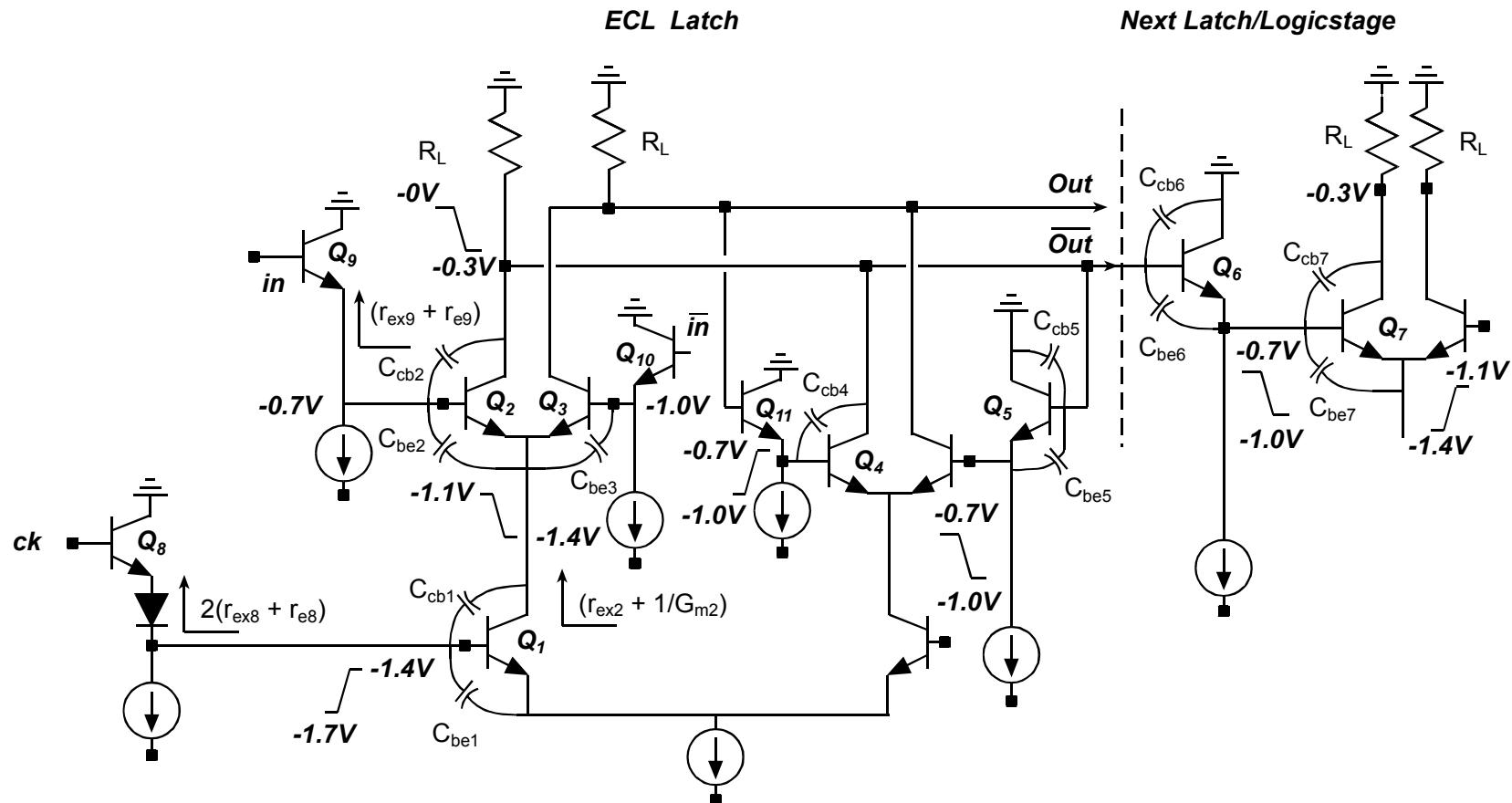


ECL DC Design



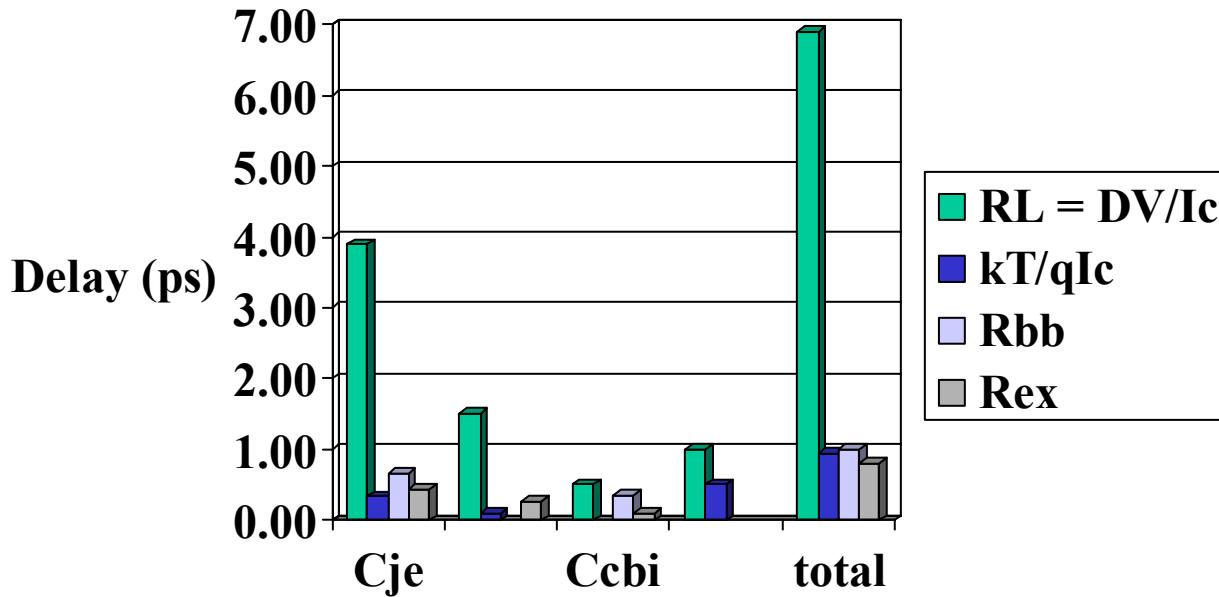
1. $\Delta V > 6 (kT/q + I_c R_{ex})$
 2. Bias devices at peak f_T, J_{max}
 3. All devices active or cutoff
 4. Thermal limitations

DC analysis: determine voltage swings



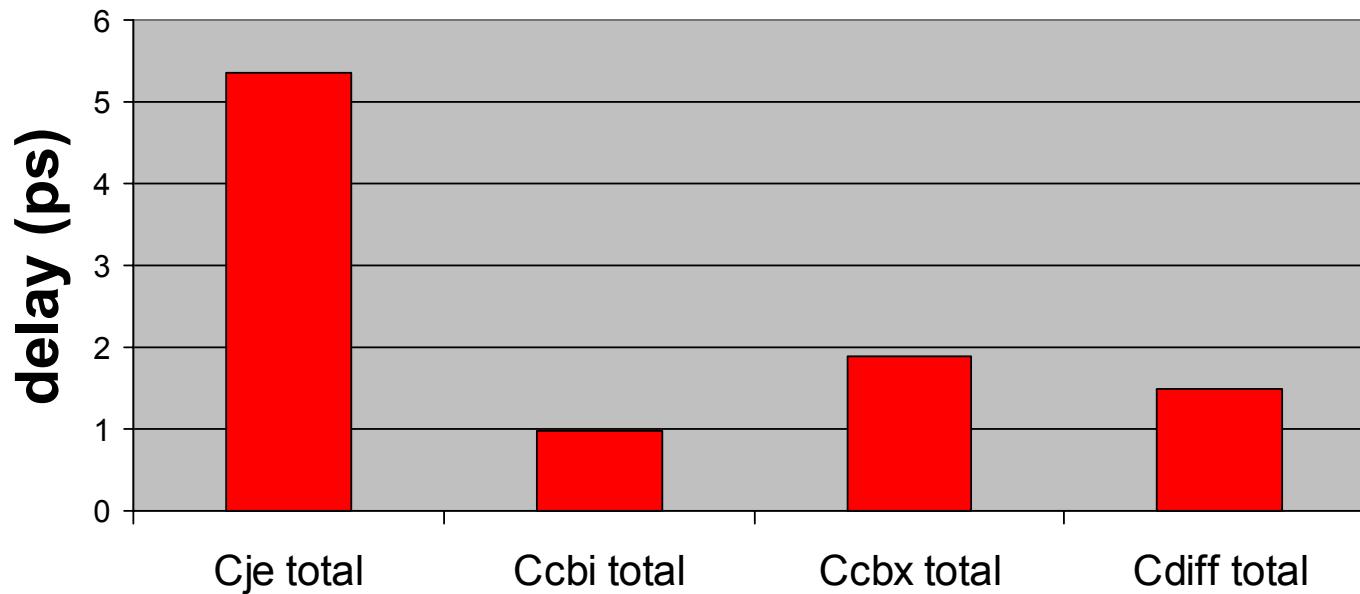
Source: T. Mathew, UCSB

What HBT parameters determine logic speed ?



Calculate $R_{ii}^0 C_i$ time constants for each capacitor

Relative contribution of capacitances



$$\text{Total delay} = \tau = 9.7 \text{ ps} \quad t_{pd} = 0.7 \tau = 6.8 \text{ ps}$$

$$\text{SFD maximum clock frequency} = 1/(2t_{pd}) = 73.5 \text{ GHz}$$

What HBT parameters determine logic speed ?

	C _{je}	C _{cbx}	C _{cbi}	C _{diff}	total	%
R _L = $\Delta V/I_C$	3.90	1.50	0.50	1.00	6.90	71
kT/qI _C	0.34	0.10	-	0.50	0.94	10
R _{bb}	0.66	-	0.35	-	1.00	11
R _{ex}	0.44	0.27	0.10	-	0.81	8
total	5.34	1.90	1.00	1.50	9.70	100
% of total delay	55	20	10	15	100	

Sorting delays by capacitances:

55% C_{je}; 30% C_{cb}; only 15% C_{diff} [e.g. (τ_b + τ_c)]

Sorting delays by resistances and transit times:

71% ΔV_{logic}/I_C; 11% R_{bb}; 15% (τ_b + τ_c)

R_{ex} has a strong indirect effect

$$\Delta V > 6(kT/q + R_{ex}I_C)$$

What do we need for fast logic ?

Gate Delay Determined by :

Depletion capacitance charging through the logic swing

$$\left(\frac{\Delta V_{LOGIC}}{I_C} \right) (C_{cb} + C_{be,\text{depletion}})$$

Depletion capacitance charging through the base resistance

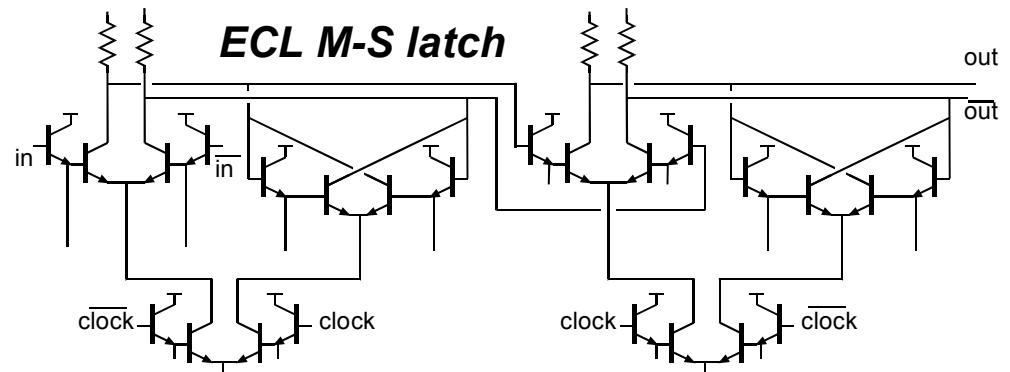
$$R_{bb} (C_{cb} + C_{be,\text{depletion}})$$

Supplying base + collector stored charge through the base resistance

$$R_{bb} (\tau_b + \tau_c) \left(\frac{I_C}{\Delta V_{LOGIC}} \right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6 \left(\frac{kT}{q} + R_{ex} I_c \right)$$



Neither f_τ nor f_{max} predicts digital speed

$C_{cb}\Delta V_{logic}/I_c$ is very important

→ **collector capacitance reduction is critical**

→ **increased III-V current density is critical**

R_{ex} must be very low for low ΔV_{logic} at high J_c

InP: R_{bb} , $(\tau_b + \tau_c)$, are already low, must remain so

Source: M. Rodwell, UCSB

Improving Delay

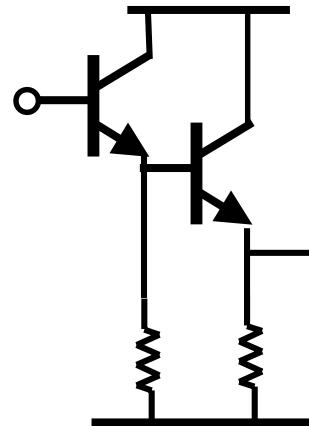
- Optimize emitter width
- Scale device areas for minimum delay
 - emitter areas of emitter follower and diff pair HBTs need to be separately optimized

Improving Delay

- Differential interconnections
 - Lower voltage swing
 - No reference voltage needed
 - Steeper pulse edges
 - Less crosstalk
 - Reduced jitter
- On-chip termination of transmission lines
 - Shunt termination with R_L at input of next stage
 - Even and odd mode terminations

Improving Delay

- Cascaded emitter followers
 - As f approaches f_T , current gain $\Rightarrow 1$
 - Used in SiGe due to lower f_T
 - Watch out for ringing! Z_{in} can have negative real part.



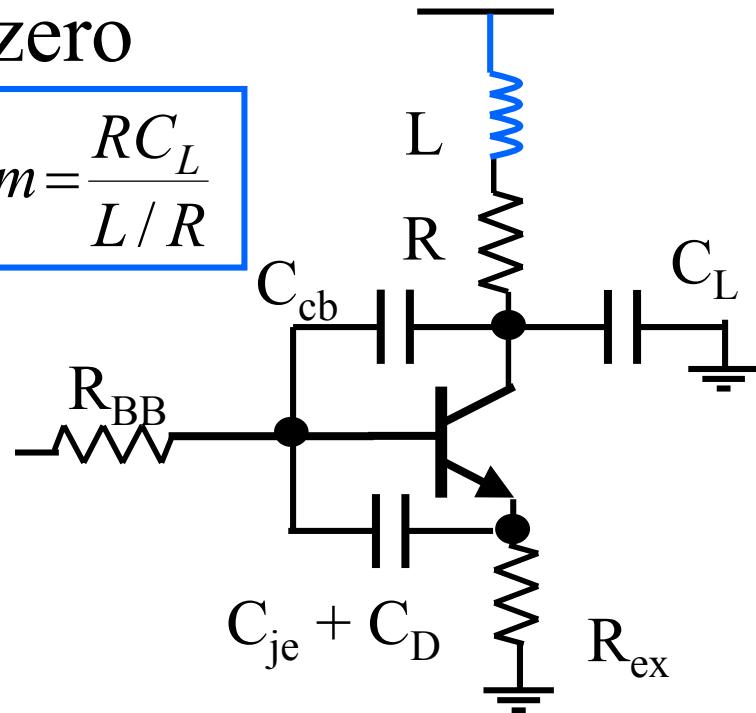
Ref. 4.9

Improving delay

- Shunt peaking: add zero

$$m = \frac{RC_L}{L/R}$$

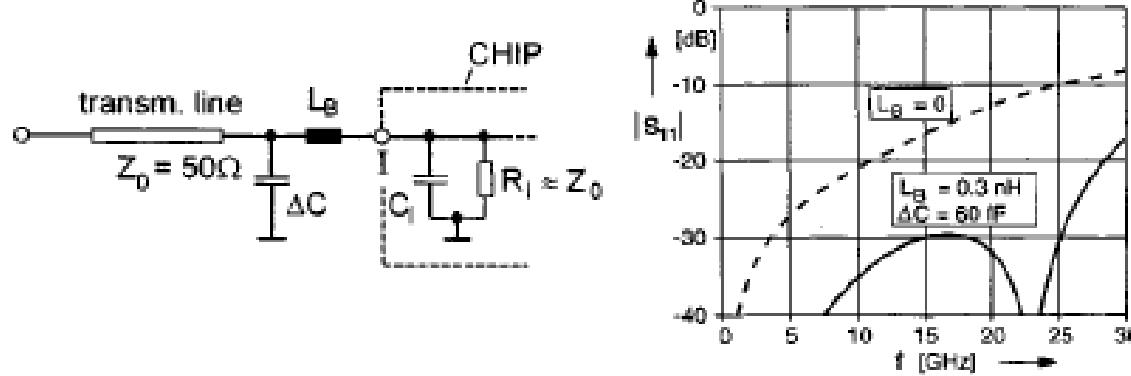
M	Risetime	Overshoot
1.66	2.1	11.4%
2.0	1.9	6.7
2.4	1.7	3.1
4.0	1.4	0
oo	1	0



Ref. 4.11

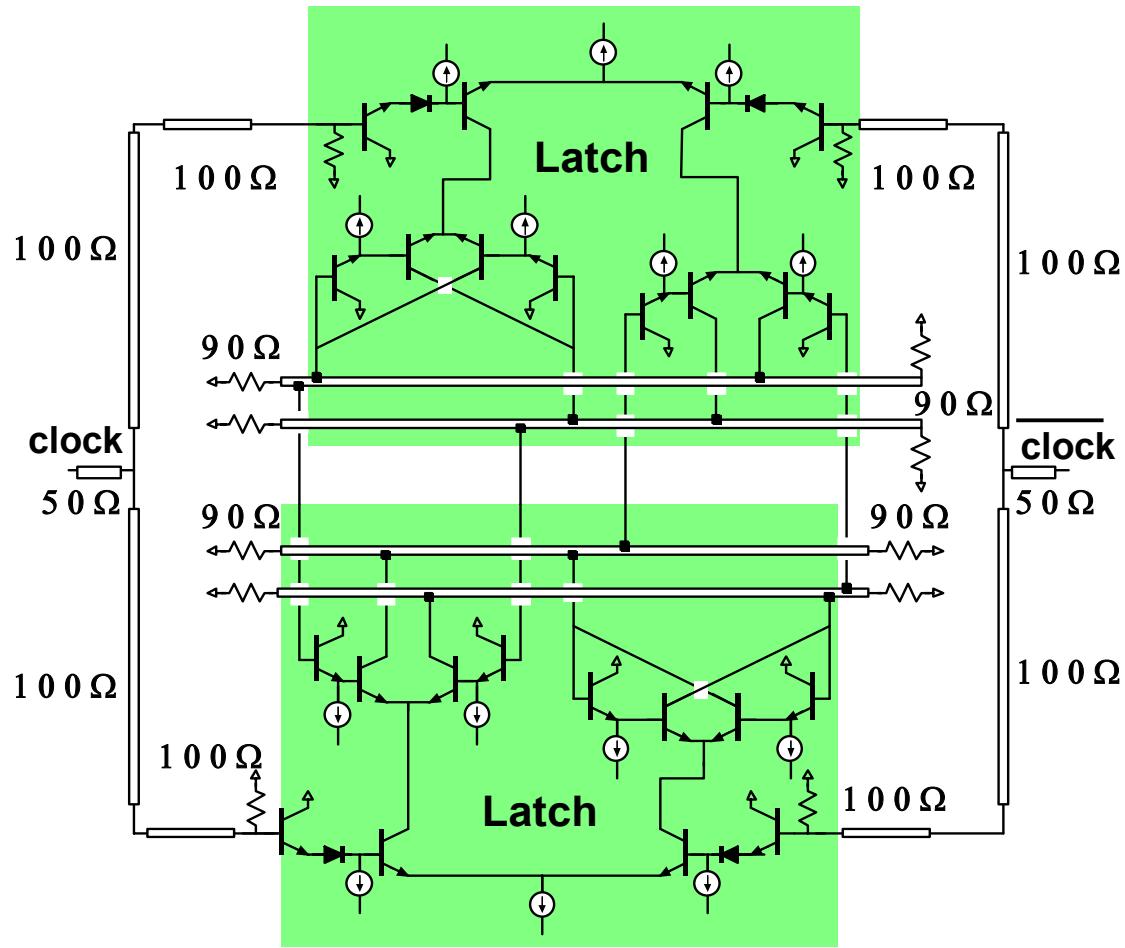
Improving delay

- Parasitic absorption
 - Use bondwire and capacitor to make lumped element transmission line at Z_0



Ref. H. M. Rein and M. Moller, IEEE J. Solid State Cir., pp. 1076-1089, Aug. 1996.

Circuit diagram: Static Frequency Divider



Design specs

- ECL topology
- $J_E = 1.0\ mA/\mu m^2$
- $V_{EE} = -3.5V$
- microstrip interconnect lines
- Internal node sees $\Delta V = 300\ mV$
- Output buffer has $\sim 100\ mV$ swing.

Results: 50 - 75 GHz measurements

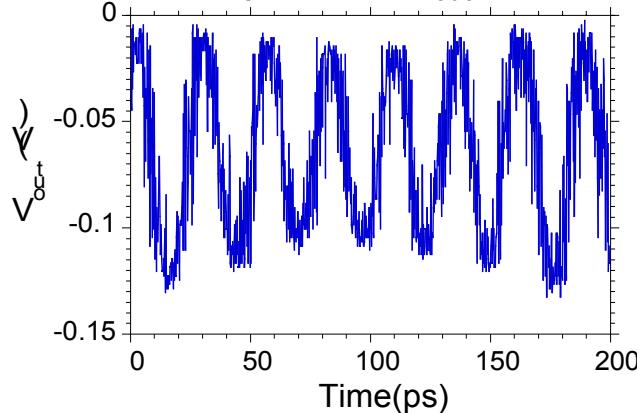
Operating conditions:

$$V_{EE} = -3.9 \text{ V}$$

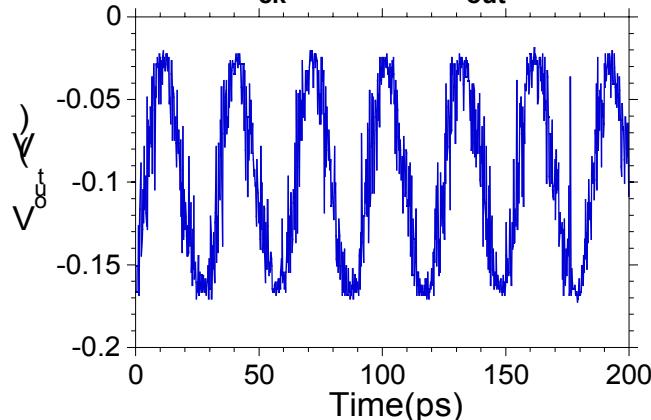
$$J_{e\max} = 1.8 \text{ mA}/\mu\text{m}^2$$

Power dissipated is 800 mW

Divider: $f_{\text{ck}} = 75 \text{ GHz}$, $f_{\text{out}} = 37.5 \text{ GHz}$



Divider: $f_{\text{ck}} = 66 \text{ GHz}$, $f_{\text{out}} = 33 \text{ GHz}$



Output waveform on oscilloscope

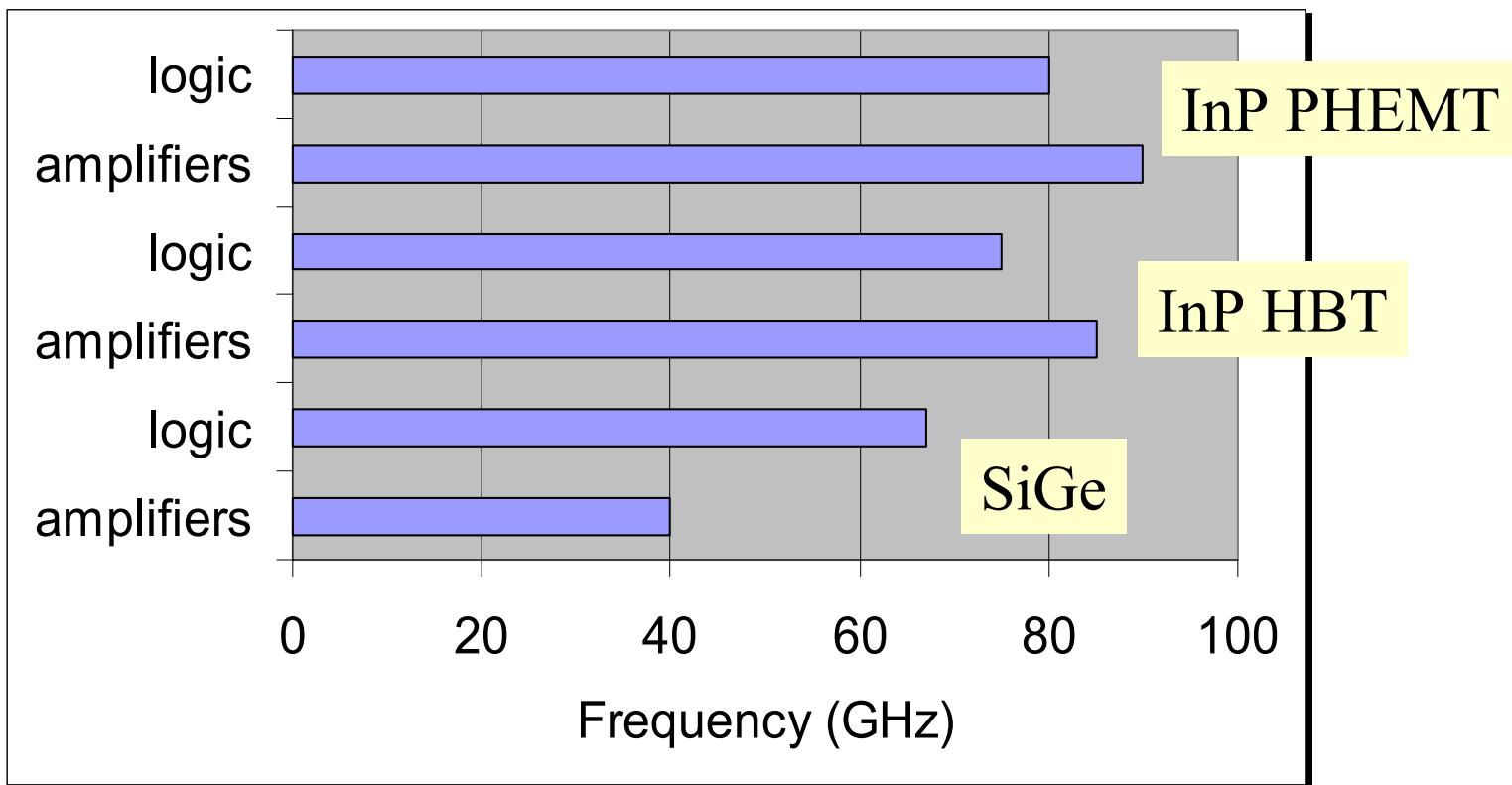
OCTC prediction: 73.5 GHz

ADS simulation: 90 GHz

Maximum measured: 75 GHz

Ref. 5.14

State-of-Art in HBTs, 2001: small-scale circuits

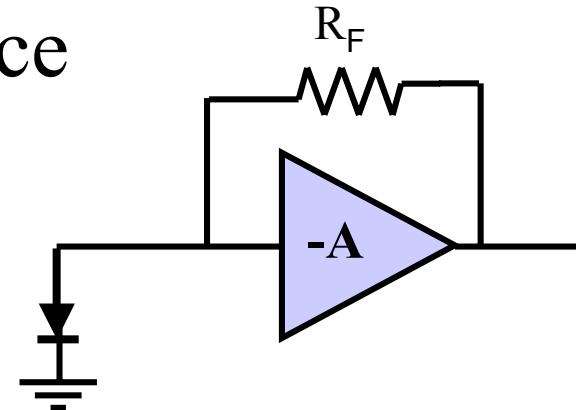


Si / SiGe has rough parity in logic with InP despite lower f_τ , f_{\max}
due to higher current density, better emitter contacts

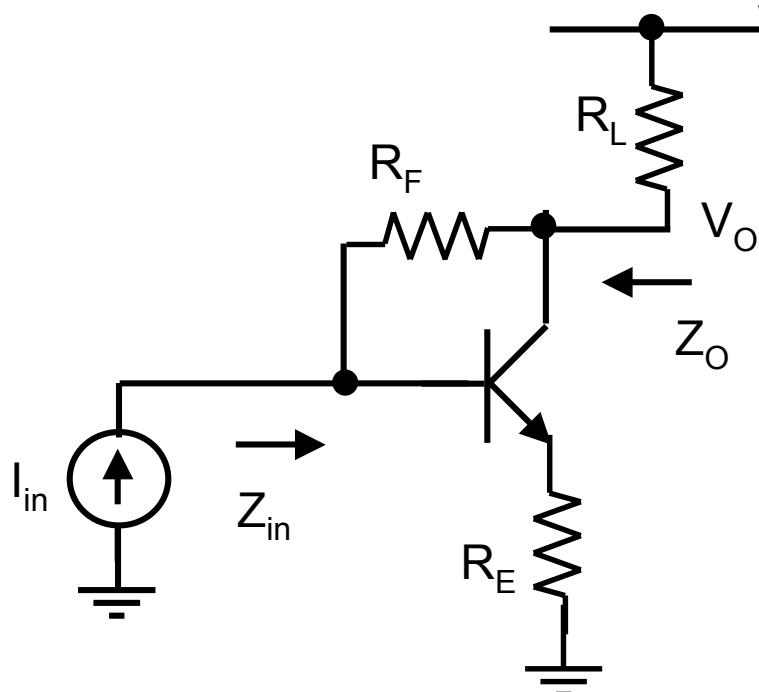
Si/SiGe has significantly slower amplifiers

Analog: application #2: Wideband amplifier

- 2. Photodiode preamp; limiting amps for CDR
 - Well-behaved transient response is essential
 - Data “eye” must remain open
 - Time constant analysis can again be useful
- Study amplifier performance
 - Transimpedance amp
 - Bandwidth enhancement
 - Transient response



TIA 1: CE with dual feedback



R_E and R_L set the gain;
 R_F sets Z_{in} and Z_o

Design equations:

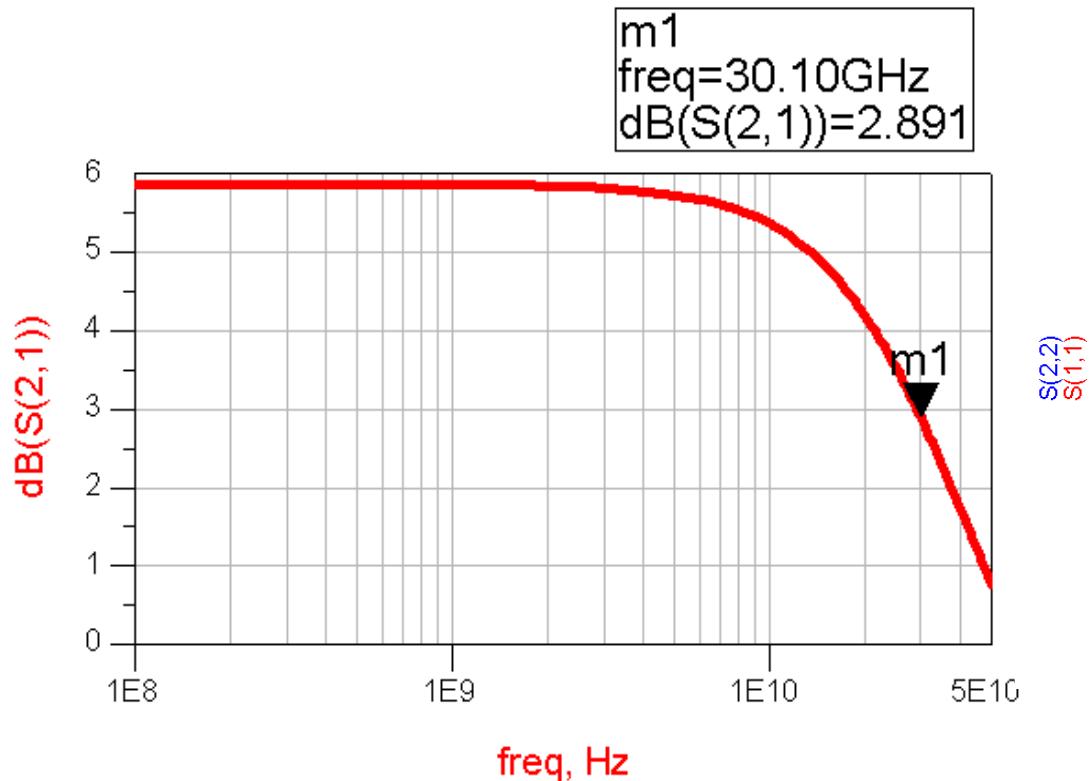
$$A_v = \frac{V_o}{I_i R_s} = -\frac{R_L}{R_E} \left[\frac{R_F - R_E}{R_F + R_L} \right]$$

$$Z_o = Z_{in} = R_s = R_L = R$$

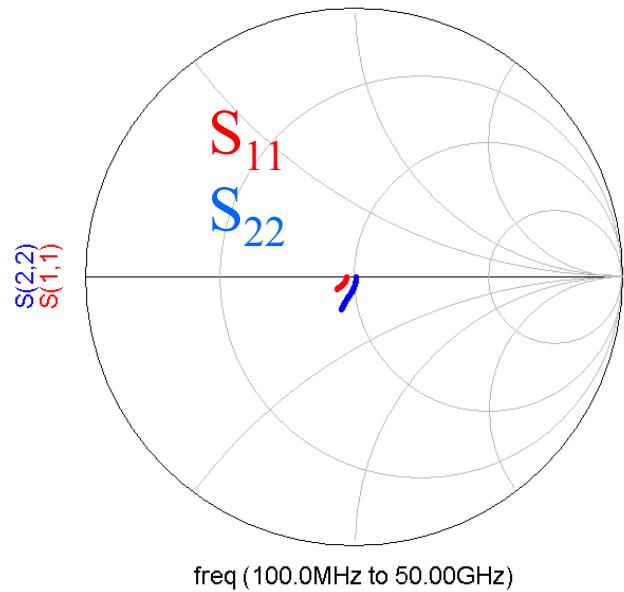
$$R = \frac{R_F}{1 - A_v}$$

Design for 50Ω , $S_{21} = 6$ dB
InP-based HBTs

CE with dual FB

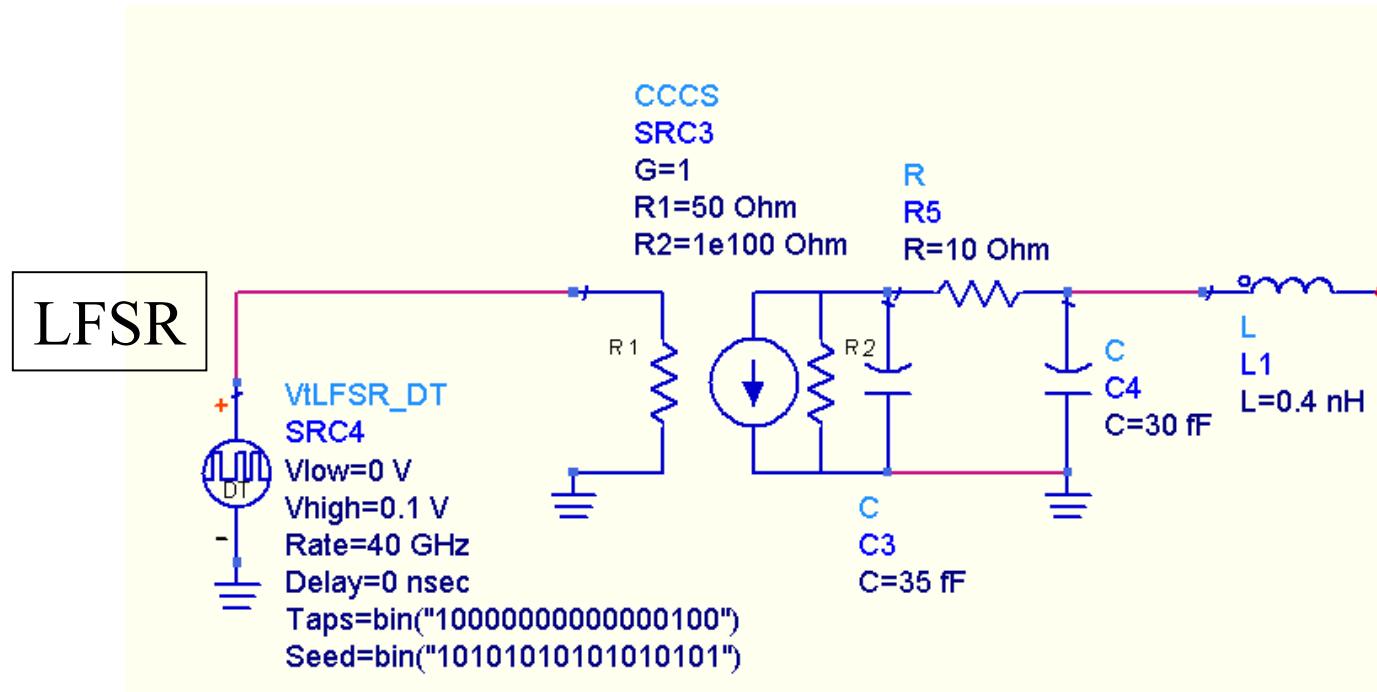


3 dB BW = 30 GHz



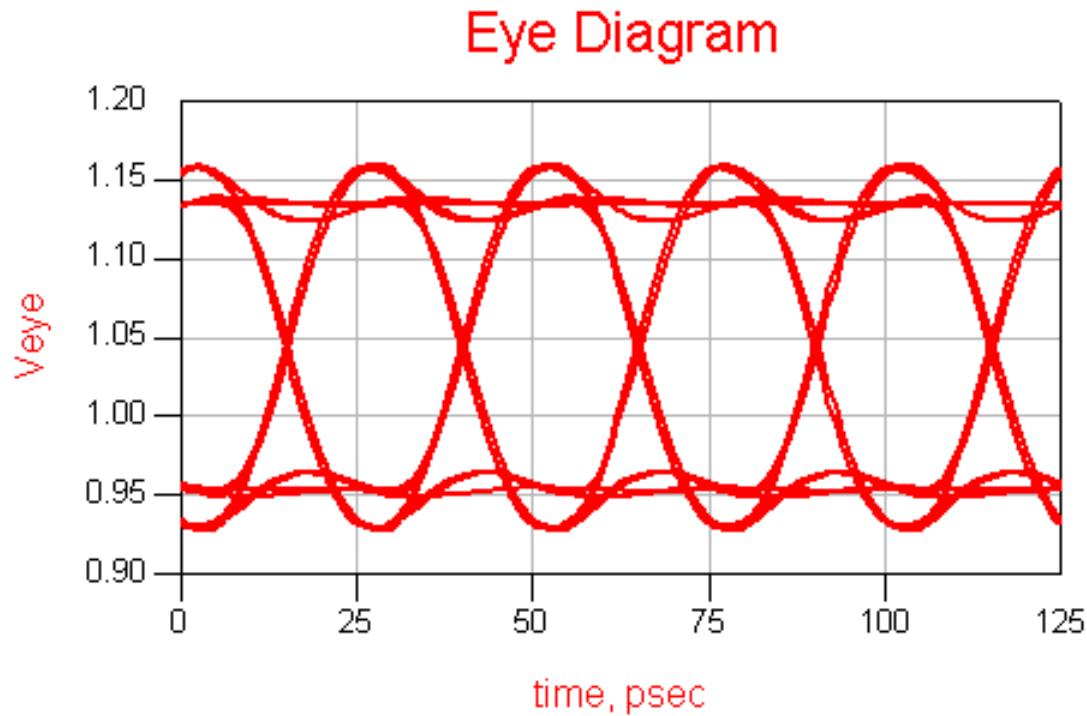
Model for 50 Gb/s photodiode

- Transient simulation
 - Model of source: photodiode with bondwire



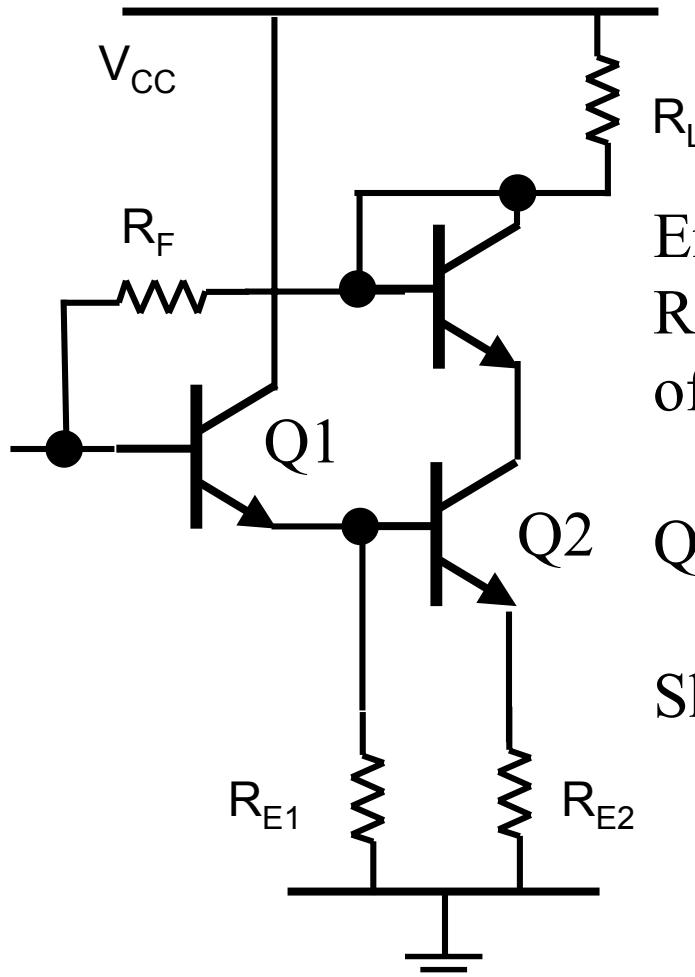
Ref: 6.1 H.-M. Rein

CE TIA 1: 40 Gb/s transient response



Well behaved transient response. 30 GHz bandwidth adequate

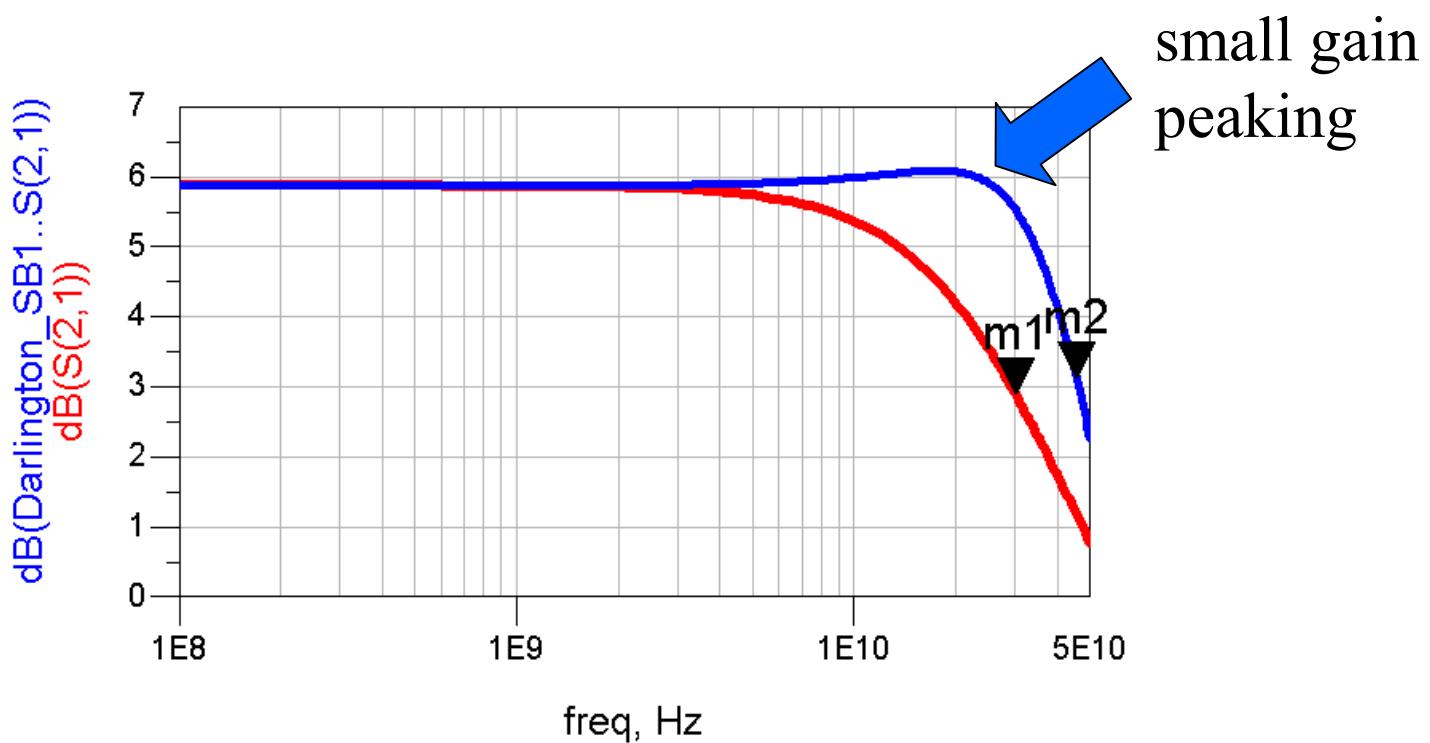
Improve BW: Darlington TIA 2



Emitter Follower first stage:
Reduces time constant at base
of Q2.

Q1 also decreases input capacitance

Shunt FB: R_F sets Z_{in} and Z_o



CE w. dual FB

30 GHz

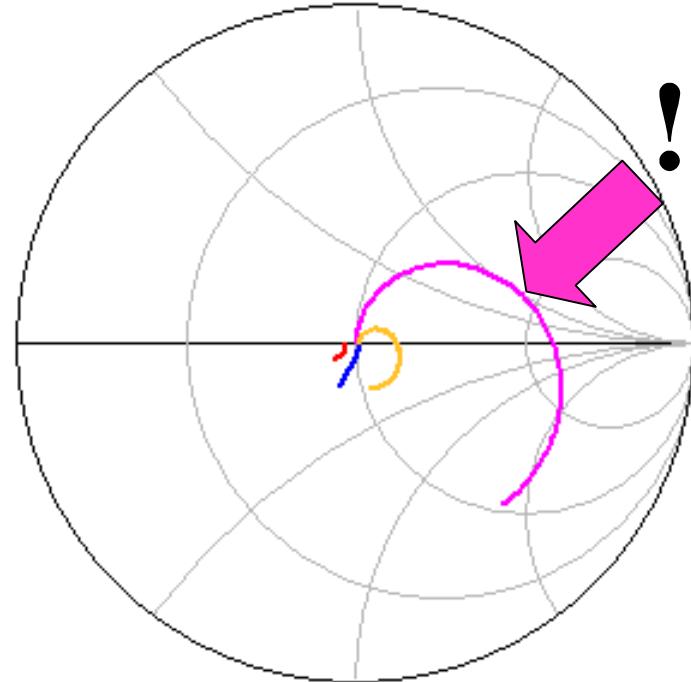
Darlington w. dual FB

45 GHz

Big bandwidth improvement!

S_{11} CE TIA 1
 S_{22}

Darlington SB1...SB2
Darlington SB1...SB2
 $S_{(1,1)}^{(2,2)}$



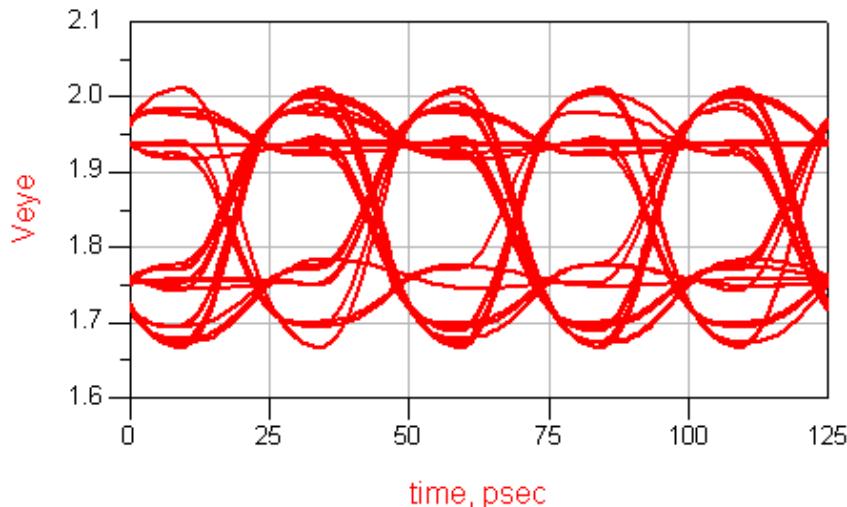
freq (100.0MHz to 50.00GHz)

S_{11} Darlington TIA 2
 S_{22}

We have exchanged
bandwidth for S_{11}

How will this affect
the transient response?

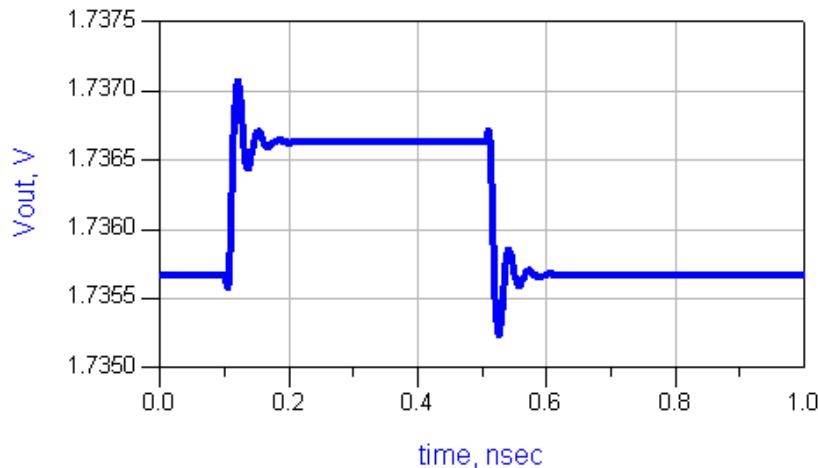
Eye Diagram



Darlington TIA

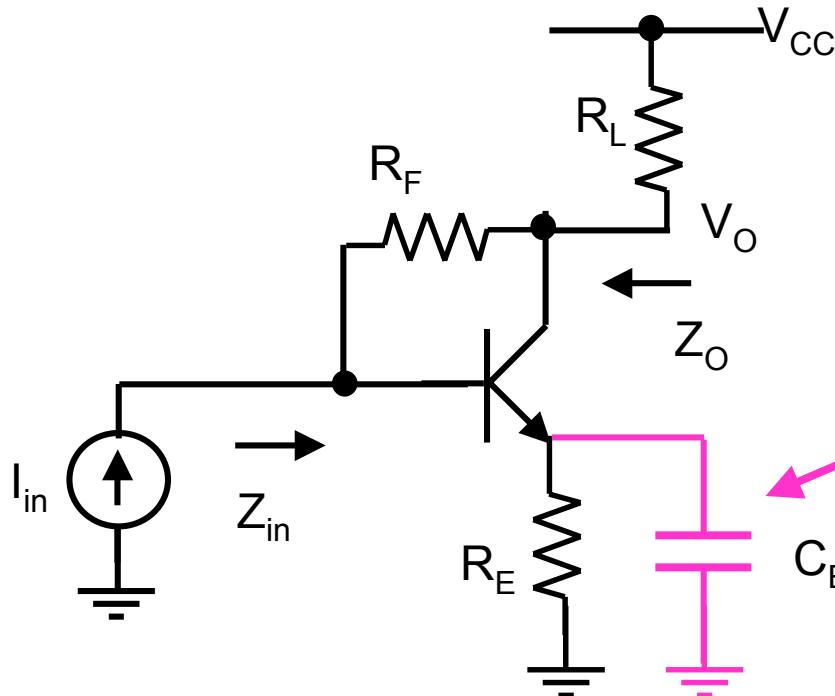
Transient response is poorer even though bandwidth has improved.

Step Response



Ringing is significant

Emitter zero peaking: TIA 3



Another classic scheme
for bandwidth, risetime
enhancement

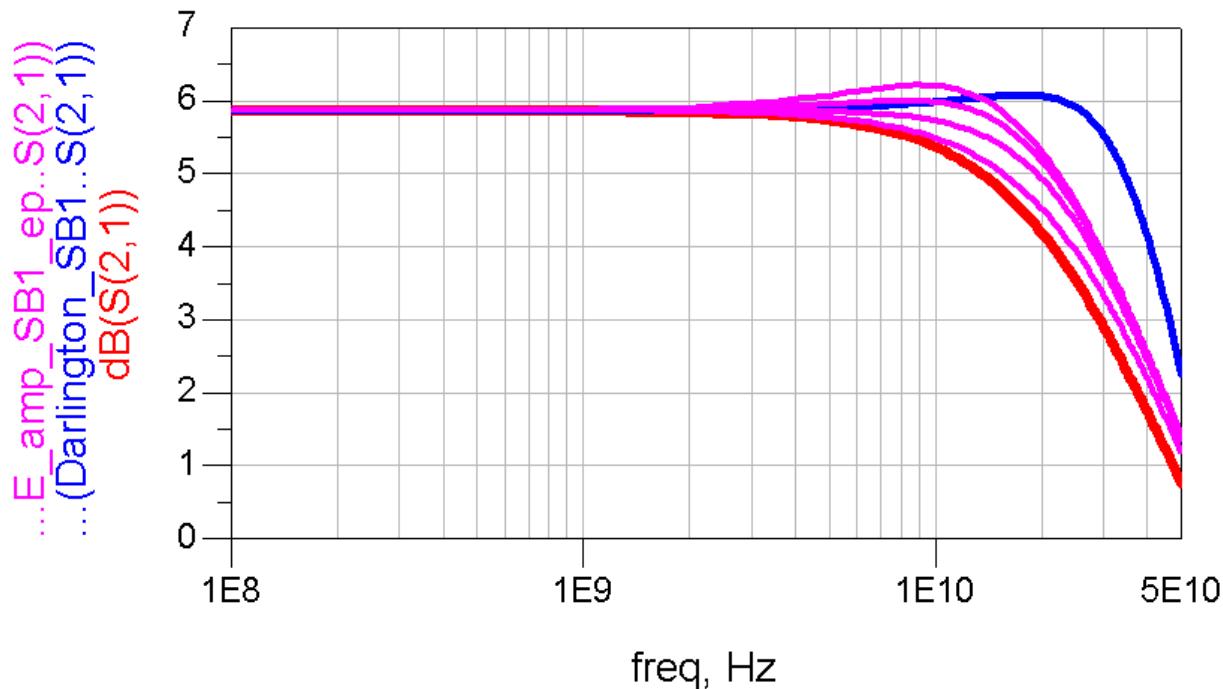
Zero added at $s = 1/R_E C_E$

Improve bandwidth/risetime
by compensating for pole

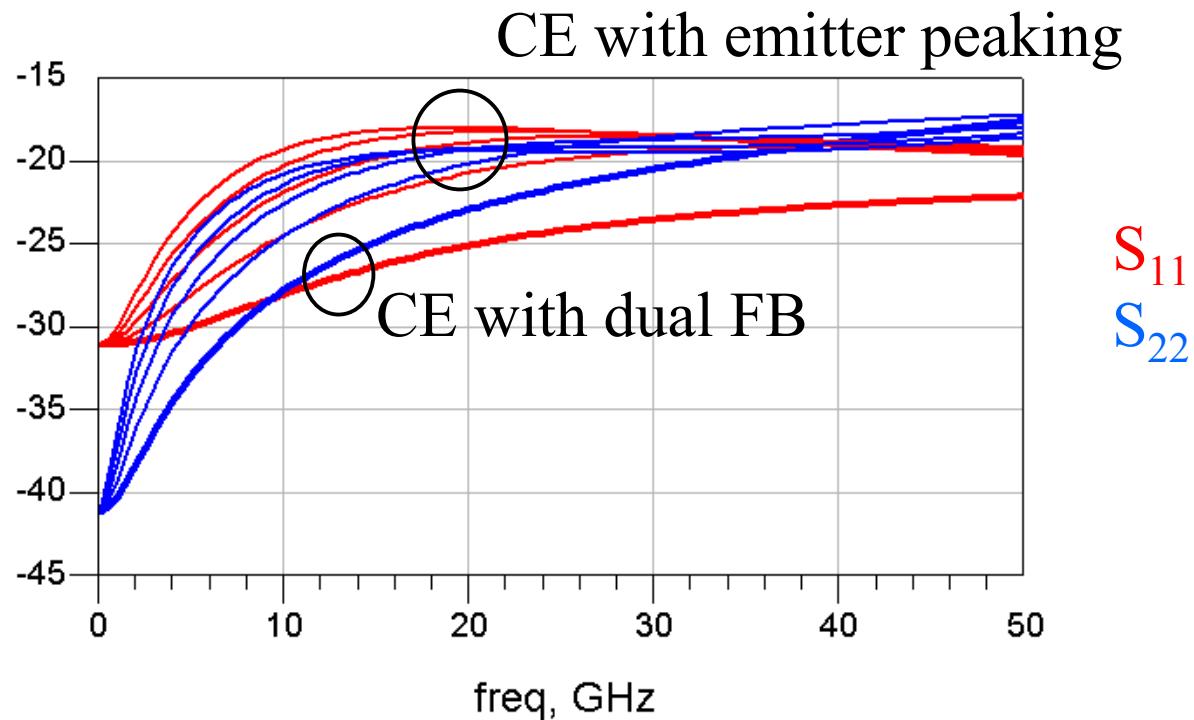
Works best when $p_2 \gg p_1$

Ref. 4.11

CE with dual FB	30 GHz
Darlington	45 GHz
CE with emitter peaking	37 GHz



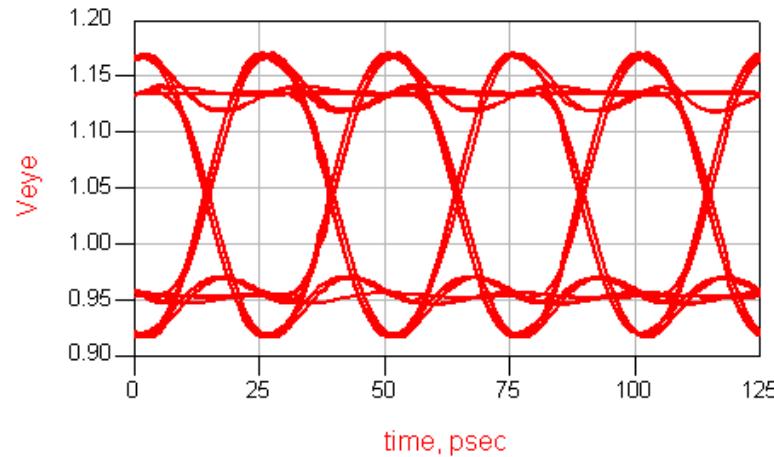
- Bandwidth improves with increasing CE
- Avoid excessive gain peaking



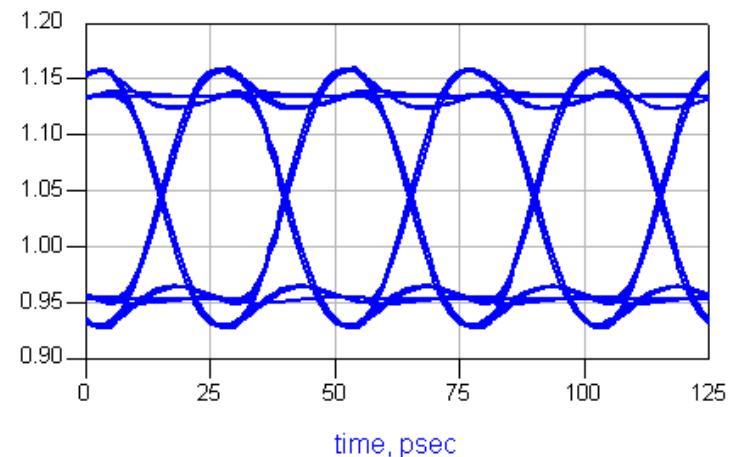
S_{11} , S_{22} degraded slightly by emitter peaking, BUT ...

Transient response at 40 Gb/s is better
than Darlington –
But, not as good as simple CE with FB

CE with emitter peaking
TIA 1



CE with dual FB
TIA 3



Preliminary conclusions:

- Each stage introduces extra poles
 - Can reduce phase margin due to higher order poles
- Careful design can improve BW, but
- 3 dB BW can be improved while degrading transient response
- Photodiode and interconnection model must be included

How do we analyze the TIA?

- Necessary conditions for the transfer function
 - Neglect higher than second-order terms
 - No complex-conjugate pole pairs
- Estimate pole frequencies with time constants

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{1 + a_1 s + a_2 s^2}$$

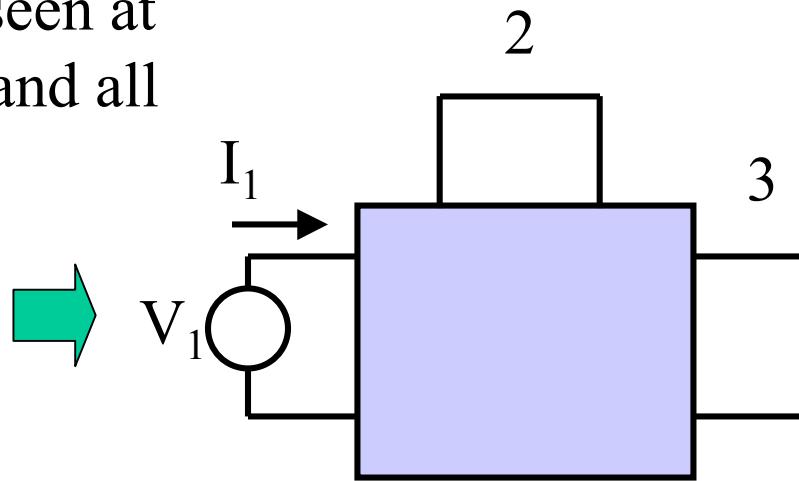
$$a_1 = \sum_{i=1}^n R_{ii}^o C_i \quad (\text{as before} - \text{approximates dominant pole})$$

n = number of capacitors

a_2 can be estimated

Define R_{ii}^j as the resistance seen at port i when port j is shorted and all other ports open.

Here is an example of R_{11}^2



a_2 is the sum of products of short circuit and open circuit time constants associated with all possible pairs of capacitors.

For a 3 capacitor network, a_2 is

$$a_2 = R_{11}^o C_1 R_{22}^1 C_2 + R_{11}^o C_1 R_{33}^1 C_3 + R_{22}^o C_2 R_{33}^2 C_3$$

Ref. 6.2

Note that the first time constant is an OCTC that has already been calculated.

In addition, for any pair of capacitors, we can find an OCTC for one and a SCTC for the other. The order does not matter.

$$R_{ii}^o C_i R_{jj}^i C_j = R_{jj}^o C_j R_{ii}^j C_i$$

The second pole frequency can be estimated by the separated pole approximation:

$$\frac{V_o(s)}{V_i(s)} = \frac{k}{(1 + a_1 s)(1 + a_2 s / a_1)}$$

Here we assume that the a_3 and higher terms are small and $a_1 \gg a_2/a_1$ – or use quadratic formula to find poles.

So, how does this help?

- If we know a_1 and a_2 , we can estimate
 - Bandwidth
 - Gain peaking
 - Risetime
 - Overshoot and ringing frequency
 - And, most important, we can see what must be changed to avoid transient response problems!

Rewrite the denominator in a standard notation:

$$1 + a_1 s + a_2 s^2 = 1 + \frac{2\zeta s}{\omega_n} + \frac{s^2}{\omega_n}$$

Natural frequency: $\omega_n = a_2^{-1/2}$

Damping factor: $\zeta = \frac{a_1 \omega_n}{2}$

Good pulse response requires $\zeta > 1$. This prevents complex poles
BW, peaking, ringing, etc. all can be estimated from these 2
factors. (see appendix for a table)

Conclusions

- Both frequency and time domain responses can be improved by careful analysis and design
- Simulation complements, not replaces, analytical methods

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To our son, Jonathan Benedikt

In memoriam, Oliver Winterer (1970–2006)

Preface

Electronic RF-communication and sensing systems have dramatically changed our daily lives since the invention of the first electronic transistor in 1947. Advanced semiconductor devices are key components within electronic systems and ultimately determine their performance. In this never ending challenge, wide-bandgap nitride semiconductors and heterostructure devices are unique contenders for future leading-edge electronic systems due to their outstanding material properties with respect to speed, power, efficiency, linearity, and robustness. At the same time, their material properties are challenging compared with any other material system due to high growth temperatures and many other intrinsic properties.

Wide bandgap semiconductors have attracted a lot of attention in the last ten years due to their use in optoelectronic and electronic applications. The field is developing rapidly due to the high investments in US, Japanese, and increasing European research and development activities. Some of the knowledge acquired may not be available to the general public because of military or civil restrictions. However, this work compiles and systemizes the available knowledge and evaluates remaining issues. This book is of interest to graduate students of electrical engineering, communication engineering, and physics; to material, device, and circuit engineers in research and industry; and to scientists with general interest in advanced electronics.

The author specially thanks those people, without whom and without whose individual contributions such a challenging work would have been impossible. He owes special thanks to:

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VIII Preface

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List of Symbols

Δ	Step, difference, change
$\Delta E_V, \Delta E_C$	Discontinuity of the valence/conduction band at a heterointerface
ΔE_g	Total difference of the bandgaps at a heterointerface
Δf	Frequency interval
ΔV	Voltage drop over the depletion zone
$\Theta(T_0)$	Temperature-dependent thermal resistance
α, β, γ	General exponent
α	General temperature coefficient
α	Common base current gain
α_a, α_c	Coefficients of thermal expansion along <i>a</i> - and <i>c</i> -axis
α_{AB}	Temperature exponent of the ternary A_xB_{1-x}
α_H	Hooge parameter
α_n, α_p	Impact ionization parameter for electrons and holes
α_n	Fitting parameter in the LS-model
α_T	Base transmission factor
α_S	Fitting parameter in the LS-model
β	Common emitter current gain in bipolar devices
γ_i	Emitter injection efficiency
δ	The base recombination factor
ε	Permittivity
ϵ_{ij}	Dielectric tensor components
ϵ_0	Dielectric constant
ε_r	Relative permittivity

XVIII List of Symbols

$\varepsilon_r^{\text{eff}}$	Effective permittivity
$\varepsilon_r^{\text{inf}}$	Relative permittivity for $\omega \rightarrow \infty$
η_d	Drain efficiency
κ_L	Lattice thermal conductivity
$\kappa_L(T)$	Thermal conductivity as a function of temperature
κ_{300}^A	Thermal conductivity at 300 K of material A
λ_n	Fitting parameter in the LS-model
μ_ν	Mobility of carrier type ν
μ_{AB}	Mobility of the ternary semiconductor $A_xB_{1-x}N$
τ	Phase term of the transconductance g_m
τ_{thermal}	Thermal time constant
ϕ_B	Schottky barrier potential
ψ	Electrostatic potential
ψ_i	Polynomials of the potential
ρ_s	Semiconductor resistivity
ρ_c	Metal resistivity
σ_B	Total interface charge at the boundary
$\sigma_{B,\text{SP}}$	Interface charge due to spontaneous polarization
$\sigma_{B,\text{PZ}}$	Interface charge due to piezoelectric polarization
σ_A	Electric drift-region-conductance per unit area in the semiconductor
τ_D	The delay due to the extension of the depletion zone to the drain
τ	Small-signal phase constant
τ_{RC}	Channel-charge RC-delay
τ_T	Total delay
τ_e, τ_b, τ_c	Emitter, base, collector delay
τ_{TR}	Transistor delay
τ_{thermal}	Thermal time constant
ω	Oscillation frequency
A	Area
A_R	Richardson constant
A_1, \dots, A_n	General coefficient
A_ν	Coefficient for impact ionization for carrier $\nu = n, p$
B	Direct radiative recombination parameter
B_0	Bulk modulus
BV_{CEO}	Open collector-emitter breakdown voltage

BV_{DS}	Drain–source breakdown voltage
$BV_{DS\ RF}$	RF drain–source breakdown voltage
BV_{GD}	Gate–drain diode breakdown voltage
BV_{GS}	Gate–source diode breakdown voltage
C	Correlation parameter
C	Capacitance in the passive model
C_{ij}	Elastic constants index i, j
C_{th}	Thermal capacitance
C_{ds}	Drain–source capacitance
C_g	Gate capacitance
C_{gd}	Gate–drain capacitance
C_{gs}	Gate–source capacitance
C_{jc}	Collector junction capacitance
C_{je}	Emitter junction capacitance
$C_{\text{pds}}, C_{\text{pgs}}, C_{\text{pgd}}$	Parasitic drain–source, gate–source, and gate–drain capacitances
$C_{gs,0}, C_{gd,0}$	Large-signal charge modeling coefficients
C_0	Static capacitance
C_{ss}	Parasitic capacitance in the dispersion model
C_{th}	Thermal capacitance
D_{nB}, D_{pE}	Diffusivity of electrons in the base, holes in the emitter
E	Local electric field
E_A	Acceptor energy
E_a	Activation energy
E_{break}	Breakdown field
E_{crit}	Critical field
E_C	Conduction band energy
$E_F(x)$	Fermi energy at position x
E_{f1}	Fermi-level correction energy
E_g	Bandgap energy
$E_{g,\Gamma}$	Bandgap energy in the Γ -valley
$E_{g,\Gamma_1}, E_{g,\Gamma_3}$	Bandgap energy in the Γ_1, Γ_3 -valley
$E_{g,G-A}$	Bandgap energy in the G–A valley
$E_{g,L}$	Bandgap energy in the L-valley
$E_{g,L-M}$	Bandgap energy in the L–M valley
$E_{g,X}$	Bandgap energy in the X-valley
$E_{g,0}$	Bandgap energy at $T_L = 0$ K
E_V	Valence band energy
G	Conductance in the passive model
G_{ass}	Associated gain
G_p	Power gain
$G_{m,2}, G_{m,d}, G_{m,2,d}$	Current parameters in Volterra approach
H	Hardness

XX List of Symbols

I_0	Current parameter in the diode equation
I_0	Current at time t=0
I_B, I_C, I_E	Base, collector, and emitter currents
I_D	Drain current
$I_{D\max}, I_{D\min}$	Maximum, minimum drain current
$I_{D\max,RF}, I_{D\min,RF}$	Maximum/minimum RF-drain current
I_{DS}	Drain-source current
I_{DPP}	Peak-to-peak drain current
I_{Dsat}	saturated drain current
I_{DSn}, I_{DSP}	Drain-source current in the LS-modeling
I_{Dq}	Quiescent drain current
I_{DSS}	Saturated drain current, typically at $V_{GS} = 0 \text{ V}$
I_G	Gate current
II_3	Ratio of input intermodulation 3rd order
IM_3	Intermodulation distortion ratio 3rd order
IMD_3	Intermodulation distortion 3rd order
I_{ij}	Current at port with index i,j
I_{opt}	Drain current optimized for noise figure
I_{pk}, I_{pk0}	Peak current parameter in LS-model
K_{bg}	Dispersion parameter in the LS-model
K_{trg}	Soft-breakdown pinch-off parameter
K_C	Fracture toughness
L	Channel length
L	Line inductance in the passive model
L_e	Emitter length
L_D, L_G, L_S	Drain, gate, and source inductances
L_D	Length of the depletion zone
L_{sb}	Soft breakdown function
L_{sb0}	LS-parameter for the soft-breakdown
L_{sd1}	Auxiliary function
MAG	Maximum available gain
M_C	Number of equivalent minima at the conduction band
MSG	Maximum stable gain
$MTBF$	Median time before failure
$MTTF$	Median time to failure
N_A	Acceptor doping concentration
N_B	Base carrier concentrations
N_C	Effective density of states of the conduction band
N_D	Donor doping concentration
N_{DC}	Donor doping concentration in the collector

N_E	Emitter carrier concentration
N_F	Noise figure
$N_{F,\min}$	Minimum noise figure at optimum impedance
N_T	Concentration of traps
N_V	Effective density of states of the valence band
OIP_3	Output intercept point third order
P_i	Function in the charge model
PAE	Power-added-efficiency
$P_{-1\text{dB}}$	Output power at 1 dB compression
P_{DC}	DC-power
P_{diss}	Dissipated power
P_{in}	Input power
P_{ij}	Large-signal parameter for the pinch-off voltage
P_{out}	Output power
P_{SP}	Spontaneous polarization
P_{PZ}	Piezoelectric polarization
P_{sat}	Saturated output power
R	Resistance
R_{Con}	Contact resistance
R_D	Drain resistance
$R_{D,\text{semi}}$	Semiconductor contribution to R_D
R_L	Load resistance/impedance
$R_{S,\text{met}}, R_{D,\text{met}}$	Metal contribution to R_S and R_D
R_S, R_G, R_D	Parasitic source, gate, and drain resistances
R_S	Series resistance of diode
R_{band}	Band edge contribution to the source resistance R_S
R_{bb}	Base resistance
R_{chan}	Channel resistance
R_{ds}	Drain–source resistance
R_{gap}	Contribution of the contact gap to R_{bb}
R_{gd}, R_{gs}	Gate–drain/–source resistance
R_i	Input resistance
R_n	Equivalent noise resistance
R_{on}	On-resistance
R_{opt}	Optimum impedance
R_{spread}	Spread contribution to R_{bb}
R_{ss}	Parasitic output resistance in the dispersion model
R_{th}	Thermal resistance
S_{ij}	Scattering (S-) parameter, $i, j = 1, 2$

XXII List of Symbols

$S_\nu(f)$	Spectral noise density
T_{chan}	Channel temperature
T_{Debye}	Debye-temperature
$T_{\text{Drain}}, T_{\text{Gate}}$	Drain and gate noise-temperature
$T(E_x)$	Tunneling probability
T_L	Local lattice temperature
T_{sub}	Substrate temperature
T_0	Backside temperature in the LS-model
U	Unilateral gain
V_1	Variable in the Curtice model
$V_{\text{BE}}, V_{\text{CE}}, V_{\text{BC}}$	Base-emitter, collector-emitter, and collector-base voltages
$V_{\text{breakdown}}$	Breakdown voltage
$V_{\text{DS}}, V_{\text{GD}}, V_{\text{GS}}$	Drain-source, gate-drain, and gate-source voltages
$V_{\text{DS}0}, V_{\text{GS}0}$	Quiescent drain-source/gate-source voltage
$V_{\text{D,max,RF}}, V_{\text{D,min,RF}}$	Maximum/minimum RF- V_{DS} -voltage
$V_{\text{GS},X}$	Dispersion corrected V_{GS} -voltages
$V_{\text{GS},3}^{\text{psat}}, V_{\text{GS},3}^{\text{plin}}$	Linearity parameters
V_{bgate}	Breakdown parameter in the LS-model
V_{dgt}	Gate-drain voltage function
V_{kl}	Voltage at device port k,l
V_{knee}	Knee voltage
V_p	Pinch-off voltage
V_{p2}	Doping correction to the threshold voltage
V_{thr}	Threshold voltage
W	Wafer bow
W_e, W_{eb}	Emitter-(base) width
W_g	Gate width
X_{EB}, X_E	Thickness of the emitter, base
Y_{ij}	Y -parameter for $i, j = 1, 2$
Z_{ds}	Complex output conductance
Z_{ij}	Z -parameter for $i, j = 1, 2$
Z_0	Characteristic impedance
a, b, c, d, n	General parameters
$a_{\text{gate-lag}}, a_{\text{drain-lag}}$	Dispersion parameters for gate and drain-lag
$a_{\text{gate,cw}}, a_{\text{drain,cw}}$	Dispersion parameters comparing pulsed and cw
a_0, c_0	Lattice parameters
c_{300}	Heat capacity at 300 K
$c_{\text{L,AB}}$	Nonlinear coefficient of the thermal conductivity of the ternary semiconductor

d	Thickness, length
d_{AlGaN}	Thickness of AlGaN
d_{eff}	Effective gate-to-channel separation
d_{doping}	Channel layer thickness
d_{sub}	Substrate diameter
e_{ij}	Piezoelectric coefficient
f_T	Current gain cut-off frequency
$f_{T,\text{ext}}$	Extrinsic current gain cut-off frequency
f	Frequency
f_c	Frequency for $k = 1$
f_c	Lattice mismatch
f_{\max}	Maximum frequency of oscillation
$f_{10 \text{ dB}}$	Maximum frequency which leaves 10 dB of power gain
$f(t, \mu, \sigma)_{\text{lognorm}}$	Log-normal distribution function
$f(t, \mu, \sigma)_{\text{norm}}$	Normal distribution function
f_1, f_2	Distribution function
g_{ds}	Output conductance
$g'_{\text{ds}} \text{ m } g''_{\text{ds}}$	Derivatives of output conductance
$g_{\text{ds,ext}}$	Extrinsic output conductance
$g_{\text{ds,ext}}(\text{CW(RF or Pulsed)})$	Extrinsic output conductance for CW, RF, or pulsed operation
g_m	(Complex) transconductance
g'_m, g''_m	Derivatives of transconductance
g_{mi}	Intrinsic transconductance
$g_{\text{m,max}}$	Maximum transconductance
\hbar, \hbar	(Reduced) Planck constant
h_{21}	Current-gain
$h(t)$	Thermal response function in the time domain
i_{ds}	Intrinsic drain source current
i_{II}	Impact ionization current in the LS-model
i_d, i_g	Noise current at drain and gate
k_B	Boltzmann constant
k_f	Fukui factor
$k_n, k_{\text{rel},n}$	Drain-lag dispersion model parameters
k	Stability factor
$l_{\text{fps}}, l_{\text{fpd}}$	Field-plate extension to the source and drain side
$l_{\text{gd}}, l_{\text{gs}}$	Gate-to-drain/-to-source separation
l_{gg}	Gate-to-gate pitch
l_g	Gate length
mb	Doping coefficient
m_e	Free electron mass

XXIV List of Symbols

m_n	Effective electron mass
$m_n(\Gamma\text{-K}), m_n(\Gamma\text{-A}),$	Effective electron mass at the $\Gamma\text{-K/A/M}$ transition
$m_n(\Gamma\text{-M})$	
$m_n(\text{X})$	Effective electron mass in X-valley
$m_{\nu,\text{AB}}$	Effective carrier mass of the semi-conductor $\text{A}_x\text{B}_{1-x}\text{N}$
$m_{n,\text{l}}$	Longitudinal electron mass
$m_{n,\text{t}}$	Transversal electron mass
m_p	Effective hole mass
$m_{p,\text{h}}$	Effective heavy hole mass
$m_{p,\text{l}}$	Light hole mass
$m_{p,\text{so}}$	Spin-orbit hole mass
m^*	Tunneling mass
\mathbf{n}	A normal vector
n	Electron concentration
n	Ideality factor
n	Refractive index
n_{channel}	Channel charge density
n_i	Intrinsic carrier concentration
n_{sheet}	Sheet carrier concentration
p	Hole concentration
q	Elementary charge
$q_{\text{bulk,traps}}$	Charge of bulk traps
q_{channel}	Channel charge
$q_{\text{diel,interface}}$	Interface charge
q_{doping}	Doping charge
q_{initial}	Dynamic charge
$q_{\text{semi,interfaces}}$	Charge at the semiconductor interfaces
t	Time
t	Thickness of the current-supporting layer
t_{ad}	Thickness of the adhesive
t_{sem}	Semiconductor thickness
t_{sub}	Substrate thickness
t_{subm}	Submount thickness
$\bar{v}_{\text{ds}}, \bar{v}_{\text{gs}}$	Static voltage components in dispersion model
v_{ds}, v_d	Intrinsic drain (source) voltage
v_{eff}	Effective carrier velocity
v_{gs}, v_g	Intrinsic gate (source) voltage
v_{peak}	Peak carrier velocity
v_{sat}	Saturated carrier velocity
x, y	Material composition parameter
y	Distance

List of Acronyms

2DEG	Two-Dimensional Electron Gas
3G	3rd generation (of mobile communication)
4G	4th generation (of mobile communication)
4H, 6H	Polytypes of SiC
AC	Alternating Current
ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
AFM	Atomic Force Microscopy
AlN	Aluminum nitride
AESA	Active Electronically Scanned Array
ASIC	Application Specific Integrated Circuit
BCB	Bencocyclobutene
BEEM	Ballistic Electron Emission Spectroscopy
BGA	Ball-Grid-Array
BJT	Bipolar Junction Transistor
BN	Boron Nitride
BS	Backside Cooling
BV	Breakdown Voltage
CAD	Computer Aided Design
CAFM	Conductive Atomic Force Microscopy
CAIBE	Chemically-Assisted Ion Beam Etching
CAT-CVD	Catalytic Chemical Vapor Deposition
CAVET	Current Aperture Vertical Electron Transistor
CDMA	Code Division Multiple Access
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
CW	Continuous Wave

c	cubic
DBF	Digital Beam-Forming
DC	Direct Current
DD	Drift-Diffusion
DLT(F)S	Deep Level Transient (Fourier) Spectroscopy
DHBT	Double Heterojunction Bipolar Transistor
DHFET	Double Heterojunction Field Effect Transistor
DHHEMT	Double Heterojunction High Electron Mobility Transistor
DOD	U.S. Department of Defense
DPD	Digital Predistortion
DRA	Driver Amplifier
EBIC	Electron-Beam Induced Current
ECR	Electron Cyclotron Resonance
ECMP	Electrochemical-Mechanical Polishing
EDGE	Enhanced Data Rates for GSM Evolution
EDX	Electron Diffraction
EER	Envelope Elimination and Restoration
ELO, ELOG, LEO	Epitaxial Lateral Overgrowth
ESD	Electrostatic Discharge
ET	Envelope-Tracking
EUV	Extreme Ultraviolet
EVM	Error Vector Magnitude
FC	Flip-Chip
FET	Field Effect Transistor
FIB	Focussed Ion Beam
FIT	Failures in Time
FOM	Figure-Of-Merit
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GCPW	Grounded Coplanar-Waveguide
GSM	Global System for Mobile Communications
HBT	Heterojunction Bipolar Transistor
HCI	Hot Carrier Injection
HEMT	High Electron Mobility Transistor
HFET	Heterostructure Field Effect Transistor
HPA	High-Power Amplifier
HPSI	High-Purity Semi-Insulating (substrates)
HR	High-Resistivity
HTCC	High-Temperature Cofired Ceramics
HTCVD	High-Temperature Chemical Vapor Deposition
HVPE	Hydride Vapor Phase Epitaxy
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IDLDMOS	Interdigitated-Drain LDMOS

IF	Intermediate Frequency
II	Impact Ionization
IMPATT	IMPact Avalanche Transit Time
InAlN	Indium Aluminum Nitride
InAs	Indium Arsenide
InGaN	Indium Gallium Nitride
InN	Indium Nitride
JFET	Junction Field-Effect Transistor
LDMOS	Laterally diffused MOS
LED	Light-emitting Diode
LEEN	Low-Energy Electron-Excited Nanoscale Luminescence Spectroscopy
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPCVD	Low-Pressure Chemical Vapor Deposition
LT	Low-Temperature
LTCC	Low-Temperature Cofired Ceramics
MAG	Maximum Available Gain
MBE	Molecular Beam Epitaxy
MC	Monte Carlo
MCM	Multi-Chip Module
MEMS	Micro-Electro-Mechanical Systems
MERFS	Micro Electromagnetic Radio Frequency System
MESFET	MEtal Semiconductor Field Effect Transistor
MHEMT	Metamorphic HEMT
MIC	Microwave Integrated Circuit
MIM	Metal–Insulator–Metal
MISFET	Metal Insulator Field Effect Transistor
MISHEMT	Metal Insulator Semiconductor HEMT
MMIC	Monolithic Microwave Integrated Circuit
MOCVD	Metal Organic Chemical Vapor Deposition
MOD	Ministry of Defense
MODFET	Modulation-Doped FET
MOMBE	Metal Organic Molecular Beam Epitaxy
MOS	Metal–Oxide–Semiconductor
MOSFET	Metal–Oxide–Semiconductor FET
MOSDHFET	Metal–Oxide Double Heterostructure FET
MOVPE	Metal Organic Vapor Phase Epitaxy
MSG	Maximum Stable Gain
MSL	Microstrip Line
MTBF	Mean Time Before Failure
MTTF	Mean Time to Failure
NBTI	Negative Bias Temperature Instability
NID	Non-Intentionally Doped
NiCr	Nickel Chromium

XXVIII List of Acronyms

OFDM	Orthogonal Frequency-Division Multiplexing
ONO	Oxide–Nitride–Oxide
PA	Power Amplifier
PAE	Power-Added Efficiency
PAMBE	Plasma-Assisted Molecular Beam Epitaxy
PAR	Peak-to-Average Ratio
PAS	Positron Annihilation Spectroscopy
PCB	Printed Circuit Board
PCDE	Peak Code Domain Error
PEC	Photo-enhanced Electrochemical Etching
PECVD	Plasma-enhanced Chemical Vapor Deposition
PHEMT	Pseudomorphic HEMT
PIC	Polarization-Induced Charge
PL	Photoluminescence
PLM	Polarized Light Microscopy
PVT	Physical Vapor Deposition
RF	Radio Frequency
RIE	Reactive Ion Etching
RMS	Root-Mean Square
RTA	Rapid Thermal Annealing
Rx	Receiver
SAR	Synthetic Aperture Radar
SAW	Surface Acoustic Wave
SEM	Scanning Electron Microscopy
SH	Self-Heating
SHBT	Single Heterojunction Bipolar Transistor
SHFET	Single Heterojunction Field Effect Transistor
SHHEMT	Single Heterojunction High Electron Mobility Transistor
s.i., SI	Semi-Insulating
SiC	Silicon Carbide
SiCOI	Silicon Carbide on Insulator
SiCoSiC	Silicon Carbide on polySiC
SIMS	Secondary Ion Mass Spectroscopy
SiN	Silicon Nitride
SIP	System-In-Package
SIT	Static Induction Transistor
SKPM	Scanning Kelvin Probe Microscopy
SMD	Surface Mount Device
SoC	System on a Chip
SOI	Silicon On Insulator
SopSiC	Silicon on poly-crystalline SiC
SPDT	Single Pole Double Throw
SRPES	Synchrotron Radiation Photoemission Spectroscopy

SRH	Shockley–Read–Hall
SSPA	Solid-State Power Amplifier
STEM	Scanning Tunneling Electron Microscopy
TaN	Tantalum Nitride
TDD	Threading-Dislocation Density
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TLM	Transmission-Line Model
TMGa, TMAl, TMIn	TrimethylGallium, TriMethylAluminum, TriMethylIndium
T/R,TRX	Transmit/Receive
TWA	Traveling Wave Amplifier
TWTA	Traveling Wave Tube Amplifier
UWB	Ultra-Wide Band
VCO	Voltage-Controlled Oscillator
WBG	Wide BandGap
WBS	Wide Bandgap Semiconductor
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide interoperability For Microwave Access
Wz	Wurtzite
XRD	X-Ray Diffraction
Zb	Zincblende

Introduction

This monograph is devoted to the development of III-N semiconductor-based electronics for high-power and high-speed RF-applications. Material properties of these polar materials, the state-of-the-art of substrates, epitaxial growth, device and processing technology, modeling, and circuit integration, and examples are discussed. A full chapter is devoted to the critical aspect of device reliability. The work concludes with integration and packaging aspects specific to the new properties of III-N-based-circuits and subsystems.

In the second chapter, general material and transport properties, advantages, and theoretical electrical and thermal limits are presented. Further, the state-of-the-art for nitride-based substrates, materials, electronic devices, and circuits are reviewed systematically.

For epitaxial growth, both the aluminum and indium-based binary and ternary compounds are described with emphasis on AlGaN/GaN and In–Ga–N-based heterostructure systems in Chapter 3. Epitaxial growth techniques such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) are analyzed systematically. Nitride-specific material characterization, doping, and material quality issues are analyzed. Substrate properties are reviewed systematically with respect to electronic requirements.

Currently a major focus of development is devoted to high electron mobility transistors (HEMTs) with gate lengths down to 30 nm and cut-off frequencies up to 190 GHz. Thus, for this class of devices, specific field-effect transistor problems such as Schottky and ohmic contacts, and lithography of optically transparent materials are discussed. State-of-the art recess processes and passivation technologies are analyzed. Bipolar device technology issues are reviewed.

In the device modeling and characterization Chapter 5, DC, small-signal, and noise characterization and modeling are presented with respect to nitride-specific questions. As frequency dispersion is a major source of performance and device degradation, the characterization and reduction of dispersion involving pulsed-characterization and other advanced techniques are dis-

cussed. Large-signal characterization and modeling are discussed for nitride devices, including the modeling of contacts, diodes, dispersion, and thermal aspects.

Chapter 6 discusses circuit examples for high-power RF amplifiers with a focus on increased impedance, thermal management, and high RF-power management between 0.5 and 100 GHz. Low-noise amplifiers are presented and analyzed for high-dynamic range, robustness, and high linearity. The last section of the chapter treats other circuits functions such as mixers and oscillators. Again, nitride-specific advantages and challenges are investigated.

In Chapter 7, nitride-specific device and circuit reliability issues and device failure mechanisms are analyzed and described systematically. The last chapter describes integration and packaging considerations, thermal-mounting and thermal-packaging considerations, for state-of-the-art amplifiers, and subsystems.

III-N Materials, and the State-of-the-Art of Devices and Circuits

In this chapter, general material and transport properties, advantages, and theoretical electrical and thermal limits of nitride semiconductors are presented with respect to electronic applications. This chapter further provides an overview of substrate materials. The state-of-the-art for nitride-based materials, electronic devices, and circuits are reviewed systematically. The last section defines application-specific requirements on nitride semiconductor devices from a more system oriented point of view. The chapter concludes with a number of problems.

2.1 State-of-the-Art of Materials Research

A systematic overview of the material properties is given in the following. For a systematic introduction, Fig. 2.1 depicts the bandgap at a lattice temperature of 300 K for various semiconductor materials as a function of lattice constant. The selection of the specific material constant as lattice constant in noncentrosymmetric materials may be arbitrary, however, is useful for a systematic introduction. With the bandgap of InN recently suggested to be about 0.8 eV and the bandgap of AlN to be 6.2 eV at room temperature, the III-N material system covers a very broad range of energies and thus emission wave lengths from the infrared to the deep ultraviolet unchallenged by any other available material. Electronically, a very broad range of bandgap energies is found resulting in extremely high bulk material breakdown voltages, which can be traded in for low-effective mass and high mobility of GaN with $m_n = 0.2 m_e$, or even of InN with $m_n = 0.11 m_e$ (potentially even $m_n = 0.04 m_e$ [2.122]) by changing the material compositions in the heterostructures. At the same time, a second trade-off is imminent and different from any other semiconductor material system. Due to the strong polar material properties, the modification of the material composition results in dramatic modifications of the polar crystal properties, and thus of available

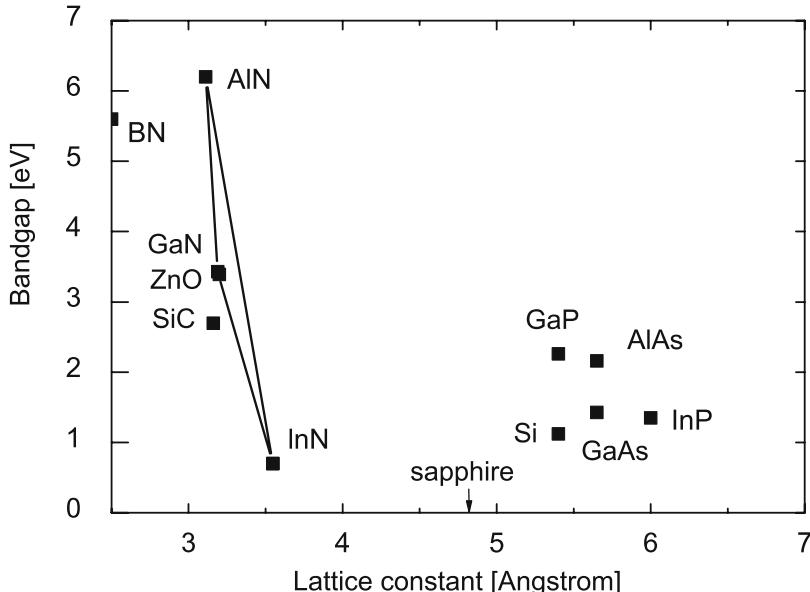


Fig. 2.1. Bandgap energy at $T_L = 300\text{ K}$ as a function of lattice constant of III-N semiconductors: Other III-V semiconductors are given for comparison

carrier concentrations obtained at the interfaces and thus available in the devices. Thus, and in some respect very similar to silicon, the huge success of III-N material is not mainly due to the intrinsic bulk material transport properties (especially the p-material properties do not compare well with n-properties in III-N materials), but due to the interface properties. In the case of silicon, the success is based on the formation of a native oxide which can be optimized and used tremendously, e.g., [2.411], and is recently replaced by other dielectrics, which also are well behaved on silicon, e.g., [2.136, 2.145].

In the case of III-N heterostructures, the interfaces allow for the formation of n-channels and intrinsically provide extremely high carrier concentrations $\geq 10^{13}\text{ cm}^{-2}$ through polarization engineering without further impurity doping. On the contrary, and unlike silicon, the semiconductor–dielectric interfaces remain a challenge in the III-N world, as suitable interfaces can be formed from a practical point of view, however, these interfaces and their long term behavior are not well understood mainly due to the high-sheet charge concentrations.

2.1.1 Binary Materials

The binaries of the elements Al–In–Ga–B–N are the basic materials for the semiconductor material class named Nitrides: gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), and boron nitride (BN). Epi-

taxially grown silicon nitride (SiN), although not of crystalline quality, may be added from time to time. Boron nitride (BN) is still relatively immature as a semiconductor material [2.99]. Initial results on the material and device level are available [2.99], featuring the especially good thermal conductivity of BN, second only to diamond when semiconductor materials are compared. Good overview papers and collections are available, with a focus also on optoelectronic and general material properties, and, e.g., in [2.100, 2.101, 2.244, 2.315, 2.324, 2.369, 2.389]. Laser diodes are particularly addressed in [2.323]. The properties of SiN and SiO₂ are reviewed, e.g., in [2.440].

Crystal Structures for Electronic Applications

The III-N semiconductors can be found in three common crystal structures:

- Wurtzite
- Zincblende
- Rock salt

At room temperature GaN, AlN, and InN are found in the wurtzite structure, while BN prevails mostly in the cubic structure. The zincblende structure can also be found for GaN and InN for thin films, while for AlN no stable zincblende phase has yet been detected [2.99]. However, this work addresses also some mostly theoretical work on Zb-AlN. The rock salt phase is of no importance to electronic devices so far. In the wurtzite structure the growth is typically performed along the *c*-axis. Recently, growth along the *m*-plane has been reported [2.61, 2.342], as the resulting nonpolar material has a positive influence on diodes efficiency in optoelectronics.

Gallium Nitride (GaN)

Gallium Nitride (GaN) is the basic material of this material class which is typically used for all device layers requiring fast carrier transport with a high breakdown voltage. GaN is used as the channel material in various FETs and also as the base material in AlGaN/GaN HBTs, e.g., [2.311]. Most of the ohmic contact layers in any device incorporate binary n-doped and p-doped GaN. GaN can further be grown as a semi-insulating material with growth parameters close to those of the semiconducting layers.

Mechanical and Optical Properties

The crystal structure and the mechanical and thermal properties of GaN are discussed in a number of publications, e.g., in [2.4, 2.244, 2.315, 2.389]. The data of all III-N binaries are also compiled in table form in the Appendix. As an initial quantity, Table 2.1 compiles the data on the mass density. The Vickers hardness and fracture toughness of bulk GaN in comparison to other semiconductors are given in [2.92]. More recent results are presented in [2.524]. Table 2.2 compares the values of the hardness *H* and fracture toughness *K_C*.

Table 2.1. Mass density of III-N and other semiconductor materials

Material	GaN	AlN	InN	BN	Si	Ref.
Mass density (g cm^{-3})	6.1	3.23	6.81	3.48	2.33	[2.17, 2.99, 2.443]

Wz wurtzite, *Zb* zincblende, *c* cubic, *d* diamond

Table 2.2. Vickers hardness H and fracture toughness K_C of III-N and other semiconductor materials

Material	GaN	AlN	InN	BN	SiC	Si	Ref.
H (GPa)	12	14	11.2	55–65	33	9	[2.92, 2.451]
K_C ($\text{MPa m}^{1/2}$)	0.8	2.6	—	—	3.3	0.7	[2.92, 2.244]

Table 2.3. Elastic constants of wurtzite III-N semiconductors and other materials

	GaN (Wz)	AlN (Wz)	InN (Wz)	BN (c)	Ref.
C_{11} (GPa)	390	396	223	831	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{33} (GPa)	398	373	200	—	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{44} (GPa)	105	116	48	450	[2.372, 2.451, 2.485]
C_{12} (GPa)	145	137	115	190	[2.99, 2.275, 2.372, 2.449, 2.485]
C_{13} (GPa)	106	108	92	—	[2.275, 2.372, 2.449, 2.485]

Wz wurtzite, *c* cubic

Table 2.4. Elastic constants of zincblende III-N semiconductors

	GaN (Zb)	AlN (Zb)	InN (Zb)	BN (c)	Si	Ref.
C_{11} (GPa)	293	304	187	820	165.8	[2.244, 2.371, 2.485]
C_{44} (GPa)	155	193	86	480	79.6	[2.244, 2.371, 2.485]
C_{12} (GPa)	159	160	125	190	63.9	[2.244, 2.371, 2.485]

Wz wurtzite, *Zb* zincblende, *c* cubic

Table 2.5. Coefficients of thermal expansion (CTE) of III-N semiconductors and other materials at room temperature

	GaN (Wz)	GaN (Sa)	AlN (p)	InN (p)	BN (c)	SiC	Sap.	Si	Ref.
α_a (10^{-6}K^{-1})	3.1	3.8	2.9	3.6	1.15	3.2	4.3	2.6	[2.99, 2.222, 2.243]
α_c (10^{-6}K^{-1})	2.8	2.9	3.4	2.6	—	3.2	3.2	2.6	[2.222, 2.243]

Wz wurtzite, *Sa* epitaxially on sapphire substrate, *c* cubic, *p* powder

c-BN is a particularly hard material, while GaN, AlN, and InN have nearly the same hardness. This hardness makes c-BN attractive in various ceramic materials. The elastic constants of wurtzite gallium nitride determined by Brillouin scattering are reported, for example, in [2.372] and are compiled in Table 2.3. A prediction of the high-temperature elastic constants of GaN, AlN, and InN is given in [2.381]. Deduced from this, a bulk modulus B_0 of GaN is found to be 210 GPa. For BN, a comparison of the different calculated and measured values is given in [2.99]. First principle calculations of the properties of zincblende AlN and GaN are given in [2.177]. The elastic constants of the zincblende phase are compiled in Table 2.4. The pressure dependence of the elastic constants of zincblende BN, AlN, GaN, and InN is analyzed in [2.178].

The linear coefficients of thermal expansion (CTE) at room temperature and at elevated temperatures are important for the growth. Those of wurtzite GaN have been measured between room temperature and $\geq 750\text{K}$ for both bulk GaN and epitaxial layers grown on sapphire, e.g., in [2.243]. The data are compiled in Table 2.5. Table 2.5 further compares the CTE of III-N semiconductors to silicon carbide and other typical substrates materials. The differences in CTE and its temperature dependence have a similar impact to layer growth of heterostructures as the lattice constants, as discussed in Chapter 3. The thermal conductivity of GaN was initially reported in [2.423] and many of the references date back to this publication. More recent measurements, especially as function of dislocation density in thin layers, can be found in [2.120, 2.216, 2.264] and are discussed later with respect to the modeling and the importance of the crystalline quality. The data are compiled in Table 2.16.

Dielectric Constants

Compiling the basic dielectric properties, Table 2.6 gives both the static and the high-frequency dielectric constants. The dielectric constant of GaN is slightly lower than in silicon and GaAs (not shown). InN has the highest values of the three binary materials.

Overviews of further optical functions of GaN such as the refractive index are given in [2.3, 2.298]. The absorption spectrum of GaN at room temperature and the absorption coefficient are presented in [2.64].

Table 2.6. Dielectric constants of III-N and other semiconductor materials

Material	GaN (Wz)	AlN (Wz)	InN (Wz)	GaN (Zb)	BN (c)	Si	Ref.
ε_r	9.5 \perp , 10.4 \parallel	8.5	15.3	9.5	7.1	11.9	[2.3, 2.64, 2.492]
$\varepsilon_r^{\text{inf}}$	5.5	4.77	8.4	5.35	4.5	–	[2.3, 2.64, 2.492]

Wz wurtzite, Zb zincblende, and c cubic

Basic Transport Properties

Electronic transport in GaN is mostly understood, but a number of issues remain for further research. These include, e.g., the maximum carrier velocity v_{peak} in bulk material and at heterointerfaces, which are discussed later. General electrical properties of GaN, as well as AlN and $\text{Al}_x\text{Ga}_{1-x}\text{N}$, are compiled in [2.123]. An early, but accurate estimate of the carrier concentration dependence of the bulk mobility in GaN, InN, and AlN using the variational method is given in [2.64]. Based on more recent data, a mobility and carrier vs. doping concentration analysis for wurtzite MOCVD-grown bulk GaN is provided in [2.259]. Both donor and acceptor concentrations in the order of 10^{17} cm^{-3} are extracted. A specific mobility model for bulk GaN including the dependence on the free electron concentration is given in [2.308]; however, newer experimental results require an update of the actual parameters.

Table 2.7. Comparison of the low-field mobility values in various III-N bulk and 2DEG materials

Material	n/p	T_L (K)	N_D/N_A (cm^{-3})	μ ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	Method	Ref.
GaN (Wz)	n	300	$N_D = 1 \times 10^{17}$	990	MC	[2.113]
GaN (Wz)	n	450	$N_D = 1 \times 10^{17}$	391	MC	[2.113]
GaN (Wz)	n	600	$N_D = 1 \times 10^{17}$	215	MC	[2.113]
GaN (Wz)	p	300	$N_A = 3.6 \times 10^{16}$	150	meas.	[2.123]
GaN (Wz)	n 2DEG	300	0	2,000	MC	[2.337]
GaN (Wz)	n	77	$N_D = 1 \times 10^{16}$	6,000	VP	[2.64]
GaN (Zb)	n	300	$N_D = 1 \times 10^{17}$	1,100	MC	[2.17]
GaN (Zb)	n 2DEG	300	0	2,100	MC	[2.337]
GaN (Zb)	p	300	$N_A = 1 \times 10^{13}$	350	meas.	[2.21]
AlN (Wz)	n	300	$N_D = 1 \times 10^{17}$	135	MC	[2.349]
AlN (Wz)	n	77	$N_D = 1 \times 10^{16}$	2,000	VP	[2.64]
AlN (Zb)	n	300	0	200	MC	[2.17]
AlN (Zb)	n	100	0	400	MC	[2.17]
InN (Wz)	n	300	$N_D = 1 \times 10^{17}$	3,000	MC	[2.35]
InN (Wz)	n	300	$N_D = 1.5 \times 10^{17}$	3,570	meas.	[2.114]
InN (Wz)	n	77	$N_D = 1 \times 10^{16}$	30,000	VP	[2.64]
InN (Zb)	n	100	$N_D = 1 \times 10^{17}$	9,000	MC	[2.17]
BN (c)	p	300	$N_A = 5 \times 10^{18}$	500	meas.	[2.253]

Wz wurtzite, Zb zincblende, c cubic, VP variational principle, MC Monte Carlo, meas. measured

Low-Field Mobility

Several predictions and measurements are available for obtaining estimates for the maximum low-field mobility in both bulk and 2DEG electron gas. Table 2.7 compiles the data of the low-field mobility with respect to temperature and impurity dependence of the mobility in III-N bulk materials. The maximum values from [2.64] are given for completely uncompensated material.

Recent advances in material growth show great improvements in channel mobility of optimized AlGaN/GaN 2DEG channel-layer material with Hall mobility values of up to $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [2.435] at room temperature in agreement with theoretical predictions [2.337]. For the analysis of the mobility in bulk and 2DEG-GaN, the temperature dependence is plotted in Fig. 2.2 taken from [2.37] and data therein. The effects to influence mobility include:

- Phonon scattering by acoustic and optical phonons
- Ionized impurity scattering [2.37] at both background impurities and surface donors
- Threading dislocations [2.258, 2.329, 2.435]
- Alloy scattering [2.34, 2.414]

The maximum drift mobility of wurtzite bulk GaN is about $1,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The hole mobility in bulk GaN is much lower with maximum values of $175 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The reduced impurity scattering in 2DEG channels at

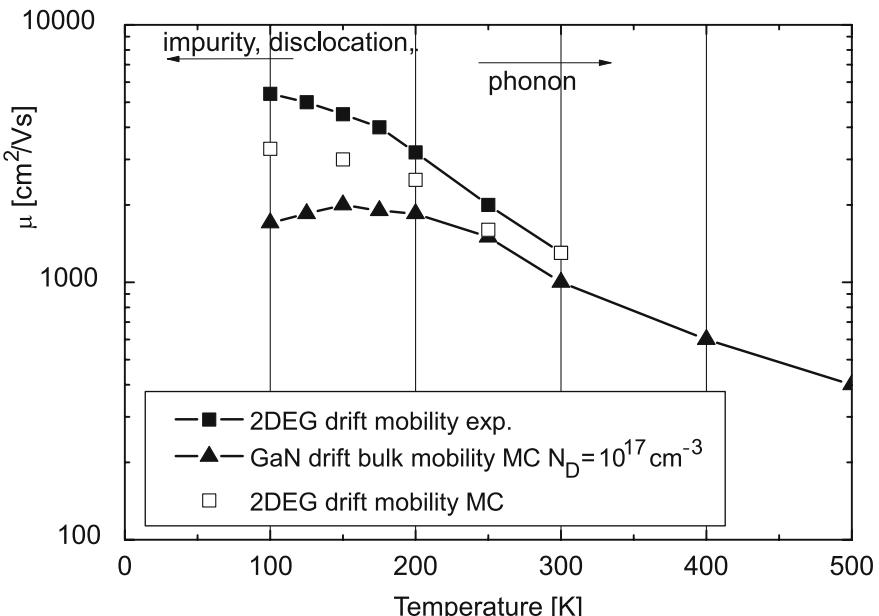


Fig. 2.2. Drift mobility as a function of lattice-temperature T_L for bulk GaN and 2DEG-GaN depicting the different limiting effects from [2.37, 2.329]

very low surface scattering levels yield 2DEG-mobility values of up to $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for both wurtzite and zincblende material. A theory of charged dislocation scattering in GaN is given [2.258]. The fit of the temperature-dependent Hall data can be correlated with the dislocations observed by TEM. The impact of threading dislocations on the transverse mobility in GaN is further discussed in [2.493]. The model explains the impact of trap occupancy and related scattering on the mobility at different doping levels. Alloy disorder is a limiting factor to transport at GaN heterointerfaces, as discussed in [2.414]. Further analysis is provided in Chapter 3. AlN is an insulator due to the high activation energy of the donors and the large bandgap. The theoretical low-field mobility of AlN is discussed in [2.17]. It is found to be phonon-limited with the electron mobility values given in Table 2.7. Theoretical values for the drift mobility of $135 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for fully uncompensated material have been found. Similar to InN, the hole transport properties of AlN are not understood very well. The predicted low-field drift mobility of InN at room temperature is found to be as high as $3,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in [2.35] and $3,700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in [2.17]. At 100 K, a maximum low-field mobility as high as $9,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is predicted for zincblende InN material [2.17]. Variational principle calculations leads to predictions of $30,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 77 K for completely uncompensated material at low impurity concentrations of 10^{16} cm^{-3} . Again, hole transport in InN is not well understood due to the lack of proper p-doping [2.170].

High-Field Transport

Several MC calculations of the velocity-field characteristics of wurtzite GaN considering the high-field transport are available and given, e.g., in [2.37, 2.121]. There is a significant discussion on the extraction of delay times in HFETs and resulting carrier velocities, which disagree with the MC calculations, see also Sect. 2.2.7. Table 2.8 compiles the bulk saturation velocity and critical field parameters from various sources. The comparison reveals the increase of both the saturation velocity v_{sat} and the critical field E_{crit} compared to other high-speed materials such as silicon, GaAs, and SiC. Peak velocity values as high as $3 \times 10^7 \text{ cm s}^{-1}$ are found for electrons in GaN. The differences between wurtzite and zincblende semiconductors are found to be insignificant. AlN has a very high critical field in agreement with the high bandgap energy, whereas the critical field of InN is lower than in GaN. The predicted electron peak velocity in InN can be as high as $4 \times 10^7 \text{ cm s}^{-1}$.

Apart from bulk material, MC simulations in 2DEG AlGaN/GaN channels including hot-phonon and degeneracy effects are provided in [2.380] by a combined MC and Schrödinger–Poisson analysis. The wavefunctions for the confined electrons are calculated. The simulation suggests that the degeneracy in the 2DEG reduces the electron drift velocity, while hot phonons reduce the drift velocity and increase the electron energy relaxation time. The energy relaxation time at RT extract by MC simulation amounts to

Table 2.8. Comparison of the velocity-field characteristics in various bulk materials

Material	n/p	T_L	E_{crit}	v_{peak}	v_{sat}	N_D/N_A	Ref.
		(K)	(kV cm $^{-1}$)	(10 7 cm s $^{-1}$)	(10 7 cm s $^{-1}$)	(cm $^{-3}$)	
GaN (Wz)	n	300	175	2.5	–	2×10^{16}	[2.500]
GaN (Wz)	n	300	150	2.7	2.5	1×10^{16}	[2.37]
GaN (Wz)	n	300	140	2.9	1.8	1×10^{17}	[2.121]
GaN (Wz)	n	77	150	3.2	2.7	1×10^{16}	[2.37]
GaN (Wz)	p	300	–	–	0.48	–	[2.286]
GaN (Zb)	n	300	145	2.6	1.34	1×10^{17}	[2.17]
GaN (Zb)	p	300	–	–	0.92	–	[2.286]
AlN (Wz)	n	300	450	1.7	1.4	1×10^{17}	[2.121, 2.349]
AlN (Wz)	n	300	447	2.3	2.16	1×10^{17}	[2.113]
AlN (Wz)	p	300	–	–	–	–	–
AlN (Zb)	n	300	550	1.8	1.59	1×10^{17}	[2.17]
AlN (Zb)	p	300	–	–	–	–	–
InN (Wz)	n	300	65	4.2	1.8	1×10^{17}	[2.121]
InN (Wz)	n	300	52	3.4	–	1×10^{17}	[2.113]
InN (Zb)	n	300	45	2.9	1.4	1×10^{17}	[2.17]
InN (Zb)	p	300	–	–	–	–	–

Wz wurtzite, Zb zincblende, c cubic

0.3 ps at 10 kV cm $^{-1}$ [2.380]. Experimental determination of the hot electron energy relaxation time in MBE-grown n-GaN is presented in [2.521]. The extracted value amounts to 0.2 ps at a carrier concentration of 10 18 cm $^{-3}$. Similar field-dependent investigations in AlGaN/GaN heterostructures based on microwave noise are given in [2.281]. RT data yields energy relaxation times of 0.3 ps at 10 kV cm $^{-1}$ and 1 ps at 2 kV cm $^{-1}$. The transient electron transport based on MC simulations in wurtzite GaN, InN, and AlN is discussed in [2.121]. In the transient situation very high theoretical overshoot values are observed. However, the paper also depicts the trade-off between transient overshoot and saturated velocity in bulk FET-like transient transport.

Band Structure of GaN

The band structure of GaN has been analyzed in a number of publications, e.g., in [2.108, 2.127, 2.128, 2.238, 2.522]. However, it is not yet fully understood, especially with respect to the higher energy bands. A comprehensive overview of the band parameters of wurtzite and zincblende GaN, AlN, and InN is given in [2.485] in a continuation of the great III-V overview in [2.486]. A consistent set of parameters is presented for both the wurtzite and zincblende binary III-N materials. From an experimental point of view, absorption coefficient,

energy gap, exciton binding energy, and recombination lifetime of Wz–GaN are measured and reported in [2.317]. From these both bandgap, exciton energies, and radiative constants can be derived.

Table 2.9 compiles available mass parameters from band structure calculations and measurements. Various predictions exist for the effective electron mass in GaN, e.g., in [2.128]. The conduction band electron effective mass in wurtzite GaN is measured to be $0.2 m_e$, as reported in [2.91]. The effective mass parameters are further collected from the band structure calculations in [2.127, 2.128, 2.238, 2.486]. The heavy hole masses $m_{p,h}$ are further distinguished along the x - and z -direction. The hole effective mass in p-GaN and the influence of band splitting and band anisotropy on free hole statistics

Table 2.9. Comparison of the effective mass parameters in various III-N semiconductor materials

	m_n (m_e)	$m_n(\Gamma - K)$ (m_e)	$m_n(\Gamma - A)$ (m_e)	$m_n(\Gamma - M)$ (m_e)	Ref.
GaN (Wz)	0.2	0.36	0.27	0.33	[2.91]
AlN (Wz)	0.48	0.42	0.33	0.40	[2.349]
InN (Wz)	0.11 (0.05)	–	–	–	[2.122, 2.486]
	$m_n(\Gamma)$ (m_e)	$m_{n,l}(X)$ (m_e)	$m_{n,t}(X)$ (m_e)	Ref.	
GaN (Zb)	0.15	0.5	0.30	[2.108, 2.485]	
AlN (Zb)	0.25	0.53	0.31	[2.108, 2.485]	
InN (Zb)	0.07–0.11	0.48	0.27	[2.485]	
	$m_{p,h}$ (m_e)	$m_{p,l}$ (m_e)	$m_{p,so}$ (m_e)	Ref.	
GaN (Wz)	1.4	0.3	0.6	[2.108, 2.244]	
AlN (Wz)	3.52 (z)	3.53 (z)	0.25 (z)	[2.108, 2.244]	
AlN (Wz)	10.42 (x)	0.24 (x)	3.81 (x)	[2.108, 2.244]	
InN (Wz)	1.63	0.27	0.65	[2.108, 2.244]	
	$m_{p,h}$ (m_e)	$m_{p,l}$ (m_e)	$m_{p,so}$ (m_e)	Ref.	
GaN (Zb) [100]	0.74	0.21	0.33	[2.108]	
GaN (Zb) [111]	1.82	0.18	0.33	[2.108]	
GaN (Zb) [110]	1.51	0.19	0.33	[2.108]	
AlN (Zb) [100]	1.02	0.35	0.51	[2.108]	
AlN (Zb) [111]	2.85	0.30	0.51	[2.108]	
AlN (Zb) [110]	2.16	0.31	0.51	[2.108]	

Wz wurtzite, Zb zincblende

in wurtzite GaN are discussed in [2.400]. The degeneracy effects are strong and require detailed investigations to obtain the effective hole mass at the particular density-of-states.

Bandgap Energies

The bandgap energy parameters of different crystal structures in III-N materials are compared in Table 2.10. Further, the intervalley separation energies in k-space are of practical importance for the high-field transport of electrons and holes. They are compiled in Table 2.11 for both wurtzite and zincblende structures. The uncertainty of the band structure and energy gap prevails specifically for AlN and InN for the higher bands.

The data of wurtzite GaN and AlN are based on the first principle calculations in [2.441] and the erratum [2.442]. At heterointerfaces between two semiconductors, the energy band discontinuities and bandgap alignments are of high importance, as they determine the energy barriers which the carriers have to surmount. All III-N materials lead to so-called type-I transitions. However, in conventional heterostructures, the alignments are symmetrical with respect to the growth order starting from the substrate. In highly polar semiconductors, such as the III-N material system, this is not necessarily the case, due to the strain effects depending on the substrate (bottom), and the resulting strain and thus polarization charge in the thin top layer. The valence band discontinuities for GaN, AlN, and InN have been complied, e.g., in [2.275]. The valence band alignment energies are found for the three binary materials, as given in Table 2.12. The additional transitions toward ternary material are also discussed later. BN is not included in this comparison, as the cubic phase BN cannot be grown lattice-matched to the other materials.

Table 2.10. Comparison of the bandgap parameters in various bulk materials at 300 K

	(Wz)	Ref.		(Zb)	Ref.
GaN $E_{g,\Gamma 1}$	(eV) 3.43	[2.121]	$E_{g,\Gamma}$	(eV) 3.38, 3.1, 3.2	[2.108]
GaN $E_{g,\Gamma 3}$	(eV) 5.29	[2.121]	$E_{g,X}$	(eV) 4.57, 4.7	[2.108]
GaN $E_{g,L-M}$	(eV) 5.49	[2.121]	$E_{g,L}$	(eV) 5.64, 6.2	[2.108]
AlN $E_{g,\Gamma 1}$	(eV) 6.2, 6.12	[2.121, 2.245]	$E_{g,\Gamma}$	(eV) 5.94, 6.0	[2.108]
AlN $E_{g,L-M}$	(eV) 6.9	[2.121]	$E_{g,X}$	(eV) 5.1, 4.9	[2.108]
AlN $E_{g,G-A}$	(eV) 7.2	[2.121]	$E_{g,L}$	(eV) 9.42, 9.3	[2.108]
InN $E_{g,\Gamma 1}$	(eV) 0.77	[2.501]	$E_{g,\Gamma}$	(eV) 0.75	[2.486]
InN $E_{g,G-A}$	(eV) 4.09	[2.121]	$E_{g,X}$	(eV) 2.486	[2.486]
InN $E_{g,\Gamma 3}$	(eV) 4.49	[2.121]	$E_{g,L}$	(eV) 5.79	[2.486]

Wz wurtzite, Zb zincblende

Table 2.11. Comparison of the intervalley separation energies in various bulk materials at 300 K

	(Wz)	Ref.		(Zb)	Ref.
GaN –	(eV) –	–	Γ	(eV) –	–
GaN $\Gamma - 3$	(eV) 1.9	[2.121]	$\Gamma - X$	(eV) 1.4	[2.17, 2.244]
GaN $L - M$	(eV) 2.1	[2.121]	$\Gamma - L$	(eV) 1.6–1.9	[2.244]
AlN Γ	(eV) –	–	–	(eV) –	–
AlN $\Gamma - (L - M)$	(eV) 0.7	[2.121, 2.441]	–	(eV) –	–
AlN $\Gamma - K$	(eV) 1.0	[2.121, 2.441]	–	(eV) –	–
InN –	(eV) –	–		(eV) –	–
InN $\Gamma - (M - L)$	(eV) 2.9–3.9	[2.244]		(eV) –	–
InN $\Gamma - A$	(eV) 0.7–2.7	[2.244]		(eV) –	–

Wz wurtzite, *Zb* zincblende

Table 2.12. Comparison of the bandgap alignment parameters in various bulk materials at 300 K

Top	Bottom	GaN	AlN	InN	Ref.
	(eV)	(Wz)	(Wz)	(Wz)	
GaN	(Wz)	0	0.7	1.05	[2.275]
AlN	(Wz)	0.7	0	1.81	[2.275]
InN	(Wz)	1.05	1.81	0	[2.275]

Top	Bottom	GaN	AlN	InN	Ref.
	(eV)	(Zb)	(Zb)	(Zb)	
GaN	(Zb)	0	0.85	0.51	[2.324]
AlN	(Zb)	0.85	0	1.09	[2.324]
InN	(Zb)	0.51	1.09	0	[2.324]

Wz wurtzite, *Zb* zincblende

Further empirical pseudopotential calculations of wurtzite GaN and InN are given in [2.522]. For the complete band structure, a nonlocal pseudopotential calculation of the III-nitride wurtzite phase materials system is performed in [2.128] for binary compounds such as GaN, AlN, and InN. Band structure calculations of wurtzite-type GaN and AlN are given in [2.298, 2.441]. Particularly the complicated valence band structure and the effective mass parameters of the wurtzite nitrides are obtained. The cubic approximation is found to be fairly successful in the analysis for the valence-band structures of the wurtzite-type nitrides.

Table 2.13. Comparison of the direct recombination parameters in various bulk materials at 300 K

	GaN (Wz)	AlN (Wz)	InN (Wz)
B ($\text{cm}^3 \text{s}^{-1}$)	1.1×10^{-8} [2.317]	0.4×10^{-10} [2.489]	2×10^{-10} [2.533]
Wz wurtzite			

The band structure in zincblende GaN, AlN, and AlGaN is described in [2.108]. Particularly, the energies of Γ , X , and L valley of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ as a function of mole fraction x of are calculated.

Table 2.13 gives the direct recombination parameters of the III-N semiconductors for the direct band structure. As can be derived, the direct recombination in GaN is very strong and about an order of magnitude higher than, e.g., in GaAs.

Aluminum Nitride (AlN)

Second to GaN, AlN is the most important binary material in the III-N material family for electronic applications and is mostly used as its ternary compound $\text{Al}_x\text{Ga}_{1-x}\text{N}$, e.g., in barriers heterostructures. It is characterized to be an insulator due to the high-bandgap energy and the high-activation energy of donors. Binary AlN is usually grown nucleation layer to start the growth on s.i. SiC or sapphire substrates, e.g., [2.96] and as an interlayer at the channel/barrier interface, e.g., [2.66].

Mechanical and Optical Properties

Basic properties such as the crystal structure, mechanical properties, and thermal properties of AlN are compiled in [2.287]. The mass density of AlN is much smaller than in GaN or InN, as given in Table 2.1. As depicted in Tables 2.2 and 2.3, thermal expansion and Vickers hardness of AlN are relatively similar to those of GaN. Elastic constants of AlN are given for the wurtzite phase in Table 2.3 and for the zincblende phase in Table 2.4.

The intrinsic thermal conductivity of AlN is determined in [2.428]. Its high-thermal conductivity is better than that of any other semiconductor apart from BN, SiC, and diamond, as is compiled in Table 2.16. This makes AlN a potentially attractive substrate material. The optical functions, such as the refractive index n , of AlN are given in [2.287]. The optical functions are also compiled in [2.260], including the dielectric functions and the absorption functions.

Basic Carrier Transport Properties

Although not of primary importance to most devices except in very thin layers close to the channel, transport in AlN is relatively well investigated

by MC simulations, also with respect to the understanding of the transport in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ for various material compositions x . An early compilation of the transport data of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and AlN is given in [2.123], yielding the low mobility of wurtzite AlN for both n- and p-type material, as given in Table 2.8. The low-field electron mobility of AlN is calculated to be $135 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature and at a doping concentration of 10^{17} cm^{-3} .

High-Field Transport

The electron high-field transport in wurtzite AlN is investigated by MC simulations in [2.349]. Further MC simulations on the transient transport in AlN are given in [2.121]. The characteristics are determined by the relatively high-effective electron mass of $0.48 m_e$, the large bandgap of $\approx 6.2 \text{ eV}$, and the very small intervalley separation. The resulting velocity-field characteristic yields a very high critical field of 450 kV cm^{-1} [2.349], as shown in Table 2.7. The saturation velocity in AlN reaches $1.4 \times 10^7 \text{ cm s}^{-1}$ at room temperature, while the peak velocity in the bulk is calculated to be $1.7 \times 10^7 \text{ cm s}^{-1}$ at a doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$.

Band Structure of AlN

The high-bandgap energy of AlN of 6.2 eV at room temperature allows the bandgap in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ to be modified in a broad range from the value of GaN to that of AlN. With the bandgap of InN found to be even smaller than that of GaN, an even wider range is available for the material $\text{In}_x\text{Al}_{1-x}\text{N}$. Early calculations of the band structure of wurtzite and zincblende AlN are collected in [2.236]. The band structure of wurtzite AlN is calculated in [2.128]. Electronic band structure properties of zincblende AlN are further calculated by the empirical pseudopotential method in [2.108]. From these calculations, effective electron and hole mass parameters can be obtained, as compiled in Table 2.9. The direct recombination parameter is depicted in Table 2.13, taken from [2.489] and used for the development of light-emitting diodes with very high bandgap and resulting photon energy.

Indium Nitride (InN)

InN and its compounds $\text{In}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$ so far are not yet widely used in electronic devices [2.230]. When used, both InAlN/GaN [2.143] as well as AlGaN/InGaN [2.425] heterostructures have been reported. The indium contents are low, e.g., in [2.85, 2.150], to achieve the lattice match to GaN buffer layers. The MOCVD growth of InN is complicated caused by the high-growth temperature and resulting defect background concentrations and the high amount of residual nitrogen vacancies due to the higher growth temperatures required relative to MBE growth, as described in Chapter 3. The MBE growth of InN is under development and allows improved material quality and thus the use of the full range of material composition in the

material $\text{In}_x\text{Ga}_{1-x}\text{N}$. High-quality InN has been recently grown by MBE, e.g., [2.114, 2.501]. A full review of the epitaxial growth is given in [2.38]. A bulk electron mobility of $3,570 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K is obtained. The mobility at 150 K is as high as $5,100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. P-type InN has been recently reported in [2.170], which is essential for the realization of bipolar or optoelectronic pn-devices.

Mechanical and Optical Properties

An initial compilation of mechanical, optical, and thermal properties of InN is given in [2.449, 2.451]. Mechanical data are compiled in Tables 2.1 and 2.2; however, the data are relatively uncertain, due to the lack of real bulk InN material [2.449]. Elastic constants of InN are given in Table 2.3. The thermal expansion coefficients CTE in both wurtzite and zincblende structures are compiled in Table 2.5. The CTE and the lattice constants suggest the growth on sapphire substrates [2.54]. The thermal conductivity and the heat capacity of InN are still primarily based on estimates and extrapolations, as explained in [2.449], see also Table 2.16. The optical functions of InN are compiled in [2.299]. Due to the new research on samples with improved material quality, the bandgap and optical functions of InN are reconsidered, e.g., in [2.278, 2.279, 2.425]. This fact also had a drastic impact on the calculation of transport properties and the higher band, which have not yet been fully repeated based on the new band structure.

Basic Carrier Transport Properties

An early compilation of the transport properties in InN is given in [2.54, 2.453]. The early data are characterized by high background concentrations of 10^{19} – 10^{20} cm^{-3} and associated low mobilities. An early evaluation of the InN mobility as a function of temperature and compensation ratio using variational principle calculations is given in [2.64]. In theory, very high mobility values of $4,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are calculated, which, however, have not been fully reached experimentally. An electron mobility of $1,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and a sheet carrier concentration of $1.2 \times 10^{14} \text{ cm}^{-2}$ have been obtained experimentally at the InN/AlN interface, as reported in [2.307]. Polarization engineering of n-InAlN/GaN HFETs and the effect on DC- and RF-performance are described in [2.186, 2.187]. The use of $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ is critical, as the polarization-induced charge (PIC) is a much stronger function of the material composition x than in the AlGaN/GaN material system, as explained later. P-channel $\text{In}_x\text{Ga}_{1-x}\text{N}$ HFETs based on polarization doping are demonstrated in [2.450]. Hall measurements indicate a 2D-hole gas (2DHG) mobility of approximately $700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a low temperature $T_L = 66 \text{ K}$.

High-Field Transport

Mostly, the simulated results on transport in InN are still based on the assumption of a direct bandgap of InN of 1.89 eV and an associated band structure.

This was recently corrected to the much smaller bandgap value of ≈ 0.77 eV at room temperature [2.501]. Most of the initial MC simulations thus have to be taken with a grain of salt. Electron transport in wurtzite–InN is calculated by Leary in [2.348]. Further ensemble MC calculations on the wurtzite material by Bellotti et al. are given in [2.35]. The intervalley separation energies are given in Table 2.11. As depicted in Table 2.8, the velocity-field characteristics yield a maximum carrier velocity of up to 4.2×10^7 cm s $^{-1}$ at a critical field of about 52–65 kV cm $^{-1}$ in the homogenous bulk case [2.113, 2.121]. These properties are promising, however, compared to GaAs or InGaAs material they are not really surprising when considering the low effective mass, the low bandgap, and maximum electron velocity. Transient-transport calculations in InN given in [2.121] report velocity overshoot values above 10 8 cm s $^{-1}$. Quite outstanding theoretical HFET cut-off frequencies are derived from these simulations as upper bounds for a theoretical pure InN-channel-FET performance.

Band Structure

The data for the band structure of InN are taken, e.g., from the band structure calculations in [2.128], which do not yet account for the recent modification of InN bandgap energy. More experimental data on the electronic structure of MBE-grown InN are provided in [2.307]. The effective electron mass of InN has been found to be $0.11 m_e$ [2.486], as compiled in Table 2.9. This effective mass value has to be considered high relative to the bandgap of 0.77 eV, when we compare it to other semiconductors, such as InAs or InP. Initial values of the optical bandgap of InN were reported by Tansley in [2.450]. This leads to a value of 1.89 eV at room temperature. More recent reports on the optical properties of InN, resolving the discrepancies of several publications at different growth and doping conditions, are given in [2.278, 2.279]. The bandgap of InN is found to be 0.77 eV at room temperature [2.425], as given in Table 2.10. The difference is explained by the existence of oxy-nitrides, which have a much larger bandgap. This low bandgap means a really conventional electronic III-V material, e.g., with respect to the expected breakdown of devices. Optically it means that a very broad range of wave lengths is available in the III-N systems from deep ultraviolet to red. The intervalley separation energies of both wurtzite are compiled in Table 2.11, based on the bandgap of 1.89 eV. Currently, there is little information on the intervalley energies of Zb–InN.

Boron Nitride (BN)

Boron nitride can be found in several crystallographic forms. The most important insulating or semiconducting form of BN is cubic material, which is metastable under normal conditions [2.53, 2.99, 2.253]. Ceramic BN is widely used for industrial tools as abrasive. The great advantage of cubic-BN is its Vickers hardness [2.253] and its good thermal conductivity, as compiled in Table 2.16. Even ultraviolet pn-diodes can be formed from c-BN, as given

in [2.300]. Despite the material growth problems, ultraviolet LED can be formed [2.491], which operate up to very high temperatures of 530°C [2.300].

Mechanical and Optical Properties

The mass density of cubic c-BN is given in [2.99], as compiled in Table 2.1. The outstanding Vickers hardness of BN can be observed in Table 2.2 [2.99]. Elastic constants of cubic BN are compiled in Table 2.3. The thermal expansion for cubic BN is given in Table 2.5. The values for the cubic phase are very similar to those of Zb-GaN. Thermal conductivity measurements and heat capacity measurements of cubic BN will be given in Table 2.16. The thermal conductivity of BN amounts to values of up to $750 \text{ W m}^{-1}\text{K}^{-1}$, which is higher than in any other semiconductor. The theoretical limit found is as high as $1,300 \text{ W m}^{-1}\text{K}^{-1}$.

Basic Carrier Transport Properties

Basic mobility evaluation of cubic BN as a function of carrier concentration have been provided, e.g., in [2.253]. Cubic BN is typically p-doped [2.135]. A Hall mobility of $500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is found at a carrier concentration of $5 \times 10^{18} \text{ cm}^{-3}$ [2.253]. For n-type material, only few experimental data exist, e.g., [2.300, 2.496]. As c-BN is an insulator [2.496], the transport is characterized by high-activation energies of the carriers of $\geq 0.2 \text{ eV}$.

High-Field Transport

Band structure calculations are given in [2.71] with the result that cubic BN is an insulator with a bandgap of 7.1 eV. Thus, no MC transport calculations are available for c-BN.

Dielectric Breakdown Fields

Table 2.14 compiles measured dielectric breakdown fields for various III-N bulk materials. The dielectric breakdown field of GaN is reported to be about 3 MV cm^{-1} . AlN has a much higher breakdown field due to the higher bandgap, which can be even higher than the value given in Table 2.14 [2.388]. The dielectric breakdown field of InN is not well investigated. The latter is due to the high trap concentrations N_T and the new findings for the fundamental bandgap. The breakdown fields of bulk c-BN reported in [2.53] vary from 2 to 6 MV cm^{-1} .

Table 2.14. Comparison of the bulk breakdown fields in various bulk materials at 300 K

	GaN (Wz)	Ref.	AlN (Wz)	Ref.	InN (Wz)	Ref.	BN (c)	Ref.
E_{break} (MV cm^{-1})	3.3	[2.61]	8.4	[2.388]	1.2	[2.244]	2–6	[2.253]

Wz wurtzite, c cubic

Band Structure of BN

Band structure calculations of cubic BN are available [2.496]. Similar calculations, but not of cubic phase BN, are provided in [2.237]. The bandgap of cubic BN is found to be similar to AlN and reported to be $E_g \approx 6.4$ eV at RT in [2.253]. Further calculations of cubic BN in pseudopotential local density formalism are provided in [2.497]. The calculated charge density of the BN is very similar to other III-V semiconductors. A defect analysis of Be, Mg, and Si in cubic BN is reported in [2.135, 2.448]. The substitution of B by Mg or Be typically leads to the p-type behavior of the grown material.

2.1.2 Material Limitations

The transport properties of III-N materials and the limitations of these materials have been discussed above. Further issues are discussed in the next paragraphs.

Recombination, Generation, and Breakdown

Recombination and generation are of fundamental importance for optoelectronic and bipolar electronic devices. However, due to the influence of electron trapping in FETs, these effects also critically determine their device performance. For high-field effects at increased driving forces, an experimental evaluation of impact ionization in GaN is discussed in [2.229]. The impact ionization parameters are extracted from a AlGaN/GaN HFET device with a gate length of $0.9\text{ }\mu\text{m}$. For the high-field region of $\geq 10^6\text{ V cm}^{-1}$ the data can be fitted to the classical relation:

$$\alpha_n = A \cdot \exp(-K/E), \quad (2.1)$$

$$\alpha_n = 2.9 \times 10^8 \exp(-3.4 \times 10^7/E). \quad (2.2)$$

For lower fields, this expression needs to be modified, as the field dependence is weaker due to the weakness of real carrier multiplication. The relations in (2.1)/(2.2) suggest that the critical field is a factor of 8 higher when compared to GaAs-data taken from a similar extraction procedure. MC simulations of electron impact ionization in both zincblende and wurtzite GaN are provided in [2.212]. At comparable fields, the electrons are cooler in the wurtzite structure, thus the ionization rates are lower than in the zincblende phase. A similar study on the electron initiated impact ionization in Zb-GaN can be found in [2.340]. The simulations suggest a very soft breakdown threshold similar to the device findings in [2.229]. MC simulations of hole-initiated impact ionization in both GaN-phases are discussed in [2.339]. The critical field for the hole-initiated II in Zb-GaN are found to be similar to those for the electron-initiated II and amount to 3 MV cm^{-1} . For the wurtzite structure, the breakdown is similar for high-electric fields, while for lower field, the hole II-rate appears to be greater. Electron-initiated impact ionization

Table 2.15. Breakdown fields, bandgap energies, and dielectric constants for various semiconductor materials

Material	Breakdown field (MV cm ⁻¹)	E_g (eV)	ϵ_r (-)	Ref.
Si	0.3	1.12	11.9	[2.463]
GaAs	0.4	1.43	12.5	[2.463]
InP	0.45	1.34	12.4	[2.463]
GaN (Wz)	3.3	3.43	9.5	[2.463]
AlN (Wz)	8.4	6.2	8.5	[2.388, 2.463]
InN (Wz)	1.2	0.7	15.3	[2.244, 2.451]
BN (c)	2–6	6.4	7.1	[2.253]
4H–SiC	3.5	3.2	10	[2.463]
6H–SiC	3.8	2.86	10	[2.463]
Diamond	5	5.6	5.5	[2.463]

in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is evaluated by ensemble MC simulation in [2.56] for the full material composition range. The results obey the simple expression, as given in (2.1). As expected, the critical fields increase with the increase in the material composition and bandgap. Very low impact ionization rates are observed for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in general. A study of RF-breakdown in bulk GaN and GaN MESFETs is given in [2.112]. It is found that the RF-breakdown voltage increases with the frequency of the applied RF-large-signal excitation. The difference is explained by the time-response of the particle energy. The critical field for impact ionization at AlGaN/GaN HFETs is found to be around 3 MV cm⁻¹ at room temperature, as reported in [2.95]. This agrees well with the breakdown field in bulk GaN. Breakdown fields and related material properties are again compiled for comparison in Table 2.15 for various homogeneous materials. Generally, the increase of the breakdown fields with increasing bandgap is observed. The wide bandgap materials have breakdown fields, which are an order of magnitude higher than those of conventional semiconductors. The substrate material SiC and diamond have breakdown fields similar to III-N semiconductors.

2.1.3 Thermal Properties and Limitations

In addition to their electrical limits III-N semiconductor devices are subject to strong thermal (self-)heating. Table 2.16 compiles the thermal properties of several binary semiconductor materials. The temperature dependence of the thermal conductivity is modelled according to:

$$\kappa_L(T_L) = \kappa_{300\text{ K}} \cdot \left(\frac{T_L}{300\text{ K}} \right)^\alpha, \quad (2.3)$$

as also stated in Chapter 8.

Table 2.16. Thermal properties of III-nitride binary and ternary materials at 300 K

	κ_{300} ($\text{W K}^{-1} \text{m}^{-1}$)	α (–)	c_{300} ($\text{J K}^{-1} \text{kg}^{-1}$)	Ref.
Si	148	–1.35	711	[2.406]
GaAs	54	–1.25	322	[2.356]
InP	68	–1.4	410	[2.356]
GaN (Wz)	130	–0.43	491	[2.120, 2.423]
AlN (Wz)	285	–1.57	748	[2.428]
InN (Wz)	38.5, 45, 80, 176	–	325	[2.223, 2.428, 2.449]
BN (c)	749	–	600	[2.99]
6H-SiC	390	–1.5	715	[2.57]
6H-SiC	490	–	690	[2.244, 2.331]
4H-SiC	330	–	690	[2.244, 2.416]
V-doped SiC	370	–	690	–
Sapphire	42	–	750	–
Diamond	2,000–2,500	–1.85	520	[2.405]

Thermal Conductivity and Heat Capacity

Silicon serves as a reference. The thermal conductivity of silicon is not reached by GaAs. On the contrary, GaN has a thermal conductivity similar to silicon. The thermal conductivity at 300 K κ_{300} of AlN is better than the κ_{300} of GaN, while InN has a very low value [2.223]. BN has the best value of all III-N materials. Initial determination of thermal properties of GaN is given in [2.423]. Further thermal data is compiled in [2.4]. The intrinsic thermal conductivity for AlN is determined in [2.428]. The thermal conductivity of GaN is often quoted dating back to the work of Sichel [2.423]. However, several investigations are available which especially focus on the effects of dislocations on the thermal conductivity. A good overview of the data are presented and the methods of measurements are compiled in [2.120]. The effect of dislocations on the thermal conductivity in GaN is investigated experimentally in [2.264]. The measurements show a dramatic increase of the thermal conductivity at reduced dislocation density of 10^8 cm^{-2} , especially at temperatures below 200 K. The theoretical predictions in [2.216] support a maximum value for the thermal conductivity in GaN of nearly $200 \text{ W K}^{-1} \text{ m}^{-1}$. The experimental data for the thermal conductivity of InN ($\leq 45 \text{ W K}^{-1} \text{ m}^{-1}$) is much lower than the theoretical predictions of 176 $\text{W K}^{-1} \text{ m}^{-1}$ [2.223].

The data for the heat capacity are also compiled in Table 2.16. The heat capacity is given for constant pressure. For SiC, the measured value of the polytype 6H-SiC is used for SiC in general [2.356]. The heat capacity of the binary semiconductors is lower than of the substrate material. More analysis with respect to the packaging materials and to the dynamic response is provided in Chapter 8.

2.1.4 Ternary and Quaternary III-N Materials

The existence of ternary and even quaternary materials in the III-N system is a fundamental advantage relative to other wide bandgap semiconductor materials, such as SiC. The possibility of growing $\text{Al}_x\text{Ga}_{1-x}\text{N}$, $\text{In}_x\text{Ga}_{1-x}\text{N}$, and $\text{In}_x\text{Al}_{1-x}\text{N}$ in heterostructures with the III-N binaries allows bandgap engineering. This has tremendous impact on the electronic and optoelectronic application of the materials. The material parameters of the quantity P are combined by quadratic interpolation in the following two approaches:

$$P_{\text{A}_x\text{B}_{1-x}\text{N}} = P_{\text{A}} \cdot x + P_{\text{B}} \cdot (1 - x) + C_{\text{P},\text{AB}} \cdot x \cdot (1 - x). \quad (2.4)$$

In the second approach, (2.4) can be written in another way, i.e.:

$$P_{\text{A}_x\text{B}_{1-x}\text{N}} = a + b \cdot x + c \cdot x^2 \quad (2.5)$$

resulting in different coefficients, which can be directly correlated with the binary materials. Sometimes (2.5) is extended to a third-order polynomial:

$$P_{\text{A}_x\text{B}_{1-x}\text{N}} = a + b \cdot x + c \cdot x^2 + d \cdot x^3. \quad (2.6)$$

All relevant quantities will be analyzed in the following sections using the aforementioned formulae in quadratic interpolation. If necessary, cubic or other interpolation schemes will be mentioned.

Aluminum Gallium Nitride ($\text{Al}_x\text{Ga}_{1-x}\text{N}$)

$\text{Al}_x\text{Ga}_{1-x}\text{N}$ is the most important ternary compound, as the lattice-mismatch relative to GaN can be effectively controlled for nearly all material compositions. A distinction may be required for wurtzite and zincblende AlGaN materials, as the zincblende material has a transition from a direct to an indirect semiconductor [2.235].

Mechanical and Optical Properties

For mass density, Vickers hardness, and dielectric constants, typically no bowing is applied, and the values can be interpolated linearly with high precision between the binary values of GaN and AlN. The heat capacity of the ternaries is interpolated linearly as given in (2.7):

$$c_{\text{L},\text{AB}} = (1 - x) \cdot c_{\text{L},\text{A}} + x \cdot c_{\text{L},\text{B}}. \quad (2.7)$$

The thermal conductivity of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is interpolated as the following equation (2.8), taken from [2.357]. Data for the thermal conductivity of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ is given in [2.255]. The derived parameters are given in Table 2.17.

$$\kappa_{\text{AB}} = \left(\frac{(1 - x)}{\kappa_{\text{A}}} + \frac{x}{\kappa_{\text{B}}} + \frac{x \cdot (1 - x)}{C_{\kappa,\text{AB}}} \right)^{-1}. \quad (2.8)$$

Table 2.17. Interpolation of the thermal conductivity κ in III-N ternary materials

	$C_{\kappa,AB}$ (W m ⁻¹ K ⁻¹)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	6.95	[2.255]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	1.4	[2.356]
$\text{In}_x\text{Al}_{1-x}\text{N}$	3.3	[2.356]

Similarly, the temperature dependence α_{AB} is interpolated linearly.

$$\alpha_{AB} = (1 - x) \cdot \alpha_A + x \cdot \alpha_B. \quad (2.9)$$

The strong material composition dependence of the thermal conductivity is found for all ternary III-V semiconductors [2.356]. A thermal conductivity of 25 W m⁻¹ K⁻¹ is found for $\text{Al}_{0.4}\text{Ga}_{0.6}\text{N}$ [2.255].

Basic Carrier Transport Properties

An evaluation of temperature-dependent transport properties in zincblende $\text{Al}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Ga}_{1-x}\text{N}$ semiconductors using MC simulations is given in [2.17]. The data for (2.6) are compiled in Table 2.18. The table further gives the interpolation of the low-field mobility according to the harmonic mean:

$$\frac{1}{\mu_{AB}} = \frac{x}{\mu_A} + \frac{1-x}{\mu_B} + \frac{x \cdot (1-x)}{C_{\mu,AB}}. \quad (2.10)$$

The database for the mobility of $\text{In}_x\text{Al}_{1-x}\text{N}$ and $\text{In}_x\text{Ga}_{1-x}\text{N}$ is still relatively poor. However, initial values are provided based on the investigations in [2.65]. The alloy-scattering potential is found to be important for the bowing of the drift mobility of both $\text{In}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$, both for room temperature and at 77 K [2.65]. The alloy scattering is considered relatively less important for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in [2.65]. However, the value extracted for the mobility of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in [2.113] show also a strong dependence on the material composition. This is confirmed by the numerical study of the alloy scattering in AlGaN and InGaN [2.34].

The values for the bowing of the drift mobility are given in Table 2.18.

High-Field Transport

Table 2.19 compiles values for the bowing of the saturation velocity, which is calculated both according to the polynomial approach of (2.6) and according to quadratic bowing, as given in (2.14).

As can be found in [2.17], the critical field and the peak velocities typically do not vary linearly as a function of material composition for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ or $\text{In}_x\text{Ga}_{1-x}\text{N}$ between the binary constituents. Again a polynomial approach is used, as given in Table 2.19. In another approach, quadratic bowing can be applied:

$$v_{\text{sat},\text{AB}} = (1 - x) \cdot v_{\text{sat},\text{A}} + x \cdot v_{\text{sat},\text{B}} + x \cdot (1 - x) \cdot C_{v_{\text{sat}},\text{AB}}, \quad (2.11)$$

$$v_{\text{peak},\text{AB}} = (1 - x) \cdot v_{\text{peak},\text{A}} + x \cdot v_{\text{peak},\text{B}} + x \cdot (1 - x) \cdot C_{v_{\text{peak}},\text{AB}}, \quad (2.12)$$

$$E_{\text{crit},\text{AB}} = (1 - x) \cdot E_{\text{crit},\text{A}} + x \cdot E_{\text{crit},\text{B}} + x \cdot (1 - x) \cdot C_{E_{\text{crit}},\text{AB}}. \quad (2.13)$$

Table 2.18. Interpolation of the mobility μ in III-N ternary compounds for different models at RT

$\mu(x)$	a ($\text{cm}^2 (\text{Vs})^{-1}$)	b ($\text{cm}^2 (\text{Vs})^{-1}$)	c ($\text{cm}^2 (\text{Vs})^{-1}$)	d ($\text{cm}^2 (\text{Vs})^{-1}$)	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$ (Zb)	1,157	-1,329	-283	671	10^{17}	[2.17]
$\text{In}_x\text{Ga}_{1-x}\text{N}$ (Zb)	465	755	-61	676	10^{17}	[2.17]
$\mu(x)$	$C_{\mu,\text{n},\text{AB}}$ ($\text{cm}^2 (\text{Vs})^{-1}$)	$C_{\mu,\text{p},\text{AB}}$ ($\text{cm}^2 (\text{Vs})^{-1}$)	Ref.			
$\text{Al}_x\text{Ga}_{1-x}\text{N}$ (Wz)	40	1e6			[2.113, 2.356]	
$\text{In}_x\text{Ga}_{1-x}\text{N}$ (Wz)	97	1e6			[2.65]	
$\text{In}_x\text{Al}_{1-x}\text{N}$ (Wz)	1e6	1e6			[2.65, 2.452]	

Wz wurtzite, Zb zincblende

Table 2.19. Interpolation of the saturation velocity v_{sat} , the peak velocity v_{peak} , and E_{crit} in III-N ternary compounds

v_{sat}	a (10^7 cm s^{-1})	b (10^7 cm s^{-1})	c (10^7 cm s^{-1})	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	1.3425	0.574	-0.3215	10^{17}	[2.17]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	1.3286	0.3657	-0.2857	10^{17}	[2.17]
	$C_{v_{\text{sat}},\text{AB}}$ (10^7 cm s^{-1})	$C_{v_{\text{peak}},\text{AB}}$ (10^7 cm s^{-1})	$C_{E_{\text{crit}},\text{AB}}$ (kV cm^{-1})	N_D (cm^{-3})	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	-3.85	-0.1	50	10^{17}	[2.17, 2.356]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	0.35	-1	-25	10^{17}	[2.17]
$\text{In}_x\text{Al}_{1-x}\text{N}$	-	-	-		-
	E_{crit} (kV cm^{-1})	N_D (cm^{-3})	Ref.		
GaN (Wz)	225	2×10^{16}		[2.211, 2.500]	
GaN (Wz)	140	10^{17}		[2.121]	
AlN (Wz)	450	10^{17}		[2.121]	
InN (Wz)	65	10^{17}		[2.121]	
GaN (Zb)	150	10^{17}		[2.17]	
AlN (Zb)	550	10^{17}		[2.17]	
InN (Zb)	45	10^{17}		[2.17]	

The parameters are also given in Table 2.19. The values of the velocities of the binaries are given in Table 2.8, while the critical fields E_{crit} are repeated in Table 2.19 from Table 2.8.

Band Structure

Band structure properties of ternary $\text{Al}_x\text{Ga}_{1-x}\text{N}$ alloys are given in [2.127, 2.235]. The bowing of the effective masses m_ν and the bandgap E_g are described by quadratic interpolation:

$$m_{\nu,\text{AB}} = (1 - x) \cdot m_{\nu,\text{A}} + x \cdot m_{\nu,\text{B}} + x \cdot (1 - x) \cdot C_{m_\nu,\text{AB}}, \quad (2.14)$$

$$E_{g,\text{AB}} = (1 - x) \cdot E_{g,\text{A}} + x \cdot E_{g,\text{B}} + x \cdot (1 - x) \cdot C_{E_g,\text{AB}}. \quad (2.15)$$

For $\text{Al}_x\text{Ga}_{1-x}\text{N}$, the dependence of the fundamental bandgap on alloy material composition and on pressure are discussed in [2.410]. A relatively strong bowing is observed for $\text{Al}_x\text{Ga}_{1-x}\text{N}$. The bowing parameters are compiled in Table 2.21. Further information on the dependence of the bandgap on the material composition of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ for ($0 \leq x \leq 1$) based on ultraviolet photodetectors grown on sapphire are given in [2.489]. The parameters for the bowing of the masses and bandgap are given in Table 2.20 and Table 2.21. As can be seen the bowing is mostly neglected. Band structure nonlocal pseudopotential calculations of the III-N wurtzite phase materials of the ternary alloys $\text{Al}_x\text{Ga}_{1-x}\text{N}$, $\text{In}_x\text{Ga}_{1-x}\text{N}$, and $\text{In}_x\text{Al}_{1-x}\text{N}$ are given in [2.127]. The data include a systematic collection of the effective mass bowing parameters at the relevant conduction band minima. The interpolation of the bandgap energies is given in Table 2.21. The recent changes for InN are included. Distinctions of the bowing are necessary in the zincblende structure, as direct-indirect transitions occur for $\text{In}_x\text{Al}_{1-x}\text{N}$ and $\text{Al}_x\text{Ga}_{1-x}\text{N}$. For $\text{Al}_x\text{Ga}_{1-x}\text{N}$, this occurs at $x = 0.69$ [2.254], while for $\text{In}_x\text{Al}_{1-x}\text{N}$, this occurs for $x = 0.187$ [2.256].

Table 2.20. Interpolation of the effective masses in III-N ternary materials

	$C_{m_n,\text{AB}}$ (Wz)	$C_{m_p,\text{AB}}$ (Wz)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	0.0048	0	[2.127, 2.485]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	0	0	[2.485]
$\text{In}_x\text{Al}_{1-x}\text{N}$	0	0	[2.485]

Wz wurtzite, Zb zincblende

Table 2.21. Interpolation of the bandgap energy in III-N ternary materials

	$C_{E_{\text{gap}},\text{AB}}$ (Wz)	$C_{E_{\text{gap}},\text{AB}}$ (Zb)	Ref.
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	-0.7, -1.33	Γ : -0.7, X: -0.61	[2.410, 2.485]
$\text{In}_x\text{Ga}_{1-x}\text{N}$	-1.4	-1.4	[2.279, 2.485]
$\text{In}_x\text{Al}_{1-x}\text{N}$	-2.5	Γ : -2.5, X: -0.61	[2.485]

Indium Gallium Nitride ($\text{In}_x\text{Ga}_{1-x}\text{N}$) and Indium Aluminum Nitride ($\text{In}_x\text{Al}_{1-x}\text{N}$)

The importance of InN and its ternary compounds is due to the smaller bandgap relative to GaN, allowing for a broader variety of layers for bandgap engineering also into the visible optical range for optoelectronic devices. High-quality $\text{In}_x\text{Ga}_{1-x}\text{N}$ layers were recently grown by MBE, e.g., in [2.114, 2.501], mostly on sapphire substrates. $\text{In}_x\text{Al}_{1-x}\text{N}$ is lattice-matched to GaN for $x = 0.17$, which has recently drawn attention to this material for HEMT device applications [2.230, 2.485].

Mechanical and Optical Properties

Initial layer preparation and optical properties of $\text{Ga}_{1-x}\text{In}_x\text{N}$ thin films are demonstrated and compiled in [2.352]. The initial material is mostly polycrystalline. The thermal conductivity and the heat capacity of $\text{In}_x\text{Ga}_{1-x}\text{N}$ are interpolated from the binaries, as shown in (2.7) and (2.8) with parameters from Table 2.16 and Table 2.17.

Basic Carrier Transport Properties

Similar to InGaAs and InAlAs, initial expectations for InN and its compounds yield lower effective mass than GaN [2.128]. However, good quality films, especially for high In-contents, have not been realized with MOCVD growth, e.g., [2.181]. MBE growth has allowed InN to be grown with improved material quality, e.g., [2.86]. An initial compilation of the transport properties in $\text{In}_x\text{Ga}_{1-x}\text{N}$ is given in [2.54, 2.453] and in the references therein.

High-Field Transport

MC analysis of the wurtzite $\text{In}_x\text{Ga}_{1-x}\text{N}$ is given in [2.113]. The analysis is based on the wrong bandgap of InN. The analysis of peak velocities and mobility of the ternary material is strongly dependent on the alloy scattering in the resulting ternary material [2.34]. The parameters for the peak velocity v_{peak} , the saturation velocity v_{sat} , and the critical field E_{crit} are compiled in Table 2.19. MC simulations of the temperature-dependent transport properties of zincblende $\text{In}_x\text{Ga}_{1-x}\text{N}$ are given in [2.17] and are also compiled in Table 2.19. The critical field E_{crit} decreases strongly with the indium content. Similarly the saturation velocity of $\text{In}_x\text{Ga}_{1-x}\text{N}$ increases from GaN to InN. Very few data are available on the transport properties of $\text{In}_x\text{Al}_{1-x}\text{N}$. Al-rich $\text{In}_x\text{Al}_{1-x}\text{N}$ will certainly reveal insulating properties similar to AlN. $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is the most important composition to understand. Calculations and initial data on the low-field mobility can be found in [2.452]. The prediction yields a low-field mobility of $\leq 200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x \leq 0.5$. High-field transport in InAlN is so far not understood very well.

Band Structure

For the band structure, nonlocal pseudopotential calculations of $\text{In}_x\text{Ga}_{1-x}\text{N}$ and $\text{In}_x\text{Al}_{1-x}\text{N}$ are given in [2.127] and are still based on a fundamental bandgap of 1.89 eV. The conduction band offset of InGaN/GaN is reported in [2.530]. The ratio of conduction to valence band offset is 58:42. With the improvements in material quality based on MBE growth, small bandgap bowing has been reported, e.g., in [2.501]. The bandgap bowing has been thoroughly investigated with respect to both bowing of InGaN and the bandgap value of InN in [2.86, 2.278]. InN is found to be a small bandgap semiconductor with a bandgap energy of 0.77 eV at RT [2.86]. The data are extracted from optical absorption, photoluminescence, and photomodulated reflectance. The higher bands are still under consideration, e.g., [2.163, 2.373, 2.523].

2.2 Polar Semiconductors for Electronics

Next to the basic knowledge on the bulk material properties, further substantial material analysis is required. III-N semiconductors provide the occurrence of significant electrical polarization effects that dominate especially the interfaces [2.499]. This fact deserves discussion in an extra section, since the effects are much stronger than in any of the semiconductors in use so far. A good overview is given in [2.499]. Precisely defining doping and doping profiles is one of the core competencies of silicon CMOS electronics, e.g., [2.32, 2.149]. However, for III-N devices, control of the polarization effects gains an importance similar or even greater than the impact of the impurity doping profiles in other semiconductor materials. Fig. 2.3 gives the crystal structure of wurtzite GaN, as described, e.g., in [2.11, 2.12]. The noncentrosymmetric GaN crystal leads to a strong ionicity and a residual electrical polarity of the semiconductor. Fig. 2.3 depicts the planar nature of the polarity. The analysis of the crystal structure further reveals the physical mechanisms of the charge control, the overall available carrier concentration, and their dependence from the layer structure.

2.2.1 Spontaneous Polarization

A basic understanding of the impact of material growth conditions by various methods in the AlN/GaN/InN material system on the polarization charge is achieved and reported in [2.11, 2.12, 2.90]. The findings are based on the crystal polarization constants of Bernardini et al. in [2.36]. The importance of both spontaneous and piezoelectric components is pointed out there, in contrast to earlier publications, e.g., [2.22]. The spontaneous polarization occurs along the *c*-axis of wurtzite structures and leads to strong electric fields of 3 MV/cm [2.12]. Results for the PIC of the model are compared in [2.12] to experimental results for HEMT channels achieved at the date of publication; in the meantime, additional progress has been achieved for the improvement

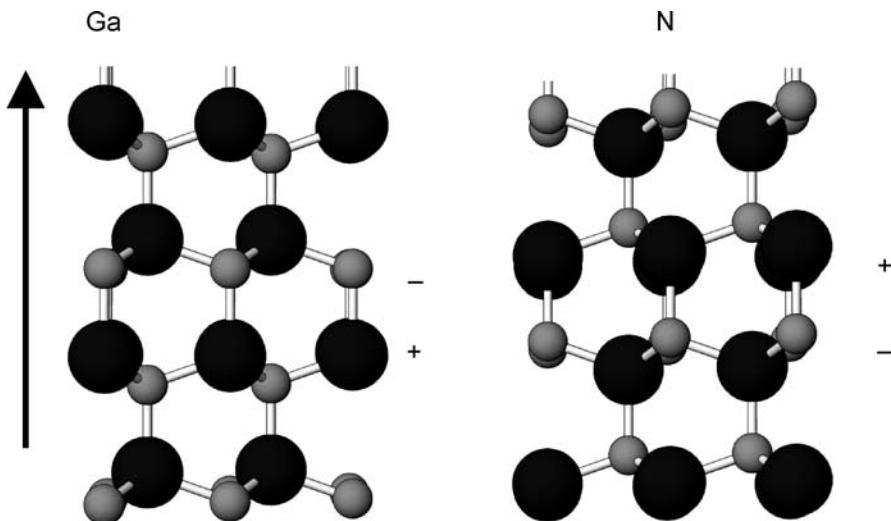


Fig. 2.3. Crystal structures of GaN for (a) (left) Ga-face, and (b) (right) N-face growth

in III-N material quality, i.e., for the reduction of defects. Basic findings for III-N layers grown by the two most important growth techniques, MOCVD and MBE, presented in these and other publications include:

- The absolute value of the piezoelectric constants of III-N semiconductors are ten times higher than in conventional III-V and II-VI semiconductors [2.36].
- Very similar mobility values, sheet carrier concentrations, and material quality are achieved for III-N semiconductors grown by MBE and MOCVD [2.96].
- Spontaneous polarization is more important than piezoelectric polarization for $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure interfaces [2.12, 2.36].
- Spontaneous polarization can be as important as piezoelectric polarization or even more important for $\text{In}(\text{Al})\text{N}/\text{GaN}$ interfaces and still lead to very high sheet carrier densities [2.12, 2.36, 2.231].
- The polarity of the polarization can be changed and even be inverted as a function of strain and thus of material composition.
- A difference exists between MBE- and MOCVD-grown material with respect to the variety of the polarity at the charged interfaces [2.12, 2.90].
- Theoretical and experimental results agree to a certain extent [2.11].
- Uncertainties arise from the impact of surface conditions [2.11] and Fermi-level pinning at the passivation interfaces, dislocations [2.11], possible polarity intermixing; the latter, however, is unlikely in good structures.
- Surface roughness and nonabrupt interfaces are considered less influencing the sheet carrier concentration.

Table 2.22. Parameter sets for the spontaneous polarization of III-N binary semiconductors

Material	GaN (C m ⁻²)	AlN (C m ⁻²)	InN (C m ⁻²)	Ref.
P_{SP}	-0.029	-0.081	-0.032	[2.36]
P_{SP}	-0.034	-0.090	-0.042	[2.485]

GaN layers can either be grown Ga-face(-up) or N-face(-up), compare Fig. 2.3. For the orientation of the polarization in this book, the positive direction points from the metallic cation (Ga,In) to the nitride anion (N) along the *c*-axis. Thus, in the case of a Ga-face interface, the polarization points toward the substrate, while for a N-face interface, the polarization is directed toward the surface of the layer sequence. For further evaluation, the devices are either (a) considered to be grown on a thick buffer, relaxing the mismatch from the substrate to the lattice constant of the device layers, or (b) the strain is residual in the device material. For the polarization analysis Table 2.22 gives parameter sets for the spontaneous polarization for the binary III-N materials from various sources. For all materials, the effective spontaneous polarization is negative and the magnitude increases from GaN to InN to AlN.

Interfaces between Binary and Ternary Materials

The following interpolation schemes can be used for the spontaneous polarization in the GaN/AlN, the InN/GaN, and the InN/AlN material system:

$$P_{SP,Al_xGa_{1-x}N/GaN}(x) = \left(-0.052 \cdot x - 0.029 \right) (\text{Cm}^{-2}), \quad (2.16)$$

$$P_{SP,In_xGa_{1-x}N/GaN}(x) = \left(-0.003 \cdot x - 0.029 \right) (\text{Cm}^{-2}), \quad (2.17)$$

$$P_{SP,In_xAl_{1-x}N/GaN}(x) = \left(0.049 \cdot x - 0.081 \right) (\text{Cm}^{-2}). \quad (2.18)$$

The methodology and the parameter values for the AlGaN/GaN interface are taken from [2.36]. A similar theoretical study of the macroscopic polarization and the impact on the GaN HEMT in a nonlinear model of the material composition is given in [2.527].

2.2.2 Piezoelectric Polarization

In addition to spontaneous polarization, piezoelectric effects were first considered to be responsible for the sheet carrier densities in GaN devices, e.g., in [2.525]. Early *C*–*V* measurements of the piezoelectrically induced charge (spontaneous polarization is not considered explicitly) in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure FETs are given in [2.525] for both MBE- and MOCVD-grown material. The piezoelectric polarization is based on strain to the III-N crys-

Table 2.23. Piezoelectric constants e_{ij} , dielectric constants ϵ_{ij} , and lattice parameter a_i , c_i sets of III-N binary wurtzite semiconductors

Material	GaN	AlN	InN	BN	Ref.
e_{33} (C m^{-2})	0.73	1.46	0.97	—	[2.36]
e_{31} (C m^{-2})	-0.49	-0.6	-0.57	—	[2.36]
e_{33} (C m^{-2})	—	1.55	—	—	[2.12]
e_{31} (C m^{-2})	—	-0.58	—	—	[2.12]
e_{15} (C m^{-2})	—	-0.48	—	—	[2.12]
e_{33} (C m^{-2})	1	—	—	—	[2.338]
e_{31} (C m^{-2})	-0.36	—	—	—	[2.338]
e_{15} (C m^{-2})	-0.3	—	—	—	[2.338]
ϵ_{11} (—)	9.5	9.0	—	—	[2.29, 2.36]
ϵ_{33} (—)	10.4	10.7	—	—	[2.29, 2.36]
a_0 (\AA)	3.189	3.112	3.54	2.534	[2.11]
c_0 (\AA)	5.185	4.982	5.705	4.191	[2.11]

tal and a displacement of the anion-sublattice to the cation-sublattice, see Fig. 2.3. This can lead to very high electric fields of 2 MV/cm.

Table 2.23 gives a summary of the piezoelectric constants of the different III-N binary materials [2.11] for comparison and further evaluation. The lattice parameters have been added where necessary. In various publications, e.g., [2.36], the piezoelectric component is considered to have the highest uncertainty relative to the other components. The piezoelectric polarization induced by strain along the c -axis in a strained layer of wurtzite-type III-N semiconductors is calculated, according to [2.11]:

$$P_{\text{PZ}} = 2 \cdot \frac{a - a_0}{a_0} \left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}} \right). \quad (2.19)$$

In (2.19), C_{13} and C_{33} denote the elastic constants, which require special attention due to the residual strain in the semiconductor layers on top of the buffer. a and a_0 are the lengths along the hexagonal edge, which are similarly modified. For the lattice, elastic, and piezoelectric constants, the following linear interpolations are used for the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ material system [2.12]:

$$a_0(x) = (-0.077 \cdot x + 3.189) \cdot 10^{-10} \text{ (m)}, \quad (2.20)$$

$$c_0(x) = (-0.203 \cdot x + 5.189) \cdot 10^{-10} \text{ (m)}, \quad (2.21)$$

$$C_{13}(x) = (5 \cdot x + 103) \text{ (GPa)}, \quad (2.22)$$

$$C_{33}(x) = (-32 \cdot x + 405) \text{ (GPa)}, \quad (2.23)$$

$$e_{33}(x) = 0.73 \cdot x + 0.73 \text{ (C m}^{-2}), \quad (2.24)$$

$$e_{31}(x) = -0.11 \cdot x - 0.49 \text{ (C m}^{-2}). \quad (2.25)$$

For the $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ material system, where GaN forms the channel, the interpolation reads:

$$a_0(x) = (0.418 \cdot x + 3.112) \cdot 10^{-10} \text{ (m)}, \quad (2.26)$$

$$c_0(x) = (0.723 \cdot x + 4.982) \cdot 10^{-10} \text{ (m)}, \quad (2.27)$$

$$C_{13}(x) = (-16 \cdot x + 108) \text{ (GPa)}, \quad (2.28)$$

$$C_{33}(x) = (-149 \cdot x + 373) \text{ (GPa)}, \quad (2.29)$$

$$e_{33}(x) = -0.49 \cdot x + 1.46 \text{ (C m}^{-2}\text{)}, \quad (2.30)$$

$$e_{31}(x) = 0.03 \cdot x - 0.6 \text{ (C m}^{-2}\text{)}. \quad (2.31)$$

For the $\text{GaN}/\text{In}_x\text{Ga}_{1-x}\text{N}$ material system, where GaN forms the barrier layer with the higher bandgap energy the interpolation reads growing the InGaN pseudomorphically on GaN:

$$a_0(x) = (0.351 \cdot x + 3.189) \cdot 10^{-10} \text{ (m)}, \quad (2.32)$$

$$c_0(x) = (0.52 \cdot x + 5.189) \cdot 10^{-10} \text{ (m)}, \quad (2.33)$$

$$C_{13}(x) = (-11 \cdot x + 103) \text{ (GPa)}, \quad (2.34)$$

$$C_{33}(x) = (-176 \cdot x + 405) \text{ (GPa)}, \quad (2.35)$$

$$e_{33}(x) = 0.24 \cdot x + 0.73 \text{ (C m}^{-2}\text{)}, \quad (2.36)$$

$$e_{31}(x) = -0.08 \cdot x - 0.49 \text{ (C m}^{-2}\text{)}. \quad (2.37)$$

The calculation of the PIC derived from the above polarization results is described later.

2.2.3 Device Design Using Polarization-Induced Charges

Deduced from the above considerations, the resulting charge can be calculated for the various interface combinations and growth conditions in several device configurations. In this context, mechanisms of the 2D-electron gas formation in AlGaN/GaN HEMTs are investigated by synchrotron radiation emission spectroscopy in [2.160]. The surface Fermi-level at the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ interface is found to be pinned at an energy of 1.6 eV below the conduction band minimum independent of the Al-content. Initial measurements of the piezoelectrically induced charge in AlGaN/GaN HFETs are given in [2.525]. For a heterointerface, the following formulae hold for the interface charge σ_B derived from the tensor of the wurtzite crystals mentioned above [2.11]:

$$\sigma_B = \mathbf{n} \cdot \mathbf{P}, \quad (2.38)$$

$$= P_{\text{bottom}} - P_{\text{top}}, \quad (2.39)$$

$$= P_{\text{SP,bottom}} - [P_{\text{SP,top}} + P_{\text{PZ,top}}], \quad (2.40)$$

$$= \sigma_{B,\text{SP}} + \sigma_{B,\text{PZ}}. \quad (2.41)$$

Deduced from (2.38)–(2.41), various interface combinations and devices can be constructed for their use in heterostructure FETs and HBTs. Some will be

discussed later. The situations are displayed graphically in Fig. 2.4 with focus on electron devices. Hole-based devices are neglected due to the poor transport properties in the III-N system. For an electron channel, two conditions must be fulfilled:

- A positive interface charge must be present at the interface based on the overall polarization
- The bandgap in the semiconductor, to where the electrons are driven, must be smaller than of the other layer (as III-N semiconductor only form type I transitions).

I: Al_xGa_{1-x}N/GaN Single Heterojunction HEMT

For an Al_xGa_{1-x}N layer grown on top of a relaxed GaN layer, spontaneous polarization and piezoelectric polarization are parallel and under tensile strain. Depending on the growth conditions, the following situations occur:

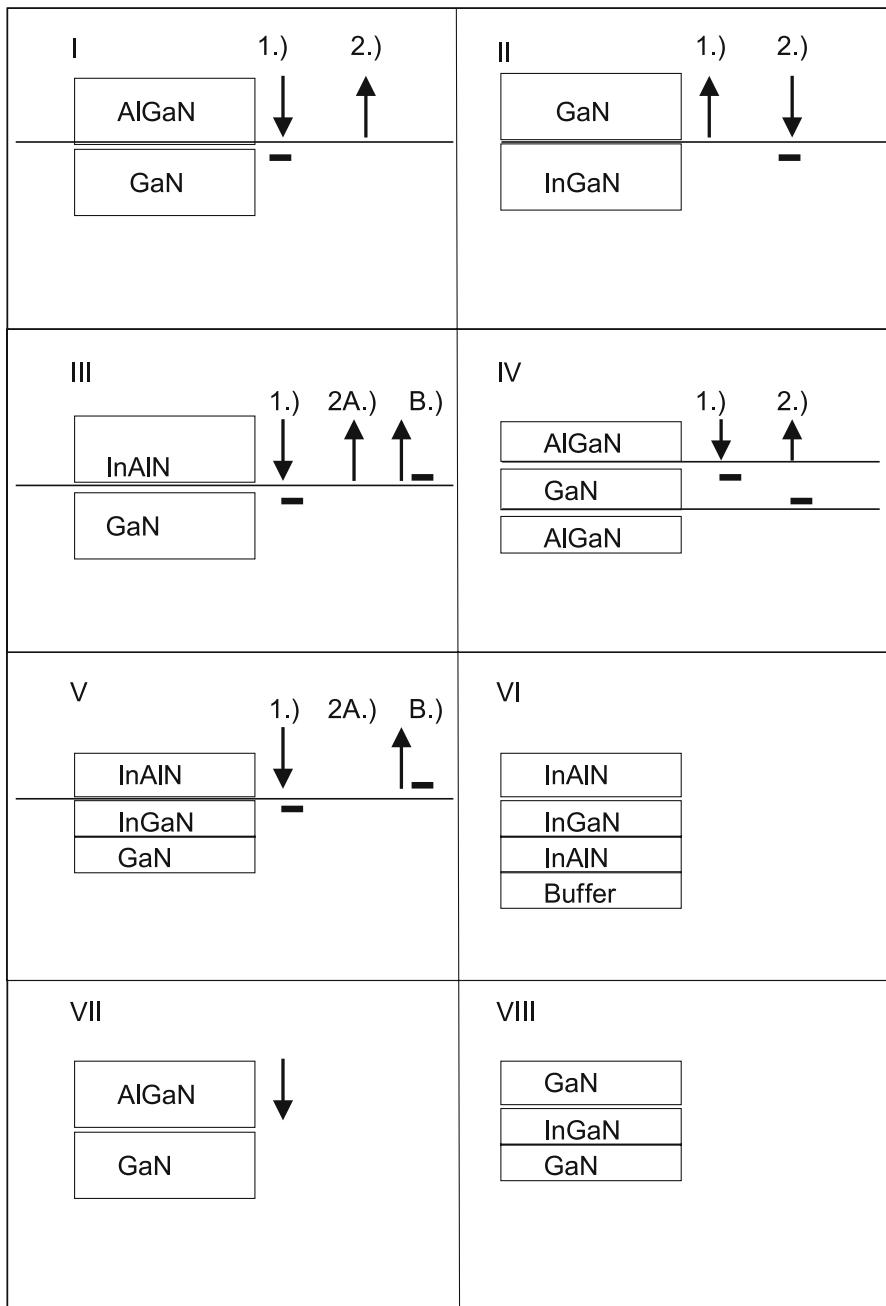
1. In the case of Ga-face, i.e., a anion surface, the polarity of the parallel polarization components results in an electron GaN channel formation at the interface.
2. In the case of N-face or cation-type growth, however, the orientations of both the polarization components are changed and thus no electron channel formation occurs at the AlGaN/GaN interface.

In this context it is an important assumption for the charge analysis that no additional material or layers are grown on top of the AlGaN barrier layer. Additional surface states and the interaction with additional interfaces reduce the carrier concentration at the interface under consideration. This is also true for nucleation layer sequences used to compensate the lattice-mismatch directly at the substrate–buffer interface.

II: GaN/In_xGa_{1-x}N Single and Double Heterojunction HEMT

For the interface of In_xGa_{1-x}N with various concentrations grown pseudomorphically on top of a relaxed GaN buffer, the In_xGa_{1-x}N layer is under compressive strain for all material compositions. Spontaneous and piezoelectric polarization are antiparallel and the piezoelectric polarization is stronger than the spontaneous polarization. The following situations can occur, depending on growth conditions:

1. In the case of Ga-face growth, the residual polarization points toward the GaN, thus the effective charge at the interface is negative, and no electron channel is formed.
2. In the case of N-face growth, the effective interface charge is positive and a 2DEG forms a channel in the In_xGa_{1-x}N.

**Fig. 2.4.** Polarization situations for various III-N devices

III: In_xAl_{1-x}N/GaN Single Heterojunction HEMT

For the interface In_xAl_{1-x}N/GaN, the two binaries InN and AlN forming In_xAl_{1-x}N have a bandgap both smaller and larger than the bandgap of GaN, which makes the situation more complicated. The GaN buffer is grown relaxed on the substrate, thus the In_xAl_{1-x}N layer on top is under different strain unless for In_{0.17}Al_{0.83}N, which is lattice-matched to crystalline GaN.

1. For Ga-face growth, both polarization components are parallel for $x < 0.17$, and an electron channel forms in the GaN layer for $x < 0.3$ due to the resulting overall polarization, e.g., [2.231].
2. For N-face growth the interesting situation arises for $x > 0.3$. Both polarization types are antiparallel in the In_xAl_{1-x}N with the following distinction:
 - A.) For $0.3 < x < 0.6$, no electron channel forms in the In_xAl_{1-x}N as the bandgap of In_xAl_{1-x}N is still bigger than of GaN.
 - B.) For $0.6 \leq x \leq 1$ the bandgap of GaN is larger than of In_xAl_{1-x}N, thus a 2DEG and thus an electron channel forms in the In_xAl_{1-x}N.

IV: Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N Double Heterojunction HEMT

The realization of double heterojunction devices is very desirable due to enhanced carrier confinement for both HEMT and HBT and improved back-side isolation for FETs. The assumption of a relaxed GaN buffer on top of the substrate has to be dropped in this case. A good trap-free Al_yGa_{1-y}N material has to be grown relaxed on a substrate such as SiC or sapphire with a material composition grading of the Al_yGa_{1-y}N buffer and leading to an Al_xGa_{1-x}N/GaN/Al_yGa_{1-y}N heterostructure. Double heterostructure FETs are realized, e.g., in [2.289]. A smaller composition y is chosen for the buffer layer to reduce the mismatch toward the substrate. When growing AlGaN on top of SiC, either N-face or Ga-face polarization can be chosen for the first interface:

- In the case of a Ga-face growth, a conventional double heterojunction FET forms with an electron channel at the upper heterointerface.
- In the case of an N-face growth, an inverted double heterojunction FET forms with an electron gas at the lower interface under the assumption, that the upper barrier does not modify the strain of the GaN channel layer.

Typically, a Ga-face approach will be chosen which improves the isolation of the channel toward the buffer layer and thus typically reduces the $I_{D\min}$ for FETs. Further, in [2.289], the transconductance g_m is increased as compared to the single heterojunction device.

V: In_xAl_{1-x}N/In_yGa_{1-y}N Double Heterojunction HEMT on GaN Buffer

In the Al_xGa_{1-x}N/GaN material system, the sheet carrier concentration density in the channel is increased by the increase of x and at the same

time limited by the increase of defect concentration in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer for rising x and the onset of relaxation. An $\text{In}_y\text{Ga}_{1-y}\text{N}$ channel layer is a more general case of the situation III of the InAlN/GaN HFET. An $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{GaN}$ double heterojunction FET can be formed in this case. The formation of electron or hole gases is dependent on both material compositions x and y . In [2.230], mole fractions of $0.08 \leq x \leq 0.27$ and $(0 \leq y \leq 0.18)$ are suggested for the formation of HFETs, based on the analysis of the maximum strain values possible in the $\text{In}_x\text{Al}_{1-x}\text{N}$ barrier. $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ is lattice-matched to GaN. Strain analysis based on a relaxed GaN buffer yields the following distinction [2.230]:

- For $\text{In}_x\text{Al}_{1-x}\text{N}$ with $x \leq 0.17$ the $\text{In}_x\text{Al}_{1-x}\text{N}$ is under tensile strain and the piezoelectric field in the channel is in favor of the increase in electron concentration.
- For $\text{In}_x\text{Al}_{1-x}\text{N}$ with $x \geq 0.17$, the $\text{In}_x\text{Al}_{1-x}\text{N}$ is under compressive strain, and the strain reduces the electron concentration [2.231].
- Assuming an $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ barrier lattice-matched to GaN, the channel material $\text{In}_y\text{Ga}_{1-y}\text{N}$ can be varied:
- The compressive strain in the $\text{In}_y\text{Ga}_{1-y}\text{N}$ can be varied in the range $0.08 \leq x \leq 0.27$ in order to further enhance the charge carrier density and the upper $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}$ interface. A value of $y = 0.1$ and $x = 0.17$ is suggested in [2.230] to double the drain current density, as compared to the $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ structure.

The situation V 2B.) in Fig. 2.4 becomes very unlikely in this case, as the bandgap of the InGaN in the channel reduces with increasing y . Very high currents are predicted for these HFETs in [2.230] with maximum current levels beyond 4 A mm^{-1} . Technical realizations yield maximum drain currents of 0.4 A mm^{-1} , e.g., in [2.232]. High-saturated drain current levels of 1.33 A mm^{-1} have been reported in [2.84].

VI: $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{In}_z\text{Al}_{1-z}\text{N}$ Double Heterojunction HEMT on Arbitrary Buffer

The assumption of the growth on relaxed GaN buffer must be further modified for the growth on arbitrary substrates. Double heterojunction devices can be formed in the $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}$ material system. An $\text{In}_z\text{Al}_{1-z}\text{N}$ buffer will be grown on top of a substrate. The selection $z = 0.17$ yields a situation with the buffer lattice-matched to GaN. Arbitrary mole fractions yield the most complicated situation, i.e., a double $\text{In}_x\text{Al}_{1-x}\text{N}/\text{In}_y\text{Ga}_{1-y}\text{N}/\text{In}_z\text{Al}_{1-z}\text{N}$ heterojunction HEMT with three material compositions x , y , and z . The situation is similar to that of the AlGaN/GaN/AlGaN heterostructure device; however, as the two polarization components are antiparallel, more distinctions are necessary. The distinction yields a similar analysis for the material composition as in the case of a single heterojunction using InAlN grown on a GaN layer. However, the transition to any substrate is critical, as a second channel can form at the nucleation layer/InAlN buffer interface.

VII: $Al_x Ga_{1-x} N/GaN$ NPN-Single Heterojunction Bipolar Transistor

Polarization engineering in III-N HBTs is a secondary concern relative to the present severe issues like collector leakage due to the impact of dislocations, and processing issues, such as aggressive etch processes with subsequent surface damage increasing base ohmic contact resistance, e.g., [2.269, 2.283]. Material growth is, of course, of critical importance in the bipolar device; however, it is important, mostly with respect to mismatch reduction. Subsequent bandgap engineering requires the inclusion of the polarization effects [2.282], as their neglect would be misleading. A very simple AlGaN/GaN HBT can be grown using a thick GaN n-doped subcollector and a GaN n-doped collector on top of a substrate. A p-doped GaN base is added, as performed, e.g., in [2.383]. The emitter layer consists of $Al_x Ga_{1-x} N$ and typically reveals material compositions $x = 0.1$ [2.513]. The AlGaN emitter is typically capped with a GaN layer which is highly Si-doped, and the transition is either graded or abrupt. The GaN-base p-doping, typically Mg, is degenerate with nominal doping levels of $p \geq 10^{19} \text{ cm}^{-3}$, although the activation is relatively low, i.e., $\leq 10^{18} \text{ cm}^{-3}$. This is due to the high activation energy [2.382] of the deep acceptor Mg with $E_A - E_V \approx 170 \text{ meV}$. The growth at the base/emitter heterointerface will thus be Ga-face with a channel-like (donor-like) positive polarization charge at the emitter(AlGaN)/base(GaN) junction. This further results in a negative polarization (acceptor-like) charge at the graded AlGaN/GaN-Si interface near the top contact. Deduced from this, an additional electron barrier is created in the conduction band at the base/emitter junction and within the emitter grading. In [2.282], these additional peaks are flattened by smoothing the interface by material grading. This feature allows the prevention of hole injection into the emitter without hindering the electron transport. Several other issues will be discussed in the context of polarization engineering and its subsequent effects. The carrier lifetimes in the base at the GaN pn-junctions at different mobility levels are discussed in [2.141], yielding values between 24 and 240 ps. The impact of the polarization doping to the base layer is discussed in [2.23, 2.420]. Normal collector-down device/emitter up configuration see reduced p-doping for the Ga-face growth, while collector-up devices experience additional carrier concentration through polarization doping in the p-layers.

VIII: $GaN/In_x Ga_{1-x} N/GaN$ Double Heterojunction Bipolar Transistor (DHBT)

Due to the limited doping activation of Mg in GaN and to several other issues in AlGaN/GaN HBTs, GaN/ $In_x Ga_{1-x} N/GaN$ npn-DHBTs have been developed and successfully demonstrated, e.g., in [2.271]. Again, polarization engineering is only a secondary concern. The advantage of $In_x Ga_{1-x} N$ as a base material is caused by the increase of the p-doping activation, e.g., up to $7 \times 10^{18} \text{ cm}^{-3}$ as reported in [2.269]. This is based on the lower acceptor activation energies in p- $In_x Ga_{1-x} N$. The base layers are grown with a material composition of $0.17 \leq x \leq 0.25$ [2.311], yielding a doping activation of $4 \times$

10^{18} cm^{-3} . A double heterojunction is desirable due to the higher bandgap of GaN in the collector and the increased leakage current of a GaN/InGaN single heterojunction device, as mentioned in [2.269]. On the other hand, the conduction band spike at the collector/base interface has to be reduced, e.g., by material grading in the base towards the lower interface [2.269].

2.2.4 Analytical Calculation of Channel Charge Concentrations

For the calculation of the resulting charge at the heterointerface, the following interpolation formulae have been suggested in [2.22, 2.525], assuming no additional doping in the barrier and no surface effects apart from the interface under consideration:

$$n_{\text{sheet}} = \frac{\sigma(x)}{e} - \left(\frac{\epsilon_0 \cdot \epsilon(x)}{d_{\text{AlGaN}} \cdot e^2} \right) [e \cdot \phi_B(x) + E_F(x) - \Delta E_C(x)]. \quad (2.42)$$

Derived from (2.42), the maximum sheet carrier concentration of $6 \times 10^{13} \text{ cm}^{-2}$ at a GaN/AlN interface can be calculated [2.12]; however, it strongly depends on the degree of relaxation at the GaN/AlN interface. Recent HFET device examples with very high sheet carrier densities can be found in [2.68] using $\text{Al}_{0.34}\text{Ga}_{0.66}\text{N}/\text{GaN}$ HFETs which yield sheet carrier densities of $1.45 \times 10^{13} \text{ cm}^{-2}$. Fig. 2.5 gives the dependence of the sheet resistance and Fig. 2.6 of the 2D-sheet carrier concentration from the material composition at an $\text{GaN}/\text{Al}_x\text{Ga}_{1-x}\text{N}$ heterostructure interface presented in recent publications. The impact of both barrier thickness and substrate is neglected in Fig. 2.5 and Fig. 2.6. Further the insertion of doping and of an AlN interlayer is depicted, for details see Chapter 3. Fig. 2.5 suggests a statistically proven linear variation of the sheet resistance from 500 to $200 \Omega \text{ sq}^{-1}$. Fig. 2.6 shows a variation of the sheet carrier concentration of $7 \times 10^{12} \text{ cm}^{-2}$ for $x = 0.15$ to $1.6 \times 10^{13} \text{ cm}^{-2}$ for $x = 0.5$. At the same time, the influence of the additional n-doping in the barrier layers on the carrier concentration can be seen in Fig. 2.6, as discussed later. Both MBE and MOCVD provide similar charge concentrations as a function of the mole fraction.

2.2.5 Doping Issues

Independent of the impact of polarization as a source of carriers, bulk doping is of fundamental importance for the definition of material and device characteristics, as in any semiconductor. Review on the doping issues of III-N materials is supplied, e.g., in [2.87, 2.370, 2.437]. Some doping parameters are given in Table 2.25. III-N semiconductors are doped with impurities such as Si, Ge, Se, O, Mg, Be, and Zn. Typical unintentional impurities are C, H, O, and grown-in defects, such as vacancy and antisite point defects [2.417].

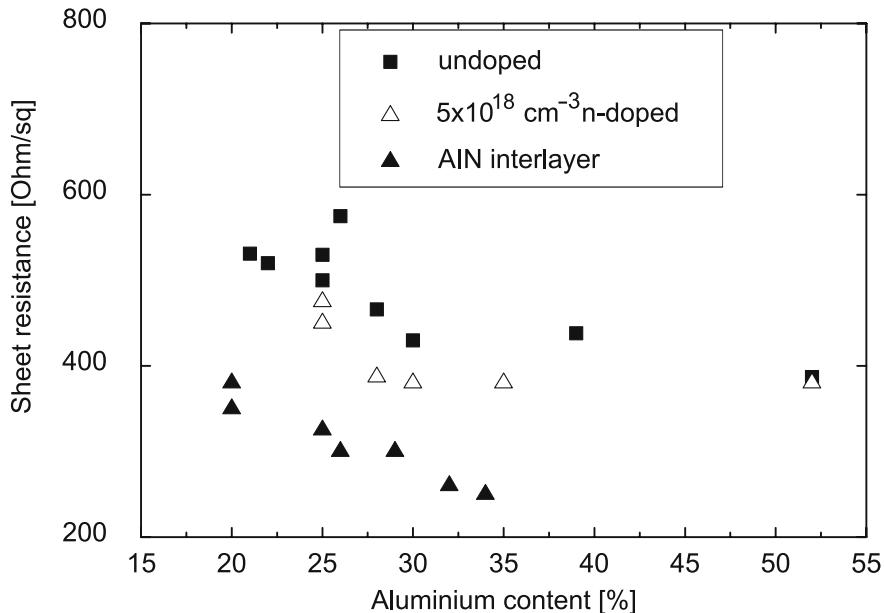


Fig. 2.5. Sheet resistance of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures as a function of aluminum content x

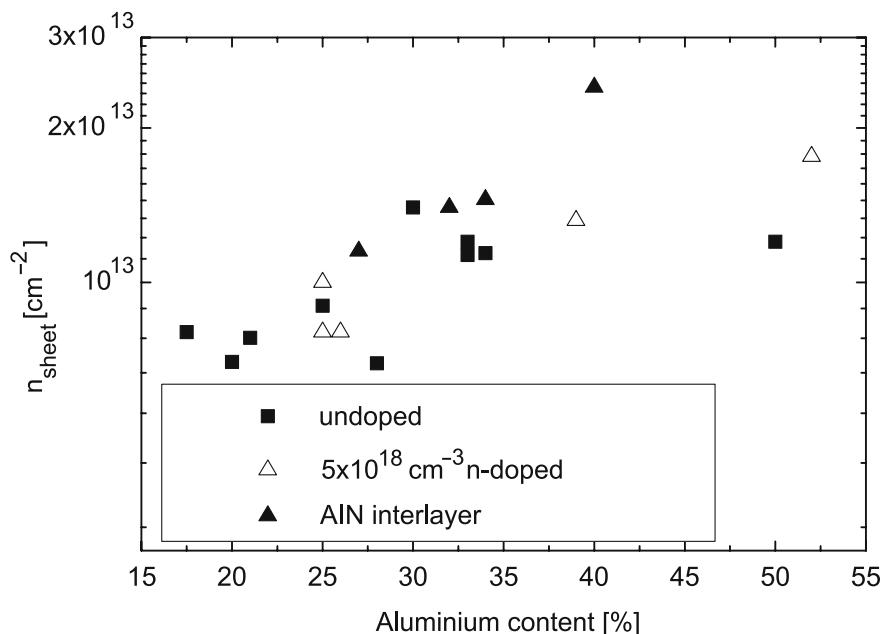


Fig. 2.6. Sheet carrier concentration in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures as a function of aluminum content x

N-Doping

In electronic devices, n-doping is of critical importance for δ -doped high-voltage HFETs and the definition of contacts in FETs and HBTs. NID-GaN is found to be typically n-type. This is caused by either nitrogen vacancies, Ga interstitials or oxygen incorporation depending on the growth method [2.351].

Silicon doping is the typical choice for intended n-doping. The activation energy of silicon in GaN is 5–9 meV which allows effective doping [2.351]. Apart from the polarization doping, silicon doping can serve as additional carrier source in the channel. Given the high-operation voltages, the stability of such silicon doping in the barrier layer is crucial, as δ -doping is affected by the field peaks in any HEMT.

P-Doping

The reduced performance of p-doping of GaN is the most critical issue reducing optoelectronic device performance in III-N materials. This includes diodes [2.322, 2.325, 2.432], laser diodes [2.326], and bipolar transistors [2.383] on the electronic side. The issues involve:

- High-contact resistances and nonohmic behavior at the base [2.383] due to:
 - Reduced current gain at RT due to high-thermal activation energy of Mg of 120–200 meV as an acceptor [2.225]
 - Reduced activation of Mg due to the formation of Mg–H during MOCVD growth
- Mg MOCVD reactor memory leading to soft pn-junction doping profiles and reduced confinement of p-doping to the base layer [2.383] for both MBE- and MOCVD-growth.

Photoluminescence measurements in Mg-doped GaN grown by metal organic vapor-phase epitaxy (MOVPE) are described, e.g., in [2.248]. An ionization energy of the acceptor of 173 meV is concluded. The bandgap narrowing for high doping concentrations is found to be in the order of 10 meV. For MBE growth, the following modifications are necessary:

- No Mg-reactor memory occurs
- Sharper doping profiling is possible

The maximum doping activation of Mg in GaN is thus of the order of $\leq 10^{18} \text{ cm}^{-3}$ at room temperature. More details with respect to the growth conditions will be given in Chapter 3.

2.2.6 Surfaces and Interfaces

Due to the aforementioned properties of III-N heterostructures, surfaces and interfaces require special attention in this book. The principal properties of the different interfaces shall be discussed here, while their technological realization is considered in Chaps. 3 and 4.

III-N/III-N Interfaces

Apart from the polarization effects already discussed in detail, several effects at a semiconductor/semiconductor interface occur, due to the change of the material or the material composition:

1. An energy alignment of the valence band and conduction band is observed.
2. Strain effects occur due to the modification of the lattice constants at the interface.
3. The interface is a preferred location for states, e.g., [2.160].
4. In III-N semiconductors, the differences in the polarization occur at the interface, leading to excess carrier concentrations.
5. Due to the quantization effects near the interface, transport occurs very close to the interface, which is especially true for the III-N materials due to the specific band structures.

The next paragraphs compile the enumerated issues.

Energy Alignment and Bandgap Energies

The energy alignment occurs in three different types of transitions in any semiconductor, e.g., [2.356]. The $\text{GaN}/\text{Al}_x\text{Ga}_{1-x}\text{N}$ semiconductor/semiconductor interface is a typeI interface. For both electrons and holes, energy barriers are formed in one direction. Thus channel or charge-accumulation areas can form, if the appropriate carriers are provided. The conduction band energy offset alignment of a ternary material $\text{A}_x\text{B}_{1-x}\text{N}/\text{CN}$ is described, e.g., for the $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ interface:

$$\Delta E_C(x) = 0.7 \cdot [E_g(\text{Al}_x\text{Ga}_{1-x}\text{N}) - E_g(\text{GaN})]. \quad (2.43)$$

The bandgap energy for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ as a function of material composition can be described as:

$$E_g(x) = x \cdot E_g(\text{AlN}) + (1 - x) \cdot E_g(\text{GaN}) + (1 - x) \cdot x \cdot C_{E_g, \text{AlGaN}}. \quad (2.44)$$

The bowing factor $C_{E_{\text{gap}}, \text{AB}}$ is already given in Table 2.21. The valence band offset energy ΔE_V is then determined accordingly from the following equation:

$$E_g(\text{Al}_x\text{Ga}_{1-x}\text{N}) = \Delta E_C + \Delta E_V + E_g(\text{GaN}). \quad (2.45)$$

The above relations can be generalized for several other material combinations $\text{A}_x\text{B}_{1-x}\text{N}/\text{C}_x\text{D}_{1-x}\text{N}$ in the III-N system. Table 2.24 summarizes the parameters for the energy alignment for the combinations in the III-N world. Overviews are given in [2.203, 2.429]. Table 2.24 gives the full summary of all parameters according to (2.43)–(2.45). The alignment of the ternary semiconductors depends critically on the bowing parameters of the bandgap, which are discussed in Table 2.21. The modifications of the bandgap energies due

Table 2.24. Parameters for energy alignment of the III-N binary and ternary interfaces at RT

Material	Interface type (-)	E_g (eV)	E_g (eV)	ΔE_C (eV)	ΔE_V (eV)	Ratio (-)	Ref.
AlN/GaN (Wz)	Type I	6.2	3.43	1.97	0.8	0.7/0.3	[2.11]
AlN/GaN (Zb)	Type I	5.1	3.38	0.92	0.8	0.53/0.47	[2.203]
InN/AlN (Wz)	Type I	0.77	6.2	3.62	1.81	0.66/0.34	[2.203]
InN/AlN (Zb)	Type I	0.75	5.1	3.31	1.04	0.76/0.24	[2.203]
InN/GaN (Wz)	Type I	0.77	3.43	1.61	1.05	0.6/0.4	[2.203]
InN/GaN (Zb)	Type I	0.75	3.38	1.58	1.05	0.6/0.4	[2.203]
GaN/Al _{0.2} Ga _{0.8} N	Type I	3.43	3.79	0.252	0.108	0.7/0.3	[2.230]
GaN/In _{0.17} Al _{0.83} N	Type I	3.43	4.7	0.66	0.61	0.52/0.48	[2.230]
In _{0.1} Ga _{0.9} N/ In _{0.17} Al _{0.83} N	Type I	3.03	4.7	0.868	0.801	0.52/0.48	[2.230]
GaN/In _{0.2} Ga _{0.8} N	Type I	3.43	3.58	0.09	0.06	0.6/0.4	[2.203]

to the different directions of the polarization at the interface and in quantum wells are discussed, e.g., in [2.498]. The energy levels in In_xGa_{1-x}N/GaN quantum wells are analyzed for thickness between 23 and 130 Å. By variation of the composition the energy levels can be adjusted to the needs of the application.

Bulk and Interface Traps

Typical trap energies and other defect properties observed experimentally at the heterojunctions and in the bulk are given in Table 2.25. Good overview of defects in bulk materials are given in [2.89,2.221,2.315,2.389,2.390]. The occurrence of traps is of critical importance. It is partly caused by the heteroepitaxy, i.e., the growth on nonnative substrates. As the wide bandgap properties are modified by these traps with activation energies in the range of conventional semiconductors, such as Si or GaAs, the breakdown properties are critically affected, i.e., reduced. Table 2.25 compiles typical trap parameters. At the interfaces, traps lead to the pinning of the Fermi-level, as is described in [2.160]. The pinning of the Fermi-level in GaN is found to be about midgap, which puts GaN in a similar situation as GaAs. Other reports suggest a Fermi-level pinning at $E_C - 0.5$ eV [2.250] due to nitrogen vacancies or at $E_C - 0.8$ eV due to oxygen. Further details are given below.

Strain in III-N Semiconductors

As is discussed with the polarization effects, strain is a very important parameter in the design of substrate semiconductor buffer. In addition, the lattice-mismatch among different semiconductor layers is important for the resulting material quality and crystal stability. Table 2.26 compiles the lattice constants a_0 and the resulting lattice-mismatch along a_0 between the various III-N mate-

Table 2.25. Trap and doping parameters in III-nitride materials

	Doping	Energy (eV)	Donor	Ref.
GaN	n	$E_C - 0.44$	–	[2.490]
GaN	n	$E_C - 0.5$	–	[2.250]
GaN	n	$E_C - 0.005$	Si	[2.351]
GaN	p	$E_V + 0.22$	Mg	[2.350, 2.475]
GaN	p	$E_V + 0.23$	C	[2.350]
GaN	p	$E_V + 0.25$	Be	[2.350]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.017$ ($x = 0$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.054$ ($x = 0.18$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	n	$E_C - 0.090$ ($x = 0.6$)	Si	[2.351]
$\text{Al}_x\text{Ga}_{1-x}\text{N}$	p	$E_V + 0.4$	Mg	[2.475]

Table 2.26. Lattice constant a_0 (matrix diagonal) and mismatch for the III-N binary materials at 300 K

Material	GaN (Å)(%)	AlN (Å)(%)	InN (Å)(%)	SiC (Å)(%)	Sapphire (Å)(%)	Silicon (Å)(%)	Ref.
GaN (sub.)	3.189	2.3	10.6	3.3	14.8	–	[2.449]
AlN (sub.)	2.4	3.119	12	1.0	12.5	–	[2.323]
InN (sub.)	10.6	12	3.5446	14	25.4	–	[2.323]
SiC (sub.)	3.3	1.0	14	3.081	–	–	[2.323]
Sapphire (sub.)	14.8	12.5	25.4	11.5	2.777 (4.758)	–	[2.323]
Silicon (sub.)	16.9	18.7	7.6	–	–	3.84 (5.431)	[2.419]

rials and substrates. The lattice-mismatch is calculated according to

$$f_c = \frac{a - a_0}{a_0}. \quad (2.46)$$

For SiC substrates, the lattice-mismatch is calculated from the lattice constant a . For silicon and sapphire the calculation needs some explanation. Silicon is a well investigated material and only the III-N-relevant parameters shall be given. GaN can be grown in the hexagonal phase on the 111-plane of the silicon. In this case the effective lattice constant of 3.84 Å can be used. For sapphire, the growth is along the 0001-direction. This leads to an effective constant of 2.77 Å. Applying the rules of Matthews and Blakeslee [2.280] or Fischer [2.11] for the pseudomorphic growth of III-N materials, the critical thicknesses given in Table 2.27 are obtained for the semiconductor/semiconductor transitions. Table 2.27 gives estimates of the critical thickness for typical material compositions. $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ can only be grown with a thickness of 20 nm on top of fully relaxed GaN. The less conservative calculation approach of Fischer [2.115] leads to a critical thickness of 40 nm for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$. Thus AlGaN relaxation can occur for the composition $0 \leq x \leq 0.4$ for thicknesses

Table 2.27. Critical thicknesses obtained by various methods

Material	Thickness (nm)	Method	Ref.
Al _{0.2} N _{0.8} N on GaN (sub.)	20	calc. (MB)	[2.11]
Al _{0.2} N _{0.8} N on GaN (sub.)	40	calc. (Fischer)	[2.11]
AlN on GaN (sub.)	2.9	measured	[2.199]
In _{0.1} Ga _{0.9} N on GaN (sub.)	10	calc. elastic	[2.146]
In _{0.17} Al _{0.83} N on GaN (sub.)	∞	—	[2.231]
In _{0.27} Ga _{0.77} N on GaN (sub.)	15	calc. (Fischer)	[2.231]

MB Matthews/Blakeslee

of up to 30 nm in AlGaN barriers grown on GaN. In_xAl_{1-x}N can be grown lattice-matched on GaN for $x = 0.17$. The critical thickness of In_{0.1}Ga_{0.9}N on GaN is 10 nm. This leaves ample opportunities for heterostructure design.

III-N/Dielectric Interfaces

The physical nature of the III-N semiconductor surfaces toward vacuum, gases, liquids, or any dielectric material determines device performance to a high extent. A key property of GaAs materials as compared to silicon-based device technology is the lack of an unpinned GaAs/oxide interface [2.117, 2.118]. Similar surfaces prevail for III-N devices with SiN. For GaN, a Fermi-level pinning close to a midgap energy level is described in [2.483]. Using SiO₂ as a dielectric, the interface GaN/SiO₂ is found to have a very low surface charge density, as reported in [2.276, 2.277]. For the Al_{0.24}Ga_{0.76}N surface, experimental evidence for the Fermi-level pinning is found in [2.154, 2.160]. The underly-

Table 2.28. Fermi-level (surface potential) energies of III-N semiconductors at vacuum and dielectric interfaces

Material	Surface potential (eV)	Ref.
n-GaN/Vacuum	$E_C - 1.2$	[2.303]
n-GaN/Vacuum	$E_C - 2.8$	[2.477]
n-GaN(Si)/Vacuum	$E_C - 1.5, E_C - 0.2$	[2.205]
GaN/SiN	$E_C - 2.4$	[2.82]
GaN/Si ₃ N ₄	$E_C - 0.27$	[2.25]
GaN/SiO ₂	$E_C - 0.13$	[2.25]
Al _{0.34} Ga _{0.66} N/Vacuum	$E_C(\text{Al}_{0.34}\text{Ga}_{0.66}\text{N}) - 1.65 \text{ eV}$	[2.154]
Al _{0.24} Ga _{0.76} N/Vacuum	$E_C(\text{Al}_{0.24}\text{Ga}_{0.76}\text{N}) - 1.6 \text{ eV}$	[2.160]
Al _{0.35} Ga _{0.65} N/Vacuum	$E_C(\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}) - (1.4 \text{ to } 1.7 \text{ eV})$	[2.209]
GaN/Al _{0.35} Ga _{0.65} N/Vacuum	$E_C(\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}) - (1.4 \text{ to } 0.6 \text{ eV})$	[2.208]
In _{0.3} Ga _{0.7} N/Vacuum	$E_C(\text{In}_{0.3}\text{Ga}_{0.7}\text{N})$	[2.247, 2.477]
InN/Vacuum	$E_C(\text{InN}) + 0.6 \text{ eV}$	[2.477]

ing data are obtained by synchrotron radiation photoemission spectroscopy (SRPES). Table 2.28 compiles available surface and interface data. Due to the more ionic bond between gallium and nitrogen relative to more covalent semiconductors such as GaAs and InP, the pinning or Fermi-level stabilization at the surface should be less pronounced, as argued in [2.429]. However, several reports exist on the stabilization of the Fermi-level for GaN, $\text{Al}_x\text{Ga}_{1-x}\text{N}$, and InN [2.154, 2.160].

III-N/Metal Interfaces

The properties of III-N/metal interfaces are essential for the performance of nearly all device applications.

N-type Ohmic Contacts

The formation of ohmic contacts is a fundamental component in the fabrication of semiconductor devices. For n-contact in III-N, intrinsic doping is the most important contender for reducing the contact resistance. Due to the wide bandgap properties, the typical contacts yield special formation properties such as high-annealing temperatures between 500°C [2.197] and 900°C [2.31]. Special geometric definitions, such as recessed ohmic contacts [2.198] or non-alloyed implanted contacts [2.526], have been suggested. At the same time, good ohmic contacts are also more easily achieved for III-N semiconductors, due to the high sheet carrier density at the interface, due to both the impact of polarization or due to impurity doping, especially using silicon.

P-type Ohmic Contacts

P-contacts are very well investigated due to their fundamental importance in the field of optoelectronics, e.g., in [2.325]. P-contacts issues prevail due to both the reduced doping activation and deep activation energies relative to the valence band. These properties of p-doping limit the performance of optoelectronic devices, which is one reason for the great number of publications on this topic. Detailed overview data in this book are given in Chapter 4.3.1.

Schottky Contacts

The formation of Schottky contacts on III-N semiconductors is a very critical capability for two reasons. First, wide bandgap FETs are required to support very high fields because of the high operation voltages required, while the semiconductor/metal transitions form Schottky interfaces with barrier heights of ≤ 1.5 eV. Second, for high-power applications, the Schottky contacts are subject to the very high channel lattice temperatures $\geq 300^\circ\text{C}$. Thus, Schottky contacts currently form a weakpoint within the semiconductor device architecture, especially with respect to reliability. Further overview data are given in Chapter 4.3.2.

2.2.7 Transport Properties in Polarized Semiconductors

The polarization effects at the interface favor very strong quantization effects. The transport properties in this highly quantized situation [2.421] will be discussed again in this section.

Monte Carlo Simulations

Long before the realization of advanced GaN HEMTs, which allow the extraction of high-speed properties, a large number of predictions have been made, especially by ab-initio calculations or by Monte Carlo simulations based on these calculations [2.492]. Initial electron mobilities of GaN, InN, and AlN are calculated by variational principle in [2.64]. Initial MC simulations of the velocity-field characteristics in bulk wurtzite-phase GaN are presented in [2.37]. They predict a maximum electron velocity of $3.1 \times 10^7 \text{ cm s}^{-1}$ and a saturation field of 150 kV cm^{-1} at room temperature. The analysis is performed between 77 and 1,000 K. Simulations of the transient transport in GaN and InN are given in [2.121]. Most of the initial simulations mentioned so far do not consider the interaction of the electrons with longitudinal and transversal optical phonons correctly [2.19, 2.517], and further, in the case of InN, use the bandgap of 1.89 eV at RT, e.g., [2.348]. Fig. 2.7 gives the comparison of simulated and measured velocity-field characteristics of GaN. The data in Fig. 2.7 are taken from [2.37, 2.121]. Additionally, Fig. 2.7 depicts experimental

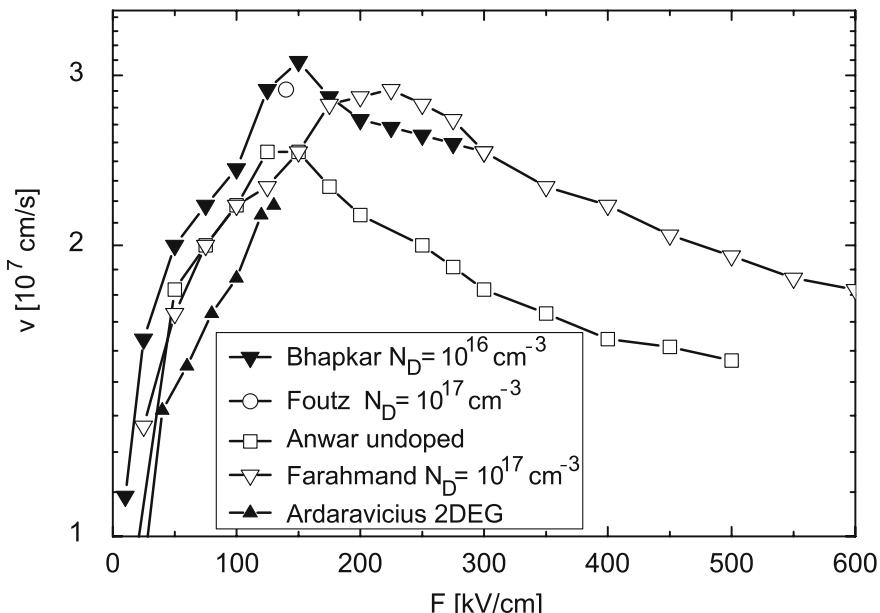


Fig. 2.7. Simulated velocity-field characteristics in bulk GaN by various authors

data of an AlGaN/GaN DEG which includes the interaction of the nonequilibrium phonon taken from [2.19]. Hot phonons and hot-electron penetration into AlGaN and GaN layers are responsible for the lower than expected drift velocity. Ensemble Monte Carlo calculations within the density functional theory of GaN and ZnS are given in [2.119]. Ab-initio band structure calculations are used. These simulations propose both lower peak velocities and no occurrence of the Gunn effect in GaN. Device simulations for heterostructures including the quantization effects in the channel are given in [2.46]. The saturation velocity used is as low as $1.2 \times 10^7 \text{ cm s}^{-1}$. The electron relaxation time amounts to 0.1 ps for all materials. Very good agreement of measured velocities and MC simulations can be obtained [2.30], as also given in Fig. 2.7. Measured saturation velocities of $2.5 \times 10^7 \text{ cm s}^{-1}$ and a critical field at 180 kV cm^{-1} are found for n-type bulk GaN. Peak velocities v_{peak} of $3.1 \times 10^7 \text{ cm s}^{-1}$ at an electric field of 140 kV cm^{-1} are reported for AlGaN/GaN heterostructures. The obvious contradiction of several measurements and simulations will be discussed in the next section.

Velocity Measurements

Bulk and HFET MC simulations are not easily verified by experiment due to the sub-micron gate situation in FETs, the heterointerface situation in HFETs, and the strong field gradient near the gate [2.375]. Time-resolved electroabsorption measurements of the velocity-field characteristics in a bulk GaN pin-diode are presented in [2.500]. A time-of-flight technique is used. They predict a maximum electron velocity v_{peak} in bulk GaN of $1.9 \times 10^7 \text{ cm s}^{-1}$ and a saturation critical field of $E_{\text{crit}} = 225 \text{ kV cm}^{-1}$. The measured peak velocity v_{peak} is still slightly lower than the prediction of the MC analysis. Other extraction techniques lead to stronger deviations. Derived from delay time analysis of HFETs, the maximum effective electron velocity in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs, i.e., the quantized channel situation, with $l_g = 1.3 \mu\text{m}$ is found to be $1.2 \times 10^7 \text{ cm s}^{-1}$ in [2.5]. This is lower than the prediction of the MC simulations. Further extractions suggest that parasitic effects mask the real experimental effective velocity of $3.3 \times 10^7 \text{ cm s}^{-1}$ in a channel of AlGaN/GaN HFETs [2.42], which is found when considering the parasitic effects. Without the consideration of R_S and R_D , an effective velocity of $1.3 \times 10^7 \text{ cm s}^{-1}$ is extracted. The influence of charge control (charge nonconfinement or real-space transfer) at the heterostructure interface on carrier velocity is described in [2.462]. The source resistance R_S is found to be modulated in a nonlinear physical model. This modulation at high forward current I_D is correlated with the occurrence of space charge regions and carrier nonconfinement from the channel to the barrier under the source contact. Determination of quantum scattering lifetimes by Shubnikov-de Haas oscillations and parallel conduction are given in [2.409]. A ratio of the classical scattering time to the quantum scattering time of 6.1/1 is observed. This ratio indicates what proportion of the lifetime is represented by large angle scattering vs. all

scattering events. The typical range found for the ratio for GaAs heterostructures is in the range 9–13 [2.409]. The results suggest that in addition to the optimization of the channel layers, also the parallel conduction in doped barrier layers has to be taken into account. With these considerations, all effects have been mentioned, which explain the inconsistency of measurements and simulations.

2.2.8 Polarization-Based Devices and Their Specific Properties

The strong polarization effects in III-N materials allow a number of special devices which are unique with respect to their properties. The first unique device is, of course, the classical III-N heterostructure FET, which yields extremely high channel carrier concentrations, even though there is no intentional impurity doping. For regular AlGaN/GaN HEMTs, the direct effects of spontaneous and piezoelectric polarization effects on the output characteristics of AlGaN/GaN HEMTs are discussed in [2.391]. The polarization critically influences the channel formation and thus also the output characteristics. The advantage of this paper is to show the direct correlation between device properties and polarization effects.

The high-dielectric constant of piezoelectric layers grown on top of a non-piezoelectric substrates can be effectively used in other electronic devices [2.338]. AlN [2.55] and GaN [2.242] surface-acoustic-wave (SAW) filters using the piezoelectric properties have been demonstrated. Epitaxially grown GaN piezoelectric thin-film SAW filters are grown on amorphous GaN buffers on sapphire. The low surface roughness of the material ensures good wave propagation while the good isolation between the electrodes ensure low electric losses. High-wave propagation velocities of $5,800\text{ m s}^{-1}$ and low insertion loss of -7.7 dB are achieved [2.242]. The devices provide high fractional bandwidth and very low coefficients of frequency are obtained. Voltage controlled SAW filters on 2DEG AlGaN/GaN heterostructures are demonstrated in [2.129]. The external voltage applied to transducer is used to minimize the insertion losses in this case. This technology is suggested for cointegration with GaN MMICs. Further sensor devices are discussed with the applications at the end of this chapter.

2.3 Electrical and Thermal Limitations of Materials and Devices

Several predictions are being used to estimate the ultimate performance of nitride-based materials and devices. This section summarizes the most important figures-of-merit used in the analysis to predict the ultimate performance for fully developed device technologies.

2.3.1 Physical Modeling of Devices

Nearly all available simulation approaches have been used to model and predict the performance of III-N semiconductors and semiconductor devices. These include basic material research to obtain the band structure by density functional approaches [2.119], basic transport considerations to perform MC simulations [2.517], device drift-diffusion, and hydrodynamic multidimensional modeling approaches [2.46, 2.48], Monte Carlo approaches for both materials and devices [2.15, 2.111], as well as compact device modeling approaches [2.183, 2.392].

Material Modeling for Polar Devices

Material modeling from basic properties to devices is described, e.g., in [2.49, 2.111]. The complexities that arise in Monte Carlo-based modeling of noncubic symmetry semiconductors and their related devices are discussed in [2.50]. Owing to the increased size and number of atoms per unit cell, the band structure is far more complex in noncubic than in zincblende-phase semiconductors. This leads to a greater number of bands, smaller Brillouin zone, and an increase in the number of band intersections. Example articles are provided in [2.15, 2.49, 2.111, 2.492]. The detailed material properties have already been discussed in this chapter.

Device Simulation Including Polarization Effects

III-N device simulation is not very different from approaches in other semiconductor systems [2.406]. A quasi-2D-modeling of GaN-based heterostructure devices including quantum effects is given in [2.392]. An optimized effective mass-approach is coupled to a quasi-2D-model for the current flow. The PICs are included as surface charge in the Poisson equation which is solved self-consistently with the Schrödinger equation. The idealized model predicts very high drain currents of 2.5 A mm^{-1} for an $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ HEMT. On the HFET device level, full band Monte Carlo simulation of zincblende GaN MESFETs, including realistic impact ionization rates, are provided in [2.110]. The drain current in GaN MESFETs increases gradually with drain voltage V_{DS} . This is different from the impact ionization in GaAs MESFETs and it is related to the different impact ionization coefficients. Gate length scaling for $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}/\text{GaN}$ HFETs by 2D-full band MC simulation including polarization effect is analyzed in [2.15]. The polarization effects are included by constant interface charges at the barrier ($-\sigma$) and channel interface ($+\sigma$). From this, a cut-off frequency \times gate length product $f_T \times l_g$ of $16 \text{ GHz } \mu\text{m}$ can be deduced for a device with a gate length of 100 nm. The maximum predicted output power P_{out} amounts to 46 W mm^{-1} for a gate length $l_g = 0.9 \mu\text{m}$, and 20 W mm^{-1} for a 100 nm device. The simulated on-state breakdown voltages are 300 and 60 V, respectively. Several other approaches have been described to include strong polarization effects in device simulation. The

carrier-concentration-dependent electron mobility in an AlGaN/GaN electron gas is analyzed by magnetoresistance and capacitance-conductance analysis in [2.185]. The effects of quantization are included in the mobility analysis. Scattering from interface states in AlGaN/GaN heterostructures is correlated with the high polarization field in the heterointerface. At temperatures higher than 200 K polar optical phonon scattering dominates the transport, yet both interface charge and roughness affect the mobility at the low and high sheet carrier density. For the compact models, a detailed physically based compact HFET model which includes thermal effects is given in [2.6]. The gradual channel approximation is used based on parameters on MC simulation. The thermal compression of a AlGaN/GaN device on sapphire substrate can be modeled very accurately. A theoretical study of GaN/AlGaN HEMTs by a compact model including a nonlinear formulation of the polarization is given in [2.527]. The cut-off frequency, transconductance, and current–voltage characteristics are computed in good agreement to measurements. The effect of the nonlinear polarization model on the sheet carrier density is also presented. An electrothermal Monte Carlo method is used for the investigation of submicrometer GaN HEMTs in [2.393]. The polarization effects are included according to (2.19). Additionally, fixed negative charges can be included to simulate surface traps. Peak velocities of $6 \times 10^7 \text{ cm s}^{-1}$ are reached at the drain side of the gate for a gate length $l_g = 200 \text{ nm}$. The maximum electron energies are as high as 2 eV.

Devices: Field Shaping and Breakdown Management

In addition to basic evaluation studies such as the comparison of zincblende-phase GaN, cubic-phase SiC, and GaAs MESFETs using a full band MC simulator [2.492], field shaping [2.183] and high-breakdown design are the principal applications of device simulations [2.358]. Such approaches allow the estimation and increase of maximum breakdown voltage BV_{DS} , and thus of the maximum output power P_{out} . Examples can be found [2.418, 2.465]. The impact of strain engineering on device level is stressed in [2.47]. Two findings are stressed: first, there are little changes in the DC- and transient-characteristics even for large stresses in overlayers. This is based on the stiffness of nitride semiconductors. A second finding focusses on the relaxation of the AlGaN. Piezoelectric polarization effects are more pronounced for devices with larger relaxation. Electric field shaping is presented in [2.358] for an AlGaN/GaN HEMT using field plates. The geometry of a field plate is optimized for reduced field peaking in the channel by 2D-simulation. A closed-form expression for the drain voltage dependence of the electric field using field plate is discussed in [2.183]. Direct analysis of the reverse gate leakage current I_G is provided by 2D-simulation in [2.182]. The mechanisms of direct tunneling, direct tunneling through a thin layer, and trap-assisted tunneling are distinguished by their field sensitivity. This allows to fit measured gate currents for various devices by 2D-simulation.

2.3.2 Devices: Figures-of-Merit

Apart from more specific simulation approaches, the prediction of the ultimate performance of semiconductor devices has a long-standing tradition. A great number of predictions are available for the promising material system of III-N semiconductors. Instead of repeating these various predictions, see, e.g., [2.301, 2.396, 2.462, 2.463], this work systemizes the figures-of-merits (FOMs) and calculates some principal dependencies. A good overview and comparison of different approaches is also given in [2.72].

Early initial predictions for wide bandgap compound semiconductors for superior high-voltage unipolar power devices are given in [2.415]. As given in (2.47), Johnson's FOM describes the power frequency product per unit width [2.167]:

$$\text{FOM}_{\text{Johnson}} = \frac{(v_{\text{sat}} \cdot E_{\text{crit}})^2}{2\pi}. \quad (2.47)$$

In (2.47), E_{crit} denotes the critical dielectric breakdown field and v_{sat} the effective saturation velocity of the material. A more microwave-oriented FOM is provided by Eastman in [2.132]. It combines microwave power, e.g., at 10 GHz, with the transit frequency f_T and the capacitive input reactance X_c [2.132], and the saturation velocity, as given in (2.48) [2.97]:

$$\text{FOM}_{\text{Eastman}} = P_{\text{out}}(\text{Class-A}) \cdot f_{10 \text{ dB}} \cdot R_L = 1.210^{23} \text{ W Hz}^2 \Omega. \quad (2.48)$$

$P_{\text{out}}(\text{Class-A})$ is the maximum output power in Class-A operation, $f_{10 \text{ dB}}$ is the maximum frequency yielding 10 dB of power gain, and R_L is the load impedance. This FOM is dedicated to the analysis of devices for the most important applications in high-power high-efficiency amplifiers. Wu [2.502] stated Baliga's FOM [2.26] as an efficiency measure for GaN HEMTs:

$$\text{FOM}_{\text{Baliga}} = \mu \cdot E_{\text{crit}}^2, \quad (2.49)$$

where again E_{crit} denotes the critical dielectric breakdown field and μ denotes the carrier mobility. High-efficiency devices have high-breakdown voltages (high E_{crit}) and low-access resistances (high mobility μ). The access resistances of III-N devices are typically higher, while the critical fields are significantly higher than in other fast semiconductors. This allows for efficient devices. Another FOM suggests maximizing the product of charge density n_{channel} and mobility μ to maximize gain and eventually, the current gain cut-off frequency f_T :

$$\text{FOM}_{\text{Gain}} = \mu \cdot n_{\text{channel}}. \quad (2.50)$$

Derived from this the channel charge density n_{channel} itself can also be maximized, as given in (2.51):

$$\text{FOM}_{n_{\text{channel}}} = n_{\text{channel}}. \quad (2.51)$$

Derived from (2.51), III-N HEMTs have a tremendous advantage in sheet carrier density as compared to other materials, while the absolute amount

Table 2.29. Properties relevant for low-noise applications for different HEMTs with a gate width $W_g = 2 \times 60 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$

Material (-)	$N_{F,\min}$ at 10 GHz (dB)	G_{ass} at 10 GHz (dB)	BV_{DS} (V)	FOM_{LNA}	Ref.
GaAs PHEMT	0.5	14	6	168	[2.474]
InAlAs/InGaAs HEMT	0.3	16	4	213	[2.335]
AlGaN/GaN HFET	0.6	12	50	1,000	[2.220]

of carriers in the channel is not considered. Further, both (2.50) and (2.51) do not consider any breakdown issues, so an optimization only according to these FOM can be misleading, as the optimization may deteriorate breakdown, e.g., due to on-state channel breakdown. Fig. 2.8 illustrates Johnson's FOM, whereas Fig. 2.9 shows the channel Hall mobility versus charge carrier density as compared to values reported in the literature. As can be seen III-N HEMTs provide much higher sheet carrier densities for similar mobility values, as compared to GaAs HEMTs. A FOM from a thermal point of view is provided by Shenai et al. in [2.415]:

$$\text{FOM}_{\text{Shenai}} = \kappa_L \cdot \sigma_A E_{\text{crit}}. \quad (2.52)$$

In this case, κ_L is the thermal conductivity of the material in the heat-flow path (both semiconductor, substrate, and appropriate transition), σ_A is the electric drift-region-conductance per unit area in the semiconductor, and E_{crit} is the dielectric breakdown field. In terms of heat conductivity and conductance per unit area, III-N materials such as GaN and AlN are in the same order as Si, while the peak electric field at breakdown is significantly higher for III-N materials. For low-noise applications, the following FOM can be used, as defined by Nguyen in (2.53):

$$\text{FOM}_{\text{LNA}} = \frac{G_{ass} \times BV_{DS}}{N_{F,\min}}. \quad (2.53)$$

Table 2.29 compares the minimum noise figure $N_{F,\min}$, the associated gain G_{ass} , and the breakdown voltage BV_{DS} for a heterojunction FET with a gate width $W_g = 2 \times 60 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$. In this comparison, the linear impact of the breakdown voltage in (2.53) favors the AlGaN/GaN HEMT very much, while the actual low-noise performance is not outstanding. This FOM is thus suitable for applications which require both low-noise performance and extreme robustness.

2.3.3 III-N Devices: Frequency Dispersion

AlGaN/GaN HEMTs are found to be highly frequency-dispersive and did not yield the expected output power, especially in the beginning of device development, e.g., in [2.206]. Newer publications, e.g., [2.219], announced

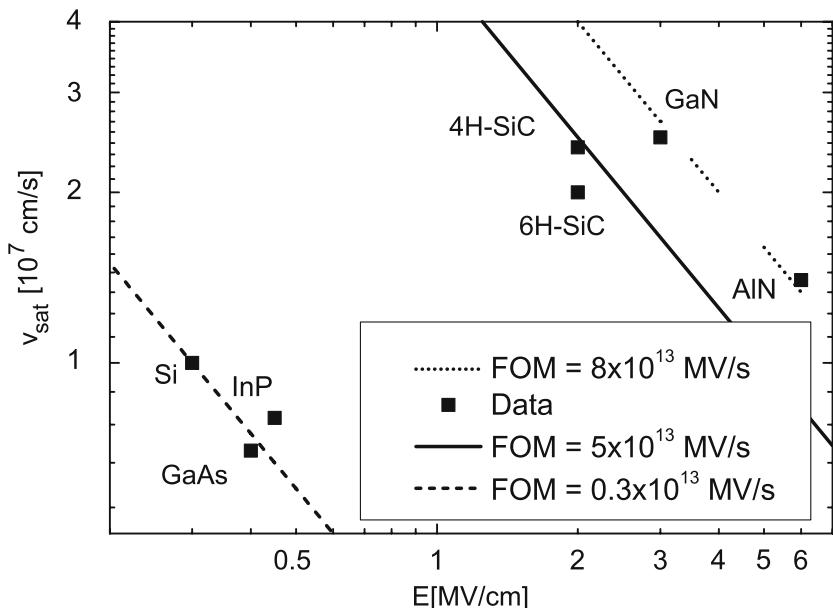


Fig. 2.8. Johnson's figure-of-merit in the E_{crit} vs. v_{sat} diagram

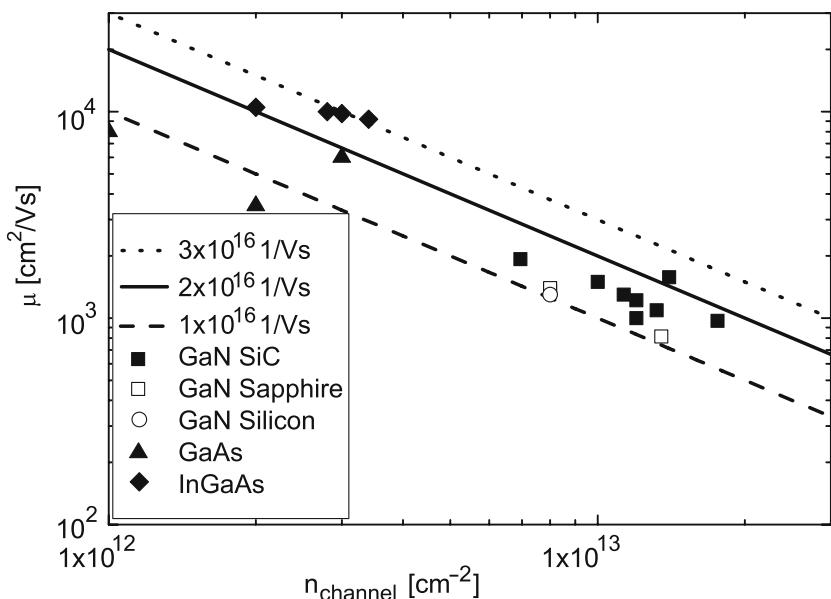


Fig. 2.9. Channel Hall mobility as a function of sheet charge carrier density n_{sheet} in GaN, GaAs, and InGaAs

dispersion-free devices and have to be taken with some caution; however, a lot of knowledge has been acquired for the reproducible control and reduction of dispersion. These results are discussed in more detail in Chapter 4. The aspect of performance degradation through dispersion, as described later, can be taken further. Related reliability issues are analyzed in Chapter 7.

Properties of GaN Semiconductors in Favor of Dispersion

One could ask why dispersion effects are so much correlated with III-N devices. In the GaAs and InGaAs material systems, frequency dispersion has been discussed in detail [2.51] but has not been found that crucial relative to the performance actually expected. In comparison to GaAs MESFETs, to (In)GaAs HEMTs, and other related devices, the physical origins of frequency dispersion in III-N HEMTs are more pronounced due to:

- Very high surface charge densities $n_{\text{sheet}} \geq 10^{13} \text{ cm}^{-2}$
- Lattice-mismatch of semiconductor materials relative to the heterosubstrates
- The relatively high concentration of threading dislocations and other defects due to high epitaxial growth temperatures up to 1,100°C and high growth temperature gradients within the growth process
- The small absolute channel charge relative to the overall possible carrier charge in the whole device including buffer and nucleation layers

In the III-N material system vertical instead of lateral devices have also been realized, such a current aperture vertical electron transistors (CAVETs), e.g., in [2.516], which show reduced dispersion relative to the lateral devices, such as GaN MESFETs and HEMTs.

Observation of Dispersion

In a large number of publications, the following experimental findings are attributed to frequency dispersion; see, e.g., [2.206, 2.480, 2.535]. These include:

- Current collapse; i.e., the difference of continuous-wave (cw) currents measured from different quiescent bias, or a pronounced negative output conductance, which occurs even in devices with small gate width and is not primarily caused by thermal effects [2.336, 2.480]
- DC-current dispersion; i.e., the difference of cw-DC- or pulsed-DC from different quiescent bias [2.480, 2.483]
- Time dependence of the DC-device currents with time constants and related frequencies between the Hz and 100 MHz range [2.209, 2.483]
- RF-current slump; i.e., the difference of DC- and extracted RF-device current characteristics
- A (bias-dependent) shift of the threshold voltage
- RF-power slump; i.e., the reduction of the output power caused by RF-current slump [2.206]

- Premature power and gain compression [2.130]
- Gain reduction through a second virtual gate and thus possible gate length extension

The effects are certainly related, e.g., the RF-power slump in this enumeration is caused by the RF-current slump, i.e., reduction of $I_{DS,RF}$. The above-mentioned current reduction effects intermix with device degradation mechanisms. The suppression of dispersive effects is analyzed in Chapter 3 and Chapter 4. Further, the impact on performance issues and modeling of dispersion is discussed in Chapter 5 and the degradation-related issues are discussed in Chapter 7.

2.4 Substrates for Electronic Devices

Wide bandgap semiconductor substrates are components critical to the system electronics industry. The availability of affordable, freely available, large-diameter, high-quality substrates will heavily influence the final system introduction of wide bandgap devices and MMICs into systems. Good overview articles on the present status are available, e.g., in [2.9, 2.41].

2.4.1 Criteria for Substrate Choice

The following properties of substrates are evaluated in this book:

- Lattice-mismatch relative to the materials of the device layers
- Thermal conductivity κ_L and coefficient of thermal expansion (CTE)
- Maximum electrical isolation (at different temperatures)
- Price and price per area [2.41]
- Availability with respect to diameter (2–8 in.)
- Crystal quality and residual defect density [2.103]
- Surface properties and residual defects density [2.267]
- Wafer warp and wafer bowing [2.341]
- Mechanical and chemical properties with respect to thinning and viahole etching

Table 2.30 gives an overview of the most important physical properties of the substrate materials under consideration for III-N devices. These include lattice-mismatch, thermal conductivity, CTE, and isolation. Some aspects of Table 2.30 are discussed in detail. GaN is a very suitable substrate material choice; however, neither conducting nor semi-insulating GaN substrates are so far available in sufficient diameter and quality [2.106, 2.328]. Some promising results are mentioned in [2.384, 2.385]. GaN substrates can be either produced by growth on a foreign substrate or by a boule growth technique. 3-in. GaN grown by HVPE on sapphire substrates are reported in [2.80]. The situation is similar for AlN, which has also a very good thermal conductivity [2.404]. The thermal conductivity of SiC is outstanding. Due to growth conditions

Table 2.30. Basic properties of substrate and III-N semiconductor materials

Material	Lattice constant a (Å)	Mismatch to GaN (%)	κ_L (W m ⁻¹ K ⁻¹)	CTE (10 ⁻⁶ K ⁻¹)	Isolation (Ω cm)	Ref.
GaN	3.189	0	130	5.59	$\geq 10^9$	[2.341, 2.384]
6H SiC	3.08	3.4	490	4.2	$\geq 10^{11}$	[2.341, 2.384]
6H s.i. SiC	3.08	3.4	370	4.2	$\geq 10^{11}$	[2.341, 2.384]
Sapphire	$4.758/\sqrt{3}$	13	50	7.5	—	[2.123]
Silicon	5.4301	17	150	3.59	$1\text{--}3 \cdot 10^4$	[2.341]
AlN	3.112	1	200	4.2	$\geq 10^{12}$	[2.341, 2.384]

and potential doping, the thermal conductivity of semi-insulating (s.i.) SiC can be reduced relative to pure crystalline SiC. The suitability of sapphire is strongly reduced due to its low thermal conductivity. All other substrate options except sapphire have a better thermal conductivity than GaN. Sapphire, even if thinned to 50 μm, reduces the reported power densities of devices in cw-operation to values of GaAs PHEMTs, e.g., in [2.16]. The difference in CTE of substrates and semiconductor materials affects both material growth and device reliability, because of the strain in the material. The maximum substrate isolation will further define the need to grow additional insulating semiconductor layers in the device. This will affect the attenuation of passive lines. For AlN, GaN, and SiC, the isolation has been developed to levels $\geq 10^9 \Omega \text{ cm}$ at RT. Once the epitaxial layers are grown, one of the most critical consequences of the lattice-mismatch is the resulting bow of the wafer. Based on the data given in Table 2.30, an approximative scaling rule for the wafer bow is suggested in [2.341]:

$$W \approx t_{\text{sem}} \cdot d_{\text{sub}}^2 / t_{\text{sub}}^2. \quad (2.54)$$

Equation (2.54) formulates a relationship between the substrate diameter d_{sub} , the epitaxial layer thickness t_{sem} , and the substrate thickness t_{sub} based on a given bow, known, e.g., for given substrate and epitaxial thicknesses, and diameter. For a typical thickness of up to 4 μm for the epitaxial layers and a 2-in. wafer of a given thickness, a bow of 10 μm results. For a 4-in. wafer of the same thickness, this results in a bowing of 40 μm, which is close to the maximum tolerances of an optical stepper, as mentioned in [2.341]. This is mentioned here, as the bowing has to be accounted for during gate alignment and with respect to the mechanical stress during backside processing. The issues of properties, present availability, and crystal quality are discussed in the next sections for every type of material.

2.4.2 Silicon Carbide Substrates

Semi-insulating silicon carbide is one of the most attractive substrate materials for electronic applications, due to the favorable combination of lattice-

mismatch, isolation, and thermal conductivity [2.9, 2.427]. It is available with increasing quality and diameters up to 4 in. [2.385]. Both polytypes 4H- and 6H-s.i. SiC are used. On the contrary, III-N optoelectronic applications use conductive SiC substrates [2.387] with similar diameters. Most of the outstanding electronic device results have been reported on semi-insulating SiC materials, e.g., [2.362].

Currently, the greatest amount semi-insulating SiC material is produced by Cree [2.427]. The growth method is based on physical vapor transport deposition (PVT). There is a number of other vendors for semi-insulating material, e.g., such as II-VI [2.103, 2.273] and Toyota in [2.320].

Norstel/Okmetic developed a high-temperature CVD (HTCVD) method for the growth of s.i. SiC substrates. II-VI produces undoped 2- and 3-in. 6H-SiC grown by PVT [2.14, 2.103, 2.273]. Detailed examples are given in [2.78, 2.159, 2.484]. Both growth methods PVT and HTCVD result in different substrate properties, e.g., with respect to residual mobility [2.246]. For conductive material, several vendors are available, e.g., [2.159, 2.359, 2.424].

A number of issues remain for the growth of SiC, so a comprehensive substrate analysis is still necessary. These issues include:

- Control and reduction of average micropipe defects density [2.427]
- General defect reduction, such as polytype inclusions and Si segregation [2.103, 2.274]
- Subsurface damage removal [2.273]
- Surface polishing to reduce average roughness [2.433]
- Availability of 2–6-in. wafers of increased and homogenous quality, e.g., [2.360]

Substrate isolation at RT is not considered a problem for SiC anymore, as levels beyond $10^9 \Omega \text{ cm}$ at RT have been repeatedly reported [2.384]. This argument needs to be refined for high-temperature operation, as the substrate isolation mechanism is strongly temperature-dependent depending on the isolation method [2.529]. The availability of 4–6 in. diameters is desirable as most of the current GaAs fabrication lines are operated with these diameters.

SiC Substrate Characterization

Micropipes have been considered as the main obstacles for high quality SiC substrates and have attracted much attention for the definition of substrate quality, e.g., [2.103]. Micropipes are screw defects with a large Burger's vector which stretch through the complete crystals during bulk growth. Fig. 2.10 gives an optical image of a micropipe in a codoped semi-insulating SiC substrate. Polytype-control and background impurity control are of ultimate importance. Roughness is another criterion for substrates. Fig. 2.11 gives a microimage of a single micropipe for a surface with a residual roughness of 3 nm. Contrary to Fig. 2.11, Fig. 2.12 gives a microimage of a surface with a roughness RMS = 0.3 nm. The average micropipe density has been reduced

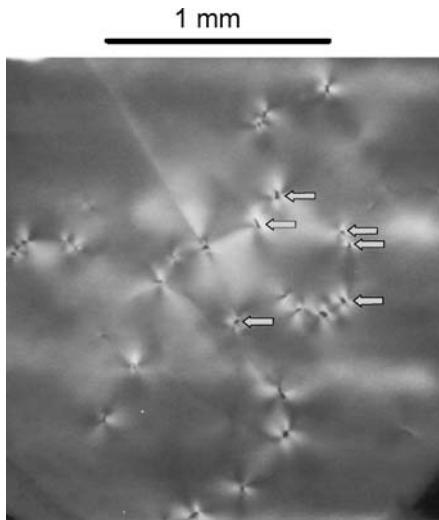


Fig. 2.10. Optical image of a micropipe cluster in s.i. SiC

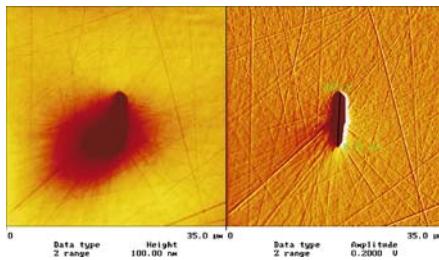


Fig. 2.11. AFM image of a micropipe in s.i. SiC, RMS = 3 nm

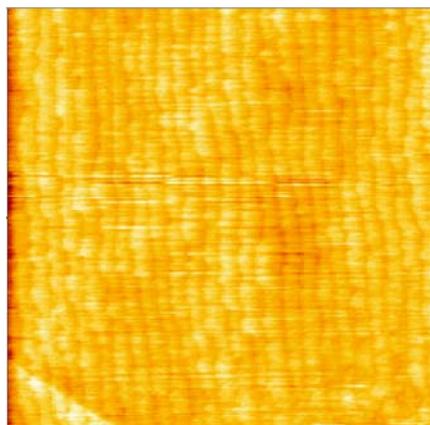


Fig. 2.12. AFM image of a CMP-polished surface of a s.i. SiC, RMS = 0.3 nm

constantly during the substrate development, e.g., [2.384]. However, since micropipes define a killing defect for any active [2.28] and most passive devices (see Chapter 8), such as MIM capacitances, their average reduction is crucial, especially when increasing substrate diameter [2.433]. Filling micropipes by epitaxial growth is nearly impossible due to the typical geometry depicted in Fig. 2.11. Other dislocations than micropipes [2.103, 2.159] have an impact on material quality and on device performance. This is mainly due to the fact that they serve as nucleation centers for other defects in the epitaxial layers [2.274]. Basal-plane as well as screw dislocations have been found by high-resolution X-ray diffraction and synchrotron white beam topography in 4H–SiC [2.159]. The transformation mechanism of threading edge dislocations in the substrate into the epitaxial layer is discussed.

Subsurface damage [2.273] and grain boundaries, especially in the periphery of the crystals, are of significant importance for III-N device performance. Subsurface damage is not visible to some characterization methods. It becomes visible, e.g., after significant thermal or chemical treatment [2.103, 2.174]. The subsurface damage can be removed by the application of chemical–mechanical polishing, as reported in [2.174]. For the final substrate, several characterization methods are possible. Fig. 2.13 gives a comparison of two optical polarization images of 3-in. s.i. SiC substrates for the analysis of overall surface quality. The right image depicts a very good wafer, while the left wafer depicts a mediocre quality. Several other substrate characterization methods are applied. The polarized light microscopy (PLM) method is further explained in [2.267]. The procedure allows a fast method to analyze micropipe (clusters), screw dislocations, and domain boundaries. The wafers can further be analyzed with and without epitaxial layers in order to investigate the defect propagation into the epitaxial layers. Micro-Raman can be used for topography of SiC crystals

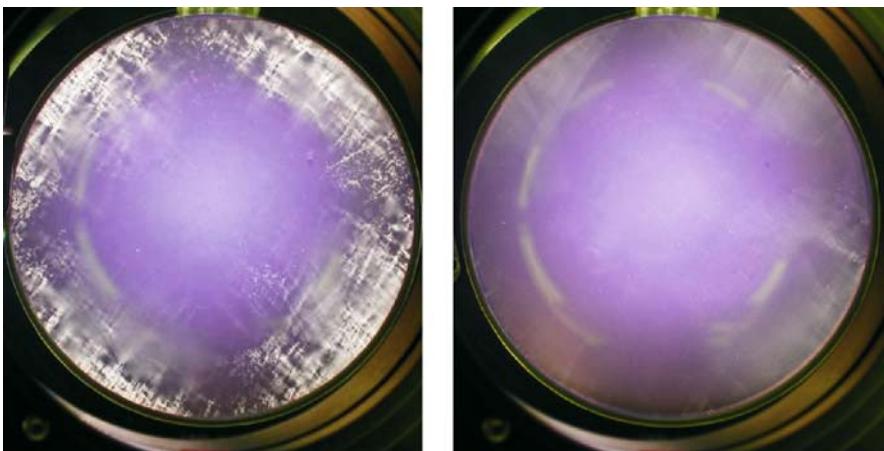


Fig. 2.13. Optical polarization images of two 3-in. s.i. SiC wafers

with a spatial resolution of $1\text{ }\mu\text{m}$ [2.274]. Further, X-ray topography allows detailed analysis of the defect, as is performed, e.g., in [2.204]. The issues now are discussed with the respective substrate growth method.

Doped Conducting SiC Substrates in Electronic Applications

Doped conducting substrates are readily available by several industrial vendors for optoelectronic applications, e.g., [2.41]. N-type SiC substrates are ten times more cost-efficient than semi-insulating substrates and are presented, e.g., in [2.103, 2.316]. The conductivity is achieved by impurity doping with nitrogen. However, there are also significant demonstrations of high-power AlGaN/GaN HEMTs for electronic applications, e.g., [2.174] on n-doped SiC substrates using $\approx 10\text{ }\mu\text{m}$ -thick HVPE-based AlN interlayers. Very uniform device performance is given on this quasi-semi-insulating substrate approach. Further AlGaN/GaN HEMTs on p-type 6H-SiC substrates are given in [2.368]. Very high current levels $I_{\text{Dmax}} \geq 1.4\text{ A mm}^{-1}$ and a cut-off frequency of 53 GHz are reported for devices with a gate length $l_g = 0.25\text{ }\mu\text{m}$.

Semi-Insulating Codoped Substrates

For semi-insulating substrates with isolation levels of $\geq 10^6\text{ }\Omega\text{ cm}$ [2.83, 2.384], two basic mechanisms are used to obtain substrate isolation. In a first approach, SiC substrates are compensated by codoping, typically with vanadium [2.484]. The substrates suffer from the limited solubility of vanadium in SiC [2.433]. The following substrate properties result from the codoping:

- The deep traps activate at high-operation voltages and degenerate the performance of SiC MESFETs [2.484].
- Vanadium codoping degrades bulk crystal quality due to increased local stress.
- The micropipe density increases due to the codoping [2.535].
- Codoping reduces lattice thermal conductivity by about 25% [2.83].

High-Purity Semi-Insulating (HPSI) Substrates

The negative effects of the codoping in s.i. SiC were discovered during SiC MESFET development, as discussed, e.g., in [2.433, 2.484]. SiC MESFETs on codoped substrates did not reach the expected power levels, which led to the development of undoped intrinsically compensated semi-insulating substrates. In this second approach, undoped high-resistivity or high-purity semi-insulating substrates (HPSI) [2.9, 2.294] with diameters up to 4 in. are under development with micropipe densities as low as 35 cm^{-2} . They promise the following properties [2.294]:

- Increased uniformity suitable for MMIC processes
- Increased resistivity and isolation

- Increased thermal conductivity [2.83]
- Reduced dispersive effects in the devices

However, in comparison to conducting SiC substrates, a smaller growth parameter window also has to be taken into account [2.535] for the growth of HPSI SiC substrates.

SiC Wafer-Size Scaling

Much of the III-N device results are so far achieved on 2-in. and 3-in. substrates. 3-in. s.i. SiC substrates are available with similar or improved quality relative to the 2-in. wafers [2.384]. Apart from the obvious cost improvement, wafer scaling is extremely desirable, as the history of GaAs has shown that uniformity of the devices eventually increases with increased substrate diameter, e.g., [2.446]. Further, equipment considerations are relevant, as most of the III-V processing facilities today are based on 4–6-in. equipment, which makes 2 and 3-in. processing a very cumbersome and expensive task. Four inch wafers with improving quality have been announced repeatedly [2.360, 2.385] and first production of GaN HEMT on 4-in. s.i. SiC substrate has been demonstrated.

2.4.3 Sapphire Substrates

Sapphire is a promising material due to the availability of cost-effective 2–4-in. diameter substrates [2.148]. It is widely used for development issues of electronic devices, and despite the lattice-mismatch, very impressive power densities of $\geq 12 \text{ W mm}^{-1}$ and high-pulsed-output powers have been achieved [2.16, 2.66]. In addition to the adaption of the epitaxial parameters, the following substrate-related device issues have to be solved:

- General thermal management due to the reduced thermal conductivity
- Full wafer thinning:
 - Mechanical treatment of this hard material in the course of the thermal management, e.g., thinning from 500/250 μm to 50 μm as suggested in [2.16]
 - Impact of substrate quality during backside process
 - Wafer breakage due to the aforementioned issues
- Mismatch-induced stress and wafer bowing of thinned sapphire substrates due to the high lattice-mismatch to GaN
- Processing issues, e.g., in lithography due to the high substrate-related wafer bowing [2.16]

On the device level, results for AlGaN/GaN HEMTs on 4-in. sapphire substrates are given in [2.20]. The epitaxial growth gives a relatively high standard deviation of $> 4\%$ for the Hall mobility. However, the high standard deviation can be well correlated with the standard deviation of the device parameters. The power performance of AlGaN/GaN HEMTs on sapphire substrate at 4 GHz is discussed in [2.478]. Power levels of 5 W mm^{-1} are reached at 2 GHz.

The epitaxial structure exhibits a thickness of $\geq 3\text{ }\mu\text{m}$. Using an additional HVPE-grown buffer on sapphire substrates, the uniformity of DC- and RF-performance of MBE-grown AlGaN/GaN HEMTs is analyzed in [2.125]. The fast growth of a GaN buffer layer by HVPE is combined with MBE epitaxial layer growth on 2 in. wafers. The DC-parameters of 258 devices, such as threshold voltage and transconductance show very low standard deviation.

2.4.4 Silicon Substrates

Because of quantity of its use and its economic importance, silicon is the most important semiconductor and substrate material. Thus, the use of silicon as a substrate material is desirable, mostly for cost efficiency reasons. However, the use of silicon also introduces a number of critical issues and engineering challenges for III-N devices, as enumerated below:

- The impact of the lattice-mismatch relative to GaN with respect to material defects, quality, and device reliability [2.169].
- The difference in the thermal expansion coefficients, especially for high-power operation [2.328] (of similar gravity with respect to reliability, but not so often mentioned).
- The availability and cost of 2–6-in. insulating silicon substrates with isolation levels of $10\text{--}30\text{ k}\Omega\text{ cm}$.
- The RF-transmission-line losses of passive lines for RF-frequencies [2.109].

The lattice-mismatch to III-N material in principle is a disadvantage; however, the substrate quality of silicon with respect to defects is outstanding compared to, e.g., SiC. Silicon substrates are virtually defect free, which helps a lot with device reliability [2.306]. To overcome the silicon issues, some very interesting epitaxial procedures have been developed, e.g., [2.168, 2.333], as will be described in Chapter 3. On the device level, AlGaN/GaN HEMTs on (111) silicon substrates are demonstrated, e.g., in [2.161, 2.162]. Very high power densities on silicon-substrates are reported by Triquint at 10 GHz [2.94, 2.109] and Nitronex at 2 GHz [2.52, 2.169]. Microwave and noise performance of $0.17\text{ }\mu\text{m}$ AlGaN/GaN HEMTs on (111) high-resistivity silicon substrates are reported. A minimum noise figure $N_{\text{F},\text{min}}$ of 1.1 dB is reported with an associated gain $G_{\text{ass}} = 12\text{ dB}$ at 10 GHz in [2.296]. The power density is 1.9 W mm^{-1} at 10 GHz [2.295, 2.297], while the PAE is only 18%. Promising reliability results for GaN HEMTs on silicon substrate have been given in [2.94] and [2.333] and are detailed further in Chapter 7.

2.4.5 GaN and AlN Substrates

Native GaN and AlN substrates have been only recently developed and used for electronic applications, although they are most important for optoelectronic applications. However, native substrates face increasing attention to the expected improvement in electronic device reliability, e.g., [2.73]. For native

substrates, the lattice-mismatch is fully eliminated as compared to the heterosubstrates.

GaN Substrates

GaN substrates are only recently available in n-conducting and semi-insulating form with diameters suitable for electronic device fabrication, i.e., in 2-in. format. Free-standing GaN substrates are available based on two growth processes. First of all, GaN templates on sapphire can be used to reduce the defect density for optoelectronic devices, e.g., [2.33, 2.140]. The defect density is $8 \times 10^7 \text{ cm}^{-2}$ for this kind of technique for a $10 \mu\text{m}$ layer grown by MOCVD. This kind of quasibulk approach can be used in a variety of ways, e.g., ELO or related approaches. In some approaches, the host substrate such as sapphire is removed leaving free-standing GaN. The second method is the growth of GaN boules, e.g., in [2.137, 2.328] by HVPE. Si-based n-doping is used for conductive substrates, while Fe doping is used to obtain s.i. substrates. Free-standing GaN substrates based on a similar procedure are provided by Sumitomo, e.g., in [2.140]. Impressive results of AlGaN/GaN HEMTs on free-standing GaN substrates have been demonstrated, e.g., in [2.73, 2.106]. The GaN substrates are fabricated by HVPE and are Fe-doped to achieve a resistivity of $10^6 \Omega \text{ cm}$. The homoepitaxy changes the defect situation in the buffer completely, which makes these devices potentially more reliable. From an electronic device perspective, nitride devices are mostly unipolar devices. The bipolar devices face a number of substantial technological drawbacks, as described in Subsect. 2.5.6. Thus, the lattice-mismatch is relatively less important so far. In order to compare the impact of the crystal lattice constant and crystal quality, Fig. 2.14 gives the reported residual dislocation defect concentration as a function of the substrate lattice-mismatch relative to GaN for various substrate options. Fig. 2.14 shows, that only bulk GaN or ELO techniques (i.e. quasibulk GaN approaches) can provide the very low defect densities required especially for optoelectronic (laser) devices, whereas GaN electronic devices are typically grown with defect densities of 10^8 – 10^9 cm^{-2} on various substrates.

AlN, ZnO, and Diamond Substrates

Native AlN substrates are also under discussion for optoelectronic applications [2.107, 2.403, 2.404, 2.407]. AlN itself is highly resistive and has a better thermal conductivity than GaN, actually the thermal conductivity is very similar to SiC. Further, compared to all other nonnative substrates, it has the lowest lattice-mismatch (Fig. 2.14). For the use of AlN for GaN-based lasers even the residual mismatch of the AlN relative to GaN lattice constant is too high to provide reliable GaN lasers without the use of additional concepts such as epitaxial regrowth techniques (ELO) to reduce the defect concentration [2.321]. This defect concentration of epitaxial layers grown on AlN substrates by migration enhanced MOCVD amounts to mid 10^6 cm^{-2} . However,

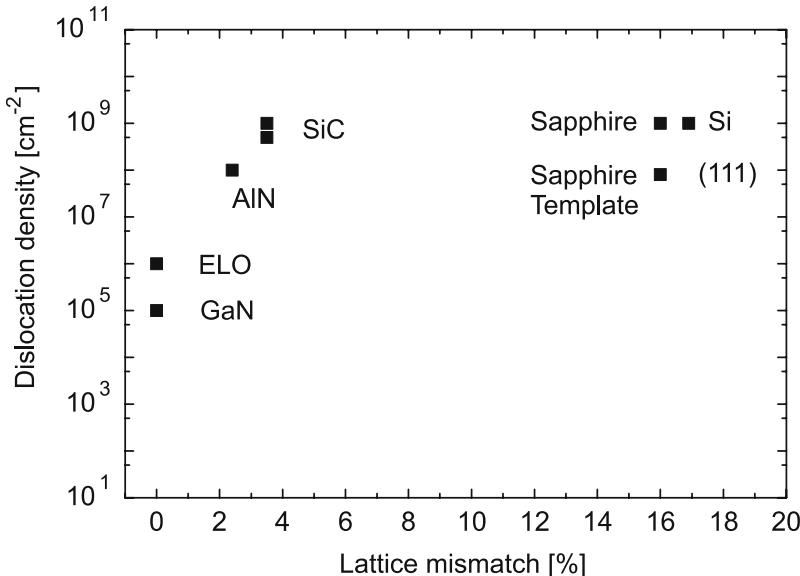


Fig. 2.14. Dislocation density as a function of lattice-mismatch relative to GaN

deep ultraviolet lasers are becoming feasible with the availability of a native substrate [2.404]. Free-standing AlN substrates with a thickness of $112\text{ }\mu\text{m}$ based on an Si(111) host substrate have recently been reported [2.224]. The boule growth of AlN by sublimation–recondensation is described as a growth method of the AlN substrates, e.g., in [2.404, 2.407]. High-purity AlN ceramics is sublimed in nitrogen atmosphere and recondensed on a seed substrate. GaN/AlGaN HEMTs on AlN substrate have been realized as reported, e.g., in [2.151]. The substrate diameter is so far limited; however, AlN substrates may enable more growth orientations and reduce the need of complex strain engineering. Electronic HEMTs on $30\text{ }\mu\text{m}$ -thick intermediate AlN layers grown by HVPE on SiC substrates are reported in [2.239]. The reduction of the gate-lag without surface passivation is attributed to the reduced amount of surface states related to dislocations and other defects. $10\text{ }\mu\text{m}$ -thick AlN layers are used in [2.174] to isolate conductive SiC substrates from the device. This approach is potentially a very low cost solution combining the advantageous thermal conductivity and isolation of AlN/SiC with a conductive low-cost substrate.

Further extending the material choices for substrates, wurtzitic zinc oxide (ZnO) materials and substrates are now available as large single crystals. For the optoelectronic applications, it is attractive due to a lattice-mismatch relative to GaN of only 2% and a large exciton binding energy of 60 meV . An overview of ZnO as a semiconductor material is described, e.g., in [2.257]. Next to the native substrate, also a developed wet-etch chemistry is available for ZnO as compared to the III-N. The advantages for electronic devices are

the high breakdown fields and the high saturation velocity. CVD diamond provides the highest thermal conductivity of any potential substrate material. Recent reports in [2.165] provide AlGaN/GaN HEMTs on diamond substrate. The devices are initially grown on Si substrate and then transferred to the CVD diamond via an atomic attachment process. The devices are found to be relatively dispersive and the beneficial impact of the improved heat removal cannot be clearly demonstrated.

2.5 State-of-the-Art of Devices and Circuits

Numerous overviews on nitride devices and research issues are available due to its dynamic development, e.g., [2.353, 2.361, 2.401, 2.455, 2.464]. General overviews of GaN/AlGaN heterostructure devices for photodetectors and field-effect transistors are given, e.g., in [2.96, 2.301, 2.422, 2.465]. General properties of undoped AlGaN/GaN HEMTs for microwave power amplification are discussed in [2.96]. Early reports of AlGaN/GaN HEMTs can be found, e.g., in [2.190], while initial reports for GaN MESFETs can be found in [2.418]. Although it is impossible to provide a full picture of all the achievements, a systematic overview of the published key issues, to the best of the author's knowledge, is given in the following. Some of the results may be outdated quite soon; however, the story of the development is highlighted.

2.5.1 Nitride-Based Diodes

GaN Diodes

Nitride-based diodes are attractive due to their high breakdown voltages in combination with high-carrier velocities leading to higher conversion efficiencies [2.76] and improved temperature performance. Possibly GaN also provides the material property of negative feedback leading to Gunn oscillations, as discussed, e.g., in [2.408]. A theoretical discussion of GaN diodes with respect to negative differential resistance is provided in [2.8]. Simulation results for the operation of wurtzite and zincblende GaN Impact Avalanche Transit Time (IMPATT) diodes are given in [2.8, 2.363]. Further, the possibility of high-frequency operation at D-band (140–220 GHz) of GaN-based IMPATT diodes is discussed in [2.8].

SiC-Based Diodes

SiC diodes serve as a reference and target high-speed high-power density switching applications, e.g., [2.387]. They are applied for switch-mode power supplies, e.g., in computer servers [2.359]. Though the overall numbers of SiC Schottky diodes produced so far are very small relative to the mass market of silicon diodes, the high power density, the low R_{on} [2.494], and the high-temperature operation provide very interesting niche markets. Commercial

SiC diode process of Cree in [2.368, 2.427] and Infineon [2.434] are available with strong research efforts underway on circuit and application level, e.g., [2.366, 2.434]. The reduction of the reverse recovery current during conversion and the improvements in conversion efficiency relative to Si diodes are mentioned, especially at frequencies beyond 100 kHz. SiC diodes are further discussed for the replacement of converters in hybrid car power-conversion applications [2.359].

2.5.2 Power Electronics

III-N wide bandgap semiconductors are unique with respect to power electronics from low frequencies to the RF-domain. The motivation for the use of III-N-based diodes [2.76] and FETs [2.397] stems from their increased switching speed and thus their conversion capabilities and more efficient transmission and distribution of electric power at increased operation temperatures, e.g., [2.334]. The target is the development of a technology for fast and efficient GaN-based electrical switches at a wide range of power levels. General overviews of wide bandgap semiconductor power electronics are provided in [2.334, 2.469, 2.494]. Typical expectations and specifications are:

- High stand-off voltage, e.g., $>1\text{ kV}$ [2.76, 2.438]
- High absolute current levels, e.g., up to 2 kA conducting current [2.76]
- A low forward voltage drop, e.g., $\leq 2\%$ of the rated voltage
- Higher operation temperature (e.g., 225°C [2.334])
- High frequency switching operation, e.g., at 50 kHz and above

The use of GaN-diodes in low-frequency control applications is discussed in [2.59]. GaN is predicted to have insertion and isolation loss properties similar to other semiconductors. The trade-off between parasitic resistance, breakdown voltage, and off-state capacitance is discussed. GaN devices do not necessarily provide higher breakdown voltages, but GaN FETs provide lower switching energies for the same breakdown voltages. Principal design considerations for III-N high-power devices are given in [2.27]. Planar Schottky devices are fabricated to obtain principal device parameters. Based on that, AlGaN thyristor switches with breakdown voltages of 5 kV at current densities of 200 A cm^{-2} with frequencies above 2 MHz are predicted based on the basic device parameters. Future military applications of wide bandgap power semiconductor devices are discussed in [2.105]. The high-power handling capabilities of the SiC and GaN devices in general allow more efficient power distribution at higher power levels and more compact device sizes. Estimates of the theoretical limit of lateral wide bandgap semiconductor devices for switching applications are given, e.g., in [2.396]. Lateral switching devices based on GaN and SiC are discussed for breakdown voltages of 1 kV and on-resistances of $1\text{ m}\Omega\text{ cm}^2$. The main advantage of the wide bandgap devices is the drastic reduction in gate width and chip area, and in power loss. At the same time the increase of the power density in the GaN FETs by a factor of

6 leads to an increase of the thermal dissipation and requires a significantly improved packaging technique.

RF-Switches

A high-power Tx/Rx RF-switch IC using AlGaN/GaN HFETs on sapphire substrate is described in [2.158]. The device is capable of handling a power of 46 dBm at 1 GHz with an insertion loss of 0.26 dB and an isolation of 27 dB. The high-breakdown voltage leads to a reduction of the number of FETs as compared to circuits realized with GaAs technology. A single pole double through (SPDT) switch implemented with GaN HFETs featuring a double recess technique is presented in [2.144]. A low insertion loss of 1.1 dB and an isolation of 21 dB can be realized. The double recess technique including an ohmic and a gate recess allows to optimize the access resistance and leakage current independently.

DC–DC-Converter

Fast and efficient DC–DC-converters are one application for AlGaN/GaN HEMTs. An overview of the suitability of wide bandgap semiconductors for this application is given in [2.460]. As an example, a 600 V fast DC–DC-converter AlGaN/GaN power HEMT is demonstrated in [2.397]. An optimized design including a source-terminated field plate delivers $R_{\text{on}} = 0.5 \text{ m}\Omega \text{ cm}^2$ and a maximum switching current density of 850 A cm^{-2} . The power efficiency varies between 83% at 100 kHz and 75% at 500 kHz. A demonstration of a Class-E amplifier with a PAE of 89.6% at 27.1 MHz is given in [2.394, 2.395]. The applied drain voltage is 330 V. The devices are grown on n-SiC substrate and use a source-terminated field plate. Even higher breakdown voltages of 1.6 kV and low $R_{\text{on}} = 3.4 \text{ m}\Omega \text{ cm}^2$ are reported in [2.459]. With the application of conductivity modulation, even higher breakdown voltages are achieved, e.g., [2.471]. A typical FOM for power conversion and switching reads:

$$\text{FOM} = \frac{V_{\text{breakdown}}^2}{R_{\text{on}}} = q \cdot \mu \cdot n_{\text{sheet}} \cdot E_{\text{crit}}^2. \quad (2.55)$$

The limits of the material system used can be deduced with the approximation given in (2.55). A more advanced approximation including a surface limit is given in [2.459]. These limits are also depicted in Fig. 2.15. There are several examples for the trade-off between breakdown voltage and on-resistance for GaN HEMTs in comparison with Si and SiC devices, as given in Fig. 2.15. Data points are taken from [2.2, 2.63, 2.138, 2.213, 2.310, 2.398, 2.438, 2.445, 2.471, 2.472]. Silicon devices beyond the actual Si limit have been realized [2.310]. The third parameter, the switching time, is not explicitly mentioned in Fig. 2.15. However, turn-on delays of 7.2 ns can be reached with GaN FETs. This turn-on delay is only a fraction of the Si MOSFET value. Further improvements are found for wide bandgap semiconductor with respect to heat dissipation and reduced chip area, as discussed in [2.396]. A recent general

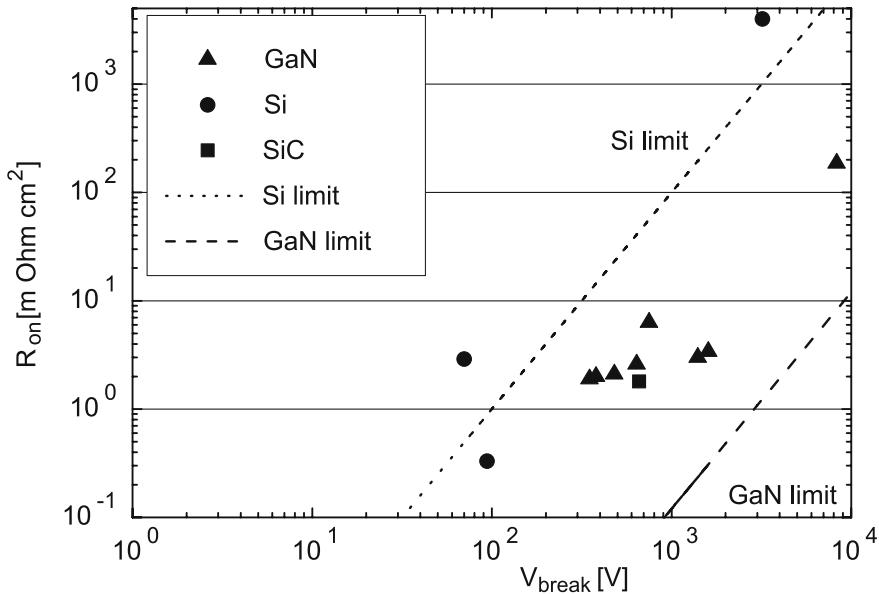


Fig. 2.15. On-resistance R_{on} as a function of breakdown voltage for switching applications

overview on the use of diamond for power applications is given in [2.207]. This material system promises very high breakdown voltages of 10 kV [2.396] and operation temperatures of 1,000°C, while this approach is still in its infancy.

2.5.3 RF-Metal Semiconductor Field-Effect Transistors (MESFETs)

MESFETs have been introduced as the first wide bandgap FETs into industrial production.

SiC MESFETs

A compilation of substrate and semiconductor material properties of SiC is given in [2.139]. Both static induction transistors (SIT) and SiC MESFETs are discussed. Pulsed-output power levels of 900 W of SiC SITs at 425 MHz with a drain efficiency of 80% are reported as well as output power levels of 80 W at 3.1 GHz with MESFETs. Substrate and epitaxial issues for SiC power devices are discussed in [2.433]. A classification of the residual defects is also given. A complete SiC MESFET technology, especially for S-band RF-applications, is provided by Cree [2.75]. The transition of this technology from discrete MESFETs to a high performance MMIC technology is described in [2.293].

The MMIC devices yield excellent wafer-to-wafer uniformity and a high power density of 4 W mm^{-1} up to frequencies of 3.5 GHz. Silicon carbide MESFET performance and its application in broadcast power amplifiers between 0.5 and 0.9 GHz are reported in [2.454]. The SiC devices yield a much higher operation voltages of up to 55 V in comparison to Si LDMOS. This leads to increased output densities of $\geq 2 \text{ W mm}^{-1}$, but especially higher input and output impedances for SiC MESFETs. A comparison of SiC and GaN transistors for microwave power applications is given in [2.463]. The main distinction suggested is the power density of SiC MESFETs with $5\text{--}6 \text{ W mm}^{-1}$ up to X-band, while GaN is predicted to achieve up to 10 W mm^{-1} up to 100 GHz on the device level.

GaN MESFETs

GaN MESFETs provide wideband properties similar to SiC MESFETs; however, both lack the potential advantages of heterojunctions. The advantage of GaN MESFETs relative to SiC MESFETs is the increased speed performance. This speed performance is, however, inferior to GaN heterostructure devices, e.g., as demonstrated in [2.62, 2.379]. A theoretical comparison by simulation of GaN MESFET-based on different GaN material phases wurtzite and zincblende GaN is given in [2.111]. The wurtzite structure yields higher breakdown voltages and lower transconductance than the zincblende structure. The simulated cut-off frequencies of wurtzite MESFETs are significantly lower, again based on the lower transconductance. Another systematic comparison of zincblende-phase GaN, cubic-phase SiC, and GaAs MESFETs using a full-band Monte Carlo simulator is given in [2.492]. A factor-of-four improvement of the breakdown voltage for GaN devices is found as compared to GaAs MESFETs for the same gate length of 100 nm. The experimental realization of doped-channel GaN heterojunction MESFETs are described in [2.62]. The devices with a gate length of $0.25 \mu\text{m}$ yield an output power density of 1.7 W mm^{-1} at 8.4 GHz on sapphire substrates. The doped channel layer has a thickness of 50 nm and is n-doped with $n = 2 - 5 \times 10^{17} \text{ cm}^{-3}$. The $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ layer has thickness of 18 nm. Epitaxially grown GaN junction FETs are given in [2.531]. The cut-off frequencies are $f_T = 6 \text{ GHz}$ and $f_{\max} = 12 \text{ GHz}$ for a gate length of $0.8 \mu\text{m}$. The channel mobility is $270 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for a free carrier concentration of $1.3 \times 10^{18} \text{ cm}^{-3}$. The nominal p-doping of the pn-junction is $5 \times 10^{19} \text{ cm}^{-3}$. The impact of p-doped overlayers on the dispersion in GaN junction FETs is described in [2.166]. The p-doped layer removes the low-frequency dispersion as it screens the channel from the surface states. This concept is promising, as the reproducibility of an epitaxial concept is higher than of a technological approach. However, the Mg trap depth is not sufficient to avoid carrier modulation, which leads to longer effective gate length and thus lower f_T and f_{\max} . A GaN MESFET based purely on polarization doping through a graded AlGaN barrier layout without any impurity doping is compared to a conventional impurity n-doped GaN MESFET

in [2.379]. The polarization-doped devices with a gate length of $0.7\text{ }\mu\text{m}$ yield $f_T = 19\text{ GHz}$ and $f_{\max} = 46\text{ GHz}$.

2.5.4 Metal Insulator Semiconductor Field-Effect Transistors (MISFETs)

Nitride MISFETs are very attractive candidates for improved performance of the gate diodes relative to nitride MESFETs and HEMTs with metal/semiconductor Schottky-gates. At the same time MISFETs require the mastery of the insulator/semiconductor interface. This interface affects threshold voltages and other device properties to a great extent. GaN-based MOSFETs (Metal Oxide Semiconductor FETs) have been demonstrated, e.g., in [2.191]. The comparison of the $\text{SiO}_2/\text{AlGaN}/\text{GaN}$ MOSFETs with regular Schottky-gate HEMTs yields similar drain current densities, while the gate current density is reduced by six orders of magnitude for the MOSFET. The threshold voltage is shifted by -3 V for the MOSFET relative to the HEMT. A quarter micron $\text{SiN}/\text{AlGaN}/\text{GaN}$ MISFET was developed as reported in [2.1]. Again the threshold voltage V_{thr} is shifted to negative values of -7 V . This MISFET further yields a high power density of 6 W mm^{-1} up to 26 GHz . The DC- and small-signal parameters of the MISFET are very similar to those of the HEMT. An overview of III-N insulating gate FETs is further provided in [2.193]. The low-leakage currents of the MISFETs found at RT are also reduced at temperatures of 300°C . Further, the MISFET concept is applied to double heterojunction $\text{AlGaN}/\text{InGaN}/\text{GaN}$ structures, which reduce the current collapse to a high extent [2.192, 2.426].

Power Performance of MISFETs

Several demonstrations of the power performance of III-N MISFETs are available [2.69, 2.74]. Reduced gate-leakage of MIS gate devices relative to MESFETs and consequently improved linearity at 4 GHz are demonstrated in [2.69]. The third-order intermodulation ratio of 30 dBc is reached with a power density of 1.8 W mm^{-1} and an associated PAE= 40% at 2 GHz . SiO_2 is used as the gate dielectric. The microwave performance of undoped AlGaN/GaN MISFETs on sapphire substrates is given in [2.74]. A power density of 4.2 W mm^{-1} at 4 GHz is obtained at $V_{\text{DS}} = 28\text{ V}$, again with a very negative threshold voltage $V_{\text{thr}} = -10\text{ V}$. The extrinsic transconductance is 100 mS mm^{-1} . $\text{SiO}_2/\text{AlGaN}/\text{InGaN}/\text{GaN}$ MOS double heterostructure FETs (MOSDHFETs) are demonstrated in [2.192, 2.426] with the introduction of the new channel material InGaN. The importance of the additional carrier confinement is to reduce the spillover into trapping states. A Cat-CVD Insulated AlN/GaN MISHFET is given in [2.142]. Very thin AlN layers with a thickness of 2.5 nm are used as barrier layers. On top of this barrier a 3 nm SiN layer is deposited by Cat-CVD. This layer combination allows a very small gate-to-channel separation, which is used combination with gate length

of 60 nm to achieve a cut-off frequency $f_T = 107 \text{ GHz}$. The application of GaN MISFETs for low-loss switching is discussed in [2.217]. A 1 mm wide AlGaN/GaN MOSHFET yields switching powers of 43 W with 40 dB of isolation and 0.27 dB insertion loss at 100 MHz. The SiO₂ thickness is 7 nm in this case. The very negative threshold $V_{\text{thr}} = -9 \text{ V}$ is achieved for the device, which yields a maximum saturated pulsed-drain current of 2 A mm^{-1} .

2.5.5 High-Electron Mobility Transistors (HEMTs)

GaN HEMTs or heterojunction FETs (HFETs) are currently the most widespread and most advanced electronic nitride devices. They make full use of heterostructures and the advantageous breakdown and transport properties of undoped GaN. A huge number of compilations of GaN HEMT data is available, e.g., in [2.39, 2.96, 2.301, 2.302, 2.463]. Initial overviews are given in [2.40, 2.312, 2.422]. Initial microwave results of AlGaN/GaN HEMTs have been given in [2.40, 2.190, 2.506]. An overview of AlGaN/GaN HEMT technology is provided by Keller et al. and Mishra et al. from UCSB in [2.188, 2.301]. P_{sat} An overview of the application of GaN-based HFETs for advanced wireless communication is provided in [2.341]. Recent developments and trends in GaN HFETs in Europe are given in [2.455, 2.476]; overviews of the US activities are given, e.g., in [2.361, 2.401]. This section provides a systemized data collection which is presented with emphasis on the frequency aspect and the achievements relative to the theoretical predictions. To systemize device performance, Fig. 2.16 gives a compilation of the product cut-off frequency $f_T \times l_g$ as a function of gate length l_g . A product of $12 \text{ GHz } \mu\text{m}$ is found for $l_g \geq 300 \text{ nm}$ for GaN HFETs. A GaAs reference value of $15 \text{ GHz } \mu\text{m}$ is assumed. For gate lengths smaller than 300 nm, the short-channel effects become visible for GaN HFETs. Fig. 2.17 gives a compilation of the output power per unit gate width as a function of frequency. A distinction is made between pulsed- and cw-output power. The maximum power densities reach 12 W mm^{-1} without additional measures at the gate, while output power densities $\geq 40 \text{ W mm}^{-1}$ have been reported using field plates [2.511]; however, reliability concerns prevail. Significant improvements of the output power up to 101 GHz have been reported as compared to all other semiconductor technologies [2.291, 2.378]. Similar to Fig. 2.17, Fig. 2.18 gives the absolute cw- and pulsed-output power as a function of frequency. The power levels on the transistor level reach 370 W under cw-operation conditions [2.488] at 2 GHz. Under pulsed-operation with low duty cycles, even higher output power values of up to 1 kW have been reported [2.268, 2.304, 2.503]. For low-noise operation, Fig. 2.19 gives the minimum noise figure $N_{\text{F},\text{min}}$ as a function of frequency for both a single-recess GaAs PHEMT and a planar GaN HFET. The comparison yields promising minimum noise figure for the GaN HFET, which is slightly increased relative to the GaAs PHEMT [2.153, 2.262]. The next paragraphs systematically discuss the various frequency bands with respect to power and noise performance.

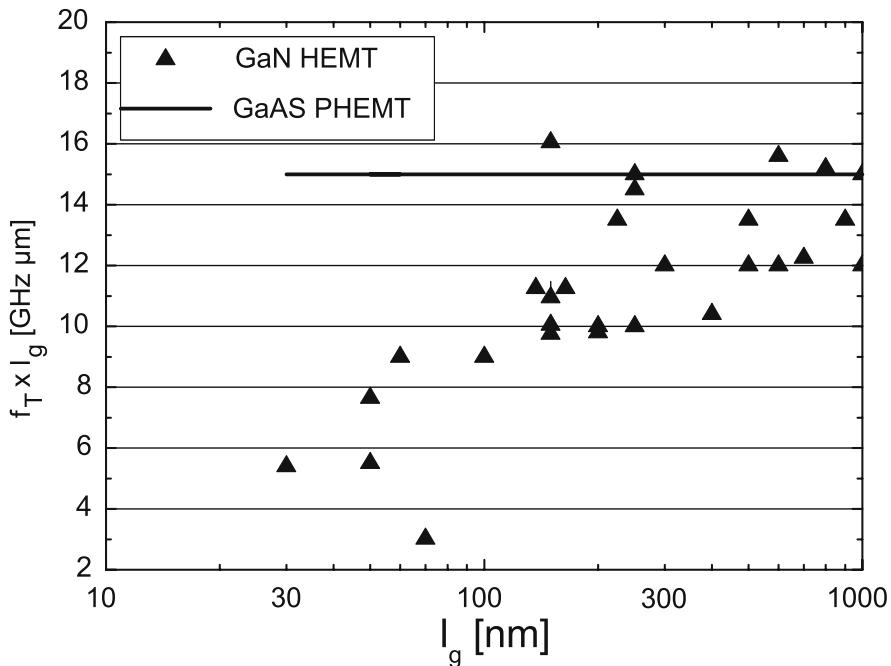


Fig. 2.16. Product cut-off frequencies $f_T \times l_g$ as a function of gate length l_g

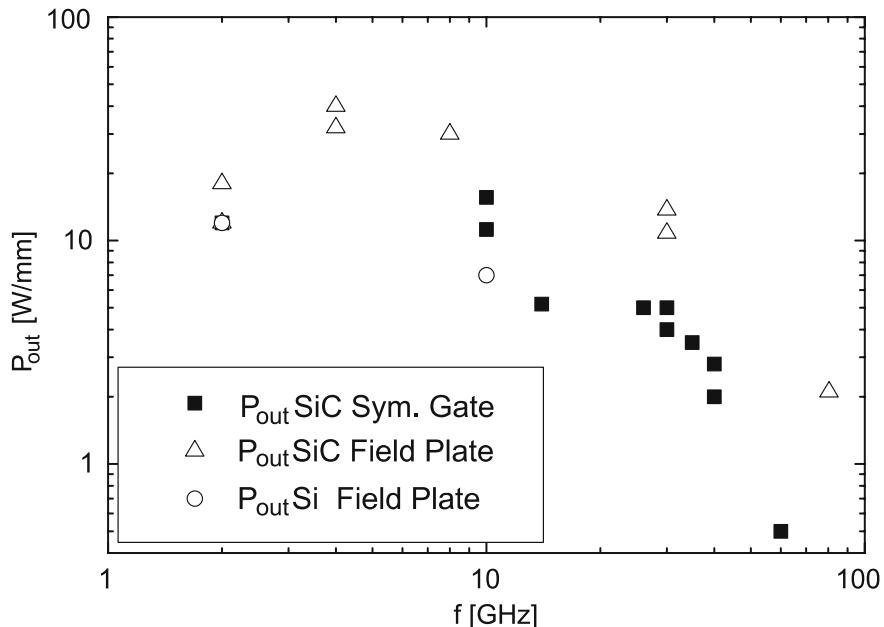


Fig. 2.17. Measured output power per unit gate width as a function of frequency

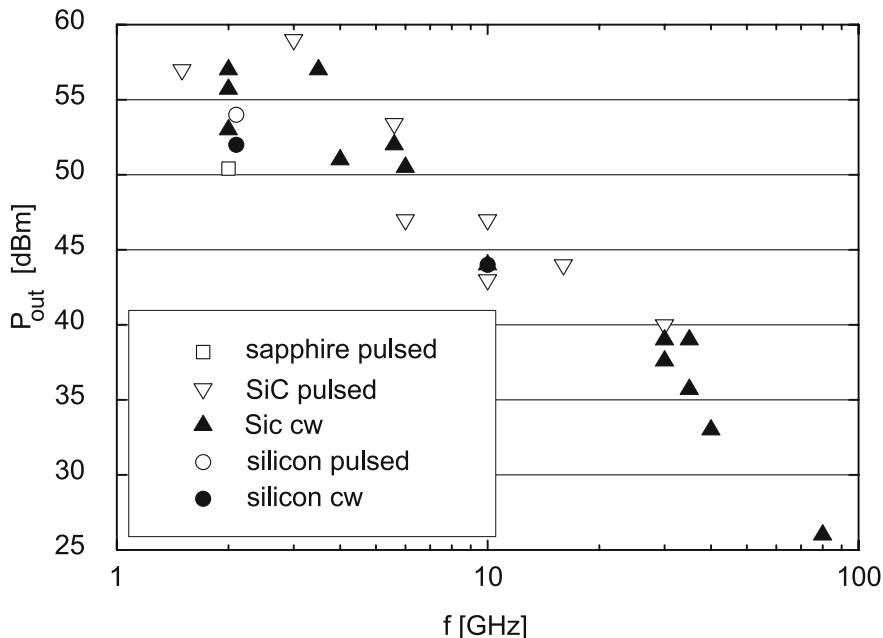


Fig. 2.18. Absolute cw- and pulsed-output power of AlGaN/GaN HFETs on various substrates as a function of frequency

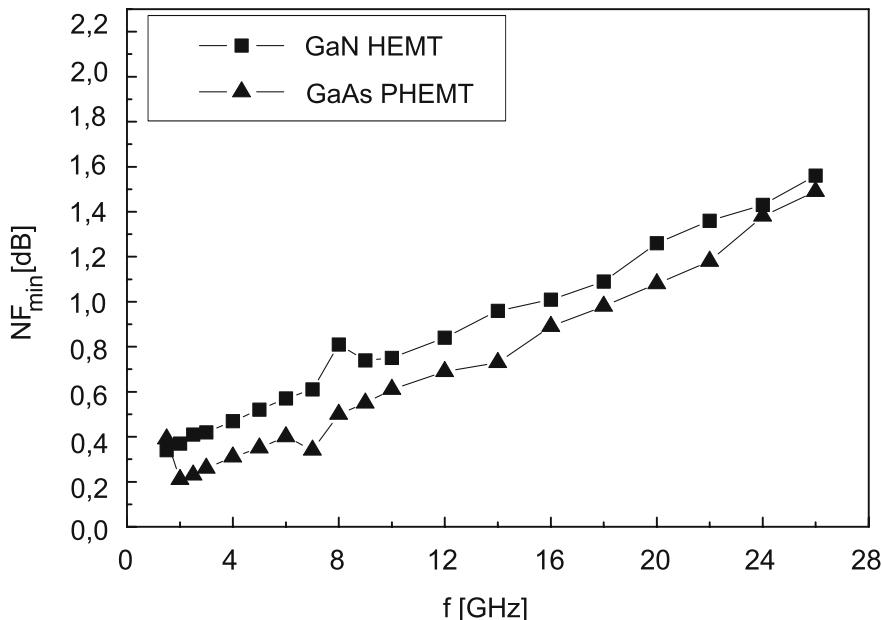


Fig. 2.19. The minimum noise figure $N_{\text{F},\text{min}}$ for GaAs and GaN HEMTs as a function of frequency at a drain current $I_{\text{D}} = 100 \text{ mA mm}^{-1}$ for $l_{\text{g}} = 150 \text{ nm}$

L-Band and S-Band Frequencies (1–3 GHz)

GaN HEMTs are attractive for base-station applications, due to the increased operating voltages ≥ 28 V, higher impedance levels, and reduced thermal memory effects. Overviews and guidelines for future directions are given, e.g., in [2.309] and in [2.495].

Mobile Communication

Cree gave the first report of cw-power operation of GaN HEMTs on SiC with output power levels beyond 100 W with 108 W at 2 GHz in [2.362]. Higher power operation at 3.5 GHz has recently been demonstrated in [2.503] with output power levels of 550 W in pulsed-operation with low duty cycle at $V_{DS} = 55$ V in a single-stage design. On s.i. SiC substrate, an 80 W/96 W AlGaN/GaN HFET with a field-modulation plate is demonstrated by NEC in [2.343, 2.345]. The 24 mm device yields a peak PAE of 54% for an operation bias $V_{DS} = 32$ V. The 4 mm subcell yields a power density of 8.1 W mm^{-1} at $V_{DS} = 41$ V. An AlGaN/GaN field-plate-FET with a gate width of 32 mm using a recessed gate is demonstrated in [2.344]. The cw-power density is 4.7 W mm^{-1} and the peak PAE is 64% at 2 GHz and $V_{DS} = 47$ V. Similarly, a cw-output power of 179 W is then reported in [2.190] for a gate periphery of 48 mm. The linear gain is 9.3 dB at 2 GHz, the PAE is 64% at $V_{DS} = 46$ V. A similar transistor operated under one-carrier WCDMA conditions presents 280 W of single-ended-amplifier output power in [2.487] with the application of a gate width of 48 mm with a linear gain of 12.6 dB at $V_{DS} = 48$ V. The drain efficiency is 29% at 8 dB of backoff from the saturated power in WCDMA operation. The output power levels can be increased to 370 W with paralleled devices, again achieved under one-carrier WCDMA conditions at 2.14 GHz. In this case the linear gain is 11.2 dB at $V_{DS} = 45$ V. AlGaN/GaN HFETs on thinned sapphire substrates with 110 W of pulsed-output power at 2 GHz at $V_{DS} = 40$ V are presented by NEC in [2.16] with $W_g = 32$ mm device. The related cw-output power is much lower and reaches 22.6 W for a $W_g = 16$ mm device. The sapphire substrate is thinned to 50 μm in this case.

Fujitsu and Eudyna have demonstrated some of the most advanced device results with respect to base-station applications. Early results present a 36 W cw-AlGaN/GaN power HEMT using a surface-charge-controlled structure [2.198]. This structure combines a doped GaN cap to screen the polarization charges at the AlGaN/GaN interface with very well optimized material. Both the barrier thickness and the SiN passivation are optimized. An improved intermodulation distortion profile of such AlGaN/GaN HEMTs at a drain bias voltage $V_{DS} = 30$ V is reported in [2.318]. No sweet-spot behavior is found for two-tone measurements in deep class-A/B operation. Further technology development is described in [2.195, 2.197]. CW-operation of a 24 mm device at $V_{DS} = 50$ V is achieved with a peak PAE of 60% and an output power of 48 W at 2 GHz. Output power levels of 150 W in cw- and 174 W at 2.1 GHz in WCDMA-operation at $V_{DS} = 63$ V are reported in [2.172, 2.196] for a single

packaged device. The PAE is 54% in cw-operation. For four-carrier WCDMA signals including the application of predistortion system, a peak efficiency of 40% is reached in Class-A/B operation while the WCDMA ACLR specification of -50 dBc at 10 MHz offset is preserved. The gate width is 36 mm with a unit finger length of $400\text{ }\mu\text{m}$. Based on these devices, a GaN HEMT amplifier in dual-device push-pull configuration is demonstrated in [2.171, 2.195]. The devices are again biased at $V_{DS} = 50\text{ V}$. The cw-output power of the amplifier at 2.1 GHz is 136 W with an associated PAE of 53% and a linear gain of 12.9 dB. The amplifier is further characterized in one-carrier WCDMA operation. With the application of a DPD system, a peak output power of 250 W is reached. The associated drain efficiency is 37% at an ACLR of -55 dBc . The average output power amounts to 46.5 dBm. The technology transfer and very promising reliability results are reported at $V_{DS} = 60\text{ V}$ [2.197, 2.330]. The devices can be operated at a compression level of $P_{-3\text{dB}}$ at $V_{DS} = 60\text{ V}$ for 1,000 h at room temperature. The resistance of the ohmic contacts is found to stable within 6% at high current density of $2 \times 10^6\text{ A cm}^{-2}$ at 250°C in nitrogen ambient. High-efficiency Class-E amplifiers in this technology are given in [2.473]. The amplifiers reach 82% of drain efficiency at 2.1 GHz, an output power of 10 W, and a linear gain of 19.5 dB. 45% of drain efficiency are reached for two-carrier WCDMA operation at ACLR of -50 dBc . The technology has further been exploited for air traffic radar. Pulsed-output-power levels of 500 W at 1.5 GHz for radar operation are reported in [2.268]. The amplifier consists of four chips with a gate width of 36 mm each with an overall gate width of 144 mm in a dual push-pull configuration. Even higher output power levels are obtained at S-band in [2.304]. A maximum pulsed-output power of 59.3 dBm is obtained between 2.9–3.3 GHz with a linear gain of 14 dB at $V_{DS} = 65\text{ V}$ and 10% duty cycle. The pulse width is $200\text{ }\mu\text{s}$ and the associated PAE amounts to 50%. Again a four-chip configuration is used with a single finger gate width of $375\text{ }\mu\text{m}$ and a total gate width of $4 \times 36\text{ mm} = 144\text{ mm}$.

RF Microdevices announced the commercial application of GaN FETs on 4 in. sapphire [2.412] and later on 3 in. s.i. SiC substrates in [2.134, 2.482]. The technology comprises very high power cw-densities of $\geq 22\text{ W mm}^{-1}$ at 2.14 GHz and $V_{DS} = 80\text{ V}$. A 20 mm devices delivers more than 100 W of output power with an associated PAE of 55% at $V_{DS} = 48\text{ V}$. Dual-gate devices are used for driver applications in [2.481]. Different dual-gate technologies are compared to single gate technologies. As an outcome a ground-terminated field plate on top of the SiN yields higher gain per stage, higher PAE, and better reliability under RF-drive.

Freescale provides AlGaN/GaN HEMTs on s.i. SiC for an industrial process [2.131]. Very high cw-power densities of $10\text{--}11\text{ W mm}^{-1}$ are reached with PAE levels of 67% at 2.14 GHz. Devices with 12.6 mm periphery yield output power levels of 74 W or nearly 6 W mm^{-1} in cw-operation. The SiC substrates are thinned to $100\text{ }\mu\text{m}$.

GaN devices on silicon substrates show much economic potential due to the low substrate cost. Conducting and high-resistivity silicon substrates are

suitable candidates for operation of up to 10 GHz [2.109]. The performance of AlGaN/GaN HFETs fabricated on 100 mm silicon substrates for wireless base-station applications is further evaluated in [2.52]. Despite the high lattice-mismatch, very good reliability data are reported predicting 20 years of lifetime based on a junction temperature of 200°C and 10% drift of the parameters. Cw-power densities of up to 12 W mm^{-1} at 2.14 GHz and $V_{DS} = 50 \text{ V}$ are reached with this AlGaN/GaN HEMT technology [2.169]. The gate width in this case is 100 μm , the maximum PAE 52%, and the power gain 15 dB. Recent reports announce cw-power levels of 150 W at 2.14 GHz with a drain efficiency of 65% and a linear gain of 16 dB, when operated at $V_{DS} = 28 \text{ V}$ [2.319]. The overall gate periphery is 72 mm in a single package with a single finger geometry of $0.7, \mu\text{m} \times 200 \mu\text{m}$. Promising reliability results have been reported in [2.168, 2.367]. Devices with a periphery of 36 mm are tested under RF-drive with an extrapolated drift of P_{sat} of $\leq 1 \text{ dB}$ in 20 years at 28 V. On amplifier level, very promising PAE vs. ACLR results are reported in [2.201, 2.202] with PAE levels of 50% based on Nitronex GaN HEMTs. Envelope-tracking is used to obtain high PAE values of 50% for a nonconstant envelope input. An average output power of 37 W is reached at a peak-to-average ratio (PAR) of 7.67 dB. The linear gain in this operation is 10 dB. With the application of a digital predistortion the error vector magnitude (EVM) of 1.74% is reached with an ACLR of -51 dBc at 5 MHz offset. Specific WiMAX applications based on GaN on silicon are presented in [2.456]. Eight millimeter and 36 mm devices are tested under orthogonal frequency-division multiplexing (OFDM)-modulation between 3.3 GHz and 3.8 GHz. At 3.5 GHz, the 8 mm device delivers an average output power of 1.5 W at 3.5 GHz, while the 36 mm device delivers 7 W. EVM is 2% and the drain efficiency (DE) amounts to $\geq 27\%$. The devices are fully packaged and qualified between -40°C and 85°C .

Several other processes are available. The performance of AlGaN/GaN HEMTs for 2.8 GHz and 10 GHz power amplifier applications is evaluated in [2.528] for military applications. Pulsed-output power levels of 41 W at 2.8 GHz with power densities up to 9.2 W mm^{-1} are obtained early in the development.

C-Band Frequencies (4–8 GHz)

C-band frequencies are used for both communication and radar applications and require high-power operation and high-temperature robustness in combination with high PAE. This frequency range typically cannot be reached by either LDMOS or SiC MESFETs. GaN HEMTs on s.i. SiC substrate using a field-plate gate concept are demonstrated at operating voltages of $\geq 90 \text{ V}$, resulting in cw-output power densities $P_{out} \geq 30 \text{ W mm}^{-1}$ at 4 GHz and 8 GHz [2.512]. Although the scaling of this performance to higher gate widths is questionable with respect to the thermal management, reliability, and efficiency, the fundamental high-speed power performance of GaN is visible. At C-Band, the University of California reported a GaN HEMT on s.i. SiC

with an output power of 2.8 W with a density of 18.8 W mm^{-1} and a PAE of 43%. A maximum PAE of 71% is reported with a power density of 6 W mm^{-1} at 4 GHz [2.67]. A 60 W and 100 W internally matched C-band GaN HEMT with $W_g = 24 \text{ mm}$ is given in [2.346, 2.347]. The cw-output power is 100 W at 5 GHz with 31% PAE and a linear gain of 12.9 dB at $V_{DS} = 56 \text{ V}$. Applying pulsed-operation with 1% duty cycle, an output power of 156 W is found at 4 and 5 GHz [2.346]. Record cw-output power values of 140 W at 5.6 GHz from a single chip are reached with the application of $W_g = 50.4 \text{ mm}$ [2.173, 2.519]. A cell division concept is applied to suppress odd-mode loop oscillations while maintaining good gain. Record output power levels of 220 W at C-band are reported in [2.520] in a two-chip amplifier by improvements of device performance and reduction of the thermal resistance. 167 W are obtained from a single chip at 7 W mm^{-1} . Similarly 60 W of output power are obtained from a 16 mm chip at 45% PAE. These examples demonstrate the combination of high-gain and high-breakdown in GaN HFETs which have demonstrated much higher power densities, output power levels, and operation bias, while maintaining efficiency.

X-Band Frequencies: (8.2–12.4 GHz)

Power operation of AlGaN/GaN HEMTs at X-band is particularly attractive, due to the increase of operating voltages relative to GaAs while maintaining high-speed operation and thus guaranteeing high-gain and high-efficiency operation. The increase in operating voltage from typically 5–8 V for GaAs PHEMTs to $\geq 40 \text{ V}$ will reduce the need to transport high currents on system level. Applications in the X-frequency band include transmit-receive (TRX) modules for naval and airborne phased array radar applications. Power-added efficiency is a major concern, both on the device and system level. Typical device targets are mentioned in [2.384]. PAE values of 60% are required at $V_{DS} = 40 \text{ V}$ with a power density of 6.4 W mm^{-1} for a device with 1.28 mm. Further the long term reliability of 10^6 h is required. Early reports of the power operation at X-band by the UCSB and Rockwell are given in [2.439, 2.507]. The output power density was 1.7 W mm^{-1} and 2.3 W mm^{-1} at that time for small devices. An early report of very high-power density of AlGaN/GaN HEMTs on s.i. SiC with 9.8 W mm^{-1} at 8 GHz is demonstrated by the UCSB in [2.504]. Basic predictions of the power operation limits are provided by Trew et al., focusing on the impact of the wide bandgap-material-properties on RF-power performance with respect to dispersion, e.g., in [2.462, 2.463, 2.465]. Output power densities of $10\text{--}12 \text{ W mm}^{-1}$ are predicted at X-band. The experimental power-frequency limits of AlGaN/GaN HEMTs for X-band are evaluated by Eastman and coworkers, e.g., in [2.96, 2.98, 2.132]. Small periphery devices with $l_g = 300 \text{ nm}$ yield power densities of 11.7 W mm^{-1} at 10 GHz with an associated PAE of only 43% at $V_{DS} = 40 \text{ V}$. At low V_{DS} bias, the PAE is as high as 55%. Geometrical considerations for the operation at X-band, e.g., the barrier-layer thickness, are evaluated in [2.457]. Triquint announced a power

MMIC process for radar applications at X-band [2.467]. Output power densities of 12 W mm^{-1} at 10 GHz have been reported with an associated PAE of 50%. An outstanding performance is also announced on Si substrates at X-band in [2.94]. The power densities for a small periphery device are as high as 7 W mm^{-1} at 10 GHz with an associated PAE of 37% at $V_{DS} = 40 \text{ V}$. Again, the PAE is limiting in this case.

In cooperation with General Electric, a power density of 9.2 W mm^{-1} with 13.8 W cw-output power at 10 GHz and 55 V drain bias using AlGaN/GaN HEMTs on SiC substrate are demonstrated by Lockheed in [2.18]. The associated PAE is 35%. At lower bias $V_{DS} = 30 \text{ V}$, the power density is 6.7 W mm^{-1} with an associated PAE of 55%. Very promising hybrid single-stage X-band amplifiers are demonstrated by Hughes in [2.292] yielding output power values of $\geq 22.9 \text{ W}$ with a cw-PAE as high as 43%. More recent GaN MMICs in microstrip transmission-line technology are given in [2.313]. The devices with a gate length of 150 nm use a field plate. Output power levels of 20 W with 43% PAE are reached in pulsed-operation. The III-N activities of Raytheon for high-power and low-noise X-band applications are discussed in [2.210]. PAE, uniformity, and reliability are considered the main challenges for the application of GaN HEMTs in TRX modules. The thermal management considerations in [2.210] further predict an order of magnitude increase in heat removal within a TR module with the insertion of GaN technology. With the application of innovative power combining techniques, multichip solid-state power amplifiers with overall 150 W output power levels are announced for X-band [2.79]. The PA is based on 16 chips similar to those reported in [2.81]. On hybrid packaged transistor level, Toshiba developed a 11.52 mm -gate-periphery GaN HEMT with a maximum output power of 81 W in cw-operation. The PAE amounts to 34% at 9.5 GHz and a gain compression level of 3 dB [2.444]. The unit gate width is $160 \mu\text{m}$ and no field plate technology is used for a gate length $l_g = 0.7 \mu\text{m}$. A similar result is obtained with a gate periphery of 12 mm and a gate length $l_g = 0.5 \mu\text{m}$ with a hybrid AlGaN/GaN HEMT. The two chip device yields an output power of $\geq 60 \text{ W}$ and a maximum PAE of 35%. The linear gain is 10 dB at a duty cycle of 10% and $V_{DS} = 40 \text{ V}$ in Class-B operation [2.518].

Double Heterostructure Devices

Double heterostructure devices overcome the disadvantage of the single heterostructure, which provides only limited electron confinement in the channel. The second heterojunction reduces the poor pinch-off characteristics and high-output conductance, which both degrade power performance and PAE at RF-frequencies for single heterojunction devices [2.289]. Initial reports on AlGaN/InGaN/AlGaN double heterojunction devices (DHFETs, DHHEMTs) based on the AlGaN/InGaN material system are given in [2.425], as also mentioned in [2.210]. The AlGaN/InGaN/GaN provided an initial output power of 6.3 W mm^{-1} at 2 GHz and $V_{DS} = 30 \text{ V}$. Very promising AlGaN/GaN/AlGaN

DHFETs on s.i. SiC for microwave and millimeter-wave power applications are given in [2.289], grown by MBE at HRL. The DHFETs yield higher transconductance and lower output conductance than SHHEMTs. PAE improvements of 10% are found at 10 GHz for a process with a gate length of 150 nm at $V_{DS} = 30$ V, while the power density is maintained.

Ku-Band (12.4–18 GHz) and K-Band (18–26 GHz)

Ku-band amplifiers find their applications in radio communication systems, such as satellite and mobile phone systems for point-to-point communication [2.314] and for military applications. Traveling-wave-tube amplifiers with very high efficiency levels of 70% and output power levels of 150 W with low weight are given in [2.288]. GaAs-based solid-state reference amplifiers for Ku-band operation can be found, e.g., in [2.314, 2.468], with a 40 W Ku-band high-efficiency hybrid solid-state power amplifier (SSPA). A good comparison of GaAs MMICs is given in [2.249]. Typical MMICs yield maximum output power levels of 5–10 W and PAE levels of $\geq 30\%$. References for conventional HPAs in efficiency-critical applications at K-band can be found in [2.24] based on InP HBTs. Output power levels of 870 mW are found at 20 GHz and 37% PAE. Initial reports of K-band power operation of III-N devices are given in [2.479, 2.505] with an output power density 3 W mm^{-1} at 18 GHz and 20 GHz for AlGaN/GaN HFETs on s.i. SiC substrate. AlGaN/GaN HEMTs operating at 20 GHz with a cw-power density $\geq 6 \text{ W mm}^{-1}$ are reported in [2.312]. For applications requiring high efficiency, such as satellite communication, a power density of 3.2 W mm^{-1} with an associated PAE of 71% using AlGaN/GaN HEMTs at 20 GHz is reported in [2.399], again for a small gate width device. A power density of 6.7 W mm^{-1} at 18 GHz is reported in [2.227] with an associated PAE of 26%. Even higher power densities at 18 GHz have been achieved using field-plated gates, however, with a gain of only 5.8 dB in [2.226] for a small gate width of 100 μm . An output power density of 5.1 W mm^{-1} is reported for AlGaN/GaN HEMTs on silicon substrate in [2.93]. The devices have a periphery of 100 μm . Residual challenges for Ku-band devices include the increase of power-added efficiency for large periphery devices in applications requiring high efficiency, as GaAs PHEMTs and InP HEMTs have set high standards with respect to this requirement, e.g., [2.24, 2.466].

MM-Wave Frequencies

MM-wave operation of GaN FETs beyond 30 GHz has been demonstrated with improved material homogeneity and an increasing number of electron-beam T-gate processes being available on s.i. SiC, e.g., in [2.179].

Ka-Band (26.5–40 GHz)

GaN HEMTs are very attractive devices for Ka-Band MMIC applications due to their combination of high-speed and high-power performance [2.354].

State-of-the-art GaAs-PHEMT-based reference devices and MMICs can be found, e.g., in [2.214, 2.266] and the references therein. A record compact size MMIC with an area of only 9 mm^2 and 4 W of output power level at 30 GHz is given in [2.215]. Power levels of 10 W at Ka-band can be reached with the grid amplifier concept [2.88] or up to 6 W on MMIC level, see [2.266]. Early reports on short-gate-length AlGaN/GaN devices with a gate length $l_g = 0.12\text{ }\mu\text{m}$ with high contact resistance R_C demonstrate current gain cut-off frequencies $f_T = 46\text{ GHz}$ and $f_{\max} \geq 100\text{ GHz}$ in [2.58]. More recent devices with the same gate nominal gate length yield a cut-off frequency f_T of 120 GHz [2.228]. State-of-the-art cw-power densities achieved at 26 GHz with AlGaN/GaN HEMTs on s.i. SiC substrate are reported in [2.241] yielding a power density of 5 W mm^{-1} and a linear gain of 7 dB with an associated PAE of 30.1% at $V_{DS} = 25\text{ V}$. Former TRW, now NGST, demonstrated power operation with 1.6 W mm^{-1} power density at 29 GHz and an associated PAE of 26% in [2.430, 2.431] at an early stage. Ka-band MMICs with pulsed-output power levels of 11 W at 34 GHz are mentioned [2.436]. Strong contributions to AlGaN/GaN HEMT power operation in Ka-band are provided by NEC. They demonstrated power densities of 7.9 W mm^{-1} at 30 GHz for a $2 \times 60\text{ }\mu\text{m}$ device with a gate length of 250 nm in [2.233]. The device with a gate length of 90 nm yields an MSG of 8.3 dB at 60 GHz. Similarly, a cw-output power of 2.3 W at 30 GHz is demonstrated in [2.184] yielding a power-added efficiency of up to 50%. Further, a saturated output power of 5.8 W at 30 GHz for a GaN with $W_g = 1\text{ mm}$, a peak PAE of 43.2%, and a linear gain of 9.2 dB are demonstrated in [2.156, 2.157] using a gate length of $0.25\text{ }\mu\text{m}$ and small contact spacings of $0.7\text{ }\mu\text{m}$. For frequencies targeting, e.g., missile radar applications at 35 GHz, Triquint demonstrated saturated power densities of $\geq 4\text{ W mm}^{-1}$ with an associated PAE of 23% at 35 GHz in [2.240]. The device has a linear gain of 7.5 dB for a gate width $W_g = 200\text{ }\mu\text{m}$. Even higher peak PAE values of 53% have recently been reported [2.179]. An output power of 3.5 W at 35 GHz is demonstrated in [2.510] using AlGaN/GaN HEMTs on s.i. SiC substrate with a gate width of 1.05 mm and a gate length of $0.18\text{ }\mu\text{m}$. The compression level for the peak power is $P_{-2\text{ dB}}$. The prematched devices yield a linear gain of $\geq 8\text{ dB}$ at 35 GHz. Further results of field-plate devices evaluated at 30 GHz and 35 GHz are given in [2.508]. Output power levels of 8 W with an associated PAE of 31% at 31 GHz are reached in cw-operation. With the inclusion of an InGaN back barrier layer, a power density of 13.7 W mm^{-1} in cw-operation is obtained at 30 GHz and $V_{DS} = 60\text{ V}$. The associated PAE is 40% [2.509]. At even higher frequencies, 40 GHz power operation is investigated in [2.194, 2.376] yielding power densities of $\geq 1.2\text{ W mm}^{-1}$ and absolute power levels of 0.5 W. More recently, high performance AlGaN/GaN HEMTs with a power density of 2.8 W mm^{-1} at 40 GHz and a PAE of 10% are demonstrated in [2.44]. The gate length is $l_g = 0.18\text{ }\mu\text{m}$, and the gate width is $W_g = 0.1\text{ mm}$. Improved devices deliver 4.5 W mm^{-1} at 40 GHz [2.45]. MMICs in this technology with output power levels of 5 W at 30 GHz are given in [2.43]. The dual-stage design gives a linear gain of 13 dB and a PAE

of 20%. The output periphery is 1.6 mm. Even higher power densities have been achieved at 40 GHz. The power density amounts to 10.5 W mm^{-1} and 34% PAE at $V_{DS} = 30 \text{ V}$ for a $W_g = 2 \times 75 \mu\text{m}$ device [2.354]. The gate length is $l_g = 160 \text{ nm}$.

V-Band (50–75 GHz) and W-Band (75–110 GHz)

Solid-state-based power generation and amplification between 50 and 120 GHz is typically limited to power levels of 25 dBm, see, e.g., [2.155, 2.447]. Operation both at high-power levels as well as higher operation voltages is therefore desirable. The impact of III-N devices can thus be substantial. AlGaN/GaN dual-gate HEMTs on s.i. SiC substrate are used to demonstrate V-band power operation at 60 and 65 GHz in [2.377]. Power gain of 8 dB is reached at 60 GHz, the maximum power density is 0.5 W mm^{-1} at 60 GHz. For a gate length $l_g = 140 \text{ nm}$, a cut-off frequency $f_T = 91 \text{ GHz}$ is achieved in [2.164]. The f_{max} is as high as 122 GHz. Several results exist for the scaling of the gate length. Vertically scaled T-gated AlGaN/GaN HEMTs are reported in [2.45]. An extrinsic transconductance of 500 mS mm^{-1} is reported for devices with $l_g = 100 \text{ nm}$. The cut-off frequencies are $f_T = 125 \text{ GHz}$ and $f_{max} = 174 \text{ GHz}$. The first GaN W-band MMICs in microstrip technology are demonstrated by HRL [2.291]. The devices deliver output power levels of 316 mW at 80.5 GHz which have been obtained in cw-operation. The power density is 2.1 W mm^{-1} , the associated power gain amounts to 17.5 dB for three stages. On sapphire substrates, AlGaN/GaN HFETs with cut-off frequencies $f_T = 152 \text{ GHz}$ at $V_{DS} = 5 \text{ V}$ are reported for $l_g = 60 \text{ nm}$. Even higher cut-off frequencies $f_T = 181 \text{ GHz}$ and $f_{max} = 186 \text{ GHz}$ are reported in [2.143]. When changing the barrier material to InAlN, $f_T = 172 \text{ GHz}$ is achieved with a gate length of 60 nm [2.143]. These devices are not fully passivated. Passivated AlGaN/GaN HEMTs on s.i. SiC yield $f_T = 153 \text{ GHz}$ for $l_g = 90 \text{ nm}$ [2.355] with the application of a Ge-spacer technology. More of such high-speed specific process modules will be required; however, the potential of III-N HEMTs for mm-wave operation is visible.

RF-Noise Performance

Low-noise operation of III-N HEMTs is attractive due to the combination of high-carrier velocities, good carrier confinement in the channel, and increased robustness with respect to high-input power levels relative to other high-speed devices such as InAlAs/InGaAs HEMTs, AlGaAs/InGaAs PHEMTs, or Si/SiGe HBTs. Various overviews [2.353] and reports are available on the low-noise performance of GaN FETs. A matched minimum noise figure $N_{F,\min}$ as low as 0.72 dB at 8 GHz is reported in [2.262, 2.364] for a device with $l_g = 120 \text{ nm}$ and $W_g = 100 \mu\text{m}$. The associated gain is 12 dB at 8 GHz. The maximum G_{ass} is found for a drain current $I_D = 150 \text{ mA mm}^{-1}$, while the minimum noise figure is found for $I_D = 100 \text{ mA mm}^{-1}$. Minimum noise figures $N_{F,\min}$ of AlGaN/GaN HEMTs on s.i. SiC of 0.75 dB at 10 GHz and 1.5 dB

at 20 GHz are reported, respectively, in [2.220] for a $2 \times 60 \mu\text{m}$ device with $l_g = 150 \text{ nm}$. Fig. 2.19 gives the dependence of the noise figure $N_{F,\min}$ as a function of frequency for $I_{DS} = 100 \text{ mA mm}^{-1}$ in comparison to a GaAs PHEMT of the same gate length $l_g = 150 \text{ nm}$. The low-noise performance of GaN HEMTs on sapphire substrate as a function of aluminum concentration in the barrier layer on the device level is discussed in [2.261]. The intrinsic minimum noise figure $N_{F,\min}$ at a given frequency decreases nearly linearly with increasing Al-content between 20% (1.7 dB) and 35% (0.92 dB), measured at 12 GHz. GaN HFETs on s.i. SiC substrate with excellent low-noise performance at low DC-power levels and $V_{DS} = 1 \text{ V}$ are demonstrated in [2.153]. Devices with a thin AlGaN Schottky barrier layers of 15 nm are compared to devices with 30 nm barrier thickness. The $N_{F,\min}$ is below 0.8 dB across the 2–12 GHz frequency-band with associated gains of better than 12.5 dB for the device with the thinner barrier. The associated gain G_{ass} increases by 2 dB and the minimum noise figure $N_{F,\min}$ is reduced by 0.2 dB for the devices with the thinner barrier. On silicon substrates, very promising noise figures $N_{F,\min}$ at 10 GHz are reported for $0.17 \mu\text{m}$ gate length devices in [2.295, 2.296]. The $N_{F,\min}$ amounts to 1.1 dB at 10 GHz with an associated gain of 12 dB, measured at $V_{DS} = 10 \text{ V}$. The $N_{F,\min}$ at 18 GHz amounts to 1.75 dB. Low-power linearity of GaN HFETs on s.i. SiC is discussed in [2.364]. Overdrive testing and studies for the use of GaN LNA in synthetic aperture radar applications are presented, e.g., in [2.31]. MMIC-based LNA circuit examples on s.i. SiC substrates are given, e.g., in [2.31, 2.102]. These are further discussed later and in Chapter 6.

Indium-Based (H)FETs

The use of indium is also investigated in III-N heterostructure devices. Improvements in speed and effective mass similar to the (In)GaAs material system are targeted when indium is used in the channel. Further, the use of indium is discussed in order to reduce some of the high surface-charge density and strain issues causing dispersion, e.g., in [2.85, 2.284, 2.327]. The piezoelectric effects can be omitted for certain material compositions in InAlN/GaN HFETs. Further, the conduction band off-set is increased as compared to typical $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}$ HFETs [2.231]. HFETs can be realized in the (Al)GaN/InGaN, InAlN/GaN, and InAlN/InGaN systems. In addition, indium can further be used as a dopant in AlGaN/GaN HFETs to reduce interface roughness, e.g., [2.228, 2.240].

InAlN/GaN Heterostructure FETs

$\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ HFETs provide strong spontaneous polarization with very high sheet carrier concentrations $\geq 2 \times 10^{13} \text{ cm}^{-2}$ while the piezoelectric contribution is suppressed as the strain is minimized, as repeatedly stated [2.126, 2.186]. InAlN/GaN HFETs promise larger bandgap energies in the InAlN

barrier, a larger conduction band off-set at the channel interface, and thinner barrier layers [2.284]. The latter may be useful for the realization of mm-wave devices with high aspect ratio [2.126]. Very high drain current densities of 4.5 A mm^{-1} are expected for the InAlN/GaN HFETs [2.230], based on the high-sheet carrier concentration already demonstrated [2.84]. $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ single heterostructure HFETs grown by MOCVD on c-sapphire substrate are reported in [2.187]. With In contents $x = 0.04$ to $x = 0.15$ sheet carrier concentrations of $4 \times 10^{13} \text{ cm}^{-2}$ have been reached. For gate lengths $l_g = 0.7 \mu\text{m}$, cut-off frequencies $f_T = 11 \text{ GHz}$ and $f_{\max} = 13 \text{ GHz}$ are achieved. The performance of InAlN/GaN HFET with 60 nm gate length and f_T values of 170 GHz is already discussed above [2.143]. Unstrained $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{GaN}$ HEMTs on s.i. SiC are reported in [2.126]. With a gate length $l_g = 250 \text{ nm}$ a cut-off frequency $f_T = 43 \text{ GHz}$ is reached with a DC-transconductance of 355 mS mm^{-1} and a barrier thickness of 7.5 nm. The power densities at 10 GHz reach 2 W mm^{-1} with an associated PAE of 29%. The pinch-off voltage is -1.7 V .

InGaN/GaN Heterostructure FETs

On the device level, GaN/InGaN/GaN double heterostructure FETs are demonstrated in [2.85]. These DHHEMT structures are considered to be more stable with respect to device dispersion, as mentioned in [2.327]. Kelvin probe microscopy shows no change in the surface potential of InGaN DHHEMTs contrary to AlGaN/GaN HFETs. Device characteristics of GaN/In_{0.15}Ga_{0.85}N/GaN doped-channel double heterostructure HFETs are shown in [2.150]. The devices yield a maximum transconductance $g_{m,\max}$ of 65 mS mm^{-1} , a maximum drain current of 272 mA mm^{-1} , and current gain cut-off frequencies $f_T = 8 \text{ GHz}$ and $f_{\max} = 20 \text{ GHz}$ for a gate length of $1 \mu\text{m}$. The output power at 1.9 GHz is 26 dBm for a gate width of 1 mm, i.e., 0.4 W mm^{-1} . P-channel InGaN HFET structures based on polarization doping without external acceptor doping are discussed in [2.534]. The channel sheet carrier concentration is 10^{11} cm^{-2} with a hole mobility of $700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at $T_L = 66 \text{ K}$. The maximum drain currents measured at room temperature (RT) are extremely low. MOSFET InGaN structures are also reported. AlGaN/InGaN/GaN DHFETs using SiO_2 as a passivation layer and gate dielectric layer yield a saturated output power density of 6.1 W mm^{-1} at 2 GHz and $V_{DS} = 30 \text{ V}$ [2.426]. The maximum transconductance $g_{m,\max}$ amounts to 110 mS mm^{-1} for the MOSDHFET structure, while the simple DHFET structure yields 170 mS mm^{-1} . Pure InN/AlN MISFETs on Si(111) substrates are reported in [2.251]. A 26 nm-thick InN layer is grown by RF-plasma-assisted MBE (PAMBE) on AlN. A current density of $\geq 500 \text{ mA mm}^{-1}$ is reached with a very low breakdown voltage of 3 V and a threshold voltage of -7 V . These examples show the promising principle operation of indium-based FETs so far. The main emphasis of In-based development focusses on material growth, while the device development requires the suppression of leakage currents and the stabilization of the InAlN interface toward the dielectric.

2.5.6 Heterojunction Bipolar Transistors (HBTs)

The family of III-N-based field-effect transistors has been heavily exploited, as discussed in the previous sections. The use of bipolar transistors has also been considered; however, substantial hurdles have delayed the development of III-N-based bipolar devices. At the same time, very few reports exist on bipolar devices in the SiC material system, e.g. [2.532].

AlGaN/GaN Heterojunction Bipolar Transistors

Complications with the p-doping in GaN [2.218,2.225] in epitaxial design [2.23] and issues with the processing [2.283] known from the optoelectronic devices have interfered with the successful development of bipolar AlGaN/GaN transistors.

Performance Predictions of PNP- and NPN-Devices

Various theoretical predictions have been made about the possible performance of AlGaN/GaN heterojunction bipolar transistors. Performance predictions for npn- $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HBTs are given in [2.374]. Spontaneous and piezoelectric polarization are shown to have only minor impact on the device performance. Incomplete ionization and reduced activation of the base dopant are shown to be the main issues. Limiting factors and optimum design of npn- and pnp-AlGaN/GaN HBTs have been addressed and performances have been investigated by simulation in [2.311]. Again, the high-base resistance induced by the deep acceptor level is found to be one of the causes of limited current gain values for npn-bipolar devices. The analysis for pnp-devices indicates limited RF-performance caused by the reduced minority hole transport across the N-GaN base. Simulations of the characteristics of AlGaN/GaN heterojunction bipolar transistors are given in [2.234]. The 2D-simulations show the great potential of AlGaN/GaN HBT with high calculated β , high breakdown voltage BV_{CE0} of 55 V, and a maximum cut-off frequency $f_T = 18$ GHz. Similar optimistic predictions are given in [2.7]. Generally, AlGaN/GaN HBTs are discussed also for high operation temperatures, e.g., 300°C in [2.382], since the activation of the acceptor Mg-doping and the performance increase for higher operation temperatures. The measured current gain amounts to 10 for a $90 \mu\text{m}^2$ device at this temperature due to the reduction of the base resistance.

AlGaN/GaN Heterojunction Bipolar Transistors Fabrication

GaN/AlGaN HBT fabrication issues are discussed in [2.383]. A standard III-V HBT process is applied to material grown by both MBE and MOCVD, while the annealing temperature of the ohmic contacts is increased to 700–800°C. Current gain levels of 10 are reached at elevated temperatures of 300°C for both material types. At the same time, the junction leakage is significantly

increased at high temperature. However, remaining issues include these leakage currents and the reduced base conductivity. The main performance problem for HBTs is thus the reduced current amplification [2.283, 2.514]. Both the lifetime of 25 ps and diffusivity of electrons in Mg-doped GaN are found to be low compared to practical base width of, e.g., 100 nm. The collector leakage is correlated with the threading dislocation density. The maximum operation bias is 70 V. Selective area growth of AlGaN/GaN HBTs is used in [2.413] to analyze its potential advantages as compared to more traditional growth techniques by normal MOCVD. Both linear ohmic contacts and improved material quality and interfaces could be obtained by the use of this more complicated technique applying a two-step procedure for the base contact. Very high voltage operation ≥ 330 V with a high current gain of AlGaN/GaN HBTs using selectively regrown emitters on sapphire substrates is given in [2.513]. The high-breakdown voltage is attributed to the low-background doping level in the 8 μm -thick GaN collector and the suppression of leakage in the lateral base/collector junction due to etch damage in the 2–3 μm spacing. Further, the use of ELO growth, reducing the number of threading dislocations, significantly reduces the collector leakage [2.283]. Further analysis of the leakage currents is given in [2.514]. Anomalously high current gains at low current levels in AlGaN/GaN can be observed. The calculated extrinsic β of the devices can be misleading due to leakage and ohmic contacts parasitic contributions, while the intrinsic performance is low due to purely intrinsic effects. AlGaN/GaN HBTs thus have promising theoretical performance; however, this performance still cannot be exploited due to epitaxial and technological issues.

InGaN/GaN Heterojunction Bipolar Transistors

The problems of p-doping of binary GaN can be overcome by using InGaN as a base material. NPN-GaN/InGaN/GaN DHBTs on s.i. SiC substrates with current gains of 3,000 can be fabricated [2.270]. This is ascribed to the lower acceptor activation energies and higher overall doping activation, e.g., in $\text{In}_{0.14}\text{Ga}_{0.86}\text{N}$ [2.225, 2.269]. Active carrier concentrations of 10^{18} cm^{-3} can be achieved. The InGaN is regrown by MOVPE in this case.

Base transit time analysis in GaN/InGaN/GaN HBTs is performed in [2.70]. The contribution of the base transit time decreases with increasing temperature, while the collector transit time remains nearly constant. Similar to AlGaN/GaN devices, this behavior makes the devices more suitable for high-temperature operation [2.152]. Double heterostructure GaN/InGaN/GaN HBTs on s.i. SiC substrate are presented in [2.269, 2.271] and several of the doping and processing issues are resolved. The breakdown voltage of the DHBTs in [2.271] exceeds 50 V, while a low current gain is observed without the application of regrowth. Further improvements of the epitaxy by using base regrowth [2.270] and improved processing yield a current gain $\beta = 2,000$ in [2.271] for an emitter geometry of $50 \times 30 \mu\text{m}^2$. The maximum current is as high as 80 mA. Based of these developments, the further development of

the GaN/InGaN (D)HBT is a promising candidate to overcome some of the epitaxial and processing limitations.

2.5.7 MMIC HEMT Technology

Apart from demonstrations on the device level, the demonstration of microwave integrated circuits (MICs) and monolithic microwave integrated circuits (MMICs) is a core competence for any RF-technology. The state-of-the-art is discussed in the following with focus on the III-N issues.

High-Power MMIC Technologies

Coplanar Waveguide High-Power MMICs

Initial coplanar AlGaN/GaN HEMT MMICs on s.i. SiC substrates are reported in [2.133] for broadband applications. The transmission-lines have impedance levels between 30 and 80Ω . MMICs with saturated output power levels beyond 37 dBm are realized between quasi-DC and 8 GHz. Several demonstrations of high-power coplanar MMICs on s.i. SiC are available for X-band. They are given in detail in Chapter 6. Coplanar K-band MMICs on sapphire substrate are reported in [2.332]. The devices exhibit a small-signal gain of 10 dB and a 3 dB bandwidth of more than 4 GHz between 20 and 24.5 GHz. A 200 μm -thick SiN is used for the MIM capacitances, while WSiN is used for the resistors. Further details on the passive components are given in Chapter 8.

Microstrip Transmission-Line High-Power MMICs

The first complete microstrip transmission-line high-power MMIC technology on s.i. SiC for SiC MESFETs and AlGaN/GaN HEMTs is presented by Cree in [2.362]. A 24 W high-power amplifier at 16 GHz is presented. Specific via etching techniques are required, which will be detailed in Chaps. 4 and 8. Triquint announces a full GaN HEMT MMIC technology on s.i. SiC with a saturated power density of 12 W mm^{-1} at 10 GHz and an associated PAE=50% [2.467]. A similar microstrip MMIC process on silicon substrate is presented by Triquint in [2.109]. The silicon substrates are thinned to 100 μm in this case. The vias can be etched by standard Si processing equipment. The other passive components are not modified compared to the GaAs process. Further MMIC details are given in Chapter 6. At Ka-band, a comparison of both coplanar and microstrip line HEMT MMICs on s.i. SiC has been presented by HRL in [2.290]. The coplanar MMIC yields an output power of 1.6 W at 33 with 4 GHz bandwidth, while the MSL MMIC yields 2.2 W at 27 GHz with 8 dB gain between 24 and 32 GHz. When additional external tuning is used, a PAE of 27% is reached. The substrates are thinned to 50 μm . The via geometry is $30 \times 30 \mu\text{m}^2$. A recent report by NGST gives a dual-stage

MMIC power amplifier in microstrip technology with a pulsed-output power of 11 W at 34 GHz. The duty cycle is very low and unusual for the telecom application [2.436, 2.439].

Low-Noise MMIC Process Technologies

GaN HEMTs are attractive for LNA MMICs due to high sheet carrier densities n_{sheet} and high intervalley energy ($\approx 1.5 \text{ eV}$). One of the first GaN LNA MMICs is presented in [2.102]. A coplanar-waveguide dual-stage broadband LNA yielding a minimum noise figure of 2.4 dB and a gain of 20 dB between 3 and 18 GHz is presented in [2.102]. The devices are biased at 2.5 V $\leq V_{\text{DS}} \leq 4 \text{ V}$. The third-order intercept point is better than 34 dBm at 8 GHz, which demonstrates the good input linearity of the MMIC. The impact of linearity, high-input power levels, and a discussion of typical destruction levels in GaAs is given in [2.60]. Typical catastrophic destruction levels of GaAs PHEMT LNA MMICs amount to 20 dBm without additional circuitry [2.60]. GaN HEMTs with similar gate periphery can be driven to input power levels of 30 dBm without degradation of the output power. Further the exceptional linearity with an output intercept point of 43 dBm is proven. A full investigation of single- and dual-stage X-band LNAs, including linearity investigations, is presented in [2.220]. The trade-off between minimum noise figure at low $V_{\text{DS}} = 7 \text{ V}$ and good input and output linearity at high $V_{\text{DS}} = 25 \text{ V}$ is discussed. The noise figure of the full MMIC at X-band is mainly determined by the passive components. A coplanar C-band high-dynamic-range LNA MMIC has been presented in [2.515]. The noise figure is as low as 1.6 dB at 6 GHz and does not exceed 1.9 dB between 4 and 8 GHz. The input port of the circuit can endure up to 31 dBm of input power. The MMIC shows noise figures comparable to other semiconductor technologies, while the dynamic range and the survivability are strongly enhanced. A microstrip transmission-line technology on s.i. SiC substrate is used to demonstrate wideband dual-gate LNAs between 0.1 GHz and 5 GHz in [2.60]. A linear gain of 15 dB is found with a saturated output power of 33 dBm at a compression level at 13 dB. Further MMIC examples and design consideration are discussed in Chapter 6.

2.6 Applications Issues

A large number of possible applications has been suggested for III-N devices. Without taking into account all possibilities, some key applications are systemized in this section. A large number of overview papers have been provided on this issue in the literature. The impact of wide-bandgap microwave devices on defense and naval systems is discussed in [2.105, 2.189]. Specific overview articles on radar applications are given, e.g., in [2.104, 2.147, 2.263, 2.272]. The application in power systems is discussed in [2.470, 2.494]. Future directions and technology requirements of wireless communication systems are discussed, e.g., in [2.116, 2.309].

2.6.1 Broadband Communication

The most important nonmilitary application of III-N devices is the partial replacement of Si LDMOS transistors in base-station applications for mobile communication. For such broadband/multiband communication applications the following advantages for wide bandgap semiconductors are typically named:

- The increase in relative bandwidth for a given power level
- The higher output impedance level to match, i.e., higher impedance and reduced C_{ds} per unit gate width for load matching
- Increased efficiency through new circuit and system concepts
- Improved linearity for the same output power
- Thus increased linear output power
- A Reduction of memory effects
- Potentially, less effort for the thermal management based on high-temperature operation

Examples for the development of device and amplifiers in L-band and S-band are given in Chaps. 2 and 6.

2.6.2 Radar Components

The particular application of III-N solid-state high-power amplifiers and low-noise amplifiers is discussed for radars for several reasons. The particular applications include:

- Active electronically scanned arrays (AESA)
 - For airborne radars [2.104, 2.272],
 - For ground-based air defense radars [2.272],
 - For naval radars [2.147]
- For airborne and spaceborne reconnaissance systems, e.g., [2.263]

Radar applications are the main drivers in the development of the III-N electronic materials. The fundamental improvements through the use of wide bandgap amplifiers involve on the system level:

- Better power×aperture gain [2.535]
- The possibility of high-power ultra-wideband (UWB) systems [2.147, 2.272]
- And higher reliability and survivability

The resulting improvements on the device and module level for defense applications include:

- Increasing power-added efficiency on system level by the increase of operation bias
- Elevated temperature operation allowing for reduced cooling [2.147]
- Reduced cooling through higher junction temperatures [2.124]

- Reduced limiter usage in the receiver path [2.272]
- Increased absolute output power levels [2.147]
- Improved reliability and increased system availability due to graceful degradation [2.263]
- Higher robustness with respect to supply voltage variations [2.263]
- Possibly the use of modulation schemes for increased functionality [2.147]

The frequency ranges involve S-band, C-band, X-band [2.104], and potentially Q-band [2.384]. Ultra broadband electronic warfare applications will further involve the range from 6–18 GHz [2.272]. In addition, Ka-band missile applications at 35 GHz are being discussed [2.179].

2.6.3 Electronics in Harsh Environments

As for other wide bandgap materials, nitride semiconductors have been suggested for their application in harsh environments, such as:

- Airborne operation [2.147]
- Space applications with high radiation levels, elevated temperatures, and strong temperature gradients [2.263]
- Space applications with requirements for reduced volume, reduced weight, and energy consumption [2.263]
- Car engines, i.e., microwave ignition [2.252] and energy-efficient DC–DC-conversion [2.470]

The particular functions include:

- RF-power sources and power generation [2.180]
- Highly linear RF-mixers [2.13]
- Robust RF-receivers [2.262, 2.364]
- DC–DC-conversion [2.470]
- Chemical sensors [2.365]
- Fluid sensors [2.285], biogen sensors [2.365], and (combustion) gas sensors [2.200, 2.365, 2.402, 2.458]
- Pressure sensors [2.175]
- Strain sensors [2.365]

A good overview of the sensor capabilities of GaN, especially with respect to its pyroelectric capabilities, is given in [2.10]. A sensor array using conventional semiconductor arrays for the operation regime between 200°C and 400°C is given in [2.461]. Various gaseous constituents can be discriminated. Gas sensors for hydrogen and propane are reported, based on MOSFETs in [2.176], and, based on n-type GaN and Pt-based Schottky contacts operating at 400°C, in [2.265]. Pressure sensors based on the pressure-induced conductivity changes in AlGaN/GaN HEMTs on Si substrates are reported in [2.175]. The pressure dependence can be used in pressure sensing applications; however, the pressure dependence poses also serious consequences on

the variation of the wafer bow and overall strain when dicing and handling the device.

2.7 Problems

1. Summarize the substrate situation for III-N electronic devices.
2. Given all the advantages named in the text, name at least three technical disadvantages of III-N semiconductors with respect to epitaxy and technology.
3. Name the advantages of double heterostructure devices relative to single heterostructure devices.
4. To this date, what are the shortcomings of AlGaN/GaN heterostructure bipolar transistors?
5. Do you expect a difference for unipolar and bipolar devices with respect to the influence of the substrate? Discuss!
6. Calculate the cross-section of a copper wire to be able to transport 1 W of DC-power for an operation bias at 5 V and at 50 V.

Epitaxy for III-N-Based Electronic Devices

Epitaxy is a core competency for the production of III-N devices. In this chapter, growth procedures for gallium-, aluminum-, and indium-based binary and ternary compounds are described with emphasis on AlGaN/GaN-, InGaN/GaN-, and (In)GaN/InAlN-based heterostructure systems. Nitride-specific material characterization, doping, and material quality issues are analyzed. Unlike Chapter 2, this chapter systematically reviews substrate properties with respect to the requirements of electronic device growth. This chapter mainly addresses the growth of both metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). In general, MOCVD growth of GaN is performed at much higher temperatures (well above 1000°C) than MBE growth, which is typically performed at temperatures of about 700°C [3.205,3.206]. MBE growth enables the growth of very precise interfaces, which improve transport properties. The two methods can also be combined, e.g., to a methodology called migration-enhanced MOCVD, as described, e.g., in [3.44]. Other techniques such as hydride vapor phase epitaxy (HVPE) have also been mentioned, but do not play a dominant role for the fabrication of the active layers.

Surface Preparation

Specific surface preparation methods have been developed, which improve the surface roughness before epitaxial deposition and are used prior to the actual growth procedure. Further, specific procedures assure that the reactor spaces are not contaminated by extrinsic pollution. Standard surface-polishing techniques are based on plastic deformation by an abrasive, e.g., diamond. Electrochemical-mechanical polishing procedure (ECMP) improves the reproducibility of the epitaxial growth and is preferred to purely mechanical polishing (CMP), as the induced subsurface damage is reduced. A proprietary ECMP process of SiC applied by NovaSiC is mentioned in several publications, e.g., in [3.154,3.162,3.216]. A full description of a two-step ECMP procedure is given in [3.112]. The procedure is characterized by a balance of anodic oxidation and oxide removal [3.216] to obtain a defect-free surface of the substrate.

A high-temperature hydrogen etching process is used to further smooth the surface to atomic levels. On the device level, a correlation of the gate-leakage current and substrate defects in 2-in. SiC substrates is given in [3.126]. A clear correlation showing a reduced yield of the FETs for an increased defect density in a particular area is visible. The increased defect concentration in selected areas of the wafer leads to a statistical increase of the gate leakage current of about 100% measured at $V_{DS} = 20\text{ V}$.

Substrate Surface Cleaning and Backside Metallization

Further wafer preparation includes the deposition of a Ti layer on the backside of the transparent substrate prior to growth to provide an effective heat transfer [3.162], typically for MBE growth only. A sputtered Mo thermal-contact layer is used for ammonia MBE in [3.213]. Various surface heating procedures have been reported for the in-situ preparation of the substrates within the reactor chambers or preparatory chambers. Prolonged heating of Si(111) for up to 10 h at 600°C with subsequent oxide removal by rapid thermal annealing is reported, e.g., in [3.180]. An ex-situ exposure to hydrogen at 1,600°C is reported in [3.205] prior to an in-situ surface cleaning by Ga deposition and desorption within the reactor chamber. The impact of reactor loading leakage and the impact of the contamination of sapphire substrates is discussed in [3.94]. Various cleaning conditions and sequences with prebake and flush for moisture removal prior to growth are discussed. A potential reaction is the composition of H_2O from hydrogen and Al_2O_3 . Oxygen incorporation serving a shallow donor is considered a major obstacle for semi-insulating GaN. The investigation includes a prebake of the sapphire and a flush of the substrates by hydrogen between 10 min and 12 h. The optimized procedure includes both the prebake in-situ and no flush, and is critical in order to obtain semi-insulating GaN buffers.

3.1 The AlGaN/GaN Material System

The growth of AlGaN/GaN heterostructures is a basic technology for the production of high performance HEMT and HBT devices. General overview articles and comparisons between the various growth methods for the AlGaN/GaN system are given, e.g., in [3.36, 3.39, 3.138]. An overview of MBE growth of AlGaN/GaN heterostructures is given in [3.172].

3.1.1 Metal Organic Chemical Vapor Deposition (MOCVD)

Metal organic chemical vapor deposition (MOCVD) is the name of a growth technique that involves a dynamic flow in which gaseous reactants pass over a heated substrate and react chemically to form a semiconductor layer [3.36]. It is widely spread for the fast and precise growth of many III-V materials,

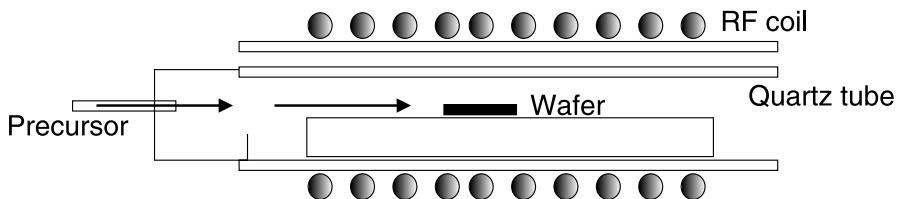
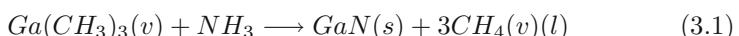


Fig. 3.1. Scheme of metal organic chemical vapor deposition (MOCVD) growth

e.g., for InGaP/GaAs [3.156] and $In_{0.53}Ga_{0.47}As/InP$ [3.61]. III-N MOCVD-based material growth is very attractive due to the large amount of experience and success available from the growth of optoelectronic devices, e.g., [3.141], and the increased growth rates relative to molecular beam epitaxy (MBE). Thus, MOCVD is widely used for the growth of heterostructures for electronic applications [3.94]. Fig. 3.1 gives a schematic view of MOCVD growth of III-N materials. The precursors TriMethyl-Gallium (TMGa), TriMethyl-Aluminum (TMAI), and TriMethyl-Indium (TMIn) react with ammonia (NH_3) on the hot substrate surface to form semiconductor layers. Additional sources such as nitrogen, silane (SiH_4), disilane (Si_2H_6) [3.48], and Bis(cyclopentadienyl) magnesium (Cp_2Mg) sources [3.105,3.121] are needed. The substrate is located on top of a graphite susceptor. Various reactor concepts have been developed [3.1,3.142] to accomplish and optimize the laminar flow of gases on larger area surfaces [3.7] and within multi-wafer concepts, e.g., in [3.48,3.192,3.221]. Both reactor concept and geometries, often kept proprietary, influence the growth conditions to a high extent. This fact also limits the comparability of parameters such as growth temperature, gas flows, and others parameters, which are adjusted externally. However, a principal understanding of the requirements for III-N growth can be obtained.

Growth Chemistry

The growth kinetics and chemistry of III-N semiconductors by MOCVD are described in various publications which shall be briefly mentioned here [3.138, 3.167, 3.169, 3.172]. The details of the complex reactions are not fully understood and especially the intermediate reactions are found to be very complex. The principal reaction to form GaN reads [3.142]:



A similar reaction occurs for AlN(s) replacing gallium by aluminum. The chemistry is governed by strong reactions of the precursors at room temperature. Further ammonia requires pyrolysis, which is not very efficient. Thus, high growth temperatures beyond $1000^\circ C$ are used along with high V/III-ratios (>1000) and high gas velocities.

Optimized Conditions for MOCVD Growth

One of the key advantages for the AlGaN/GaN material system is based on the fact that the complete range of solid solutions from GaN to pure AlN is available using MOCVD growth. Typical growth rates for GaN are about $2 \mu\text{m h}^{-1}$ [3.219]. Overview articles of the development of the growth conditions of AlGaN/GaN heterostructures are reported, e.g., in [3.34, 3.92, 3.168]. The aluminum content or mole fraction x in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures is varied between 0 and 0.6 in [3.92]. The defect density in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer on GaN is found to increase significantly for $x \geq 0.3$ for typical barrier thicknesses of 18 nm for AlGaN/GaN HFETs. Further, the mobility in GaN channels along AlGaN/GaN hetero-interfaces decreases with decreasing barrier-layer thickness and with increasing Si-doping concentrations. Sheet carrier concentrations of $1.8 \times 10^{13} \text{ cm}^{-2}$ are reached at $x = 0.44$. The AlGaN-spacer thickness between the channel and the Si-doped barrier layer is varied between 0 and 3 nm. A mobility of $1,650 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT is found for 3 nm thickness. The sheet carrier concentration decreases from 1.5 to $0.8 \times 10^{13} \text{ cm}^{-2}$ with the increase of spacer thickness from 0 to 3 nm. Very good layer properties and reproducibilities have been reported for optimized growth conditions on two-inch and three-inch wafers, e.g., in [3.221]. The wafer-to-wafer variability of the sheet resistance mapping is $\leq 3\%$ on 3-in. s.i. (0001)SiC wafers. The critical growth parameters will now be discussed in detail.

Growth Temperature Schemes: Nucleation and Buffer for MOCVD

The growth temperatures critically determine the properties of the semiconductor layers. A typical temperature scheme for the growth of an AlGaN/GaN heterostructure sequence is given in [3.94]. On sapphire substrates, a 15–25 nm thick AlN nucleation layer is used in a growth temperature range of 500°C to 700°C. The consequent growth of the main GaN buffer layers is performed at $\geq 1,000^\circ\text{C}$. For all temperatures, the changes of the growth temperature due to different thermal contacting at the backside of the substrate have to be considered. A GaN nucleation temperature of 550°C on 2-in. sapphire substrate is reported in [3.218]. A slightly misoriented grain morphology is obtained, which results in poor electrical properties. Growth at a temperature of 530°C for the nucleation layers is reported in [3.192] on 3-in. sapphire substrates. The growth of AlN as a nucleation layer on sapphire substrate with a temperature of 500 to 700°C is reported in [3.219]. Above the AlN nucleation layer, all layers are grown at much higher temperatures, especially the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ heterobarrier. AlGaN-based nucleation layers for growth on s.i. SiC substrates are reported in [3.185]. Defect-poor surfaces on top of GaN buffer layers with thicknesses up to 5 μm can be observed optimizing the alloy composition and thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ nucleation layers. The deposition temperatures of the $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$ nucleation layer amount to 1,010°C on s.i. SiC and 1,040°C on sapphire for the same nucleation. The minimum Al-content is 6% for SiC nucleation and 15% for the nucleation on sapphire.

AlGaN nucleation on s.i. SiC substrates has also been reported in [3.102]. The thickness of the nucleation layer is 500 nm, followed by the GaN buffer. Growth of AlN nucleation layers on SiC is another standard procedure and has repeatedly been investigated, e.g., in [3.103]. The temperature is varied in [3.103] depending on the crystal structure of the n-type SiC substrate: A nucleation temperature of 1,080°C is used for the 6H-SiC substrates, while 980°C is used for 4H-SiC substrates. The thickness is 100 nm in both cases. The hotter growth for the 6H-SiC substrates shows smaller grains than for the growth on 4H-SiC, which means that the morphology of the AlN influences the quality of the subsequent layers. The specific nucleation of III-N materials on Si substrates is discussed below.

Growth Temperature Schemes: Channel and Barrier

The substrate temperatures reported for the growth of conducting GaN by MOCVD typically exceed 1,020°C [3.219]. The associated growth rate is $1.2 \mu\text{m h}^{-1}$. A growth temperature of 1,080°C for the growth of the main GaN layer is reported using hydrogen as a carrier gas in [3.93] on sapphire substrates. Growth temperatures of 1,180°C are reported for the GaN channel and the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ heterobarrier in [3.174] on sapphire substrates. An analysis introducing additional layers in the buffer layer is given. The growth temperature is chosen accordingly for Al-, In-, and Ga-based binary and ternary semiconductors within the interlayer. A temperature of 1,125°C for the growth of $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}$ in the heterostructure is reported in [3.93]. The impact of the variation of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ growth temperature between 1,060 and 1,125°C is reported in [3.92]. The Al-incorporation changes from 0.37 to 0.42 at otherwise constant conditions with the variation of the growth temperature from 1,060 to 1,125°C. Hot growth of the AlGaN layer is considered promising in [3.93] with respect to the output power, while a termination of the growth in the cool-down using nitrogen is found to be most suitable, again with respect to output power considerations of the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}/\text{GaN}$ HEMTs realized on SiC. Highly-resistive thick $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ layers grown by MOCVD at 1,150°C are reported in [3.23]. When the growth temperatures of $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ are reduced to 920°C and silicon and indium codoping are applied, highly conductive $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ layers are reported. Mobility values of $22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and bulk carrier concentrations of $2.5 \times 10^{19} \text{ cm}^{-3}$ are reached. The termination conditions of the semiconductor surfaces are discussed below with the specific methodology, e.g., cap layers [3.30, 3.93], or in-situ passivation layers, see [3.133].

MOCVD Gas Flow and Group V/III Ratio

Similar to the growth temperature discussed in the previous section, the element group-V/group-III ratio is of critical importance for the material properties. A nitrogen-rich growth is necessary in general because of the very different

chemical bindings and, to a lesser extend, different atomic weights of the constituents N and group III-metals [3.142]. The absolute and relative gas flows and pressures are quantities that are strongly dependent on the susceptor and reactor geometries. Several reactor-specific investigations are available in the literature, e.g., in [3.1, 3.23, 3.92]. Optimization of the GaN nucleation layer on sapphire substrates as a function of nitridation conditions, group V/III ratio, growth temperature, and growth pressure is discussed in [3.218]. TMG flows of $32\text{ }\mu\text{mol min}^{-1}$ and NH_3 flows of 0.09 mol min^{-1} , i.e., N-rich conditions, are reported for GaN growth. The V/III ratio is thus 2,775. A group V/III ratio of 1,800 for GaN growth and 900–1,800 for AlGaN growth by MOCVD are reported in [3.39] for $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}/\text{GaN}$ heterostructures on SiC and sapphire. A group V/III ratio of 2,000–2,600 is reported in [3.219] for the growth of GaN. In a comparison of two reactor concepts, a V/III ratio of 2,660 is reported for the growth of the GaN channel-layers on AlN nucleation layers in a so-called showerhead reactor in [3.219]. In a second quartz tube reactor, a group V/III ratio of 2,000 is used for the same TMG flow of $23\text{ }\mu\text{mol min}^{-1}$. A V/III ratio of 2,100 is reported for GaN growth at a growth temperature of $1,030^\circ\text{C}$ in [3.218]. The V/III ratio is increased to 2,775 for a growth temperature of $1,065^\circ\text{C}$ to accommodate for the increased N-desorption.

Growth Pressure

The pressure in MOCVD is the most fundamental parameter next to temperature and V/III ratio. It basically determines the incorporation of the various constituents like the group-V and group-III materials, including group-IV dopants like Si and C. The influence of growth pressure on the morphology and carrier compensation in GaN and related alloys is described, e.g., in [3.219]. For very low pressures of 40 Torr, the GaN layers are highly resistive and yield very low carrier mobility nearly independent of the growth temperature. Very high growth pressures at 200 Torr and beyond lead to the loss of the resistive nature of GaN, e.g., at atmospheric pressure [3.6]. In an intermediate growth pressure range, both high mobility and high resistivity (i.e., low nonintentional doping) can be reached in GaN Layers. Optimized growth pressures of 130 and 65 Torr are reported for GaN layers [3.219].

Similar reports of a pressure of 76 Torr are given in [3.39] for $\text{Al}_{0.35}\text{Ga}_{0.65}\text{N}/\text{GaN}$ heterostructures, and 100 mbar for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HFET layers [3.48]. Further results at a growth pressure of 76 Torr are reported in [3.218] for the growth of the GaN nucleation layer on sapphire, while 150 Torr is used for the rest of the layers. This pressure, at which pressure prereactions occur, is strongly dependent on the reactor geometry. This critical pressure is found to be 150 Torr for GaN for the reactor used in [3.218]. For the growth of $\text{Al}_x\text{Ga}_{1-x}\text{N}$, the pressure dependence is modified depending on the Al mole-fraction [3.92]. For a given V/III ratio and growth temperature, the Al-mole fraction is particularly influenced by the partial pressures of Al and Ga, and their deviation from the equilibrium partial pressures, as further detailed in [3.92]. Thus, lower pressures than for optimized GaN layers

are needed for good Al-incorporation in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layers, as reported in [3.219]. A medium growth pressure of 76 Torr is reported in [3.94, 3.185] for the growth of $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}/\text{GaN}$, due to the tendency of TMAl to form adducts with ammonia. At this pressure of 76 Torr, such prereactions are still not fully suppressed. Again, their occurrence is again strongly reactor-dependent. Relatively high pressure of 300 mbar is reported for the growth of $\text{Al}_{0.33}\text{Ga}_{0.67}\text{N}/\text{GaN}$ heterostructures in [3.93]. The high pressure growth also leads to increased incorporation of nonintentional doping such as C and Si.

Crystal Misorientation

The control of the misorientation of the substrate as compared to the III-N layers is of further importance for the layer quality. Growth of GaN on both on-axis and off-axis 6H-SiC substrates is reported in [3.103]. A 3.5° off-axis 6-H substrate is used for comparison. A strong impact on the surface conditions has been repeatedly reported, e.g., [3.103]. However, the impact of the misorientation on electronic device performance is not yet fully understood. This is due to the lack of SiC substrates that are oriented according to tight specifications with respect to the misorientation.

The slight misorientation from c-plane (0001)-sapphire substrates is well investigated for optoelectronic applications [3.58]. The emission from the photoluminescence of material on misoriented substrates is higher than for the on-axis material. The impact on GaN LED output power is further investigated in [3.228]. For the misorientation of 0.17° the morphology changed to small-step-type morphology. However, the optical output powers of the GaN LEDs are nearly identical despite the misorientation. The impact of the different optical surface properties has also to be considered.

For 4H-SiC and 6H-SiC substrates reports on the impact of the misorientation on layer and device performance are available [3.145, 3.171, 3.189, 3.195]. MOCVD-grown GaN epitaxial layers show a good morphology for on-axis substrates, while the crack density increases with the increase of the misorientation in [3.171].

This effect can be overcompensated by other growth parameters, such as the growth temperature, as shown for GaN diodes on 4H- and 6H-SiC in [3.145] and for heterostructures in [3.103]. An increase of the mobility and a carrier reduction in Si-doped GaN films is obtained with a slight misorientation of 3.5° compared to the on-axis layer. Positron annihilation spectroscopy shows that with increasing misorientation on 4H-SiC the concentration of nitrogen vacancies in GaN increases, while the number of shallow traps decreases [3.195]. This can potentially have an impact on device isolation in the buffer layer, if the misorientation is not controlled. With the application of MBE growth the importance of the misorientation rises, as described in [3.189]. The morphology of GaN grown on 4H-SiC(0001) with a very strong misorientation of 8° is strongly affected by undulations, while this is not the case for a misorientation of $\leq 0.3^\circ$. Deduced from that, a controlled misorientation

can be useful for the electronic device performance, if the growth parameters are properly matched.

Nucleation Layer

The conditions for the growth of the nucleation layer are critical for the defect concentrations, residual conduction, and the distribution of the defects and traps in all layers grown on top of it [3.103,3.185]. The nucleation layer is naturally highly dependent on the substrate choice. Several nucleation approaches have been suggested, both AlGaN (on SiC and sapphire), GaN (on sapphire), and AlN (on SiC and sapphire) nucleation have already been mentioned. The use of insulating AlGaN nucleation layers for the growth of AlGaN/GaN heterostructures on s.i. SiC and sapphire substrates is described in [3.185]. The nucleation layer thickness is 180 nm in this case. The TDD is about $5 \times 10^9 \text{ cm}^{-2}$. The impact of the nitridation and nucleation conditions of the growth on the low-temperature GaN nucleation layer on the morphology on sapphire substrate is investigated in [3.218]. Dislocation densities estimated by XTEM of less than 10^8 cm^{-2} are reported for a 2 μm thick GaN layer. The grain orientation can be improved with increased nitridation temperatures. Further, the quality of the epitaxial GaN is improved by increased growth temperatures and pressures. In [3.219], AlN nucleation layers are grown on sapphire substrates. Thicknesses of 20 nm are fabricated at a growth temperature of 500–700°C. The TDD varied only slightly with values of $1\text{--}2 \times 10^9 \text{ cm}^{-2}$. The nucleation on s.i. SiC can also be performed with AlN nucleation. The thickness of the nucleation layer is 120 nm in [3.183], which is higher than that for AlN nucleation on sapphire. The temperature dependence of the nucleation with AlN on SiC has already been discussed [3.30]. The AlN thickness is 100 nm in this case. The optimization of the nucleation layer is further monitored by the drain-lag type of pulsed-measurements for processed HFETs, as discussed in Chapter 5.

Buffer Isolation

The growth of the buffer layer in an AlGaN/GaN heterostructure is basically a trade-off between high isolation and surface morphology. For the buffer isolation, a minimum isolation requirement of $1 \times 10^7 \Omega \text{ cm} - 10^{11} \Omega \text{ cm}$ is suggested in [3.40,3.139]. Earlier examples include values of $10^5 \Omega \text{ cm}$ in [3.219] for high-resistivity GaN layers. The impact of the growth temperature of a GaN buffer between 1,070 and 1,150°C is discussed in [3.139]. Buffer isolation resistances between 10^4 and $10^{11} \Omega \text{ cm}$ are reached. Relatively higher growth temperature yield increased isolation in this regime. Further, it is mentioned that the isolation reduces by an order of magnitude when the test bias is switched from 2 to 40 V. The impact on surface morphology is also discussed in a trade-off, as hotter growth temperatures increase the surface roughness.

Buffer-Layer Thickness

The overall thickness of the epitaxial layers in the hetero-epitaxy is determined by the buffer layer, which varies between 350 nm [3.5], approximately 3 μm , e.g., in [3.139] and 5 μm in [3.132]. The impact of buffer layer thickness is discussed in more detail in [3.5]. A minimum thickness of 350 nm is used. The thickness is varied in the following trade-off. Thin buffer layers promise reduced thermal impedance and low growth time, while the growth of thicker layers reduces the effect of threading dislocation density TDD and the effect of the residual strain from the lattice-mismatch [3.132]. Further, the surface morphology improves for the buffer thickness between 2 and 3 μm on sapphire substrates, as mentioned in [3.40]. GaN buffer layers grown by MOCVD with thicknesses up to 5 μm are reported in [3.132]. Thicker buffer layers promise smoother growth fronts with improved interface roughness, reduced dislocation density, and further removal of the active region from the defective nucleation layers. The negative impact of thicker buffers on the thermal resistance to the substrate is further discussed in Chapter 8. The impact of various buffer materials and interlayers, such as InGaN, AlGaN, and GaN, on wafer bowing, grown in various ways by MOCVD, is discussed in [3.174]. In general, multi-layer structures are found to enhance wafer bowing, see [3.5]. Recent reports demonstrate the introduction of thin (3 nm) InGaN layers in the buffer layer very close, i.e., at a distance of 10 nm, to the channel layer [3.154]. This is achieved in order to obtain a similar function as a real double heterojunction structure. A graded $\text{Al}_x\text{Ga}_{1-x}\text{N}$ -buffer approach grown by MOCVD is presented in [3.78]. The mole fraction x is varied from 0.3 at the nucleation layer to 0.05 near at the buffer channel interface. The thickness of the graded layer is 1 μm , the GaN channel thickness is 10 nm.

Codoping of the Buffer Layers

Unintentional codoping is a major problem for nonoptimized growth conditions [3.23, 3.94] in III-N semiconductors. Codoping introduces nonintentional background carrier concentration and thus persistent nonintentional conductivity. This fact has been the reason for a number of publications [3.6, 3.23, 3.94]. Nitrogen vacancies and oxygen serve as shallow donors [3.94] typically considered for GaN layers. Carbon prevails in the MOCVD reactor due to the methyl-precursors [3.28]. Mg and Fe are intentional dopants of interest, which, however, can be residual from reactor memory effects. In a number of the high-performance single-heterostructure devices, Fe or C [3.6, 3.63] are used to control the isolation in the buffer by pinning and thus stabilizing the Fermi levels through deep acceptors [3.28]. This codoping is one method used to control the Fermi-level in the buffer and to overcome the need for a second heterojunction. In [3.64], the use of Fe doping for applications in AlGaN/GaN HEMTs is described to improve the stability of the semi-insulating GaN layers and to reduce dispersion, especially the drain-lag. At the same time, the Fe doping does not modify the good structural quality of the layer. Thus the

improved isolation is achieved without a high TDD necessary to obtain good isolation without codoping. The impact of high-temperature rapid thermal annealing (RTA) on the properties of Fe-doped semi-insulating GaN is investigated in [3.164] at temperatures between 750 and 1,050°C. The Fe distribution is found to be nonuniform and to increase close to the interfaces. The Fermi-level is pinned at $E_C - 0.5$ eV. The paper also states a strong residual gradient and diffusion of the Fe concentration in the buffer layer, partly based on a memory effect [3.15]. The reduction of dislocation density on both sapphire and s.i. SiC substrates through intentional Fe codoping is investigated in [3.15]. High-resistivity layers are obtained by both modulation doping and continuous bulk Fe-codoping. The Ferrocene flux is modulated to overcome the maximum doping level of $1 \times 10^{19} \text{ cm}^{-3}$. A more detailed study of the Fe doping at the regrowth interface of GaN on a GaN on sapphire template is given in [3.111]. The Fe doping of the interface is found to be crucial for the quality of the transistor layers on top of a 2-μm thick buffer. These thick Fe-doped layer leads to good mobility and increased carrier concentrations in the active transistor layers while no charge is found at the regrowth interface.

The impact of the excess incorporation of carbon on the trap states in MOCVD-grown material is investigated in [3.6]. Low-pressure growth at 76 Torr, compared to 760 Torr, leads to increased C incorporation in the GaN layers grown at 1,040°C. Carbon is considered to supply shallow but also deep acceptor levels in n-type GaN. This carbon contributes to the compensation of free carriers. C-doped samples are found to be highly resistive, while codoping with both Si and C leads to highly compensated layers. This finding is of critical importance, as O and C are typically present in any MOCVD reactor chamber. Oxygen incorporation during MOCVD growth is investigated in [3.23]. Higher growth temperatures at 1,150°C lead to reduced oxygen and carbon incorporation at levels of 10^{17} cm^{-3} , while the incorporation of carbon and oxygen can be strongly correlated. Growth temperatures of 920°C for $\text{Al}_{0.65}\text{Ga}_{0.35}\text{N}$ lead to oxygen concentrations of up to $1.5 \times 10^{19} \text{ cm}^{-3}$ and carbon concentrations of $1 \times 10^{18} \text{ cm}^{-3}$. In-codoping further suppresses the formation of native defects with acceptor character. Doping compensation is further of critical importance for the device behavior at high voltages, as explained in Chapter 5.

Dislocations in MOCVD Material

The threading dislocation density (TDD) was already discussed with the lattice mismatch in Chapter 2. The TDD is naturally dependent on the substrate type and quality. TDDs of $\approx 5 \times 10^8 \text{ cm}^{-2}$ on s.i. SiC substrates and of low 10^9 cm^{-2} on sapphire substrates are reported for both MOCVD and MBE material in [3.39, 3.185]. These numbers are confirmed in a variety of publications, e.g., [3.36, 3.92]. MOCVD-grown material is analyzed by combined scanning capacitance microscopy and AFM measurements in [3.60]. Threading dislocations are found to be surrounded by a negative charge.

A TDD of $2 \times 10^9 \text{ cm}^{-2}$ is mentioned for optimized MOCVD-based epitaxy of AlGaN/GaN on 4-in. silicon(111) substrate [3.204]. A good overview on the strain engineering on Si(111) is given in [3.34].

Epitaxial lateral overgrowth (ELOG) by MOVPE allows a reduction of the TDD below $\leq 10^9 \text{ cm}^{-2}$ on sapphire substrates, as reported, e.g., in [3.86]. The leakage in AlGaN/GaN HBTs is reduced by an ELOG procedure with a concentration of threading dislocations of 10^8 cm^{-2} in the defect-reduced part. Areas with TDDs reduced to $\leq 10^6 \text{ cm}^{-2}$ in the defect reduced part are reported in [3.86]. However, these stripes are typically $10\mu\text{m}$ wide only. The use of ELOG of GaN on conducting 6H-SiC substrates can yield dislocation densities as low as $2.2 \times 10^7 \text{ cm}^{-2}$ in the wings (i.e., the defect-reduced area) and $2 \times 10^9 \text{ cm}^{-2}$ in the windows (defect-rich area), as reported in [3.53]. GaN laser growth requires a TDD of 10^6 cm^{-2} obtained with an effective lattice mismatch of 0.01% to the heterosubstrate [3.34]. The TDD in bulk AlGaN grown by MOCVD on SiC substrates for solar blind detectors is found to be higher than in GaN layers. The overall TDD (mostly edge type) reach $2-5 \times 10^{10} \text{ cm}^{-2}$ in the AlGaN, as shown in [3.157].

Partial dislocation annihilation by Si- δ -doping in GaN grown by MOCVD on silicon substrates is described in [3.31]. Screw dislocations are bent to neighboring dislocations, whereas edge dislocations are not affected by the burst of silicon during the growth. Fig. 3.2 depicts a GaN layer grown on sapphire(0001) (α -Al₂O₃) substrate to give a more qualitative image of the dislocation density. The GaN layer is etched by a photo-enhanced chemical (PEC) etching technique. The different etch rates in the area of the dislocations can be observed. Further, the extension of the dislocations is visible reaching 500 nm into the GaN layer. This fact requires a minimum buffer layer thickness to protect the actual device layers.

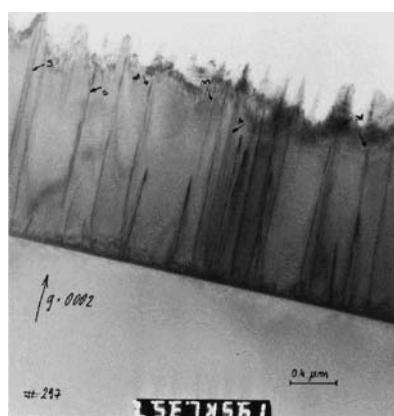


Fig. 3.2. SEM image of a PEC-etched GaN buffer on sapphire substrate

Impact of Growth on Carrier Mobility

Fig. 3.3 gives the temperature dependence of the drift mobility especially for temperatures lower than RT. Various mechanisms that influence the electron mobility can be separated. Data for both 2DEG AlGaN/GaN heterostructures and bulk GaN are given. The different contributions to the mobility lead to the overall mobility. The limiting effects dominating at different temperatures are the following:

- Impurity scattering dominating from below 70 K [3.144]
- Polar optical phonon scattering dominating above 70 K [3.21, 3.144]
- Acoustic phonon scattering [3.65, 3.101]
- Dislocation scattering
- Polar dipole scattering
- Interface scattering [3.4]

Impurity and polar optical scattering are the classical scattering mechanisms to reduce the mobility in the bulk, as described in [3.21], see Fig. 3.3. Acoustic phonon scattering is discussed in [3.65, 3.101] and found to be of significance. It can be distinguished from the other scattering mechanisms at temperatures below 20–50 K and plays a role in AlGaN/GaN heterostructures. Peak mobilities in 2DEGs of $80,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 4 K are observed for sheet carrier concentrations of $0.4 \times 10^{12} \text{ cm}^{-2} \leq n_{\text{sheet}} \leq 3 \times 10^{12} \text{ cm}^{-2}$ [3.65].

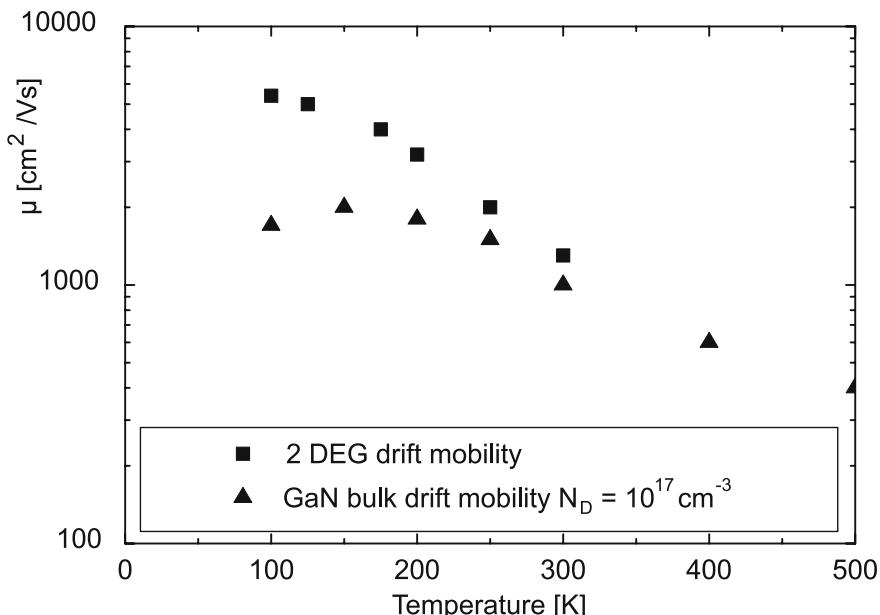


Fig. 3.3. Drift mobility as a function of lattice temperature in MOCVD material

Thus, for the III-N heterostructures, additional mechanisms prevail, which limit the mobility and which are discussed in [3.4, 3.80, 3.81]. Interface scattering is found to be relevant for carrier densities $\geq 7 \times 10^{12} \text{ cm}^{-2}$ [3.4]. For lower sheet carrier densities than $7 \times 10^{12} \text{ cm}^{-2}$, the mobility is limited by the interface charge and the related Coulomb scattering. Theoretical approaches to the additional dislocation scattering [3.80] and dipole scattering [3.81] are suggested. Dipole scattering of electrons in the heterostructures occurs due to the fluctuations from perfectly periodic dipole in highly polar semiconductors. Further, the high dislocation density of 10^8 cm^{-2} in AlGaN/GaN 2DEGs leads to an additional scattering mechanism [3.81]. However, mobilities of $51700 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 13 K are reached for carrier densities $\geq 2 \times 10^{12} \text{ cm}^{-2}$. The effect is different from the 3D-bulk impact of dislocations, as described in [3.120]. The drift mobility in heterostructure is further investigated, e.g., in [3.200]. The distinction of the carrier mobility between peak and the drift mobility in AlGaN/GaN heterostructures is made in [3.200]. Peak values of the mobility of $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for low carrier densities of $0.4 \times 10^{13} \text{ cm}^{-2}$ are found on s.i. SiC substrates, while the actual drift mobility at high carrier densities of $1 \times 10^{13} \text{ cm}^{-2}$ amounts to $1,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature. The peak mobility for layers on sapphire for comparable nominal barrier structures is only $1,300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature.

MOCVD-Grown Heterostructures

Nearly all electronic high-performance GaN FET and bipolar devices contain heterostructures of some kind. Thus, the specific growth of heterostructures and results are addressed in this section.

Heterostructure Transport in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$

Fig. 3.4 depicts the extracted heterostructure Hall mobility data taken from a more statistical point of view from various publications, e.g., [3.13, 3.39, 3.102, 3.139]. The data on the AlGaN/GaN heterostructures are given for various substrates, including the channel resistivity contours. The Hall mobility values in general range between 500 and $2,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ depending on the substrate and material quality and some specific growth measures. The transport situation in heterostructures differs from a bulk approach, so that additional mechanisms influence the mobility, as is already discussed in chapter 2 and also further described in [3.82]:

- Alloy scattering mechanisms, especially at high sheet carrier densities
- Interface roughness
- Scattering for remote surface donors
- Scattering due to threading dislocations

Typical sheet resistances of $130\text{--}500 \Omega \text{ sq}^{-1}$ can be found for various compositions, as shown in Fig. 3.4. Numerous publications are available for the

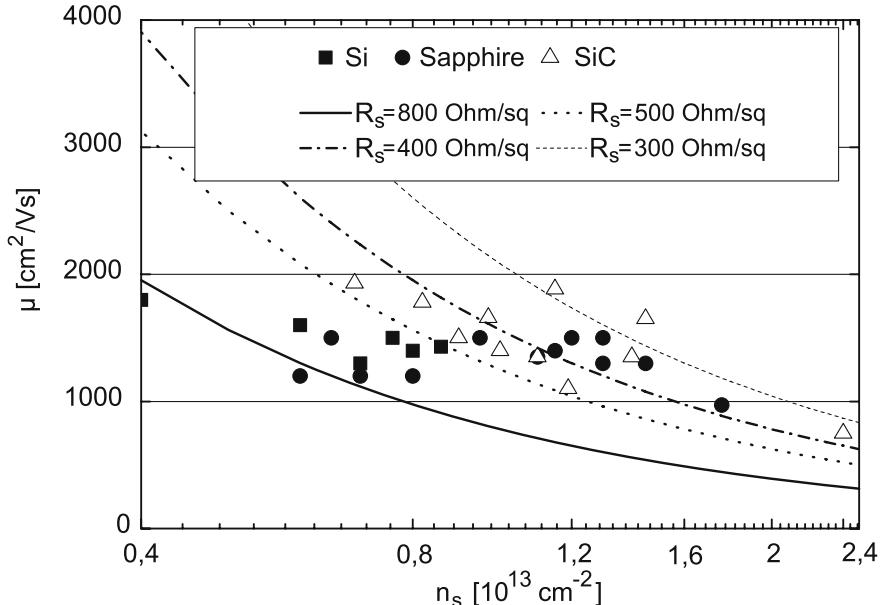


Fig. 3.4. Hall mobility as a function of sheet carrier concentration for AlGaN/GaN heterostructures grown on various substrates in MOCVD material

Al-content range between 10 and 35% [3.13, 3.39, 3.102, 3.139]. Even higher Al-contents ($x \geq 0.35$) in AlGaN/GaN MODFETs with Al-contents up to 52% are reported in [3.92, 3.136, 3.222]. The detailed influence of the MOCVD growth parameters will now be discussed.

Material Composition Dependence

The material dependence of the properties of the ternary materials is of great importance and determines several device parameters critically, as is already shown with the sheet resistance. Fig. 3.5 gives the Hall mobility data as a function of Al-content in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier in MOCVD-grown heterostructures for completely undoped structures with a constant barrier thickness. The mobility is only weak function of the sheet carrier concentration up to a concentration of approximately $1 \times 10^{13} \text{ cm}^{-2}$. Beyond that value, the Hall mobility decreases with increasing carrier concentration. Fig. 3.6 gives the Hall mobility as a function of carrier concentration in AlGaN/GaN heterostructures on sapphire for a given Al-mole fraction and barrier thickness with the Si δ -doping varied. The values for the sheet carrier concentration range from $4.5 \times 10^{12} \text{ cm}^{-2}$ to about $1.2 \times 10^{13} \text{ cm}^{-2}$. The impact of doping of the $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier can be observed in Fig. 3.6 for a given experiment at otherwise constant growth parameters. We see that the Si δ -doping in the barrier in the range 10^{17} cm^{-3} (nid) to $3 \times 10^{19} \text{ cm}^{-3}$ has a significant impact on the sheet carrier concentration, and that the doping has also a strong impact on

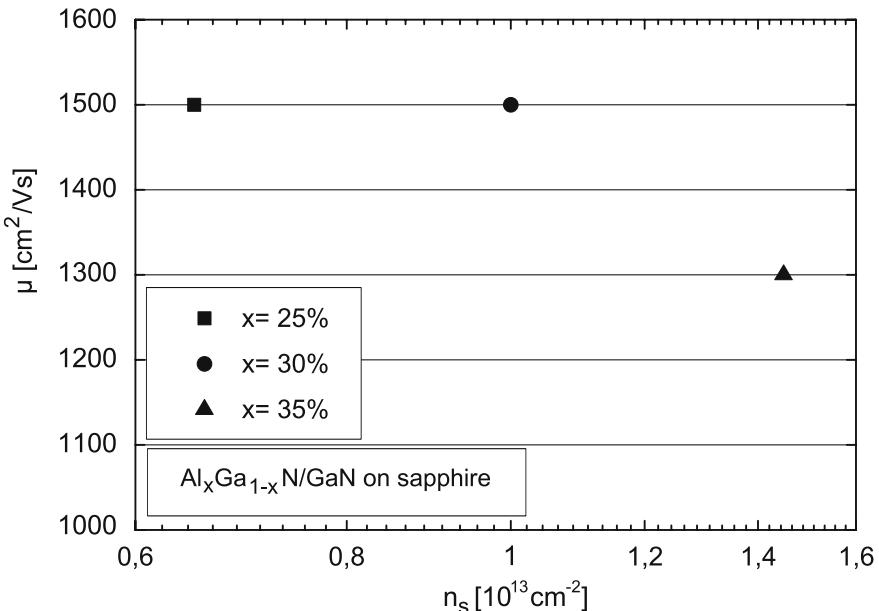


Fig. 3.5. Hall mobility as a function of sheet carrier concentration with the Al-content as a parameter in undoped MOCVD heterostructures on sapphire substrate

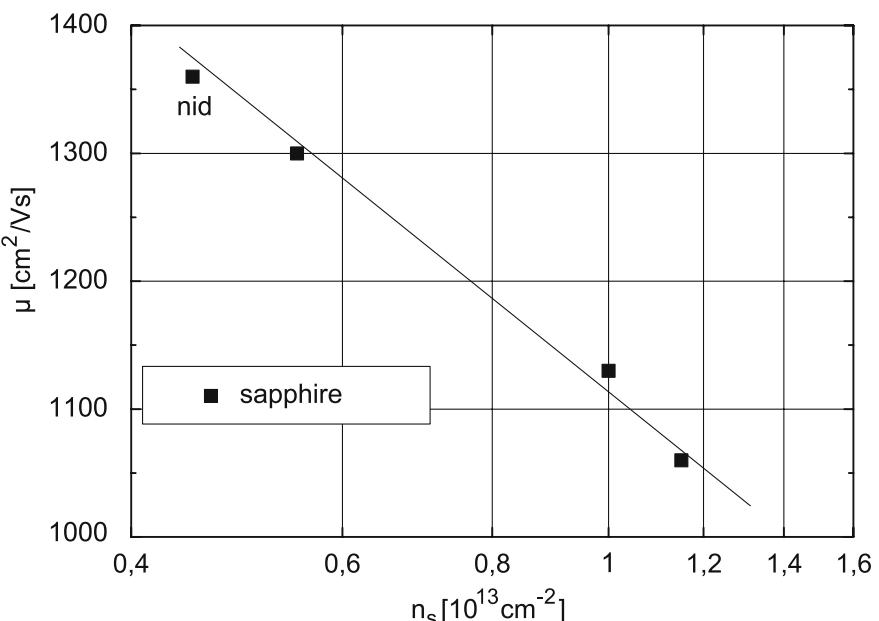


Fig. 3.6. Hall mobility as a function of sheet carrier concentration for different doping levels in the barrier for MOCVD material on sapphire and SiC substrates

the carrier mobility. Very similar data is found for growth on s.i. SiC in [3.48]. Additional effects arise from the introduction of AlN interlayers [3.139], as described further below. Depending on the growth parameters, sheet carrier densities of $2 \times 10^{13} \text{ cm}^{-2}$ can be reached [3.25, 3.92].

Uniformity

Epitaxial uniformity is a basic requirement for the reproducible device and MMIC production. The uniformity is currently given for 2-in. to 4-in. wafer sizes, e.g., [3.192]. For the average standard deviation of the sheet resistance, typically a value $\leq 1\%$ is specified for both 2-in. and 3-in. wafers on MOCVD material grown on sapphire and s.i. SiC substrates [3.192]. Fig. 3.7 shows the homogeneity of the sheet resistance within a multi-wafer growth reactor chamber for 2-in. s.i. SiC wafers, which achieves a standard deviation of 1%. The improvement in uniformity due to the transition from 2-in. to 3-in. s.i. SiC wafers is, e.g., investigated in [3.221]. The run-to-run reproducibility is significantly improved for the 3-in. growth, which is a prerequisite for reproducible device production. In a direct comparison, average standard deviations $\leq 3\%$ on 3-in. MBE-grown and MOCVD-grown material are reported in [3.221]. The substrate quality impact on the uniformity is strong, especially for SiC substrates with still evolving quality. Some general findings shall be listed here: With the increasing substrate diameter, improved substrate-related unifor-

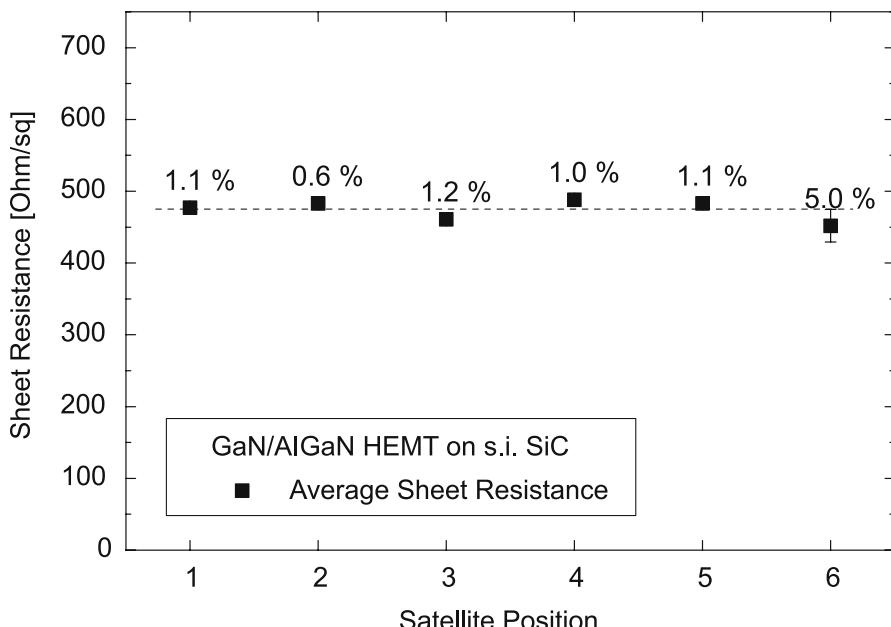


Fig. 3.7. Homogeneity of sheet resistance in MOCVD material within a $6 \times 2''$ reactor

mity and a wafer-to-wafer uniformity of AlGaN/GaN HEMT epitaxial wafers on sapphire and s.i. SiC substrates are reported [3.193]. The typical standard deviation of the sheet resistance is 2% on 4-in. sapphire substrates. Very reproducible AlGaN/GaN HEMTs are grown on n-type SiC with very low standard deviations of $\leq 1\%$ of the device parameters [3.96]. Typically, the substrate quality improves with the increase of the substrate diameter. This scaling benefit is similar to the findings of silicon technology and related substrate scaling. The contribution of the homogeneity of the material composition is investigated, e.g., in [3.161]. The material composition $x = 0.12$ of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ directly grown on s.i. SiC varied by $x \pm 0.005$ due to terrace steps on the growth surface.

Fig. 3.8 gives a topogram to demonstrate the on-wafer homogeneity of the sheet resistance on a 3-in. wafer. The homogeneity is very much influenced by the substrate quality, which is also visible in Fig. 3.8. The largest deviations of the sheet resistance can be correlated with substrate nonuniformities in the upper left edge shown in Fig. 3.8, resulting from substrate growth. Further particular growth issues to increase uniformity include the following:

- The uniform distribution of the defects such as micropipes and others in the substrates
- The uniformity of the temperature and of other growth parameters over the wafer
- The growth windows with respect to relative requirements and to relative deviations
- Such as the uniformity of the thermal contact of the substrate during growth

These issues are related to the particular reactor concepts, such as the wafer rotation during growth. These issues are now discussed in the following sections.

Material Analysis

Several state-of-the-art methods are used for the characterization of the III-N heterostructures. These advanced methods are necessary to optimize this complicated material system with regard to the great variety of effects. Atomic force microscopy (AFM) typically reveals surface roughness. The measurements are performed for areas with some $10\text{ }\mu\text{m}$ dimension, e.g., [3.204]. An example of an AFM image is given in Fig. 3.9 for the growth of GaN surface on sapphire substrate. A RMS roughness of 0.4 nm is observed. Structural topography by X-ray diffraction (XRD) and two-dimensional XRD maps reveal structural properties such as micropipes, dislocations, and grain boundaries of substrates and overgrown semiconductor layers [3.100]. The line widths in XRD measurements further allow the investigation of the lattice-mismatch and the Al-content in the barrier layer, as explained, e.g., in [3.204].

Photo-luminescence measurements at various temperatures reveal possible trap mechanisms, e.g., as stated in [3.219], between 2.25 and 3.0 eV . Fig. 3.10

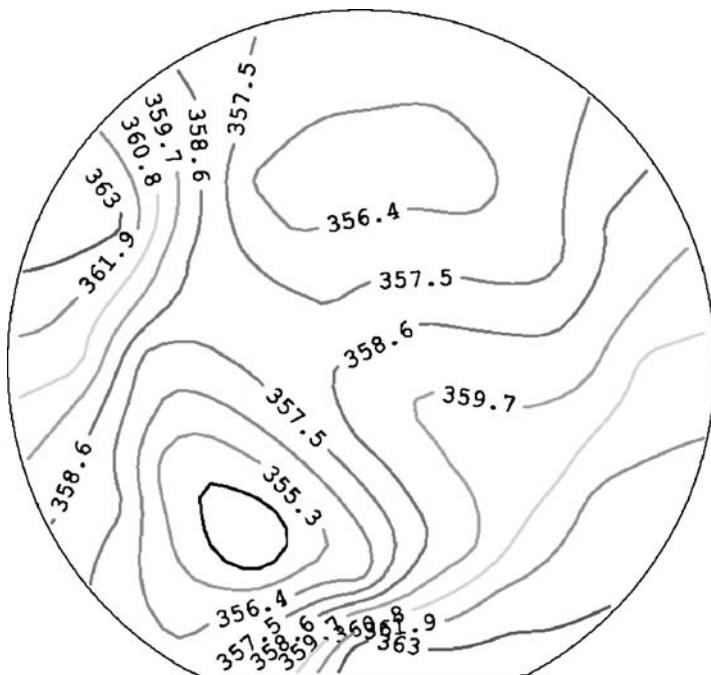


Fig. 3.8. On-wafer homogeneity of sheet-resistance of an AlGaN/GaN MOCVD-grown heterostructure on 3-in. s.i. SiC substrate, average $359 \Omega \text{ sq}^{-1} \pm 0.7\%$

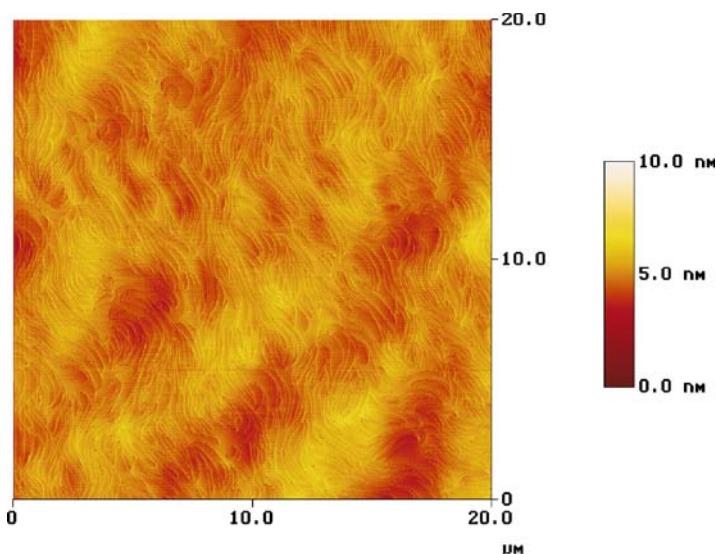


Fig. 3.9. Atomic force microscope image of a surface of a GaN layer MOCVD-grown on sapphire substrate

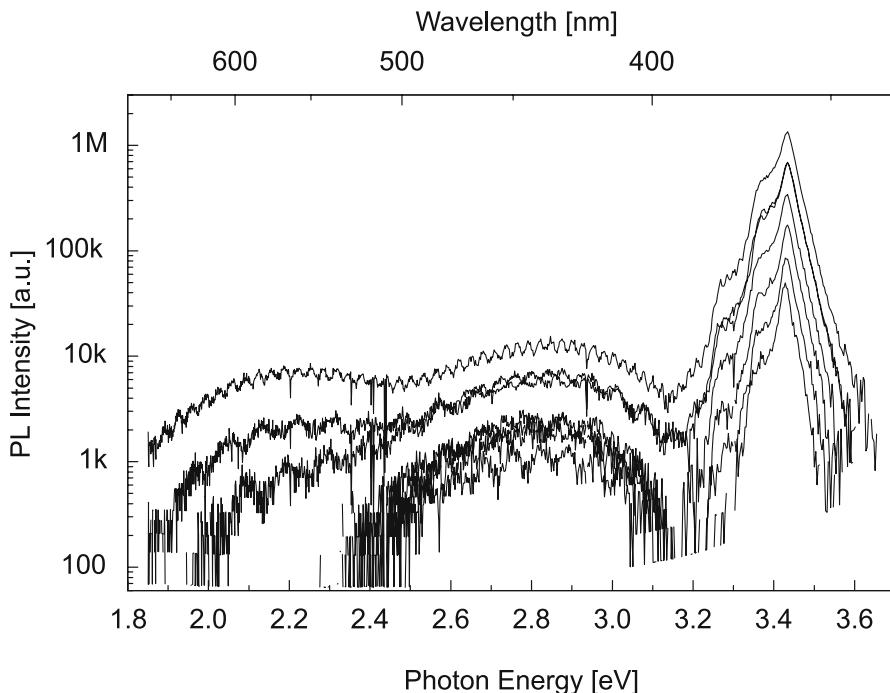


Fig. 3.10. Photoluminescence spectra of AlGaN/GaN heterostructures for different excitation energies

gives a spectrum of an AlGaN/GaN HEMT structure on s.i. SiC. There is yellow luminescence visible at a photon energy of $\approx 2.8\text{ eV}$. The significance of this data is based on the electron recombination in high-resistivity films, potentially with edge-type threading dislocations [3.219] leading to high resistivity. An alternative explanation is the removal of a particular trap with changes of growth parameters.

MOCVD Growth on s.i. SiC(0001) Substrate

SiC(0001) requires the matching of the GaN layers to the 4H- or 6H-s.i. substrate. Direct growth of GaN on (0001) 6H-SiC leads to columnar grain with rough, faceted surfaces and high non-intentional net carrier concentrations [3.59]. Typical nucleation layers for growth on SiC are high-temperature AlN layers [3.215,3.222]. Further details are given below. An example of multi-wafer epitaxy of AlGaN/GaN heterostructures on s.i. silicon carbide for power applications is given in [3.102]. Fig. 3.11 shows the sheet carrier concentration in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures as a function of Al-content on s.i. substrate for a mole fraction between 0 and 40%. A very linear dependence is visible for these samples from $x = 0.13$ to 0.35. As the Al-content defines the sheet carrier concentration at the interface, Fig. 3.12 gives the homogeneity of

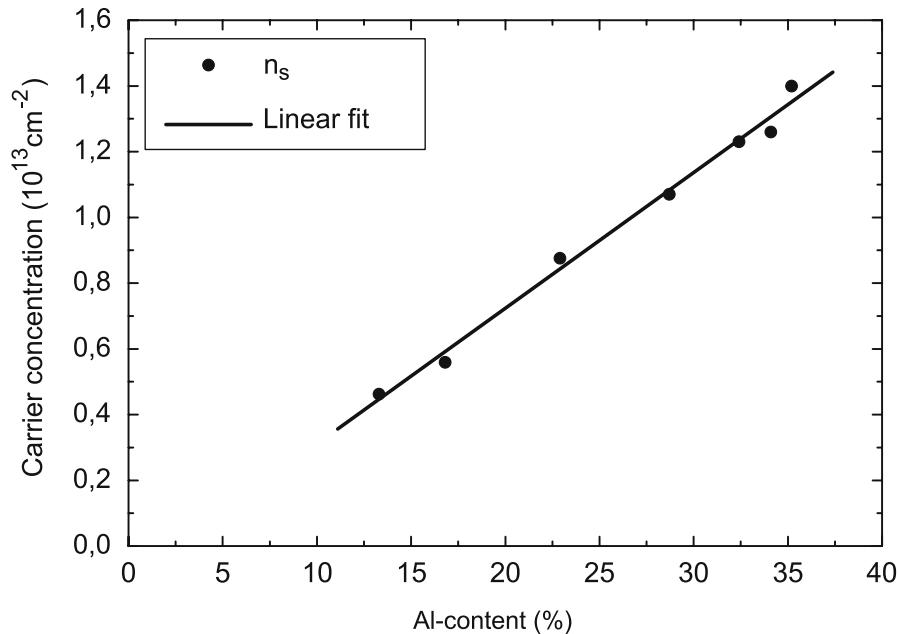


Fig. 3.11. Sheet carrier concentration as a function of Al-content for MOCVD-grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on s.i. SiC substrate

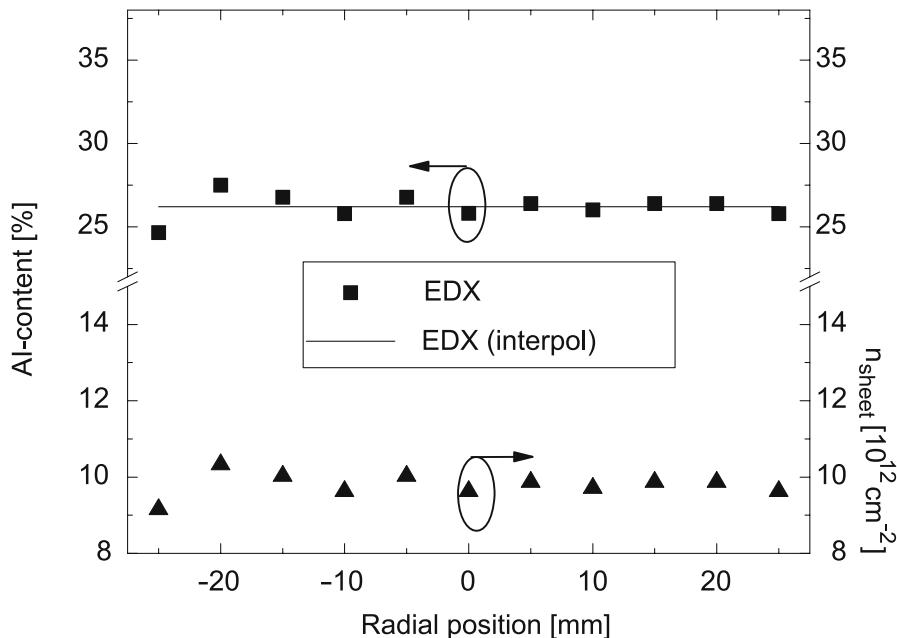


Fig. 3.12. Al-content and corresponding variation of the sheet carrier concentration as a function of radial position for a 2-in. s.i. SiC wafer

the Al-content determined by electron diffraction (EDX) and at the same time provides the calculated difference of the carrier concentration. Even a very small variation of $x \leq 0.2\%$ provides a significant variation in the sheet carrier concentration of $\approx 1 \times 10^{12} \text{ cm}^{-2}$ over the 2-in. diameter. The n_{sheet} is calculated from the $n_{\text{sheet}}(x)$ extrapolated relation in Fig. 3.11.

MOCVD Growth on Sapphire(0001) Substrate

One of the crucial advantages of sapphire relative to SiC is the lack of micropipes and the commercial availability of larger substrate formats up to at least 6 in., as used for CMOS on sapphire with a different crystal orientation [3.95]. MOCVD growth on 4-in. sapphire substrates is reported in [3.7, 3.96]. MOCVD growth issues on sapphire substrates are the increased lattice-mismatch and the difference in thermal expansion between sapphire and GaN. The latter results in increased wafer bow [3.96] when the wafer is cooled to room temperature after growth. As an example, the wafer bowing can be reduced to $22 \mu\text{m}$ on top of $630 \mu\text{m}$ thick GaN buffer, as reported in [3.193]. Epiready 2–4 in. sapphire substrates have been used in [3.192]. The standard deviation of the sheet resistance is $\leq 1\%$ for all diameters. The Al-composition varies by 0.2% over the 3 in. wafer. The AlGaN thickness varies by $29.25 \pm 0.75 \text{ nm}$. Fig. 3.9 depicts the AFM image of a GaN surface on sapphire substrate. The surface root mean square (RMS) roughness on sapphire amounts to only 0.4 nm for an area of $20 \times 20 \mu\text{m}^2$. The peak-to-peak roughness can be as high as 15 nm , which has several implications for the scaling of the devices to small gate lengths.

MOCVD Growth on Silicon(111) Substrate

Growth on silicon substrates is very attractive as a cost effective method and also relates the III-N material system to the most successful semiconductor system. First demonstrations of MOCVD-grown AlGaN/GaN HEMTs on silicon substrate have been claimed, e.g., in [3.29]. The results are obtained on p-type Si(111) substrates with a buffer layer of 500 nm thickness on top of a 30 nm AlN nucleation layer. An overview of the MOCVD growth on silicon substrate is given in [3.34]. The silicon material can either be conductive or highly resistive ($30 \text{ k}\Omega \text{ cm}$). Highly resistive silicon is more expensive than conductive substrates and available only in smaller diameters. However, highly resistive silicon is advantageous to reduce the substrate RF-losses, especially at frequencies higher than 2 GHz [3.42]. Buffer growth is of great importance due to the increased lattice-mismatch between silicon and the III-N material system. A critical thickness of the buffer growth of $1 \mu\text{m}$ is mentioned in [3.34]. Furthermore, the difference in thermal expansion is pronounced, as explained in Table 2.5. Mismatch engineering is thus of critical importance. Patterned substrate techniques are described, e.g., in [3.85]. AlGaN/GaN HEMTs are fabricated on top of rectangular silicon ridges. The rectangular stripes have

a maximum size of $168 \times 52 \mu\text{m}^2$, which limits the application of this techniques to small devices. The stress distribution in patterned GaN films grown by MOCVD on (111) silicon is investigated in [3.208]. The intentional cracking of the layers grown reduces the tensile strain in small area stripes. Low-temperature (LT) AlN-interlayers are used for strain engineering [3.34]. The LT-AlN layers are combined with high-temperature layer stacks. These methods can be used to reduce the threading dislocation density in the heterostructure layers [3.37]. Crack-free GaN material is reported in [3.79] on 2-in. p-type silicon grown by MOCVD. The buffer thickness is $2.5 \mu\text{m}$, which further reduces the dislocation density on top of specially designed layer sequences used for nucleation. The RMS surface roughness reported amounts to 0.64 nm determined by AFM. A commercial GaN HFET process on 100 mm diameter silicon substrates is given in [3.204], using GaN epitaxial layers up to $2 \mu\text{m}$ thickness in the SiGaNticTM process. The standard deviation of the $\text{Al}_{0.21}\text{Ga}_{0.79}\text{N}$ spectral-peak wavelength at 324 nm across a 100 mm wafer is as low as 0.6%. The Hall mobilities reach $1,430\text{--}1,500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a sheet charge carrier concentration of $\approx 8 \times 10^{12} \text{ cm}^{-2}$. The difference in thermal expansion and lattice-mismatch have particular impact on the device reliability, which is further discussed in Chapter 7.

3.1.2 Molecular Beam Epitaxy (MBE)

MBE is the second attractive growth method for III-N semiconductors. The growth of semiconductors by MBE occurs via reactions between thermal-energy molecular, atomic, or ionized beams of the constituent elements on a heated substrate in an ultrahigh vacuum; see, e.g., in [3.36]. The advantage of MBE is a very precise definition of the interfaces and the increased flexibility of the polarity of the interfaces [3.87, 3.196]. These advantages are available at the expense of reduced growth rates relative to MOCVD growth. The growth rates of III-N MBE typically amount to $0.5\text{--}1 \mu\text{m h}^{-1}$ [3.132]. Fig. 3.13 gives the schematic of a MBE growth chamber. The molecular beam of Ga and Al originate from effusion cell sources. An elemental group-V N-source is impossible due to the very high binding energy of the N_2 . N radicals are thus generated either by a RF-plasma source [3.17, 3.132, 3.166] or by an ammonia source, as reported, e.g., in [3.194, 3.213]. The background pressure amounts to $\leq 10^{-11} \text{ mbar}$ during MBE growth, as given, e.g., in [3.89]. The substrates are typically rotated during growth. Growth temperatures amount to 800°C for GaN growth. Growth conditions of MBE can be characterized by growth diagrams, given for III-V semiconductors, e.g., in [3.36, 3.88, 3.149].

State-of-the-Art of MBE Growth

Overviews on molecular beam epitaxial growth of III-N materials are given, e.g., in [3.50, 3.87, 3.172]. More general overviews of growth and doping of III-V nitrides including MBE growth are given in [3.39, 3.150]. AlN is typically used

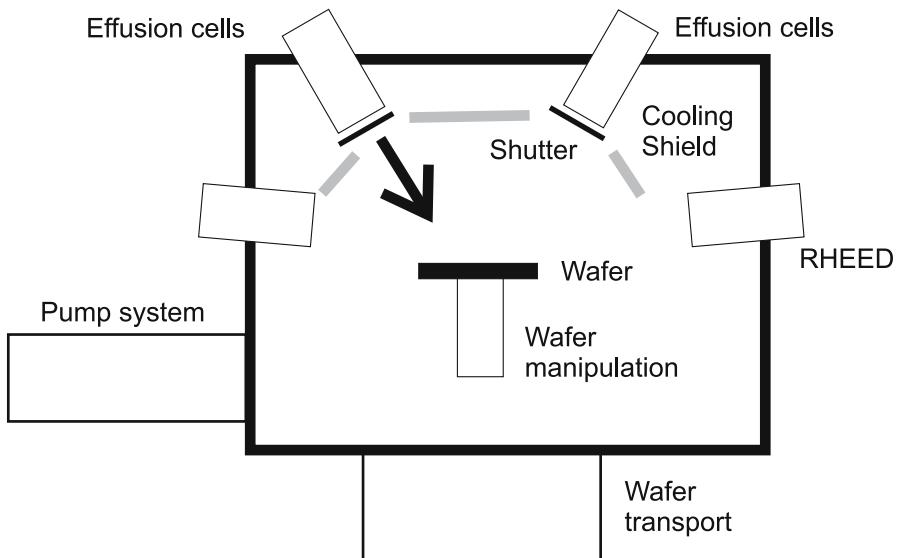


Fig. 3.13. Scheme of molecular beam epitaxial (MBE) growth

as a nucleation layer for MBE [3.90,3.132,3.216]. Issues in scaling nitride MBE systems to 4-in. single-wafer production are discussed in [3.188]. The scaling of the RF-plasma system is investigated, especially with respect to the small growth window in the Ga/N flux ratio. The second issue in wafer-size scaling is the growth temperature uniformity for increased wafer size. Compared to other III/V-MBE systems, the temperature control is more complicated due to the high growth temperatures of III-N materials, leading to high radiative losses. Further, the optical transparency of the substrates, such as SiC and sapphire, in the infrared complicates heat absorption. MBE-growth conditions are investigated in a number of publications, e.g., in [3.17, 3.41, 3.66, 3.67, 3.113, 3.165, 3.205, 3.213], and are detailed below. On the device level, high-power GaN/AlGaN HEMTs grown by plasma-assisted MBE operating up to 25 GHz are described in [3.124, 3.125, 3.132, 3.216]. An X-band power amplifier is given featuring a cw-output power of 22.9 W using four hybrid 1 mm cells. The amplifier yields a PAE of 37%. Further impressive device examples and a comparison of HEMTs grown either by plasma-assisted MBE or MOCVD are given in [3.39, 3.166]. Device examples of ammonia-based GaN MBE are given in [3.10]. AlGaN/GaN HEMTs with gate lengths of 130 nm feature very high drain current densities $\geq 1.3 \text{ A mm}^{-1}$ and a cut-off frequency $f_T = 103 \text{ GHz}$.

Optimized Growth Conditions for MBE Growth

Similarly, as in MOCVD growth, optimized growth conditions for MBE are very system- or machine-specific. However, general trends will be outlined here.

Growth Temperatures for III-N MBE Growth

Before the actual growth procedure, the substrates are typically inserted into the growth chamber via a preparation chamber. The substrates are outgased in the preparation chamber. A typical substrate outgas temperature in the preparation chamber is reported to be 700°C in [3.90]. Further temperature steps for oxide removal reach 1,000°C. The reported nucleation temperature using AlN nucleation on sapphire substrate is 800°C, as reported in [3.150]. A nucleation temperature of 835°C on s.i. 6H-SiC substrates is used in [3.90]. The growth of the insulating GaN buffer layer on top of a nucleation layer is reported to be performed at 745°C in [3.90, 3.125] for Ga-rich conditions. The GaN channel layers are typically grown at 800°C using atomic nitrogen, as reported in [3.40]. The backside of the substrate is metalized by tungsten in this case. Thick bulk GaN layers are grown by plasma-assisted MBE between 600 and 800°C for different Ga/N flux ratios on SiC(0001), as reported in [3.205]. The threading dislocation density can be reduced from 10^{11} cm^{-2} for a growth temperature of 600°C and Ga-lean growth to 10^{10} cm^{-2} for a growth temperature of 800°C and Ga-rich growth. The nominal growth temperatures for GaN using ammonia-based MBE growth is 910–920°C and 880°C for AlN [3.10, 3.212]. A growth temperature for a bulk GaN layer of 860°C is reported in [3.194] for ammonia-based MBE on sapphire(0001). Magnetron sputter epitaxy is used in this case for the initial deposition of a AlN nucleation layer. The growth of quaternary $\text{Al}_x\text{Ga}_{1-x-y}\text{In}_y\text{N}$ materials by plasma-assisted MBE on GaN templates is described in [3.137]. Substrate growth temperatures range from 590 to 650°C. The use of the MBE technique increases the material composition range, which is ($0 \leq x \leq 0.5$, $0 \leq y \leq 0.2$) in this case.

N-Group-III Ratio for MBE Growth

Similar to MOCVD growth, the V/III ratio is a critical parameter for the MBE growth, however, for a very different material transport. A distinction is made for RF-plasma-assisted MBE (PAMBE) and ammonia-based MBE. The V/III-ratio determines the quality of the epitaxial layers. The impact of the Ga/N flux ratio on trap concentrations and morphology in GaN grown by plasma-assisted MBE is discussed in [3.67, 3.68]. The distinction of the Ga-rich, intermediate, and N-stable regime is made. N-stable-grown GaN films are semi-insulating. GaN layers grown with ratios in the intermediate regime yield fewer pits with an atomically flat surfaces. At high Ga/N-ratio Ga droplet formation occurs. However, the mobility decreases significantly. The best material is thus grown within the intermediate regime. The best combination of

surface morphology and material quality is achieved by a modulated technique varying alternately Ga-rich and Ga-lean growth, see, e.g., [3.33, 3.117]. The growth diagram for GaN, grown homoepitaxially by plasma-assisted MBE, is given in [3.67] for a growth temperature of 720°C. The surface morphology and GaN mobility are optimized for the various Ga-flux conditions. Similar surface structure diagrams between 550 and 700 K are given in [3.66].

The growth conditions such as V/III ratio and temperature for AlGaN are investigated for plasma-assisted MBE in [3.41]. The $\text{Al}_{0.45}\text{Ga}_{0.55}\text{N}$ layers are grown at temperatures between 650 and 750°C. Particularly, the O_2 incorporation is investigated. It is found that the incorporation is minimized for the higher growth temperatures.

For ammonia-MBE, carbon-doped insulating GaN MBE layers are grown on s.i. SiC substrates at a temperature of 910°C [3.211, 3.212, 3.214]. For the AlN nucleation in [3.194], argon and ammonia fluxes are adjusted leading to growth rates of $3.4 \text{ nm min}^{-1} \equiv 204 \text{ nm/h}$ at a very high deposition pressure of 1.4 mTorr. GaN-layer deposition pressures of 3×10^{-6} Torr are reached during the growth. The growth rates reach $1\text{--}2 \mu\text{m h}^{-1}$ by the adjustment of the ammonia flow to 50 sccm.

Nucleation Layer Growth by MBE

The nucleation layer is of very high importance on various substrates, as this region with its polycrystalline inclusions contributes significantly to the quality of the MBE-grown active semiconductor layers and thus to device performance. The growth of an AlN nucleation layer by plasma-assisted MBE on s.i. 4H–SiC substrate is reported in [3.89]. The layer thickness is 100 nm, grown at a temperature of 835°C. The N_2 pressure is 2×10^{-5} Torr for the nucleation layer. A 60 nm thick AlN nucleation layer is used in [3.124] grown by PAMBE on s.i. SiC substrate under Al-rich growth conditions at 745°C. Similar thicknesses and conditions are reported in [3.125]. Hundred nanometer thick AlN nucleation layers are grown by RF-PAMBE at 835°C [3.90]. An AlN nucleation layer on sapphire with a thickness of 70 Å is used in [3.39] for RF-plasma-assisted MBE on sapphire substrate. Al-rich surfaces to obtain Ga-polarity are used. The GaN growth rate is $0.5 \mu\text{m h}^{-1}$ at a growth temperature of 800°C. On silicon substrate, a 50–60 nm thick AlN nucleation layer is used, grown by reactive MBE in combination with a 500 nm special layer sequence and a $1.5 \mu\text{m}$ thick GaN buffer [3.135]. The TDD amounts to $7\text{--}9 \times 10^9 \text{ cm}^{-2}$.

Growth and Isolation of the Buffer Grown by MBE

A large variety of buffer layers grown by MBE are reported for heteroepitaxy. The growth rate of GaN achieved by MBE in general is smaller than in MOCVD growth, e.g. $0.5 \mu\text{m}$ in [3.132]. This lower growth rate favors reduced layer thicknesses for MBE growth, especially for the buffer layer.

As an example for a optimized buffer sequence, after the growth of a 45 nm thick AlN nucleation layer on 4H-s.i. SiC, a 400 nm thick GaN two-layer sequence is used in [3.162, 3.166, 3.206] to improve the isolation, grown

with a flux variation stepping from a low Ga-flux regime to a high Ga-flux regime. Further, the AlN and the first 100 nm are C-doped with CBr_4 . This sequence is followed by a 1 μm thick undoped GaN buffer/channel-layer. Two micrometer GaN thick buffer layers grown by PAMBE on s.i. 4H–SiC substrate are reported in [3.132]. The growth rate is 0.5 $\mu\text{m h}^{-1}$.

Grown by ammonia-MBE on s.i. 4H–SiC substrate, a 2 μm thick highly insulating C-doped GaN buffer layer is reported in [3.213]. The layer is followed by a 200 nm undoped GaN channel layer grown at a nominal temperature of 920°C. Beryllium-doped GaN buffer layers grown by RF-plasma-assisted MBE on n-type 6H–SiC are reported in [3.90]. The leakage through a 1 μm thick buffer is reduced by the Be-doping at concentrations between 10^{18} and 10^{19} cm^{-3} . Even the lowest doping concentration leads to significant reduction of the leakage by three orders of magnitude.

On high-resistivity silicon substrate, a 1.5 μm -thick GaN buffer is reported in [3.135], grown by MBE on a 50 nm-thick AlN nucleation layer. Crack-free GaN bulk buffer layers with thicknesses up to 3 μm grown on silicon substrate are reported in [3.180]. Ammonia is used as a nitrogen source for the MBE. Buffer layers with thicknesses between 1 and 2.5 μm are investigated for AlGaN/GaN heterostructures. Hall mobility values up to $1,600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are achieved at room temperatures. The TDD range between 5×10^9 and 10^{10} cm^{-2} .

The interface the substrate is especially susceptible to isolation issues due to the high concentration of defects. Indications for conduction parallel to the GaN/sapphire interface in PAMBE-grown material are investigated in [3.3]. The buffer material is etched to different thicknesses. The results show that the apparent carrier concentration increases near the interface, while the mobility decreases. Both interface conduction and impurity band conduction near the interface are considered to explain this behavior.

Codoping in MBE Material

Similar to MOCVD-grown material, intentional codoping is of great importance for the isolation of the nucleation and buffer layers. During MBE growth, this codoping is achieved mostly by carbon and (non-intentional) oxygen, as Fe sources are not available. Carbon introduces a midgap state which helps to increase the isolation in buffer layers. Codoping by carbon for MBE-grown GaN buffer material in the buffer is reported, e.g., in [3.162, 3.163, 3.166]. A 45 nm-thick C-doped nucleation layer is grown by PAMBE on s.i. SiC. This layer is followed by a sequence of GaN buffer layers. By adjustments of the CBr_4 pressure linearly from 15 and 5 mTorr, the background C-doping concentration is varied linearly from 1.2×10^{18} , 8×10^{17} , and $4 \times 10^{17} \text{ cm}^{-3}$. A systematic investigation of carbon codoping via CBr_4 in PAMBE-grown material is reported in [3.162]. Doping levels of $2\text{--}6 \times 10^{17} \text{ cm}^{-3}$ significantly reduce the buffer leakage in AlGaN/GaN single heterostructures on s.i. SiC substrate. Unintentional oxygen incorporation into GaN layers is a major problem in

MBE growth. Several sources such as the background vacuum pressure, the nitrogen source, and the metal source are potential candidates. A systematic investigation is given in [3.41] for AlGaN layers grown by PAMBE on sapphire substrates. Ga-rich growth of AlGaN reduces the oxygen incorporation by a factor of three. Temperature reduction from 750 to 650°C significantly increases the oxygen incorporation. The nitrogen source is considered as a main source of oxygen in the MBE growth system, which is operated at a background pressure of 10^{-11} Torr. Intentional oxygen incorporation into GaN grown by PAMBE has been investigated in [3.165]. The doping is found to be controllable and reproducible up to doping level of 10^{18} cm^{-3} . Oxygen is an effective donor with low compensation and the incorporation is found to be strongly dependent on the growth polarity. PAMBE-grown GaN layers with N-polarity incorporate about 50 times as much oxygen than Ga-face material. Oxygen doping levels of 10^{22} cm^{-3} can be achieved.

Channel and Barrier Layers Grown by MBE

The growth conditions for the GaN channel layers is of primary importance for the material quality. Several detailed suggestions are available. GaN channel layers are grown by PAMBE at 735°C at a growth rate of $0.37 \mu\text{m h}^{-1}$ in Ga-rich conditions [3.89]. The $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ heterobarrier layers are grown at the same temperature and the same nitrogen flow as GaN in this case. The GaN channel layers in [3.124] are grown by PAMBE on s.i. 6H-SiC under Ga-rich conditions at 745°C near the border of Ga-droplet formation. The upper half of $\text{Al}_{0.34}\text{Ga}_{0.66}\text{N}$ layers are doped by Si to $1 \times 10^{18} \text{ cm}^{-3}$. Similar growth temperatures for PAMBE on sapphire are used in [3.75, 3.77] with a growth temperature of 730°C for GaN, and 760°C for the subsequent $\text{AlN}/\text{Al}_{0.4}\text{Ga}_{0.6}\text{N}$ growth. This temperature is significantly lower than the growth temperature for similar AlGaN layers grown by MOCVD. For ammonia(NH_3)-based MBE growth on s.i. SiC, the GaN channel layers are typically grown at higher temperatures, i.e., 920°C, as reported in [3.213]. A similar temperature of 910°C for GaN is reported in [3.10, 3.214] on 4H-SiC(0001). A growth temperature of 790°C is mentioned in [3.180] for growth on conducting p-type silicon(111) substrates. The resulting mobility data and sheet carrier densities are detailed below.

Dislocations in MBE Material

The TDD in the MBE-grown layers can be reduced to densities similar to those achieved for MOCVD-grown material. On s.i. SiC substrate, the dislocation density can be reduced to $\leq 10^9 \text{ cm}^{-2}$, as observed by plan-view TEM in [3.17]. Plasma-assisted MBE (PAMBE) is used in this case.

Leakage current mechanisms in Schottky diodes are investigated in [3.133, 3.134] in plasma-assisted MBE material grown on GaN templates, which again are grown by MOCVD on sapphire substrates. A leakage mechanism is isolated during the investigation based on threading dislocations. The mechanism has

an exponential temperature dependence, and so either a trap-assisted tunneling or a one-dimensional hopping mechanism is considered for the physical origin. A similar investigation of the impact of different dislocation types such as edge-, screw-, and mixed -type in GaN grown by PAMBE on MOCVD templates on sapphire substrates is given in [3.184]. A combination of scanning Kelvin probe microscopy (SKPM) and conductive atomic force microscopy (C-AFM) is used. Edge- and mixed-type dislocation are found to be negatively charged with limited contribution to the leakage, while pure screw dislocations, on the contrary, provide a conductive leakage path. The TDD obtained for the GaN templates on sapphire is found to be maintained through the subsequent MBE growth and is determined by electron-beam current microscopy (EBIC) to be $8 \times 10^8 \text{ cm}^{-2}$.

On resistive silicon substrate, the threading dislocation density amounts to $5\text{--}7 \times 10^9 \text{ cm}^{-2}$ reported in [3.32, 3.135] for MBE-grown material and observed by TEM. The overall layer thickness is $2.6 \mu\text{m}$. Further investigations of p-type silicon(111) substrate in [3.180] demonstrate an increase of the threading dislocation density of GaN on silicon substrate relative to s.i. SiC or sapphire substrates by a factor of two in the same investigation.

MBE-Grown Heterostructures

The basic properties such as mobility and sheet carrier densities grown by MBE are very similar to those obtained by MOCVD growth. Fig. 3.14 gives the mobility as a function of Al-content in MBE-grown material. Similarly, Fig. 3.15 gives the sheet carrier concentration. The maximum sheet carrier concentrations reach $2 \times 10^{13} \text{ cm}^{-2}$. Similar tendencies for the MBE-grown material are observed as for MOCVD, compare Fig. 3.6.

Fig. 3.16 depicts the mobility as function of sheet carrier concentration for various substrates in MBE-grown material at 300 K. Again, very strong variations are observed for a given Al-content depending on the substrate type and the growth conditions, compare Fig. 3.7. The maximum Hall mobility is close to $2000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at RT. The results presented in Fig. 3.16 are now analyzed in detail for the different substrate types.

MBE Growth on s.i. SiC

High-performance heterostructures are achieved using both RF-plasma-source MBE and ammonia MBE [3.132, 3.214, 3.217]. Low-field mobility values of GaN/AlGaN heterostructures on 6H-SiC as high as $75,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ measured at 4.2 K grown by PAMBE have been reported, while the RT mobility values amount to $1,400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.216]. An additional ECMP surface polish is reported to be crucial to the reproducibility of the heterostructure device results on the SiC substrate.

Sheet carrier densities of up to $2.1 \times 10^{13} \text{ cm}^{-2}$ have been obtained on s.i. SiC substrates using RF-PAMBE. The associated room temperature mobility is $1,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.16]. Very thin barrier AlGaN layers

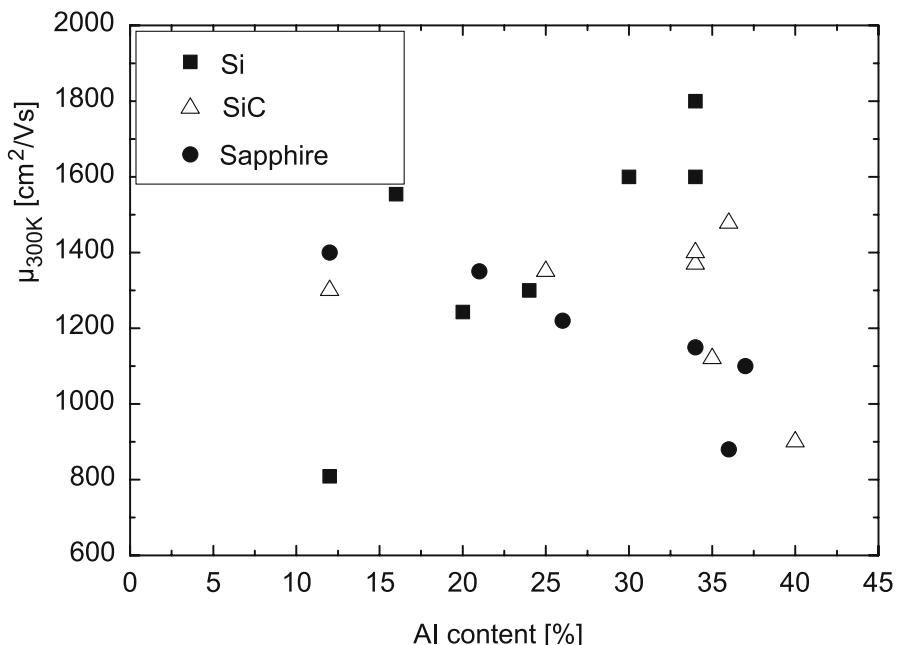


Fig. 3.14. Hall mobility as a function of Al-content in MBE-grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on various substrates

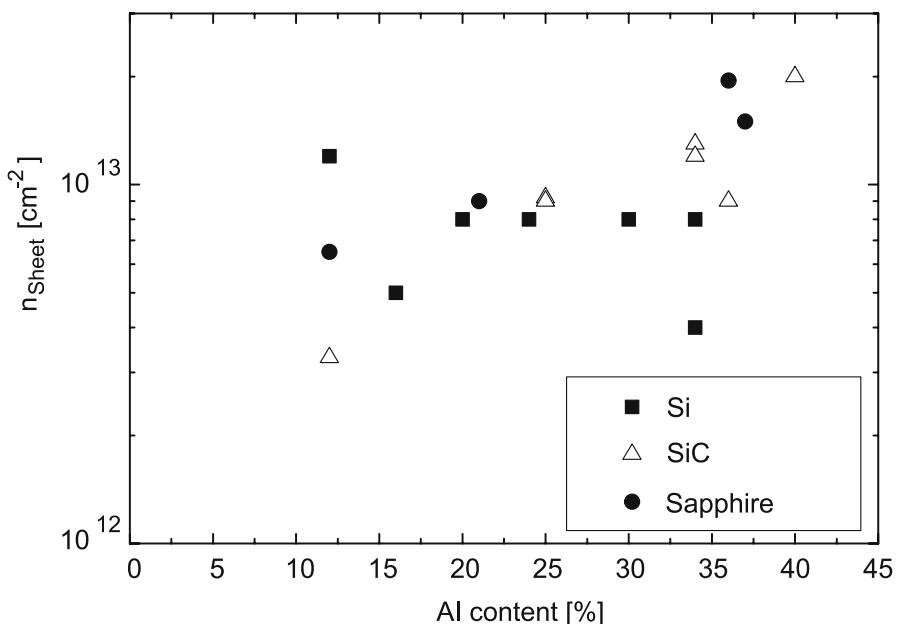


Fig. 3.15. Sheet carrier concentration as a function of Al-content in MBE-grown $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on various substrates

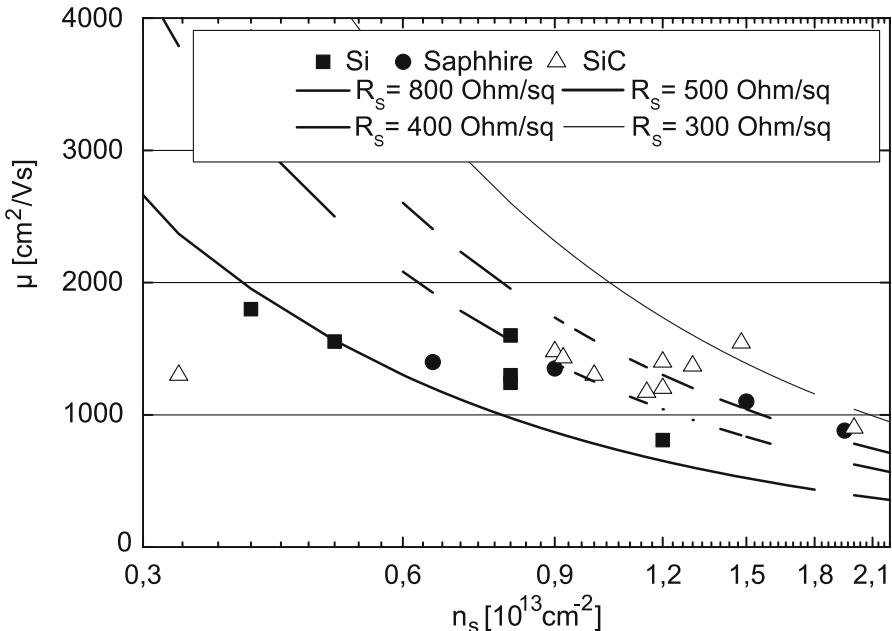


Fig. 3.16. Mobility in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures on various substrates as a function of sheet carrier concentration

of 8 nm thickness lead to reduced sheet carrier densities of $8 \times 10^{12} \text{ cm}^{-2}$ due to the reduced polarization effect [3.75]. Very high cut-off frequencies $\geq 100 \text{ GHz}$ of AlGaN/GaN HFETs on s.i. SiC substrates grown by ammonia MBE are reported in [3.10]. The AlGaN/GaN heterostructure mobility is $993 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, while a high sheet carrier density of $1.6 \times 10^{13} \text{ cm}^{-2}$ is measured. Inverted n-face AlGaN/GaN/AlGaN HFETs on s.i. SiC substrates show a room-temperature mobility of $860 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. The sheet carrier density amounts to $7.8 \times 10^{12} \text{ cm}^{-2}$ [3.26]. The latter result demonstrates the increased flexibility by MBE growth, as inverted polarization with N-face growth can be obtained.

MBE Growth on Sapphire

Most of the initial bulk material investigations and heterostructure results by MBE have been performed on sapphire substrates [3.39] or on GaN-templates grown on c-sapphire by MOCVD, e.g., [3.66–3.68, 3.133, 3.134, 3.137]. RT mobility values of $1,211 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ are reported in [3.212] for $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructures grown by ammonia-based MBE. The mobility is only a weak function of the Al-mole fraction at RT. The mobility at 77 K amounts to $5,660 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 10\%$, while it is $3,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 20\%$, and $2,600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for $x = 30\%$. Further room temperature results for growth on sapphire are compiled in [3.214]. Using metal organic

sources, III-N MBE can be performed leading to metal organic molecular beam epitaxy (MOMBE) [3.113]. Metal organic species are used for the group-III elements, while the group-N elements are generated by plasma or ammonia.

MBE Growth on Silicon(111)

Several reports exist for the MBE growth on silicon(111) substrate. MBE growth of AlGaN/GaN HEMTs on resistive Si(111) substrates using ammonia MBE are reported in [3.32,3.179,3.180]. The range for the resistivity in the substrate amounts to $4\text{--}20\text{ k}\Omega\text{ cm}$ for high resistivity [3.135] and $0.002\text{ }\Omega\text{ cm}$ [3.180] for p-doped substrates. The carrier densities reach $8\times10^{12}\text{ cm}^{-2}$ with room-temperature mobilities of $1,600\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, respectively [3.135]. The TDD is $5\text{--}7\times10^9\text{ cm}^{-3}$. Mobilities of up to $2,100\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ on Si(111) have been reported in [3.16] with Al-contents up to 50%. The report further claims no change in the surface morphology for such high Al-contents. The use of silicon substrates with substrate resistivities of $20\text{ k}\Omega\text{ cm}$ leads to very good noise performance using an AlGaN/GaN HEMT structure on silicon with $\geq2\text{ }\mu\text{m}$ thickness. Good mobility values of $1,300\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ are reported in [3.213] with an associated sheet carrier density of $3.3\times10^{12}\text{ cm}^{-2}$ grown by ammonia-based MBE. The mobility at 77K amounts to $11,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. Picogiga reports MBE growth with an ammonia source on high resistivity silicon substrates with up to 4-in. diameter in [3.16]. The typical RMS roughness is $3\text{--}5\text{ nm}$ and the TDD is in the range of 10^9 cm^{-2} . The typical isolation of the buffer amounts to $10^6\text{ }\Omega\text{ cm}$. Further, pseudomorphic growth of a AlGaN/GaN/AlGaN double heterostructure is reported to improve the buffer leakage.

3.1.3 MOCVD and MBE Growth on Alternative Substrates

Apart from the direct homo- and heteroepitaxial growth on a crystalline substrate, advanced alternative substrate methodologies have also been developed, e.g., [3.129]. A hybrid technique is used to fabricate AlGaN/GaN HEMTs on diamond substrate [3.84,3.229]. $\text{Al}_{0.27}\text{Ga}_{0.73}\text{N}/\text{GaN}$ heterostructures are conventionally grown on 2-in. silicon(111) substrates. The wafers are then mechanically frontside-mounted on a mechanical substrate. The silicon substrate is then removed. A $25\text{ }\mu\text{m}$ thick CVD grown polycrystalline diamond substrate is then atomically bonded to the GaN buffer. The procedure potentially combines the very good thermal conductivity of diamond with III-N semiconductor devices, as detailed in [3.229]. Remaining issues include the additional need of another mechanical substrate to enable the processing of the wafers. SiC on insulator (SiC on SOI or SiCOI) composite substrates are another substrate alternative, combining the advantages of crystalline and poly-SiC substrates and facilitating the substrate thinning possibilities [3.46]. With the application of the Smart Cut[©] and cleaving technology, a 270 nm SiC layer is bonded onto the oxide of a silicon(100) handle substrate [3.16].

The MOCVD growth of GaN on SiC is facilitated, as the lattice-constant of the SiC material is decisive for the HEMT layers, as reported in [3.217]. A growth recipe for GaN HEMT on SiC can be used. AlGaN/GaN HEMTs fabricated based on this procedure yield similar DC-characteristics and breakdown voltages as devices fabricated on silicon(111) substrates. The devices grown on the hybrid substrates show stronger thermal compression of the output characteristics. This is attributed to the increased thermal resistance R_{th} of the SiO_2 layer. The advantage of silicon and SiC are combined in the silicon on polycrystalline SiC (SopSiC) technology [3.108, 3.129]. A high resistivity silicon wafer is bonded on top of a polycrystalline SiC substrate. Smart-Cut splitting is used to remove some of the HR-silicon substrate, so that a crystalline substrate surface is maintained. The composite substrate has the good thermo-mechanical properties of polycrystalline SiC. This allows to increase the substrate diameter beyond the diameter of available s.i. SiC substrates. A MOCVD-based wafer technology on metallic nickel substrates is described in [3.209]. The metallic substrate is based on nickel electroplating and laser lift-off. Prior to lift-off, the Schottky diode epitaxial layers are grown by MOCVD on sapphire substrates. MBE growth of GaN on LiGaO_2 is described in [3.38]. Lithium gallate has limited thermal conductivity, while it has a very low lattice-mismatch relative to all other hetero-substrates available for III-N devices. As a true insulator, the RF-losses can be greatly reduced compared to compensated material. The material grown by MBE has a TDD of only $4\text{--}5 \times 10^8 \text{ cm}^{-2}$. AlGaN/GaN HEMT on AlN templates on sapphire are reported in [3.8]. The TDD can be reduced to $1.5 \times 10^8 \text{ cm}^{-2}$ in this case.

3.1.4 Epitaxial Lateral Overgrowth (ELO)

Epitaxial lateral overgrowth (LEO) or (ELO(G)) is most important in the reduction of the dislocation density especially for III-N optoelectronic devices such as lasers [3.141]. A good overview of ELO is given in [3.51]. Threading dislocation densities as low as $2.2 \times 10^7 \text{ cm}^{-2}$ are reported in [3.53]. Several examples exist for ELO growth for electronic devices. The effect of threading dislocations on AlGaN/GaN HBT performance is reported in [3.127]. Device results obtained on conventional substrates and ELO substrates are compared. The reduction of the threading dislocation is found crucial for the reduction of the emitter-collector leakage, which is reduced by four orders of magnitude. A comparison of AlGaN/GaN HEMTs on sapphire substrates with and without grooves is provided in [3.45]. The devices with local grooves and increased crystalline quality yield an increase of drain current, transconductance, and output power. Further, the leakage currents are reduced.

3.1.5 Hydride Vapor Phase Epitaxy (HVPE)

HVPE is a very attractive option as a high-throughput and low-cost methodology for the growth of GaN quasi-substrates [3.159] due to its high growth

rate, which enables very thick III-N layers [3.198]. The growth rates for HVPE of device layers are typically adjusted to $0.05\text{--}0.3\mu\text{m min}^{-1}$, as reported in [3.109]. A good overview of the growth of GaN by HVPE is given in [3.198]. The principle of hydride vapor phase epitaxy for III-V element semiconductor is based on the flow of group-V hydride precursors and hydrogen chlorides in combination with nitrogen through a multizone furnace, typically consisting of quartz. The furnace has three functions and areas: a source zone, a mixing zone, and a deposition zone.

A quasi-substrate approach for epitaxial layer growth is presented in [3.159]. The HVPE layers are grown on GaN MOCVD templates on sapphire substrate. A detailed strain analysis is performed, which explains the strong wafer bending after removal of the sapphire substrate. Thicker sapphire substrates are suggested to reduce the wafer bending. On the device level, the fabrication and characterization of heterojunction GaN diodes is described in [3.35]. The active GaN layers are grown by HVPE on 4H-SiC substrates. Layers with thicknesses between 10 and 200 μm grown by HVPE are investigated. GaN/AlGaN HEMTs grown by HVPE on AlN/SiC substrates are described in [3.109]. A 30 μm -thick insulating AlN layer is deposited on undoped conducting SiC substrates. The actual HEMT layer structure consists of a 3 μm -thick GaN layer and a 40 nm-thick $\text{Al}_{0.28}\text{Ga}_{0.72}\text{N}$ layer grown by MOCVD. The device yields relatively low low-frequency dispersion, which is attributed to the reduction of the lattice-mismatch and the consequent dislocation reduction in the very thick AlN buffer layer. The use of HVPE-grown buffer layers on sapphire substrate is described in [3.52]. MBE is used to grow the epitaxial layers. The uniformity of the device DC-parameters despite the more complicated approach. Complete growth of AlGaN/GaN HEMTs by HVPE on sapphire substrates is reported in [3.123]. Both buffer layers and epitaxial layers are grown by HVPE and yield an RMS surface roughness of $\leq 0.2\text{ nm}$. AlGaN/GaN HEMTs with a gate length $l_g = 1\mu\text{m}$ are defined with a transconductance in excess of 110 mS mm^{-1} and $I_{D\max} = 0.6\text{ A mm}^{-1}$.

3.2 Indium-Based Compounds and Heterostructures

The growth of (Al)In(Ga)N and related ternary and quaternary materials for electronic applications has not yet been as exploited as the growth of (Al)GaN [3.2]. The InGaN/GaN heterostructures are essentially developed for optoelectronic applications, e.g., [3.176]. The promise of very low effective masses of InN down to $0.05 m_e$, see [3.49], and the remarkable transport properties [3.177] motivate the development of growth for electronics, e.g., [3.116, 3.130, 3.151, 3.175, 3.224]. The growth kinetics of InN and InGaN are reviewed, e.g., in [3.14, 3.225]. In general, the decomposition temperature of InN is relatively low, typically $\leq 600^\circ\text{C}$, as mentioned in [3.73]. The growth of InAlN is described, e.g., in [3.74, 3.91]. Thus, the growth temperatures of InN by MOCVD typically amount to $300\text{--}500^\circ\text{C}$. This temperature range is

typically too low for the growth of low-defect material, when MOCVD growth or ammonia-based MBE are being used. This is due to the decomposition rate of the ammonia gas in the reactor [3.73], as the temperature must satisfy the temperature conditions of NH₃ pyrolysis, while the dissociation of InN must be avoided [3.146]. The realization of double heterojunction FETs is very desirable, since the enhancement of the confinement effect in double heterojunction is favorable for device performance [3.115]. In-inclusion may help to increase the flexibility of the barrier definition at the frontside and the back-side of the channel [3.116]. Further, increased sheet carrier densities can be achieved in InAlN/GaN heterostructures, as discussed below [3.91, 3.122].

3.2.1 MOCVD Growth of Indium-Based Layers

Early reports on MOCVD growth of InN on various substrates, such as Al₂O₃ or even GaAs, can be found in [3.226]. Growth is performed at atmospheric pressure on α -Al₂O₃, and good conductive properties are reached with intrinsic concentrations $n = 5 \times 10^{19} \text{ cm}^{-3}$ and Hall mobility values of $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. In more recent reports, low-temperature MOCVD growth of InN is analyzed, e.g., in [3.173]. Thin InN films of 100 nm thickness are grown at 530°C on low-temperature (grown at 400°C) InN nucleation layers and on high-temperature GaN buffer layers. A near band-edge PL emission of 0.75 eV is observed already in this publication, which points to the revision of the bandgap energy of InN. On the device level a comparison of Al_{0.15}Ga_{0.85}N/GaN/Al_{0.15}Ga_{0.85}N and Al_{0.15}Ga_{0.85}N/InGaN/Al_{0.15}Ga_{0.85}N double heterostructure HEMTs (DHHEMTs) grown by MOCVD on s.i. SiC substrates is given in [3.122]. The comparison of the devices at 77 K proves the superiority of the double heterostructure concept with respect to 2DEG mobility and sheet carrier density. AlGaN/GaN/AlGaN DHHEMTs show enhanced mobility relative to the AlGaN/GaN single heterostructures. The mobility amounts to $>8,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the DHHEMT at 77 K. The inclusion of a In_xGa_{1-x}N layer with $x = 6\%$ leads to an increase of the mobility for a given sheet carrier density.

Growth Conditions: Material Transport and Temperature

Growth conditions of InN by MOCVD are characterized by low growth-temperatures and high growth-pressure [3.14]. It is the most difficult among the III-nitrides because of the low dissociation temperature of InN and the high equilibrium N₂ pressure. A good overview on the growth parameters and the substrate situation is given there [3.14]. InN growth on sapphire substrate by MOCVD reported in [3.226] yields InN with carrier densities of $5 \times 10^{19} \text{ cm}^{-3}$ and a room-temperature Hall mobility of $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. A very high V/III ratio of 10^5 is used for MOCVD in this case. TMI and ammonia are used as precursors at growth temperatures of 450–550°C and reactor pressures of 0.1–1 bar. The increase of the growth rate and the use of

nitrogen increase the In incorporation at a given temperature, as reported in [3.36]. The impact of reactant gas on the growth of InN by MOVPE is reported in [3.227]. Growth rates of InN as high as $2\text{ }\mu\text{m h}^{-1}$ are reached. A $0.5\text{ }\mu\text{m}$ thick InN layer yields intrinsic carrier concentrations of $10^{19}\text{--}10^{20}\text{ cm}^{-3}$. The room-temperature Hall mobility range is $260\text{--}120\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$. Growth temperatures of $400\text{--}600^\circ\text{C}$ have been used. A 1 nm thick $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ notch can be introduced into the GaN/AlGaN SHHEMT layer sequence to form a double heterostructure composed of GaN/ $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ /AlGaN [3.154, 3.224]. The GaN buffer growth is performed at 550°C . The temperature is then increased to 810°C for the growth of the InGaN. A 11 nm-thick GaN channel is grown at 920°C , followed by an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier grown at $1,020^\circ\text{C}$ [3.153]. The devices yield excellent cut-off frequencies of $\geq 150\text{ GHz}$ for a gate length of 100 nm.

3.2.2 MBE Growth of Indium-Based Layers

Molecular beam epitaxy, especially plasma-assisted MBE, is advantageous for the growth of indium-based compounds, as the growth temperature can be modified significantly as compared to MOCVD growth. Nitrogen radicals can be generated in the plasma source independent from the growth temperature, which does not have to satisfy the requirements of NH_3 pyrolysis. This principal effect especially increases the material quality. A review of MBE growth of InN and InGaN is given in [3.146].

Growth Conditions: Temperature and Material Transport

Reports on the growth of InN films and InAlN/InN heterostructures similar to the InGaAs/InAlAs material system can be found in various publications, e.g., in [3.74, 3.76, 3.146, 3.199]. The bandgap energy of InN has been under constant investigation during the development of the material system. A good review of the recent material development and bandgap investigations of InN and InGaN is given in [3.147]. Recent estimates of the bandgap energy of InN derived from photoluminescence properties of undoped and Si-doped InN films grown by PAMBE amount to 0.76 eV at RT [3.76]. The impact of the interface and crystalline effects is further detailed. In general, the material quality can be improved significantly by PAMBE growth, as compared to ammonia-based MBE and MOCVD. Indium incorporation and surface segregation during $\text{In}_x\text{Ga}_{1-x}\text{N}$ growth by PAMBE are discussed in [3.24]. The temperature for the growth of InGaN on sapphire substrates is chosen between 580 and 620°C . A low-temperature GaN buffer is grown at 550°C . The growth rates for both GaN and InGaN amount to 200 nm h^{-1} . The material fluxes are adjusted to match $\text{In}_x\text{Ga}_{1-x}\text{N}$ with an indium fractions of $0\text{--}0.5$. High-quality InN films based on plasma-assisted MBE are reported in [3.73]. The growth temperature for the low-temperature InN buffer layer amounts to $240\text{--}420^\circ\text{C}$, while the actual InN layers are grown at $380\text{--}520^\circ\text{C}$. Both an annealing step at growth

temperature and a rapid cooling at 200°C after the actual growth are applied. The mobility increases as a function of growth temperature between 380 and 490°C, whereas the intrinsic carrier concentration drops. The maximum Hall mobility at room temperature reaches $1,420 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at a background electron concentration of $1.4 \times 10^{18} \text{ cm}^{-3}$. The corresponding growth temperature is 490°C. Earlier reports in [3.71] show Hall mobilities of $1,420 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at electron concentrations of $1.6 \times 10^{18} \text{ cm}^{-3}$ for 350 nm thick films. PAMBE growth, characterization, and properties of InN and $\text{In}_x\text{Ga}_{1-x}\text{N}$ on sapphire substrates are further reported in [3.146]. The importance of the V/III ratio is pointed out in a trade-off between In-droplet formation (In-rich growth) and high N-partial pressure (to avoid dissociation). Considering both limitations the V/III ratio at the surface should be controlled to stoichiometry maintaining the the surface slightly N-rich [3.146]. The growth temperature is chosen between 460 and 550°C. Further, the importance of the nitridation procedure on the sapphire and the two-step growth with the low-temperature buffer are highlighted. The effects of atomic hydrogen irradiation on indium incorporation and ordering in $\text{In}_x\text{Ga}_{1-x}\text{N}$ grown by RF-MBE at 640–700°C are discussed in [3.152]. The indium incorporation and ordering are enhanced by the presence of H₂. InAlN is grown by MBE at a temperature below 460°C for the incorporation of In due to the wek In-N bond [3.91]. The next paragraph addresses heterostructure growth.

3.2.3 Indium-Based Heterostructure Growth

Both (In)GaN/InAlN and InGaN/GaN heterostructures can be formed once indium sources are available in the growth system. Al-rich $\text{In}_y\text{Al}_{1-y}\text{N}$ can be used effectively as barrier material for heterostructures with high sheet carrier densities [3.91]. Growth temperatures of 400 and 480°C are reported in [3.72] for the growth of $\text{In}_{0.15}\text{Al}_{0.85}\text{N}$ barriers on GaN by PAMBE on sapphire substrates. Sheet carrier densities of $1.7 \times 10^{13} \text{ cm}^{-2}$ and associated Hall mobility values of $654 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at room temperature are reported using an additional AlN interlayer. After the growth of an AlN-nucleation layer at 900°C, the GaN buffer layer is grown at 730°C by PAMBE. The AlN interlayer with a nominal thickness of 1.3 nm is grown at 760°C. For the $\text{In}_{0.15}\text{Al}_{0.85}\text{N}$ barrier layer, the growth is performed at 400 and 480°C. Better mobility and surface quality are achieved for the higher growth temperature. The subsequent processing of InAlN/GaN HFETs is also reported.

$\text{In}_{0.2}\text{Al}_{0.8}\text{N}/\text{GaN}$ heterostructures grown by MOCVD on sapphire(0001) substrates are given in [3.107]. The layer sequence includes a low-temperature GaN nucleation layer, a 1.4 μm-thick GaN buffer layer, and a 10 nm $\text{In}_{0.2}\text{Al}_{0.8}\text{N}$ barrier layer grown between 800 and 850°C. The Hall mobility and sheet carrier concentration amount to $2 \times 10^{13} \text{ cm}^{-2}$ and $260 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. InAlN/GaN heterostructures grown by MOCVD on silicon(111) substrate are reported in [3.210]. A 300 nm-thick (Al)GaN nucleation layer is deposited on high-resistivity 3-in. n-silicon substrates. A 1 μm-thick GaN buffer is capped

by an $\text{In}_{0.16}\text{Al}_{0.84}\text{N}$ barrier layer. A 1 nm AlN layer can be included between channel and barrier. The barrier layer thickness is 20–25 nm. The Hall mobility amounts to $1,200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ without inclusion layer, and $1,800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ with AlN-inclusion layer. The related sheet carrier densities are 0.8×10^{13} and $1.5 \times 10^{13} \text{ cm}^{-2}$. The findings in this section demonstrate the potential to increase the sheet carrier density in the heterostructures with the use of In and potentially to improve the associated mobility.

3.3 Doping and Defects

Doping and defects are fundamental for electronic device fabrication in any semiconductor system [3.202]. Defects in MOCVD- [3.143] and MBE-grown material [3.69] are found to be strongly growth-method dependent, as reported in various publications, e.g., [3.57, 3.118, 3.170]. Defects can be categorized in point, line, and areal defects [3.119, 3.170]. The important point defects are vacancies and interstitials, the line defects are threading dislocations, and areal defect are stacking faults [3.119]. These defects are thus discussed for each growth method. Good overview articles on defects in III-N materials are given in [3.118, 3.138, 3.160]. Early overview data for defect related donors, acceptors, and traps in GaN grown by MOCVD, MBE, and HVPE are given in [3.118]. The impact of surface stoichiometry and polarity on the defect structure for GaN is discussed in [3.178]. Point defects can be deliberately generated by various types of irradiation, such as electrons, protons, ions, γ -ray, and metal deposition by electron beam. The signatures obtained from the defect creation can then be compared to as-grown materials. It is stressed in [3.118] that shallow defects are dominating and that impurities such as Si and O are dominant in early as-grown GaN layers rather than defects. Threading dislocations in n-GaN are reported to have an acceptor-like behavior [3.118].

A very recent extensive review of the luminescence of defects in GaN, InN, and AlN is given in [3.170]. GaN is considered to break the long-standing paradigm that high defect densities precludes electronic device performance. Minimum nonintentional acceptor concentrations are found to be 10^{15} cm^{-3} even in the purest material. This also leads to a minimum of uncontrolled compensation in n-type material. Zn, Mg, C, Si, H, O, Be, Mn, and Cd are considered the most important impurities. The dominant role of extended defects such as treading dislocations and point defects such as nitrogen vacancies is also discussed in [3.160]. It has further been found in GaN and the related materials AlN, InN, InGaN, InAlN, AlGaN, that hydrogen is present in relatively high concentrations in as-grown samples, especially in p-type GaN [3.148]. It has been shown experimentally that the amount of oxygen present during material growth can have a strong influence on the background conductivity, indicating that it is a shallow donor in GaN. Carbon can also be a significant residual impurity in MOCVD-grown nitrides. Its

source is typically the precursor. Typical characterization methods for defects include [3.118] the following:

- Temperature-dependent Hall measurements for the determination of the donor and acceptor concentrations
- X-ray diffraction (XRD)
- Transmission electron microscopy (TEM)
- Photoluminescence (PL)
- Atomic force microscopy (AFM)
- Positron annihilation spectroscopy (PAS)
- Magneto-resonance
- Deep-level transient spectroscopy (DLTS) [3.118]

The analysis of threading dislocations has already been mentioned. A more detailed analysis is presented in the following.

3.3.1 MOCVD Growth

Shallow- and deep-level defects in n-doped GaN grown by MOCVD are described in [3.54].

Doping in n-Doped and p-Doped MOCVD Material

Silicon introduces a shallow donor level in GaN at $E_C - 0.022\text{ eV}$ [3.54, 3.56] and is found to be the dominant donor impurity in unintentionally (nid)-doped material. A deeper donor is also found at $E_C - 0.034\text{ eV}$. Oxygen is another donor for GaN [3.160]. It is found to have a strong impact on the n-type background conductivity. It is prevailing due to the precursor NH_3 in MOCVD-grown material. A donor state at $E_C - 0.078\text{ eV}$ is mentioned.

Mg and Zn are the most important acceptors in a number of p-dopants for III-N semiconductors, such as C-, Mg-, and Be-. They generally are not very efficient acceptors. The p-doping of GaN is complicated by the following effects, which have been named repeatedly [3.143]:

- Large thermal activation energy of 120–200 meV [3.54]
- Hydrogen passivation of MOCVD-grown GaN:Mg [3.143, 3.160] and
- Significant Mg reactor memory leading to broad Mg profiles, reported, e.g., in [3.62, 3.186]

Early overviews of the compensation mechanisms of p-doping are given by Nakamura in [3.143] and further, e.g., in [3.105, 3.121]. Mg has been described early as an acceptor in GaN at an electronic level of approx. $E_V + 0.2\text{ eV}$, e.g., in [3.54]. It is the most important acceptor for GaN. A midgap trap level is isolated in p-type GaN with a photoionization energy of 1.8 eV. However, none of the deep levels is found to be of sufficient concentration to compensate the shallow acceptors. Mg accumulation effects in bulk samples at doping levels of 3×10^{19} to $9 \times 10^{19}\text{ cm}^{-3}$ due to surface treatment and air exposure

are reported in [3.62]. A strong surface band bending is observed of 1.2–1.6 eV for GaN:Mg. This is considered to be due to high-density surface states. Even strong wet etching by KOH and NH₄OH does not modify this high surface state density [3.62]. Hydrogen in general plays a dominant role for the passivation of acceptors [3.160]. Early reports of the activation of p-type GaN material by post-annealing steps at 800°C in nitrogen are given in [3.121, 3.143]. A more detailed overview on the impact of hydrogen is given in [3.160]. Carbon is a residual impurity in MOCVD-grown material. C is discussed to be both an acceptor and an amphoteric. Maximum hole concentrations of $3 \times 10^{17} \text{ cm}^{-3}$ are reached at a mobility of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [3.160]. P-doping of AlGaN is even more complicated than GaN, as reported, e.g., in [3.47]. The background is the even higher activation energy of Mg in AlGaN, the increased compensation due to Si in the precursors, and the interaction with Si, C, and O. The measured hole concentrations in AlGaN are even more strongly reduced than in GaN. Other p-dopants such as Ca, Zn, C, and Cd in the material have to be considered, as also reported in the overview on defects in GaN in [3.160].

Defects in MOCVD-Grown Material

Defect concentrations in the form of threading dislocations and other defects are of critical importance, as most of the electronic devices are grown by heteroepitaxy and a minimum mismatch relative to the semiconductor layers. A great number of reports exist on different defect types [3.138, 3.160, 3.170]. DLTS analysis of the barrier-layer material AlGaN is of importance due to the impact on dispersion in III-N FETs, similar to that of AlGaAs in GaAs PHEMTs. A donor-like deep-level defect in Al_{0.12}Ga_{0.88}N grown by MOCVD on SiC substrate is found by DLTS at $E_C - 0.77 \text{ eV}$, as reported in [3.55]. Deep levels are found by DLTS at threshold energies of 0.83 and 1.01 eV in n-doped GaN [3.54] grown by MOCVD. Further deep levels between $E_C - 0.87 \text{ eV}$ and $E_C - 1.59 \text{ eV}$ are reported. Luminescence, especially yellow luminescence, is of particular interest for electronic material analysis, e.g., by photoluminescence and surface photovoltage spectroscopy [3.181]. Yellow luminescence and related deep traps in undoped GaN grown by MOCVD are investigated in [3.22, 3.181]. For GaN layers the band energy of the luminescence is about 2.2 eV with a broad spectrum. It is present for different substrate types. The background of this emission are deep traps about 1 eV above the valence band which capture photoelectrons. Localized high current densities around screw dislocations in GaN films grown by MOCVD are investigated by ballistic electron emission spectroscopy (BEEM) in [3.18]. A correlation of the threading dislocations and charged traps is suggested, which leads to poor Schottky characteristics. Both donor- and acceptor-type behavior of threading dislocations are reported, as also stated in [3.118]. Apart from the detailed detection of single defects and traps, the correlation of defects with device performance is interesting. Deep traps in GaN MESFETs and their correlation with current

collapse are analyzed in [3.55]. Two electron trap energies are isolated for this n-channel device. The defect energies of 1.8 and 2.85 eV below the conduction band have also been reported in other publications, e.g., in [3.22]. Variation of the edge dislocation concentration with the AlN nucleation layer design is directly correlated with the AlGaN/GaN reliability [3.57]. Traps can also be created by device operation and related degradation, as reported in [3.187]. Further analysis is provided in Chaps. 4 and 7.

3.3.2 MBE Growth

Surveys on doping and defects for MBE-grown materials are given, e.g., in [3.160, 3.170, 3.203].

Doping of n-doped and p-doped MBE Material

The most important n-dopant in MBE material is silicon. N-doped GaN material grown by MBE is characterized by a number of particular defects. Deep-level transient spectroscopy (DLTS) investigations in MBE-grown GaN material are given in [3.69]. The n-type GaN material is grown by MBE on MOCVD-grown templates on sapphire substrate. The characteristic capture-time constant obtained amounts to $8.6\text{ }\mu\text{s}$ for a line-type deep trap at $E_C - 0.91\text{ eV}$. A defect found at $E_C - 0.59\text{ eV}$ does not show the behavior of a line or point defect. A comparison of the MBE growth of thin wurtzite GaN on 6H-SiC, silicon(111), and sapphire substrates is given in [3.190]. Cross-sectional TEM measurements of the n-type GaN materials reveal the domination of threading defects at the substrate/buffer or buffer/film interfaces at residual concentrations of $10^8\text{--}10^9\text{ cm}^{-2}$.

N-doping is typically performed by standard silicon effusion cells, e.g., [3.68]. Silane can be used as a silicon source for ammonia-based MBE [3.194]. Next to silicon, oxygen is also considered as a donor for MBE grown material [3.160]. Residual water vapor in MBE chambers or oxygen impurities leaked from the quartz containment vessel often employed in N_2 plasma sources is considered as the source.

P-doping of MBE material is different from that of MOCVD material. Typical for MBE, the doping profiles of MBE III-N material can be very sharp. Mg p-doping of GaN by PAMBE on MOCVD-grown GaN templates on sapphire substrates is described in [3.186]. MBE growth can cure two further disadvantages of GaN:Mg growth by MOCVD. It avoids hydrogen passivation of the Mg, and no Mg reactor memory is observed during MBE growth. The GaN:Mg layers are grown by PAMBE at 650°C . Mobilities $\mu_p = 24\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $p = 1.8 \times 10^{17}\text{ cm}^{-3}$ and $\mu_p = 7.5\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at $p = 1.4 \times 10^{18}\text{ cm}^{-3}$ are reached. The incorporation of Mg is uniform and very sharp profiles can be realized due to the low growth temperature, as verified by SIMS measurements. The sharp profiles further allow very precise superlattice engineering and Mg profiling, as reported in [3.106]. Superlattice dimensions are varied

between 2 and 14 nm in order to enhance the active hole concentration in the superlattice beyond 10^{18} cm^{-3} , especially at low temperatures.

Defects in MBE Material

Deep level defects in n-type GaN material grown by MBE are described, e.g., in [3.207] found by DLTS. Five deep traps are reported between $E_C - 0.23 \text{ eV}$ and $E_C - 0.96 \text{ eV}$. The capture cross-sections amount to $2 \times 10^{-15} \text{ cm}^2$ (0.59 eV) and $3 \times 10^{-14} \text{ cm}^2$ (0.91 eV). Similar point defect serving as electron traps are found at $E_C - 0.06 \text{ eV}$ and at $E_C - 0.9 \text{ eV}$. Capture cross-sections of 5.0×10^{-15} and $7.4 \times 10^{-17} \text{ cm}^2$ are determined for electron levels of 0.21 and 0.23 eV in PAMBE-grown AlGaN/GaN/AlGaN heterostructure material [3.158]. The 0.21 eV defect is related to a nitrogen vacancy, while 0.23 eV is associated with extended defects.

Defect microstructure of thin wurtzite GaN films grown by MBE on SiC substrates, silicon substrates, and sapphire substrates are analyzed by TEM in [3.190]. Threading dislocations are line defects along the growth direction. The defect microstructure is dominated by threading defects that originated at the buffer/substrate or buffer/epilayer interface. A defect density of $10^8 - 10^9 \text{ cm}^{-2}$ is found to be prevailing depending on the substrate. This density is residual despite the reduction of defects by the use of a 1 μm -thick buffer layer. HVPE-grown material has also been investigated in several publications, e.g., in [3.170, 3.223]. Three traps are isolated in [3.223] at energies $E_C - 0.65 \text{ eV}$, $E_C - 0.61 \text{ eV}$, and $E_C - 0.27 \text{ eV}$.

The previous section has demonstrated the impact of impurities and defects; however, the most important requirement for electronics is their avoidance and control during material growth, which is part of this chapter. Control of processed-induced defect creation will be addressed in Chapter 4.

3.4 Epitaxial Device Design

In the previous sections, a number of specific growth features and their characteristic methodologies have been discussed for the InGaN/AlGaN/InAlN/GaN material system. This section addresses particular features for device growth. As an example, Fig. 3.17 gives the layer sequence of advanced HFETs for both the III-As and the III-N material system. Fig. 3.17 visualizes and compares the concept of a double heterojunction and the specific device features with respect to epitaxial growth, as also proposed, e.g., in [3.104]. These features are detailed in the following sections and compared, where necessary, to III-As devices.

3.4.1 Geometrical Considerations

Geometrical considerations are numerous in the design of III-N devices. Most data are available on the fabrication of HFETs.

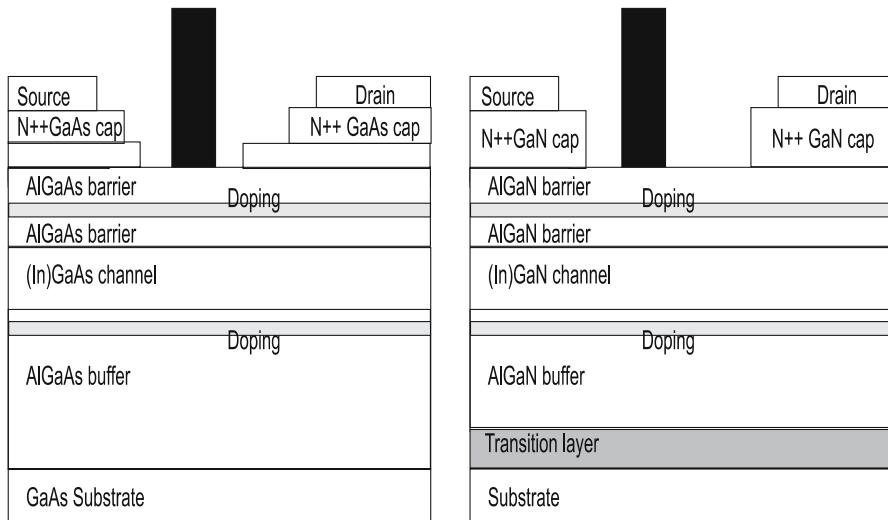


Fig. 3.17. Schemes of advanced double-heterojunction HFETs: (*left*) GaAs, (*right*) GaN

Barrier-Layer Design: Thickness

The barrier-layer thickness in HEMTs is a principal design feature. It is evaluated in [3.197]. Nonrecessed AlGaN/GaN HEMTs with barrier thicknesses of 10 and 20 nm are compared. As expected, the device with the thinner barrier layer shows reduced current due to the reduced polarization effects and higher transconductance. Further, a reduced saturated power density is obtained. RF-loadline measurements show the reduction of RF-full channel current as compared to DC full channel current and the increase in the RF-knee voltage for the devices with a smaller gate-to-channel separation. Thus there is a reduction in output power due to these surface-induced dispersive effects. The second effect on the output power at a given voltage is the expected reduced polarization effect, as also argued in [3.75]. The barrier thickness and mole fraction also strongly influence the vertical field distribution in the barrier, as measured by photoreflectance spectroscopy in [3.20]. The polarization effects lead to electrical fields $\geq 1 \text{ MV cm}^{-1}$ [3.220]. A systematic investigation of the gate-to-channel-separation is performed in [3.75] for AlGaN/GaN HEMTs with a gate-length of $1 \mu\text{m}$ grown by PAMBE on sapphire substrates. The gate-to-channel separation is varied between 8 and 25 nm. The reduction of the gate-to-channel separation leads to a significant increase of the transconductance from 185 to 360 mS mm^{-1} . At the same time, the drain current at $V_{GS} = 1 \text{ V}$ is reduced from 1.1 to 0.68 A mm^{-1} . The positive threshold voltage shift is about 0.23 V per 1 nm change of the layer thickness. For very-high operation frequencies, a gate-to-channel separation of 11.3 nm is used in [3.77] for an HFET with a gate length of 60 nm . Very

thin $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layers in MOSHFETs are reported in [3.70]. A 7 nm-thick AlGaN layer leads to a threshold voltage of -0.3 V . The situation is close to a normally-off device. Al_2O_3 gate layers are used. The MOSHFET allows the overdrive of the device up to gate voltages of $+4\text{ V}$. Theoretical estimates for the impact of the barrier-layer thickness and the Al-content on the power performance and corresponding gain compression are discussed in [3.43]. An increase in output power is predicted with increasing barrier thickness and Al-content. Further geometrical issues for the design of (H)FETs include the following:

- The distance of δ -doping layers to the channel [3.48]
- The position of the (backside) InGaN layer to the channel [3.26, 3.153, 3.154]
- The thickness of doped GaN layers in recess processes, e.g., in [3.98]

The distance of the δ -doping of AlGaN/GaN HEMTs is optimized in a similar procedure as for GaAs PHEMTs, as reported in [3.48]. The considerations include scattering of the carrier in the channel and also doping efficiency. The optimum value amounts to 3–6 nm. The thickness of GaN cap layers needs to be optimized with respect to the surface depletion, as performed in [3.98]. In recess structures, the layer depth needs to be adjusted to the GaN etch process, as further described below and in Chapter 4.

Barrier-Layer Design: Mole Fraction

The Al-mole fraction in the barrier is a critical parameter in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ and $\text{In}_x\text{Al}_{1-x}\text{N}/\text{GaN}$ HFETs. Increased Al-contents promise higher sheet carrier concentrations in the channel at nearly constant mobilities. Devices with Al-concentrations of $\geq 35\%$ are reported, e.g., in [3.94, 3.222]. The findings with an increase of the mole fraction in the barrier layer include the following:

- Eventually a saturation of the sheet carrier concentration due to relaxation of the AlGaN barrier layer, and grain formation, which both reduce the polarization effects
- Reduced doping efficiency of the Si doping
- Increased ohmic contact resistances

Typically, optimized single heterostructure FETs have Al-contents of 20–30% [3.204]. Al-contents between 26 and 52% are investigated on 4-in. sapphire substrates in [3.136]. The increase in Al-content leads to reduced surface quality and increased gate leakage, especially for Al-contents of 52%. The geometrical considerations have already been discussed above.

3.4.2 Growth of Cap Layers

Cap layers are introduced to moderate the transition at the semiconductor-passivation interface. In many publications, thin undoped GaN layers are

reported for improved contact formation, e.g., in [3.12, 3.216]. The thicknesses are 1 nm in [3.32, 3.135], 3 nm in [3.12], and up to 5 nm in [3.166, 3.216]. The specific formation of electron and hole gases in cap layers can be investigated by photoreflectance spectroscopy [3.19, 3.191]. It becomes obvious, that small variation in the cap layers thickness in the nm-range have strong impact to the field distribution. Highly n-doped caps are generally used in any semiconductor system to facilitate ohmic contact formation in order to increase the density of states at the metal semiconductor interface. This is especially necessary for wide bandgap semiconductor devices, which require very high annealing temperatures to reach ohmic-type contacts. Highly-doped GaN caps have further repeatedly been suggested to reduce dispersive effects, e.g., in [3.12, 3.75, 3.97]. The resulting devices show reduced dispersion even for the unpassivated situation [3.182]. However, the high doping levels lead to prohibitive gate-leakage currents, which unfortunately reduce the operation voltage without the applications of further steps such as recessing to $V_{DS} = 15$ V only [3.182]. P-doped GaN caps with very high nominal Mg concentrations of 1×10^{20} cm $^{-3}$ have been used to minimize RF- and DC-dispersion in AlGaN/GaN HEMTs, as reported in [3.12, 3.30]. The physical effect of high n- and p-type doping concentration is similar and is based on the compensation of traps and related charge at the semiconductor/passivation interface. The effect of MOCVD growth-termination conditions at the top cap layer above the barrier layer and the impact of wafer cool-down on the performance of the total GaN FETs is further investigated in [3.93]. A modest improvement in the device power density is observed for wafers, if, after deposition of the AlGaN layer under constant growth conditions, the samples are cooled down to room temperature in pure nitrogen. Insulating low-temperature-grown GaN-cap layers are used for the reduction of the dark currents in Schottky-barrier photodetectors [3.110]. The low-temperature GaN is grown at 560°C and reduces the dark current by four orders of magnitude. Superlattice cap layers have been recently proposed in order to reduce the source resistance of AlGaN/GaN HFETs [3.140]. Fifty nanometer thick superlattice-cap layers followed by a 20 nm n⁺-doped GaN cap are proposed. The layer thicknesses of the AlGaN barrier and of the superlattice layers are optimized with the aim to reduce the potential barrier at the AlGaN/GaN channel interface below the ohmic contacts. This leads to an overall reduction of the access resistances.

3.4.3 Doping

III-N devices are intrinsically doped by unintentional impurities and by polarization doping. In several reports, the intentional doping is completely based on the polarization mechanism, e.g., [3.39]. However, conventional impurity doping is used repeatedly in both HEMT [3.48] and HBT [3.128] structures for several reasons. On the device level, the impact of barrier doping on the performance of unpassivated AlGaN/GaN/SiC HEMTs grown by MOCVD is

reported on in [3.13]. Conventionally doped unpassivated AlGaN/GaN heterostructures are found to be less sensitive to dispersive mechanisms due to shielding of the channel from the barrier/dielectric interface. The effects of the variation of δ -doping and geometry in AlGaN/GaN HEMTs on SiC substrate are described in [3.48]. Both the position and the nominal doping concentration of the δ -doping are varied for spacer thicknesses of 3–9 nm. The sheet charge is optimized for a spacer thickness of 6 nm, while the mobility increases with increased distance. A doped-channel AlGaN/GaN HFET with isoelectronic doping in the channel is described in [3.83]. The thickness of the doped channel layer is 70 nm in this case, which is much larger than the typical extension of an AlGaN/GaN channel layer, which is estimated to be ≤ 10 nm.

3.4.4 AlN Interlayer

The channel-barrier interface in HFETs has been optimized with respect to several aspects, e.g., interface roughness [3.139, 3.155] and trap reduction [3.9, 3.82]. To that end, AlGaN/GaN high-power microwave HEMTs have been optimized by the introduction of a thin AlN interlayer with a thickness of a few monolayers, e.g., in [3.183]. The concept has repeatedly been published with different focuses [3.9, 3.11, 3.139]. The insertion of the thin AlN layer produces a larger effective conduction band discontinuity ΔE_C . This increase in effective ΔE_C is due to the polarization-induced dipole in the AlN [3.183]. This AlN interlayer concept implies the following advantages:

- Increased effective bandgap discontinuity [3.183]
- Decreased alloy scattering [3.9, 3.183] and thus increased channel mobility
- Increased mobility for a given sheet carrier concentration [3.139]
- Increased sheet carrier density [3.139]
- Reduced interface trapping [3.9]

Additional issues to be considered are the following:

- The introduction of an additional tunneling barrier near the ohmic contacts
- Potentially a diode-like access resistance [3.99], similar to RTD

This kind of diode-like behavior is caused by the potentially strong band bending at various bias conditions. If additionally an AlN interlayer is introduced to serve as a barrier layer, a resonance is possible between the contact and the diode. Fig. 3.18 gives the sheet carrier concentration and Hall mobility of AlGaN/AlN/GaN heterostructures as a function of AlN interlayer thickness, as shown in [3.139]. An optimized mobility is found for the thickness of ≈ 1 nm with mobility values of $1,700 \text{ V s cm}^{-2}$. The sheet carrier concentration increases steadily from 0.9 to $1.4 \times 10^{13} \text{ cm}^{-2}$. Fig. 3.19 further gives the sheet resistance as a function of AlN-interlayer thickness. A minimum is found at an interlayer thickness of about 1 nm. Further analysis of the drift mobility as a function of carrier concentration in [3.9] shows that the effect of the AlN layer specifically enhances the mobility at high carrier concentrations. In another

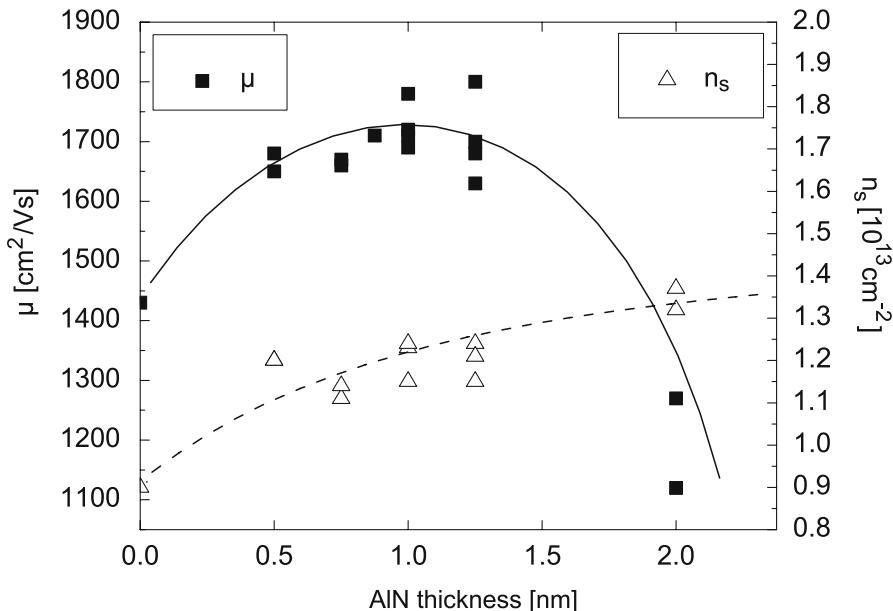


Fig. 3.18. Sheet-carrier concentration and mobility as a function of AlN interlayer thickness

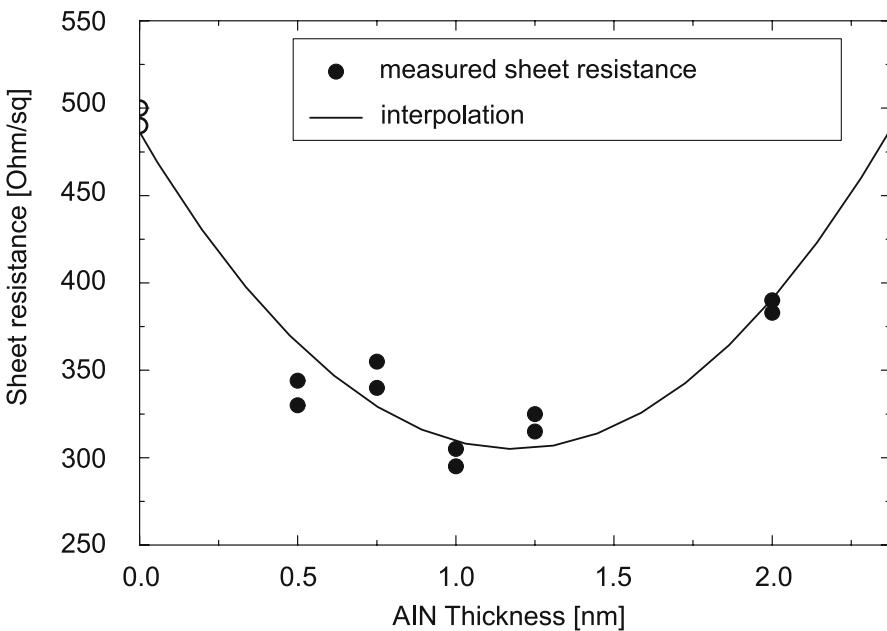


Fig. 3.19. Sheet resistance as a function of AlN interlayer thickness

device concept the AlGaN barrier layer can also be completely removed and the effect of the barrier is then performed entirely by the AlN-interlayer, as reported in [3.155].

3.4.5 Channel Concepts

Simple planar HFET structures use the extended buffer layers under the barrier as channel layers. Near the interface, the GaN is highly conductive. Nominaly, the channel layer is grown at a similar temperature to that used for the buffer layer, e.g., [3.92]. More advanced composite-channel concepts with varying Al-mole fractions in the channel/barrier have been introduced in [3.114]. The first channel forms at the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ interface, while the second channel forms at the $\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}/\text{GaN}$ interface. It has further been suggested that this graded-channel concept enhances linearity at 2 GHz; however, the improvements in linearity claimed are within the statistical scattering of the measurement data. Doped HFET channels with isoelectronic Al-doping in the channel have been described in [3.83]. The Al-doping is used to improve the crystalline quality of the channel layer by reducing the amount of threading dislocations serving as acceptors. This leads to an overall enhancement of the mobility. However, the absolute values of the Hall mobility reported can also be achieved by other means. Further channel concepts are based on double heterostructures. The layers for this concept can be grown by both MOCVD and MBE. $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}/\text{GaN}/\text{Al}_{0.05}\text{Ga}_{0.95}\text{N}$ based on MBE growth are described in [3.131]. The Al-fraction in the buffer has to be optimized with similar care as a GaN buffer with respect to unintentional doping, lattice mismatch, and defect mitigation. The Al-fraction thus cannot be chosen as freely as for a conventional AlGaAs/GaAs/AlGaAs HEMT layer structure.

3.4.6 Epitaxial In-Situ Device Passivation

Typically, the dielectric passivation in III-N devices is introduced by process-technological means, e.g., [3.136, 3.204]. This procedure is sometimes called ex-situ passivation. SiN can further be deposited in-situ, i.e., directly in the reactor growth chamber during MOCVD growth, as reported, e.g., in [3.201]. A thin SiN layer (4 nm) is deposited in the MOCVD chamber by flowing disilane and ammonia. The deposition is performed at a temperature of 980°C with a deposition rate of 0.1 \AA s^{-1} [3.27]. The growth temperature of the SiN is thus lower than that typically used for the AlGaN barrier. MBE layers can also be passivated in-situ; however, this is not done in the same MBE reactor chambers, but using subsequent MOCVD growth. Such a procedure thus includes an interruption of the growth process, as reported, e.g., in [3.166]. The more technologically based features of device design, such as recesses, contacts, implantation, and device passivation issues, are discussed in Chapter 4.

3.5 Problems

1. *Discuss the major differences of III-N growth by MOCVD, HVPE, and MBE with respect to relative advantages/drawbacks!*
2. *For which kind of devices does MBE growth have unique properties?*
3. *Discuss the possible advantages and drawbacks of indium-based FETs!*
4. *Discuss epitaxial measures for dispersion control!*
5. *What are typical growth issues for III-N HBT layers?*
6. *Which particular improvements/drawbacks can be found for GaN heteroepitaxy of HFET layers on GaN substrates?*

Device Processing Technology

A major focus of the development of III-N devices is devoted to process technology. III-N-based high electron mobility transistors (HEMTs) with gate lengths down to 30 nm and cut-off frequencies up to 180 GHz have been reported [4.91, 4.92]. Thus, for this class of devices, specific field-effect transistor problems, such as Schottky and ohmic contact definition, implantation, device isolation, lithography of transparent materials, and etching are discussed in this chapter. State-of-the-art recess processes and device passivation technologies are analyzed. Despite the limited number of publications, bipolar device technology issues are reviewed. As in every other semiconductor material system, the processing of nitride-based materials requires the development of a lot of specific technology, related mostly, but not exclusively, to the wide bandgap material properties. This specific development is addressed in this chapter.

4.1 Processing Issues

A large number of technological issues have to be solved to achieve III-N devices optimized for specific applications. A guideline to solve these issues, seen from a very general point of view, includes the following:

- The separation of process technology issues from epitaxial issues to achieve high uniformity as addressed, e.g., in [4.188]
- The improvement of the reproducibility of the processing steps and their results from wafer-to-wafer and run-to-run
- The improvement of the uniformity of process technology and yield
- The scaling of the process technology for different substrate diameters [4.23, 4.188]
- The increase and stabilization of long-term device reliability

With respect to improved FET and bipolar device performance, the processing issues include particularly the realization of the following:

- Devices with
 - High transconductance for high gain
 - High efficiency
 - High power at high-voltage operation
- Devices with high gain, low RF-noise, and low-phase noise

These requirements particularly include the need for the following:

- Good device isolation
- The realization of low-contact and access resistances
- FETs with
 - Improved gate barriers and reduced gate and drain leakage
 - Domain breakdown management by field shaping in the gate region to reduce leakage and to increase breakdown voltages
- Sufficiently high current levels in a trade-off with the necessary breakdown voltages
- Improved techniques for high current gain in bipolar devices
- Reduced low-frequency dispersion in all of its characteristics
- Backside processing of very hard and inert substrates materials with respect to thinning and viahole-etching

The measures to improve the devices are discussed with each processing step further below; however, these issues include the following:

- The introduction of new device concepts, such as
 - Single-field and multiple-field plate FET concepts with different electrical terminations
 - Polarization-engineered devices
- The understanding of critical processing steps, such as
 - Surface pre- and postprocessing
 - Implant and annealing processes
 - Vertical and lateral structuring
- The introduction of new materials, such as
 - III-N specific passivation layers
 - New contact metal sequences

These issues and requirements will now be discussed in detail.

State-of-the-Art

Details of device process technology are subject to intellectual property issues and thus to reduced publicity. Early reviews of III-N technology development are given, e.g., in [4.22, 4.263]. The overviews in general stress the requirement of specific elimination of trapping effects. Further overviews of III-N processing technology are given, e.g., in [4.55, 4.124, 4.188]. Typical process flows consist of

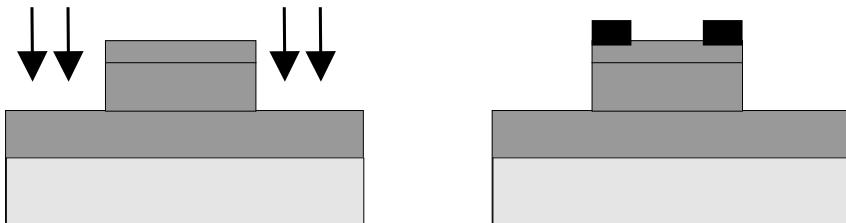


Fig. 4.1. Process flow of a GaN FET: (a) (left) mesa isolation, (b) (right) ohmic contact formation

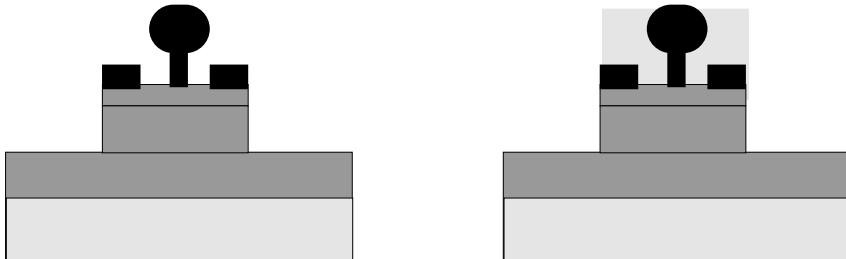


Fig. 4.2. Process flow of a GaN FET: (c) (left) gate definition, (d) (right) device passivation

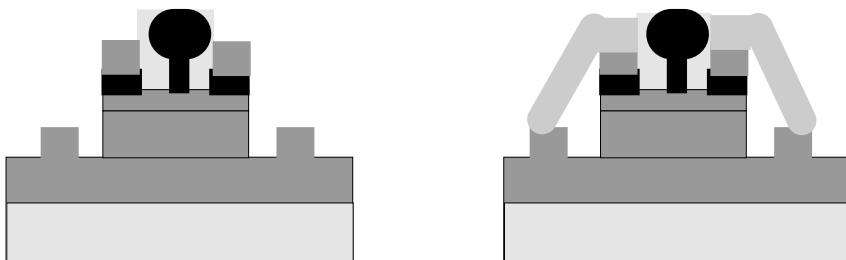


Fig. 4.3. Process flow of a GaN FET: (e) (left) second metal, (f) (right) galvanic metal

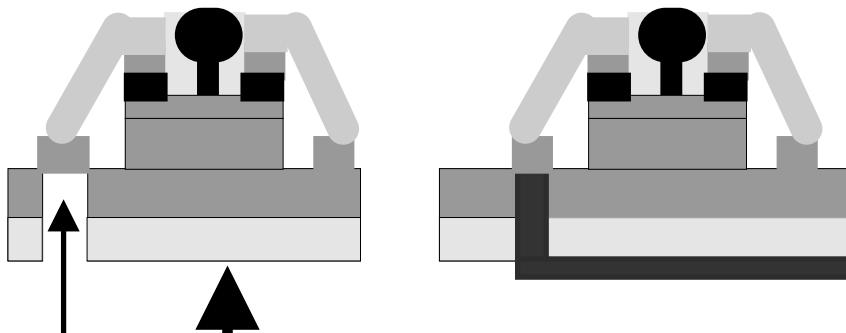


Fig. 4.4. Process flow of a GaN FET: (g) (left) thinning and etching, (h) (right) backside metallization

conventional III-V technology modules with selected III-N specific adaptions, such as rapid thermal annealing with very high temperatures. An advanced manufacturable GaN HEMT technology on 4-in. diameter high-resistivity Si substrates is described in [4.81]. It is fully based on optical stepper technology. Six mask levels are used for the formation of AlGaN/GaN HFETs. A similar high-voltage technology is proposed by Eudyna/Fujitsu in [4.128]. The processing is performed on 3-in. s.i. SiC substrates. The ohmic contacts are formed with a recess structure. A commercial GaN/AlGaN-based HFET device technology on s.i. SiC substrate is presented by RFMD in [4.221, 4.222]. The processing can be performed on a GaAs production line, while some nitride specific steps are inserted. Typical descriptions of basic GaN HEMT process flows are given, e.g., in [4.97]. A typical process flow is depicted in Figs. 4.1–4.4. The processing of FETs thus includes the following steps, but not necessarily in this order:

1. Device isolation
2. Ohmic contact formation
3. Gate recess definition
4. Gate definition and first metal formation
5. Partial and full device passivation
6. Galvanic processing, including the passive components
7. Backside processing
8. Dicing

Additional steps, such as ohmic recess formation [4.127], ohmic implantation [4.289], (multiple) gate-recess, and field-plate formation [4.283] can be added. Typical processes following this processing order can be found, e.g., in [4.22, 4.124, 4.166]. Typical modifications to this process flow include the following:

- The exchange of the order of ohmic definition and device isolation, especially when applying implantation [4.22]
- Early device passivation to reduce surface pollution before and during processing, e.g., [4.68, 4.244]
- A different processing order when opening the passivation for the SiN-assisted gate [4.81]

The processing steps will now be discussed in detail.

4.2 Device Isolation

Device isolation is one of the primary process steps and increasingly important due to the high-voltage operation proposed for III-N FETs. The two principal technologies of mesa etching and implantation are described in the following.

4.2.1 Mesa Structures

Mesa isolation is the simplest technique for the structuring of devices and for their electrical isolation from their next neighbors. The active semiconductor layers between different devices are physically removed, typically by etching down to an insulating layer or to the substrate. In the case of III-N FETs, the etch is performed mostly to the insulating GaN buffer, as shown in Fig. 4.1. Typically, residual currents measured between devices in mesa structures have to be reduced to levels of $\leq 10^{-9}$ A at voltages of 50 V [4.188] and above in order to ensure reliable device isolation. This is equivalent to resistances of $10 \text{ M}\Omega \text{ cm}$ and above. The resulting issues from the mesa process include the following:

- The control and reduction of surface currents
- The isolation of interconnect lines along conducting semiconductor layers at the mesa ridges
- The control of etched surface morphology

Several mesa processes have been described in the literature. A Cl₂/He-based ICP-RIE plasma dry etch is used in [4.30]. A Cl₂-based ECR process is proposed for device isolation in [4.55]. The typical etch depth is 200 nm. A medium RF-power Cl₂-based RIE etch process is described in [4.28]. The mesa etch depth is 120 nm. The etch rates for the mesa isolation reach 1 nm s^{-1} at RF-power levels of 100 W. A BCl₃-based RIE process is described in [4.58]. The RF-power level is 10 W and the etch rate reaches 6 nm min^{-1} in this case. The addition of CH₄ to BCl₃/H₂/Ar during ICP-based RIE improves the anisotropy of the etch and reduces the mask erosion [4.152]. The key disadvantage of such mesa processes is the generation of three-dimensional device structures on the wafer. This fact increases the complexity for the passive connection lines. Further mesa ridges are created that pose additional challenges for high-voltage isolation.

4.2.2 Ion Implantation for Isolation

Planar device processing is thus very desirable as it avoids the issues resulting from the mesa structures, such as interconnect lines above mesa ridges and isolation of horizontal and vertical surfaces. Ion bombardment represents a very attractive technique: Ion implantation processes allow isolation [4.19] and planar area selective doping [4.108] at the same time. Implantation for isolation is used in several state-of-the-art industrial processes, e.g., [4.81].

Isolation by Implantation

Overview articles on implantation in wide bandgap semiconductors with focus on GaN are provided, e.g., in [4.82, 4.147, 4.201, 4.214]. Ion mass, ion energy, and implantation temperature are the critical parameters. Damage build-up

is to be reduced and post-implant annealing is to be reduced. H, He, and N implant isolation of n-type GaN is discussed in [4.19]. He-implantation leads to resistivities of $10^{10} \Omega \text{ cm}$ at room temperature. The temperature stability of the resistivity of the implanted structures up to $T_L = 300^\circ\text{C}$ is also mentioned. The implanted layers have a resistivity of $10^4 \Omega \text{ cm}$ at 300°C . Zn⁺ implantation for device isolation is reported in [4.193]. Similarly, highly resistive GaN layers formed by ion implantation of Zn along the C-axis are described in [4.199]. Zn implantation is performed at an ion energy of 350 keV and a dose concentration of $1.9 \times 10^{14} \text{ cm}^{-2}$ and leads to a Zn concentration between $10^{17}\text{--}10^{18} \text{ cm}^{-3}$. The isolation levels obtained in both GaN layers and AlGaN/GaN heterostructures reach $10^{11} \Omega \text{ sq}^{-1}$, while a thermal activation energy of 0.67 eV is found. The resistivity of the Zn layer even increases after RTA. A detailed analysis of the temperature-dependent implant damage during Ar⁺ implantation is given in [4.254]. The implantation is performed at an energy of 150 keV at a dose of $3 \times 10^{15} \text{ cm}^{-2}$ at temperatures between 0 and $1,000^\circ\text{C}$. The implantation damage has typically two peaks, one near the surface and one in the bulk material in a depth range of 100–200 nm. The impact of implantation and post implant-annealing on the optical properties of GaN is described in many publications, e.g., [4.147] for Zn implant in [4.234]. The typical findings yield a curing of the optical damage after RTA, while the damage cannot be fully removed. Early annealing studies of MOCVD- and MBE-grown material for various implants, including Ar, Mg, Si, Be, C, and O, are given in [4.229]. An overview on disorder and thermal and ion-beam-assisted annealing is given in [4.147]. The associated annealing is performed under flowing NH₃ or N₂ gas. The recovery of the bulk material is very similar under both NH₃ and N₂, while the latter provides better surface quality. The use of ion implantation for ohmic contact formation is described in the next section.

4.3 Contact Formation

The formation of metal–semiconductor interfaces or contacts defines a second critical process step for any electronic device. Both ohmic and Schottky contacts are of critical importance with respect to device functionality, performance, and long-term reliability. Good overviews of ohmic contacts to GaN are given, e.g., in [4.82]. A great variety of metal-systems have been proposed for the formation of low-contact resistances and high thermal and electrical stability, which are discussed in the following.

4.3.1 Ohmic Contacts

The formation of ohmic contacts requires the solution of a number of issues for III-N semiconductor devices, which are now summarized.

Issues of Ohmic Contact Formation

The issue include the following:

- The increase of the density of states at the interface for wide bandgap semiconductors with a bandgap of $\geq 3.4\text{ eV}$
- The pretreat of the sensitive semiconductor surface prior to metal deposition
- The control of the metal morphology due to the high annealing temperatures of at least 600°C [4.163] necessary due to the wide bandgap, including:
 - The control of the vertical diffusion of metal by high temperature annealing [4.50]
 - The control of the lateral diffusion of contact metals to avoid surface and gate leakage
 - The control of the morphology for e-beam or optical pattern recognition

Fig. 4.5 summarizes a number of geometrical situations for the ohmic contacts. The different contact situations can be systemized as follows:

- a. The metal is deposited on top of the barrier layer without annealing [4.289]
- b. The metal is annealed into the barrier layer
- c. The annealing is continued into the channel layer
- d. The metal is deposited on a highly-doped cap
- e. An ohmic recess is applied into the highly doped cap before annealing [4.128]
- f. The recess is additionally applied to the barrier layer before annealing

In general, the formation of ohmic contacts at a semiconductor surface requires a high density of states near the interface to push the Fermi-level in the semiconductor close to the conduction band. The wide bandgap of III-N semiconductors renders this more difficult, while the polar properties can be used to engineer beneficial high densities-of-states at the interface. This is accomplished by superlattice engineering in the cap layers for ohmic contact formation in [4.191]. Several investigations of the current transport in various metal and semiconductor materials and interfaces are available, e.g., for GaN in [4.82] and for InGaN and InN in [4.257]. In the case of as-deposited metal contacts, thermionic emission is the dominating transport mechanism. For annealed contacts to InN and InGaN, field emission is dominating [4.154]. The annealing procedures are intended to provide strong vertical material diffusion, while lateral diffusion has to be minimized even at the high annealing temperatures required. A comprehensive study of the annealing characteristics of the contacts in AlGaN/GaN HEMTs on s.i. SiC substrate is provided in [4.165]. Variations of the annealing temperatures between 800 and 830°C and of the metal stack are investigated. The contact resistances vary between 0.5 and $2\Omega\text{ mm}$. The metal stacks contain Ti (10 nm), Al (50–100 nm), Ni

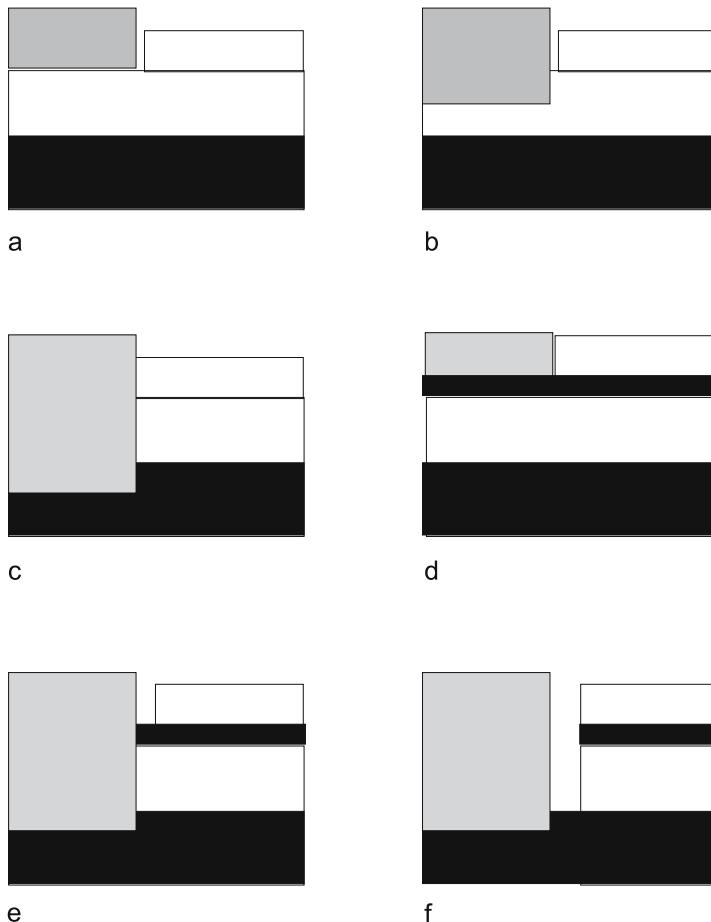


Fig. 4.5. Different ohmic contact situations

(20 nm), and Au (50 nm). The contacts covered by WSiN is found to be stable up to 400°C. For the analysis of the annealing procedure, Fig. 4.6 gives the measured contact resistance as a function of annealing temperature taken from [4.165] and others. Although the data given yields significant scattering, the general tendency of reduced contact resistances at higher temperatures is visible. At the same time, the morphology of the contacts deteriorates with increasing temperature. The annealing temperatures amount to up to 900°C, as reported, e.g., in [4.158, 4.252]. This results in very low contact resistances and leads potentially to problems with pattern recognition during e-beam lithography [4.274].

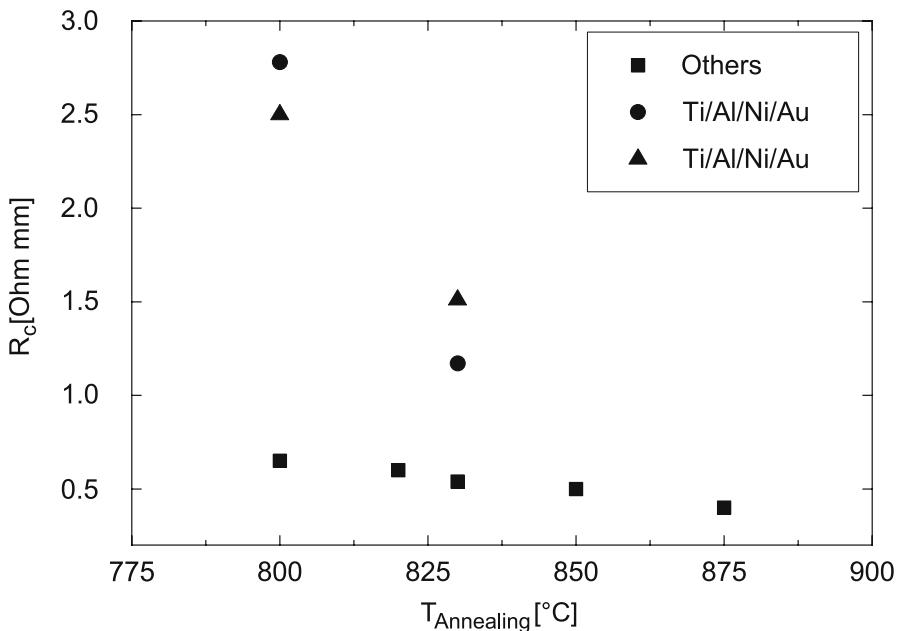


Fig. 4.6. Measured ohmic contact resistance as a function of published annealing temperatures from various publications

Ohmic Contact Material Systems

A large number of metal systems have been suggested for ohmic contact definition in the III-N semiconductor system. Table 4.1 gives an overview of metal systems and some details for both n- and p-type ohmic contact formation on GaN. The table further compiles annealing temperatures, applied impurity doping in the heterostructures, and resulting contact resistances. The table is based on annealing of metal sequences into the semiconductor layers without further measures, such as recesses, unless stated otherwise.

N-Type Ohmic Contacts

Early reports for ohmic contacts on n-type GaN are given in [4.162] using Ti/Al contacts alloyed at 900°C for 30 s. Improved ohmic contact stability is reported for Ti/Al/Pt/Au multilayer contacts to n-type GaN compared to Ti/Al/Au contacts [4.154]. The annealing temperature range is 750–950°C. Pt is used as a diffusion barrier for Au penetration. Ti/Al/Ni/Au contacts are suggested in [4.81] formed by rapid thermal annealing (RTA). They are used in the industrial processing of Nitronex and provide contact resistance of $0.75\Omega\text{cm}$. A more systematic comparison of several metals and materials systems is given in [4.209] for GaN/AlGaN/GaN heterostructures. The comparison is given for the metal systems on top of GaN cap layers. The

thermal stability of the contacts is compared for annealing temperatures up to 800°C and short-term annealing (typically 1 min). Afterwards, the devices are compared in long-term aging (200 h) at aging temperatures of up to 500°C. Ti/Al/Ni/Au multilayer ohmic contacts encapsulated by SiN are investigated in [4.137]. It is found that the composition of the SiN_x encapsulation layers critically affects the morphology of the contacts. This morphology, however, has great influence on edge definition, and thus on e-beam pattern mark recognition [4.137] during the subsequent lithography of the gates. The morphology of the contacts is especially important for processes with small margins, i.e., for small gate lengths and contact spacings [4.263]. The use of highly Al-doped-sputtered ZnO layers on top of AlGaN/GaN heterostructures provides a mediocre ohmic contact resistance of $2.7 \Omega \text{ mm}$ without any further contact annealing, as is reported in [4.197].

P-Type Ohmic Contacts

A very large number of publications exists for p-type ohmic contacts on GaN due to their importance for optoelectronic devices, e.g., [4.45, 4.226]. As the optoelectronic properties, such as optical transparency, do not play any role for electronic devices, the different metal contact systems are compared with respect to their electric properties. The comparison is given in the lower part of Table 4.1. Because of the intrinsic properties of GaN, the p-type ohmic contact resistances are typically two orders of magnitude higher than that for

Table 4.1. Ohmic contact materials and properties of ohmic contacts on GaN

Material	Ann. temp. (°C)	Doping (cm ⁻³)	Resistance ($\Omega \cdot \text{cm}^2$)/(Ωmm)	Ref.
Au	500	n	$10^{-1} \Omega \cdot \text{cm}^2$	[4.162]
Al	500	n	$10^{-1} \Omega \cdot \text{cm}^2$	[4.192]
Ti/Al	900	n	$8 \times 10^{-6} \Omega \cdot \text{cm}^2$	[4.192]
Ti/Al	850	n	$1.6 \times 10^{-4} \Omega \cdot \text{cm}^2 / 3.4 \Omega \text{ mm}$	[4.9]
Ti/Al/Au	750	n	$6 \times 10^{-6} \Omega \cdot \text{cm}^2$	[4.154]
Ti/Al/Pt/Au	850	n	$12 \times 10^{-6} \Omega \cdot \text{cm}^2$	[4.154]
Ti/Al/Ti/Au/WSiN	850/830	n	$0.5 \Omega \cdot \text{mm}$	[4.165, 4.166]
Ti/Al/Ti/Au	850	n	$0.6 \Omega \cdot \text{mm}$	[4.245]
Ti/Al/Ni/Au	830	n	$1.5 \Omega \cdot \text{mm}$	[4.165, 4.166]
Ti/Al/Ni/Au	n.a.	n	$0.75 \Omega \cdot \text{mm}$	[4.81]
Ni/Au	450	p	$1.7 \times 10^{-2} \Omega \cdot \text{cm}^2$	[4.226]
Ni/Au	600	p	$6.1 \times 10^{-4} \Omega \cdot \text{cm}^2$	[4.133]
Ni/Pd/Au	350–600	p	$1 \times 10^{-4} \Omega \cdot \text{cm}^2$	[4.45]
Ag (ZnO)	530	p	$5.5 \times 10^{-4} \Omega \cdot \text{cm}^2$	[4.11]
Pt/Re/Au	600	p	$1.4 \times 10^{-3} \Omega \cdot \text{cm}^2$	[4.210]

the best n-type contacts. Several overviews of the p-type ohmic contacts are available, due to their importance for laser and LED efficiency, e.g., in [4.189]. Ni/Au contacts on p-type GaN are proposed in [4.133, 4.226]. The annealing temperatures are 600 and 450°C. Contacts derived from this metal system using Ni/Pd/Au layer sequences are reported in [4.45] with low contact resistances. Contact resistances of $1 \times 10^{-4} \Omega \text{ cm}^2$ are reported on Mg-doped GaN. Record low values of $4.5 \times 10^{-6} \Omega \text{ cm}^2$ are claimed for heavily Be-doped GaN samples. Transparent Ag-based contacts are reported in [4.11] with contact resistances of $5 \times 10^{-4} \Omega \text{ cm}^2$. Several other multilayer metal systems have been investigated featuring, e.g., the use of Re in Pt/Re/Au contacts in [4.210]. The main electronic application of p-contacts are metal-stacks used for base contacts in npn-GaN HBTs [4.173, 4.175, 4.211, 4.224, 4.281]. Ni/Pt/Au metal stacks are used for dry-etched p-type ohmic contacts [4.211]. As-deposited metal stacks are found to be rectifying. Annealing at progressively higher temperatures improve the ohmic behavior. However, even at annealing temperatures of 800°C, the p-type contacts are not purely ohmic. Pd/Au layer stacks are applied for regrown base contacts on GaN in [4.175, 4.281]. Ni/Au is used in [4.224] for the formation of regrown contacts on p-Mg-doped GaN. GaN/InGaN DHBTs promise improved p-contacts [4.173]. In this case, Pd/Au layer stacks have been used for selectively p-regrown contacts. Al/Au metal stacks are used for the n-type contacts.

Ion Implantation for Doping

Implanted contacts form an interesting alternative to reduce contact resistances in the access regions, as reported, e.g., in [4.289]. References are simple planar contacts, high-temperature annealed contacts, or diffusion-based contacts, as reported, e.g., in [4.289].

Doping Implantation for N-Type Ohmic Contact Formation

The implantation introduces additional mask steps into the process flow [4.289]; however, it provides an area-selective definition of conducting semiconductor layers. Doping implantation further allows for efficient channel definition and contacts without the need for epitaxial changes. At the same time, implanted contacts require annealing steps with very high temperatures. Early reports of high-temperature annealing of GaN, AlN, and InN at temperatures of $\geq 1,000^\circ\text{C}$ are given in [4.101]. A powder technique is used to allow for surface protection and to provide N_2 partial pressure during the annealing. Ion implantation of silicon for n-type and magnesium for p-type doping and subsequent high temperature annealing steps of GaN are described, e.g., in [4.297]. The implantation in bulk GaN is performed at an implantation dose of $5 \times 10^{14} \text{ cm}^{-2}$ and energies of 180–250 keV using Si, Mg, or Mg^+ . The annealing temperatures after implantation range from 700 to 1,100°C. The activation of ion-implanted silicon in AlN/GaN epitaxial films by annealing is

discussed in [4.54]. The layers are implanted at an energy of 100 keV at a dose of $5 \times 10^{14} \text{ cm}^{-2}$. The electrical activation of the silicon amounts to 19%. The annealing temperature is 1,150°C in this case. The isolated silicon donor energy is found to be 15 meV, deduced from Hall-effect measurements. On the device level, the fabrication of GaN PIN-diodes by Si⁺ ion implantation is described in [4.108]. The electrical activation achieved amounts up to 25–30% at annealing temperatures between 1,150 and 1,200°C. The maximum annealing temperature for GaN layers grown by MBE is found to be approximately 800°C for GaN without impact on the structural properties, as reported in [4.296]. The yellow luminescence is significantly reduced after this annealing temperature. At even higher temperatures of up to 1,000°C, the structural decomposition of the material becomes visible. Thus, structural changes are to be expected for the material for the annealing temperatures proposed after implantation. A rapid thermal annealing procedure is described at very high annealing temperatures of up to 1,500°C for Si-doped GaN in [4.64]. The activation of Si implants is further discussed in [4.290]. The doses range between 5×10^{14} and $1.5 \times 10^{16} \text{ cm}^{-2}$ at energy levels of 100 keV. The resulting contact resistances of Ti/Al/Ni/Au contacts are as low as $0.02 \Omega \text{ mm}$ at doses of $5 \times 10^{15} \text{ cm}^{-2}$ and subsequent annealing. However, morphological changes have to be considered. The formation of n-type ohmic contacts in AlGaN/GaN HEMTs without any alloying is described in [4.289]. The ohmic contacts are formed by silicon implantation at 200°C with doses of $1.5 \times 10^{15} \text{ cm}^{-2}$ at energies of 30 and 60 keV. The Ni mask is removed after implantation and the sample surface is capped by AlN. The activation of the silicon is performed at 1,500°C with 100 bar overpressure for 1 min. Afterwards a conventional GaN HEMT process is applied. The resulting contact resistance amounts to $0.4 \Omega \text{ mm}$ measured in transmission-line measurement (TLM) structures. The morphology of the resulting contacts is greatly improved compared to conventional contacts with subsequent RTA. The formation of complete GaN junction FETs by ion implantation is described in [4.298]. N- and p-type doping is achieved by Ca- and Si-implantation followed by RTA at 1,150°C. No information is provided on the morphological changes.

Doping Implantation for Ohmic P-Type Contact Formation

P-doping of GaN is generally less efficient than n-doping. To resolve the low-effective activation of p-doping in GaN layers, several implantation studies have been performed. Mg-based doping with P-coimplantation for Mg is investigated in [4.297]. Electrical activation is achieved by RTA at temperature in excess of 1,000°C. The surface morphology is improved for both Ar and N₂ atmospheres. Effects of rapid thermal annealing (RTA) on beryllium implanted in-situ activated p-type GaN are described in [4.103]. The implantation is performed at an energy of 50 eV and a dose of 10^{14} cm^{-2} . Optimum RTA temperatures for the activation are found to be 1,100°C for 15 s. Multiple annealing steps are proposed to increase the effectiveness of Be-activation relative to single step annealing. No contact information is provided.

Regrown Ohmic Contacts

Apart from planar and implanted contacts, more complicated contact concepts and processes have been developed to address specific issues. Epitaxially regrown contacts can solve specific device issues, while they have the great disadvantage of loosing the natural sequence of epitaxial and subsequent technological process steps. Regrown contacts have particular advantages for the definition and protection of p-type contacts. A study to improve the current gain of AlGaN/GaN HBTs using a regrown emitter contact is given in [4.284]. The emitter contact is selectively regrown on the base layer, which is patterned by a dielectric mask. This technique is used to overcome the Mg-memory effect during MOCVD growth, which normally causes a displacement of the base-emitter junction. The technique is further useful to avoid etch damage of the base layer during processing. The etch damage is otherwise prohibitive, especially for the thin base layers necessary to increase the current gain in AlGaN/GaN HBTs [4.284]. A specific analysis of the p-n diodes in a comparison of regrown and conventional contacts is given in [4.282]. N-doped AlGaN layers are selectively regrown on the p-doped GaN surfaces. A Pd/Au metal sequence is deposited on the p-type GaN. Improved ideality factors and reverse leakage currents are obtained for the pn-diodes when growth pressure, growth temperature, and the semiconductor diode layer sequence are optimized compared to the as-grown p-type GaN. Regrown n-type contacts can also be used in FETs to reduce the access resistance. Self-aligned AlGaN/GaN HFETs with extrinsic transconductance values as high as 400 mS mm^{-1} are reported in [4.33]. They are based on a regrown ohmic contact concept for a gate length of $1.2 \mu\text{m}$. Source and drain GaN layers are grown selectively by MOCVD. A 170 nm thick Si-doped GaN layer doped at $1 \times 10^{18} \text{ cm}^{-3}$ is grown on the etched surfaces. A layer sequence of Ti (20 nm)/Al (200 nm)/Ni (40 nm)/Au (40 nm) is deposited and annealed at 830°C for 30 s. The resulting source resistances are $0.95 \Omega \text{ mm}$. AlN/GaN insulated gate heterostructure FETs with regrown n+ GaN ohmic contacts are reported in [4.122]. Four nanometer thick AlN is used as a gate insulator in this case. After selectively removing the AlN insulator, both source- and drain-contact n-type GaN layers are regrown on the GaN channel with a thickness of 150 nm. Ti/Al/Au contacts are deposited and annealed at 900°C at 30 s in N_2 atmosphere. The contact resistance achieved with the regrowth method is as low as $0.22 \Omega \text{ mm}$.

4.3.2 Schottky Contacts

Metal–semiconductor Schottky contacts are the most critical elements in all those FETs that do not have a metal–oxide contact. Schottky-contact properties define charge control [4.238] and the hot spots of the electric fields in the gate region, as depicted in Fig. 4.7. This figure gives the simulated distribution of the electric field under the gate contact in an AlGaN/GaN HEMT, in this case with a gate length $l_g = 600 \text{ nm}$. It can be seen that the field gradients

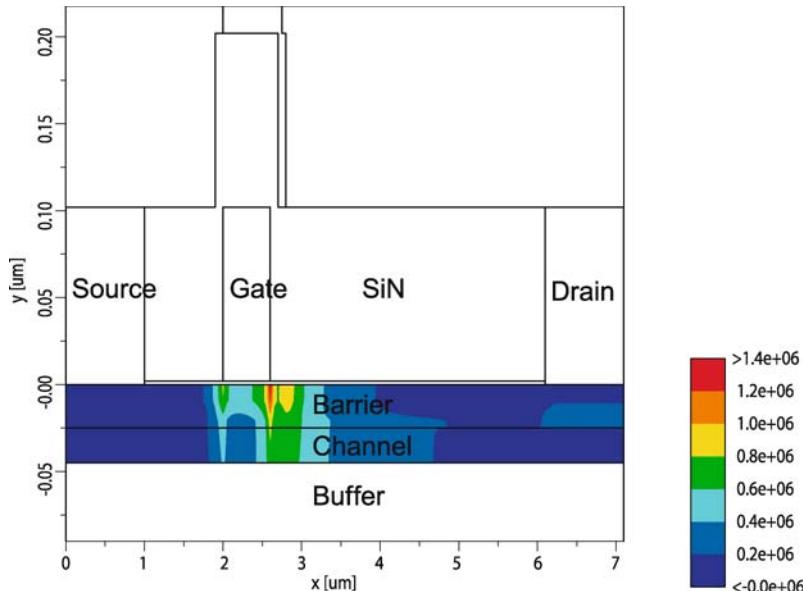


Fig. 4.7. Simulated field distribution in V/cm in an AlGaN/GaN HFET at $V_{DS} = 60$ V

are located at the drain side end of the gate, and so a very precise gate definition is fundamental for FETs. Direct measurement of gate depletion regions has been reported. High breakdown voltages of up to 405 V in AlGaN/GaN HFETs with simple Schottky contacts have been measured, as reported, e.g., in [4.261]. A fourth terminal is applied to the device that can be individually monitored. From this analysis the distribution of the depletion zone can be directly measured. It is found that the extension of depletion zone strongly varies with the voltage, which mitigates field peaking. It can be deduced from this analysis and from Fig. 4.7 that the impact of the surface is critical to the analysis. In a Schottky contact the forward current through a diode is considered ideal when $n = 1$, as given in (4.1) [4.78]. Nearly ideal Schottky contacts with low ideality factors n , as defined in (4.1), avoid early gain compression in FET power devices. The gate current is modeled:

$$I_G = I_0 \cdot \exp \left(\frac{q \cdot (V - I \cdot R_S)}{n \cdot k_B \cdot T_L} \right). \quad (4.1)$$

R_S denotes the series resistance of the diode and n the (non)-ideality. GaN FETs initially suffer from relatively high ideality factors n [4.114] due to various issues:

- High surface roughness affecting the morphology of the semiconductor–metal interface

- Isolation problems along the top semiconductor-passivation interface without the application of a gate or ohmic recess
- High drain-current levels through high (polarization and impurity) doping
- Nonohmic behavior of the access regions during the Schottky diode measurement

These issues are partly independent of the actual Schottky contact metal layer design and will be discussed further. The technological issues of the contact formation, however, include the following:

- The reduction of leakage currents at high-voltage operation of up to 300 V
- Stability with respect to high operation temperatures [4.110]
- The effects due to the formation of a Schottky gate on a polar semiconductor (Ga-face, N-face polarity) [4.219]
- Trapping behavior and dipole formation near the interface [4.219]
- Adhesion issues of the gate contacts on relatively rough interfaces
- The mechanical stability of the gates, e.g., with respect to the backside treatment of very hard substrate materials

Typically, the currents in a diode are modeled by a thermionic emission model:

$$I_G = A \cdot T_L^2 \cdot \exp\left(\frac{-q \cdot \phi_B}{k_B \cdot T_L}\right) \exp\left(\frac{qV}{n \cdot k_B \cdot T_L}\right). \quad (4.2)$$

Tunneling introduces an additional mechanism, as described in various publications, e.g., in [4.83]. The tunneling probability $T(E)$ is modeled in one dimension according to

$$T(E_x) = \exp\left[-2 \frac{\sqrt{2m^*}}{\hbar} \int_{x_1}^{x_2} \sqrt{\phi(x) - E_x} dx\right]. \quad (4.3)$$

Detailed leakage mechanisms at GaN- and AlGaN-Schottky interfaces are described in [4.83]. Temperature-dependent measurements between 200 and 300 K allow a separation of tunneling and thermionic effects in (4.2) and (4.3). Effective barrier thinning through unintentional surface-defect donors is found to enhance the Schottky-barrier tunneling in AlGaN/GaN HFETs and leads to increased leakage currents. The origins of leaky characteristics of Schottky diodes on p-doped GaN are discussed in [4.291]. The Mg concentration amounts to $5 \times 10^{19} \text{ cm}^{-3}$ near the interface. Au/Ni is used as metal stack. The defective surface region is considered critical for the formation of either Schottky or ohmic contacts for the same metal system. The physical background of the tunneling is the trap distribution near the interface, which enhances or suppresses the tunneling component. The influence of rapid thermal annealing on Ni/Pt/Au Schottky gates on n-doped AlGaN is described in [4.183]. Pt diffusion after annealing at the temperature of 600°C leads to improved Schottky barrier height.

Ti/Ni/Pt/Au gates do not show any significant change after a similar annealing treatment, since interfacial Ti serves as a diffusion barrier. Ni is found to be crucial for the formation of a stable Schottky interface. Similarly, the impact of thermal annealing on AlGaN/Ni (3 nm)/Pt (30 nm)/Au (300 nm) Schottky diodes is investigated in [4.193]. The leakage current is significantly reduced after RTA. Two reasons are considered. One explanation is the Pt diffusion to the AlGaN layer, the second explanation is the reaction of Ni with the AlGaN surface, which reduces the surface trap density.

Very high operating temperatures are considered when Ir Schottky contacts are annealed at 500°C in O₂ ambient for 24 h [4.110]. The devices are found to be stable with respect to this temperature treatment. Thermal oxidation of diffused Ga is considered to improve the Schottky barrier ϕ_B in this case. A very high degradation temperature of 700°C is found for W and WSiN refractory contacts to n-GaN in [4.228]. Nb contacts degrade at a temperature of 300°C. However, in general, the refractory gates to GaN are found to be more leaky than those to GaAs. Surface roughness of the semiconductor layers remains an issue, especially with regard to small-gate-length devices with a gate length below 300 nm. Roughness is a serious reliability issue as reported in [4.70]. An increase of the medium scale roughness is based on the cracking of the degraded AlGaN films. The local strain of AlGaN relaxes. Gate adhesion is further a major issue for the realization of the gates [4.9, 4.75]. No adhesion problems have been found for both Ni/Au- and Cu-gates, as reported in [4.9]. Pure Pt gates are considered to suffer from adhesion problems on GaN and AlGaN [4.75]. Other noble metals such as Au present similar problems [4.12].

The exposure of the gates to mechanical stress is another important issue. Additional metals on top of the gate heads introduces additional stress. Such nonuniform mechanical stress is evaluated by simulation in [4.25]. The III-N nitrides are found to be stiff, and the highest impact of stressed gate heads occurs for strongly strain-relaxed AlGaN. Further, during backside processing [4.255], the FETs devices are subject to the stress induced by substrate thinning and thermal exposure due to viahole etching adjacent to the gates. Experimental investigations regarding the mechanical stability are currently rare.

Metal Stacks for Schottky Contacts

Various metal systems have been proposed for use in Schottky contacts on III-N semiconductors. The pretreatment of the semiconductor is discussed below. Overview articles on metal stacks are found, e.g., in [4.163]. Table 4.2 compiles the most important characteristics of a large number of metals and metal systems. The Schottky barrier ϕ_B , the doping of the semiconductor, and the extracted ideality factors n are given. Out of the selection in Table 4.2, several options have been eliminated for state-of-the-art technologies. Ni/Au

Table 4.2. Schottky barriers and ideality factors on various semiconductor materials

Material	Schottky barrier $q \cdot \phi_B$ (eV)	Doping (cm $^{-3}$)	Ideality (-)	Ref.
Au	1.32	4×10^{17} /n-GaN	1.24	[4.269]
Au	0.84–0.94	n-GaN	1.03	[4.78]
Cu	1.15	n-GaN	1.04	[4.9]
Ir	0.9–1.1	n-GaN	–	[4.110, 4.111, 4.113]
Mo	0.81–1.02	n-GaN	1.04–1.29	[4.208]
Nb	0.63	n-GaN	1.5	[4.228]
Ni	1.26	n-Al _{0.15} Ga _{0.85} N	–	[4.292]
Ni	0.71	n-Al _{0.21} Ga _{0.79} N	–	[4.113]
Ni/Au	0.97	n-GaN	1.05	[4.9]
Ni/Pt/Au	0.82	n-GaN	2.1	[4.193]
Pd	1.13	Al _{0.21} Ga _{0.79} N	–	[4.113]
Pt	1.1	2×10^{17} /n-GaN	–	[4.238]
Pt/Ti/Au	–	n-GaN	–	[4.166]
Re	0.82	1.5×10^{17} /n-GaN	1.1	[4.258]
Ru	1.1	–	–	[4.111]
Ti	0.58	4×10^{17} /n-GaN	–	[4.18]
Ti	1	n-Al _{0.15} Ga _{0.85} N	–	[4.292]
W	0.63	n-Al _{0.21} Ga _{0.79} N	–	[4.113, 4.228]
WSi	0.58	n-Al _{0.21} Ga _{0.79} N	–	[4.113]
WSiN	Leaky	1×10^{17} /n-GaN	–	[4.228]
Ni	2.0	p-GaN	–	[4.163]
Nb	Leaky	p-GaN	–	[4.228]
WSiN	0.8	p-GaN	–	[4.228]

is a favorite system in use. As a general trend, the Schottky barriers on AlGaN are higher than those on GaN. Nitronex reported the use of Ni/Au in [4.114]. Cree has also mentioned the use of Ni/Au in [4.275, 4.277]. Fujitsu/Eudyna and NEC [4.8] have reported on the use of Ni/Au in [4.118] for both HEMTs and MIS-HEMTs. RFMD also reported the use of Ni/Au in [4.221, 4.222]. Triquint reported the use of Pt/Au for high-power e-beam defined field-plate gates in [4.53, 4.153]. Other gate-stack options, such as Ir or W may be useful especially for high-temperature operation.

Cleaning and Pretreatment of the Gated Surface

Surface cleaning prior to metal deposition plays an important role for the yield and the homogeneity of the process, e.g., [4.114]. After opening the protecting SiN passivation layers [4.114] or resist layers prior to gate deposition, the

remainders on the semiconductor surface have to be fully removed to increase process robustness. At the same time, etch-damage has to be avoided. Opening the SiN dielectric involves plasma dry etching, as proposed, e.g., in [4.245]. This procedure has to be optimized for low-semiconductor damage, as performed in [4.114]. ICP-RIE is used for this procedure, as plasma density and ion energy can be effectively decoupled and damage can be reduced. Thus, sufficient etch rates can be achieved without the use of high DC-substrate bias.

Resist and oxide removal is another critical step before gate formation. A wet NH₄OH treatment in 1:10 volume is applied in [4.183] to remove native oxides. A similar oxygen plasma followed by a 1:10 NH₄OH/H₂O treatment for 15 s is suggested in [4.238]. An O₂-plasma-ashing in combination with diluted HCl:H₂O (ratio 1:1) treatment is used in [4.9] for the same purpose. The same HCl treatment is mentioned in [4.258]. Surface oxide removal by aqua regia (HNO₃:HCl=1:3) is suggested in [4.208]. The impact of a short HCl dip prior to gate–metal deposition is studied in [4.141]. A trade-off is found achieving either low-leakage and stronger current collapse or increased leakage and negligible current collapse. The trade-off is attributed to the existence of a thin interfacial oxide layer under the gate, which is partly or fully removed by the HCl etch. Residual oxide leads to reduced leakage but increased dispersion in the general trade-off between leakage and dispersion. The design of the gate head is discussed in the following section.

Device Annealing

Rapid thermal annealing is a crucial procedure for the formation of ohmic contacts, as has already been reported. Further, annealing can be instrumental in removing the etch damage, e.g., [4.204]. In addition, annealing can be effectively used to stabilize devices during or after processing with respect to long-term reliability [4.99]. A study of the post-annealing effects on the AlGaN/GaN HEMT performance after gate formation is given in [4.130]. The annealing is performed at 400°C for 10 min in N₂ atmosphere. The annealing is reported to reduce the number of surface defects with a time constant of $\leq 10\text{ }\mu\text{s}$, resulting in a reduction of low-frequency dispersion observed by pulsed-DC-measurements with different time constants. Further annealing leads to the creation of traps with a time constant of $\geq 10\text{ }\mu\text{s}$. Furthermore, the annealing of gate contacts has a large impact on the threshold voltage, as reported, e.g., in [4.59]. A device annealing is performed at 500°C and leads to a substantial change of the barrier height and the leakage currents. Similarly, gate annealing procedures have been developed to stabilize the gate process. Gate annealing in nitrogen atmosphere at 600°C for 5 min is reported in [4.193].

Gas Sensitivity

Any metal–semiconductor contact has a sensitivity to gases present at the metal–semiconductor interfaces. This sensitivity is based on the adsorption of

the gases and the resulting modification of the space charge zone under the gate. This can possibly be exploited at extremely high operating temperatures $\geq 300^\circ\text{C}$ due to the WBG properties of III-N semiconductors.

The hydrogen response of Pt-GaN Schottky diodes is investigated in [4.219] and in [4.132]. Hydrogen is found to dissociate on the Pt surface forming atomic hydrogen, which modifies the effective barrier height. Similar investigations of the hydrogen sensitivity of Pd/GaN diodes are reported in [4.271] and in [4.132]. The forward and reverse currents are significantly changed by the Schottky barrier reduction in the presence of hydrogen. The devices can be operated up to temperatures of 473 K. The changes of the effective Schottky barrier height in an atmosphere with 10% H₂ are typically in the order of 50 meV. Hydrogen-induced reversible changes in the drain current of Sc₂O₃/AlGaN/GaN MOS-HEMTs are discussed in [4.119]. The gas-induced effect is based on the dissociation of the molecular hydrogen at the Pt contact, followed by the diffusion of the atomic hydrogen to the oxide/semiconductor (Sc₂O₃/AlGaN) interfaces, where the channel charge is modified, as already mentioned above.

4.4 Lithography

Lithography is a fundamental processing step for any semiconductor device. Optical lithography has been reported on for the formation of ohmic and gate contacts and further layers of III-N devices in [4.98, 4.166, 4.223]. Electron-beam gate lithography [4.263] has been used in the III-N material system for the gate formation of GaN FETs with gate lengths $\leq 300\text{ nm}$. Minimum physical gate lengths $l_g = 30\text{ nm}$ have been reported [4.93]. Even direct contact lithography is still used, mainly for contact definition, especially for 2-in. substrate diameter technologies, e.g., in combination with electron lithography [4.16, 4.126].

4.4.1 Optical Lithography

Optical stepper lithography provides parallel illumination of the wafer and thus provides a fast and thus cost effective lithography for mass production [4.61]. With the development in the silicon VLSI industry, optical gates down to physical lengths of 25 nm are being realized with UV [4.106, 4.187] and potentially with EUV optical stepper technology [4.232]. In the III-V semiconductor industry, the optical steppers used are typically i-line type and are based on 248 nm wavelength technology [4.61, 4.114]. Gate lengths down to at least 250 nm are typically realized, and the gate length can be decreased even to 150 nm, when phase shift masks are applied, e.g., [4.164]. The gate definition of GaAs and GaN FETs can be subdivided into the fundamental steps [4.61, 4.114]:

- Gate stem or trunk definition
- Opening of the dielectric [4.114]
- Resist removal
- Metal evaporation [4.114]
- Patterning of the gate head
- Gate head metal evaporation
- Gate head lift-off

The order of these steps can partly be changed and steps can be omitted based on the different processes, such as simple stem-gate, T-gate, or SiN-assisted gate.

For III-V semiconductors, Triquint announced an improved fabrication process-based on a dielectrically defined quarter micron optical T-gate for high-power GaAs PHEMTs, as reported in [4.61]. The improvement in power density in GaAs up to 2 W mm^{-1} at 10 GHz is attributed to reduced surface state density. A similar process has been reported for GaN FETs in [4.114]. This process enables early passivation of the semiconductor and thus protection of the semiconductor layers. The gate stem is defined by ICP etching of the SiN. A low-damage etch recipe is applied to provide accurate pattern transfer and critical dimension control. The absolute resolution of the i-line steppers typically used for III-V semiconductors amounts to at least 330 nm [4.61, 4.164]. Phase-shift mask can be used to reduce the gate length for optically-defined devices to $0.15\text{ }\mu\text{m}$, e.g., [4.239]. For GaN and related semiconductors, optical lithography on optically transparent substrates such as SiC or sapphire increases the complexity and raises several additional issues. These include the following:

- Reliable mark/pattern recognition of the optical stepper due to substrate transparency [4.98, 4.137]
- Increased surface roughness imposing problems with frontside/backside resolution [4.137]
- Radius-dependent angle illumination through wafer bowing

The increased accuracy of steppers relative to the direct contact lithography is necessary for gate and recess definition with positioning accuracies better than 100 nm. This is critical if the distances between the contacts are reduced to $\leq 500\text{ nm}$ for high-speed operation.

4.4.2 Electron Beam Lithography

Electron beam processes provide increased resolution and positioning accuracy for the definition of gates. Devices with gate lengths down to 30 nm have been reported for the III-N system [4.91, 4.93]. The absolute and relative accuracy of e-beam lithography amounts to a few nanometer, allowing for the gate definition of 14 nm gate in VLSI [4.123]. At the same time, the big disadvantage of electron-beam technology is the linear illumination of the reticle, which is

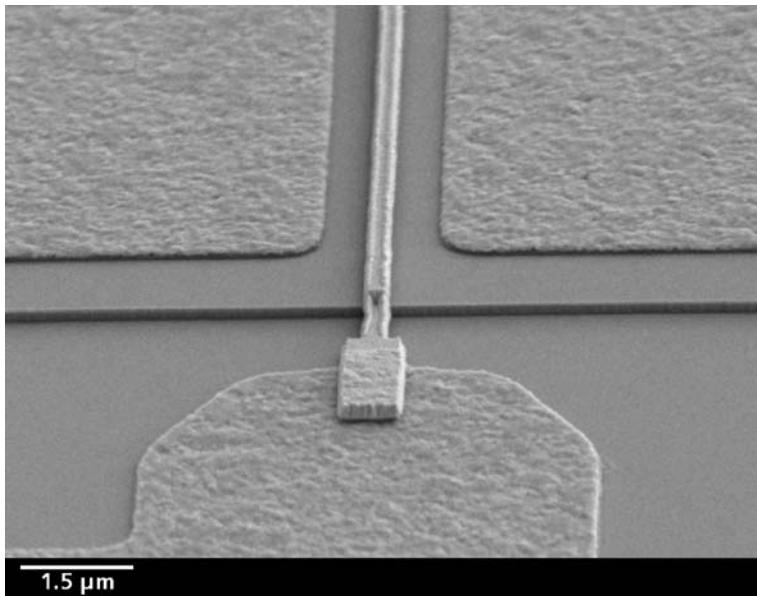


Fig. 4.8. SEM image of an e-beam T-gate with a gate length $l_g = 150$ nm

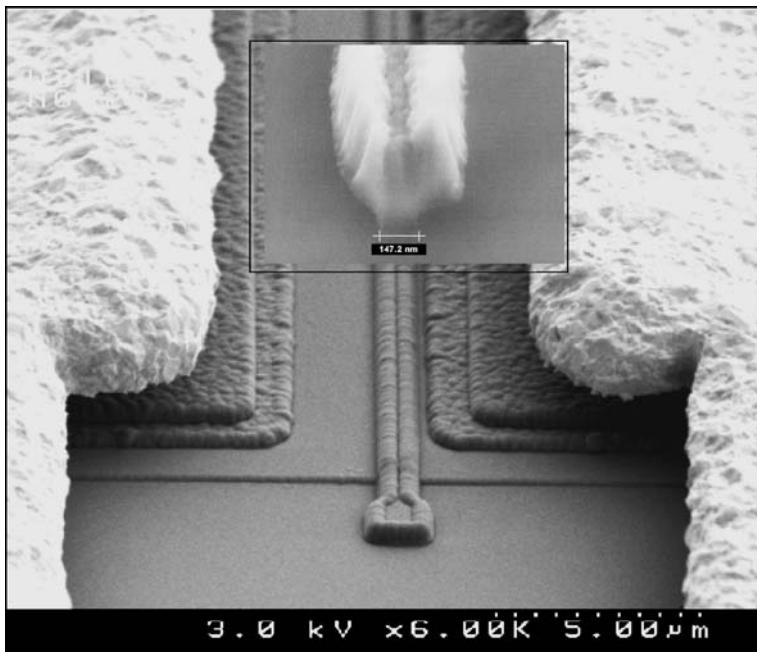


Fig. 4.9. SEM image of an e-beam T-gate with a gate length $l_g = 150$ nm including galvanic metal, smaller image: SEM image of an e-beam gate with a gate length $l_g = 150$ nm at higher resolution

time consuming. The double and triple-layer [4.113, 4.150] resist systems such as PMMA used for III-N devices are very similar to those developed for GaAs, e.g., [4.121]. A trilayer PMMA/P(MMAMAA)/PMMA resist is used for the definition of 120 nm gate in [4.150]. Mushroom-gate [4.126] and Γ -shaped gate structures [4.148] have been reported. Fig. 4.8 gives the SEM image of an e-beam gate of an AlGaN/GaN HFET with a gate length $l_g = 150$ nm. The good morphology and edge quality of the ohmic contacts is vital for the pattern recognition and positioning accuracy during the gate processing. Fig. 4.9 gives a similar image including the galvanic-metal layer. The contact spacing is asymmetric in this case. The T-shaped structure is visible on top of the gate stem in the enlargement in Fig. 4.9.

4.4.3 Field Plates and Gate Extensions

Conventional metal–semiconductor gate contacts provide a potential weak-point for III-N devices. Devices with conventional gates do not exploit the full basic breakdown properties of wide bandgap semiconductors, as the highly uniform field distribution provides early breakdown. For this reason gate contact designs have been modified to enhance breakdown voltages by the use of gate extensions [4.237, 4.245], single field plates, [4.120, 4.294], and multiple field plates [4.283]. An example is given below in Fig. 4.13. Figures 4.10 and 4.11 show various concepts of the field plate and the naming convention of the geometry. The field plate can either be realized as an additional metal layer on top of the SiN layer covering the conventional gate stack, as depicted in Fig. 4.10 [4.279]. In the second concept the field plate can be directly integrated in the conventional gate stack, as shown in Fig. 4.11. In addition, a second source-terminated field plate or shield structure can be added [4.243, 4.245]. The most important parameter apart from the gate length l_g and the contact separations between source, gate, and drain are the length of the field plates, electrically connected either to the source, or the gate. The respective lengths, l_{fps} and l_{fpd} , are depicted in both Fig. 4.10 and Fig. 4.11. Further, the vertical height of the field plates above the semiconductor have a strong impact on the field distribution in the barrier and channel. Several simulation studies are available for the optimization of the geometry [4.120, 4.218], see also Fig. 4.13. The geometry of the field plate, i.e., the length l_{fpd} is varied and the resulting field distribution along the channel is visible. As a rule of thumb, the field plate length has to match the gate length, e.g., [4.280]. An exception is given for a very small gate length of 100 nm where the gate extension is longer, e.g., 360 nm, as reported in [4.237].

State-of-the-Art

The field-plate concept is widely used for silicon LDMOS [4.26] and GaAs HEMTs, e.g., for base station applications, as cited in [4.264]. The concept yields improvements in both power density and V_{DS} voltages [4.280]

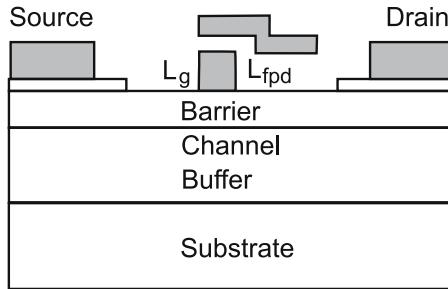


Fig. 4.10. Gate field plate and geometry (source- or gate-terminated) (type A)

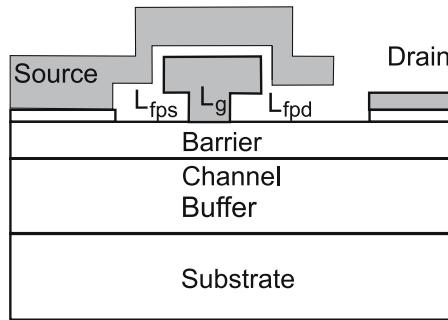


Fig. 4.11. Gate extension in combination with a source-terminated field plate (type B)

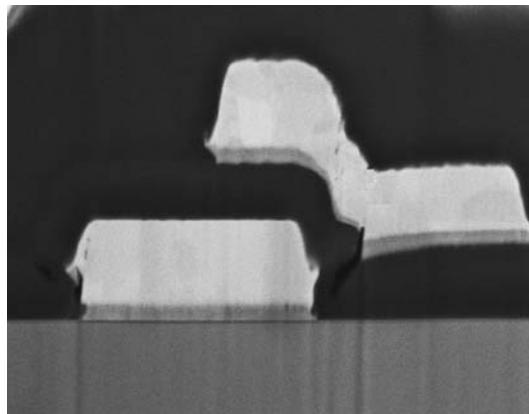


Fig. 4.12. SEM image of a gate with a gate length $l_g = 900 \text{ nm}$, including a field plate of type A

for all semiconductors. Further improvements discussed include device linearity [4.38] and device compression behavior, especially for GaN. Fig. 4.12 gives an SEM image of a gate structure with gate length $l_g = 900 \text{ nm}$, including

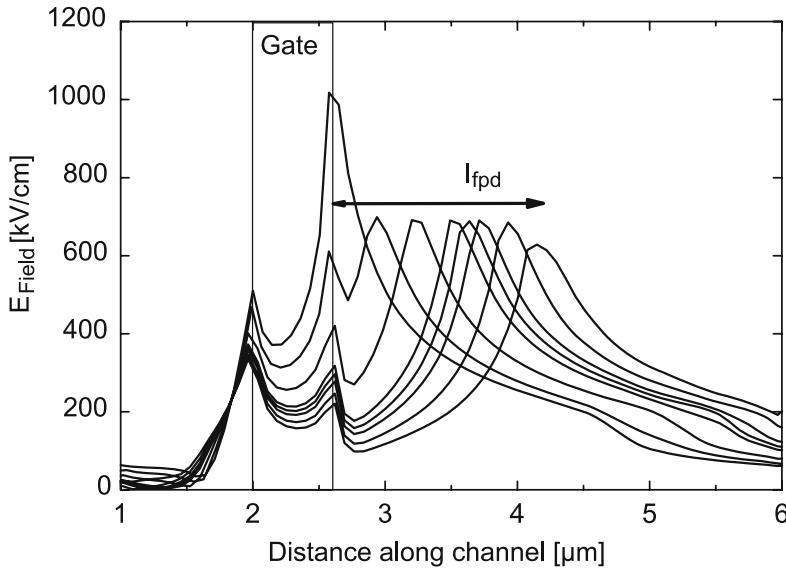


Fig. 4.13. Simulated field distribution along the channel of a conventional FET ($l_g = 600 \text{ nm}$, $l_{fps} = 0$) as compared to a field-plated FET of various lengths l_{fpd} at $V_{DS} = 60 \text{ V}$

a field plate of type A of Fig. 4.10. Initial reports on the enhancement of the breakdown voltage through a field plate in AlGaN/GaN FETs are given in [4.294]. The overlapping gate structure is defined into a 150 nm thick SiN layer. The drain-side overlap of the gate l_{fpd} is $0.3 \mu\text{m}$. Ando et al. reach output power densities $P_{sat} = 12 \text{ W mm}^{-1}$ at 2 GHz on s.i. SiC substrate using gate-recessed devices and field plates [4.5, 4.7]. The maximum V_{DS} operation voltage is 66 V. GaN HEMTs with a gate length $l_g = 1 \mu\text{m}$ use gate extensions between 0.3 – $2 \mu\text{m}$. The process is combined with a gate recess with an etch depth of 14 nm. The maximum two-terminal gate-drain breakdown voltage achieved is 200 V at $l_{fpd} = 1 \mu\text{m}$. World records for RF-output power densities as high as 32 and 40 W mm^{-1} are reached with field-plated devices through optimization in [4.278, 4.279]. The length of the field late is varied between 0 and $1.1 \mu\text{m}$. A typical increase of the gate capacitance of the field plate of 10–15% is considered as a guideline. The field plate consists of a layer stack of 10 nm Ti and 500 nm Au. Power and linearity characteristics of field-plated recessed-gate AlGaN/GaN HEMTs are reported in [4.38]. Devices with a gate length $l_g = 0.6 \mu\text{m}$ use a gate-recess etch-depth of 12 nm and a 100 nm thick SiN nitride. Although limited by thermal issues, sapphire substrates can be used for the development of field plates to achieve output power densities $P_{sat} = 12 \text{ W mm}^{-1}$ at $V_{DS} = 50 \text{ V}$ in [4.37]. The SiN thickness is 70 nm in this case for devices with a gate length $l_g = 0.7 \mu\text{m}$. The length of the field plate is $l_{fpd} = 0.7 \mu\text{m}$. Conventional gate structures with multiple field plates of type A

for power switches with high breakdown voltages are described in [4.283]. The additional degree of freedom with multiple field plates is used to further reduce the field peaking for gate-to-drain spacings of up to $24\text{ }\mu\text{m}$ for an AlGaN/GaN HFET with a gate length $l_g = 1.5\text{ }\mu\text{m}$. The nitride thickness is 180 nm. The length of the field plates is $l_{\text{fpd}} = 0.5\text{--}0.7\text{ }\mu\text{m}$ for the first field plate and additional $0.5\text{--}0.7\text{ }\mu\text{m}$ for the second field plate. The maximum breakdown voltages claimed in [4.283] reach 900 V. The device with no field plate yields 250 V, the device with one field plate 650 V. The field plates in [4.283] are completely connected to the gate. However, this electrical connection or termination leaves an additional degree of freedom, as discussed later. Again for power-switching and power-supply electronics, field-plated AlGaN/GaN HFETs with breakdown voltages beyond 600 V have been reported, e.g., in [4.218]. In this case, the gate is a conventional metal stack and a source-terminated field plate is used, as depicted in the left part of Fig. 4.11. The gate length is $l_g = 1.5\text{ }\mu\text{m}$. The passivation is a combination of 360 nm SiN, followed by 600 nm of SiO₂. The study is continued with the application of the same overlapping structure from the drain contact. The additional drain field plate allows the reduction of the field peak at the drain edge of the ohmic contact without further increase of the GaN layer thickness. A very simple slant field plate for power applications is suggested in [4.51]. The gate can be realized in one lithography step with a self-aligned integrated field plate. Breakdown voltages $\geq 1,000\text{ V}$ are obtained, which otherwise require multiple field plates with complicated multiple lithography steps.

The additional capacitance introduced with field plates needs consideration. Switching speed capabilities of field-plated AlGaN/GaN HEMTs up to 100 MHz are reported in [4.52]. In this case, three field plates are introduced. The gate length is $2\text{ }\mu\text{m}$ and the shift of the field plate extension is $0.6\text{ }\mu\text{m}$ for each field plate. The devices provide a breakdown voltage of 550 V. AlGaN/GaN MOS-HFETs including a field plate are reported in [4.2]. The gates with a gate length of $1.2\text{ }\mu\text{m}$ are deposited on a 16 nm thick SiO₂ layer deposited by PECVD. The overhang of the field plate (type A) is $1\text{ }\mu\text{m}$. The devices are covered with a leaky SiN dielectric. Operation voltages of $V_{\text{DS}} = 55\text{ V}$ are reported with this concept. Recent reports on innovative combinations of source and gate connected field plates are presented in [4.8] and [4.243]. The gate extension concept (type B) is combined with a source-terminated field plate. The devices are similar to those depicted in Fig. 4.11. The interlayer thickness of the SiN is 490 nm, which determines the separation of the two field plates. Output power densities up to 10 W mm^{-1} at 2.14 GHz for large-periphery devices are reached in pulsed-operation [4.38]. For operation frequencies of 10 GHz, gate extensions can also be used for smaller gate length of $0.35\text{ }\mu\text{m}$, see [4.245]. A drain-side extension of $0.18\text{ }\mu\text{m}$ is used for an SiN thickness of 40 nm. This leads to output power density of 16.5 W mm^{-1} and 47% PAE at $V_{\text{DS}} = 60\text{ V}$ for $W_g = 150\text{ }\mu\text{m}$. The improvements of the gate extension are especially visible at $V_{\text{DS}} \geq 25\text{ V}$.

Design Considerations and Trade-Offs

The major advantage of field-plated- and gate extension-HEMTs is the reduction of the electric field peaking, as depicted in Fig. 4.13 in comparison to a conventional FET without any field plate. The high gradients in carrier concentration near the gate lead to very strong field peaking. Further, the field plate leads to the depletion of the interface between semiconductor and the passivation layer. This is true for both the source and drain side of the gate contact. The application of the field plate thus leads to reduced dispersion, better pinch-off, improvement in device reliability, and to an increase of the effective gate length. The two typical situations for field plate designs in Fig. 4.10 and Fig. 4.11 shall be discussed in more detail. The first design (type A) is an additional metal on top of the gate contact separated from the gate by an additional dielectric layer. This requires additional processing steps in addition to the gate head formation. The potential of the field plate is either gate or source-connected (not visible). An independent fourth potential for the device is typically not considered. The approach requires the precise definition of the gate head, as the real geometry of the field plate is dependent in the shape of the gate head. The second design (type B) is given in Fig. 4.11. The approach combines a gate extension with a second field plate connected to the source contact. The gate-terminated field plate with the extension is easy to process and does not require additional process steps. Fig. 4.13 shows the enormous potential for the reduction of the maximum electrical field at $V_{DS} = 60$ V for a gate-terminated field plate of type A. The simulation shows a significant reduction of the electric field along the channel. Multiple field-plate designs of type B, as given in Fig. 4.11, can further reduce the field peaking. However, these advantages have to be carefully traded off against several technological issues and performance reductions, either related to gain, RF-bandwidth, and manufacturability. These include the following:

- The possible increase of the gate resistance R_G [4.168]
- The introduction of additional parasitic capacitances at source, gate, and drain [4.276]
- The introduction of additional processing steps and related processing uncertainty [4.37, 4.279]
- Additional reliability issues at the metal/insulator and semiconductor/insulator interfaces, e.g., due to the additional strain imposed by the metal layers

The possible increase of the gate resistance is an obvious effect. It is based on the effective decrease of the gate cross-section in some of the field-plate concepts, especially of type A, and the increase of the line resistance of the gate. A novel gate feed technology to reduce the gate resistance has been presented in [4.168]. Additional feeder structures are introduced for better connection of the gate finger, especially for very long gate fingers. Gate-connected field plates further lead to an additional contribution of gate-to-source capacitance

C_{gs} and gate-to-drain capacitance C_{gd} and thus lead to a reduction f_{max} , and thus of the power gain [4.280]. The effect of the C_{gd} increase is typically dominating. Source-connected field plates, however, increase the source-to-drain capacitance C_{ds} [4.276]. The trade-off for the optimization of the field plates includes reducing the field peaking to enhance breakdown, while preserving a good power gain and keeping the additional capacitive contributions low. These capacitive contributions can be understood from another point of view. The gate-terminated field plate has the effect of a partial increase of the gate length. As shown in Fig. 4.10, once the vertical heights are reduced to zero, the field plate is nothing else than an extension of the gate length l_g . For the source-terminated field plate, the effect on the capacitances is different. The gain parameters, represented, e.g., by the MAG/MSG or f_{max} , are not primarily affected. However, the source-to-drain capacitance C_{ds} is increased by a parasitic contribution [4.276], which has a strong impact on the output matching of the devices. As will be explained in Chapter 6, the capacitance C_{ds} has a limiting effect on both bandwidth and input/output matching. Thus, the parasitic contribution through the source-terminated field plate is critical, especially for broadband applications. The additional processing effort is obvious; however, it can be reduced, as the sole application of a gate extension does not involve additional lithography. Field plates as shown in Fig. 4.10 provide additional mask layers on the SiN, while the multiple field-plate approach involves further additional mask steps. For very small gate length of 100 nm [4.2], the definition of the field plate requires a second e-beam step for the definition of the gate head. The additional metallization layers further involve additional reliability issues. In the case of a source-terminated field plate, the full V_{DS} voltage drops between the field plate and the drain ohmic contact. As the optimized dielectric layers are typically very thin (100 nm), the maximum voltage of up to 200 V drops over this distance. However, the overall advantages dominate and successful realization of various field-plate concepts will make this approach a standard technology module for III-N FETs.

4.5 Etching and Recess Processes

The etching of semiconductors is a crucial step in semiconductor processing [4.172]. The generation of nonplanar structures is a basic need during the formation of semiconductor devices. Mesa etching was already described in Sect. 4.2.1. Controlled removal of material and etch-damage-control in critical device regions are important for the development of reproducible semiconductor process technologies. The tight crystalline bond strengths in GaN and other III-N semiconductors lead to the wide bandgap, but also make these semiconductors chemically inert and difficult to etch. This is especially true with respect to the polar nature of these semiconductors, where even very mild etching conditions can modify the surface charge densities significantly,

e.g., [4.56]. The criteria for the evaluation of etching processes are enumerated and discussed in the following. They include the following:

- Etch rate, e.g., [4.203]
- Material selectivity [4.220]
- Etch anisotropy [4.204]
- Persisting etch damage [4.56]
- Surface morphology [4.56]
- Etch delay [4.29]

General overview articles on the etching of III-N semiconductors are provided, e.g., in [4.56, 4.172, 4.204].

4.5.1 Dry Etching

Dry plasma-based etching has become a dominant patterning technique for the etching of III-N semiconductors, e.g., [4.204]. This is especially true, because wet etching of III-N semiconductors is less effective than in other III-V semiconductor material systems [4.181, 4.204] and can hardly be called an industrially-suitable technology module. Dry etching of III-N materials was initially developed for highly anisotropic mesa etching, targeting high etch rates of $\geq 1 \mu\text{m min}^{-1}$, smooth surfaces, and nonselective material removal [4.190]. Isotropic etching of III-N semiconductors leading smooth surfaces, low plasma-induced damage, and material-selective etching, has found increased interest, e.g., [4.204]. It is needed for the definition of recess and contact structures, however, this technique also suffers from severe obstacles.

Etch Methodologies

Several methodologies for plasma generation are being used for semiconductor dry etching. Dry etching is performed either by physical reaction or by chemical reaction or a combination of both. The most important basic techniques have been demonstrated for III-N semiconductors, e.g., [4.204]:

- Reactive ion etching (RIE) including reactive and sputtering material removal based on
 - Inductively coupled plasma (ICP-RIE) [4.43, 4.220]
 - Electron cyclotron resonance (ECR-RIE) [4.203]
- Ion beam etching methods such as chemically-assisted ion beam etching (CAIBE)

Pure RIE etching is based on reactive and physical material removal and intended for anisotropic etch profiles at relatively high etch rates. High-density plasma generation methods, such as ICP and ECR, use plasmas with increased ion densities. The advantages of ICP and ECR compared to pure RIE are based on the decoupling of the plasma density from the particle energy, so that anisotropy and damage in the semiconductor can be more effectively

separated and thus controlled [4.43]. As reported below, the methodologies of ICP, ECR, and RIE can be combined [4.56, 4.69]. CAIBE is an ion beam etching method. It allows a decoupling of ion energy and ion density and thus a higher energy of the ions in the process. It produces high etch rates of $>100\text{ nm min}^{-1}$ through the introduction of a chemical component such as Cl_2 into the plasma. It is often used for mesa etching, e.g., in [4.126].

Plasma Chemistries

Plasma-based etching techniques use several plasma chemistries. A good overview article on the chemistry is given in [4.204]. Chlorine-chemistry etching is the substantial method for dry etching of the Al/Ga/In/N material system. Initial studies of the etching of GaN by RIE using BCl_3 and SiCl_4 are reported in [4.161]. Etch rates of 17.5 \AA s^{-1} are reported using BCl_3 chemistry. Several studies are available with respect to the additive gases, RF-source power [4.43], acceleration bias [4.56], and discharge composition [4.203]. High-density-plasma-based reactive ion etching (ICP-RIE) of GaN, AlN, and InN is reported in [4.220]. Both Cl_2/SF_6 and Cl_2/Ar plasma chemistries are investigated. Etch rates of up to 680 nm min^{-1} are reached with the application of a high DC bias of 280 V. At the same time, high GaN:AlN selectivities of 8:1 can be reached in a Cl_2/Ar plasma at 10 mTorr, 500 W ICP-source power, and 130 W cathode RF-power. A study on inductively coupled plasma (ICP)-RIE Cl_2 etching of GaN, AlN, InN, InAlN, and InGaN is given in [4.43]. The DC-bias is again relatively high, i.e., 100 V. The etch is strongly ion-assisted and thus anisotropic. Etch selectivities of InN of 6 over the other nitrides are achieved. An increase in etch rate with source power is found as well as a decrease of the etch rate with pressure. The etch rates typically reach several 10 nm min^{-1} , so that etch-depth control is a critical issue [4.43] considering device definition. A GaN:InN selectivity of 6.5:1 is reached at a pressure of 5 mTorr.

The effects of added gases, such as H_2 , Ar, and CH_4 , on ICP-RIE Cl_2 -dry etching of GaN and InGaN are reported in [4.156]. Pure Cl_2 plasma at a pressure of 10 mTorr produces strong anisotropic etching and very rough surface morphologies. The ICP power is 500–2,000 W, the RF-power amounts 100–250 W at high DC-bias of up to 400 V.

The significant etch delay observed during the RIE etching of GaN using Cl_2 -chemistries is explained by persistent hard-to-etch surface oxides, e.g., in [4.29, 4.190]. This oxide can cause an etch delay of some 10 s. This etch delay is equivalent to about 10–15 nm of nominal etch depth, which is in the order of typical recess depths. This fact causes a big uncertainty for FET definition. A BCl_3 plasma pretreatment can remove the etch dead time, as reported in [4.29].

The etching of GaN by RIE and SF_6 chemistry is systematically investigated in [4.15] for DC-bias between –250 and –400 V. Etch rates of up to 167 \AA min^{-1} are reached. The etch rate increases with increasing SF_6 flow. It is stressed that SF_6 is less corrosive than Cl_2 and Br_2 plasmas.

Electron cyclotron resonance-based reaction ion etching (ECR-RIE) of GaN using chemistries of H₂, He, Ar, and CH₄/Ar/H₂ are investigated in [4.56]. Consistent changes of plasma-induced damage are found for the increase of the DC-bias/ion energy. The damage is further correlated with the mass of the ions, e.g., for Ar.

ECR-based plasma etching of GaN, AlN, and InN using iodine or bromine plasma chemistries is reported in [4.203]. The etch rates for iodine chemistries are typically higher than those for Cl₂-chemistries, while bromine (HI)-based chemistries yield a reduction of the etch rate. The investigations are performed at a pressure of 1 mTorr for microwave powers between 200–1,000 W. InN yields higher etch rates for bromine chemistry than for chlorine chemistries.

Etch Damage and Contamination

Dry-etch-induced damage is of critical importance to the underlying semiconductor layers and their appropriate functioning in the device. Several investigations of etch damage are available, e.g., [4.190, 4.204, 4.212]. Etch damage modifies both the conductivity and the carrier mobility through the introduction of both defects and disorder [4.56]. This is also true for the optical properties of devices, where several investigations on etch damage and its recovery are available, e.g., as reported for ICP etching of LEDs in [4.157]. Several mechanisms have been proposed to cause etch damage in III-N semiconductors. Ion channeling of Ar⁺ is suggested for low energy bombardment of GaN in [4.77]. It is found that GaN is more sensitive to ion channeling based on the decrease of the photoluminescence observed after ion bombardment. The second effect is atomic displacement of the lattice or amorphization. The effect of RIE and photo-assisted RIE on n- and p-doped GaN is investigated in [4.190]. The displacement damage is found to accumulate near the surface at low RF-powers of 50 W at medium –100 V DC-acceleration bias and short exposure times. Contamination is another critical problem in dry-etch processing. Oxygen contamination of GaN is reported in [4.161] after RIE etching using BCl₃. The samples that have undergone BCl₃ etching show increased content of oxygen in the top 10 nm of the GaN layer, determined by Auger spectroscopy. The oxygen is deduced to react from the surface with the damaged semiconductor layers. An impact on the first 10 nm of the device can be substantial. The impact of the presence of hydrogen in III-V semiconductor dry-etch processes is described in [4.63]. Hydrogen has two functions for the etching: its addition to the plasma considerably improves the surface morphology during the etch. At the same time hydrogen addition reduces the etch rate of mask materials such as Si₃N₄, which reduces mask erosion during etching. Residual hydrogen further passivates donors and acceptors in the semiconductors [4.63].

Several device issues can be traced to etch damage. The high access base resistance in III-N n-p-n bipolar transistors can be attributed to etch damage

of the p-type contact during mesa formation, as reported, e.g., in [4.71]. P-type GaN is especially sensitive to etching, and a large number of publications is devoted to this problem. For the formation of contacts in optoelectronics, see [4.11, 4.133, 4.210, 4.226]. Annealing procedures can be used to reduce the ohmic contact resistances on p-type GaN in [4.210]. An RTA is performed at 600°C. Surface morphology is another issue after substantial material removal by dry etching in devices [4.156, 4.172]. The increase in the RMS through etching leads to microstructural changes that have a strong impact on devices. During mesa and etch-processes, several issues may occur, which, however, have not fully been detailed in the literature for III-N devices. They include the following:

- General adhesion problems of metals due to reduced surface quality after non-optimized etching [4.156]
- Mask erosion during processing [4.63, 4.266]
- Carrier passivation or compensation in the barrier layer of FETs [4.30]

Similar issues have been reported and solved for GaAs devices by optimization of the etch procedure. The impact of the recess etching on the barrier is discussed in more detail below.

4.5.2 Wet Etching

The ability to fabricate well-defined, reproducible, flat, and plane parallel interfaces is essential for the fabrication of III-N devices [4.73]. Wet etching is the second potential alternative for chemical etching of III-N semiconductors [4.172]. The lack of chemical reactivity of group III-nitrides to wet chemical etching has been repeatedly stated, e.g., in [4.73, 4.172]. As an advantage, wet etching generally avoids, or at least reduces, etch damage. As in any other semiconductor system, the reproducibility of wet etch is controlled mainly by the etchant transport at the semiconductor surface and can thus be very sensitive to the geometry of the actual etch situation [4.73].

Wet etching of GaN by hot H₃PO₄, NaOH, and KOH is described in [4.129] for a temperature range from RT to 250°C. KOH-based solutions etch AlN and InAlN, while the etching of GaN by KOH (30% mol) is found to be critical [4.233]. The etch rates reach 3.2 μm min⁻¹. However, acids such as HCl, HNO₃, and H₂SO₄ do not reach reasonable etch rates. Generally, the etchants used have to be aggressive to reach reasonable etch rates. Further, typical etch temperatures are beyond 100°C, i.e., beyond the boiling point of pure water, so that other solvents, such as ethylene glycol, are suggested [4.233]. Highly anisotropic etch rates of up to 3.2 μm min⁻¹ can be reached with H₃PO₄. KOH reaches similar etch rates in various solvents. Wet etching of polycrystalline AlN by KOH-containing photoresist remover is reported in [4.181]. As expected, the etch rates are found to depend strongly on the crystal quality of the polycrystalline AlN. This etching of AlN is further selective with respect to InN and GaN. Wet etching of InN by aggressive KOH and NaOH

solutions is described in [4.76]. Acid solutions are found to be inappropriate, as no etch rate is observed. Alkaline solutions such as KOH and NaOH (33% weight) produce controllable surfaces. Etch rates of $10\text{--}100 \text{ \AA min}^{-1}$ are reached at 50°C . Such solutions can be particularly useful for the removal of etch damage induced by dry etching.

Wet-Etch Enhancement Techniques

Given the low etch rates of wet etching, etch-rate-enhancing techniques have been investigated in several publications. Gate-recessing of GaN MESFETs using photo-accelerated electrochemical etching (PEC) is described in [4.205]. Hg-lamp-illuminated wet etching by KOH solution yields etch rates of 50 nm min^{-1} at a concentration of 0.02 M at an illumination of 40 mW cm^{-2} . The resulting RMS roughness is 1.5 nm [4.288]. Simpler UV photo-enhanced methodologies have been suggested and are described in [4.13]. The light illumination occurs at 365 nm at 25 mW cm^{-2} . The etch rate is 50 nm min^{-1} . Photo-electrochemical wet etching of GaN using a KOH solution and broad area Hg-lamp illumination is further described in [4.287]. N⁺-doped and n-doped GaN could be etched with etch rates of $17\text{--}20 \text{ nm min}^{-1}$, while p-doped GaN could not be etched at all by this technique. HeCd-laser-based photo-enhanced wet etching of GaN is given in [4.182]. Both dilute HCl:H₂O (1:10) and 45% KOH:H₂O (1:3) are used. This results in etch rates of a few hundred $\text{\AA}/\text{min}$ for HCl and few thousand \AA min^{-1} for KOH. However, because of the aggressive chemistries, there is a lack of mask materials that can resist these chemistries [4.69]. A comparison of nitride Schottky diodes and AlGaN/GaN HFETs, etched by either ICP dry etching or KOH and H₃PO₄ PEC-wet etching, is reported in [4.235]. The PEC etch rates are found to be strongly dependent on the material composition of the Al_xGa_{1-x}N ($0.17 \leq x \leq 0.44$). Etch rates as high as 400 nm min^{-1} can be found for H₃PO₄ and up to $2,000 \text{ nm min}^{-1}$ for KOH, strongly dependent on the pH value. A selectivity of 12.6:1 is achieved for Al_{0.17}Ga_{0.83}N/GaN at pH = 15. The comparison of the HFETs fabricated by PEC and dry etching yields lower leakage currents for the PEC devices.

4.5.3 Recess Processes

Technologically related to the etching of III-N semiconductors, the development of recess processes at both ohmic and gate contacts is very desirable. On the device level, this is due to the following effects:

- A reduction of access resistances for the ohmic contacts [4.186] in FET or bipolar devices
- An improvement of charge control in the gate region [4.58] of FETs
- An increase in the gain \times breakdown voltage product through decoupling of gain and breakdown [4.186, 4.266] in FETs

The issues resulting from this processing technique are discussed in the following sections.

Issues of Recess Processes

Fig. 4.14 gives typical sketches of single gate-recessed AlGaN/GaN HFET for both material-selective (left) and nonselective (right) etching. The critical issues of the recess definition involve the etch-process-control. The gate-recess requires the processing of the most sensitive device region. Both material selective [4.268] and nonselective [4.58, 4.153, 4.186] etch methodologies have been reported. For conventional dry etch processes, the initial selectivity of GaN to AlGaN amounts to 1:1–2 only, i.e., no selectivity, [4.266]. Thus, for nonoptimized conditions, selective plasma etching is not a reproducible process for III-N semiconductors. Further, because of the expected etch damage, an additional surface recovery process may be necessary, e.g., as mentioned for Ar/Cl₂/CH₄ etching in [4.266]. A RTA step is performed at a very high temperature of 700°C for recovery, which is a critical temperature. A second issue is the depth control for the uniform definition of small-gate-length FETs, suitable for highly reproducible processes, as suggested in [4.186]. The definition of etch-stop layers is critical despite of the low selectivity of most of the III-N materials. A third issue is plasma damage and plasma material introduction/contamination, as they are used for defining enhancement-mode AlGaN/GaN FETs without a recess in [4.30]. This nonintentional contamination is well-known in the processing of GaAs and requires special attention.

Examples of Gate-Recess Processes

Cl₂-based plasma chemistry is typically used for the processing of gate recesses in III-N FETs. A baseline low-damage Cl₂/Ar/(CH₄)-based gate-recess RIE etch processing is described in [4.266]. A RTA annealing step is used after the etching. The etch mixture is further developed from Ar/Cl₂-based plasma

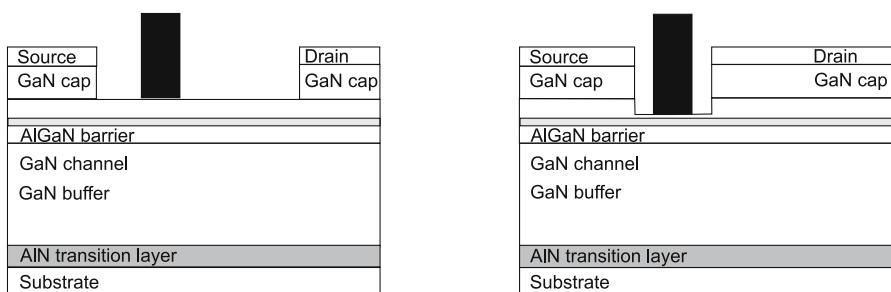


Fig. 4.14. Recessed AlGaN/GaN HEMT: (left) selective, (right) nonselective

involving an Ar/Cl₂/CH₄/O₂-based plasma rather than an Ar/Cl₂/O₂-gas-mixture. A selectivity of AlGaN to GaN of 16:1 is found with the improved plasma composition with optimized O₂-flow. A similar plasma mixture is used in [4.268]. However, a 5 nm thick GaN-doped cap layer is applied in the epitaxial layer sequence in this case. The recess is selectively etched through the GaN to the AlGaN layer. The contact resistances can be significantly reduced by the application of the recess process. Further, characterization of recess-gate AlGaN/GaN HEMTs on sapphire substrates is given in [4.149]. The gate-recess process involves nonselective Cl₂/Ar ICP-RIE etching using an etch DC-bias of -50 V and a pressure of 3 mTorr. This results in an etch rate of 12.5 nm min^{-1} . The gate-recess window has a geometrical width of $1\text{ }\mu\text{m}$ and is centered between source and drain. Cut-off frequencies $f_T = 107\text{ GHz}$ are reached with a gate length $l_g = 0.15\text{ }\mu\text{m}$. The source-drain spacing is $2\text{ }\mu\text{m}$ in this case. A systematic characterization of a Cl₂-based gate-recess process is given in [4.27]. The self-aligned gate recess involves a low-energy RIE process. The etching conditions are 15 W of RF-power, a DC-voltage of -10 V , and 10 mTorr pressure. Devices based on three different etching times (50–150 s) are compared to unetched devices. To minimize the influence of surface conditions on etch depth, the etches are preceded by an oxygen plasma and a 20 s rinse with HCl:DI (1:10). The plasma treatment is used to remove residual photoresist from the exposed regions and the HCl dip is employed to remove any possible surface oxides. The etch depth is found to be nonlinear with the etching time. One problem of this approach, however, is based on the nonselective etch procedure, which makes depth control very critical, especially with regard to the nonlinearity of the etching time. Another systematic study of the Cl₂-based etching is provided in [4.28]. Again, a significant etch delay is observed and attributed to the formation of a thin surface oxide layer. This possible etch delay has a tremendous impact on the uniformity of the threshold-voltage for large area wafers, as it directly results in additional nonuniformities of the threshold voltage V_{thr} .

On the FET device level, the application of a gate-recess process for mm-wave applications and resulting improvements in gain and PAE are reported in [4.186]. The gate recess is etched non-selectively and the recess is fully filled with gate metal in this case. The gate-to-channel separation is reduced to $d_{\text{gc}} = 11\text{ nm}$. Power and linearity characteristics of field-plated recessed-gate AlGaN/GaN HEMTs are given in [4.38] based on the recess process in [4.28]. In this case, the destructive three-terminal breakdown voltages of the recessed and nonrecessed devices are reported to be similar in the order of 110–120 V. Very high PAE values of 74% are achieved and very high operation voltages $V_{\text{DS}} = 90\text{ V}$ on similar devices with field plate lead to a power density of $\geq 18\text{ W mm}^{-2}$ [4.38].

Low gate-to-channel separations can also serve to produce enhancement-mode HEMTs. Further, etch damage during recess etching shifts the threshold voltage to more positive values, as reported, e.g., in [4.30]. In this case, a CF₄-treatment at an RF-power of 150 W for 150 s creates sufficient damage

to create enhancement-mode AlGaN/GaN HEMTs. A comparison of conventional planar and gate-recessed AlGaN/GaN HEMTs with respect to the high temperature characteristics up to 200°C is given in [4.153]. In this case, the gate recess is formed by low-power RIE etching for a gate length $l_g = 0.25\ \mu\text{m}$ and is again nonselective. The main finding for the recessed HEMTs involves reduced device leakage at higher temperatures. The nonrecessed device show a dramatic increase of the gate currents with temperature. Further, the linear gain at 10 GHz is increased by more than 2 dB for all operation bias.

Enhancement-Mode HEMTs

The realization of normally-off transistors with III-N semiconductor is a delicate task, as also will be shown in Chapter 5. The combination of thin barrier layers, recess processes, and specific surface treatments [4.30] lead to the realization of enhancement-mode or normally-off transistors, which are particularly interesting for switching applications [4.217]. Gate recessing allows the definition of the threshold voltage independent of the layer growth. An enhancement-mode HFET with $V_{\text{thr}} = 0\ \text{V}$ is achieved for a gate-to-channel separation $d_{\text{gc}} = 7\ \text{nm}$ for an AlGaN/GaN heterostructure. The recess is non-selectively etched into the 30 nm-thick AlGaN-barrier. Enhancement-Mode Si₃N₄/AlGaN/GaN MISFETs are reported in [4.265]. The layer structure consists of a 21 nm-thick AlGaN barrier layer and a 15 nm-thick SiN gate dielectric layer. This leads to a threshold voltage $V_{\text{thr}} = -4\ \text{V}$. An additional fluoride treatment with RIE in the gate area leads to a threshold voltage shift to $V_{\text{thr}} = 2\ \text{V}$. The exposure is performed by a powerful RIE CF₄-treatment with an RF-power of 150 W and a very long treatment time of 190 s. This procedure provides an enhancement-mode HEMT, however, based on a strong etch damage. Submicron AlGaN/GaN E-HEMTs are reported in [4.60, 4.185]. However, for gate lengths of 100–200 nm the product of gate length $l_g \times f_T$ is only 5–7 $\mu\text{m}\ \text{GHz}$ and thus below the expectations, partly again due to etch damage. AlN/GaN HFETs with a small gate length $l_g = 100\ \text{nm}$ and a cut-off frequencies $f_T/f_{\max} = 87/149\ \text{GHz}$ are reported in [4.95]. The AlN barrier is extremely thin and amounts to only 2.5 nm, which leads to a threshold $V_{\text{thr}} = +0.14\text{--}0.55\ \text{V}$. A special Cat-CVD passivation leads to the formation of the 2DEG in the channel, which is depleted without surface passivation.

A very positive threshold voltage $V_{\text{thr}} = 1\ \text{V}$ is achieved for AlGaN/GaN HEMTs through the application of 10 nm highly-doped p-GaN cap-layer on top of a 12 nm Al_{0.22}Ga_{0.78}N barrier with a GaN channel [4.236]. At the ohmic contacts the p-doped cap layer is etched away.

Normally-off transistors can further be realized on p-GaN layers, with p-type channels, as shown in [4.60, 4.185]. The p-channel devices yield a very low maximum drain current I_{DS} of 10 mA mm⁻¹, which is about two orders of magnitude lower than that for n-channel (H)FETs.

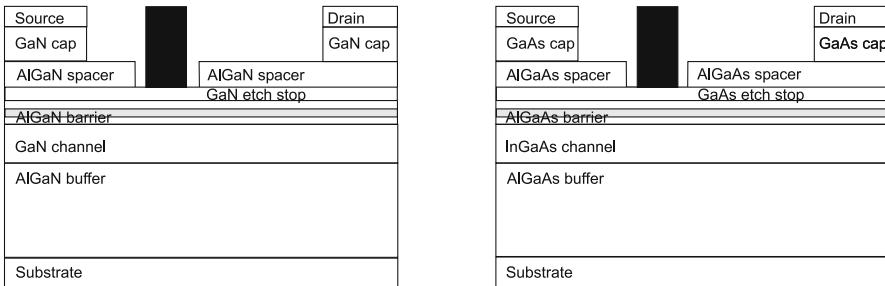


Fig. 4.15. Double Recessed HEMT: (*left*) GaN, (*right*) GaAs PHEMT

Advanced Recess Processes

As the etch methodologies still improve, more advanced etch techniques can be considered. These include ohmic-recess- and more advanced gate-recess-techniques such as double recesses [4.28]. Ohmic recesses have been proposed, e.g., in [4.127]. An etch is applied to reduce the access resistance and to control the lateral ohmic contact definition. Fig. 4.15 shows the proposal for a double gate-recess HFET device and compares it to a selectively-etched double recess GaAs PHEMT. The AlGaN/GaN material system involves the creation of channel layers through polarization charges contrary to the δ -doping of GaAs PHEMTs. The application of the double recess concept is rendered complicated due to the reduced selectivity of the AlGaN/GaN. These difficulties must be overcome to create GaN double-recessed HFETs [4.28]. A similar process has been proposed in [4.140], however, without further detailed results. The first demonstrations of AlInGaN/InGaN/GaN HFETs with a double gate-recess are provided in [4.1]. The AlGaN barrier for the double recess is etched with a BCl_3 and Cl_2 process without an etch-stop with the application of two etch bias conditions.

4.6 Surface Engineering and Device Passivation

This section addresses the technological means for engineering the ungated and the gated dielectric/semiconductor interfaces of III-N FETs in addition to the introduction in Chapter 2 and the analysis and modeling in Chapter 5.

4.6.1 Passivation of the Ungated Device Region

The material engineering of the semiconductor/dielectric interface of the ungated device region involves mostly device passivation. Physically, the deposited dielectric saturates dangling bonds at the ungated semiconductor interface to vacuum. The passivation layer modifies, i.e., mostly reduces the active trap concentration at the interface [4.105]. This passivation step is

therefore very important, due to the high polarization-induced charges present in III-N devices. The strong occurrence of low-frequency and RF-dispersion in unpassivated III-N devices [4.246] is another hint to this importance (see also Chapter 2). Technologically, device passivation can be split into several process steps:

- Surface cleaning [4.171], i.e.,
 - Material removal [4.241]
 - Modification of the surface morphology [4.21]
- Pretreatment of the semiconductor surface, i.e.,
 - Chemical reaction at the surface (e.g., oxidation) [4.85],
 - Physical conditioning, (e.g., adsorption of gases) [4.206]
- Deposition of a dielectric, e.g., [4.89]
- Strain engineering by subsequent layers [4.241].

These enumerated steps cannot be fully separated in subsequent actual processing steps. For example, the deposition of a dielectric also modifies the surface morphology and the strain at the interface. Surface passivation has several functions for the device, which include the following:

- (Early) protection of surfaces open to the process flow, e.g., [4.81] from the influence of processing steps such as coatings, developer solutions, plasmas, and ambients [4.68, 4.114]
- Removal of surface material and intended damage [4.241]
- Modification, typically a reduction of surface states [4.139]
- Physical, mechanical, and chemical stabilization of the surface [4.262]
- Compensation of surface charge [4.171] by p-type [4.47, 4.48] and n-type device capping [4.128, 4.225]
- The modification of the surface electrical currents [4.242] by isolating or conductive dielectrics or conductive interlayers [4.139]

Technological solutions to the dispersion problem can be explained by mechanisms detailed in Fig. 4.16 and in the following.

A Model for Frequency Dispersion in an HFET

The understanding and avoidance of frequency dispersion is basically a simple exercise of dynamic charge conservation. Figures 4.16 and 4.17 show two basic situations for the interaction of dielectric–semiconductor interface with the device channel:

1. In the regular situation, I, the negative channel charge in an n-type FET is caused by a positive interface charge at the heterointerface if we assume polarization doping only. Intentional doping modifies the situation, however, does not provide additional information. The interface positive charge results in a negative surface charge at the top of the barrier (Fig. 4.16), which requires compensation at the surface. If the charge at the surface is not fully compensated in a static and dynamic sense,

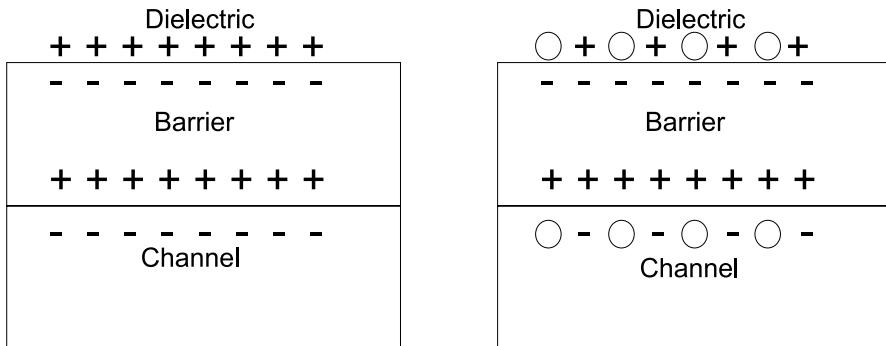


Fig. 4.16. Trapping effects at the interface dielectric–semiconductor and their impact on the FET channel

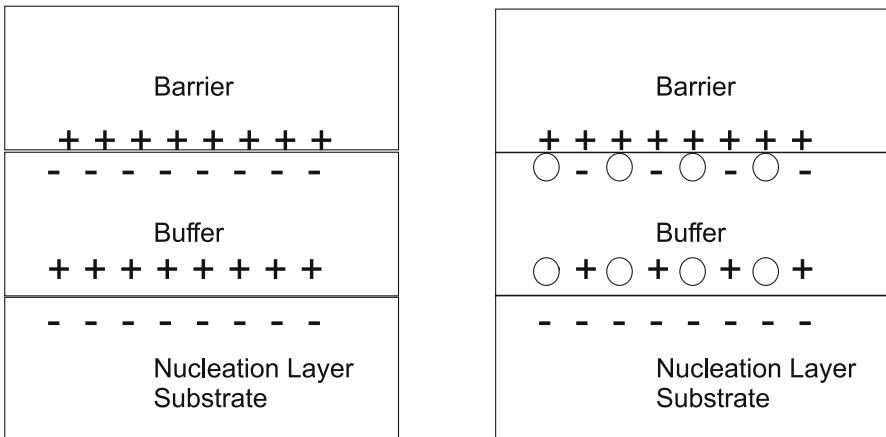


Fig. 4.17. Trapping effects in the buffer layer and their impact on the FET channel

frequency dispersive effects will occur. The modification of the surface charge during dynamic device operation will then directly interfere with the channel charge.

2. In the second situation, II, the empty charges represent the dynamic detrapping of the surface charges with different time constants. This results in a modification of the channel charge, again, meant dynamically. This dynamic trapping and detrapping is further fundamentally connected to the static and dynamic leakage currents at the semiconductor barrier/dielectric interface [4.142, 4.242]. The dynamics are influenced by various time constants involved.

These principle considerations are especially true for the ungated interface regions of the device; however, the situation is further strongly influenced by

the effects at the backside of the channel [4.20, 4.216], as depicted in Fig. 4.17. These effects at the backside include the following:

- Bulk semiconductor trapping in the device buffer [4.136]
- Trapping/detrapping at the buffer–substrate interface [4.20]
- Leakage currents in the buffer layer [4.253]

Generation and recombination processes at buffer traps can modify the charge balance, as depicted in Fig. 4.17, similar to the dielectric/(Al_xIn_{1-x})GaN interface. Further, because of the heteroepitaxy, the buffer region is highly disordered in the lower part and thus susceptible to carrier trapping. These trapping and detrapping effects at both interfaces and buffer are strongly modified by leakage currents [4.142, 4.242, 4.253], either through the buffer or at the interface. The leakage currents can occur for both DC-conduction or RF-currents. These principal effects are now detailed in the following sections.

4.6.2 Physical Trapping Mechanisms

A variety of trapping effects have been observed. General overview articles on the trapping effects in wide-bandgap microwave FETs are given, e.g., in [4.20, 4.21]. Summarizing the various findings on the mechanisms, Fig. 4.18 shows the location of traps in a typical AlGaN/GaN HFET. The device effects include the following:

- 1.) Semiconductor/dielectric surface traps [4.17, 4.139, 4.215, 4.260, 4.295]
- 2.) Barrier bulk traps [4.131]
- 3.) Interface traps at the channel/barrier interface
- 4.) Bulk traps in the buffer [4.20, 4.176]
- 5.) Interface traps at the substrate/semiconductor interface and in the nucleation layer [4.176, 4.231]
- 6.) Recombination/generation in depletion zones of the series resistances [4.144]

The underlying dynamic physical effects of both electrons and holes [4.259] are now summarized:

- Generation/recombination with surface traps at the passivation/barrier interface
- Generation/recombination with AlGaN barrier traps
- Generation/recombination with (In)GaN channel traps
- Generation/recombination with interface traps at the channel/barrier interface
- Generation/recombination with bulk traps in the buffer [4.20]
- Dynamic generation/recombination at the nucleation layer

The generation/recombination mechanisms involve the following:

- Shockley–Read–Hall generation/recombination,

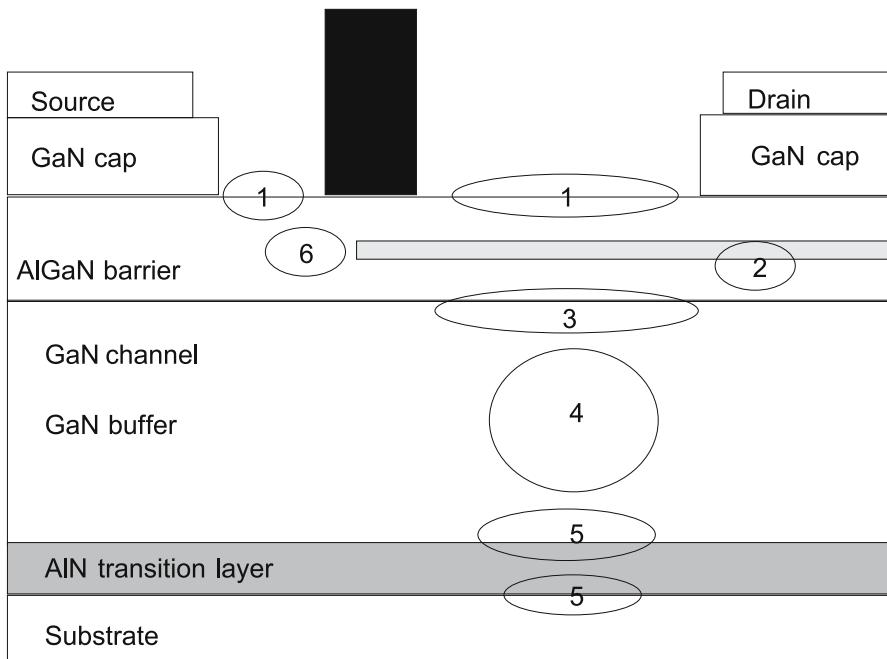


Fig. 4.18. Possible locations of traps in the GaN HFETs

- Trap-assisted band-to-band tunneling [4.215], especially
 - At the interfaces
 - With deep traps near midgap [4.198]
- Direct recombination
- Electroluminescence [4.195] (also hot carrier-induced) [4.176]

Additional (bulk and interface) traps can further be created by device degradation, e.g., [4.215].

4.6.3 Trap Characterization

Several investigations can be performed with regard to the impact of traps in III-N devices, e.g., as reported in [4.20, 4.21, 4.128]. Trapping effects on microwave performance, originating from the semiconductor/dielectric interface and in the buffer, have been investigated by a large number of methods, e.g., as detailed in [4.20, 4.135, 4.139, 4.159]. The nature of the traps is typically characterized by dynamic transient analysis. The related recombination time constants vary from seconds [4.260] to $1\ \mu\text{s}$ [4.102]. This includes also the thermal relaxation time of, e.g., $6\ \mu\text{s}$ [4.20, 4.176]. Even faster trapping has to be considered, as some devices show different dispersion when pulsed with time constants equivalent to frequencies faster than 1 MHz. Capture

cross-sections have been determined in various publications, e.g., [4.21, 4.135]. Various methodologies are available to characterize traps and defects in III-N devices on the semiconductor level, e.g., in [4.260] and on device level in [4.262]. These methodologies include the following:

- Luminescence investigations [4.24]
- Photoionization spectroscopy [4.135]
- Surface potential analysis [4.139] and
- Deep-level transient spectroscopy (DLTS) [4.159]

Traps and defects prevail in both bulk material [4.24, 4.136] and at the various interfaces within the device [4.109]. A model detailed in [4.109] states the specific importance of the access region caused by the ungated surfaces. The investigations typically provide three types of information: the changes of the device terminal characteristics under pulsed-conditions [4.179], the energy characteristics and cross-sections of the traps [4.136], and their dynamic time constants [4.135]. Trap time constants between nanoseconds [4.179, 4.259] and several hundred seconds [4.139] can be found. Apart from the trap energies, cross sections, and time constants, additional information is extracted, i.e., the thermal relaxation time of the terminal currents of HFETs, e.g., $6\text{ }\mu\text{s}$ mentioned in [4.20, 4.176]. The surface potential at the interface is additionally extracted and found to be modified, e.g., by UV illumination [4.135]. This demonstrates the impact of the surface-related trapping on the drain current [4.139].

Interface Trapping Effects

The interfaces in heterostructures are typical locations for the presence of traps, due to the abrupt modification of the crystal structure. Effects of interface traps on GaN (H)FETs are reported in [4.21, 4.249]. Some principal findings for the interface trapping are summarized:

- The effect of dispersion is often attributed to the surface effect, as device behavior differs significantly in the passivated and the unpassivated state [4.21, 4.216, 4.225]. This is, of course, true in general; however, the surface passivation has also secondary effects on the electric field distribution in the buffer.
- The investigation of surface-related drain-current dispersion effects in AlGaN/GaN HEMTs based on 2D-simulations is described in [4.177]. The impact of holes is stressed in this analysis. The extracted time constants amount to $10^{-4}\text{--}10^{-5}\text{ s}$. An activation energy of 0.3 eV is extracted from the temperature dependence of the pulsed-DC-measurements. The application of a 2D-simulation framework makes surface-related effects responsible for both gate and drain lag effects.
- Drain-current transients and surface potentials can be analyzed by direct Kelvin probing in the ungated HFET region, as reported in [4.139]. The measured surface potential is found to be strongly modified by UV-laser-

illumination. It is found that surface states cause observed transients in the drain current of GaN HFETs when they trap electrons tunneling from the gate. The findings are supported by a theoretical model.

- Low-energy electron excited nanoscale-luminescence spectroscopy (LEEN) performed on AlGaN/GaN heterostructures yields yellow luminescence at energies of 2.18 and 2.34 eV [4.24]. The luminescence originates from near the 2DEG region. Strong strain is observed in the 2 nm-thick GaN cap layer on top of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$ barrier, which yields strong optical emissions at energies ≤ 1.6 eV. The origins of the emissions are localized at the passivated interface region.
- Analysis of surface charge injection in passivated AlGaN/GaN FETs using an MOS test electrode is given in [4.194]. A major finding is that the charge center may not be located at the interface between the passivation and the semiconductor interface, but rather deep within the (bulk) dielectric overlayer. This charge may be trapped rather firmly in the passivation layer and not located in the interface states only.
- The mechanisms of the current collapse removal in field-plated HEMTs are also surface-related, as detailed in [4.143]. If the dielectric is highly insulating, the current collapse is found to be more pronounced than in the case of more conductive dielectrics under or near the gate. This confirms the direct relationship of leakage currents and dispersion removal at the interface [4.142].

Bulk Trapping Effects

Bulk material has to be considered for trapping effects, as typical electronic GaN devices require buffer layers with thicknesses of ≥ 500 nm to cover the mismatch of the heteroepitaxy, e.g., [4.114]. The effects found in buffer layers are summarized in the following.

- Studies performed by photoionization spectroscopy of traps in bulk GaN MESFETs are given in [4.135, 4.136]. A model is applied successfully that assumes a net transfer of charge from the conducting channel to the insulating buffer. The trapped carriers are reversely activated by photoionization. The procedure provides a dynamic model for drain current recovery in the MESFET using two trap levels. The trap levels isolated are consistent with persistent photoconductivity centers [4.21, 4.176]. A similar investigation is reported in [4.136] for AlGaN/GaN HEMTs grown on sapphire substrates by both MBE and MOCVD growth. Similar results in the photoionization spectra are obtained for the HEMTs grown by both methods. Similar phototransient and electroluminescence measurements are included for the diagnosis of trapping phenomena in GaN MESFETs in [4.176]. The analysis yields deep trap energies of 1.75, 2.32, 2.67, and 3.15 eV below the conduction band.
- Electroluminescence measurements on the same samples confirm the emission of light, especially at an increased operation bias $V_{\text{DS}} \geq 15$ V.

The deep traps are considered to be localized in the buffer or at the buffer/channel interface [4.176].

- Deep-level characterization via deep-level transient Fourier spectroscopy in Pt/GaN Schottky diodes on MBE RF-plasma-grown material is given in [4.159]. The existence of an additional intermediate buffer layer grown at temperatures of 690°C reduces the concentration of the deep trap levels at 0.45 eV below the conduction band by three orders of magnitude. Further, low-frequency excess noise measurements are used as a surface-sensitive measure for the analysis of traps, while the DLTS measurements are used to analyze the buffer.
- The influence of threading dislocations caused by the heteroepitaxy of III-N materials has been analyzed in various ways. A comparison of photodetectors grown by heteroepitaxy for GaN on sapphire (0001) and by MOCVD homoepitaxy of SiC on 6H SiC is given in [4.247]. The comparison yields higher leakage currents in GaN on sapphire, due to increased threading dislocations. ELO growth has proven to mitigate that effect [4.145].
- High-injection hole-lifetimes of 15 ns are determined in bulk GaN Schottky rectifiers on freestanding GaN measuring the reverse recovery transient [4.115]. The substrates are initially grown by HVPE on sapphire substrates and the sapphire is subsequently removed. This again hints at the impact of the mismatch to the material quality and related trapping.

These basic findings for the trapping are now further analyzed in the following sections.

Investigations of the Lattice Temperature Dependence of Trapping

Trapping and detrapping are processes that yield a strong lattice-temperature dependence. Thus, several investigations are available in order to analyze trap behavior in III-N devices in detail. The behavior of current collapse in AlGaN/GaN HFETs at cryogenic temperatures between 100 and 250 K are described in [4.198]. The main finding is a strong variation of the FET on-region in the output characteristics with temperature. Transient monitoring of the currents at various temperatures allows the isolation of two relaxation mechanisms when the injection time and the temperature of the device are individually varied. The time constants of the relaxation are in the range of seconds at 150 K in this case. The finding of two energy levels within the bandgap in [4.198] agrees with the results from [4.21, 4.176]. Further temperature-dependent investigations of the current collapse for AlGaN/GaN HFETs are given in [4.131]. Temperature-dependent DLTS measurements between 77 K and RT are reported. They reveal a small trap activation energy of 0.28 eV. However, the temperature dependence of the carrier concentration suggests the existence of DX centers in the AlGaN barrier. Further temperature-dependent investigations of the three terminal characteristics are given in [4.160]. The so-called kink effects in the cw-output characteristics of AlGaN/GaN HFETs are found to be more pronounced at cryogenic tempera-

tures of 100 K than at RT, and the pulsed-DC-measurements provide similar characteristics. The paper further suggests the existence of a hole contribution to the gate current at low temperatures. We can deduce from these findings that trapping is persistent at both surface and in the bulk and that their impact on the three-terminal characteristics of AlGaN/GaN HFETs is consistent with findings in GaAs devices. However, the relative impact is more pronounced than is known in the GaAs world.

The Impact of the Initial State of the Device

When freshly processed devices are analyzed, the initial measurements often differ from a stable device status, if such status exists at all. A burn-in behavior is observed, which is partly, but not exclusively, attributed to the trapping effects, related current collapse, and reliability issues. Output characteristics, e.g., in [4.285], show a degradation when the device is measured repeatedly. As burn-in effect have also been observed for several other devices, e.g., InP HEMTs [4.35], the variation of the device properties is found to stop after a burn-in procedure [4.227] for optimized devices.

4.6.4 Technological Measures: Surface Preparation and Dielectrics

A minimum of surface treatment before and during passivation is necessary and unavoidable in any device processing. As a general finding, SiN- or other material-passivation greatly enhance the power performance of AlGaN/GaN devices, e.g., in [4.17, 4.20, 4.72, 4.117, 4.241, 4.246]. The effect on leakage current and dispersion, however, has to be treated in detail, e.g., [4.242].

Surface Preparation

During device fabrication, surface treatment, and cleaning conditions are very important and at the same time unavoidable, as discussed, e.g., in [4.57, 4.171]. Because of the polar nature of the III-N semiconductor materials, the status of the epitaxial surface is critical when the wafers are removed from the growth reactor. The wafer is thus exposed to air prior to further processing and device passivation. The exposure typical leads to an initial oxidation. Early passivation techniques within the process flow have been considered relevant in [4.114, 4.117], since the exposure of the semiconductor surface to air and any kind of processing medium is found to be critical, as also known from GaAs processes [4.61, 4.262]. Typical related process steps in the context of device passivation are ohmic contact formation, annealing, device isolation, and gate recess definition. As an alternative to early SiN ex-situ passivation, in-situ passivation in the growth reactor has also been suggested in [4.104] in order to avoid surface contamination by ambients. This agrees with findings in [4.10] that both the GaN and AlGaN surfaces are found to be highly corrosive when exposed to air or other ambients. This corrosion potentially requires the application of cleaning techniques.

Cleaning Procedures and Pretreatment

Given the sensitivity to any exposure, surface and interface cleaning procedures are vital for the reduction of surface states and dispersion, e.g., [4.178]. An improved fabrication process for obtaining high-power density AlGaN/GaN HEMTs has been suggested in [4.244]. The exposure of the critical ungated surface through harmful plasmas and chemical treatments is completely avoided. For other process variants various surface cleaning procedures have been proposed for the reduction or compensation of surface states, e.g., in [4.72, 4.178]. Before PECVD deposition, the surface in [4.72] is cleaned (in this order) by acetone, methanol, isopropanol, and water. The surface is then dipped in 30:1 buffered oxide-etch for 30 s. No significant changes in device characteristics are seen after these wet cleaning and etch steps. Several other treatments are reported. The surface treatment by a combined $\text{HCl}:\text{HF}:\text{H}_2\text{O}$ (1:1:2) and subsequent HF-buffered oxide-etch (14%) for 10 s in [4.49] is found to exert little influence on the carrier distribution and mobility. This and similar findings point to the existence of stable surface oxides, which can only be removed or modified by very aggressive techniques. The passivation in [4.49] is SiO_2 . The effect of the pretreatment on pulsed-measurements is not reported. Subsequent deposition of the passivation, however, leads to a strong increase in channel-carrier concentration and reduced mobility. NH_3 low-power plasma pretreatment prior to SiN PECVD-based passivation is described in [4.57]. The NH_3 pretreatment is performed with the substrate held at 250°C. The gate-lag ratio observed during pulsed-operation and the output power degradation for long-term RF-operation can be significantly reduced. The increased device reliability is attributed to both the strengthening of the bonds at the interface and the incorporation of hydrogen, which passivates defects. A similar NH_3 treatment is reported in [4.117]. Dry plasma pretreatments are discussed in [4.178]. Plasmas based on SF_6 , O_2 , N_2O , NH_3 , and N_2 are applied. Contrary to wet pretreatment NH_3 -, N_2 -, and combined NH_3/N_2 -pretreatment delivers very strong changes and mitigates the drain-lag. The X-ray photoelectron spectroscopy (XPS) measurements reveal a correlation of the reduction of the carbon concentration on the AlGaN surface with the degree of the mitigation of the drain-lag. Carbon contamination of the surface in AlGaN/GaN HFETs can be mitigated by an air plasma descum and subsequent HCl dip prior to SiN deposition [4.14]. Auger spectroscopy reveals a correlation of the current collapse with the residual carbon contamination. The sensitivity of the breakdown voltage and related gate leakage and surface carrier concentrations to plasma damage in the AlGaN barrier is discussed in [4.216]. A surface-charge defect model is applied. Simulations show that a significant reduction of the surface charge to levels of $1 \times 10^{12} \text{ cm}^{-2}$ is necessary in order to reach suitable gate currents at voltages >100 V, even when a field-plate concept is applied.

Surface treatment of III-N semiconductors is especially important for p-type material. Hydrogen is typically incorporated strongly into the material

during MOCVD growth, thus the layers are specifically sensitive to surface treatment. Hydrogen plasma treatment of p-type GaN is investigated using both hydrogen and deuterium to enable secondary ion mass spectroscopy (SIMS) investigations of the hydrogen effect [4.206]. Hydrogen plasma treatment leads to a strong hydrogen passivation of carriers in the p-type GaN. This is further confirmed by the analysis of the traps at 0.3 and 0.6 eV. Capacitance vs. frequency C(f)-measurements confirm the impact of the plasma treatment on the p-type doping-activation and the suppression of the trapping. At the same time, additional trapping at 0.4 eV is created. Based on these results, the deposition of dielectric material is now analyzed.

The Deposition of Dielectrics: Passivation

The deposition of dielectrics at the semiconductor/vacuum interface yields a large number of possibilities. With the application of optimized interface passivation, the interface neutralizes the net surface charge, as given in Fig. 4.16, in both static and dynamic sense. The net surface charge arises from a polarized GaN cap or AlGaN barrier and from the residual surface states resulting from dangling bonds, absorbed ions, or charge surface residual materials (e.g., oxides [4.10]).

Silicon Nitrides (Si_3N_4)

Silicon nitride is the most popular dielectric for the III-N material system, e.g., [4.17, 4.68, 4.114, 4.128, 4.139, 4.151, 4.246]. Typical effects of the passivation by SiN on III-N devices include the increase of the output power [4.246], reduction of frequency dispersive effects [4.72], and the modification of leakage currents [4.17, 4.242], often leading to a reduction of the breakdown voltages. Further long-term device reliability is positively affected [4.151]. Various methods and recipes exist for the deposition of SiN in its various modifications, e.g.,

- Plasma-enhanced chemical vapor deposition (PECVD) [4.57, 4.68, 4.241, 4.242, 4.246] for low damage deposition with low hydrogen content, including:
 - ECR-PECVD
 - ICP-PECVD [4.57]
- Catalytic chemical vapor deposition (CAT-CVD) [4.89, 4.90, 4.151]
- Others, such as epitaxial in-situ deposition [4.207].

The variations of PECVD deposition typically include the silane and ammonia flows [4.72], the deposition temperature [4.242], deposition pressure, deposition RF-power, and thickness [4.231]. The corresponding detailed engineering is discussed below.

Stress and Stress Engineering

Deposited SiN is an amorphous material that can be influenced in variety of ways. The actual deposition can be adjusted with respect to strain and stress on the underlying material. Stress ranges of the SiN_x on the semiconductor amount to 100–2,000 MPa, as reported, e.g., in [4.79, 4.293]. For SiN deposited by PECVD on AlGaN/GaN HEMTs, several growth conditions are analyzed in [4.246]. The deposition temperature range amounts to 150–300°C. The SiN, grown under NH_3 -rich and higher temperatures conditions, gives the best power performance of the devices. The SiN is further characterized by the etch rate in buffered oxide etch. Nitrides with the lowest etch rate provide the best power densities in the III-N HFETs. A specific stress analysis of the SiN deposited by PECVD is reported in [4.241]. Dual frequency plasma deposition is used. Initial data suggests a strong impact of the induced stress. However, it is found that the surface damage through N-ion bombardment has a very strong influence on the surface, the carrier concentration, and the mobility. When this damage is avoided by a He precursor treatment and thus separated in the analysis, it is found that a uniform compressive stress on the surface has only a minimum impact on the polarization charges. The stress range amounts to –100 to 40 MPa meaning that the nitride is nearly stress-free. The mitigation of both leakage currents and current collapse by low-stress SiN_x with high refractive index is suggested in [4.116]. The in-situ CVD deposition of SiN in an MOCVD reactor is described in [4.39, 4.207]. The deposition occurs at 980°C using disilane and ammonia at a growth rate of 0.1 Å s^{-1} . The thickness of the deposited SiN amounts to 4 nm. Stress data is not provided although a very high strain of the initial SiN layers can be expected.

Temperature and Thickness of the Deposition

The SiN layer can be either composed of one or of several layers. The thickness of the initial and the subsequent passivation layers critically affects the stress and the permeability for ambients on the semiconductor layers. A PECVD-passivation of 350 nm thickness is reported in [4.72] based on silane (SiH_4) and ammonia (NH_3). The deposition is performed at 300°C after a dip in 30:1 buffered oxide etch for 30 s. The deposition leads to a significant increase in the RF-device output power. A more complete study of the various Si_3N_4 -deposition parameters is given in [4.246]. Deposition SiN-thickness, RF-deposition power, and temperatures are investigated with respect to their impact on breakdown and RF-power. The thickness of the first SiN varies between 47 and 275 nm. An optimum for the RF-output power of the AlGaN/GaN HFET is achieved for a SiN thickness of 155 nm and a high deposition temperature of 300 °C, while the breakdown voltage is not critically affected by the SiN parameter variation. The increase in RF-output power is due to the increase in drain current.

The thickness of the PECVD-SiN determined by ellipsometry is 74–80 nm [4.57] deposited at a base plate temperature of 250°C. A SiH₄:NH₃:N₂ plasma recipe is used, which yields a refractive index of 2.03–2.09. The ICP RF-power is 35 W at 13.56 MHz. The crucial parameter in this investigation is not power performance but output power degradation and pulsed-DC-data after aging. The impact of hydrogen for the passivation of defects is discussed to lead to better stability.

The industrial process in [4.114] uses a 90 nm-thick SiN layer deposited by PECVD at 300°C and a pressure of 900 mTorr. After early passivation, this SiN layer is opened by an inductively coupled plasma (ICP)-etch for further processing. In combination with a low-damage ICP etch a very good device efficiency of 65% and output power density of 11 W mm⁻¹ at 2 GHz are achieved. Further the thickness uniformity is of the order of 0.6%.

GaN HEMTs with SiN passivation deposited by catalytic chemical vapor deposition (Cat-CVD) are given in [4.89, 4.117, 4.151]. For the Cat-CVD deposited SiN in [4.151] the thickness is 50 nm after NH₃ pretreatment. The process was similarly developed for GaAs PHEMTs [4.86]. The Cat-CVD procedure with a NH₃ pretreatment provides the elimination of deposition plasma damage and thus reduces defect density at the interface. The output power degradation is 0.4 dB after 200 h of operation. For a similar Cat-CVD process, the deposition temperature is 250–300°C for a SiN thickness of 30 nm [4.90].

Based on these examples on the critical parameters strain, deposition-temperature, and -thickness the reliability aspect of SiN deposition is now discussed in more detail.

High-Field Effects in SiN

Similar to the semiconductor materials, the passivation materials and their interfaces are subject to high-field peaking and subsequent degradation effects. Further, the field distribution in the semiconductor and along the interfaces are critically affected by the SiN deposition so that the impact on reliability is strong. The typical degradation of AlGaN/GaN HEMTs with a degradation of I_{DSS} as a function of time can be compared to the degradation of the current in silicon CMOS devices, e.g., [4.34]. Shifts in the threshold voltage can be fully dominated by interface trap creation at increased bias. Thus, similar measures are required for the mitigation in III-N (H)FETs. The effect of the biasing to SiN-passivated AlGaN/GaN HEMT stressed at $V_{DS} = 17$ V and I_{DS} at $V_{GS} = 0$ V for only 1 h is strong. The PECVD deposition is performed at 300°C. The aging leads to a significant decrease in the transconductance g_m , a reduction of the saturated drain current I_{DS} , and a positive shift of the threshold voltage by at least 0.5 V [4.215]. The 1/f-noise measurements after aging reveal a significant increase of the spectral noise density after aging. These results suggest both hot electron trapping and surface-state creation during device stress.

Possible effects of SiN passivation and high-electric field on short-term AlGaN/GaN HFET degradation are discussed in [4.131]. For a hot pinch-off

stress ($V_{DS} = 20\text{ V}$, $V_{GS} = -8\text{ V}$) for 12 h, the unpassivated device shows a degradation of the saturated current of -37% . SiN passivation reduces the degradation; however, it cannot suppress it completely (-16%). The degradation is again attributed to hot electron trapping to surface states, which can be partially mitigated by the passivation. The modification of the gate lag before and after electric-field stress suggests a modification of the surface trap profiles. A similar investigation, again supported by optical response measurements, is reported in [4.184]. The current collapse can be suppressed by light illumination with energy smaller than the bandgap. The collapse is again attributed to the surface states localized in the gate-to-drain spacing rather than the gate-to-source spacing. In general, the deposition of the appropriate passivation is a key for the realization of reliable devices.

Oxide Passivation of the Ungated Interface

Oxide, e.g., SiO_2 passivation is suggested as an alternative to Si_3N_4 passivation for use in III-N HFETs. Various investigations exist to determine the different surface conditions modified by bias in MIS- and regular Schottky-gate structures, e.g., [4.10, 4.65, 4.85]. This paragraph concentrates on the passivation of the ungated regions while gate dielectrics are discussed below.

A comparison of SiO_2 and Si_3N_4 passivation on AlGaN/GaN HEMTs on silicon substrates is given in [4.17]. Both passivation layers are deposited by PECVD at 150°C (for SiO_2) and 300°C (for Si_3N_4). A higher surface trap density is considered to be responsible for the reduced power performance of the HEMTs with SiO_2 passivation. CV-investigations in MIS structures are reported in [4.10] for nitrided $\text{Ga}_2\text{O}_3/\text{SiO}_2$ films. The SiO_2 passivation is formed by remote O_2/He -based plasma using SiH_4 at 0.3 Torr. The SiO_2 films are deposited by remote PECVD. These improved oxide films provide a reduced density of interface states on n-GaN compared to Si_3N_4 on n-GaN. Effects of annealing on GaN– SiO_2 -insulator MIM-interfaces is described in [4.174]. The deposition of the dielectric on n-type GaN is performed by low-pressure CVD (LPCVD) at 900°C using disilane and ammonia. The n-GaN is cleaned with $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ at 70°C . A very low surface charge of $3 \times 10^{11}\text{ cm}^{-2}$ is found. This density increases after annealing at $1,100^\circ\text{C}$. The growth of MgO- and Sc-based oxides for their use in AlGaN/GaN HEMTs is described in [4.67]. MgO is found to produce lower interface state densities than Sc_2O_3 . However, as a passivation material MgO is found to be degrading stronger than Sc_2O_3 in the annealing steps, which follow the actual passivation procedure. The application of oxides as gate dielectrics in MOSFETs is further discussed below.

Unconventional Dielectric Materials

A great number of more unconventional materials have been investigated for the passivation of III-N devices. They include polyimide (e.g., in [4.79]), low-k Bencocyclobutene (BCB) material passivation (e.g., in [4.267]), and insulators

such as AlN [4.285]. A 4:1 polyimide-to-thinner mixture is spun on the surface of AlGaN/GaN HEMTs and cured at 300°C [4.79]. The effect of polyimide on the surface is attributed to the reduction in surface states and to the low stress of the polyimide on the surface and the nonoccurrence of plasma damage during deposition. The stress considered is lower than 70 MPa. This is an order of magnitude lower than in typical SiN films. Low-k BCB passivation of AlGaN/GaN HEMTs is described in [4.267]. The thickness of the BCB amounts to 400 nm and is compared to a relatively thick Si_3N_4 layer of 300 nm. The inherent advantage of the BCB material is the reduced dielectric constant, the simple deposition, and the lack of deposition damage. The pulsed-DC-characteristics and the RF-output-power-results of BCB-passivated devices are similar to those with Si_3N_4 passivation. The physical nature of the stabilization of the semiconductor surface is not investigated in detail; however, it is found that the degradation of the transconductance and the drain current at 85°C is smaller than that for Si_3N_4 .

The use of insulating materials of the III-N system is another option for surface deposition and, consequently, passivation. The growth of insulating AlN layers for the passivation of AlGaN/GaN HFETs by migration-enhanced epitaxy (MEE) is described in [4.104]. The growth temperature is 150°C with a growth rate of 800 Å h⁻¹. The total AlN thickness is 1,000 Å. AlN has the advantage of high thermal conductivity directly near the heat source. The physical nature of the AlN passivation is attributed to the hardness of the material, which reduces gate-bias-induced stress on the material, as explained in [4.230]. Surface passivation using AlN deposited by reactive magnetron sputtering on both MISFETs and HFETs is described in [4.285]. The thickness of the AlN passivation is 50 nm and it is deposited at a very high processing temperature of 880°C. The AlN passivation reduces both gate leakage and current collapse. Further, the repeatability of the DC measurements is improved for the AlN passivation.

The successful application of unconventional dielectric materials supports the idea that surface preparation prior to deposition has a similar impact on the device performance to that of the actual deposition of the dielectric.

4.6.5 Epitaxial Measures: Surface Preparation and Dielectrics

Being part of the growth process, epitaxial measures are very attractive for solving the issue of dispersion reproducibly already during the growth process. This is especially important for achieving reliability for high-voltage operation [4.127, 4.225]. Typical epitaxial measures involve the introduction of the following

- A highly or medium-n-doped cap [4.128] for high-power transistors without surface passivation [4.225]
- p-Capped GaN/AlGaN/GaN HEMTs [4.47, 4.48]
- AlN as a passivation material [4.104, 4.285]

- Superlattice-based contact approaches [4.196]
- In-situ deposition of SiN as a passivation material [4.104, 4.207]

The n-doped or p-doped GaN capping of AlGaN/GaN HFETs reduces the area of ungated AlGaN surface being exposed to technological treatment during the gate processing and thus the impact of trapping on the device performance. Whether the Schottky gate itself is placed on top of a GaN or an AlGaN surface is subject to the actual process design. Both options exist. Doping of the cap layers modifies the Fermi-level at the interface, as suggested and detailed, e.g., in [4.127]. The nominal doping of the p-doping in [4.47] amounts up to 10^{20} cm^{-3} . N-doping levels of $5 \times 10^{18} \text{ cm}^{-3}$ are reported in [4.225]. Superlattice-based capping approaches allow the precise definition of the Fermi-level at the interface to both the ohmic contact and to the ungated surface, as reported in [4.196]. The density of states near the ohmic contact is increased through the insertion of the highly-doped superlattice layer with 50 nm thickness. This is confirmed by an increase of the transconductance compared to a conventional n-type cap approach. An analysis of the power performance of AlGaN/GaN HEMTs grown by RF-plasma-assisted MBE including in-situ passivation by CVD is given in [4.207]. After MBE growth the samples are in-situ passivated with 4 nm SiN by high temperature CVD to form MISFETs and to reduce gate currents. The devices are then fully passivated by PECVD at 250°C. Similar approaches are used in [4.39].

4.7 Gate Dielectrics

Many publications for III-N FETs refer to the creation of AlGaN/GaN FETs with conventional metal–semiconductor Schottky gate contacts. Metal–insulator (MIS) or metal-oxide-based (MOS)FETs have been repeatedly suggested for the III-N material system, e.g., [4.3, 4.85, 4.94, 4.107, 4.118]. Several materials have been proposed for the insulating gate interfaces. These are discussed in the following sections. A distinction is necessary with respect to the impact of the dielectric to the gated and the ungated region: A dielectric can serve as a gate dielectric in the gated region and similarly in the ungated region, while it may also be useful to use a specific dielectric as a gate dielectric only and deposit a second dielectric for passivation of the ungated region.

Dielectric Materials

Several variations of gate dielectrics have been tested for III-N MISFETs, such as SiN and SiO₂ [4.3, 4.94]. Processing of gate dielectrics of GaN/AlGaN MOS-HFETs by thermal oxidation is reported in [4.107]. A 100 nm-thick Si layer is oxidized at 900°C in dry O₂ for 27–45 min. The resulting oxide thickness is 8–13 nm.

Surface passivation of GaN and GaN/AlGaN heterostructures and gate dielectric formation by dielectric Al₂O₃ and SiN films are reported in [4.85]. The critical defect creation during different plasma processing is discussed. ECR-H₂-treatment produced nitrogen-related vacancies in GaN and AlGaN, while ECR-N₂-treatment improved the surface quality. SiO₂ deposition created uncontrollable oxidation reactions. Further, the conduction band offset of SiN and Al_{0.3}Ga_{0.7}N is considered to be 0.7 eV, which leads to strong gate leakage currents governed by Fowler–Nordheim tunneling.

High-quality oxide/nitride/oxide (SiO₂/Si₃N₄/SiO₂) (ONO) insulator stacks for GaN-MIS structures with similarly low interface densities are presented in [4.65]. The stacks are deposited by jet vapor deposition. With respect to dielectric breakdown and leakage currents, these structures yield promising features. The interface trap density is extremely low and comparable to Si-MOS structures. However, III-N device performance is not provided.

Breakdown investigations of MgO/GaN MOSFETs by simulation are reported in [4.40] based on the assumption of an interface-state density of $3 \times 10^{11} \text{ cm}^{-2}$. RF-plasma-deposited Sc₂O₃ is used as a passivating oxide and gate dielectric in [4.169, 4.170] with typical thicknesses of 40 nm. The influence of the gate-oxide thickness on Sc₂O₃/GaN MOSFETs is investigated in [4.41]. Thicknesses between 10 and 80 nm are investigated by simulation, based in this case on an interface-state density of $5 \times 10^{11} \text{ cm}^{-2}$. The primary advantage found for this oxide is the mitigation of the virtual gate effect due to the low surface-state density and the reduction of the gate leakage.

Similar to silicon devices [4.250], high-k dielectrics are attractive materials to increase charge control in conventional GaN FETs. Several high-k materials have been tested for this purpose. An investigation of barium strontium titanate (BST) serving as a gate dielectric of AlGaN/GaN MOSFETs is reported in [4.80]. The BaSrTiO₃ is a solid-solution and in paraelectric state, which leads to very high dielectric constants (20–500). It is deposited by RF-magnetron sputtering as a gate dielectric with a thickness of 20 nm. This deposition also leads to a damage to the underlying GaN, which requires further investigations.

MISFETs

The principal advantage of metal–insulator–semiconductor (MIS) gate contacts is the reduction of the gate-leakage by orders of magnitude, e.g., [4.107]. This is a principle advantage relative to Schottky gates, especially in the forward direction of a diode. At the same time, the nature of the insulator–semiconductor interface has to be considered, especially also for the ungated region. It is still not fully resolved whether the Fermi-levels at the various dielectric/GaN interfaces are pinned to midgap for at least some of the dielectrics. High interface charge densities and related pinning of the Fermi-level near midgap make GaAs-based power MOSFETs nearly impossible.

Several studies are available for III-N semiconductors. Heterostructure AlGaN/GaN SiN-based MISFETs are reported in [4.46] based on (unstoppable)

RIE etch definition of the gate insulator. A 27 nm gate dielectric passivation layer is deposited early in the process and then etched for gate foot definition. The thickness of the gate dielectric after etching amounts to 18 nm. The RF-output power density achieved with these devices amounts to 4.2 W mm^{-1} at 4 GHz for devices with a gate length $l_g = 600 \text{ nm}$. Very thin SiN gate dielectric layers with a thickness of only 2 nm are reported in [4.94]. The layers are deposited by Cat-CVD using SiH_4 and NH_3 at a temperature of 300°C . Other dielectrics than SiN are used because the low conduction band discontinuity of the $\text{SiN}/\text{Al}_3\text{Ga}_{0.7}\text{N}$ interface is found to be 0.7 eV, while the discontinuity of the $\text{Al}_2\text{O}_3/\text{Al}_3\text{Ga}_{0.7}\text{N}$ interface is reported to be 2.1 eV [4.84]. Al_2O_3 oxide thicknesses as low as 3.5 nm are reported. Because of reduced Fowler–Nordheim tunneling, the leakage for the $\text{SiN}/\text{Al}_3\text{Ga}_{0.7}\text{N}$ interface can be reduced by replacing the SiN gate dielectric with Al_2O_3 .

Sc_2O_3 -based MOS-HEMTs have been reported in [4.170]. The gate leakage can be significantly reduced by 4–5 orders of magnitude depending on the annealing [4.41]. The 400 Å of Sc_2O_3 are grown by RF-PAMBE at 100°C using Sc and O_2 from a plasma source. Good small-signal performance has been reported for Sc_2O_3 -based MOSHEMTs in [4.170].

Very promising output power results are achieved based on GaN/AlGaN MOSHFETs with a 10 nm-thick SiO_2 for a gate length $l_g = 1.1 \mu\text{m}$. The deposition is achieved by PECVD. The second passivation is silicon oxynitride (SiON) with a thickness of 75 nm [4.3].

4.8 Processing for High-Temperature Operation

The specific high-temperature operation of GaN devices is often considered to be an advantage, e.g., [4.138]. Many publications suggest the application of III-N materials for high-temperature device operation, e.g., [4.99, 4.138]. On the one hand, this operation refers to high ambient and substrate temperatures, e.g., in [4.153]; on the other hand, this operation mode is caused by the increased channel- and thus also contact-temperatures at ohmic and Schottky contacts, due to self-heating during high-power operation. At the same time, only relatively few reports exist for principal improvements of the processing to meet high temperature operation; see, e.g., [4.99, 4.155]. The specific technological requirements are discussed in this section. Reliable GaAs-type channel- and substrate-temperatures amount to $\leq 200^\circ\text{C}$. As is also stated in Sect. 7.5, channel temperatures $T_{\text{chan}} \geq 300^\circ\text{C}$ are investigated to meet and extrapolate the reliability FOMs for GaN devices.

WSiN-based ohmic contacts have been suggested in [4.99, 4.100]. WSiN serves as a diffusion barrier for the ohmic contacts to improve the morphology. Different sets of metallizations are fabricated employing Ti/Al/Au metal stacks. The Schottky-contact-stacks are also varied. WSiN/Au and Ir/Au contacts are found to be suitable for high-temperature operation after testing at 400°C for 120 h. The high-temperature stability of various metals and

metal systems is further investigated in [4.209]. Re, Pt, Pd, Au, Ni, Ni/Au, Ni/Ga/Ni, Co, and Co/Au contacts are investigated for 200 h at a temperature of 500°C in N₂ atmosphere. The metals are placed on GaN-capped AlGaN/GaN heterostructures and the contacts are not encapsulated. Pt/Au stacks are found to provide very good thermal stability. Re and Ni/Ga/Ni metal stacks are found suitable for thermally stable Schottky contacts at high temperatures $\geq 400^\circ\text{C}$. Post- and mid-processing full-wafer annealing is an additional processing step to improve and stabilize device performance, as reported, e.g., in [4.155]. The annealing can be performed at several stages of the processing. Annealing of the ohmic contacts is often performed at very high temperatures of $>800^\circ\text{C}$ [4.165]. Thus the material has experienced a high temperature treatment in the early stages of the processing. A full wafer treatment can thus be applied either in the context of the gate processing or after the full process. The post-annealing temperature in [4.155] amounts to 400°C, which is consistent with the high channel temperature of 300°C expected for GaN.

4.9 Backside Processing

Backside or backend processes are required to enable area-efficient grounding of the devices and the use of microstrip transmission-lines. A backend process typically consists of the following process steps:

- Wafer thinning
- Viahole creation by etching or drilling
- Backside metallization and structuring

This sequence is well known and now discussed with respect to III-N substrates and materials.

4.9.1 Thinning Technologies

Typical substrate thicknesses used for epitaxy and frontside processing of III-N devices are thicker (350–650 μm) than the typical substrate thickness required for state-of-the-art devices and passive microstrip transmission-lines (50–150 μm). For a good thermal conductor such as SiC, thinning is not a requirement for thermal reasons, see Chapter 8. However, as the ratio of substrate thickness and transmission-line width defines the impedance for passive MMIC technologies, thinning is a requirement to reach reasonable line widths and overall MMIC sizes comparable to GaAs. For hybrid transistors, there is a benefit in gain, as thinning reduces the source inductance of the devices. This requires the development of a full wafer-scale thinning-technology in order to produce especially MMICs similar to GaAs, e.g., [4.4, 4.256] and references therein. Wafer thinning is typically performed by a combination of the following techniques: grinding, lapping, polishing, wet immersion, and spray etching [4.6].

Sapphire and SiC Substrates

Sapphire and s.i. SiC substrates have been used for both transistor and MMIC processes. Typical substrate thicknesses for through viahole and individual source viaholes amount to 50–100 µm, e.g., [4.125, 4.180, 4.255]. For a small number of processes, thinning of 2- and 3-in. s.i. SiC has been described. A thinning process to a thickness of 50 µm on 3-in. SiC wafers is demonstrated in [4.180]. This process can be used up to Ka-band frequencies, as the via inductance can be minimized to values similar to GaAs [4.240] or InP [4.74], where the minimum substrate thickness is also in the order of 50 µm. The reported inductances based on this thickness amount to 3.25 pH for three parallel round vias with 40 µm diameter. Thinning of full 2-in. wafers to 100 µm for X-band MMICs is reported in [4.255]. The inductance for a single via amounts to 14 pH. Thinning of sapphire substrates to 50 µm has been performed in [4.6]. This thickness is very necessary to reduce the thermal resistance of GaN HFETs on sapphire, as detailed in Chapter 8. The actual thinning process of sapphire is not detailed in [4.6]. However, from a purely mechanical point of view, the lattice mismatch of GaN layers on sapphire is critical, and wafer breakage is a critical issue. Silicon MOS devices on sapphire substrates have been thinned to 30 µm, as reported in [4.87].

Silicon Substrates

Thinning of silicon substrates is a standard technology, which is commonly used, e.g. [4.81]. Thinning of 2 GHz power bar GaN HFETs on silicon substrate to 150 µm (6 mil) thickness is described in [4.81]. A 4-in. full-wafer process is applied. Triquint provided an X-band GaN MMIC process with the thinning of silicon substrate to 125 µm (5 mil) [4.62].

4.9.2 Viahole Etching and Drilling Technologies

Via etching is typically accomplished with highly anisotropic ICP etching. The etching of GaAs substrates yields an etch rate of $2 \mu\text{m min}^{-1}$ for the definition of source vias [4.248]. A value for the etch rate can be found for the dry etching of InP with $0.6 \mu\text{m min}^{-1}$ [4.74].

Etching of SiC and Sapphire

Etching of SiC or sapphire is more difficult; however, it is reported in a number of publications [4.31, 4.32, 4.42, 4.66, 4.125]. Because of the inert properties of SiC and the required aggressive etch techniques, the masking of the vias is of critical importance. Aluminum is used as a mask material in [4.42] to etch SiC by SF₆/O₂ inductively coupled plasma (ICP) etching. The highly anisotropic etch is reached by a high bias voltage and a high source power of 500 W. Ninety seven micrometer-thick features and effective etch rates of 320 nm min^{-1} are reached. The main part of the optimization of the SiC etch process is the

understanding of the etch products, and the removal of the chemical byproducts, as performed by laser-induced fluorescence, e.g., [4.125]. The etch mechanism is either dominated by a more physical sputter process or by a more chemical reaction, thus a good trade-off needs to be found. The addition of O₂ or Cl₂ to the plasma determines the pathway of volatilizing additional C and thus increases the etch rate. Given the chemical inert material, very high etch rates of SiC are reported in [4.31] using an SF₆/O₂ plasma etch. The etch rates exceed 1.3 μm min⁻¹ and allow viaholes into 330 μm thick substrates to be etched. The etch mask used in [4.31, 4.32] is Ni with a selectivity to SiC of about 50:1. The etch conditions are further investigated in [4.32]. Pressure, source power, substrate bias voltage, and the distance between the substrate holder and the source are investigated for an SF₆ helicon plasma for 4H-SiC. A maximum etch rate of 1.35 μm min⁻¹ is achieved. A SiO₂ mask is used for the SF₆/O₂ etch of 3H-SiC substrate in [4.66]. The etch selectivity of SiC over SiO₂ is found to be as low as 2.6. A SF₆/chlorine/O₂ chemistry is used for the etching of 6H-SiC in [4.125]. Again etch rates are reported as a function of pressure, source power, and accelerating bias. Through-viaholes are reached in 140 μm thick substrates with an effective etch rate of 820 nm min⁻¹. Very high coil powers ≥ 500 W and DC-bias ≥ 300 V are applied. The impact of Ar and Cl₂ on the etch is also investigated. Surface roughness after etching is found to be comparable to the SF₆ etch.

Sapphire is a very hard and inert material. Thus very few reports exist on the viahole etching of sapphire substrates. However, sapphire can be structured by aggressive etching techniques, e.g., by BCl₃-based ICP etching [4.112]. Cl₂, HCl, and HBr are added. The etch rate is 380 nm min⁻¹. The etch selectivity to the photoresist used for the mask is very modest. Thus, sapphire is typically removed for optoelectronic LED applications rather than being thinned or structured, e.g., [4.213].

Etching of Silicon

Viahole etching through Si wafers is a standard VLSI technology, e.g., in [4.272]. However, the typical vias in VLSI technology are much smaller than that used for RF-devices. A source-ground-via structure process is described in [4.96] for a full 4-in. process. Conductive substrates are used to connect the frontside vias with the backside metal layer, thus no real through via is etched. The depth of the via is about 20 μm, etched by a Cl₂-plasma-etch. Through-wafer RF-viaholes in silicon substrates with high aspect ratios of 8 and substrates thicknesses of 77 μm are reported in [4.273]. The related inductance amounts to 77 pH for a 4 μm via diameter. The technique is applied in a similar fashion to typical III-V substrate viaholes. The dry etching is performed by ICP-RIE at an etch rate of 2 μm min⁻¹. The aspect ratio can be increased to 49:1.

Viahole Drilling Technologies

Apart from viahole dry-etching, laser drilling technologies have been developed [4.146, 4.202]. Such microprocessing is very attractive to structure very hard and inert materials especially for unthinned substrates. They further simplify the process by reducing the number of processing steps.

The process promises consecutive definition of high-aspect-ratio viaholes in SiC and sapphire substrates. A Q-switch Nd:YAG laser is used applying scanning optics in [4.146] at a repetition of 10 kHz. Investigations of the drilling parameters for CO₂ lasers are given in [4.134]. A Q-switched CO₂ laser is used for the drilling procedure. Using a typical repetition rate of 8 Hz, an etch rate between 230 and 870 μm min⁻¹ is reported, with pulse energies of 60 mJ per pulse. The issues of the drilling include the removal of ionized debris, depth and geometry control, and a reduction of the residual surface contamination. Another full process is reported in [4.167]. A diode-pumped solid-state laser at 355 nm is used with a spot size of 15 μm. Typical pulse energies are 65 μJ per pulse at a pulse repetition rate of 20 kHz. The actual via diameter is 100 μm. The thickness of the gold plating is 5 μm. Drilling of viaholes into 100 μm thick sapphire substrates is reported in [4.251]. The concentric viaholes are filled with gold and serve as thermal vias to reduce the thermal resistance.

4.9.3 Viahole Metallization

Galvanic and metal processing of GaN RF-devices is a standard technology. Specific optimization is required with respect to the high-power and high-voltage operation. Several complete front- and backside high-voltage III-N processes have been demonstrated [4.114, 4.222]. A 5 μm-thick electroplated galvanic metal is used for the backside metal in a process devoted to power switching applications [4.96]. Devices with very high current levels of 150 A are interconnected. Similar metallization thicknesses have been used for III-N devices, e.g., a galvanic thickness of 4 μm in [4.81] for RF-power bar devices. Such galvanic thickness at the backside is similar to those typically performed in GaAs power processes [4.44, 4.88, 4.286]. Backside metal thicknesses of 4, 7, and 10 μm are reported even for 6-in. diameters and very thin GaAs wafers of 1 mil (25 μm) [4.44]. The associated stress of the wafers is found to be equal for all metal thicknesses, while the absolute wafer bow increases with the thickness for GaAs wafers. The differences in the CTE of galvanic metals and passivation layers is found to be a cause for reliability concerns of GaN HEMTs on 3-in. s.i. SiC substrates [4.270]. Aspects of all processing steps of frontside and backside technology have been discussed in this chapter. Further considerations are given in Chaps. 7 and 8 with respect to dicing [4.88], reliability, packaging, and integration.

4.10 *Problems*

1. *Describe why GaN FETs are very sensitive to frequency dispersion!*
2. *Discuss the issues of the formation of Ohmic contacts to III-N semiconductors!*
3. *Describe the differences in etching methodologies between GaAs and GaN!*
4. *Discuss the critical processing steps of device passivation!*
5. *Summarize the most important trapping mechanisms in GaN FETs!*
6. *Describe the fundamental problems when processing an AlGaN/GaN npn-HBT!*
7. *Describe the issues of lithography for III-N devices!*
8. *Describe the alternatives for field-plate definition!*
9. *Clarify advantages and drawbacks of recess processes in GaN!*

Device Characterization and Modeling

In this chapter, device modeling and characterization are presented with respect to nitride-specific issues. DC, RF-small-signal, and noise-characterization and modeling are discussed. Further, since frequency dispersion is a major source of performance- and device-degradation, the characterization and analysis of dispersion are discussed. This includes pulsed-characterization and other advanced techniques. Furthermore, large-signal characterization and modeling are discussed for nitride devices, such as the modeling of contacts, diodes, dispersion, and thermal aspects. Last, but not least, the modeling and characterization of linearity of devices are presented.

5.1 Device Characteristics

Device-terminal quantities, such as currents and voltages, and derived quantities, such as transconductance and conductances, are the most accessible device characteristics used for the evaluation of their performance. In the case of III-N devices, continuous-wave (cw) measurements can also be most misleading for performance evaluation, as frequency dispersion plays a dominant role in the functioning of III-N devices for power and RF-applications. Additional measurements and characterization are thus required. In the following, basic device properties will be evaluated as seen from a number of characterization and modeling perspectives.

5.1.1 Compact FET Analysis

Approximation of the DC-Quantities

Several device models are available from the analysis of silicon and GaAs FETs, which will be used in this work for the evaluation of GaN FETs. First of all, AlGaN/GaN HEMTs are dominated by their high sheet-carrier densities in the channel of 10^{13} cm^{-2} and above. A calculation example of threshold

Table 5.1. Typical parameters for the calculation of the threshold voltage for an Al_{0.3}Ga_{0.7}N/GaN HFET with $l_g = 300$ nm

N_D (cm ⁻³)	d_{doping} (nm)	ϕ_B (eV)	ΔE_C (eV)	E_{f1} (eV)	$\frac{q\sigma}{\epsilon} d_{\text{gc}}$ (V)	V_{p2} (V)	V_{thr} (V)
1e19	10	0.8	0.68	0.026	4.98	1.84	-6.5
$(x = 0.3)$							
ϵ_r (-)	v_{eff} (cm s ⁻¹)	d_{eff} (nm)	C_0 (pF mm ⁻¹)	E_{crit} (kV cm ⁻¹)	n_c (cm ⁻²)	n_{sheet} (cm ⁻²)	$g_{m,\text{max}}$ (mS mm ⁻¹)
9.8	2.7e7	27	1	150	3e6	1e13	235
ΔV (V)	t (nm)	LD (nm)	$I_{D\text{max}}$ (mA mm ⁻¹)				
10	2.7	27	1,734				

voltage V_{thr} in a classical model of a short-channel pulse-doped FET can be performed according to [5.103, 5.149, 5.151] including surface charge correction

$$V_{\text{thr}} = \frac{1}{q} \left(\phi_B - \Delta E_C - V_{p2} - \frac{q\sigma}{\epsilon} d_{\text{gc}} + E_{f1} \right). \quad (5.1)$$

ϕ_B denotes the intrinsic Schottky barrier height, ΔE_C is the conduction band discontinuity, σ the surface charge density, and E_{f1} denotes a small correction energy. The doping correction V_{p2} is calculated according to

$$V_{p2} = \frac{q \cdot N_D \cdot d_{\text{doping}}^2}{2 \cdot \epsilon}. \quad (5.2)$$

ϵ is the dielectric constant of the barrier layer, N_D originally is the donor concentration in the AlGaN layer [5.169], and d_{doping} originally is the channel thickness width. The model is based on a MESFET device with a homogenous doping of concentration N_D and a channel thickness d_{doping} . The model needs modification with respect to the polarization charge, as a significant amount of carriers is not generated by impurity doping. Further, the carriers in III-N HFETs are concentrated in a very small channel depth and not in the barrier. A typical example is given here. The idea of this calculation is based on the fact that the complete channel charge density n_c arises from barrier doping and surface charge at a gate-to-channel separation d_{gc} of 27 nm. The calculated threshold voltage is $V_{\text{thr}} = -6.5$ V with the influence of the polarization doping. It is visible in Table 5.1 that an enhancement-mode AlGaN/GaN HFET is difficult to realize. However, examples of the realization are given in [5.31, 5.94]. For the maximum transconductance $g_{m,\text{max}}$, a similar calcula-

tion example can be performed:

$$g_{m,\max} = \frac{\partial I_{DS}}{\partial V_{GS}}|_{V_{DS}=\text{const.}} \approx \frac{\epsilon \cdot v_{\text{eff}} \cdot W_g}{d_{\text{eff}}} \cdot \frac{1}{\sqrt{1 + \left(\frac{n_c}{n_{\text{sheet}}}\right)^2}}. \quad (5.3)$$

n_c is defined as

$$n_c = \frac{E_{\text{crit}} \cdot l_g \cdot C_0}{q}. \quad (5.4)$$

The critical field E_{crit} is the field for the onset of saturation and C_0 is the static capacitance. An approximation for the static capacitance C_0 is given below. Deduced from (5.3), a maximum transconductance of 235 mS mm^{-1} is found, which is in good agreement with typical AlGaN/GaN HFETs. Fig. 5.1 gives the measured transconductance g_m as a function of V_{GS} for a real device. A threshold voltage $V_{\text{thr}} = -4.5 \text{ V}$, which increases for increasing V_{DS} , is observed by the linear extrapolation method. The maximum DC-transconductance amounts to 300 mS mm^{-1} and is relatively independent of the V_{DS} voltage. The maximum theoretical drain current $I_{D\max}$ can be calculated in a space-charge-zone limited model according to [5.88]

$$I_{D\max} = \frac{2 \cdot \epsilon_r \cdot \epsilon_0 \cdot v_{\text{eff}} \cdot \Delta V}{L_D^2} \cdot W_g \cdot t. \quad (5.5)$$

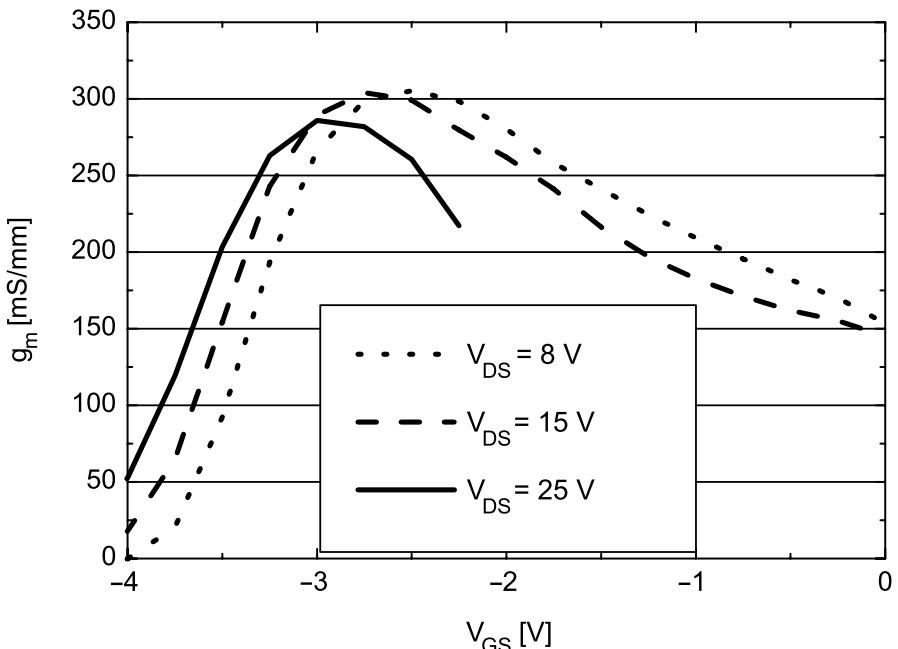


Fig. 5.1. Transconductance g_m as a function of V_{GS} with V_{DS} as a parameter for an AlGaN/GaN HEMT with $W_g = 2 \times 60 \mu\text{m}$ and $l_g = 150 \text{ nm}$

Apart from the material constants, v_{eff} denotes the effective saturation velocity of the majority carriers, and ΔV the voltage drop over the depletion zone in the drain region. W_g denotes the gate width and t the effective thickness of the layer that supports the current. L_D is the effective depletion zone length. Deduced from this, a maximum drain current of $1,734 \text{ mA mm}^{-1}$ can be calculated, if the depletion zone L_D is assumed to be 27 nm for a voltage drop $\Delta V = 10 \text{ V}$. The layer thickness t is assumed to be 2.7 nm in agreement with Schrödinger–Poisson calculations, e.g., [5.158]. Fig. 5.2 gives the output characteristics of a GaN/AlGaN HEMT on s.i. SiC substrate measured in cw-mode up to $V_{DS} = 35 \text{ V}$ in comparison to a GaAs HEMT of the same gate width $W_g = 1 \text{ mm}$. The gate length is $l_g = 300 \text{ nm}$ in both cases similar to the example in Table 5.1. The GaN/AlGaN HEMT yields higher current, higher breakdown voltage, lower transconductance, reduced thermal effects for the same power density, and higher on-resistance and knee-voltage than the optimized GaAs device. The on-resistance R_{on} in a GaN HEMT can be rewritten as

$$R_{\text{on}} = R_S + R_D + R_{\text{chan}}, \quad (5.6)$$

where R_S and R_D denote source and drain resistances and R_{chan} the channel resistance. For III-N HEMTs, the DC-approximation of (5.6) may be critical, as the measured contribution of $R_S + R_D$ alone may leave no contribu-

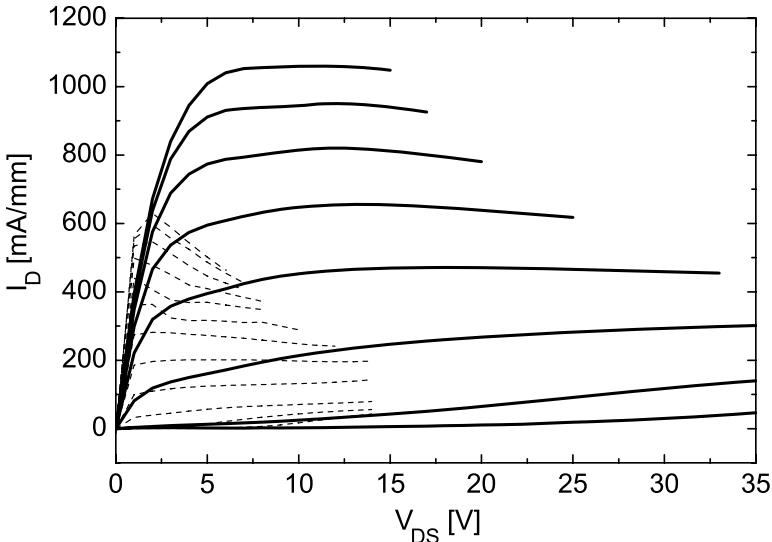


Fig. 5.2. CW-output characteristics of an AlGaN/GaN HEMT with $V_{GS} = 2 \text{ V}$, step -1 V) as a parameter compared to GaAs PHEMT output characteristics (step 0.2 V), gate width $W_g = 1 \text{ mm}$ and gate length $l_g = 300 \text{ nm}$

tion to R_{chan} . The DC-output conductance $g_{\text{ds,ext}}$, also depicted in Fig. 5.2, is defined as

$$g_{\text{ds,ext}} = \frac{\partial I_{\text{DS}}}{\partial V_{\text{DS}}} \Big|_{V_{\text{GS}}=\text{const.}} \quad (5.7)$$

A typical approximation of the open-channel contribution to g_{ds} is

$$g_{\text{ds}} = \frac{q \cdot \mu \cdot n_{\text{sheet}} \cdot W_{\text{g}}}{l_{\text{g}}} \quad (5.8)$$

Deviations from the cw-values, calculated from (5.6) and (5.7), occur both during pulsed- and RF-operation. The impact of trapping is of significant importance, so that

$$g_{\text{ds,ext}}(\text{CW}) \neq g_{\text{ds,ext}}(\text{RF}) \neq g_{\text{ds,ext}}(\text{Pulsed}). \quad (5.9)$$

Equation (5.9) holds in similar fashion for the transconductance. Further below, the importance of additional derivatives will be considered.

Modeling the Resistances in an HFET

The source-resistances in HFETs can be modeled according to

$$R_{\text{S}} = R_{\text{S,semi}} + R_{\text{Con}} + R_{\text{S,met}} + R_{\text{band}}. \quad (5.10)$$

A similar model holds for the drain resistance R_{D} :

$$R_{\text{D}} = R_{\text{D,semi}} + R_{\text{Con}} + R_{\text{D,met}} + R_{\text{band}}. \quad (5.11)$$

The contributions of $R_{\text{D,semi}}$ and $R_{\text{D,met}}$ denote the ohmic contributions of the metal and the semiconductor. R_{Con} denotes the contact resistance of the semiconductor/metal transition. The principal difference between GaAs- and GaN-devices in this modeling approach are the band contribution R_{band} at the source, due to the increased bandgap discontinuity and the resulting additional resistive contributions. This is investigated particularly in [5.184]. The influence of the dynamic access-resistances in AlGaN/GaN FETs with regard to the linearity of the transconductance g_{m} and the cut-off frequency f_{T} has been discussed further in [5.131]. The increase of R_{S} is considered to occur due to the quasi-saturation of the electron velocity in the source region of the channel. The impact of the nonlinear source resistance is confirmed at low temperatures down to 120 K [5.126]. Similar investigations with respect to the nonlinear source resistance can be found in [5.131]. The nonlinear source resistance is due to space-charge limited current conditions. A critical current density of about 40 MA cm^{-2} is isolated. For current densities beyond that value, the resistance R_{S} increases critically.

Approximation of the Small-Signal RF-Quantities

Several definitions and approximations hold for the calculation of the cut-off frequencies and related quantities. f_T is defined and approximated as

$$f_T = f(h_{21}(f) = 0) \approx \frac{g_{mi}}{C_g}. \quad (5.12)$$

C_g denotes the total gate capacitance. Physical approximations of the intrinsic RF-transconductance are similar to those of the DC-transconductance. Dispersion effects are not considered in these first order approximations. The channel capacitance C_g for the short-channel MODFET can be approximated by several bias-dependent models, for example, as given in [5.151, 5.169]. A static approximation of the intrinsic gate capacitance yields [5.151]

$$C_0 = q \cdot K \cdot W_g \cdot l_g = \frac{\epsilon \cdot W_g \cdot l_g}{d_{gc}}. \quad (5.13)$$

Based on the values in Table 5.1, a value $C_0 = 0.964 \text{ pF mm}^{-1}$ is found. In (5.13), d_{gc} denotes the separation of the physical gate to the channel layer. For GaN HFETs, this is a very well defined quantity as the vertical extension of the electron gas amounts to a few nanometer only. This value then needs modification with respect to the bias dependence.

Approximation of Large-Signal RF-Quantities

Many small-signal models exist for the approximation of the small-signal behavior of FETs. However, for large-signal operation, only a few basic approximation concepts exist. The output power P_{sat} of an RF-device can be approximated as

$$P_{\text{sat}} \approx \frac{\Delta I_D \cdot \Delta V_D}{8} = \frac{(I_{D,\text{max,RF}} - I_{D,\text{min,RF}}) \cdot (V_{D,\text{max,RF}} - V_{D,\text{min,RF}})}{8}, \quad (5.14)$$

where ΔI_D is the drain current during RF-swing and ΔV_D is the drain voltage RF-swing. This approximation does not consider nonlinear operation with the generation of harmonics. In first order the swing values are taken from pure DC-considerations. More elaborate investigations can be found in [5.116]. The dispersive effect of a knee walk-out is quantified by RF-swing and pulsed-DC-measurements. Deduced from the maximum drain current from $I_{D,\text{max}}$ in (5.5), the DC-knee voltage $V_{\text{knee}} = V_{D,\text{min}}$ is defined by the crossing of $I_{D,\text{max}}$ and R_{on} for $R_{\text{chan}} = 0$. There are no simple approximations for the definition of $V_{D,\text{max}}$ and $I_{D,\text{min}}$, once the devices are dispersive, i.e., once:

$$I_{D,\text{max,DC}} \neq I_{D,\text{max,RF}}, \quad (5.15)$$

$$V_{D,\text{min,DC}} \neq V_{D,\text{min,RF}}, \quad (5.16)$$

$$I_{D,\text{min,DC}} \neq I_{D,\text{min,RF}}, \quad (5.17)$$

$$V_{D,\text{max,DC}} \neq V_{D,\text{max,RF}}. \quad (5.18)$$

The first two relations (5.15) and (5.16) are typically considered as the knee walkout. A similar effect is found for high V_{DS} and low I_{DS} ((5.17)–(5.18)), typically considered poor RF-pinch-off. Fig. 5.3 gives an estimate of the possible saturated output power as a function of operation bias V_{DS} , assuming $I_{D,min} = 0$ and $V_{D,max} = 2 \times V_{D,op}$. It is clear from (5.14) that an increase of the knee voltage and a current reduction reduce the saturated output power. Fig. 5.3 gives the calculated values for operating voltages up to $V_{DS} = 150$ V for various knee-voltage and drain current combinations. The output power densities are given without additional thermal and reliability considerations. The power-added efficiency (PAE) is defined as

$$\text{PAE} = \frac{P_{\text{out}} - P_{\text{in}}}{P_{\text{DC}}} = \left(1 - \frac{1}{G_p}\right) \cdot \frac{P_{\text{out}}}{P_{\text{DC}}}. \quad (5.19)$$

The drain efficiency η_d is defined as

$$\eta_d = \frac{P_{\text{out}}}{P_{\text{DC}}}. \quad (5.20)$$

Approximations for the efficiency η_d can be derived from (5.14)

$$\eta_d = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{\left(I_{D,\text{max,RF}} - I_{D,\text{min,RF}}\right) \cdot \left(V_{D,\text{max,RF}} - V_{D,\text{min,RF}}\right)}{8 \cdot I_{DC} \cdot V_{DS}}. \quad (5.21)$$

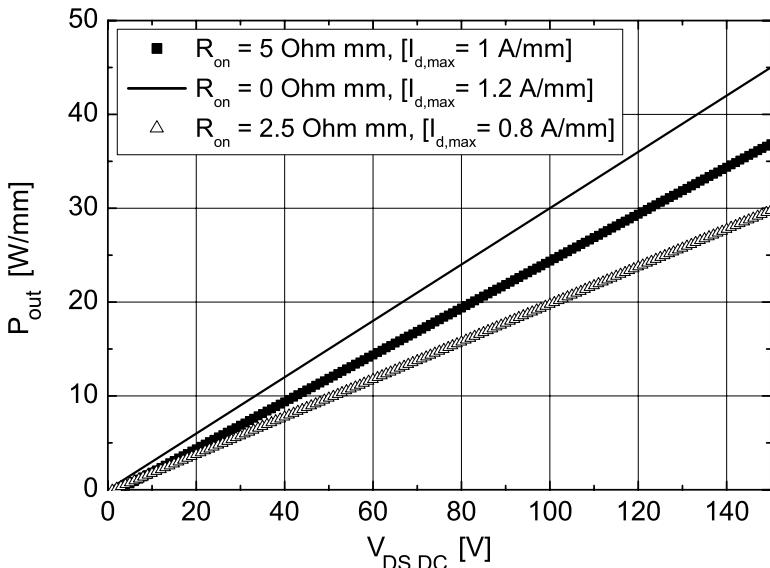


Fig. 5.3. RF output power estimate for different on-resistances and maximum drain current levels

The approximation of the efficiency depends strongly on the class of operation of the amplifier. However, if for class-A operation the relations $I_{DC} = (I_{D,max,RF} - I_{D,min,RF})/2$ and $V_{DS} = (V_{D,max,RF} - V_{D,min,RF})/2$ hold, (5.21) can be rewritten in a theoretical maximum:

$$\eta_d = \frac{1}{2}. \quad (5.22)$$

The impact of the minimum currents and of the knee voltage can be viewed if we assume $I_{D,max,RF} = 2I_{DC}$ and $V_{D,max,RF} = 2V_{DS}$:

$$\eta_d = \frac{1}{2} \cdot \left(1 - \frac{V_{D,min,RF}}{V_{DS}}\right) \cdot \left(1 - \frac{I_{D,min,RF}}{I_{DC}}\right). \quad (5.23)$$

The relative impact of the minimum voltages and currents on η_d becomes visible in (5.23). For III-N HEMTs, the high operation bias becomes favorable to mitigate the relative impact of the knee voltage in this equation. For other operation classes, the impact of the nonideal characteristics is even stronger, as the effect of nonideal pinch-off at high V_{DS} becomes more important, e.g., in class-B or class-F operation.

Characterization of Device Linearity

For the characterization of the linear operation of devices, no approximation for the third-order intermodulation product IM_3 can be given based on purely physical parameters. However, in a very simple model [5.136], some basic understanding can be obtained. The intrinsic drain–source current i_{ds} in a (MES)FET device can be rewritten as a function of the intrinsic bias

$$i_{ds} = \left[v_{gs} + \frac{g'_m}{2} v_{gs}^2 + \frac{g''_m}{6} v_{gs}^3 \right] + \left[v_{ds} + \frac{g'_{ds}}{2} v_{ds}^2 + \frac{g''_{ds}}{6} v_{ds}^3 \right]. \quad (5.24)$$

The derivative g'_m denotes $\partial g_m / \partial v_{gs}$ and g'_{ds} denotes $\partial g_{ds} / \partial v_{ds}$. Some very simple calculations show that the optimum load-resistance to cancel the second-order distortion amounts to

$$\frac{1}{R} = g_m \cdot \sqrt{\frac{-g'_{ds}}{g'_m}} - g_{ds}. \quad (5.25)$$

The third-order distortion terms cancel out for

$$\frac{1}{R} = g_m \cdot \sqrt[3]{\frac{-g''_{ds}}{g''_m}} - g_{ds}. \quad (5.26)$$

This simple calculation shows the importance of the derivatives of both conductances and of understanding them with respect to the matching of the

device. As is seen in (5.7) and (5.27), frequency dispersive effects can be formulated in a very general fashion:

$$\frac{\partial^n I_{ij}}{\partial V_{kl}^n}(\text{DC}) \neq \frac{\partial^n I_{ij}}{\partial V_{kl}^n}(\text{RF}) \neq \frac{\partial^n I_{ij}}{\partial V_{kl}^n}(\text{Pulsed}). \quad (5.27)$$

The indices i, j, k, l denote the various combinations of the ports of the three-terminal devices. The impact of dispersion on these higher order derivatives has not been exploited in detail so far. However, measurement approaches for the optimum determination of the RF-output loads up to 40 GHz with respect to linearity are available, e.g., for GaAs PHEMTs, GaN HEMTs, and Silicon LDMOS in [5.117, 5.119, 5.203].

Temperature Dependence of cw-DC-Characteristics

Temperature effects modify the device terminal characteristics. Fig. 5.4 gives the substrate-temperature-dependence of the output characteristics of an AlGaN/GaN HEMT on s.i. SiC substrate. The following thermal effects can be observed with rising substrate temperature T_{sub} and channel temperature T_{chan} :

- An increase of the on-resistance R_{on}
- A decrease of the output conductance g_{ds} for most of the $(V_{\text{DS}}, V_{\text{GS}})$ combinations, especially for high V_{GS}
- A reduction of the maximum current I_{Dmax}

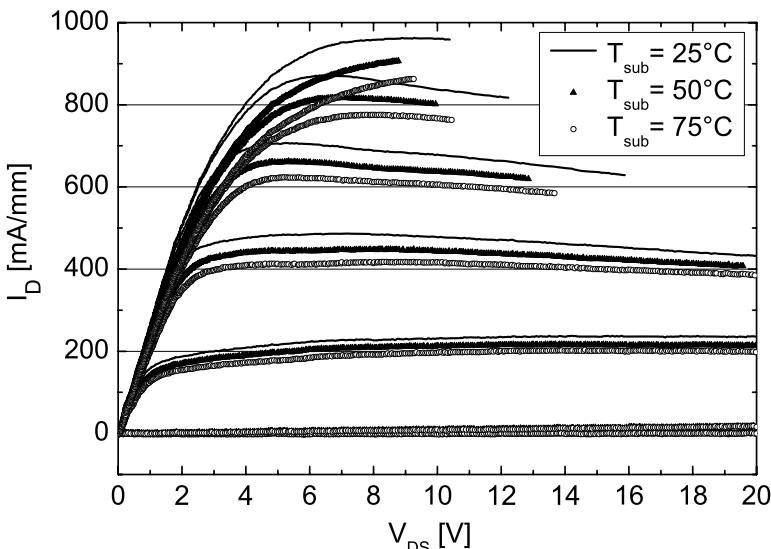


Fig. 5.4. CW-output characteristics with the substrate temperature T_{sub} as a parameter, $V_{\text{GS}} = 1 \text{ V}$, step -1 V

Apart from the reduction of the maximum currents $I_{D\max}$, the currents I_D are reduced also for lower V_{GS} branches, as shown in Fig. 5.4. This reduction in current for lower V_{GS} is not always the case, and is mostly dependent on the impact of trapping effects. The thermal impact on the maximum drain current $I_{D\max}$ in Fig. 5.4 can be approximated by a linear temperature dependence:

$$I_{D\max}(T) = I_{D\max}(T = 300 \text{ K}) \cdot (1 - \alpha \cdot T). \quad (5.28)$$

Similar coefficients are found for the transconductance g_m . The coefficients α are typically of the order of 10^{-3} K^{-1} . Further details are given in Chapter 8.

HFET Input Characteristics

Fig. 5.5 gives the input characteristics, i.e., $I_G(V_{GS})$ of an AlGaN/GaN HEMT on s.i. SiC with a gate width $W_g = 0.48 \text{ mm}$ for various V_{DS} voltages. The input characteristics are determined by the diode-like behavior. Any occurrence of channel impact-ionization is not visible in Fig. 5.5; however, impact ionization has been reported for GaN HFETs [5.24], especially at cryogenic

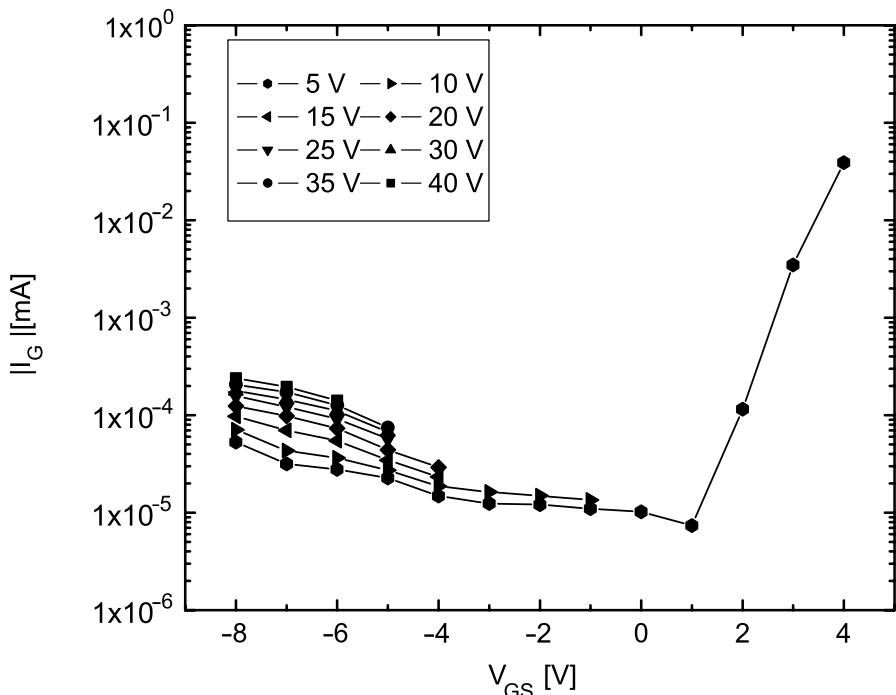


Fig. 5.5. Input characteristics of an AlGaN/GaN HEMT with $W_g = 0.48 \text{ mm}$ for various V_{DS} voltages

temperatures [5.175]. Additional ohmic contributions are visible in Fig. 5.5. The forward diode behavior is normally modeled according to

$$I_G(V_{GS}) = I_0 \cdot \left(\exp\left(\frac{n \cdot V_{GS}}{k_B T_L}\right) - 1 \right). \quad (5.29)$$

n defines the ideality factor, which expresses the deviation from ideal exponential diode-type characteristics. The ideal diode case is $n = 1$. Because of the lack of maturity of the III-N FET diodes, very high ideality factors >2 have been reported initially [5.198], which were then optimized to levels of ≤ 1.5 [5.80].

FET Breakdown Voltage

Although III-N devices are considered for very high voltage operation, breakdown voltages and their mechanisms are still under discussion, e.g., [5.205]. Very high bias of operation are reported; however, the DC-two- and three-terminal breakdown voltages do not match the RF-operation. Very careful optimization of the DC-breakdown voltages for RF-GaN FETs beyond 300 V is reported in [5.127]. The procedure is completed by testing the breakdown voltages also at elevated temperatures [5.83].

Very high operation and breakdown voltages ≥ 900 V for power devices have been reported [5.84, 5.207]. This breakdown voltage is based on the drain current evaluation in dynamic three-terminal curve tracer measurements. The general mismatch of DC- and RF-breakdown is partly due to the high amount of traps in the epitaxial layers. The impact of the drain-to-source spacing of AlGaN/GaN transistors' breakdown characteristics in a trade-off with frequency response is discussed, e.g., in [5.193]. The current gain cut-off frequency increases with the reduction of the source-to-drain spacing, while the BV_{DS} breakdown voltage decreases. Different methods to measure breakdown voltages are available. Gate-to-source (BV_{GS}) and gate-to-drain (BV_{GD}) breakdown voltages are evaluated as

$$BV_{GD\ 2T} = V_{GD}|I_G = (1 \text{ mA mm}^{-1}), \quad (5.30)$$

$$BV_{GS\ 2T} = V_{GS}|I_G = (1 \text{ mA mm}^{-1}). \quad (5.31)$$

Typically, the two-terminal breakdown criterion for the gate current in GaN/AlGaN FETs is $I_G = 1 \text{ mA mm}^{-1}$, 0.1 mA mm^{-1} , or even lower. Fig. 5.6 gives the two-terminal breakdown voltages BV_{GS} and BV_{GD} for two types of AlGaN/GaN HFETs as a function of the gate-to-drain spacing l_{gd} . The difference in the two types of HEMTs is due to the barrier doping concentration and the gate length l_g . As a reference, the dependence of the gate–source diode breakdown on the gate–drain distance is also monitored. We see the

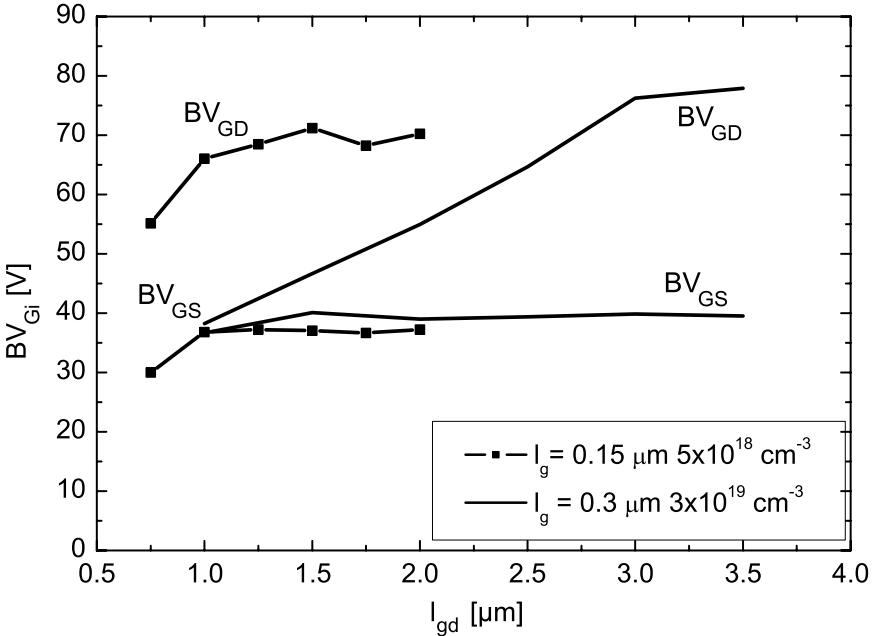


Fig. 5.6. Breakdown voltages BV_{GS} and BV_{GD} for two types of AlGaN/GaN HFETs as a function of gate–drain spacing l_{gd}

impact of both the gate length and of the barrier doping. A three-terminal version of the gate-to-drain breakdown voltage reads:

$$BV_{GD\ 3T} = V_{GD}|I_G = (1\text{ mA mm}^{-1}) \& V_{GS@\text{Pinch-off}}. \quad (5.32)$$

The three-terminal breakdown voltage BV_{DS} can be derived from

$$BV_{DS\ 3T} = V_{DS} \text{ for } I_{DS} \leq (1\text{ mA mm}^{-1}) \& V_{GS@\text{Pinch-off}}. \quad (5.33)$$

Further characterization methods involve dynamic curve tracer analysis [5.207], i.e., a dynamic or pulsed-type of analysis, typically of BV_{DS} , see (5.33). Beyond BV_{DS} , a sharp increase of the drain current I_D is used as a criterion [5.207]. For RF-large-signal operation, $BV_{DS\ RF}$ can be extracted from the direct measurement of the RF-output swing, as performed, e.g., in [5.116]. The dynamic limitation of the swing can be used directly to evaluate the maximum swing possible for the particular operation bias, frequency, and RF-loading of fundamental and harmonic frequencies [5.117]. Assuming the channel being the most sensitive part of the device, and assuming the breakdown field of GaN to be 3 MV cm^{-1} , we obtain a maximum breakdown voltage of 300 V per μm contact separation. This upper limit assumes a homogenous field distribution between the contacts. This maximum value is naturally reduced by the highly inhomogeneous field distribution, traps,

and the impact of interfaces and doping along the channel. In reality, values up to $80 \text{ V } \mu\text{m}^{-1}$ have been reported [5.112]. In this context the stability of the breakdown measurement in a dynamic sense is of critical importance, as the device is biased in a critical situation. Thus the timing of the breakdown measurements needs to be chosen carefully to ensure repeatable measurement results [5.102].

5.1.2 Compact Bipolar Analysis

Calculation of the DC-Quantities

Principal DC-considerations are available for III-N bipolar devices. They resemble the well known relations of GaAs and InP HBTs, e.g., [5.151, 5.169]. The typical obstacles observed for the realization of low base-resistance GaN/AlGaN HBTs are compiled in [5.208]. The high extrinsic base resistance is a fundamental problem. The base resistance R_{bb} can be approximated by [5.150]

$$R_{bb} = R_{Con} + R_{spread} + R_{gap}, \quad (5.34)$$

$$R_{Con} = \sqrt{\rho_s \cdot \rho_c} / 2 \cdot L_e, \quad (5.35)$$

$$R_{spread} = \rho_s W_e / 12 \cdot L_e, \quad (5.36)$$

$$R_{gap} = \rho_s W_{eb} / 2 \cdot L_e. \quad (5.37)$$

R_{Con} is the contact resistance, R_{spread} is the spreading resistance under the base, and R_{gap} is the base-emitter gap resistance. As seen in (5.35)–(5.37) all three components are high due to the high base resistivity ρ_s of p-doped GaN. ρ_c is the specific metal resistivity. For the current amplification β , the following calculations are often used. The common-emitter current gain

$$\beta = \frac{I_C}{I_B} \quad (5.38)$$

relates to the common base gain α as

$$\alpha = \frac{1}{\frac{1}{\beta} - 1}. \quad (5.39)$$

For the common base gain α , the following approximation is used for AlGaN/GaN HBTs [5.114]. α is rewritten to be composed as

$$\alpha = \gamma_i \cdot \delta \cdot \alpha_T. \quad (5.40)$$

Equation (5.40) includes the three factors: emitter injection efficiency γ_i , the recombination factor δ in the emitter base junction, and the base transport factor α_T . The recombination in Mg-doped GaN is high and the transport factor α_T low. A similar calculation of the respective quantities is given in [5.114],

derived from [5.107]. The high base resistance in (5.34) leads to a strong reduction of the extrinsic current gain due to the relation

$$\beta_{\text{extr}} = \frac{I_C}{I_{B,p}} = \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \cdot \exp\left(\frac{\Delta E_V}{k_B T}\right). \quad (5.41)$$

X_E and X_B denote the thicknesses of the base and emitter layer, N_E and N_B the carrier concentrations, and D_{nB} the diffusivities of electrons in base and D_{pE} of holes in the emitter. The impact of both the high Mg-concentration leading to reduced carrier lifetime and low diffusivity of electrons in a highly Mg-doped base is visible from (5.41). The open-collector breakdown voltage of a bipolar transistor can be approximated [5.177], as stated for AlGaN/GaN npn-HBTs in [5.97]:

$$BV_{\text{CEO}} = \frac{\varepsilon_r E_{\text{crit}}}{2qN_{\text{DC}}} \cdot (1 - \alpha)^{1/mb}. \quad (5.42)$$

E_{crit} is the breakdown field of the GaN, N_{DC} is the donor concentration in the collector, and mb is a coefficient for the doping profiling in the collector. Dynamically measured collector-emitter breakdown voltages BV_{CEO} using curve-tracer measurements of 330 V in AlGaN/GaN HBTs have been reported [5.206].

Calculation of the Bipolar RF-Quantities

Only very few reports exist for the RF-analysis of III-N HBTs [5.36, 5.115]. For the current gain cut-off frequency f_T of HBTs a relation is used [5.96] similar to FETs:

$$f_T = \frac{1}{2\pi(\tau_e + \tau_b + \tau_c)} = \frac{g_m}{2\pi \cdot (C_{je} + C_{jc})}. \quad (5.43)$$

For the maximum frequency of oscillation f_{max} , the following approximation is given for bipolar devices based on f_T :

$$f_{\text{max}} = \sqrt{\frac{f_T}{8\pi \cdot R_{bb} \cdot C_{jc}}}. \quad (5.44)$$

This well-known relation again stresses the need to reduce the base sheet resistance in AlGaN/GaN HBTs. At the same time, the base resistance R_{bb} in III-N npn-transistors is comparably high. A distributed small-signal modeling of the base resistance is thus proposed in [5.115]. The model uses a distributed collector-base element-circuit, which is repeated for 25 times in order to model both capacitances and RF-amplification. Further, a transit-time-analysis in InGaN/GaN DHBTs and AlGaN/GaN HBTs is given in [5.36]. It is found that the emitter-transit-time τ_e dominates for collector current densities of $\leq 100 \text{ A cm}^{-2}$, while τ_b dominates beyond that density.

5.2 Frequency Dispersion

The continuous increase of the probing frequency from near DC to the GHz range reveals the most important effects for III-N semiconductor devices. The spectral effects observed between 1 Hz and a few gigahertz are referred to as frequency dispersion.

5.2.1 Dispersion Effects and Characterization

A large number of publications has stressed the impact of frequency dispersion on device performance [5.87, 5.120, 5.195], as is also stated in Chapter 4. The principal terminal effects of frequency dispersion have been discussed in Sect. 2.3.3 and Chapter 4.

Dispersive Effects

The characterization of frequency dispersion on the device-terminal level includes various advanced techniques, such as the following:

- Transient current measurements [5.87]
- cw-current measurements under different optical illumination conditions [5.122]
- Low-frequency excess noise measurements [5.157]
- Pulsed-IV measurements [5.120]
- Pulsed-RF S-parameter measurements [5.87]
- cw-power measurements [5.120]
- Pulsed-power and loadpull measurements [5.22]
- Power measurements under varying terminal load conditions [5.88]

The results of such measurements have been repeatedly reported.

- Strong transients in the current characteristics of GaN-based heterostructure FETs in the time-domain, as are given, e.g., in [5.87].
- The suppression of the DC-current collapse by light illumination with light energy smaller than bandgap energy is described in [5.122]. It shows the principal influence of defects and traps on the cw-device output characteristics.
- The influence of both the ungated device region and the surface states on $1/f$ -noise is described in [5.194]. The main contribution of the excess noise is derived from the ungated region of the FET.
- In [5.46], a concise comparison of the drain excess noise in AlGaN/GaN HEMTs grown on silicon, SiC, and sapphire is given. The normalized low-frequency noise levels are strongly correlated with the leakage currents. The noise is found to stem from a source in the vicinity of the gate.
- Pulsed-DC-measurements reveal the effects of surface traps on the breakdown voltage and switching speed of GaN power switching HEMTs, as reported in [5.211]. The carrier trapping and detrapping is correlated with

the carrier injection time into the device. Trapping with deep energy levels is considered to be slower than trapping in shallow traps.

- Pulsed-IV and pulsed-RF S-parameter measurements are used for the extraction of large-signal models that assume substrate-related trapping effects [5.92,5.116]. The V_{DS} -dependence of the drain-current dynamics is used to extract a more accurate prediction for the RF-power performance.
- Power measurements under load variation have been used to investigate the current collapse in [5.88]. The knee voltage is found to increase with the drain bias. RF-stress has an impact on dispersion and power characteristics of AlGaN/GaN HEMTs, as discussed in [5.67]. Surface engineering and passivation are of fundamental importance for RF-longterm reliability [5.62].

The effects for GaN FETs will now be enumerated and followed by more detailed analysis. They include the following:

1. Drain current collapse [5.122]
2. Drain and gate current dispersion, i.e., the difference of cw-, pulsed-, and extracted RF-current device characteristics
3. Time dependence of the device currents on the low-frequency (DC-MHz) scale
4. V_{DS} -dependent shift of the threshold voltage
5. RF-power-slump
6. Premature power/gain compression

These effects are now discussed in detail:

1. Current collapse (1) is the most common feature directly observed in the DC-measurement. It describes the change/collapse of the drain current I_D as a function of V_{DS} , which is not caused by thermal effects. From a different perspective, it describes the change of output characteristics when a different bias is applied before the output characteristic is measured.
2. Current dispersion (2) describes the difference of the DC-characteristics measured in cw-mode as compared to pulsed-measurements for different pulse widths and quiescent bias independent of the thermal effects. Fig. 5.7 gives the differences in the output characteristics for a pulse length of 1 μ s, measured for different quiescent bias.
3. The time dependence (3) or transients in the time-domain of the DC-current I_D on the low-frequency time scale describes a device behavior similar to the current dispersion in (2).
4. A shift of the threshold voltage V_{thr} (4) is part of the general effects visible on the output characteristics in (1).
5. The effect of (5) denotes the lack of the RF-currents and voltages to reach areas in the (I_{DS}, V_{DS}) -current–voltage plane, which are suggested to be the DC-current characteristics. This includes particularly the knee-voltage walk-out.

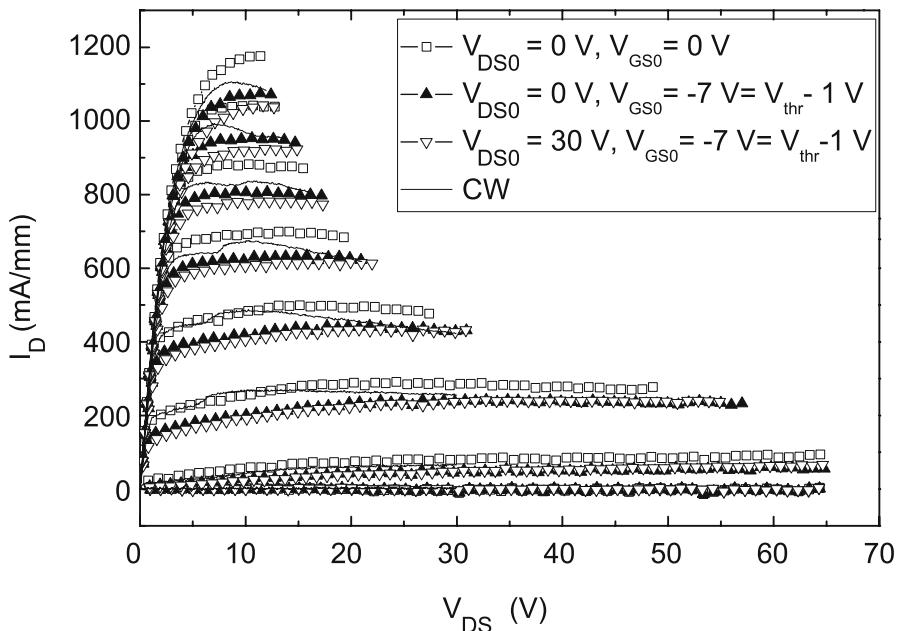


Fig. 5.7. CW- and pulsed-output characteristics that reveal the dispersion effects, $V_{GS} = -6$ to 1 V , step 1 V

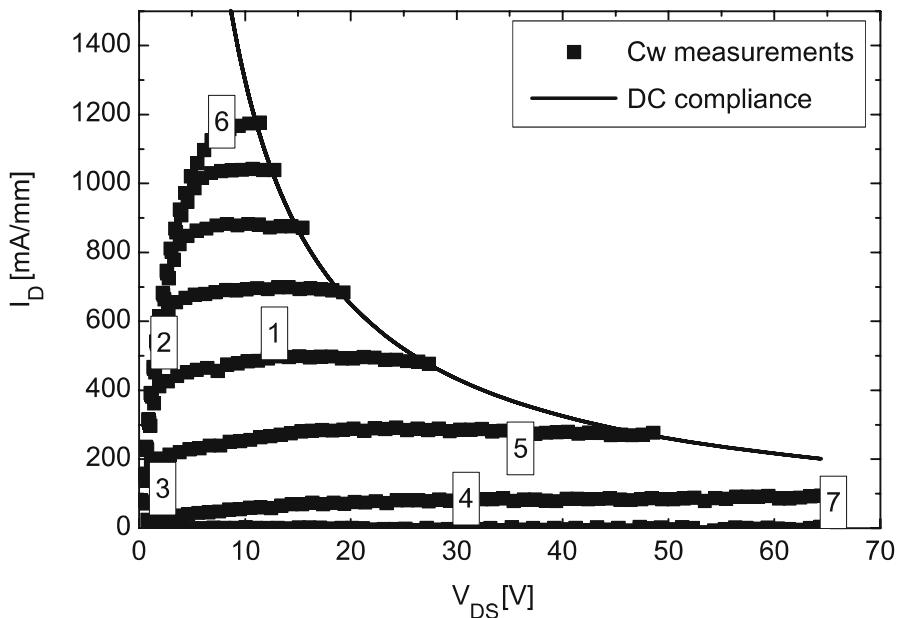


Fig. 5.8. Different quiescent biases for pulsed-measurements in the time-domain for the investigation of GaN HFETs

6. As a result of this compressive behavior, the P_{out} vs. P_{in} power characteristic yield a premature compression of gain or P_{out} , which is denoted as RF-power slump. The effects on the dynamic behavior are visualized below in Fig. 5.9.

Dispersion can be characterized by both time- and frequency-domain methods.

5.2.2 Dispersion Characterization and Analysis

Time-Domain Methods

Time-domain methods are used to separate dispersive effects. The following sequence of pulsed-DC-measurements is suggested, e.g., in [5.120, 5.182]. Fig. 5.8 clarifies two different characterization methods. The measurements include the following:

1. cw-measurements [5.101]
2. Pulsed-measurements at quiescent zero bias ($V_{\text{DS}0} = V_{\text{GS}0} = 0 \text{ V}$)
3. Pulsed-measurements at cold pinch-off $V_{\text{DS}0}$ bias (e.g., $V_{\text{DS}0} = 0 \text{ V}$, $V_{\text{GS}0} = V_{\text{thr}}$)
4. Pulsed-measurements from hot pinch-off at operation bias $V_{\text{DS}0}$ (e.g., $V_{\text{DS}0}=30 \text{ V}$, $V_{\text{GS}0} = V_{\text{thr}}-1 \text{ V}$). The timing of the measurements is of vital importance, as given in [5.182]. Additional measurements are useful for determining further effects:

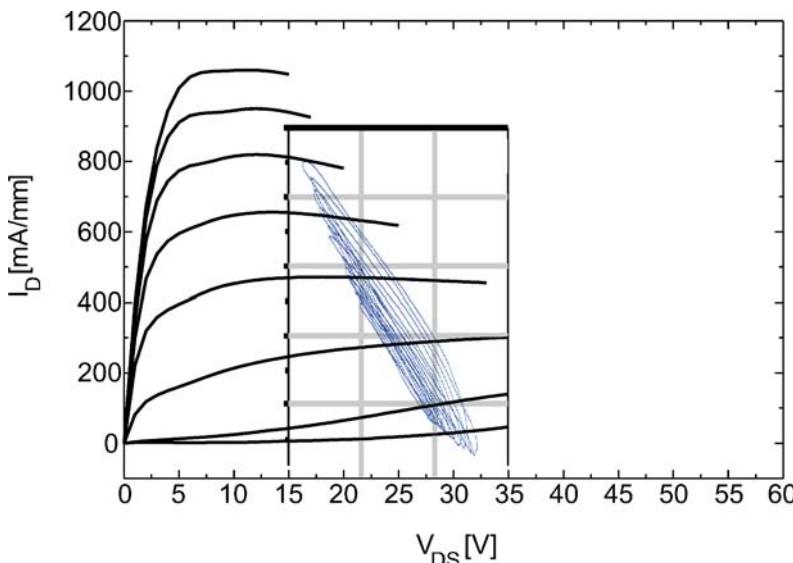


Fig. 5.9. RF-current-swing characteristics to reveal load and RF-dispersive effects

5. Pulsed-measurements from the full operation bias, e.g., at class-A bias at medium current bias ($V_{DS0} = 40\text{ V}$, V_{GS0} for $I_{Dmax}/2$)
6. Measurements in the full channel situation: on-state bias with V_{DS0} slightly above the knee voltage V_{knee} ($V_{DS} = 10\text{ V}$, $V_{GS} = 1\text{ V}$)
7. Pulsed-measurements near the breakdown voltage to reveal additional trapping effects

The procedure and its extensions allow the operation of the device at constant thermal conditions if the full-channel and class-A bias-situation are properly chosen, see Fig. 5.8. With the substrate temperature T_{sub} kept constant, self-heating (SH) due to constant dissipated DC-power on the dissipated power hyperbola is controlled. A low-duty-cycle (1% or lower) for the pulsed-measurements allows the minimization of the thermal influence of the pulses. Deduced from these measurements, the following figures-of-merit and dispersion parameters can be deduced for an operation bias $V_{DS} = 40\text{ V}$:

$$a_{\text{gate-lag}} = \frac{I_{DS,\text{pulse}, V_{GS0}=V_{thr}-2\text{ V}, V_{DS0}=0\text{ V}}}{I_{DS,\text{pulse}, V_{GS0}=0\text{ V}, V_{DS0}=0\text{ V}}} \quad (5.45)$$

and

$$a_{\text{drain-lag}} = \frac{I_{DS,\text{pulse}, V_{GS0}=V_{thr}-2\text{ V}, V_{DS0}=40\text{ V}}}{I_{DS,\text{pulse}, V_{GS0}=V_{thr}-2\text{ V}, V_{DS0}=0\text{ V}}}. \quad (5.46)$$

Further parameters are helpful to isolate the lagging:

$$a_{\text{gate,cw}} = \frac{I_{DS,\text{pulse}, V_{GS0}=V_{thr}-2\text{ V}, V_{DS0}=0\text{ V}}}{I_{DS,\text{cw}}} \quad (5.47)$$

and

$$a_{\text{drain,cw}} = \frac{I_{DS,\text{pulse}, V_{GS}=V_{thr}-2\text{ V}, V_{DS}=40\text{ V}}}{I_{DS,\text{cw}}}. \quad (5.48)$$

The ratios a_i can be evaluated at any pulsed-bias in the output characteristics. Typical bias to evaluate the dispersion to define a figure-of-merit for dispersion are the following:

- At the knee point, i.e., positive V_{GS} and $V_{DS} = V_{knee}$
- At a class-A bias, V_{DS} at operation and V_{GS} for $I_{Dmax}/2$
- At high dynamic V_{DS} close to pinch-off, which also allows to estimate the isolation under pulsed-conditions

The evaluation allows to nominally separate the effect of gate-lag (5.45) and drain-lag (5.46). The measurements can be performed with several measurement configurations. More conventional pulsed-IV-measurements setups are proposed, e.g., in [5.149]. Recently, standardized DC-test equipment is often used [5.12, 5.188], which allows characterization of devices up to 10 A of current and 200 V of bias with pulse width $\leq 50\text{ ns}$. Such a system can be extended to pulsed-S-parameter measurements of devices with similar gate periphery and power levels, as reported in [5.197].

State-of-the-Art of Dispersion Analysis

Several approaches have been proposed for dispersion analysis. In a simplified model, the ratio of the pulsed-DC-measurements in (5.45) in the time-domain accounts for the influence of the gate bias, or gate-lag, while expression (5.46) accounts for the effect of the drain voltage or drain-lag. Fig. 5.8 depicts the various quiescent bias situations. In a first order approach, the gate-lag (comparison of quiescent situation (2) and (3) in Fig. 5.8) is caused by surface or near-gate-interface effects, while the drain-lag is caused by a backgating effect in the part below the channel, i.e., in the bottom substrate, nucleation layer, or buffer layer; see, e.g., [5.16]. The inclusion of measurements such as (5.47) and (5.48) allow the extraction of further information. Quiescent bias situation (5) is a typical class-A operation bias. Situation (6) further characterizes the maximum possible drain current $I_{D\max}$. As with an initially saturated channel and barrier layer and low duty cycle, the maximum amount of carriers is available in a dispersive situation.

Temperature Dependence

The bias dependence of the mechanisms mentioned in previous sections are a good measure to isolate different dispersive effects. An accessible parameter is the substrate temperature. Typical findings for RF-dispersion down to cryogenic temperatures are reported, e.g., in [5.105, 5.128]. The findings include the following:

- Dispersion of the pulse output characteristics is more severe at a lower temperature $T_L = 150\text{ K}$, which implies that more electrons remain trapped and relax [5.128]. The output characteristics show more pronounced changes and gradients.
- Passivated HFET samples without dispersion at room temperature show increased dispersion at low temperatures of 150 K [5.105].
- The trap levels can be isolated more easily at lower temperatures, as the broadening of the levels is suppressed [5.121].
- Further, additional effects, such as the onset of impact ionization at cryogenic temperature, have been proposed [5.105].
- Investigations of frequency dispersion in AlGaN/GaN at elevated temperatures are given in [5.121]. The transition frequency of the dispersion shifts to higher frequencies with higher temperatures. The behavior is found to be consistent with the temperature behavior of the $1/f$ -noise.

The general lattice-temperature dependence reduces the impact of trapping at temperatures $T_L \geq RT$ whereas at $T_L \leq RT$ the impact is enhanced. These findings support the characterization and analysis at room temperature.

Frequency-Domain Methods

Several frequency domain methods are available for the characterization of dispersion. As an example, Fig. 5.9 shows the measured output power swing

of an AlGaN/GaN HEMT measured at 10 GHz in the RF-domain. The measurements are taken by a microwave transition analyzer (MTA) including four harmonics. Fig. 5.9 shows an RF-output swing at an operation voltage $V_{DS} = 30$ V with harmonics measured up to 50 GHz. Compared to the cw-DC and pulsed-DC output characteristics, deviations are visible especially at the knee voltage and in the near breakdown region. This powerful technique has been repeatedly applied, e.g., in [5.62, 5.64, 5.116]. It can be used for model verification [5.190] at the RF-frequency of interest. In the frequency-domain, the $1/f$ -excess noise can be directly measured from 1 Hz up to at least 10 MHz. This allows the extraction of trap- and excess-noise information. As will be shown below in Fig. 5.42, trapping effects lead to additional contributions to the excess-noise spectrum and allow the isolation of trap-specific time constants.

5.2.3 Models for Frequency Dispersion in Devices

Several models exist that describe the physical mechanisms of frequency dispersion, either in parts or from a comprehensive point of view. This section further addresses the RF-modeling of these effects. Fig. 5.10 gives the RF-representations of dispersion effects, e.g., [5.87, 5.195].

The Concept of a Virtual Gate

One of the most critical effects of the surface charges in AlGaN/GaN FET is the effect of a second, so-called virtual gate. Increased surface-charge densities effectively lead to an increase of the area that serves as the gate metal and thus cause additional capacitance between surface and the channel charge. As a result, the channel-charge is modified on various time scales. In Fig. 5.10, this second virtual gate is represented by an additional capacitance and resistance (1). This gate has an effect similar to an extended gate length [5.87, 5.195].

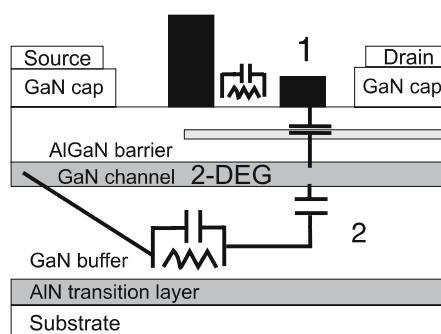


Fig. 5.10. RF-representations of dispersive effects

Backgating

A second, very prominent model for the impact of dispersion on the RF-properties is the backgating model, e.g., for AlGaN/GaN FET reported in [5.84]. In Fig. 5.10, a backside gate is depicted (2). This effect is very well known from silicon RF-MOSFETs [5.78] on conductive substrate, but it has also been described for GaAs MESFETs [5.169] and as a floating body effect for GaN/AlGaN HFETs due to the conductive nature of the AlN-interlayers on the heterosubstrate [5.128]. The interaction with a charge concentration in the buffer layer with the channel leads to an additional channel-buffer capacitance. The interaction is described for GaAs MESFETs by a junction capacitance model, as reported, e.g., in [5.169]. A dynamic current injection from the source side into the buffer interacts with the channel charge and leads to an additional RC constant.

A Charge-Control Model

Based on the previous analysis, a model will be developed to enhance the understanding of the various dispersive effects and, effectively, their suppression. As is pointed out in Sect. 2.2.3, understanding charge control is one of the most important needs within III-N FETs. The model is based on the analysis of the whereabouts of free carriers in the polar semiconductor materials, allowing exact elimination of the frequency-dependent and thus dispersive sources/drains of free carriers. The initial origin of the carriers in undoped III-N HFETs is manifold and is discussed widely for III-N FETs. The carriers originate from the following:

- Intentional and nonintentional (nid) doping of the bulk material
- δ -doping in the barrier and buffer layer
- Surface- and interface-charges due to polarization effects
- Generation/recombination with and without traps [5.157]
- The stress compensation and nonideal semiconductor layers due to the hetero-epitaxy, see Fig. 3.2

In the model, the effective free channel charge can be rewritten as the sum of the effective charges of the above mentioned mechanisms:

$$q_{\text{channel}} = q_{\text{diel,interface}} + q_{\text{semi,interfaces}} + q_{\text{bulk,traps}} + q_{\text{doping}} + q_{\text{initial}}. \quad (5.49)$$

Based on this analysis, the frequency dependence of the channel charge can be correlated with the frequency dependence of the charges q_i .

Absolute Charge Calculations

First of all, we need to calculate the absolute amount of charges in the channel relative to the source and drain at the surface to explain the sensitivity of the FETs to the changes. We assume a sheet-carrier density of $1 \times 10^{13} \text{ cm}^{-2}$ for

Table 5.2. Parameters for charge and current analysis

l_g	Source drain (μm)	$I_{D\max}$	n_{sheet} (cm $^{-2}$)	Buffer thick. (μm)	Chan. thick.
0.25 μm	4 μm	1.2 A mm $^{-1}$	1×10^{13}	2	2.5 nm
Channel e $^-$	Charge	Buffer e $^-$	Buffer q	I_{DS}	
4×10^8	64 pC	6×10^6	0.96 pC	4.8×10^7 A cm $^{-2}$	

a 4 μm long HEMT channel with a gate length of 0.25 μm and a gate width of 1 mm. The channel thickness is assumed to be 2.5 nm, based on Schrödinger–Poisson solver analysis. This results in an overall channel number of 4×10^8 electrons or a charge of 64 pC, as detailed in Table 5.2. Relative to this amount, a buffer layer with a defect concentration of 10^{16} cm $^{-3}$ and a thickness of 2 μm results in an overall charge of 6×10^6 electrons or 0.96 pC. Thus, an ideal buffer is not critical for the overall charge distribution. However, a charge contribution similar to the channel charge can be considered to be present at the following:

- The dielectric/semiconductor interface
- Substrate/buffer interface in the nucleation layer, depending on the nucleation growth

Based on calculations and the parameters in Table 5.2, the surfaces/interfaces can yield a charge contribution similar to the channel. This is one reason for the strong impact of dispersion in III-N devices. Further, the nucleation layer of ≥ 100 nm thickness can contribute a similar amount of electrons as the channel, if the growth is relatively immature.

Current Density Calculations

In addition to the charge analysis, the very high sheet-carrier concentrations at the channel interface lead to very high channel-current densities. Again based on the parameters from Table 5.2, channel-current densities of $\geq 10^7$ A cm $^{-2}$ can be calculated. Such high current densities exceed even the highest current-densities in GaAs or InP HBTs by about two orders of magnitude [5.68]. This channel current density in GaN HFETs is further about three orders of magnitude higher than in Si power MOSFETs [5.55] and about one order of magnitude higher than in InGaAs HEMTs [5.37]. The latter is due to the lower band bending in the channel and the lower effective doping in (In)GaAs HFETs [5.37]. The high current densities lead to the following physical effects, which limit the current transport:

- High-current crowding and related electromigration near the ohmic contacts [5.17]

- High current-density impact ionization for current densities $\geq 10^6 \text{ A cm}^{-2}$ [5.189]

These two effects eventually lead to the reduction of the densities during GaN FET device design in order to avoid high density effects, which are so far only known from bipolar and avalanche devices [5.184]. The impact of the current crowding in the source region is further analyzed in [5.185]. The current is space-charge limited [5.184] based on the following reasoning. Beyond a current density of 10^6 A cm^{-2} space-charge effects occur due to the lack of a background impurity doping to compensate those. Thus, the effective source resistance R_S becomes a nonlinear function of the RF-drive power, which has also a strong impact on the power [5.184] and nonlinear performance of the device [5.108].

5.2.4 Suppression of Frequency Dispersion

Based on the modeling discussed in the previous section, the following means have been found useful for the reduction of the dispersion and high-current effects:

- The reduction of the defect density wherever possible within the device [5.194]
- The applications of appropriate technological surface/interface treatment [5.194] corresponding to the defect reduction
- The introduction of doped-cap layers that provide sufficient n-carriers to compensate the free surface states [5.85]
- A reduction of the channel current density, e.g., [5.84]

In addition to these insights for device design, dispersion can further be covered by the following:

- (Over)doping of the device with polarized and doping-based carriers [5.13]
- Device leakage of various kinds [5.81]
- The use of conducting passivation material [5.194]

These effects cover some of the frequency dispersive effects; however, they do not always help with the final reliable suppression of dispersion, as overdoping and device leakage lead to significant device reliability issues. These are discussed in Chapter 7.

5.3 Small-Signal Characterization, Analysis, and Modeling

5.3.1 RF-Characterization and Invariants

Several assumptions are typically made for the characterization of passive and active RF-devices. They are illustrated in Fig. 5.11. Multipole S-parameter

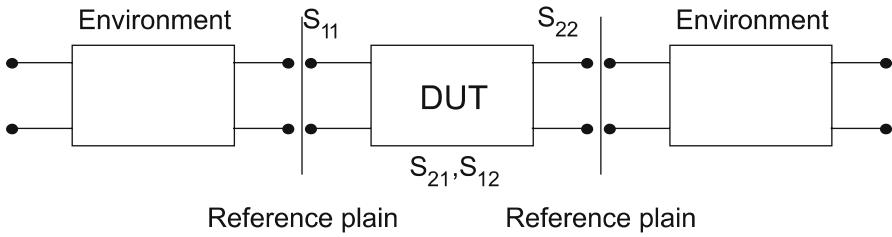


Fig. 5.11. Multipole characterization of the device-under-test (DUT)

measurements of RF-devices or device-under-test (DUT) are typically taken; see, e.g., [5.14, 5.47, 5.179, 5.201]. Derived from S-parameter measurements at a given impedance, e.g., 50Ω , all other high-frequency parameters, such as h-, Z-, Y-, and a-parameters, are available and can be converted to each other unambiguously. Several quantities can be derived from the S-parameters at the RF-reference planes given in Fig. 5.11. We derive from the S-parameters the maximum stable gain (MSG),

$$\text{MSG}(f) = \left| \frac{S_{21}}{S_{12}} \right|; \quad (5.50)$$

the maximum available gain (MAG),

$$\text{MAG}(f) = \left| \frac{S_{21}}{S_{12}} \right| \cdot \left(k \pm \sqrt{k^2 - 1} \right); \quad (5.51)$$

the unilateral gain U ,

$$U(f) = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2 \cdot k \cdot \left| \frac{S_{21}}{S_{12}} \right| - 2 \cdot \text{Re} \left(\frac{S_{21}}{S_{12}} \right)}; \quad (5.52)$$

and the device stability factor,

$$k(f) = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2 \cdot |S_{12}| |S_{21}|}. \quad (5.53)$$

Further invariants are usually derived. The current gain cut-off frequency is defined as

$$f_T = f(h_{21} = 0). \quad (5.54)$$

The maximum frequency of oscillation is derived based on the unilateral gain

$$f_{\max} = f(U = 0); \quad (5.55)$$

and based on MAG/MSG

$$f_{\max} = f(\text{MAG}/\text{MSG} = 0). \quad (5.56)$$

As a measure of the stability, the cut-off frequency for the stability f_c is defined:

$$f_c = f(k = 0). \quad (5.57)$$

These parameters are used for the characterization of III-N devices.

5.3.2 Common-Source HEMTs

The common-source FET configuration is mostly used for the application of FETs in power amplifiers. As an initial example, S-parameters of an AlGaN/GaN HEMT are measured between 0.5 and 20 GHz, as given in Fig. 5.12 for a gate width $W_g = 3.2$ mm and a gate length $l_g = 0.5 \mu\text{m}$. A large S_{21} is typical for GaN HFETs, further the output S-parameter S_{22} depicts a high impedance for a given gate width. Derived from these S-parameters, Fig. 5.13 gives the cut-off frequencies f_T and f_{\max} calculated from the S-parameters measured at $V_{DS} = 7$ V as a function of gate length l_g for a planar device without gate recess. The results nicely follow a nearly constant product of $l_g \times f_T$ of 10 GHz μm down to a gate length of 150 nm. Furthermore, f_{\max} values of 140 GHz are reached for devices with a periphery $W_g = 120 \mu\text{m}$. Fig. 5.14 gives the MAG/MSG at 40 GHz as a function of the gate width for a device with $l_g = 150$ nm. MAG/MSG values of 8 dB for devices with $W_g = 120 \mu\text{m}$ gate width are reached. More than 6 dB of gain are found for an optimized

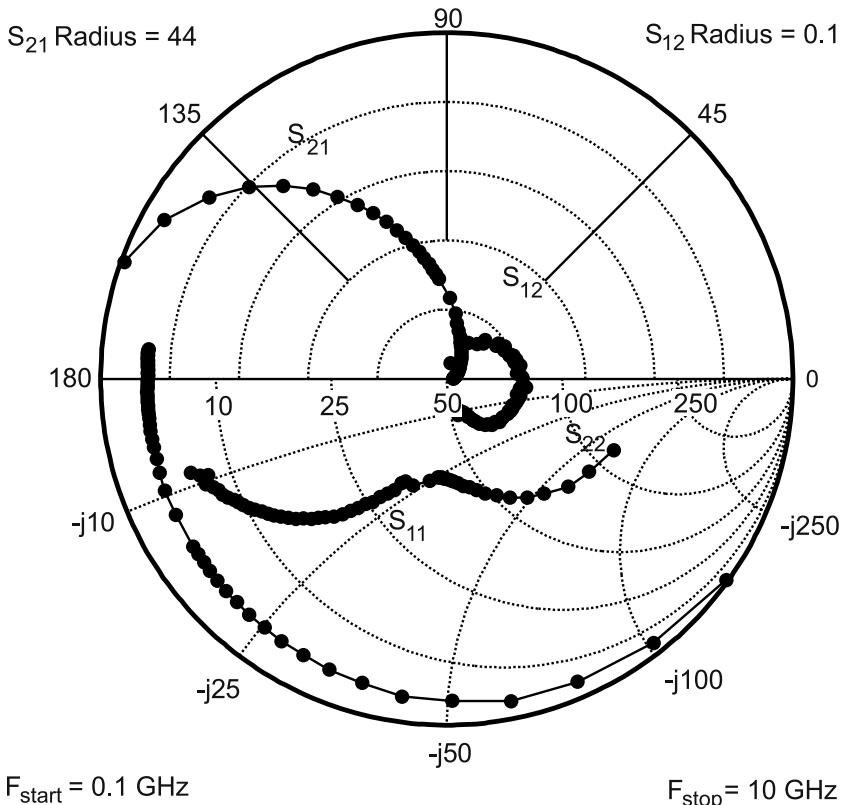


Fig. 5.12. S-parameters S_{ij} between 0.1 and 10 GHz of an AlGaN/GaN HEMT of gate length $l_g = 500$ nm measured at $V_{DS} = 30$ V for $W_g = 3.2$ mm

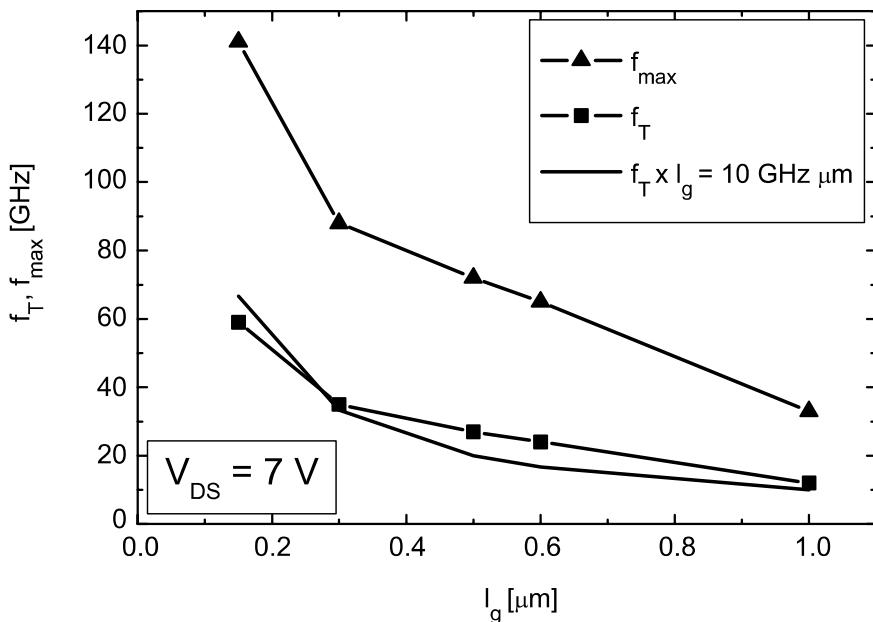


Fig. 5.13. f_T and f_{max} as a function of gate length l_g at $V_{DS} = 7 \text{ V}$ for an AlGaN/GaN HFET on s.i. SiC with $W_g = 2 \times 60 \mu\text{m}$

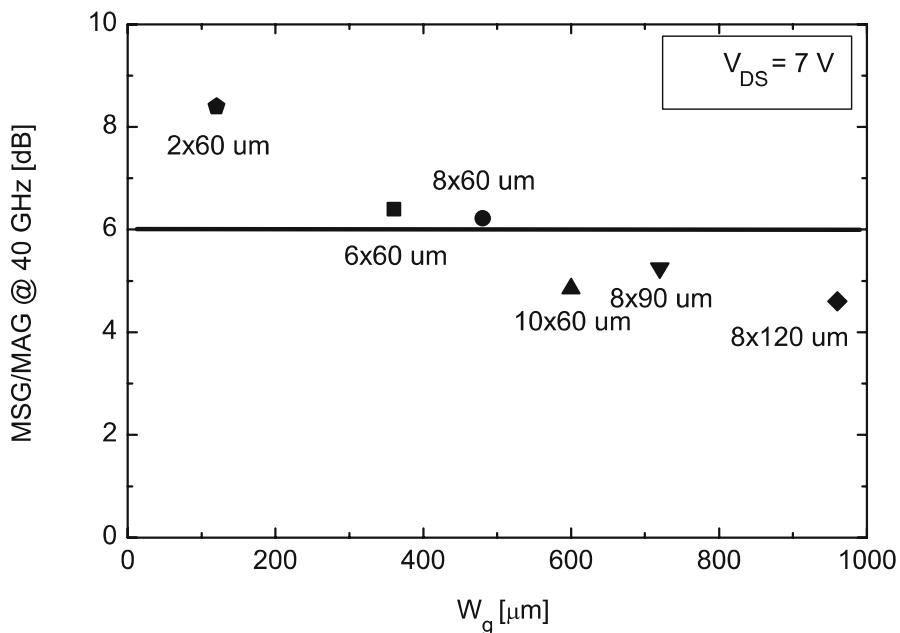


Fig. 5.14. MAG/MSG at 40 GHz as a function of gate width W_g of an AlGaN/GaN HFET on s.i. SiC with $l_g = 150 \text{ nm}$

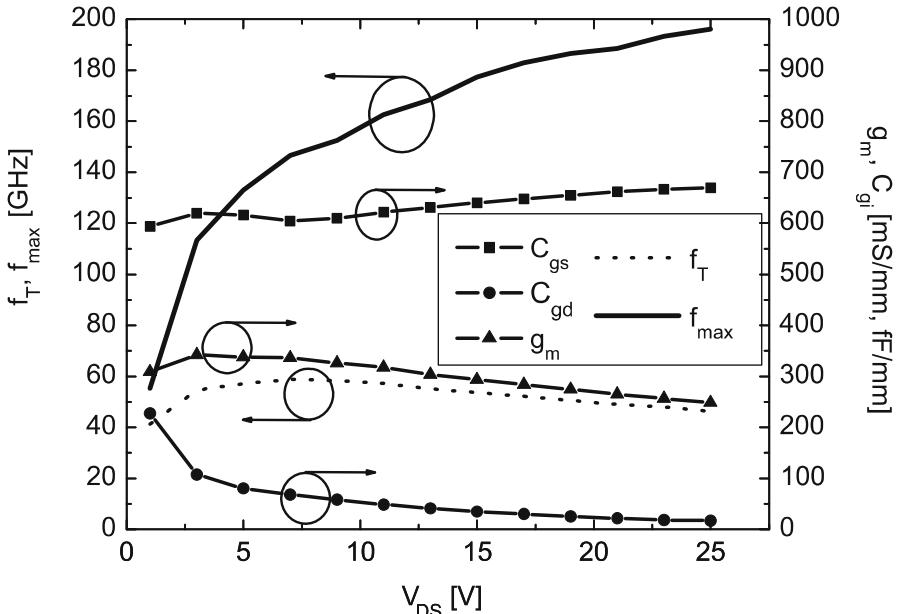


Fig. 5.15. f_T , f_{max} , g_m , C_{gs} , and C_{gd} as a function of V_{DS} for $l_g = 150$ nm

device with a gate periphery $W_g = 8 \times 60 \mu\text{m}$. Fig. 5.15 shows the cut-off frequencies f_T , f_{max} , and their most important constituting small-signal parameters, g_m , C_{gs} , and C_{gd} as a function of V_{DS} for a device with $l_g = 150$ nm. The initial approaches for a typical small-signal model for GaN devices are similar or equal to those of GaAs PHEMTs, e.g., [5.14, 5.47, 5.179, 5.201]. Fig. 5.15 shows that the cut-off frequencies f_T are nearly constant as a function of V_{DS} at constant V_{GS} . The maximum frequency of oscillation rises to values up to 200 GHz at $V_{DS} = 25$ V. This increase is based on the nearly constant transconductance g_m , the nearly constant C_{gs} , and the reduction of C_{gd} with rising V_{DS} . The physical background of the constant behavior of g_m and C_{gs} is based on the good carrier confinement of the electrons in the channel. An example of a comprehensive physics-based small-signal analysis of fully strained and partially relaxed high Al-content $\text{Al}_m\text{Ga}_{1-m}\text{N}/\text{GaN}$ HEMTs is given in [5.145]. The physical model allows close correlation of the current-gain cut-off frequency with device design parameter Al-content in the barrier. High Al-contents are found to be useful for increased transconductance. The advantages of high Al-content are traded for increased relaxation, increasing traps concentrations, and challenges with the ohmic contacting.

Temperature Dependence of the RF-parameters

The lattice temperature is another critical parameter, as GaN FETs are proposed for high-power and high-temperature operation. Fig. 5.16 gives the

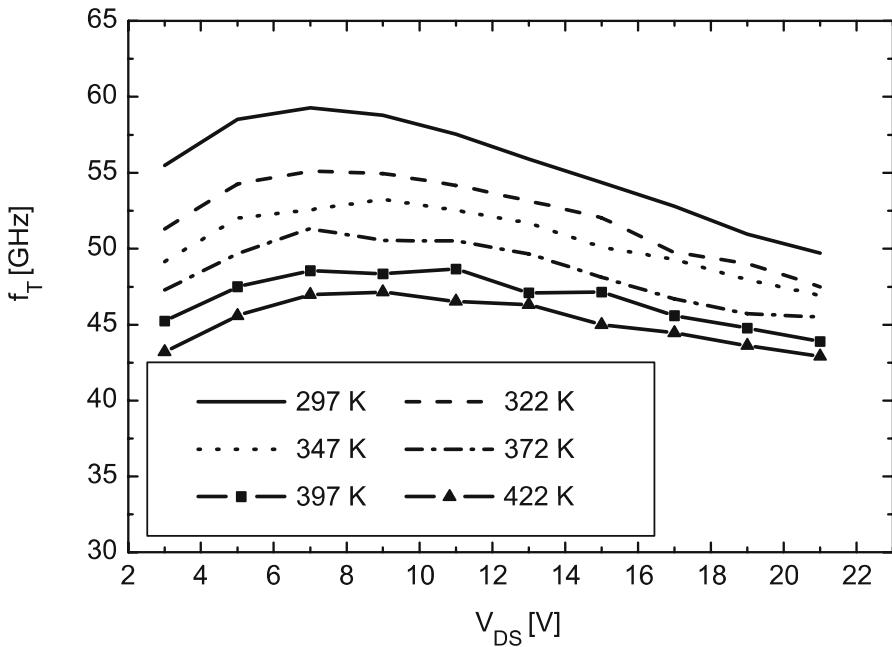


Fig. 5.16. Cut-off frequency f_T as a function of V_{DS} with the substrate temperature T_{sub} as a parameter

current gain cut-off frequency f_T as a function of V_{DS} with the substrate temperature T_{sub} as a parameter. The device has a gate length of 150 nm. The temperature at the backside on the unthinned SiC substrate is varied between room temperature and 422 K. A reduction of f_T of 25% for 100°C change in temperature can be derived from Fig. 5.16. Further, Fig. 5.17 gives the gain characteristics MAG/MSG at 40 GHz, f_T , and f_{max} as a function of V_{DS} with T_{sub} as a parameter for a device with $l_g = 150$ nm and a gate periphery $W_g = 8 \times 60$ μm . All three gain parameters in Fig. 5.17 show a similar gain reduction between 25 and 100°C, which amounts to about 25%.

Variations of AlGaN/GaN HEMT Structures

The variation and optimization of the layer structure of AlGaN/GaN HEMTs has a strong impact on the small-signal performance. As an example, Fig. 5.18 gives a comparison of the cut-off frequencies with different doping concentrations in two different HEMT structures at the same nominal gate lengths l_g . Fig. 5.18 shows that increased doping concentrations in the barrier lead to higher cut-off frequencies, while the breakdown voltages are reduced accordingly. This is depicted by the different V_{DS} ranges possible for the cw-S-parameter measurements.

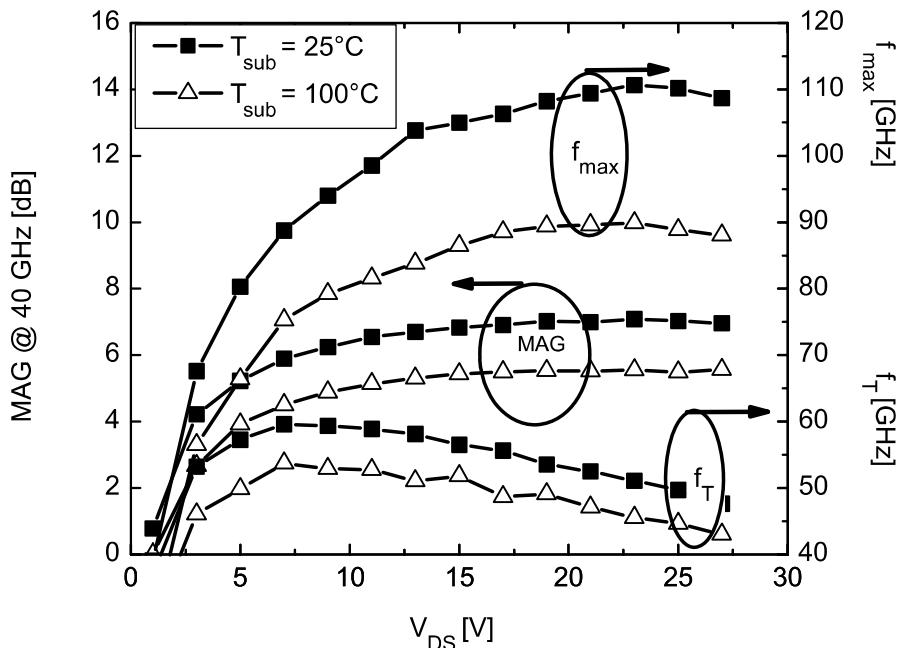


Fig. 5.17. MAG/MSG of an AlGaN/GaN HEMT on s.i. SiC at 40 GHz, f_T , and f_{max} as a function of V_{DS} with temperature T_{sub} as a parameter

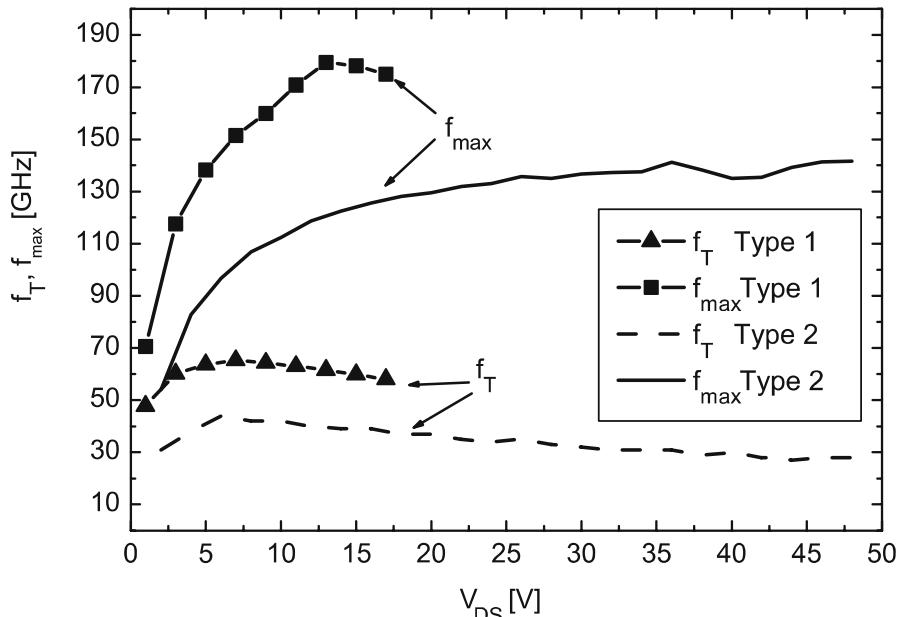


Fig. 5.18. Cut-off frequencies f_T and f_{max} as a function of V_{DS} for AlGaN/GaN HEMTs on s.i. SiC with two different doping concentrations

5.3.3 Dual-Gate HEMTs

Dual-gate and cascode AlGaN/GaN HEMTs are further attractive candidates for efficiently increasing the gain-per-stage in GaN RF-amplifiers. Two gates are placed in series within a typical HEMT. Fig. 5.19 gives an SEM image of an AlGaN/GaN dual-gate FET with a gate length $l_g = 150$ nm on s.i. SiC substrate. Fig. 5.20 gives the comparison of the measured MAG/MSG gain for both a common-source and a dual-gate device as a function of frequency measured up to 110 GHz. The devices are compared for a gate width $W_g = 4 \times 45\text{ }\mu\text{m}$ and for a gate length $l_g = 150$ nm. The dual-gate device yields about double the available gain at a given frequency for a comparable V_{DS} bias (twice the V_{DS} of the common-source device). This allows operation up to the V-frequency band with gain levels of ≥ 10 dB at 60 GHz. Further examples of cascode- and dual-gate devices can be found, e.g., in [5.34]. The gate lengths of the first amount to 0.16 and $0.35\text{ }\mu\text{m}$ for the second allow to increase the breakdown voltage of ≥ 100 V while maintaining f_T values of 60 GHz.

5.3.4 Pulsed-DC- and RF-Characteristics

Pulsed-DC- and RF-measurements are of major importance for the understanding of III-N device behavior. This is already stated in Sect. 5.2.1. A lot of measurement techniques have been developed for GaAs and Si-based devices [5.132, 5.133, 5.188, 5.197] using pulsed-techniques. As mentioned in Chapter 2, GaN MESFETs [5.183] and HEMTs [5.120] are characterized by standardized pulsed-measurements in order to separate dispersion and thermal effects.

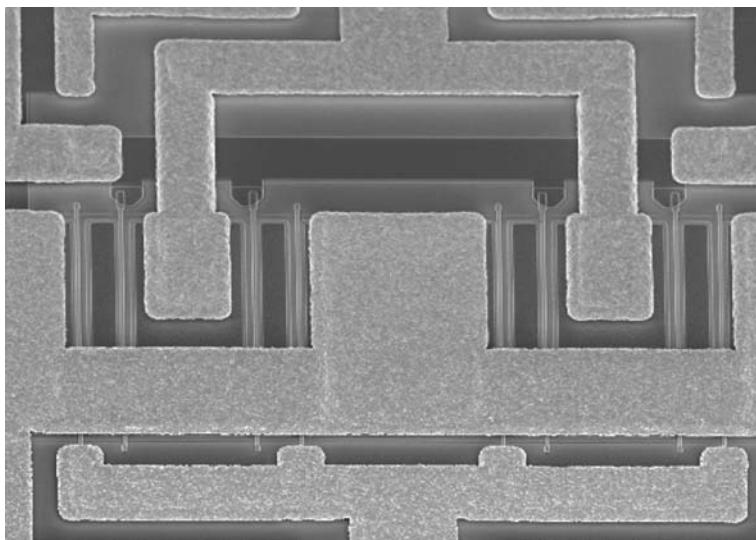


Fig. 5.19. SEM image of a dual-gate AlGaN/GaN HEMT with $l_g = 150$ nm

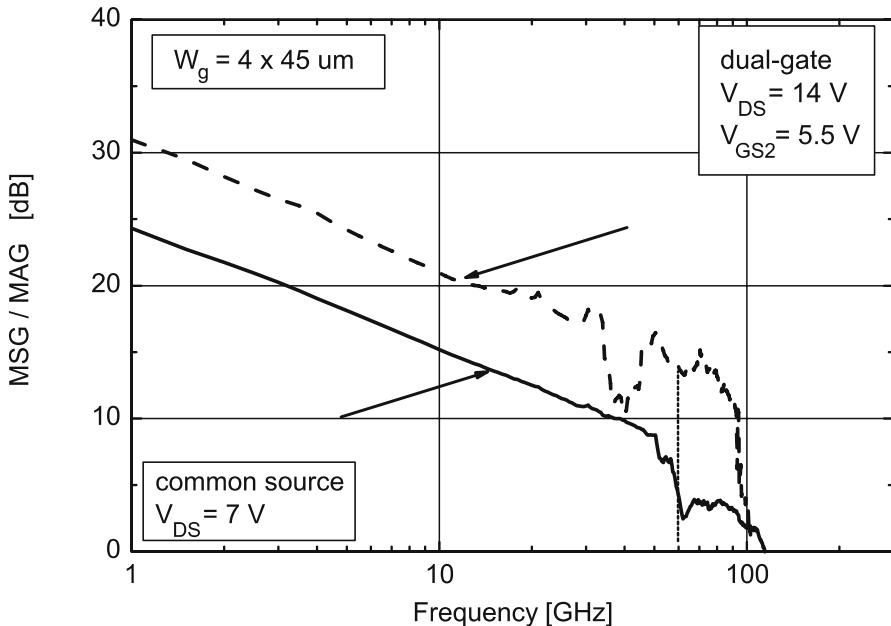


Fig. 5.20. MAG/MSG as a function of frequency for a common-source and a dual-gate AlGaN/GaN HEMT on s.i. SiC with $l_g = 150 \text{ nm}$

Fig. 5.21 gives pulsed-DC-measurements of an AlGaN/GaN HEMT on s.i. SiC, which allow to separate thermal from the dispersive effects discussed previously. This can be achieved by comparing the pulsed-characteristics for low duty-cycle, typically below 1% [5.133], at different quiescent biases and different substrate temperatures between 25 and 100°C. Given the low duty-cycle, an isothermal-like device behavior can be assumed and isothermal effects with varying substrate temperature can be separated from self-heating effects [5.129]. As seen in Fig. 5.21, the influence of the substrate temperature between 25 and 100°C at low duty-cycle is relatively modest compared to the self-heating and the dispersive effects discussed previously. To separate the impact of thermal effects on small-signal RF-parameters, Fig. 5.22 compares the measured f_T for pulsed-conditions using an Agilent 85124 pulsed-DC- and RF-measurement-system. The measurements are performed for a gate width $W_g = 3.2 \text{ mm}$ and a gate length $l_g = 500 \text{ nm}$ for different quiescent bias. The duty cycle is chosen to be low, in this case 0.1%. The overall dissipated power at the maximum bias $V_{DS} = 45 \text{ V}$ is 22.5 W. The difference in the f_T especially for the hot pinch-off conditions is clearly visible and due to dispersive effects. The main focus of pulsed-measurements is not the pure evaluation of thermal effects, but the reduction of DC-power in the device and thus the reduction of self-heating to allow modeling at high bias. Very complex dispersion modes have been isolated in GaN HFETs, which require detailed

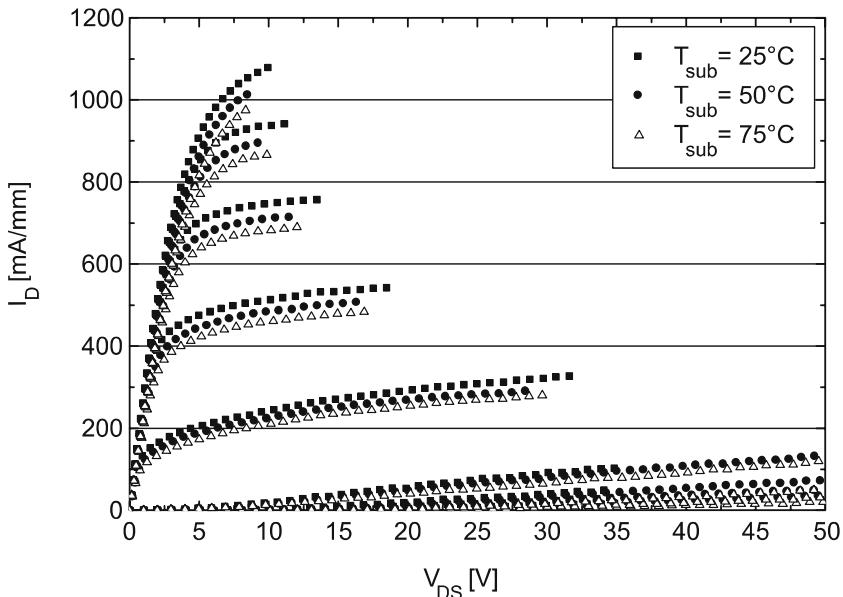


Fig. 5.21. Pulsed-output characteristics as a function of substrate temperature for a low duty-cycle of 0.1%, pulsed from ($V_{DS0} = 0 \text{ V}$, $V_{GS0} = -7 \text{ V}$)

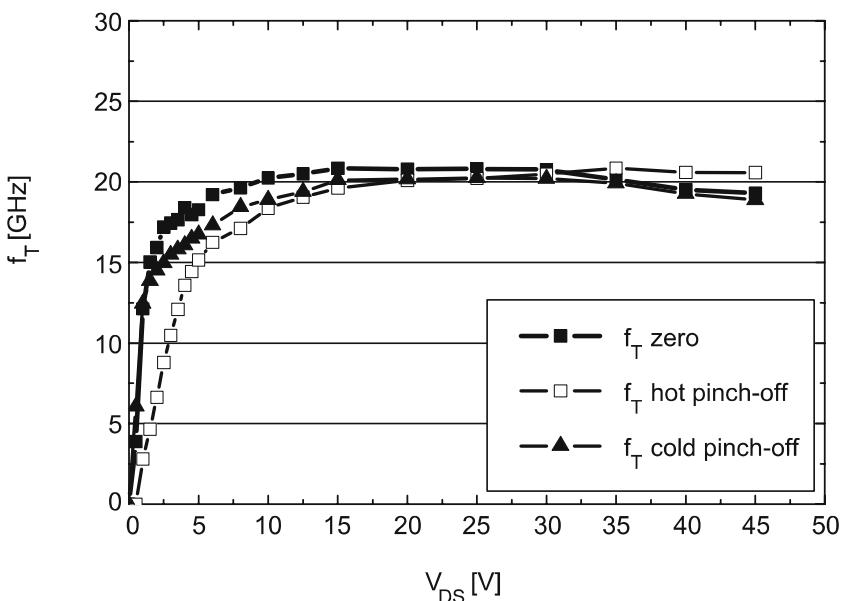


Fig. 5.22. Comparison of the cut-off frequency f_T of an AlGaN/GaN HEMT on s.i. SiC for pulsed-operation and different quiescent bias, zero: ($V_{GS0} = V_{DS0} = 0 \text{ V}$), cold pinch-off: ($V_{GS0} = -7 \text{ V}$, $V_{DS0} = 0 \text{ V}$), hot pinch-off: ($V_{GS0} = -7 \text{ V}$, $V_{DS0} = 30 \text{ V}$)

DC/RF-pulsed-analysis for modeling [5.197]. Thus, in the development and modeling of devices, biasing is possible at voltages that cannot be addressed in cw-mode, as shown in Fig. 5.22. A typical example of the application of DC/RF-pulsed-measurements is large-signal modeling for an operation bias V_{DS0} , where S-parameters at high V_{DS} -bias ($2 \times V_{DS0}$) and high current levels of $\geq I_{Dmax}/2$ are needed. However, they lead to prohibitive channel temperatures during the cw-measurements. Thus, pulsed-measurements are extremely useful.

5.3.5 Small-Signal Modeling

Small-Signal Analysis of FETs

The first approaches for the small-signal analysis of GaN FETs are similar to those of classical GaAs or InP HEMTs. This is due to the fact that GaN (H)FETs are very similar to GaAs PHEMTs or even to InP HEMTs, considering the specific shape of the device terminal characteristics. Examples for the modeling of GaAs are numerous and can be found, e.g., in [5.14, 5.47, 5.161, 5.179, 5.201]. These models have also been applied for the extraction of GaN FETs, e.g., in [5.200]. Fig. 5.23 gives the standard small-signal RF-topology for III-V FETs.

As with any FET, the device representation consists of a complex current source, a parallel output-capacitance C_{ds} and resistance R_{ds} , and an input capacitance C_{gs} . The parasitic shell is simple and similar to any microwave device. As such a model contains sufficient free parameters, the four complex S-parameters S_{ij} can be modeled well as a function of frequency, as long as the parasitic distributed effects do not play a dominant role. Thus, small-signal analysis is nearly always possible, even for very dispersive devices. The analysis of dispersion is possible also through small-signal measurements, as the virtual gate effect has significant impact on the elements extracted. Specific III-N device small-signal extraction procedures have been suggested, e.g., [5.76], which are derived from advanced GaAs methodologies [5.162]. This refers further to the modeling of the diodes and substrate effects. The characterization of forward AC behavior of GaN Schottky diodes yields a giant negative capacitance and nonlinear interfacial layer [5.198]. A similar finding is given in [5.42]. The small-signal approach of Schmalle [5.162] is applied to GaN HFETs in [5.75, 5.76]. A 22-element model is applied for the extraction of a small-signal model, valid between 0 and 60 GHz for a GaN device with $l_g = 0.5 \mu\text{m}$. The parasitic environment consists of two-shells in this case and is used beyond the cut-off frequency f_T of the device.

Substrate Effects in FETs

For AlGaN/GaN HEMTs on silicon substrates, additional effects have to be considered. The lossy and conductive substrates need to be modeled similar to

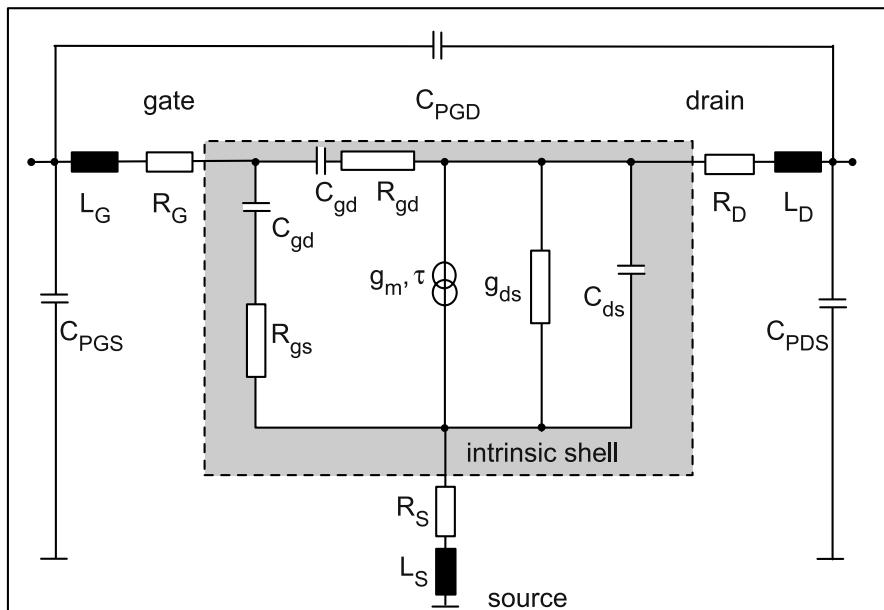


Fig. 5.23. Topology of a small-signal model of an AlGaN/GaN HFET

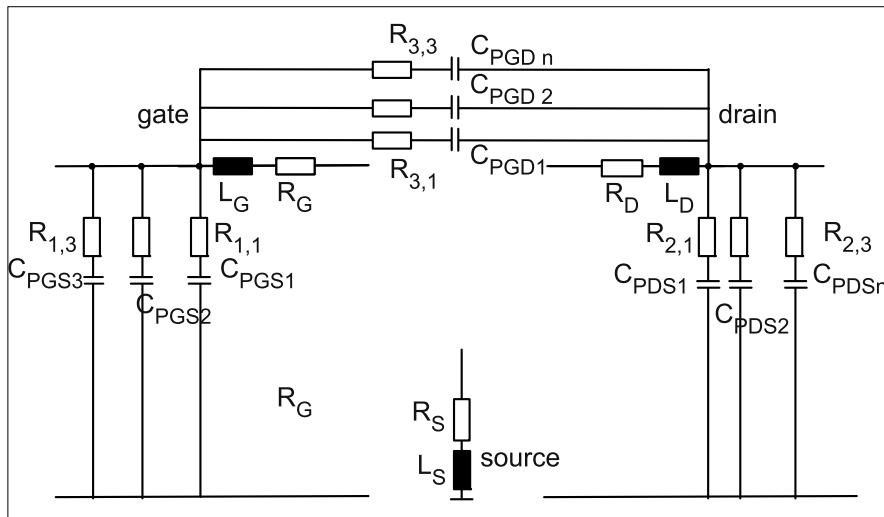


Fig. 5.24. Passive topology of a small-signal model of an AlGaN/GaN HFET

silicon RF-devices, e.g., [5.38]. The small-signal characteristics of microwave power GaN HEMTs on 4-in. Si wafers are described in [5.110]. The intrinsic shell of the HFET model is not modified. However, additional RC networks

are included to model the residual substrate conductivity and the loading of the device. The conductive substrate leads to p-Si/GaN/metal structures, which are modeled as pin-diodes in series with the impedances reflecting the substrate conductivity and the device loading. The topology of the passive environment is depicted in Fig. 5.24. Multiple structures of the RC combinations are used.

Small-Signal HEMT Example on s.i. SiC Substrate

As an example of a complete set of small-signal parameters and the corresponding parasitic elements, Table 5.3 gives a full set of parameters for an AlGaN/GaN HEMT on s.i. SiC substrate with a periphery $W_g = 4 \times 60 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$. The elements are extracted by standard procedures, e.g., [5.179]. We see a low value of the capacitance C_{gd} at $V_{DS} = 25 \text{ V}$ and a reasonable ratio of the capacitances C_{gs}/C_{gd} of $\geq 6:1$. The R_{gd} is negligible in this extraction. The output output capacitance C_{ds} amounts to 0.27 pF mm^{-1} . Table 5.4 adds the parasitic elements in this small-signal approach with one parasitic shell. The source resistance is $0.8 \Omega \text{ mm}$, while the drain resistance R_D is higher due to a non-symmetric contact spacing. Both parasitic values are significant to the reduction of the gain at high RF-frequencies.

Bias and Geometry Dependence

The extracted elements feature several characteristics and dependencies. Several interesting effects can be observed. Fig. 5.25 gives the dependence of the intrinsic capacitances C_{gs} and C_{gd} on gate length. At gate lengths between 300 and 150 nm, the C_{gs}/C_{gd} ratio drops from 8 to 5 for this planar device. At the same time, the elements are bias-dependent. Fig. 5.26 gives the extracted bias-dependence of the RF-output-conductance g_{ds} and the output-capacitance C_{ds} as a function of drain-source bias V_{DS} . At constant gate bias V_{GS} , the variation of the extracted C_{ds} is about 15%, i.e., between 5 and 25 V.

Table 5.3. Small-signal parameters of an AlGaN/GaN HEMT on s.i. SiC with $W_g = 4 \times 60 \mu\text{m}$ and $l_g = 150 \text{ nm}$ at $V_{DS} = 25 \text{ V}$

C_{gs} (pF mm^{-1})	C_{gd} (pF mm^{-1})	C_{ds} (pF mm^{-1})	g_m (mS mm^{-1})	τ (ps)	g_{ds} (mS mm^{-1})	R_{gs} ($\Omega \text{ mm}$)	R_{gd} ($\Omega \text{ mm}$)
0.65	0.09	0.27	382	1.64	15	0.22	0

Table 5.4. Extracted parasitic elements for the coplanar device from Table 5.3

L_G (pH)	L_D (pH)	L_S (pH)	R_S ($\Omega \text{ mm}$)	R_D ($\Omega \text{ mm}$)	R_G (Ω)	C_{pgd} (fF)	C_{pgs} (fF)	C_{pds} (fF)
0	75	76	0.8	1.5	2	20	4	20

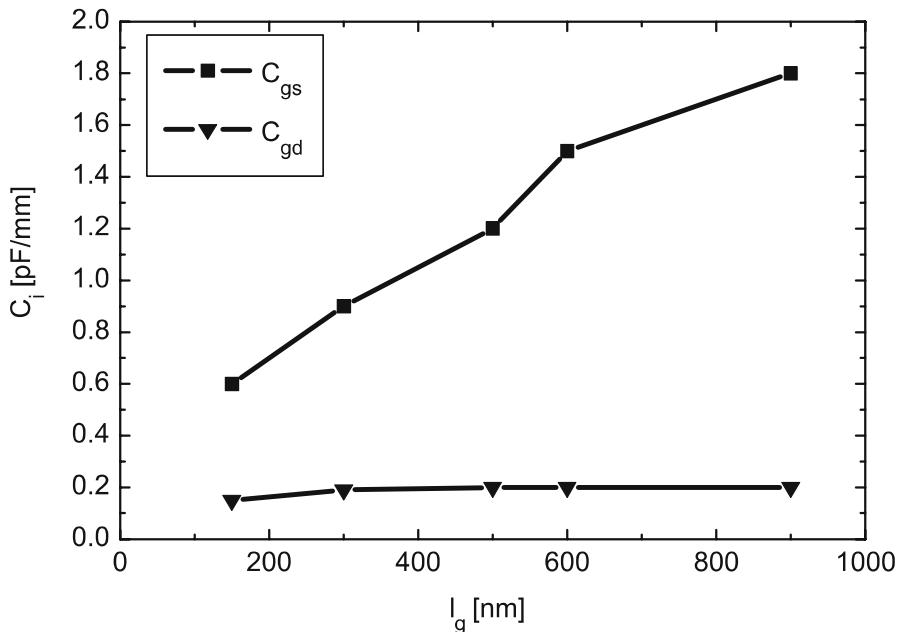


Fig. 5.25. Intrinsic capacitances C_{gs} and C_{gd} of an AlGaN/GaN HEMT on s.i. SiC as a function of gate length l_g at $V_{DS} = 7\text{V}$

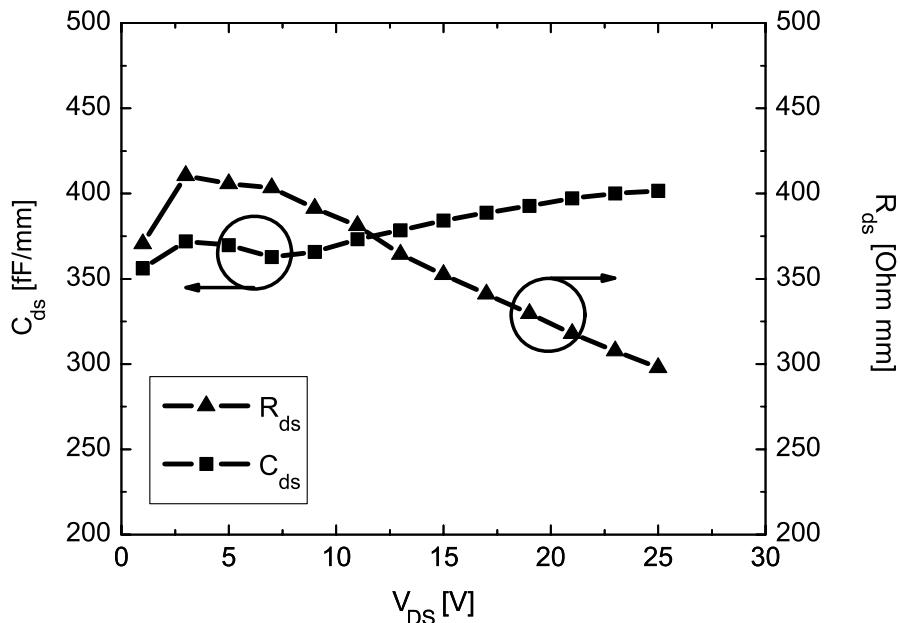


Fig. 5.26. RF-output-resistance R_{ds} and capacitance C_{ds} as a function of V_{DS} at constant V_{GS} for an AlGaN/GaN HFET with $l_g = 150\text{ nm}$

This very moderate change, which is better than the change of C_{ds} in optimized LDMOS devices, can be exploited in advanced efficient circuit concepts. The extracted R_{ds} decreases by 25% with V_{DS} for the same device.

FET Transistor Delay Analysis

Based on the measurement of S-parameters and cut-off frequencies, FET delay times can be extracted. Various approaches have been published and been used for the delay time extraction for GaAs and InP devices, e.g., in [5.123, 5.168]. The typical finding for GaN HFETs is that the expected theoretical speed performance has not fully been exploited in real devices. Transistor delay analysis and extraction of the effective channel velocity for AlGaN/GaN HFETs are reported in [5.18, 5.130, 5.174, 5.176]. The approach according to Moll [5.123] assumes for the HFET device:

$$\frac{1}{2\pi \cdot f_T} = \tau_T = \tau_{RC} + \tau_D + \tau_{TR}. \quad (5.58)$$

In this case, τ_T is the total delay time, τ_{RC} is the channel-charge RC charging-delay, τ_D is the delay due to the extension of the depletion zone to the drain, and τ_{TR} is the transistor delay time. Parasitic de-embedding is crucial for the determination of realistic delays and velocities [5.180]. The extracted velocities for III-N devices from these approaches are typically lower than the simulated maximum velocities [5.54, 5.130]. Some issues in this discussion include the following:

- The parasitic effects of the source and drain region [5.131, 5.174, 5.180]
- The lack of the electron–phonon interaction in the MC simulations predicting the maximum velocities [5.210]

The stripping of masking parasitic effects, which can be accomplished in various ways [5.18, 5.180], is thereby of crucial importance. As is analyzed in [5.174], the parasitic effects can be eliminated, so that an intrinsic effective electron velocity of $1.86 \times 10^7 \text{ cm s}^{-1}$ in HFETs can be extracted. This latter value matches better some of the MC predictions for GaN bulk material [5.15]. At the same time, specific FET overshoot effects must be considered in the simulation for the comparison, e.g., [5.4, 5.144].

Example of Delay Time Analysis

As an example of the delay analysis, Table 5.5 gives the results of the extraction for an AlGaN/GaN device on s.i. SiC with gate lengths $l_g = 240$ and 120 nm. The delay time τ_{TR} in the channel scales with the gate length. The difference of the two examples is mainly based on the parasitic delay.

HBT Small-Signal Modeling

Al(In)GaN/GaN HBTs are so far only available with a limited gain performance. Npn-HBTs are characterized by high base resistances R_{bb} and high

Table 5.5. Extracted delay times for several AlGaN/GaN HEMTs

f_T (GHz)	l_g (nm)	τ_T (ps)	τ_{TR} (ps)	τ_{RC} (ps)	τ_D (ps)	Ref.
50	240	1.5	1.3	0	0.2	[5.50]
63	120	2	0.65	0.1	1.25	[5.174]

base contact resistances. This is reflected in the small-signal modeling. A distributed modeling is used for the description of the base transit time in AlGaN/GaN HBTs in [5.115]. A hybrid pi-small-signal-equivalent model of the active transistor is used, which is repeated 25 times to account for the base effect. InGaN/GaN HBTs have been proposed to solve the base resistance issues. The delay time analysis by simulation of npn-GaN/InGaN/GaN double heterojunction devices is provided in [5.36]. For a given base width, the GaN/InGaN/GaN DHBT is calculated to be superior in current gain cut-off frequency to the AlGaN/GaN/AlGaN DHBT. The simulated temperature dependence of the current gain cut-off frequency is found to be very weak between 300 and 500 K. Delay-time extraction examples of (In)GaN HBTs based on measurements are currently scarce.

5.4 Large-Signal Analysis and Modeling

Large-signal characterization and modeling are of great importance for III-N devices, which are genuine high-power devices intended for large-signal operation. A large number of large-signal characterization results exists for various types of substrates.

5.4.1 Large-Signal Characterization and Loadpull Results

Overview data for all substrates are already given in Chapter 2. Characterization examples of GaN HEMTs on s.i. SiC substrate can be found in [5.101, 5.116, 5.202]. They include fundamental, source, and harmonic load-pull analysis at various frequencies. A similar number of III-N devices has been investigated on sapphire substrates, especially for small gate widths of $\leq 200 \mu\text{m}$, e.g., [5.101, 5.192]. Large-signal properties of AlGaN/GaN HEMTs on high-resistivity silicon substrates are reported, e.g., in [5.176, 5.181]. The characterization for III-N devices is in principle not different from that for GaAs or silicon power devices; however, it is more challenging due to the following issues:

- Higher power densities lead to more pronounced thermal effects
- Higher operation voltages require more safety measures
- More testing is required due to the impact of dispersion [5.74]

- The high-voltage measurements require more safety measures in the case of device burn-out

These issues will be raised below wherever necessary.

Loadpull Measurement Results

As an initial example, Fig. 5.27 gives the measured output power, power-gain, and power-added efficiency data of an AlGaN/GaN HEMT on s.i. SiC as a function of input power at 10 GHz in cw-mode for a gate length $l_g = 250$ nm. The tuning of the output load is performed in passive mode. The gate bias is chosen for class-A/B operation with an quiescent current I_D with 10% of the $I_{D\max}$. The device in Fig. 5.27 yields power gain compression, although the passive load is constant. Some of this behavior can still be tracked to effects of dispersion and the onset of space charge effects [5.185]. However, a PAE=50% is reached at a low compression level of -2 dB at 10 GHz. The high PAE at low compression is important in order to maintain high efficiency on system level. The drain current I_D is depicted in Fig. 5.27, which increases with input power due to the self-biasing. On the contrary, Fig. 5.28 gives output power, gain, and power-added efficiency data as a function of input power at 40 GHz for an AlGaN/GaN HEMT on s.i. SiC substrate with $l_g = 150$ nm, measured with an active loadpull system. The active system is used in this case in order to

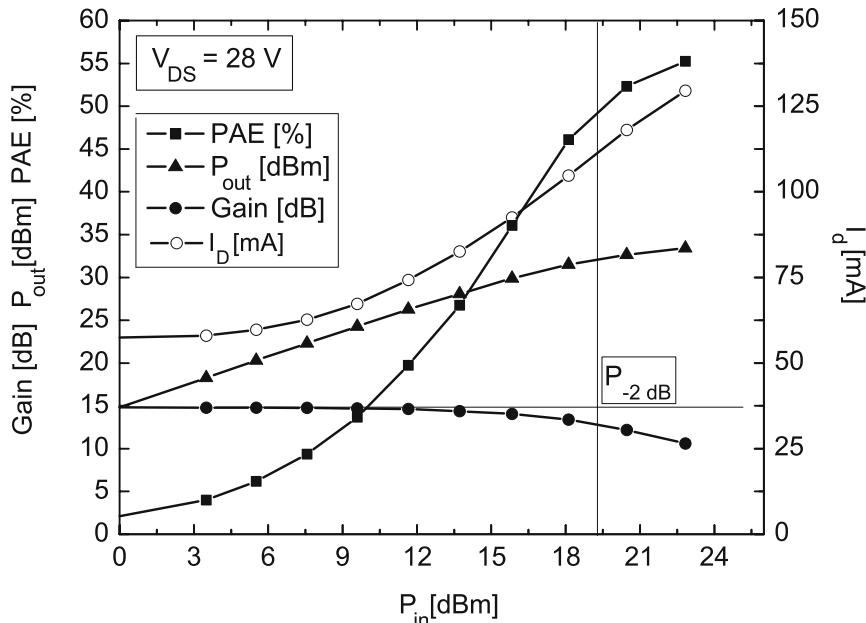


Fig. 5.27. Power sweep of P_{out} , gain, and PAE as a function of P_{in} for a $0.25 \mu\text{m} \times 8 \times 60 \mu\text{m}$ AlGaN/GaN HEMT at 10 GHz

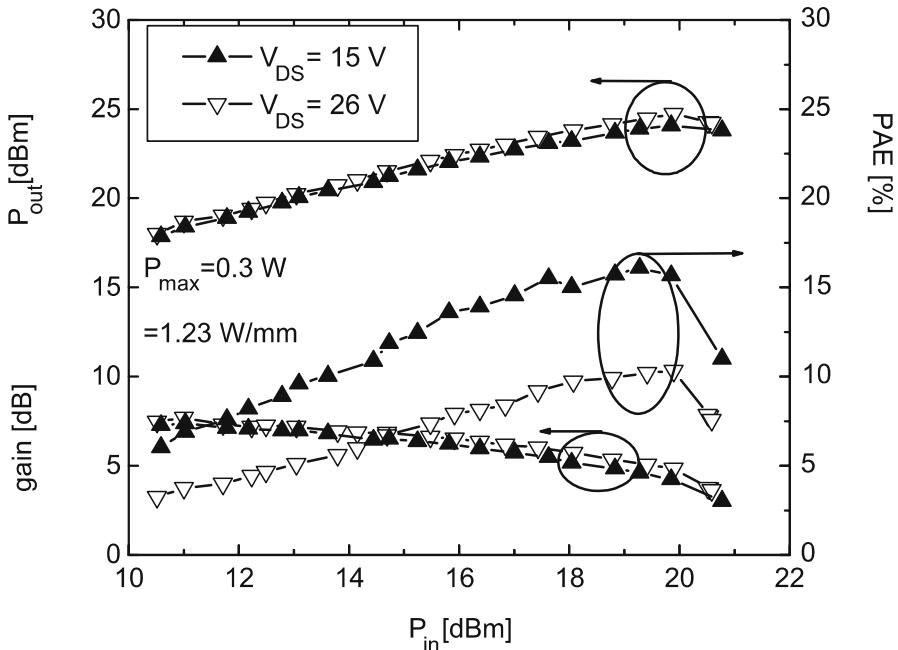


Fig. 5.28. Power sweep P_{out} , gain, and PAE vs. P_{in} of a $0.15 \mu\text{m} \times 8 \times 30 \mu\text{m}$ HEMT at 40 GHz

reach the required output load reflection coefficients for the $8 \times 30 \mu\text{m}$ device at 40 GHz. Again a premature compression is visible; in this case, however, this is partly due to the change of the active load impedance. Pulsed-power measurements help to reduce the impact of the thermal effects, while the impact of the dispersion is dependent on the pulse width. A pulsed-DC- and RF-loadpull setup is presented in [5.22] for the evaluation of GaN HEMTs under pulsed-conditions including measurements of the intermodulation distortion.

Load Impedance Dependence

Fig. 5.29 gives loadpull contours of an AlGaN/GaN HEMT on s.i. SiC with a gate width $W_g = 8 \times 60 \mu\text{m}$ measured at 10 GHz for an input power of 24 dBm. While in first order the optimum load impedance as a function of gate width at 2 GHz shows a nearly ohmic behavior in the Smith chart, for higher frequencies at 10 GHz an additional contribution is needed for the output capacitance C_{ds} . For a bias $V_{DS} = 25$ V, an optimum output impedance reflection $\Gamma = (0.45/28^\circ)$ for a 50Ω system is found by loadpull measurements for the device in Fig. 5.29. As a major finding, III-N devices are always considered to be high impedance devices. However, a strong influence is also due to the parasitics device environment. This is shown for a passive loadpull measurement at 60 GHz in Fig. 5.30 for a device with $W_g = 2 \times 50 \mu\text{m}$.

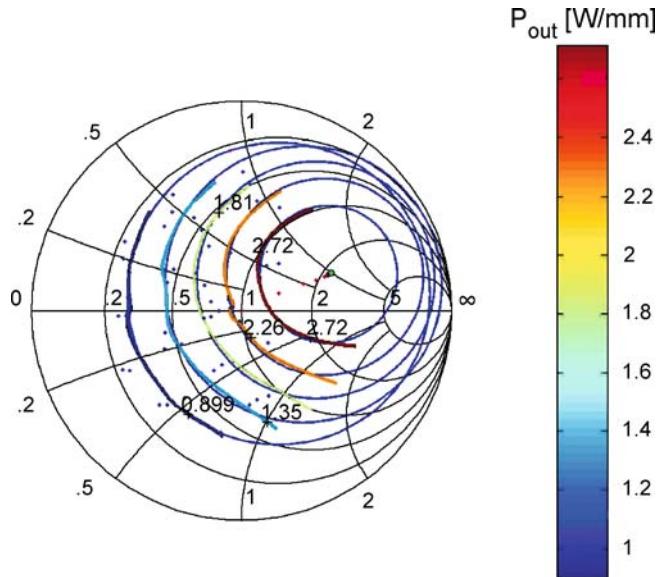


Fig. 5.29. P_{out} characteristics forming loadpull contours of an AlGaN/GaN HEMT with $W_g = 8 \times 60 \mu\text{m}$ and $l_g = 300 \text{ nm}$ at 10 GHz at an input power of 24 dBm and $V_{DS} = 25 \text{ V}$, reference impedance 50Ω

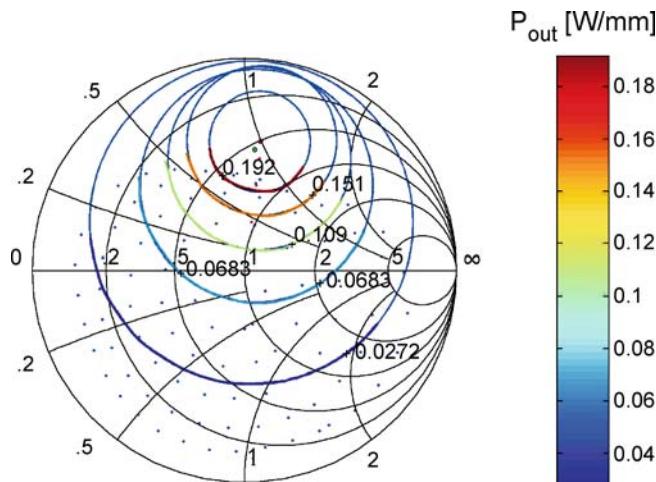


Fig. 5.30. P_{out} characteristics forming loadpull contours of an AlGaN/GaN HEMT with $W_g = 2 \times 50 \mu\text{m}$ and $l_g = 100 \text{ nm}$ at 60 GHz at an input power of 7.1 dBm at $V_{DS} = 30 \text{ V}$, reference impedance 50Ω

and a gate length $l_g = 100 \text{ nm}$. The intrinsic impedance level is transformed through the additional parasitic network representing the layout. This leads to strong deviations from the expected intrinsic high impedance at the device

terminals, especially at frequencies higher than a few gigahertz. The optimum load has a strong imaginary part that renders the matching difficult despite the higher intrinsic impedance as compared to GaAs PHEMTs of the same gate length and width. Fig. 5.31 gives the dynamic loadline of an AlGaN/GaN HEMT similar to Fig. 5.29, measured at 10 GHz including higher harmonics at $V_{DS} = 30$ V. From these measurements, the actual tuning of the output load can be controlled relative to the DC- and pulsed-output characteristics of the device. Further, the LS-prediction of the LS-modeling can be effectively verified. This analysis also allows the direct measurement of the impact of the knee walk-out and reduced RF-breakdown, see also [5.64, 5.186]. The thermal effect on the knee voltage can be suppressed by pulsed large-signal measurements [5.51]. As we see, the output swing in Fig. 5.31 is not fully symmetric to the DC-operation bias at $V_{DS0} = 30$ V. The self-biasing with increasing input

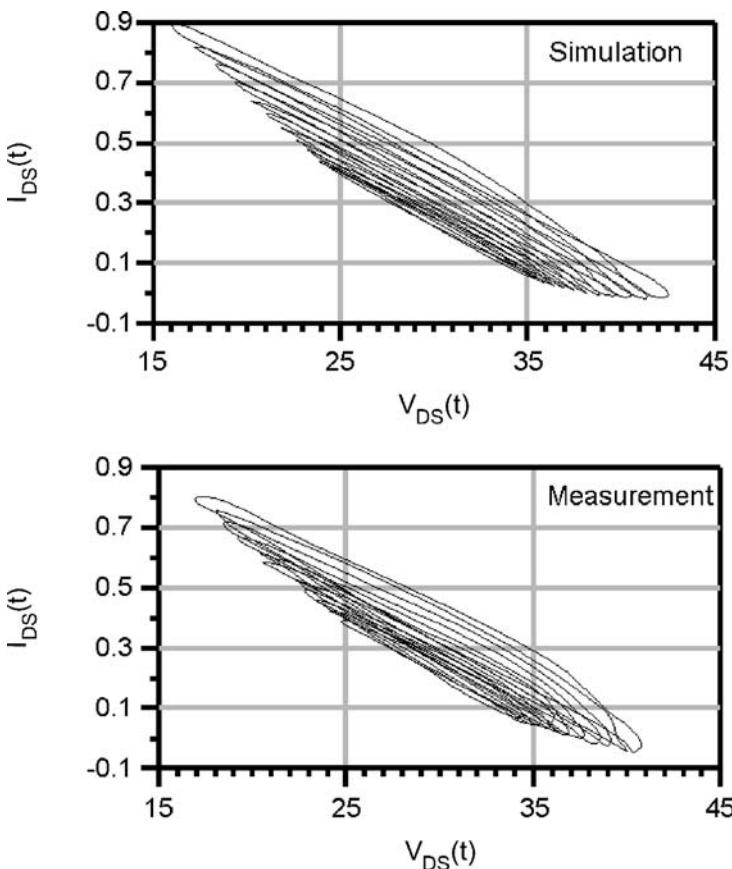


Fig. 5.31. Dynamic loadline of a GaN HEMT with $0.3\text{ }\mu\text{m} \times 8 \times 125\text{ }\mu\text{m}$ at 10 GHz and $V_{DS} = 30$ V, simulation (top), measurement (bottom)

drive is also visible. Similar data is provided in [5.116]. A related approach is used in [5.192] to reconstruct the load impedance influence on the $I_D(V_{DS})$ characteristics of AlGaN/GaN HEMTs on sapphire at 4 GHz.

Bias Dependence of Large-Signal Measurement Results

Several experiments have been performed to investigate the fundamental frequency behavior [5.64]. The bias-dependent performance of high-power AlGaN/GaN HEMTs is described, e.g., in [5.202], featuring a maximum PAE of 60%. This bias dependence involves some important characteristics:

- The maximum output power as a function of V_{DS}
- The maximum PAE as a function of V_{DS}
- The V_{GS} dependence, which defines the amplifier operation between class-A and C

Fig. 5.32 gives a comparison of the maximum in PAE as a function of V_{DS} bias for two different GaN/AlGaN HEMT technologies for the same gate length l_g . It can be seen that the maximum in PAE differs between the technologies investigated. The technology including a field plate yields PAE improvements, especially at higher V_{DS} -voltage. To estimate the potential for a given operation bias V_{DS} , Fig. 5.33 gives the calculated Cripps-load [5.41] and Cripps-output power up to an operation voltage of up to $V_{DS} = 150$ V, in order to

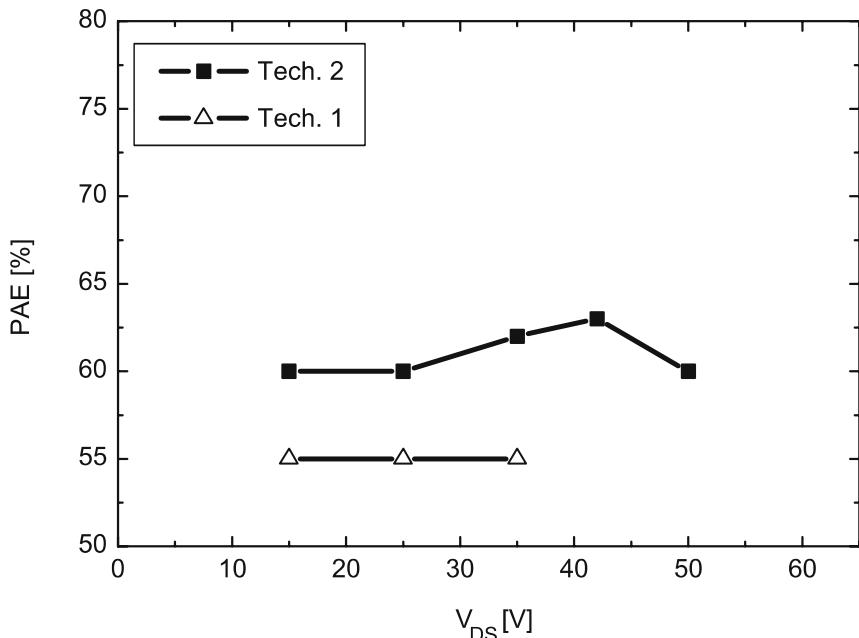


Fig. 5.32. PAE of an AlGaN/GaN HEMT on s.i. SiC as a function of V_{DS} with $W_g = 2 \times 400 \mu\text{m}$ and $l_g = 500 \text{ nm}$ at 2 GHz

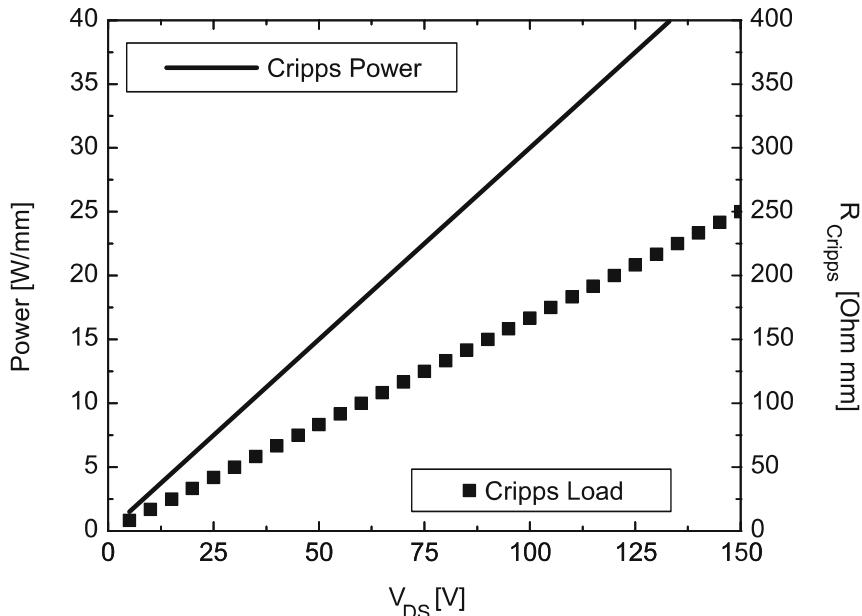


Fig. 5.33. Calculated Cripps-impedance and output power of an AlGaN/GaN HEMT with $I_{D\max} = 1.2 \text{ A mm}^{-1}$ as a function of V_{DS}

allow a comparison to measured loadpull results. The assumed current $I_{D\max}$ is 1.2 A mm^{-1} . The results strongly suggest the higher impedance level for a GaN HEMT relative to GaAs or silicon-based devices. A load of $50 \Omega \text{ mm}$ is reached approximately at $V_{DS} = 25 \text{ V}$.

5.4.2 Large-Signal Modeling

The modeling of RF-devices is, in general, a highly complex problem with a great amount of degrees-of-freedom and dependencies [5.1]. A lot of research has already been performed into the inclusion of several effects into large-signal models, e.g., [5.7, 5.10, 5.43, 5.45, 5.111, 5.170]. At the same time, these models have to remain useful, i.e., they have to be simple and simulation-time-efficient while accurate for circuit simulation. As a simple example, SPICE models of GaN devices have been reported, e.g., in [5.70]. They allow for the analysis of the devices, especially in the time-domain.

What is Different About III-N Devices?

With the aforementioned arguments and the long tradition of semiconductor modeling, one has to ask, what is so special about the III-N devices and why spend extra effort on modeling them. Fig. 5.34 depicts the frequency spectrum, the associated physical effects, and some typical characterization methods for

the large-signal modeling. III-N devices certainly do not differ in principle from any other semiconductor devices. However, some effects are more pronounced and require special attention. Further, some of the suggested new applications pose stringent requirements and open new aspects for characterization and modeling in general with regard to the frequency spectrum. First of all, on the device level GaN devices maintain the troublesome low-frequency-noise characteristics of any III-V FET device [5.194]. With regard to the domain of highly-linear power RF-amplifiers, they combine the handling of extremely high-power densities of 40 W mm^{-1} [5.204] at 4 GHz, exceeding those that have been available so far. The high power levels also lead to higher linearity for a given output power level. At the same time, given the same power level as in conventional devices, reduced thermal effects are observed, especially on SiC substrate. This includes the reduction of critical memory effects that cannot fully be compensated by predistortion in silicon LDMOS devices, e.g., [5.21]. This reduction in memory effects allows to drive GaN devices at higher power levels and closer to the saturation applying memoryless predistortion. Higher frequencies in Fig. 5.34 and Fig. 5.35 become interesting, e.g., for efficiency improvements by means of harmonic termination. These findings are especially critical, because the system requirements drastically change. The new signal forms with nonconstant signal envelopes, especially of 3G/4G mobile-communication-systems, cover the full frequency range in Fig. 5.34 and Fig. 5.35, virtually from 0 Hz to the cut-off frequencies f_T and

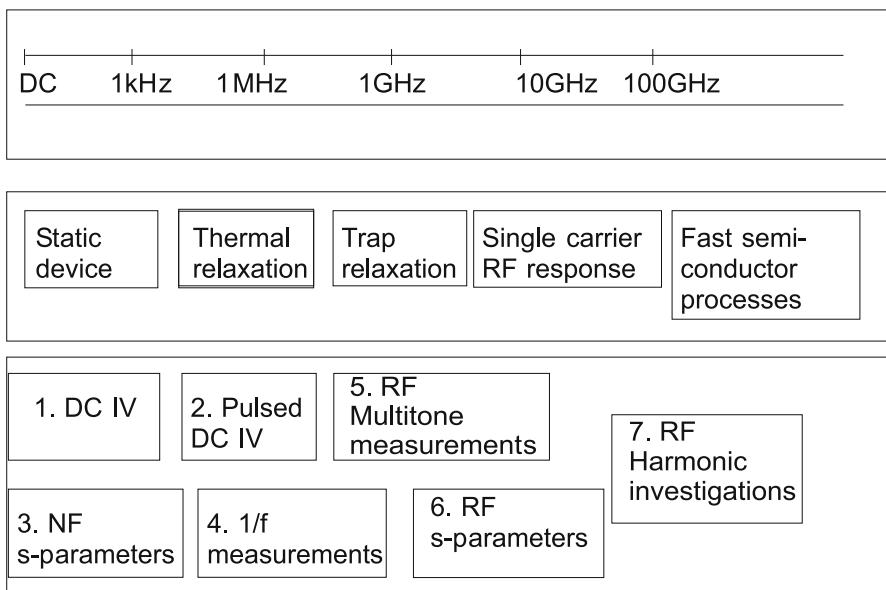


Fig. 5.34. Frequency spectrum and principal overview of RF-device effects and analysis tools

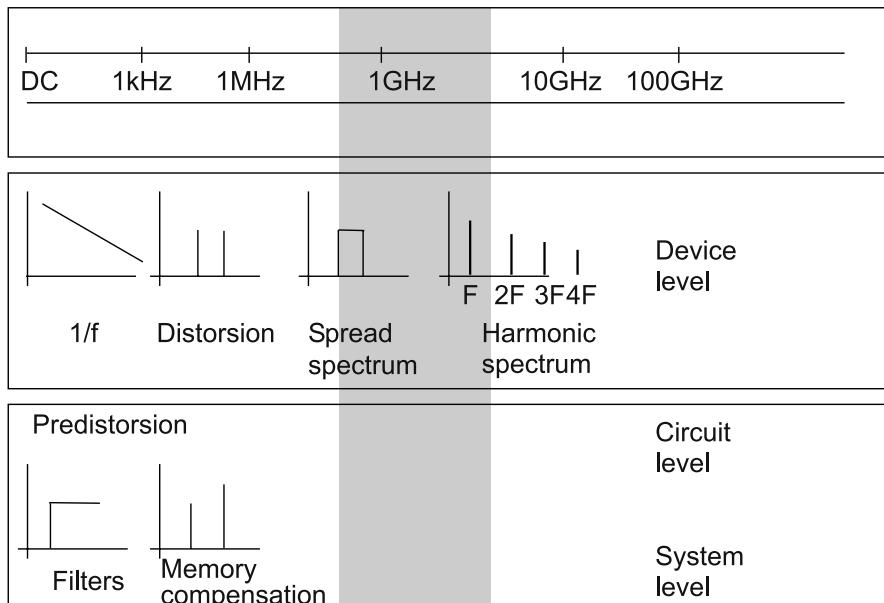


Fig. 5.35. Frequency spectra of importance for circuit and system design

f_{\max} of the device. This complete frequency range is of primary importance, as the RF-carriers are modulated by extremely broad spectra, potentially ≥ 20 MHz. RF-frequency-dispersion thus remains a challenge for the modeling. All these facts relevant for the modeling are illustrated in Fig. 5.35 with respect to the resulting circuit and system design issues. On system level, mainly predistortion and filtering issues are important, as discussed further in [5.52].

LS-Analysis Based on Small-Signal Parameters

A large number of publications is available on large-signal models based on the extraction from small-signal S-parameters in the frequency-domain [5.10, 5.43, 5.111]. These methodologies are well known from the GaAs FET world, where they are widely used [5.201]. The problem of large-signal model analysis and extraction can be broken down into two problems: the extraction of the charge parameters and the extraction of the current equations. First of all small-signal-based approaches have been adopted for GaN FETs, e.g., [5.7]. Derived from small-signal-based approaches, Fig. 5.36 gives the topology of a large-signal model suitable for III-N HFET device. However, the extraction procedures have to be modified. A description of the theoretical background of the principal modeling procedure in a state-space approach is given in [5.166].

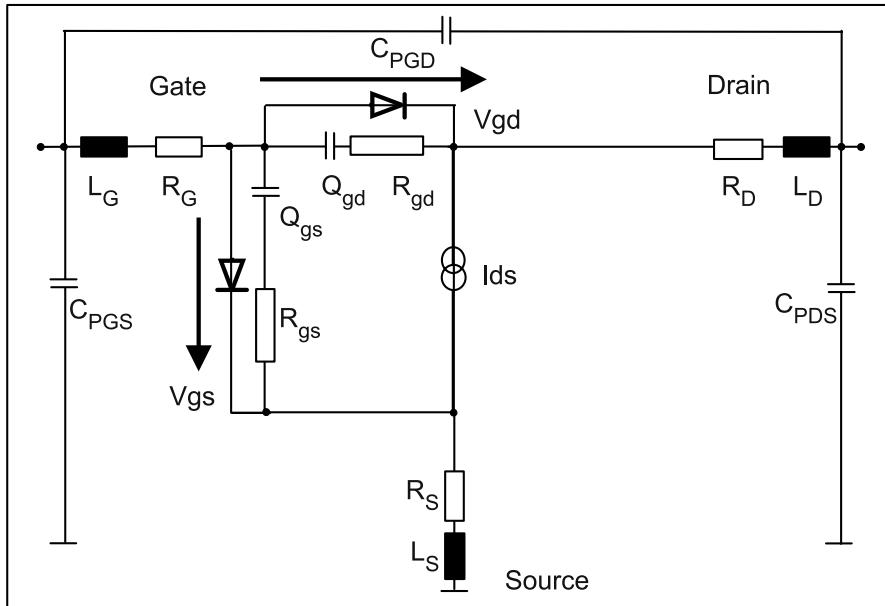


Fig. 5.36. Topology of a large-signal model of an AlGaN/GaN HFET

Analytical Approaches

Analytical current equations are widely used for the description of the DC- and RF-currents, e.g., [5.10, 5.43, 5.190]. They combine simulation efficiency with good modeling accuracy. Typical current equations for the description of the transfer characteristics based on the cubic Curtice approach read [5.170]:

$$I_{DS} = (A_0 + A_1 \cdot V_1 + A_2 \cdot V_1 + A_2 \cdot V_1^2 + A_3 \cdot V_1^3) \tanh(\gamma V_{DS}), \quad (5.59)$$

$$\text{where } V_1 = V_{GS} \cdot (1 + \beta \cdot (V_{DS0} - V_{DS})). \quad (5.60)$$

Both the simple V_{GS} description and the simplified V_{DS} description do not allow an accurate modeling of all the GaN HEMTs DC- and RF-characteristics. However, the model and its derivations have been widely used as an initial approach for modeling [5.44, 5.141, 5.142]. The model is simple and simulation-time-efficient and can be tweaked efficiently even for advanced circuit simulation [5.141], however, only if applied correctly. The extraction and validation of an analytical Curtice large-signal model for AlGaN/GaN HEMTs are provided in [5.63]. The analytical model uses the cubic Curtice-based current equation approach [5.43, 5.45]. A model for a $0.3\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ AlGaN/GaN HEMT on sapphire substrate is extracted. It is verified between 0.5 and 26.5 GHz for the S-parameters and further by time-domain large-signal measurements at 4 GHz. A similar temperature-dependent nonlinear analytical model for AlGaN/GaN HEMTs on s.i. SiC is given in [5.95, 5.199]. In this

case, the Curtice model of (5.59), (5.60) is slightly modified for the large-signal current equation and includes self-heating effects. The extraction procedure includes extensive pulsed-IV-measurements with pulse widths tuned to avoid the trapping time constants. These pulsed-measurements are also used to analyze the thermal effects and to extract the thermal coefficients and the thermal resistances. Cree reported the use of the modified Curtice current approach with four bias regions for the modeling of SiC MESFETs and GaN HEMTs [5.138, 5.141]. No additional information is given due to intellectual property constraints. The model is similar to the approach used in [5.56]. In general, the Curtice-based approaches need further modifications for the description of intermodulation and other linearity characteristics, as the higher order derivatives of the current equation are zero or trivial, due to the particular polynomial approach for the analytical current equation [5.181]. Other approaches, such as the Angelov and other analytical approaches, will be discussed below [5.181, 5.190].

Table-Based Models for GaN Devices

As an alternative to analytical approaches, table-based models have been developed, e.g., for GaAs devices in [5.8]. The table-based models yield higher modeling accuracy, while the typical numerical effort during simulation is higher, typically in the order of a factor of 1–2 in the simulation time compared to analytical approaches. The interpolation schemes have to be verified and analyzed critically in order to insure the accuracy and numerical efficiency [5.118] of the linearity modeling when using, e.g., cubic spline interpolation, see [5.154]. Table-based models for GaN HEMTs are given, e.g., in [5.118], based on GaAs approaches. The equivalent-model-elements are extracted from S-parameters and cw- and pulsed-DC-IV-measurements. Particularly, gridding and interpolation issues for dense and large gridding are discussed and optimized for numerical efficiency. The table-based data has been both extrapolated and interpolated from the measurements in order to enhance convergence speed and accuracy. Examples for further models are given below.

Aspects of Charge Modeling

The second issue of large-signal modeling is charge extraction and modeling. Both static and quasi-static approaches are used. Charge-storage is the major contributor to the linear behavior of a device, and, next to the current-source nonlinearities, a major source of nonlinearities [5.152]. A big challenge is to meet the requirement of charge conservation within the modeling approach or integrability [5.155] as this has also been an issue for the modeling of GaAs FETs. A general survey of nonlinear-charge modeling and its impact on the description of nonlinear device quantities is given in [5.152] for various device technologies such as Si, GaAs, and InP FETs. The modeling constraints of terminal charge conservation and energy conservation, and the necessary and

sufficient conditions for the construction of unique device-specific nonlinear models from experimental device data are discussed. The focus of this paper is the accurate description of PAE, IP3, and ACPR. This generalized approach is further extended to GaN HFETs in [5.166]. Examples of GaN FETs modeling are given in [5.166] for the modeling in a state-space approach. This state-space approach is used as a general framework for various model descriptions of the dispersive features of the GaN HFETs.

Several charge modeling examples are available for FETs. The Curtice model uses a linearized model of C_{gs} and C_{gd} around the operating bias; for details see [5.170]. The Chalmers model provides the following equations for a GaAs PHEMT for the charges and capacitances:

$$C_{gs} = C_{gs,0}[1 + \tanh(\psi_1(V_{GS}))][1 + \tanh(\psi_2(V_{DS}))], \quad (5.61)$$

$$C_{gd} = C_{gd,0}[1 + \tanh(\psi_3(V_{GS}))][1 - \tanh(\psi_4(V_{DS}))]. \quad (5.62)$$

The functions ψ_i are polynomials of the voltages given in the argument. Charge modeling of GaN FETs is given in [5.7]. In this case the modeling is based on an extended charge approach derived from the GaAs PHEMT world in [5.6]. In some cases, intermodulation parameters and even ACPR can be reliably predicted, if charge-storage effects are included during the extraction of table-based LS-models, see [5.30, 5.118]. Charge conservation is traded off vs. simulation accuracy, and its violation poses the need for improved and consistent modeling. The issue of charge conservation is further discussed in [5.153]. The charge conservation issue is reduced to a local charge conservation approach. The dynamic charge relaxation can further be described by a relaxation time approach [5.59, 5.155]. The requirements of integrability or charge conservation are found crucial for the description of the dynamic relaxation due to thermal or trap relaxation effects.

Examples of Analytical Current Equations for GaN HFETs

The detailed description of the current relations is the first problem for the extraction of a large-signal model. The extraction of the RF-transconductance g_m and RF-output-conductance g_{ds} for the various bias and temperature situations remains a fundamental problem, e.g., [5.1]. Equations (5.63) and (5.64) give the basic current equations used for FETs according to Angelov [5.5]:

$$I_{DS} = I_{pk} \cdot (1 + \tanh(\psi)) \tanh(\alpha \cdot V_{DS})(1 + \lambda V_{DS}) \quad (5.63)$$

$$\psi = P_1(V_{GS} - V_p) + P_2(V_{GS} - V_p)^2 + P_3(V_{GS} - V_p)^3 + \dots \quad (5.64)$$

The equations contain several fitting parameters, and further functions (P_i), which can be used to include dispersion, as detailed further. The typical LS-models of Angelov [5.5, 5.6, 5.9–5.11], Materka [5.111], and Curtice [5.43, 5.45, 5.170] are used for GaAs MESFETs and PHEMTs. The basic distinction between these models is not so much the accuracy, but the inclusion of thermal

effects, the better description of the derivatives, and of the related linearity performance. The main difference between the models thus also includes the V_{DS} -dependence of the threshold voltage [5.30, 5.44] in order to model the particular shape of the transfer and output characteristics [5.5]. An extension of the Angelov approach [5.11] more suitable for GaN HEMTs is reported in [5.190] and reads

$$I_{DS}(V_{GS}, V_{DS}) = I_0(1 + \tanh(\psi_1)) + \frac{(1 + \lambda V_{DS})}{1 + \tanh(\psi_2)\psi_3} \cdot \tanh(\alpha V_{DS}), \quad (5.65)$$

$$V_p = V_{p0} - \delta \cdot V_{DS}, \quad (5.66)$$

$$\begin{aligned} \psi_1 &= P_{11}(V_{GS} - V_p) + P_{21}(V_{GS} - V_p)^2 \\ &\quad + P_{31}(V_{GS} - V_p)^3, \end{aligned} \quad (5.67)$$

$$\begin{aligned} \psi_2 &= P_{12}(V_{GS} - V_p) + P_{22}(V_{GS} - V_p)^2 \\ &\quad + P_{32}(V_{GS} - V_p)^3, \end{aligned} \quad (5.68)$$

$$\begin{aligned} \psi_3 &= \alpha_3 \cdot (V_{DS} - V_{GS} - V_{DS0}) + \beta_3 \cdot (V_{DS} - V_{GS} - V_{DS0})^2 \\ &\quad + \gamma_3 \cdot (V_{DS} - V_{GS} - V_{DS0})^3. \end{aligned} \quad (5.69)$$

This model has been modified again and applied directly to (dispersive) GaN HEMTs, as described in [5.7]. The modified current equations include

$$I_{DS} = 0.5 \cdot (I_{DSP} - I_{DSn}), \quad (5.70)$$

$$P_1 = g_{m,\max}/I_{pk0}, \quad (5.71)$$

$$\begin{aligned} I_{DSP}(V_{GS}, V_{DS}) &= I_{pk0} \cdot (1 + \tanh(\psi_p))(1 + \tanh(\alpha_p V_{DS})) \\ &\quad (1 + \lambda_p \cdot V_{DS} + L_{sb0} \exp(V_{GD} - V_{thr})), \end{aligned} \quad (5.72)$$

$$\begin{aligned} I_{DSn}(V_{GS}, V_{DS}) &= I_{pk0} \cdot (1 + \tanh(\psi_n))(1 - \tanh(\alpha_n V_{DS}))(1 - \lambda_n \cdot V_{DS}), \\ \psi_p &= P_{1m}(V_{GS} - V_p) + P_{2m}(V_{GS} - V_p)^2 \\ &\quad + P_{3m}(V_{GS} - V_p)^3, \end{aligned} \quad (5.73) \quad (5.74)$$

$$\begin{aligned} \psi_n &= P_{1m}(V_{GS} - V_p) + P_{2m}(V_{GS} - V_p)^2 \\ &\quad + P_{3m}(V_{GS} - V_p)^3, \end{aligned} \quad (5.75)$$

$$V_p(V_{DS}) = V_{pks} - \Delta V_{pks} + \Delta V_{pks} \tanh(\alpha_S V_{DS} + K_{bg} V_{bgate}), \quad (5.76)$$

$$P_{1m} = P_1(f(T)) \cdot [(1 + \Delta P_1)(1 + \tanh(\alpha_S V_{DS}))], \quad (5.77)$$

$$P_{2m} = P_2(f(T)) \cdot [(1 + \Delta P_2)(1 + \tanh(\alpha_S V_{DS}))], \quad (5.78)$$

$$P_{3m} = P_3(f(T)) \cdot [(1 + \Delta P_3)(1 + \tanh(\alpha_S V_{DS}))], \quad (5.79)$$

$$\alpha_p = \alpha_R + \alpha_S \cdot (1 + \tanh(\psi_p)), \quad (5.80)$$

$$\alpha_n = \alpha_R + \alpha_S \cdot (1 + \tanh(\psi_n)). \quad (5.81)$$

The modification mainly consists in increasing the flexibility to react to the effects of dispersion during the extraction, while keeping the number of parameters low. The introduction of K_{bg} controls the dispersion. The parameters ΔP_i allow the adjustment of the linearity. The temperature dependence of the

carrier velocity is modeled in the functions $P_i(f(T))$. According to [5.7] these modifications allow an accurate modeling of the DC- and RF-S-parameters for GaN HFETs with small gate widths. The main issue quoted in [5.7] is the modeling of both increasing and decreasing transconductance with the drain voltage V_{DS} . A similar idea has been pursued in [5.190]. However, even if the small-signal parameters can be matched accurately for a wide bias- and frequency-range, the modeling of the large-signal and linearity characteristics is not certain and needs further consideration, for details, see [5.166].

Large-Signal Models: Dispersion Modeling

Modeling of modifications of the quasi-static behavior of devices is necessary due to the strong impact of both dispersion and thermal effects. This insight leads to the need of the separation of thermal effects from dispersion.

An Initial Approach for Dispersion Modeling

Initial modeling for the inclusion of dispersion of the output conductance g_{ds} and transconductance g_m [5.61] in an FET can be achieved by additional elements in the equivalent-circuit model. A very simple example of an equivalent circuit is given in Fig. 5.37. The modeling of the complex output conductance Z_{ds} and transconductance g_m reads

$$Z_{ds} = \frac{R_{ds} \cdot [1 + \omega C_{ss} R_{ss}]}{1 + i \omega C_{ss}[R_{ss} + R_{ds} + g_{m2} \cdot R_{ss} R_{ds}]} \quad (5.82)$$

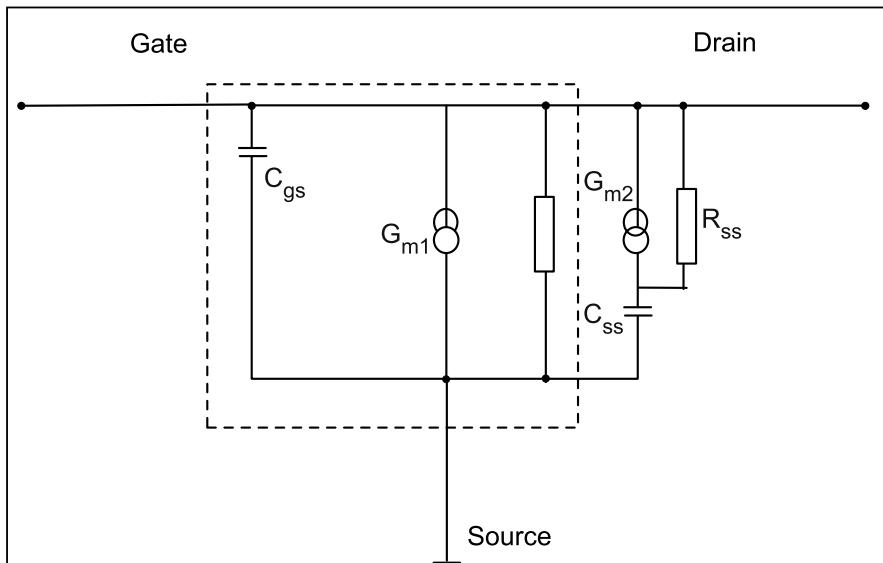


Fig. 5.37. Simplified dispersion equivalent circuit model for a GaAs FET

$$g_m(t) = g_{m1} - g_{m2} \left[\frac{i \omega C_{ss} R_{ss}}{1 + i \omega C_{ss} R_{ss}} \right]. \quad (5.83)$$

In the DC-case ($\omega = 0$) and RF-case ($\omega = \infty$), the values of g_m and g_{ds} amount to

$$Z_{ds,DC}(\omega = 0) = R_{ds}, \quad (5.84)$$

$$g_m(t)(\omega = 0) = g_{m1}, \quad (5.85)$$

$$Z_{ds,RF}(\omega = \infty) = \frac{R_{ds}}{1 + R_{ds}[1/R_{ss} + g_{m2}]}, \quad (5.86)$$

$$g_m(t)(\omega = \infty) = g_{m1} - g_{m2}. \quad (5.87)$$

We see that the additional current generator g_{m2} and the additional RC combination modify both the transconductance g_m and output conductance g_{ds} in the requested manner. A physics-based large-signal model for HFETs including the substrate-induced drain-lag is reported in [5.92]. Similarly to Fig. 5.37, the equivalent circuit for a GaAs HFET is modified by additional elements. In the circuit model, electron generation/recobination in deep traps are expressed by a parallel circuit consisting of a diode and a resistor, which are deduced from SRH statistics. The model agrees well with two-dimensional simulation results and experimental current-transient data for large-signal voltage steps. An improved large-signal model more suitable for the simulation of integrated circuits is provided in [5.113]. It models the onset of the low-frequency dispersion in GaAs HFETs. The idea is very similar to that presented in Fig. 5.37. Fig. 5.38 gives the equivalent circuit of this model. In addition to the intrin-

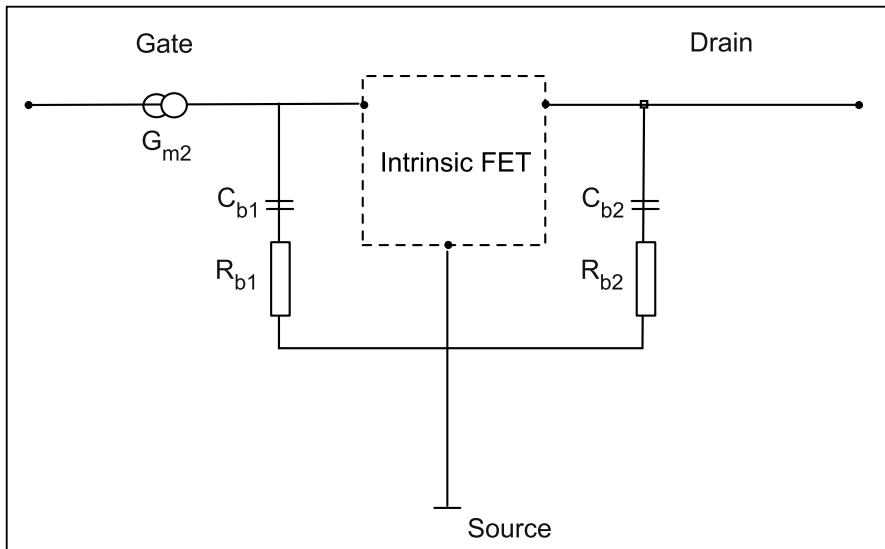


Fig. 5.38. Dispersion equivalent circuit model for a GaAs HFET

sic HFET model, an additional high-resistance network is implemented for the modeling of dispersion and current-lag. The output impedance and the pulse response of a GaAs HFET can be modeled precisely. All these initial approaches modify the relevant elements according to their behavior. A more extensive filter network is used for GaAs PHEMTs in [5.23] to model the pulsed-characteristics and even intermodulation distortion. Even the time-domain response of a 3GPP-WCDMA signal can be simulated in the baseband.

Modifications of the Current Equations

Modeling approaches for the inclusion of dispersive effects have already been presented with (5.65)–(5.69). Another approach is provided in (5.70)–(5.78). The dispersion is modeled according to the modification of the RF-drain-current-characteristics. The classical modification of the analytical current equation in the Angelov large-signal model is taken from [5.6]. The currents are initially modified as

$$\begin{aligned} I_{DS,RF} \left[V_{GS}(t), V_{DS}(t) \right] &= I_{DS,DC} \left[V_{GS}(t), V_{DS}(t) \right] \\ &\quad + \Delta I_{DS} \left[V_{GS}(t), V_{DS}(t) \right] + \Delta I_{DS}^- \left[V_{GS}(t), V_{DS}(t) \right]. \end{aligned} \quad (5.88)$$

The dispersion is included by the appropriate modification of the P-factors in (5.63) and (5.64). One example of this modification has been presented in [5.7] and (5.70)–(5.81).

Gate-Lag Modeling in Large-Signal Models for GaN HFETs

To this point, the initial modeling mainly modifies the bias-dependent small-signal equivalent circuit elements. A first approach to a dispersion correction in a real LS-model uses a frequency-dependent modification of the internal terminal bias, mostly of the V_{GS} bias, as reported in [5.79]. The gate voltage modification scheme is composed as

$$V_{GS,X} = \bar{v}_{gs} + \alpha_1 \cdot (v_{ds}(t) - \bar{v}_{ds}) + \alpha_2 \cdot (v_{gs}(t) - \bar{v}_{gs}) \quad (5.89)$$

with \bar{v}_{gs} and \bar{v}_{ds} being the static voltage components. This new $V_{GS,X}$ is inserted into the current function:

$$I_{DS} = f(V_{GS,X}, v_{ds}). \quad (5.90)$$

This methodology can be easily introduced into any large-signal model.

Another LS-model for the virtual gate effect in GaN HFETs is proposed in [5.39]. The model is based on the Agilent EEHEMT model and intends to model anomalous transients in the bias for high quiescent V_{DS0} based on surface states. A parasitic FET device is inserted in the drain path, including a voltage control circuit network, which controls the virtual gate and adjusts

the gate voltage according to the V_{DS} bias. This virtual gate model can be very flexibly adjusted to the appropriate quiescent bias and drain pulse width situations. The verified pulse width range amounts to $100\text{ ns} \leq t \leq 1\text{ ms}$ for a GaN HFET with $l_g = 150\text{ nm}$.

Drain-Lag Modeling in Large-Signal Models for GaN HFETs

A more elaborate description of the dispersion is truly two-dimensional with respect to V_{GS} and V_{DS} , as is suggested in [5.73, 5.74]. The idea of a virtual gate-lag model [5.39] can be extended to a drain-lag model based on the equivalence of drain-lag and self-backgating effects [5.73]. In first order, drain-lag effects are physically caused by trapping underneath the channel. The space charge created by the traps and changed by the drain bias adds a contribution to the (V_{DS} -dependent) pinch-off voltage V_{thr} and can be appropriately described. Depending on the time constants observed during the modeling of the feedback of this self-backgating, the virtual gate is dynamically adjusted once a drain voltage pulse is applied. The critical equation is [5.73]:

$$k_n = k_{rel\,n} \cdot g_m(V_{GS} - V_{thr}). \quad (5.91)$$

$k_{rel\,n}$ is the trap transient of the n th trap, which reacts to the drain current pulse, and translates into the dynamic adjustment of the actual control voltage at the gate terminal.

Large-Signal Models: Diodes and Ohmic Contacts

Additionally, the RF-modeling of diodes and ohmic contacts in FET has always been an important topic. Examples of the large-signal modeling of two-terminal GaAs RF-diodes are given, e.g., in [5.156]. The forward AC behavior of n-GaN Schottky diodes are analyzed in [5.198]. Negative capacitance and an additional interfacial layer are considered at the Schottky interface which leads to a nonlinear capacitive effect.

In the linear device region, ohmic contacts in wide-bandgap semiconductor devices yield a diode type contribution, as is pointed out, e.g., in [5.184]. The band structure near the ohmic contacts leads to nonlinear transport effects at both drain and source. The nonlinear source-resistance effects are described in [5.184, 5.185]. The source-resistor modulation and its bias dependence are discussed. As a result, a space-charge zone is extracted below the source which limits both RF-performance and amplifier linearity. The effect is primarily visible during the high current portion of the RF-cycle. However, a direct description of this nonlinear behavior in a lumped LS-model without physical device simulation has not been presented.

Soft-Breakdown and Impact Ionization

In the high-field-bias-domain, breakdown mechanisms in III-N devices can be included into the large-signal model, as reported in [5.186]. Additional

reverse current generators to the gate current, similar to those already considered for dispersion modeling, are included parallel to the gate–source and source–drain diode. They can describe both tunneling-induced breakdown and channel breakdown. The extraction example in [5.186] gives a good agreement for the modeling of leaky GaN HFETs with a strong difference in the DC- and RF-breakdown voltages. Other typical modifications are made to the output conductance and can be incorporated due to soft breakdown or direct impact ionization, as performed for the Angelov-model in [5.6]. The modeling of the modification of the drain current due to impact ionization in [5.133] yields

$$i_{II} = A \cdot I_{DS} \exp\left(\frac{-B}{V_{DS} - V_{DS0}}\right). \quad (5.92)$$

The inclusion of soft-breakdown into LS-modeling is further described in [5.6]. Soft-breakdown may not be a dominant issue in AlGaN/GaN devices; however, the particular behavior of small-gate-length devices ≤ 150 nm may require this feature. The drain current is modeled by the insertion of L_{sb} into the standard current equation according to

$$I_{DS}(V_{GS}, V_{DS}) = I_0(1 + \tanh(\psi)) \cdot \tanh(\alpha V_{DS}) \cdot (1 + \lambda V_{DS} + L_{sb}), \quad (5.93)$$

$$L_{sb} = L_{sb0} \cdot [\exp(L_{sd1}V_{dgt} + \dots) - 1], \quad (5.94)$$

$$V_{dgt} = \frac{V_{DS} - K_{trg} V_{GS}}{V_{tr}}, \quad (5.95)$$

$$L_{sd1} = L_{d1}(1 - L_{g1} V_{GS}). \quad (5.96)$$

The dots in (5.94) indicate potential higher orders in the voltages. This modeling can be included to match the DC-gds, especially in the near-breakdown V_{DS} region.

Large-Signal Models: Thermal Analysis

Thermal and self-heating effects are very pronounced in any power semiconductor device, e.g., [5.167]. Several variants exists for the inclusion of thermal and especially self-heating effects in LS-models. The additional inclusion of the thermal effects in the Curtice model for GaN HFET is reported in [5.95]. The channel temperature T_{chan} to be used in a temperature-dependent version of (5.60) is modeled in a global approach in [5.71]

$$T_{chan} = R_{th} \cdot V_{DS} \cdot I_{DS} + T_0. \quad (5.97)$$

R_{th} is the global thermal resistance including the temperature dependence of the thermal conductivity $\kappa(T)$ according to

$$\kappa(T) = \kappa(T_0) \cdot \left(\frac{T}{T_0}\right)^{-b}. \quad (5.98)$$

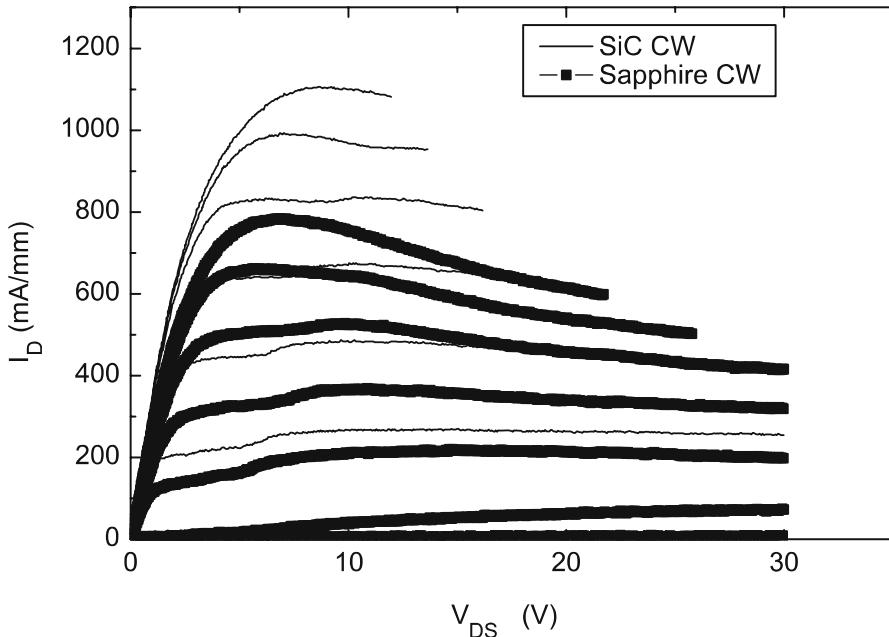


Fig. 5.39. CW-output characteristics to reveal the different thermal effects in SiC and sapphire, $V_{GS} = -5$ to 1 V, step 1 V

The thermal conductivity for s.i. SiC at room temperature amounts to $3.3 \text{ W} (\text{cm K})^{-1}$. The temperature coefficient $b = -1.5$ is used. The particular R_{th} must include the mounting situation in the application, which may strongly differ from the (on-wafer) thermal situation, from which the model is extracted. Another global temperature concept is applied in [5.6]. It reads

$$T(T_0) = \frac{T_0}{\left[1 - \frac{\Theta(T_0) \cdot P_{diss}}{4T_0}\right]^4}. \quad (5.99)$$

In this case, P_{diss} is the dissipated DC-power and $\Theta(T_0)$ is the temperature-dependent thermal resistance.

Extraction of the Thermal Resistance

A typical comparison of the different substrate properties for an AlGaN/GaN HEMT with a gate width $W_g = 1 \text{ mm}$ is given in Fig. 5.39. With otherwise nominally constant epitaxial and technological parameters, the strong difference in the drain current and derived DC- g_{ds} values due to thermal effects can be observed. The thickness of the substrates is $250 \mu\text{m}$ for sapphire and $370 \mu\text{m}$ for the s.i. SiC substrate at a constant backside temperature stabilized

by a thermal chuck. The thermal impedance itself can be extracted from different methods:

- From the DC-characteristics [5.133]
- From pulsed-output characteristics [5.72, 5.88]
- From pulsed-RF-current characteristics
- From photocurrent measurements of the optical absorption spectra [5.146]
- From verified scaling rules [5.72]

The interaction and construction of thermal models from single gate fingers to complete power cells is given in [5.72]. Even an electrothermal model for complete output stages can be constructed. Further, the methodology allows the construction of a large-signal model from verified scaling rules for the parasitics. A large-periphery device is modeled from the thermal behavior of individual FET fingers, including their interaction. This construction is a very desirable procedure, as high power devices are not always accessible to direct modeling due the need to control high currents and high power levels [5.44]. The inclusion of multilayer and multifinger thermal effects into large-signal modeling of large-periphery GaAs FETs is described in [5.20]. A consistent method is used to derive the large-periphery behavior of the devices. The model incorporates one of the critical features often neglected in the LS-modeling procedure: the actual thermal mounting situation in the application. This includes the thermal-resistance and -capacitance after wafer thinning and after the actual mounting in modules. The impact of additional thermal viaholes and of nonuniform 3D-distributions are investigated in [5.19].

Dynamic Thermal Effects

The thermal behavior is a highly dynamic process, as described, e.g., in [5.95]. The timing and the transient behavior of static thermal effects in FETs is investigated in [5.132]. The work supplies a methodology for finding isothermal measuring conditions for GaAs devices using a limited amount of pulsed-DC- and pulsed-RF-measurements at pulse-widths between $2\mu\text{s}$ and 10 ms for GaAs devices. Such near isothermal conditions can be used to investigate the substrate temperature dependence independently from the self-heating effects. Apart from the thermal resistance, in a first approach a thermal capacitance can be extracted to describe the dynamic thermal behavior with a thermal time-constant [5.95]:

$$\tau_{\text{thermal}} = R_{\text{th}} \cdot C_{\text{th}}. \quad (5.100)$$

A thermal relaxation time of $4.2 \times 10^{-5}\text{ s}$ is extracted for the Curtice approach in [5.95]. More thorough transient analysis is performed in [5.93, 5.209]. A very small relaxation time of 190 ns is extracted by electrical transmission-line pulser measurements for a thermal resistance $R_{\text{th}} = 70\text{ K W}^{-1}$. The simulated transient analysis in [5.209] for pulse width of $2\text{--}5\mu\text{s}$ at 33% duty cycle shows that the maximum temperature is not reached within the pulse duration and is further strongly related to the substrate material. Thus, a very careful analysis

is required for pulsed-operation with duty cycles between 10–100%. A more general procedure for the extraction of bias-dependent self-heating parameters is given in [5.2]. The procedure is based only on temperature-dependent electrical measurements. Both the thermal resistances and the thermal capacitances are extracted, which allows to describe the dynamic thermal behavior.

Behavioral Modeling Approaches

Behavioral modeling has recently been addressed for the modeling of RF-devices in order to enable a description of RF-devices for complex signal forms with nonconstant envelopes [5.1, 5.90]. For this very different modeling approach, a broad theoretical modeling base is available, e.g., in [5.187]. Direct extraction of the nonlinear HEMT model from vectorial LS-measurements is provided, e.g., in [5.163, 5.165]. The RF-IV characteristics of the device can be constructed purely from large-signal data. The general approach can be formulated as

$$I_1(t) = f_1(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \ddot{V}_2(t), \dots, \dot{I}_1(t), \dot{I}_2(t), \dots), \quad (5.101)$$

$$I_2(t) = f_2(V_1(t), V_2(t), \dot{V}_1(t), \dot{V}_2(t), \ddot{V}_1(t), \ddot{V}_2(t), \dots, \dot{I}_1(t), \dot{I}_2(t), \dots). \quad (5.102)$$

The procedure has been used by a number of groups for the model extraction for AlGaN/GaN HEMTs. An artificial-neural-network (ANN) model is constructed from near-optimum-load large-signal measurements, as described in [5.164]. An X-band amplifier is constructed from an ANN model of a 1 mm device between 1–26 GHz. With this very general approach, measurement data from a four-channel vector large-signal measurement setup including the phase information of the signals is used for the modeling [5.163]. The specific adaptation for GaN HEMTs includes the consideration of self-heating as an additional state variable apart from the six variables considered for a classical HEMT model.

5.5 Linearity Analysis and Modeling

One of the principal advantages of nitride devices is improved linearity compared to other device technologies at the same output power levels, e.g., [5.203]. Correspondingly, similar linearity levels for very much higher output power levels can be achieved [5.117]. The nature of these improvements can be attributed to the larger bandgap and thus increased operation voltages and output power capabilities [5.204]. A more detailed analysis, such as whether and to what extent GaN is really a more linear material, is not fully complete, e.g., [5.69, 5.71]. The full linearity is not yet exploited, especially due to the state of the technology with respect to dispersion. Charge trapping is known to be linked to electrical memory effects. Both the intermodulation levels and the side asymmetries of two-tone measurements are modified by

charge trapping, as shown by Volterra-series analysis, e.g., in [5.27]. Class-AB operation is found to be very favorable for AlGaN/GaN HFETs with respect to gain, PAE, and linearity in [5.203]. Recent advances will be analyzed in the following section.

5.5.1 Basic Understanding

The inclusion of nonlinear effects into large-signal modeling is of fundamental importance. The inclusion of intermodulation distortion into large-signal modeling for GaAs and GaN devices has been investigated for some time, e.g., in [5.56, 5.69, 5.77, 5.143]. Typical verification procedures of the LS-models include a comparison of the LS-model with multitone intermodulation measurements, e.g., as performed in [5.77, 5.143]. ACPR LS-simulations and verification have only recently been performed, e.g., [5.23, 5.30, 5.152].

Modeling

Some of the conventional current modeling approaches, such as the Curtice model, are not fully suitable for linearity analysis and simulation. The inclusion of higher derivatives of the current and charge equations into the modeling, extraction, and verification is of fundamental importance for the LS-simulation and quantitative prediction of nonlinear effects. Thus, current modeling using polynomial current approaches, e.g., in [5.43, 5.45, 5.170], leads to trivial or even vanishing higher derivatives. Therefore, models with sufficient degrees of freedom are required for the efficient inclusion of nonlinear effects [5.30]. A broad number of publications is available for the modeling and understanding of the actual behavior of the intermodulation spectra, e.g., [5.90], and of the adjacent channel power ratio (ACPR) curve forms [5.49]. The basic nulling conditions of the intermodulation in GaAs MESFETs are discussed in [5.136], as already detailed earlier. The additional contribution of self-heating to intermodulation in GaAs FETs is described in [5.135] and reads

$$I_D = I_{D,0}(T_L) \cdot (1 - \delta \cdot P_{\text{diss}}(t) \cdot h(t)). \quad (5.103)$$

$h(t)$ denotes the thermal impulse response function in the time-domain, when the current is sent through a low-pass filter. $I_{D,0}$ is the isothermal current. $h(t)$ is typically modeled with either a single-time-constant or few-time-constants response, e.g., [5.135]. An analysis of the relation of charge trapping and intermodulation in HEMT is further performed in [5.26]. A Volterra-series modeling approach is used for the drain current according to a Taylor-series expansion

$$\begin{aligned} I_D = & G_m \cdot v_g + G_d \cdot v_d + G_{m,2} \cdot v_g^2 + G_{m,d} \cdot v_g \cdot v_d + G_{d,2} \cdot v_d^2 \\ & + G_{m,3} \cdot v_g^3 + G_{m,2,d} \cdot v_g^2 \cdot v_d + G_{m,d,2} \cdot v_g \cdot v_d^2 + G_{d,3} \cdot v_d^3. \end{aligned} \quad (5.104)$$

This analysis yields the nonlinear transfer functions, as described, e.g., for GaAs FETs in [5.134].

Understanding of Intermodulation

More advanced understanding of the relevant factors of influence for analysis beyond RF-S-parameter and harmonic measurements has been achieved. The principal sources of nonlinearity in AlGaN/GaN devices are similar to those in any other FETs [5.137]. The analysis of the sources of nonlinearity yields the following:

- Quasi-static stationary analysis, e.g., [5.10, 5.43, 5.111], including
 - Nonlinear current sources [5.136]
 - Nonlinear charge sources [5.154]
 - Diode analysis [5.156]
- Thermal effects [5.71, 5.95, 5.135], including thermal memory [5.21]
- The impact of dispersion and trapping on the linearity measures [5.27]
- The impact of the baseband impedance and matching networks [5.25, 5.29, 5.49]

Following this list, the principal effects can be separated. The nonlinear current source g_m is a natural source of nonlinear behavior, as the derivatives of the transconductance are typically nontrivial, compare (5.104). The same is true for the higher derivatives of the main capacitances C_{gs} and C_{gd} , which similarly are nontrivial. The principal impact of thermal effects on the linearity is due to the pulse response in (5.100), see [5.135]. The isolated frequency of the heating is a few kilohertz, which has an impact on the variation of intermodulation with frequency and thus memory effects. A typical time constant or frequency for the thermal dissipation is in the 1–10 kHz region; however, a second contribution is visible at higher frequencies up to the gigahertz regime, e.g. [5.209], which can be significant too. Thermal memory [5.21] is especially significant for signals with high peak-to-average ratio (PAR), as detailed further.

The temperature-dependent nonlinearities in GaN/AlGaN HEMTs are analyzed in [5.71] based on a physical device model. The model is calibrated to measurement data and predict the dependence of IM_3 on both temperature between 200 and 500 K and physical device parameters such as gate length. The relative change of f_{\max} with temperature is found to be stronger for devices with $l_g = 100$ nm in comparison to devices with $l_g = 500$ nm. At the same time it is predicted that the GaN HFETs with shorter gates yield lower IM_3 and higher OIP₃ for a given gate width.

The bias dependence of the nonlinearities is of fundamental importance. A sweet-spot analysis can be performed, e.g., in [5.48], based on a Volterra-series modeling approach. This modeling approach allows a quantitative prediction of the sweet spots as a function of fundamental power. The model is further extended to random signals using a special harmonic balance machine. The intercept point behavior of GaAs FETs at Ka-band frequencies is analyzed in [5.119]. The impact of the gate biasing on the linearity is investigated, which is a typical procedure at all frequencies. The importance of the baseband

and higher-harmonics impedance with respect to intermodulation is further stressed in [5.25, 5.28]. The citations stress the impact of the parasitic bias networks and the resulting baseband impedance on the intermodulation and the resulting asymmetry of the intermodulation products. The variation of the distortion is as high as 4 dB with the baseband impedance. Further effects, such as the asymmetry of the intermodulation products, are more thoroughly investigated in [5.49]. The necessary condition for the asymmetry of the IMD generation is a significant reactive part of the baseband load impedance. However, these baseband and second harmonic effects must not be overridden by the real part of the IMD components. The memory-related contributions of intermodulation asymmetries will be discussed in the next section.

Memory Effects

Memory effects strongly influence the performance of transistors and power amplifiers in linear operation [5.178]. Their occurrence limits the system performance, as memory effects can only partially be compensated by typical linearization strategies [5.21] and thus effectively reduce the efficiency. This fact is very important for the application of GaN HFETs in base station applications, as systematic investigations have shown that GaN HFETs are better behaved with respect to thermal memory, as compared to all available semiconductor technologies, such as LDMOS and GaAs [5.21, 5.58, 5.178]. This includes the memory-related asymmetries of the intermodulation spectra, e.g., [5.90]. Memory effects can be separated into electrical [5.27] and thermal [5.21] relaxation effects within the semiconductor device. Electrical memory are caused by several nonlinear effects [5.49], e.g., by charge trapping, as discussed in [5.27]. The necessary condition for memory-like effects is a critical reactive load impedance in the baseband. Another factor that causes the electrical memory effect is the variation of terminal impedances over the input signal bandwidth around the carrier frequency, its harmonics, and the baseband frequencies [5.27], especially at high power levels, e.g., in a 90 W Si LDMOS device [5.21]. Thermal memory effects are caused by the gain variation through the temperature dependence of the electrical parameters are especially critical in statistical signals with high PAR and nonconstant envelope. Thermal memory, however, is especially critical as these variations can only partially be compensated [5.21]. Thermal compensators can be used in the predistortion to reduce the thermal memory by including a predictive function of the junction temperature. Another correction by a digital deterministic memory predistortion correction for LDMOS and GaN HEMTs is given in [5.52, 5.86]. The thermal compensation method proposed in [5.21] shows better compensation results than a purely memoryless compensation. Further, depending on the signal forms (e.g., EDGE vs. GSM vs. WCDMA signals vs. OFDM), and the amplifier concept [5.53, 5.57], the possibility to mitigate and correct the effects varies due to the nature of the signals [5.106]. Both baseband bandwidth and the number of carriers are of critical importance to the compensation, see [5.53]. The sensitivity of amplifiers to the

different types of memory effects thus varies. A great amount of modeling of memory effects on the circuit level is described. Behavioral models based on several approaches have been proposed. A parallel Wiener model is proposed and validated to quantitatively describe memory effects in silicon bipolar base-station- and in GaAs-HFETs-handheld-PAs for different power levels [5.89]. CDMA signals are used for the extraction and validation of the model. Memory effects show a strong negative impact on the improvement of a memoryless predistortion algorithm applied for the 45 W power amplifier. A polynomial model for the IMD and spectral regrowth asymmetries for a 170 W LDMOS device is proposed in [5.90]. Both analog [5.56] and digital [5.21, 5.90] compensation methods for memory have been proposed to minimize the effect of asymmetric IMD and thus of memory. However, the promise of GaN devices is a reduction of memory in such a manner that the critical thermal memory effect can be reduced in order to allow the application of standard predistortion techniques without performance losses for complicated signal forms. This will be discussed with respect to GaN FETs in the next section.

5.5.2 Nitride-Specific Linearity Analysis

A number of linearity investigations have been performed for III-N devices [5.178]. Linearity and gain characteristics of AlGaN/GaN HEMTs are described in [5.203]. The impact of the band structure at the AlGaN/GaN heterojunction is mentioned. The reduction of f_T for increasing gate voltages V_{GS} as a function of rising V_{DS} -voltage is attributed to the scattering of electrons in the AlGaN. Subsequently, the electrons scatter in k-space into higher valleys and effectively loose speed, which results in a reduction of f_T [5.144]. Requirements to the physical device structure for low intermodulation-distortion in GaN/Al_xGa_{1-x}N HEMTs are described in [5.104]. A case study is performed, which suggests an improvement in the distortion for high Al-content in the barrier and for devices with the inclusion of an AlN interlayer. Real-space transfer is reduced in this case, and the effective saturation velocity becomes independent of the gate voltage. Single-tone and two-tone time-domain large-signal characterization of GaN HFETs operated in class-A is given in [5.117]. The time-domain analysis yields nearly no phase shift for the fundamental and third harmonic output of the device well into compression for single-tone operation. This implies symmetric intermodulation products, which are experimentally confirmed by two-tone measurements. Fig. 5.40 gives the measured intermodulation product for a 1 mm device at 12 GHz at a two-tone measurement with 1 MHz tone-spacing at $V_{DS} = 20$ V. The measurement shows a nearly linear behavior in class-A/B for the IM_3 without sweet spot behavior. Reduced memory effects are a crucial advantage of GaN on s.i. SiC substrates due to improved thermal management of the actual semiconductor layer on top of a substrate with a very good thermal conductivity. Memory effects of GaN HFETs are analyzed in [5.58, 5.178]. The ACLR spectra of GaN HEMTs on s.i. SiC are found to show a reduced amount of memory relative

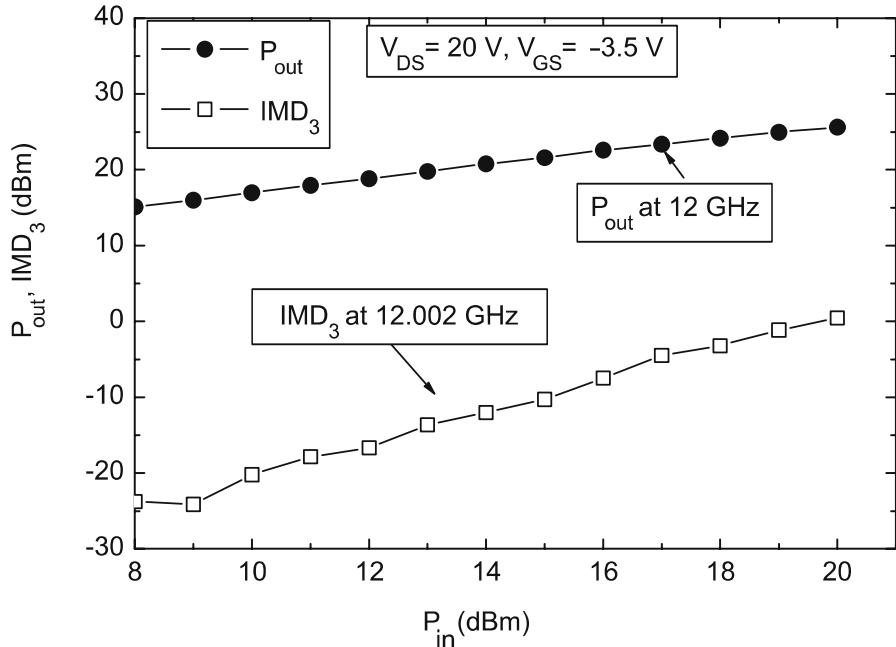


Fig. 5.40. Measurement of the output power P_{out} and intermodulation distortion IMD_3 under two-tone conditions at 12 GHz with a two-tone spacing of 1 MHz

to Si, GaAs, and other semiconductor technologies. As an example, Fig. 5.41 gives the output spectrum of a one-carrier WCDMA signal for a GaN HEMT amplifier on s.i. SiC with a gate periphery $W_g = 32$ mm. The peak output power is 47 dBm at 1.95 GHz in Fig. 5.41. ACLR levels of -39 dBc at 5 MHz and ≤ -55 dBc at 10 MHz offset are found. The shoulder behavior of the signal at 5 and 10 MHz under one-carrier WCDMA operation and the spectral regrowth behavior show very little indication of memory effects and spectral regrowth [5.58].

Linearity Modeling and Simulation of GaN HFETs

Device modeling is performed and applied mostly for simple signal forms, i.e., simple two-tone measurements, despite the complicated waveform applied in today's communication systems. The conventional Chalmers model is used to model an AlGaN/GaN HFET with a gate periphery of 2 mm in [5.30, 5.181]. It is found in [5.32] for GaN FETs that the original Chalmers model cannot correctly predict the higher derivatives of the transconductance. Instead, the approach of Fager [5.30, 5.56] is used to match the higher derivatives. The measured output power and the measured intermodulation distortion in class-A, class-AB, and class-B with double-sweet spots can be precisely matched.

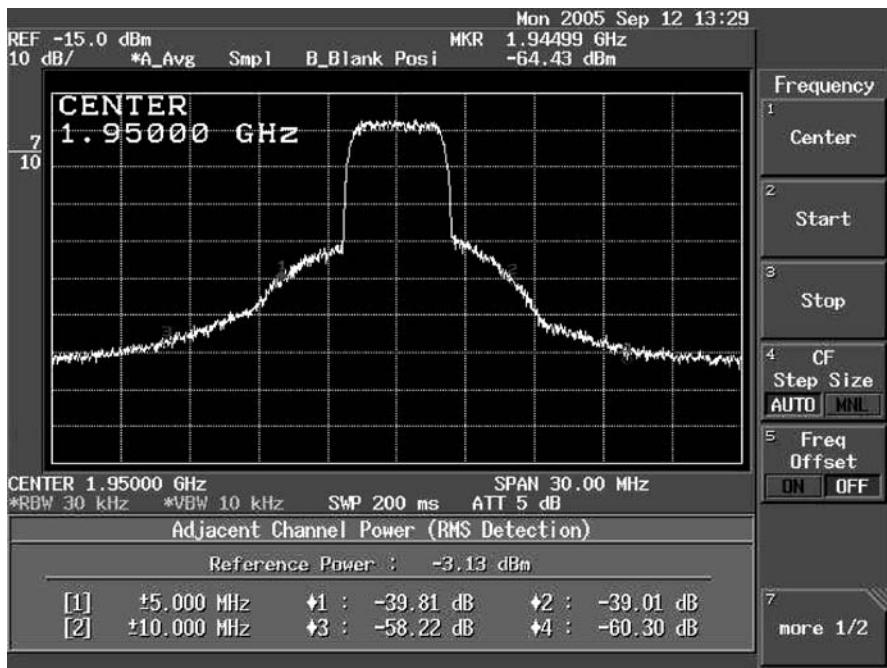


Fig. 5.41. One-carrier WCDMA spectrum at 1.95 GHz at a peak output power level of 47 dBm

The drain voltage dependence of the current is modeled according to

$$I_{DS} = \frac{\beta \cdot V_{GS,3}^2}{1 + \left(\frac{V_{GS,3}^{\text{plin}}}{V_L} \right)} \cdot (1 + \lambda V_{DS}) \tanh \left(\frac{\alpha \cdot V_{DS}}{V_{GS,3}^{\text{psat}}} \right), \quad (5.105)$$

where the $V_{GS,3}$ is an effective V_{GS} -voltage modified according to [5.56]. $\alpha, \beta, \lambda, V_L, V_{GS,3}^{\text{plin}}$, and $V_{GS,3}^{\text{psat}}$ are parameters. For more complicated wave forms, especially for nonconstant signal envelopes, few investigations exist based on large-signal modeling of GaN FET [5.32, 5.48]. A detailed analysis is complicated, as the analysis in the frequency-domain only is not suitable, due to the nonconstant envelopes. Harmonic-balance simulations with an AM-modulated signal and a Gaussian-noise baseband modulation are provided in [5.48]. Examples of the more complicated signals are given in [5.32] combining harmonic balance and the artificial frequency mapping technique. OFDM signals can be simulated efficiently, as they use equally separated carriers.

GaN HFETs with Predistortion Correction

With the increasing interest in GaN devices, several GaN device technologies have been further subject to the LDMOS type of (software) predistortion lin-

earization strategies with parameters matched to GaN. An analog dynamic gate bias technique for improved linearity of GaN FETs is described in [5.40]. A significant improvement of the third-order intermodulation of 10 dB is described, once the gain of the transistor is adjusted in accordance with the instantaneous envelope of the input signal to minimize AM-AM distortion. A large-signal model based on the Curtice approach is used to investigate the nonlinearities. The procedure also serves to improve the ACPR in WCDMA signals by 8 dB. Further, standard WCDMA procedures have been applied for the analog and especially digital predistortion of GaN FETs, e.g., [5.84, 5.125]. GaN HEMTs on s.i. SiC substrates by Eudyna have been evaluated by four-carrier WCDMA signals with 5 MHz signal spacing. A significant improvement of the ACPR of ≥ 10 dB is achieved by the application of a digital predistortion [5.84]. A similar digital predistortion strategy has been applied in [5.125]. One-carrier WCDMA signals have been applied to a dual-stage amplifier with a gate periphery of 32 mm. The ACLR criterion is met for an average output power of 35 dBm between 1.8 and 2.7 GHz with the application of the DPD. Once the DPD is applied, the average output power can be increased to 40 dBm between 1.8 and 2.7 GHz meeting the 3GPP ACLR specifications. Error vector magnitude (EVM) and peak code domain error (PCDE) are also met after predistortion. Further examples are given in Chapter 6.

5.6 Noise Analysis

The section addresses the analysis and modeling of both low-frequency and RF-noise in III-N devices. The analysis is so far limited to FETs.

5.6.1 Low-Frequency Noise

Low-frequency noise is of great interest to process analysis [5.191] and to those device functions that are limited by phase noise, such as oscillators. It defines the minimum signal that can be processed by the device [5.65]. A strong correlation can be found of low-frequency noise, material quality, and device reliability [5.191]. Origins of low-frequency noise in FETs are well discussed in the literature, e.g., in [5.65, 5.66]. The sources of noise in the frequency range between 1 Hz and 10 MHz include the following:

- Fluctuations of the channel conductance and mobility [5.65, 5.66]
- Fluctuations of the sheet carrier density [5.65]
- Thermal activation of carriers from localized states in the bulk [5.173], at heterointerfaces [5.65], and at surfaces [5.194]
- Grain boundary motion [5.65]

As an example, Fig. 5.42 gives a low-noise spectrum of a GaN/AlGaN HEMT on s.i. SiC substrate with a gate width $W_g = 2 \times 30 \mu\text{m}$ and a gate length $l_g = 150 \text{ nm}$ for various operation bias V_{DS} .

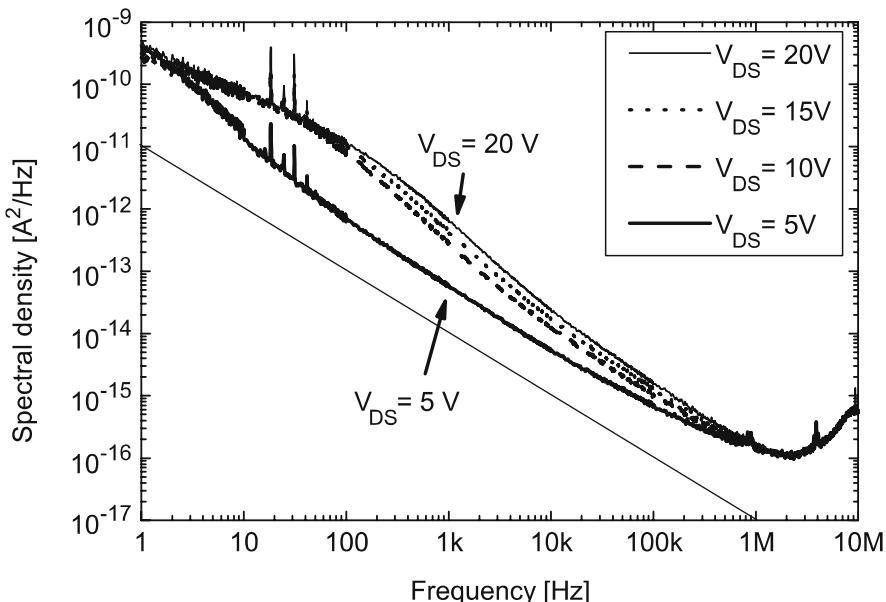


Fig. 5.42. Low-frequency noise spectrum of a GaN HFET between 1 Hz and 10 MHz as a function of drain voltage V_{DS} at a drain current $I_D = 100 \text{ mA mm}^{-1}$

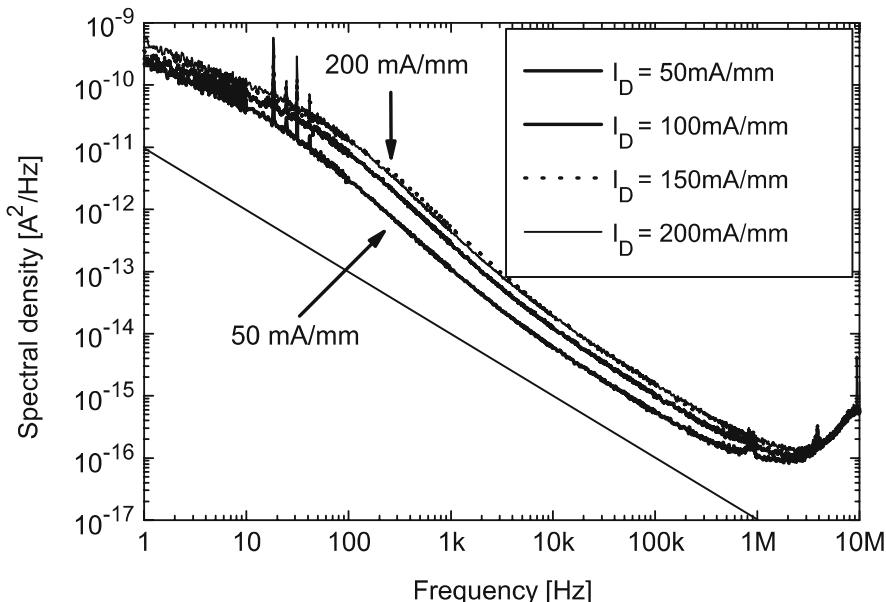


Fig. 5.43. Low-frequency noise spectrum of a GaN HFET between 1 Hz and 10 MHz as a function of drain current at $V_{DS} = 10 \text{ V}$

The lowest $1/f$ -noise level is found for the lowest V_{DS} voltage of 5 V. Fig. 5.43 gives the same spectrum as a function of drain current at a drain voltage $V_{DS} = 10$ V. An increase of the $1/f$ -noise-floor is found with rising drain current I_{DS} . The spectrum between 1 Hz and 10 MHz is further characterized by a nonsteady behavior of the noise spectrum, which is affected by trapping, as also found for devices from other materials [5.65, 5.173]. The principal modeling for the low-frequency noise is typically [5.66]

$$\frac{S_\nu(f)}{I_{DS}^2} = \frac{\alpha_H}{N \cdot f}. \quad (5.106)$$

The Hooge-parameter α_H is dimensionless, f is the frequency, and N is the total number of carriers in the devices. Typical values of the Hooge-parameter amount to 10^{-4} , which change if the crystal is damaged [5.66]. In MOSFETs, the low-noise spectrum at low drain bias can be modeled according to

$$S_\nu(f) = \frac{e \cdot \mu \cdot \alpha_H}{L^2} \cdot \frac{I_{DS} \cdot V_{DS}}{f}. \quad (5.107)$$

Thus, the spectral noise density is proportional to both the source-drain current I_{DS} and the drain-source voltage V_{DS} . Deviations from the ideal frequency behavior of the current-noise spectral density are modeled according to

$$S_\nu(f) \sim \frac{1}{f^\gamma}. \quad (5.108)$$

A γ -value of 1.2 is found for the modeling of AlGaN/GaN HFETs on sapphire substrates in [5.91], extracted between 1 Hz and 100 kHz. Higher frequency measurements may be useful to separate the impact of fast traps, as can be seen in Fig. 5.42. The factors of influence on the $1/f$ -noise are now discussed in detail. Low-frequency noise of doped-channel AlGaN/GaN HFETs on sapphire substrates is discussed in [5.91]. The noise-behavior observed gives $\gamma = 1$. The Hooge parameter is of the order of 10^{-2} and it is proportional to the channel width in this particular case. The noise is correlated with the high density of defects at the AlGaN/GaN interface, which leads to fluctuations of the channel charge.

A characterization of AlGaN/GaN MODFETs on sapphire substrates at low-drain bias of ≤ 1 V is given in [5.65]. Deviations from the purely $1/f$ -behavior are reported in [5.65] as in various other publications. The lattice-temperature dependence of the low-frequency noise of MBE-grown samples shows a variation of the parameter γ between 0.85 and 1 for a temperature range between 130 K and RT. A linear scaling of the Hooge parameter with channel width indicates an interface-related effect [5.91, 5.139], possibly, since the AlGaN/GaN interface is the only interface in direct contact with the 2DEG. However, other explanations are also possible, such as a poor contact technology at the ohmic or Schottky contacts [5.139]. The dependence of the low-frequency noise on the silicon doping in the AlGaN barrier

layer of the AlGaN/GaN HFET is analyzed in [5.173]. The findings include increased noise floor for the structure with barrier doping relative to the undoped structure and a deviation from the purely $1/f$ -behavior especially for the doped structure. The increased low-frequency noise is attributed to the increased carrier trapping/detrapping with the impurity doping in the barrier. Effects of the surface passivation and barrier-layer defects on the low-frequency noise-spectral-density are described in [5.194]. The spectra between 1 Hz and 100 kHz are measured before and after passivation. The passivated device yields lower spectral low-noise density [5.194, 5.196]. The distinction between the gated and ungated region is made, as mentioned in [5.139]. The V_{GS} -dependence is used to distinguish the noise contributions of the series resistance and of the gated region with different noise exponents. The correlation of leakage current and low-noise density is used to explain the difference between passivated and unpassivated devices, as the number of carriers is increased due to the passivation. The substrate- and gate-current-dependence of the low-frequency noise is further investigated in [5.46]. The devices on sapphire and silicon substrate provide a low-noise spectral density similar to that of GaAs devices, while the AlGaN/GaN HEMTs on s.i. SiC substrate provide an increased $1/f$ -noise level. However, for the devices on Si substrate, a correlation of the normalized leakage current and low-noise level is found, which indicates a processing issue rather than a substrate issue. Similar findings on the good correlation of the $1/f$ -noise and the transients of DC-gate and DC-drain currents after illumination with light with $\lambda = 365$ nm in AlGaN/GaN HFETs are reported in [5.82]. The drain-current and gate-current noise are distinguished by measurements. Both contributions to the $1/f$ -noise show a correlation with the transients of the DC-gate and drain currents. The correlation is not perfect, however; this suggests that the $1/f$ -noise has the same physical origins as the dispersion.

5.6.2 RF-Noise Analysis and Characterization

III-N FETs are further attractive for RF-noise applications due to the combination of high-speed and high breakdown-voltage properties. In addition the high barrier discontinuity at the AlGaN/GaN interface suppresses potential noise sources. Fig. 5.44 gives the noise sources for the RF-noise in an AlGaN/GaN HFET. These sources of RF-noise include

- Ohmic (parasitic) resistances at source and drain
- Channel noise through velocity fluctuations [5.33]
- Interface contributions
- Surface contributions, such as leakage [5.147] and traps

This low-noise behavior is further analyzed in this subsection. Several investigations are available in the literature, e.g., [5.99, 5.100, 5.109]. A typical noise-equivalent circuit is depicted in Fig. 5.45. A standard small-signal equivalent circuit is used with two additional noise sources. In the standard small-signal

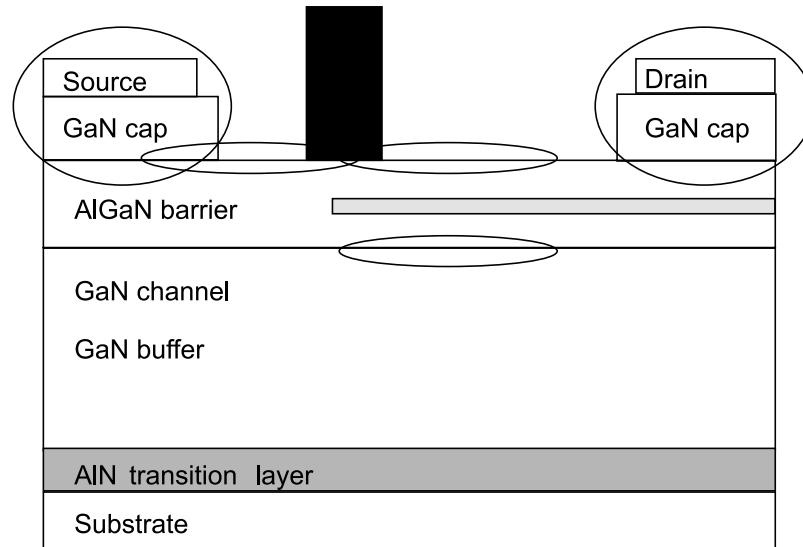


Fig. 5.44. RF-noise sources in AlGaN/GaN HEMTs

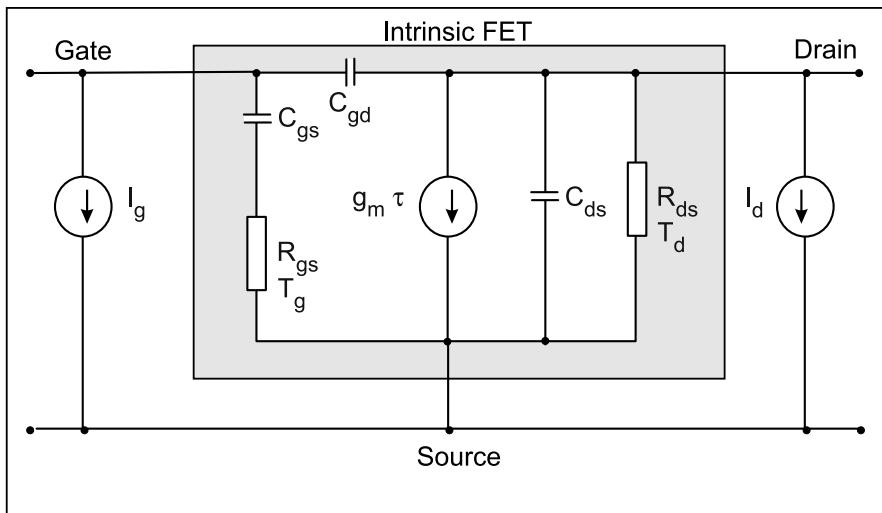


Fig. 5.45. RF-noise equivalent circuit of an FET

equivalent circuit, noise can be described by two noise-equivalent temperatures T_{Gate} and T_{Drain} . Several modifications of Fig. 5.45 are available for the intrinsic modeling of leaky HFETs, e.g., for InAlAs/InGaAs HFETs in [5.148,5.159]. The strong impact of the leakage on the noise in GaN HFETs is described in [5.159]. Additional considerations are necessary for the inclusion of impact ionization and other inductive effects [5.147]. The optimization of III-N FETs

as in any other FET can be based on the Fukui-equation [5.60]:

$$N_{F,\min} = 10 \log \left(1 + \frac{k_f \cdot f}{f_T} \left[g_{mi}(R_G + R_S) \right]^{0.5} \right). \quad (5.109)$$

The requirements for low-noise operation are visible: high gain, high cut-off frequency, and low parasitic resistances are necessary to reduce the noise figures. The Fukui-factor k_f can be approximated by [5.109]

$$k_f = 2 \cdot \left[\frac{I_{opt}}{E_C \cdot l_g \cdot g_{mi}} \right]. \quad (5.110)$$

I_{opt} is the drain current level, which minimizes the noise figure. The data used in [5.109] for GaN HFETs did not fit the approximation in (5.110). However, the principal dependence can be used. For a given gate length l_g , the intrinsic g_{mi} is lower and the access resistances are higher than that for other semiconductors, whereas the critical field E_{crit} is significantly higher. A more detailed analysis is thus required. The dependence of RF-noise parameters on the Al-content in AlGaN/GaN HFETs is analyzed in [5.109, 5.160]. A comparison of the minimum noise figure and associated gain is given for different Al-contents in the barrier layer. The best RF-low-noise operation in [5.109] is found for the highest Al-content, as the gain and cut-off parameters are best for highest Al-content, while the parasitic elements are nearly independent of the Al-content. The results in [5.160] disagree with this finding, as the four noise parameters are fully independent of the Al-content. It is found that the quality of the channel material is decisive. Intrinsic noise-equivalent-sources and circuit-parameters for AlGaN/GaN HEMTs on s.i. SiC substrate are extracted in [5.98–5.100]. Three independent noise mechanisms are identified: velocity fluctuations, gate leakage [5.159], and traps, as given in Fig. 5.44. Fig. 5.45 gives the typical de-embedded noise-equivalent-circuit model for an HFET device. The noise theory of GaN HFETs is very similar to the modeling of RF-noise in GaAs, e.g., [5.140, 5.171], or InP (H)FETs, e.g., [5.3]. The differences for the modeling of GaN devices include the following:

- Modified access resistances [5.131]
- Better overdrive capabilities, i.e., robustness and linearity [5.35, 5.124]

Some examples are now given.

RF-Noise-Measurements and Modeling

RF-noise measurements are performed in a noise parameter measurement setup, e.g., based on a noise figure meter [5.160]. The measurements are performed in an input tuner systems typically extracting the full four noise parameters. Fig. 5.46 gives the measured noise figure N_F as a function frequency for a $W_g = 2 \times 60 \mu\text{m}$ AlGaN/GaN HEMT on SiC with $l_g = 150 \text{ nm}$.

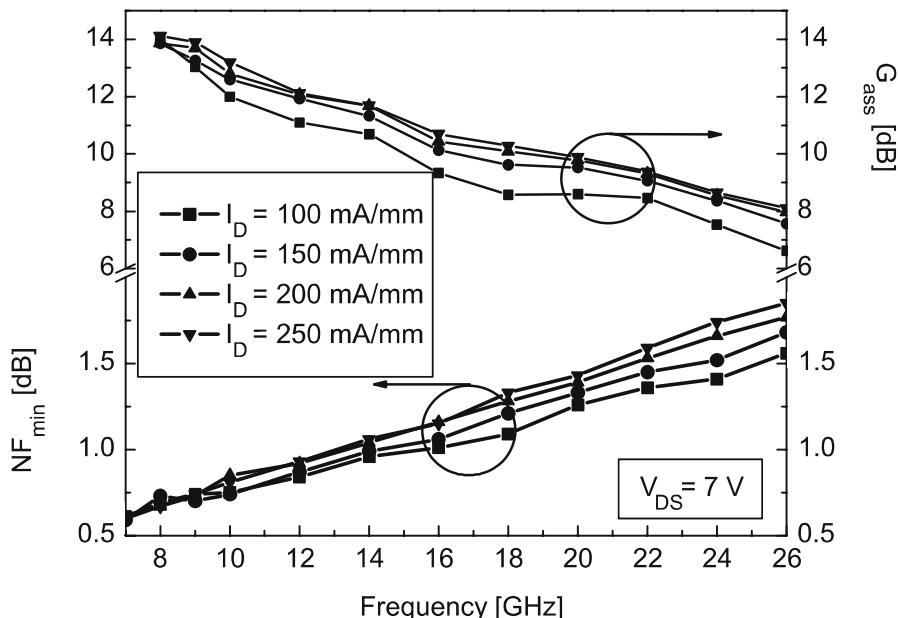


Fig. 5.46. Minimum noise figure $N_{F,\min}$ and associated gain G_{ass} as a function of frequency for an AlGaN/GaN HEMT on s.i. SiC with $l_g = 150 \text{ nm}$

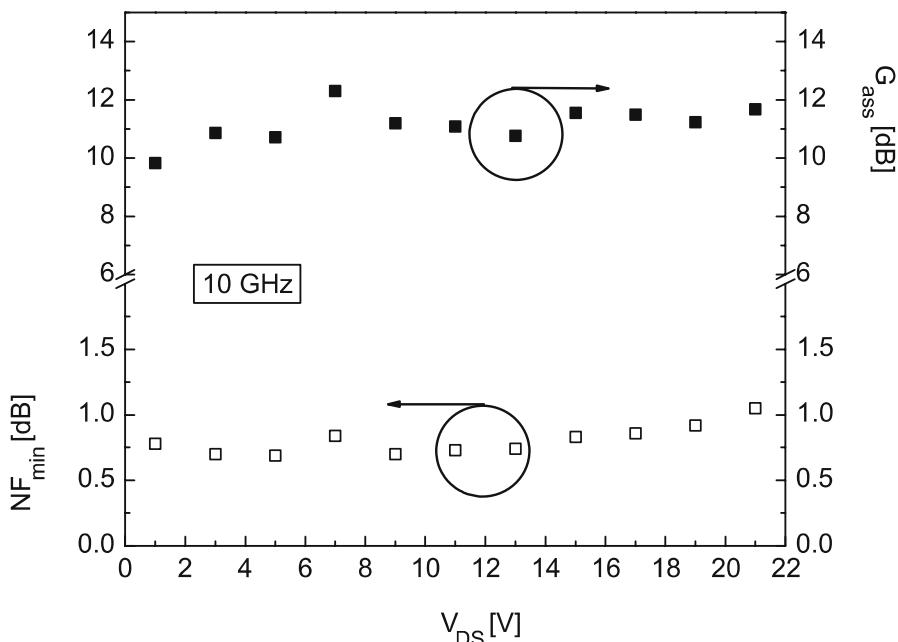


Fig. 5.47. Minimum noise figure $N_{F,\min}$ and associated gain G_{ass} at 10 GHz vs. V_{DS} and I_D for an AlGaN/GaN HEMT with $l_g = 150 \text{ nm}$

A minimum noise figure of 0.7 dB at 10 GHz for a drain current of 12 and 18 mA or 100 and 150 mA mm⁻¹, respectively, is observed. Fig. 5.47 gives the same minimum noise figure $N_{F,\min}$ and the associated gain G_{ass} at 10 GHz as a function of V_{DS} bias and current level of 150 mA mm⁻¹. A very constant behavior of the noise figure $N_{F,\min}$ and associated gain G_{ass} as a function of V_{DS} is observed for a gate length $l_g = 150$ nm. The Pospieszalski model can be extracted from the measurements in Fig. 5.46. The model reads for the gate and drain noise-sources [5.140, 5.172]:

$$I_{\text{DS}} = 4k_{\text{B}} \cdot \frac{\Delta f \cdot T_{\text{Drain}}}{R_{\text{ds}}}, \quad (5.111)$$

$$I_{\text{G}} = 4k_{\text{B}} \cdot \frac{\Delta f \cdot T_{\text{Gate}}}{R_{\text{i}}}. \quad (5.112)$$

A maximum drain temperature $T_{\text{Drain}} = 1,350$ K and a gate temperature $T_{\text{Gate}} = 300$ K are extracted at $V_{\text{DS}} = 7$ V and at drain current $I_{\text{DS}} = 150$ mA mm⁻¹. This result justifies the assumption of independent noise sources. The temperature $T_{\text{Drain}} = 1,350$ K is lower than the values found for a gate length of 700 nm in [5.160]. The extracted gate temperature T_{Gate} in [5.160] is in the same order as the room temperature. The Pucel or PRC model assumes for the noise sources [5.171, 5.172]

$$I_{\text{D}} = \langle i_d i_d^* \rangle = 4k_{\text{B}} \cdot \Delta f \cdot T_{\text{L}} \cdot g_{\text{m}} \cdot P, \quad (5.113)$$

$$I_{\text{G}} = \langle i_g i_g^* \rangle = 4k_{\text{B}} \cdot \Delta f \cdot T_{\text{L}} \cdot \frac{(\omega C_{\text{gs}})^2}{g_{\text{m}}} \cdot R. \quad (5.114)$$

The noise sources are modeled to be correlated $\langle i_d i_g^* \rangle$ with the correlation parameter C. An extraction of the Pucel model for GaN HEMTs is provided in [5.160] in comparison to a Pospieszalski extraction. In general, the insertion of an AlN interlayer into the epitaxial structure improves the noise performance.

Input Linearity of III-N FETs

III-N FETs are attractive for applications that require a high degree of survivability under strong RF-illumination, e.g., [5.124]. A linearity analysis of low-noise AlGaN/GaN HEMTs on s.i. SiC substrate is given in [5.124]. The optimum biasing for the noise figure found is 15–20% of I_{Dmax} for a V_{DS} of 1–10 V. The ratio of the input distortion II_3 vs. carrier power is investigated. Apart from the promising minimum noise figure of 1 dB at 10 GHz, the linearity at high input power levels is particularly advantageous compared to GaAs HEMTs. Further results are given in Chapter 6.

5.7 Problems

1. Mention the specific differences of GaN FETs with respect to modeling relative to GaAs FETs.
2. What is the main difference between thermal and trap-related dispersive behavior?
3. What is particular to AlGaN/GaN HBT modeling relative to GaAs HBTs?
4. Describe the expected theoretical behavior of the IM_3 -sweet-spots in a two-tone measurement of a GaN HFET!
5. Describe the differences of the WCDMA spectra of a GaN HFET relative to a spectrum of a silicon LDMOS!
6. What are the expected differences of GaN FETs as compared to state-of-the-art GaAs PHEMTs and InP HEMTs?

Circuit Considerations and III-N Examples

This chapter discusses circuit examples for III-N-based amplifiers with a focus on increased impedance, thermal management, and high RF-power management in the frequency range between a few MHz and at least 60 GHz. Low-noise amplifiers are presented and analyzed for high dynamic range, robustness, and high linearity. The last section treats highly linear power amplifiers for microwave and millimeter wave frequencies. Again, nitride-specific advantages and challenges, such as output power, linearity, and power-added efficiency (PAE), are investigated. The potential of III-N materials and devices are far from exploited in hybrid, MIC, and MMIC circuits. This chapter provides an overview of critical issues and circuit examples for nitride-based devices. As is pointed out in Sect. 2.5.7, there are relatively few reports on GaN-HEMT-based fully integrated MMICs in microstrip- or coplanar-waveguide passive technology so far, due to the tough requirements for a high-voltage passive technology.

6.1 Passive Circuit Modeling

Transmission-lines and transmission-line parameters are a critical issue for any integrated circuit device technology. Various transmission-line variants exist, e.g., coplanar-waveguide [6.145], grounded coplanar-waveguide [6.201], and microstrip transmission-lines [6.101].

6.1.1 Coplanar-Waveguide Transmission-Line Elements

Coplanar-waveguide transmission-lines or waveguides (CPW) are attractive, as they can be realized without the application of a backside process, since the ground component is guided on the frontside of the chip. A typical CPW line is given in Fig. 6.1. The position of the ground at the frontside is useful in terms of manufacturability; however, CPW is in general not as area-efficient as the microstrip line approach [6.6]. Further, CPW technology also requires

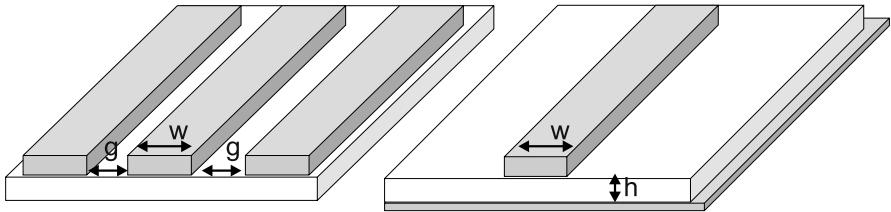


Fig. 6.1. Comparison of a coplanar-waveguide (*left*) and a microstrip (*right*) transmission-line

thinning of the wafer for thermal reasons or for mm-wave technology to suppress other propagation modes in the substrate, e.g., [6.138]. In general, the passive components in the III-N world are not very different from GaAs passive components, e.g., [6.169]. Microstrip-transmission-line models based on very few parameters are implemented in standard commercial simulators such as Agilent-ADS. III-N coplanar-waveguide models are similar to III-V passive models, however, require specific extraction. As native GaN substrates have not been used with hybrids and MMICs so far, hybrid integration of passive coplanar-waveguide components on AlN substrates for III-N devices is given in [6.66]. As AlN is a good insulator and easily available, transmission-lines, discontinuities, metal–insulator–metal (MIM) capacitors, and resistors are modeled for the realization of cost-effective hybrid AlN-substrates. Several MMIC processes are available on s.i. SiC substrate, partly also based on SiC MESFET MMICs [6.159]. Measured attenuation of coplanar-waveguides on 6H-, p-Type SiC, and high-purity semiinsulating 4H-SiC through 800 K is compared in [6.128]. The measured attenuation at RT for HPSI SiC at 10 GHz is 1 dB cm^{-1} and increases to 4.5 dB cm^{-1} at 773 K. Differences are found for different substrates. Conductive p-type 6H-SiC yield increased attenuation of coplanar-waveguides of 20 dB cm^{-1} at 1 GHz, which makes this substrate unsuitable for microwave operation. Further differences are found for the temperature dependence of the attenuation of p-type 6H-SiC and 4H-high-purity SiC. Due to the high value at RT, the increase in attenuation with temperature is not as pronounced as for HPSI SiC. Similar considerations apply for other conductive substrates for III-N devices, such as conductive or high-resistivity silicon. High-resistivity (HR) silicon with a resistivity of $1.6 \text{ M}\Omega \text{ cm}$ with losses of 6.3 dB cm^{-1} at 20 GHz and RT can be fabricated, e.g., [6.190]. However, typical HR silicon has a lower resistivity of $10\text{--}30 \text{ k}\Omega \text{ cm}$ [6.38] and higher RF-losses unless other measures are taken to minimize those, e.g., additional oxides [6.147]. The impact of the substrate conductivity on silicon transmission-lines is reviewed in [6.127].

Passive Modeling

Fig. 6.1 gives a comparison of a transmission-line in a coplanar and a microstrip technology. The signal line width w and the signal-to-ground spacing g , and

Table 6.1. Extracted electrical parameters of various passive elements on AlN, Alumina, s.i. SiC, and GaAs substrates

Element	Substrate	w (μm)	g (μm)	C _{exp} (pF m ⁻¹)	ε _r ^{eff} (-)	Ref.
70 Ω CPW Line	AlN	45	75	99	—	[6.66]
50 Ω CPW Line	AlN	70	30	—	4.74	—
50 Ω CPW Line	Alumina	70	40	—	—	—
50 Ω CPW Line	GaN (250 μm)	70	30	—	5.20	—
50 Ω CPW Line	GaAs (625 μm)	70	45	—	6.93	—
50 Ω CPW Line	s.i. SiC (370 μm)	70	30	—	5.38	—
50 Ω CPW Line	s.i. SiC (370 μm)	25	13.3	—	5.40	—

the substrate thickness h are given. The modeling considerations are not different from other semiconductor devices. Modeling of coplanar-waveguide transmission-line on s.i. SiC is given in [6.141]. Models for a coplanar transmission-line library on GaN on s.i. SiC epitaxial layers are developed and are described, e.g., in [6.152]. The detailed modeling is derived from passive modeling on s.i. GaAs or other insulating dielectric substrates, e.g., [6.56, 6.122]. In the model for a simple coplanar transmission-line the characteristic impedance is modeled according to [6.66]:

$$Z_0 = ((R + i\omega \cdot L) / (G + i\omega \cdot C))^{0.5}, \quad (6.1)$$

$$\gamma = ((R + i\omega \cdot L) \cdot (G + i\omega \cdot C))^{0.5}. \quad (6.2)$$

R , L , G , and C denote the resistance, line inductance, conductance, and capacitance. Table 6.1 compiles parameters for transmission-line elements on AlN, Alumina, GaAs, and s.i. SiC substrates. w denotes the signal width and g the width of the signal-to-ground spacing. ϵ_r^{eff} denotes the calculated effective permittivity of a coplanar-waveguide. Table 6.1 shows the similarity of GaAs, AlN, and s.i. SiC. The typical modeling includes further structures, e.g., T-junctions, steps, cross-junctions, bends, and lumped elements, such as MIM capacitors of various types [6.159], and either NiCr- or other resistors, such as TaN- and TiN-resistors. The modeling is based on the well-known methodologies, e.g., [6.51].

6.1.2 Microstrip-Transmission-Line Elements

Microstrip-transmission-line GaN MMICs based on full passive libraries have been repeatedly reported, e.g., in [6.121, 6.171]. The transmission-line parameters of GaAs technologies [6.39, 6.51] can be adjusted as for any insulating dielectric substrate. All typical elements of a passive library can be described by conventional microstrip line models provided by commercial simulators. In addition to the modeling of the new substrate materials, conventional passive hybrid matching circuits are being used, especially for lower frequencies of

≤ 10 GHz, e.g., [6.195]. This is especially true, since the available generic substrates are either expensive (SiC), or (semi)-conductive (Si), or thermally critical (sapphire). The modeling of these hybrid substrates is not different from other conventional approaches, e.g., [6.101]. However, new circuit concepts, such as harmonic terminations, require improved passive modeling, which are discussed with the new circuit concepts.

6.2 High-Voltage High-Power Amplifiers

This section compiles the principle operation modes or classes for power amplifiers with emphasis on the classes suitable for high-voltage III-N devices as compared to other semiconductor technologies.

6.2.1 Basic Principles of High-Voltage High-Power Operation

The specific properties of III-N devices allow the application of more advanced circuit concepts. Good general overviews of the amplifier classes are given in [6.30, 6.34, 6.89, 6.135, 6.176].

Amplifier Classes

The amplifier classes in general differ in the mode of the quiescent DC-bias (class-A–class-C), the modulation of the DC-bias, the load fundamental and harmonic termination (class-D–class-G), the modulation of the load (Doherty), in phase/amplitude variation [6.62], and even the digital modulation of the input signal (class-S) [6.67]. Thus, the resulting waveforms differ significantly [6.30]. Fig. 6.2 illustrates the differences in bias and load conditions for some of the examples. The single classes are described for FETs in detail as follows:

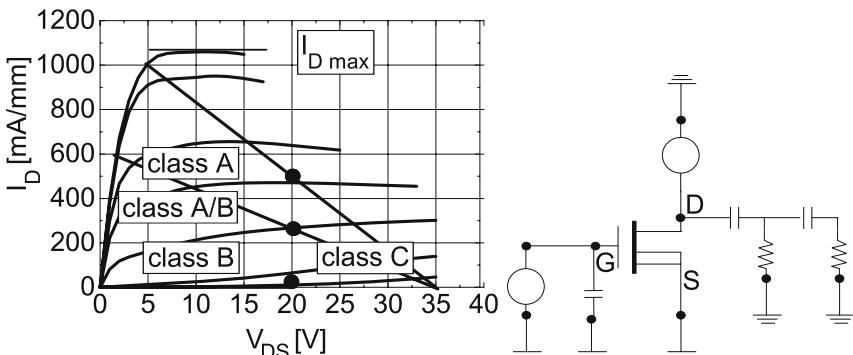


Fig. 6.2. Bias conditions and topology for different classes of operation: *left* (A–C), *right* (D–G)

- Class-A: The device is biased at a quiescent current of $I_{D\max}/2$. This operation allows for maximum gain compared to the other classes; however, the maximum theoretical PAE is 50%. The linearity is good, as the bias is chosen to avoid the nonlinearities of the diodes [6.104].
- Class-B: the device is statically biased at an operation V_{DS} with V_{GS} in a pinch-off condition with $V_{GS} = V_{thr}$. The maximum theoretical PAE amounts to 78.5% or $\pi/4\%$ [6.120, 6.191].
- Class-A/B: the biasing used lies between the aforementioned conditions A and B mostly to increase efficiency and reduce quiescent power dissipation in a trade-off between the linearity and dissipated power at the different input power levels [6.180].
- Class-C: the device is biased in extreme pinch-off with a quiescent $V_{GS} \leq V_{thr}$. The efficiency can be further increased at the expense of higher input power levels beyond 80% and reduced linearity. The theoretical efficiency limit for the class-C operation is 100%, while the associated output power of PAE = 100% is 0. This operation further requires increased breakdown voltages for the device, which favors III-N devices [6.30].
- Class-D: The Class-D-type amplifier is a switch-mode amplifier. It consists of a switch device, typically realized with two transistors. The amplifier achieves high output powers and high efficiencies up to 100% through the phase separation of RF-current and voltage. A filter is required at the output which limits the bandwidth. The amplifier is further only suitable for phase modulation. As for all switch-mode amplifiers a high f_T is required [6.30] as compared to the operation frequency to reduce losses in the switching.
- Class-E: This amplifier is again of switch-mode type, which favors transistors with high f_T . It consists of one transistor. The main characteristics of this amplifier class is an input driving similar to rectangular switching achieved [6.45, 6.46, 6.124]. This fact boost efficiency while the gain is reduced compared to a linear amplifier because of the need to over-drive. Again only phase modulation is possible. Harmonic termination is achieved through a relatively simple RCL circuit which taylors current and voltage swings. The output filters again limit the bandwidth while a high-breakdown voltage is required for the transistors [6.30]. Even when driven not fully into compression, Class-E amplifiers provide improvements in efficiency in more linear operation modes [6.95, 6.166].
- Class-F: In this operation mode, the output waveform is shaped using an output harmonic termination technique leading to a square-type output voltage waveform with a half sine wave current wave forms [6.30, 6.63, 6.89, 6.146]. The challenge of Class-F amplifiers in general is the need to match a maximum number of harmonics [6.134] while this number of harmonics is limited for practical reasons in a hybrid environment [6.146] and at the same time correlated with the maximum achievable efficiency [6.134]. Several subclasses exist depending on the use of the harmonics [6.63, 6.136]. The inverted Class-F amplifier gives a half sine wave output voltage and

Table 6.2. Characteristics of amplifier classes from A to S on a scale from – to ++ for amplitude (AM) and phase modulation (PM)

Class	Quiescent DC-current	PAE (%)	Bandwidth rel.	Linearity	Comment
A	$I_{D\max}/2$	50	++	++	
B	0	78.5	++	0	
A/B	$0 \leq I \leq I_{D\max}/2$	78.5	++	+	
C	0	100	–	–	$P_{out} = 0$ at 100%
D	A/B	100	– (filter)	–	Loss of amplitude
E	Switch	100	– (filter)	–	Loss of amplitude
F	–	100	– (filter)	–	
S	E,D	100		++	
Doherty	(A,B), F	78.5	– (load)	+	
Chireix	AB,D,E,F	100	–	++	Switch AM, PM
ET	A/B	100	0	+	
EER	D,E	100	–	++	

a square type of output current. For all Class-F type amplifiers the linearity is reduced through the generation of harmonics at the input which requires input termination compensation [6.146].

More amplifier classes have been explicitly defined:

- Analog Class-S: both the DC-supply and the load are modulated, resulting in a maximum theoretical efficiency of 100% [6.30, 6.124]
- Digital Class-S in sigma-delta mode [6.64, 6.67]

Further amplifier types have been reported, such as:

- Doherty (load modulation) [6.21, 6.30]
- Chireix (outphasing) amplifiers [6.20]
- Envelope-tracking (ET) [6.182]
- Envelope elimination and restoration (EER) or Khan [6.77] amplifiers.

They are typical examples for efficient linear amplifiers. Table 6.2 summarizes the characteristics such as gain, bandwidth, linearity, and efficiency performance characteristics of different classes [6.30]. The original classes are extended, once the DC-bias and load are also modulated, leading to various forms of variants, e.g., in [6.30, 6.54]. Further, several variants exist for the envelope-tracking depending which time constants are used [6.182]. No optimum solution is available for all applications; however, the application of more advanced concepts is vital for efficient linear PAs. III-N devices favor several of these advanced concepts.

Amplifier Examples using III-N Devices

Many reports for the realization of the aforementioned amplifier classes and types using GaN HEMTs are available:

- For pure Class-A operation; see, e.g., [6.104]
- For pure Class-B operation; see, e.g., [6.92, 6.110, 6.120, 6.191]
- For Class-C operation; see, e.g., [6.189]

Simulations of Class-B operation of amplifiers based on GaN HBTs are provided in [6.76]. The simulations reveal an issue with a mismatch of the optimum load for optimum output power and optimum gain. Output harmonic termination techniques for AlGaN/GaN HEMT power amplifiers at 2 GHz using an active integrated antenna approach are discussed in [6.24]. The output termination of the second harmonic is short-circuited, while the third harmonic is terminated with an open structure. The real harmonic termination improves the PAE by 10–15% between 1.2 and 2.4 GHz. Class-C amplifiers are typically not considered for communication amplifiers as they reduce the amount of gain by at least 6 dB and strongly reduce linearity. Deep Class-C operation is used for III-N devices to enable the high-efficiency/high-power density operation at very high operation voltage in [6.189]. Further, Class-C is used in the load-modulation transistor in the Doherty concept [6.21, 6.96]. III-N Class-D-type RF-amplifiers have been considered in a number of publications [6.45], however, so far not been extensively used [6.52]. Class-D requires high f_T for the FETs, which are available in III-N devices. However, the loss of the amplitude information and the limited bandwidth make these amplifiers unsuitable for communication applications. III-N examples are given in [6.112] with 90% efficiency reached at 30 MHz. GaN HFETs enable the operation of this amplifier class, which typically used in the lower MHz regime, up to about 1 GHz [6.3, 6.135].

GaN Class-E and Class-F Amplifiers

GaN-based switch-mode Class-E hybrid amplifiers with 80–85% PAE at 2 GHz with associated output powers of 10 W are reported in [6.153]. The targeted bandwidth for the single-stage device amounts to 200 MHz from 1.9 to 2.1 GHz with 12 dB power gain. The matching is performed for a biasing to $I_{D\max}/4$. The high f_T of the devices enables operation in Class-E up to 3 GHz with 75% associated PAE.

A two-stage class-E amplifier in [6.45] achieves 18.2 dB of gain at 2 GHz with an associated PAE=50%. Similar results are reported by Eudyna in [6.166] with a linear gain of 19 dB at 2.1 GHz and 82% of maximum drain efficiency in a single-stage 10 W device operated at $V_{DS}=50$ V. Again, the outstanding breakdown capabilities of GaN HEMTs are mentioned to overcome the high V_{DS} -voltage peaks of 135 V. A comparison between class-E power amplifiers employing LDMOS FETs at 1 GHz and SiC MESFETs at 2.14 GHz is given in [6.124]. The devices are oversized to achieve the appropriate efficiency, which is defined by the R_{on} . A proprietary LS-model based on the Curtice approach is used for simulation deep in class-B and class-C mode. Bandwidth information on the harmonic tuning for GaN HEMT class-E power amplifiers is given in [6.95]. The efficiency improvements can

be obtained for a bandwidth of $\leq 200\text{ MHz}$ at 2.14 GHz . Class-E amplifiers based on GaN HFETs have been subjected to DPD and one-carrier WCDMA signals in [6.80]. An EER/ET system is applied to obtain an average PAE of 48% and a PAR of 7.6 dB . 10 dB of gain are achieved with an average output power of 1.4 W . The predistortion reduces the EVM from critical 20 to 2.6% and thus below the critical specification of WCDMA communication. The efficiency of class-F and inverse class-F amplifiers is discussed for GaAs devices in [6.63]. Class-F and inverse class-F in theory do not differ in efficiency as RF-voltage and current are simply exchanged. In reality, inverse class-F and class-F amplifiers show differences in efficiency values for different quiescent currents I_{Dq} for both bipolar and FETs. The background of this behavior is the impact of the even-mode terminations at different current levels. Class-F amplifiers in GaN HFET field-plate MMIC technology have been demonstrated in [6.44, 6.47]. Very high output power densities of $\geq 6\text{ W mm}^{-1}$ and efficiency levels of up to 50% can be reached in this MMIC approach at 2 and 2.7 GHz . The current-gain cut-off frequency f_T amounts to $15\text{--}20\text{ GHz}$, which is a factor of 6 higher than the frequency of operation. The absolute output power of the amplifier is 38 dBm . The simulated prediction of the PAE is 55–60%. With the use of more efficient GaN HFETs, hybrid class-F amplifiers with output power levels of 16 W and associated PAEs of 80% at $V_{DS} = 42\text{ V}$ have been demonstrated recently [6.146]. The second to fourth harmonic are matched in this case. It is mentioned that the main efficiency increase is caused by the accurate matching of the first output harmonics similar to the findings in [6.134]. The input matching network provides a fundamental match and 2nd harmonic short. The gate periphery of the GaN HFETs is $W_g = 3.6\text{ mm}$, the linear gain $\geq 15\text{ dB}$. Simulated class-F and inverse class-F amplifiers are again compared with the result, that the class-F amplifier leads to higher DE for a given output power in this comparison. This is based on the fact, that the Class-F amplifier has a lower average current for the same output swing. GaN-based class-F amplifiers have also been reported in [6.25] applying a second harmonic termination at 5.5 GHz in C-band. Even more advanced approaches based on GaN FETs, such as EER amplifiers [6.58, 6.79], have been proposed, as discussed later. The Chireix outphasing amplifier is realized based on Si LDMOS [6.62]. New $\Sigma\text{--}\Delta$ transmitter architectures are being proposed with extremely high requirements to the HPA transistors with regards bandwidth, speed, and robustness [6.22]. Class-S power amplifiers-based GaN HFETs have been mentioned in [6.124], so far without further realization. However, the potential of III-N for the advanced architectures is clearly visible.

6.2.2 General Design Considerations of III-N Amplifiers

III-N devices are attractive for amplifier design due to the higher intrinsic impedances on semiconductor level [6.100]. However, this fact alone does not necessarily imply that GaN HFET amplifiers are generally higher in

impedance. A key consideration is the RF-transformation through the layout, especially in high gate width/multifinger devices or at higher frequencies, e.g., in Ka-band [6.31, 6.168]. At frequencies of 2 GHz, the intrinsic output matching is nearly ohmic, apart from the compensation of the output impedance C_{ds} [6.25] and of the parasitic contribution of layout and combining. The same is true for the input matching of the devices [6.180]. However, for large-periphery devices the situation is very different. The input impedance is very low, partly through the transformation of the parasitic access contributions to the device [6.181]. Apart from the parasitic layout contribution, the packaging contribution has to be considered, which adds significantly to the impedance. As an example, a dual push–pull packaging concept is used in [6.100] applying a dual impedance transformation, which modifies the actual device impedances with high parasitic contributions. Internal prematching concepts are also applied for large-periphery GaN HFETs, e.g., in [6.181] for class-AB, and in [6.166] for class-E operation.

6.2.3 Mobile Communication Amplifiers Between 500 MHz and 6 GHz

Benchmark: Silicon Laterally Diffused MOS (LDMOS) and GaAs Devices

Silicon LDMOS devices provide a sophisticated benchmark for the use of GaN HEMTs in third (3G) and fourth (4G) generation mobile communication base-station systems for high-bandwidth highly-linear applications. Good comparisons between different base-station device-technologies are given, e.g., in [6.99, 6.172, 6.174].

Linearity vs. Power-Added Efficiency for Silicon and GaAs

The fundamental trade-off between linearity and efficiency in highly linear operation is crucial for high-power communication applications. The efficiency at defined linearity constraints according to standards such as GSM or 3GPP standards is the key specification for any base-station system. The theoretical limits for this operation are explored in [6.172]. State-of-the-art performance for silicon LDMOS devices can be found in many publications, e.g., in [6.13, 6.42, 6.99, 6.172]. For a two-carrier W-CDMA signal the LDMOS HV6 device delivers an output power of 20 W at 2.1 GHz at an efficiency of 29% at an ACLR level of -37 dBc of 10 MHz offset [6.13]. The evolution of the LDMOS technology generations is discussed in [6.172]. Gate peripheries $W_g = 3 \times 50\text{ mm}$ are needed to obtain output power levels of 100 W. Efficiency levels of 32% are reached for an ACLR of -37 dBc in two-carrier WCDMA operation with a linear gain of 18.5 dB. A gate length of 140 nm is used for the devices. A 200 W LDMOS-based Doherty amplifier is reported in [6.42]. A maximum PAE of 34% is found for WCDMA operation at 6 dB

backoff and an APCR level of -37 dBc. Similar results are provided in [6.99], which yield 29% PAE at -37 dBc and an output power of 34 W and 2.1 GHz. The increase of PAE in highly linear amplifiers has become a major focus for LDMOS device development, which is well progressing. Even for higher operation voltages a 120 V interdigitated-drain LDMOS (IDLdMOS) on SOI substrate is discussed, e.g., in [6.196], breaking the LDMOS power limit.

GaAs-FET and -HFET high-voltage technologies have also been proposed, e.g., in [6.35, 6.109, 6.125]. The advantage of GaAs relative to LDMOS is the increased gain margin for a given gate length, which also more easily enables WiMAX applications at 3.5 GHz and beyond. A 45 W GaAs-power technology is demonstrated [6.125] with HFETs with a gate periphery of 32.4 mm and an operation voltage $V_{DS} = 26$ V for a gate length of $0.8\text{ }\mu\text{m}$. The 6-in. wafers are thinned to $25\text{ }\mu\text{m}$. A drain efficiency of 32% is achieved for an IM_3 of -37 dBc with a two-carrier WCDMA signal for an average output power of 9.2 W at 2.14 GHz.

Properties of GaN HEMT Base Station Amplifiers

GaN HEMTs are a subject of active research for base-station applications. A general overview of the suitability of different device technologies for reconfigurable, multiband, multicarrier amplifiers is given in [6.36, 6.40]. Wide bandgap semiconductors provide the clear advantage of strongly reduced memory effects. Impressive GaN device results including DPD are provided, e.g., in [6.79, 6.109, 6.129, 6.180]. Possible advantages of GaN HEMTs in amplifiers relative to silicon LDMOS and GaAs HFETs are given in the following enumeration; see, e.g., [6.40, 6.174]:

- Higher impedance levels
- Increased bandwidth, i.e., multiband and multicarrier functionality [6.40] and increasing frequency agility at system level
- Increased efficiency in linear operation [6.174]
- Improved thermal properties, and thus reduced thermal memory effects [6.40]
- Increased gain levels for the same gate length

These advantages are now discussed in more detail.

Impedance Levels

Fig. 6.3 gives the optimum impedance of GaN HFETs at 2 GHz as a function of gate width derived for $V_{DS} = 28$ V operation, which is typical of base stations using LDMOS. For comparison with an improved technology, the optimum fundamental load impedances are given at an operation voltage of 48 V. The associated output power is also given. The output capacitance C_{ds} to compensate is nearly independent of the operation bias and can be directly obtained from the gate periphery in Fig. 6.3 and a constant small-signal value, e.g., $C_{ds} = 0.3\text{ pF mm}^{-1}$.

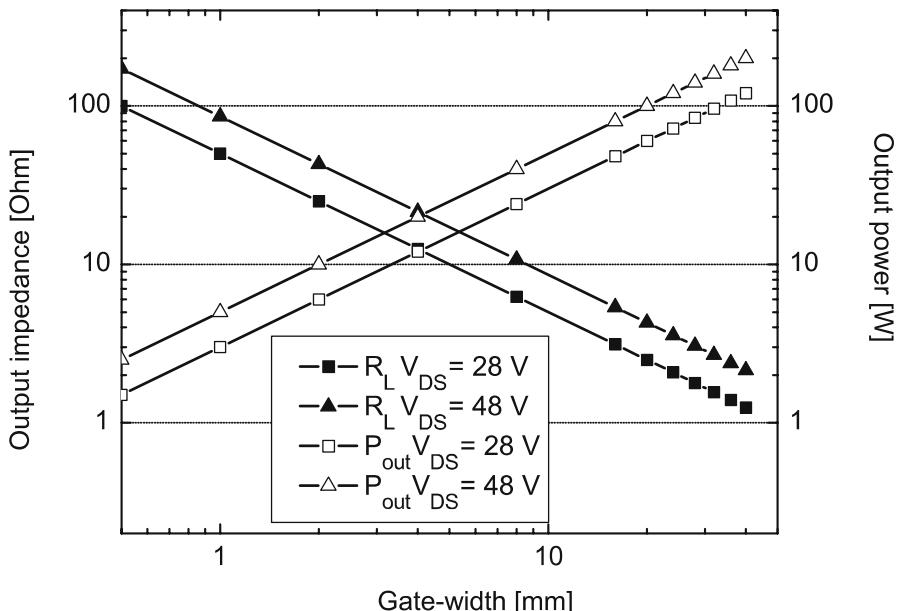


Fig. 6.3. Impedance levels and output power of a GaN power HEMT on s.i. SiC at 2 GHz as a function of gate width at $V_{DS} = 28 \text{ V}$ and $V_{DS} = 48 \text{ V}$

Linearity vs. Power-Added Efficiency in GaN Devices

The efficiency of GaN amplifiers on circuit level for highly linear applications will be discussed starting from conventional class-AB concepts [6.73], push-pull concepts [6.100], Doherty amplifiers [6.21], and switch-mode amplifiers [6.47]. The considerations are finalized with reports on more advanced circuit concepts. General linearity considerations of GaN devices are given in a number of publications, e.g., [6.59, 6.110, 6.184]. High linearity of AlGaN/GaN HFETs on silicon substrates at 4 GHz is demonstrated in [6.175]. The intermodulation distortion is significantly better than in GaAs devices with the same output power density of 1 W mm^{-1} . High-power and linearity performance of GaN HEMTs on sapphire substrates is reported in [6.184]. A significant improvement of the IM_3 is found for the GaN FET at any output power level. Another study of large-signal linearity and efficiency of AlGaN/GaN MODFETs in [6.59] shows that the optimum impedances for maximum PAE and maximum P_{out} at 5 GHz are close (however, not identical) and well behaved. Further, the third-order intercept point is found to be insensitive to the gate bias. The properties of different Si, GaAs, and GaN FETs with respect to memory effects are discussed in [6.40]. The shape of the UMTS signal for different memory situations is discussed. For static nonlinearity, i.e., without memory effects, the spectral shaping has a convex structure on a logarithmic scale. For devices with memory, a concave behavior is typically

observed. The real situation in devices is typically a combination of static and dynamic nonlinearity. The mixture of the two curvatures can then lead to an inflection point. In this investigation SiC MESFETs show no or minor memory effects relative to the strong effects observed in silicon LDMOS devices. The metric for memory effects and the application of a memoryless linearizer in [6.103] clearly suggest the strong improvements through memoryless compensation in GaN HFETs as compared to silicon LDMOS.

GaN HEMT Circuit Examples: Drivers

The need to reduce the number of stages in the base-station amplifier leads to a number of developments also for highly linear broadband driver amplifiers. A wide-band three-stage single-ended power module for multicarrier operation for drivers is given in [6.144]. A linear gain of 30 dB is reported for a bandwidth of 500 MHz between 1.8 and 2.3 GHz. The ACLR is lower than -50 dBc at an average output power of 19 dBm for a two-carrier WCDMA signal for an offset frequency $\Delta f = 10$ MHz. The use of dual-gate GaN HFETs for driver applications is discussed in [6.27, 6.177]. Linear gain levels of 30 dB per stage at 2.14 GHz can be reached at an operation bias of 48 and 60 V with similar efficiency levels. Further, RF-reliability is demonstrated. A broadband amplifier between 0.2 and 4 GHz delivers a WCDMA output power of 20 dBm at an ACLR of -45 dBc. A second example demonstrates a driver for WiMAX applications [6.27] between 3.2 and 3.8 GHz, again combining high gain (10 dB over the band) with broadband capability and linearity. This amplifier provides an output power of 27 dBm at an EVM of 2% in compliance with the WiMAX requirements.

GaN HEMT Circuit Examples: Final Stage

Several examples of power amplifiers based on GaN HEMTs exist.

GaN Class-A/B Amplifiers

A single-ended amplifier with a gate periphery $W_g = 48$ mm is reported applying a prematching concept within the device package. Output power levels of 370 W at 2.11 GHz are reached [6.111, 6.180]. The linearization of this amplifier is reported in [6.181]. For a two-carrier WCDMA signal, average output power levels of 60 W with an IM_3 of less than -50 dBc at 10 MHz offset are reached. The maximum drain efficiency of 24% is found at an average output power of 47.8 dBm and an ACLR of -35 dBc. This level of IM_3 is still in the range of modern linearization techniques to reach -45 dBc after linearization. Another single-ended GaN HFET amplifier with an output power level of 200 W is reported in [6.75]. The device is composed from two chips with a gate width of 36 mm each to reduce the thermal resistance. The bandwidth is 60 MHz at 2.11–2.17 GHz. A drain efficiency of 34% is reported at

a peak-to-average ratio (PAR) of 8 dB or 45 dBm average under two-carrier WCDMA operation. The distortion of the GaN HFET is found to be worse than in a comparable silicon LDMOS. However, after the application of a DPD system, the ACLR of -50 dBc can be achieved at 8 dB backoff and an associated PAE of 34%. Fujitsu further reported a push–pull GaN HEMT amplifier consisting of two 36 mm devices with an overall peak output power level of 250 W [6.78]. For a four-carrier WCDMA signal, an ACLR of -50 dB is reached at an efficiency of 37% at 46 dBm average output power. The single 36 mm device reaches more than 150 W of cw-output power. A broadband push–pull amplifier is given in [6.73]. The device yields more than 50.1 dBm of peak output power at 1.95 GHz under 16-channel single-carrier WCDMA operation with an operation bias of 35 V and a gain of 12.9 dB. The 3 dB-bandwidth is 400 MHz. Broadband HPAs for WiMAX applications between 3.3 and 3.8 GHz are reported in [6.163, 6.164]. The single transistors yield output power levels of ≥ 38 dBm at PAE levels of $\geq 17\%$ and EVM levels of 2% at $V_{DS} = 28$ V and 11 dB gain under OFDM operation.

Doherty Concepts

Good examples for highly efficient LDMOS power Doherty amplifiers for CDMA base stations are given in [6.15]. Efficiency levels of 40% are reached at 40 W of output power with an ACLR of -31 dBc at 2.1 GHz. The gain is ≥ 10 dB. GaN-based Doherty amplifiers are reported in [6.96]. The Doherty concept yields an efficiency of over 50% extending over 6 dB of dynamic range for output power levels of 1 W. A 40 W peak-power GaN Doherty power amplifier is reported in [6.21]. The power gain is 11 dB from 1.8 GHz to 2.5 GHz. Once linearized, a peak PAE of 65% and a linearity of -55 dBc at 5 MHz offset are obtained for a one-carrier WCDMA signal. More recently, very powerful GaN Doherty amplifiers are reported [6.165, 6.197]. A two-stage design with an average output power of 80 and 450 W peak power at 2.14 GHz is reported in [6.165]. 55% PAE are obtained at -6 dB backoff from the saturated output power. A careful design of the reference plane is applied transforming the input and output impedances of the main and the peak amplifier by means of the parasitics and the matching networks. Both main and peak amplifier consist of 2×36 mm devices. The linear gain amounts to 32 dB at 2.14 GHz. Based on similar devices, a Doherty with increased power range is proposed in [6.197]. Two devices with $W_g = 36$ mm each yield an average output power of 45 dBm at 50% at an ACLR of -38 dBc without the application of a DPD. The increased dynamic range is achieved through the asymmetrical bias of the peak and the main amplifier: the peak amplifier is biased at a lower V_{DS} of 40 V rather while the main amplifier is operated at $V_{DS} = 50$ V.

Envelope-Tracking and Envelope Elimination-Restoration Amplifiers

The envelope-tracking (ET) and the envelope elimination-restoration (EER) concept are attractive as they combine high-efficiency with high-linearity

and high-bandwidth capability and offer further opportunities for predistortion. Wide bandwidth envelope-tracking amplifiers for orthogonal frequency-division multiplexing (OFDM) applications such as WiMAX are analyzed in [6.182]. A channel bandwidth of 16.25 MHz is used, the RF-bandwidth is 83.5 MHz at 2.4 GHz. The realization is based on GaAs MESFETs. A GaN HFET-based envelope-tracking amplifier with 50% PAE is demonstrated in [6.79] under single-carrier WCDMA operation. Digital predistortion is used on two levels. Memoryless DPD is used to compensate the gain variation over the envelope of the amplifier. Deterministic memory mitigation is used to further increase the linearity. The WCDMA signals have a reduced (clipped) PAR of 7.67 dB. An average output power of 37.2 W is measured for an ACLR-level of -52 dBc at 5 MHz offset from the carrier. Further, a class-E amplifier based on GaN HFETs is used in an envelope elimination restoration/envelope-tracking (EER/ET) system in [6.80]. With an unchanged PAE of 48%, improved linearity is achieved via predistortion of the class-E amplifier. The linearized EVM is 2.6% with predistortion, while only 20% is achieved without DPD. Recently, very high efficiency EER amplifiers have been reported based on 10 W GaN HEMTs [6.58]. The actual amplifiers are realized in class-F with class-C bias for the highly efficient PA and deliver efficiencies of up to 73% with harmonic control of the second and third harmonic at 2.14 GHz under OFDM operation.

GaN HFET Switch-Mode Amplifiers

Switch-mode amplifiers generally improve efficiency, however, suffer from reduced linearity and bandwidth due to the harmonic control, e.g., [6.34]. GaN-based switch-mode class-E hybrid amplifiers at 2, 2.7, and 3.5 GHz are reported in [6.153]. PAE values of 80–84% at 2 GHz, of 76–82% at 2.7 GHz, and of 72–78% at 3.5 GHz with associated output powers of 10 W are given. The linear gain is 11–12 dB at all frequencies. A device with a larger periphery yields 63 W with 75% associated PAE and $V_{DS} = 28$ V at 2 GHz. A GaN-HEMT-based class-E amplifier at 2.1 GHz is given in [6.166]. A drain efficiency of 45% at an ACLR of -50 dBc is reached with the application of a digital predistortion. A two-carrier WCDMA signal is transmitted with a PAR of 7.8 dB. The transmission of the amplitude information contradicts the original definition of a class-E amplifier as a switch-mode amplifier. The operation voltage is 50 V. Examples of class-F and class-D amplifiers based on GaN HEMTs have already been discussed above.

Final Stages: Linearization

Analog and digital predistortion concepts from the LDMOS world have been applied to GaN HFETs. A general finding for GaN HFETs is the very positive impact of linearization techniques [6.75, 6.103]. Possibly the strong effect in GaN HEMTs is due to the low P_{-1dB} relative to the saturated power and the soft power compression behavior of the device. Further, memory effects

are strongly reduced [6.40]. The use of an analog prelinearization for GaN HFETs with an additional gate diode is described in [6.192]. The nonlinearity of the input capacitance is compensated by the application of the diode. High-efficiency feed-forward amplifiers using RF-predistortion linearizers for a modified silicon LDMOS Doherty amplifier are discussed in [6.117]. An average efficiency of 13.6% is reached at an output power of 45 W and an ACLR of -55 dBc. The linearized feed-forward amplifier has a 3.5% efficiency advantage over the nonlinearized version. Linearity and efficiency performance of GaN HEMTs on s.i. SiC substrate are given in [6.129] with the application of a PCM Sierra digital predistortion correction. The gate-width of the GaN HFET is 36 mm. Efficiency levels of 43% at an average output power of 11 W at 2.1 GHz are reached for two-carrier WCDMA signals at $V_{DS} = 28$ V. The DPD correction allows a 7 dB increase in linear output power and an increase of the PAE from 24 to 33%. The reduction of the quiescent bias to class-A/B leads to an increase of the ACLR of about 5 dB. An overview of linearization techniques and a comparison of GaN HFETs, GaAs HFETs, and silicon LDMOS devices is given in [6.91]. Future systems will require two-to four-carrier operation with up to 60 MHz bandwidth. Higher order IMD contributions are mentioned in [6.173] for GaN HFETs in comparison with GaAs FETs. The particular DPD implementation yields an improvement of the ACLR of about 20 dB for all three device technologies. System aspects, such as additional service costs at higher power densities, are also considered. Further the system aspects of a change of the operation voltage from $V_{DS} = 28$ V to 50 V are discussed [6.91, 6.173]. The need to adjust the distortion correction algorithms to the unique properties of each semiconductor technology is mentioned in [6.173]. The latter consideration gives additional potential to the GaN HFETs where the algorithms are not yet mature, i.e., not specific. It is further mentioned that the memory effects in the particular GaN PA are strong, however, can be very well suppressed by memory compensation. This concludes the base-station considerations.

6.2.4 C-Frequency Band High-Power Amplifiers

GaN HFETs are very attractive for the use in C-band (4–8 GHz), as the C-band frequencies cannot be reached by state-of-the-art SiC MESFETs and silicon LDMOS devices. Good references of packaged GaAs HEMTs for C-band applications with output power levels of 70 W and 50% PAE are given, e.g., in [6.179]. Initial reports of GaN-HEMT-based C-band high-power transistors and power amplifiers are given, e.g., in [6.25, 6.187]. The impact of second harmonic termination on the efficiency in C-band is described in [6.25]. PAE levels of 60% at 5.6 GHz are reached. Output power levels beyond 100 W at C-band are described in [6.69, 6.119]. CW-output-power levels of 60 W at 4 GHz and $V_{DS} = 61$ W are reached with an AlGaN/GaN HFET with $W_g = 24$ mm [6.155]. The device is internally matched. The linear gain is 10.2 dB with a maximum PAE of 42% in field-plate technology with a gate

length $l_g = 0.5 \mu\text{m}$. The output power is as high as 156 W at 4 GHz for pulsed-operation. The pulse width is 10 μs at a duty cycle of 1% at $V_{DS} = 50 \text{ V}$. This leads to a power density of $\geq 6 \text{ W mm}^{-1}$ for the same device with $W_g = 24 \text{ mm}$. The passive elements of the packaged device are realized on alumina substrates in a package with $12.7 \times 12.9 \text{ mm}^2$ [6.155]. This is approximately half of the area used for a GaAs FET. Power levels of 60 W, but drain efficiency levels of $\geq 50\%$ have been reported in [6.65]. The PAE is 45%. The gate width is $W_g = 16 \text{ mm}$. Short and open stubs are used to realize a broadband matching of fundamental and second harmonic at the output. The relative bandwidth achieved is 15%. A new device passivation technique leads to output power levels $P_{out} = 100 \text{ W}$ in a single device without the application of a field plate [6.69]. The gate length is $l_g = 0.4 \mu\text{m}$, the unit gate width amounts to $300 \mu\text{m}$. The device yields a gate periphery $W_g = 50.4 \text{ mm}$ with a pulsed-output power density of 2.8 W mm^{-1} . The pulsed-output power is $P_{out} = 140 \text{ W}$ with an associated PAE of 25% at a bias $V_{DS} = 40 \text{ V}$ (duty cycle 2.5%, pulse width 20 μs). The linear gain is 10 dB. The large gate periphery used make the devices very susceptible to even- and odd-mode oscillations. A detailed analysis of a GaN FET multicell configuration is given in [6.199]. The probe insertion analysis of [6.162] is used. The conditions to be fulfilled for loop oscillations read in general

$$\text{loop phase } \angle \Gamma = 0 \quad (6.3)$$

$$\text{loop gain}|\Gamma| > 1 \text{ (0 dB).} \quad (6.4)$$

Odd-mode oscillations are suppressed by adding additional losses such as isolation resistors into the loop path and further by structuring the matching circuits around the semiconductors. A record output power of 170 W at 6 GHz has been reported combining four chips with $W_g = 11.52 \text{ mm}$ of gate periphery each in a package [6.160]. The chips are internally matched. Even higher output power levels are reported in [6.200]. A single chip amplifier yields an output power of 167 W with 7 W mm^{-1} power density at 5.6 GHz ($W_g = 24 \text{ mm}$) with a strongly reduced duty cycle of 2.5% and 20 μs pulse width. In a two-chip configuration ($W_g = 48 \text{ mm}$) 220 W of output power are obtained at 5.6 GHz with a 10% duty cycle and $V_{DS} = 60 \text{ V}$. The increase of the gate-to-gate pitch to $30 \mu\text{m}$ is the key to reduce the thermal resistance to values acceptable for high power operation ($R_{th} = 9.6 \text{ K W}^{-1} \text{ mm}^{-1}$). The total package area is $8 \times 8 \text{ mm}^2$. The integration of active antennas and the application of harmonic techniques at 7.25 GHz are discussed in [6.24]. A chip with $W_g = 1 \text{ mm}$ achieves an output power of 30 dBm and a peak PAE of 55% with a power gain of 14 dB for a gate length $l_g = 0.8 \mu\text{m}$. A 30 dB suppression of the output-side harmonics is achieved. In summary, the output power levels and bandwidths for C-band HPAs can be dramatically increased as compared to the best GaAs HEMTs with further potential of area reduction and higher operation voltages.

6.2.5 X-Band High-Power Amplifiers

Efficient high-power amplifiers in the X-band (8.2–12.4 GHz) need to combine high-operation voltages and low-current levels with high-relative bandwidth and high efficiency at these frequencies. Such hybrid and MMIC amplifiers are key examples to be realized in GaN HEMT technology, e.g., [6.139].

X-Band Reference Amplifiers: GaAs PHEMT and GaAs HBT-Based MMICs

GaAs MESFET, GaAs PHEMT, and InGaP/GaAs HBT solid-state amplifiers provide benchmarks for the comparison of GaN HEMT amplifiers for high-power high-efficiency operation in C-band [6.185], X-band, and Ku-band [6.14] applications. Not all relevant results may be published; however, some overview shall be given. General MMIC design strategies suitable for X-band have been reported, e.g., in [6.6, 6.167]. CW-power levels of up to 2 kW at X-Band have been reported based on solid-state devices when several MMICs and MMIC-modules [6.4, 6.41] based on solid-state power amplifiers are combined in power. Output power levels of up to 16 W at X-band and multiwatt (≥ 5 W) at Ka-band have been reported on GaAs chip level [6.84, 6.178]. Area efficiency, bandwidth, and PAE are still being improved. Traveling wave tube (TWT) replacement by solid-state solutions is often considered, e.g., [6.32]; however, tubes are still strongly improving [6.97] and both the efficiency and the associated output power levels achieved with SSPAs are not yet fully appropriate for all applications, e.g., [6.178]. Solid-state multi-PA solutions in general feature the advantage of graceful degradation [6.4]. GaAs MMICs provide a stable, mature, and still improving reference for the evaluation of GaN HEMT MMICs. Following an impressive roadmap, GaAs device performance is still improving today and chip size is still continuously reduced, e.g., [6.49]. State-of-the-art GaAs microstrip PHEMT MMICs provide output power levels above 40 dBm [6.12] and maximum PAE levels above 50% at reduced output power levels, e.g., [6.183], while efficiency is traded for output power and bandwidth. Power densities of up to 1 W mm^{-2} can be reached on the GaAs MMIC level [6.19]. GaAs HBTs provide performance similar to GaAs HEMTs in X-band [6.28, 6.43] and S-band, e.g., [6.126]. The typical chip size is $3.3 \times 5.7\text{ mm}^2$ [6.202] for a GaAs PHEMT PA with an output power of ≥ 10 W. A GaAs HBT 10 W amplifier has a chip size of $4.74 \times 4.36\text{ mm}^2$ in microstrip transmission-line technology, as reported in [6.28]. The linear gain is 18 dB with an efficiency of better 35% over 1 GHz of bandwidth. Further MMIC size reduction of X-band amplifiers is discussed, e.g., in [6.49]. Integration of several chips leads to power levels of 160 W [6.41]. Power levels as high as 2,000 W have been reported in solid-state-based systems [6.4]. Examples of GaAs PHEMT coplanar-waveguide HPAs are given, e.g., in [6.11]. The chip size is $4 \times 4\text{ mm}^2$. A maximum output power level of ≥ 5 W and power-added efficiencies of $\geq 50\%$ are reached.

X-Band GaN Hybrid Amplifiers

Several examples are available for hybrid high-power amplifiers based on GaN technology in X-band. A hybrid amplifier with a pulsed-output power of 40.7 W at 2.7 dB compression at 10 GHz is demonstrated with GaN HEMTs on s.i. SiC with $W_g = 12$ mm. The amplifier yields a PAE of 29% in [6.130]. The linear gain is 13.5 dB in class-A operation using source viaholes. A similar result is reported in [6.26, 6.115, 6.154]. A DC-pulse width of 20 μ s is used, along with a pulse repetition of 2 kHz. The high-operation voltage is $V_{DS} = 55$ V and required to suppress the odd-mode oscillations. A single-stage hybrid GaN HFET X-band power amplifier with a saturated cw-output power of 22.9 W and 37% associated PAE at 9 GHz and $V_{DS} = 36$ V is given in [6.107]. Similarly, an output power of 21.9 W is reported with 42% of associated PAE. The saturated cw-power density yields 6.3 W mm^{-1} on the transistor level. The linear gain of the amplifier amounts to 9 dB with a measured bandwidth of 2 GHz. Further examples include a hybrid GaN HEMT push–pull amplifier in class-AB operation at 8 GHz, demonstrated in [6.92]. Output power levels of 36 dBm are reached at 5.2 GHz with a periphery $W_g = 2 \times 1.5$ mm. The amplifier yields a PAE of 42%. High-linearity and high-efficiency class-B amplifiers at 10 GHz, realized in GaN HEMT technology, are given in [6.120]. PAE levels of 54% are predicted for the push–pull configuration, however, are not verified by experiments. Power combining of hybrid GaN HFETs yields 60 W–81 W of output power, as reported in [6.161, 6.198]. On hybrid packaged transistor level, Toshiba developed a GaN HEMT with a maximum output power of 81 W in cw-operation based on two 11.52 mm chips. The PAE amounts to 34% at 9.5 GHz and a gain compression level of 3 dB [6.161]. The backside is thinned to 150 μm to reduce the thermal resistance. The overall package size is $11 \times 12.9 \text{ mm}^2$. The device is optimized for an operation bias $V_{DS} = 20$ V and $I_{DS} = 4$ A. A similar result is obtained with a gate periphery of 2×12 mm and a gate length $l_g = 0.5 \mu\text{m}$ with a hybrid AlGaN/GaN HEMT. The devices are thinned down to 100 μm . The two chip device yields an output power of ≥ 60 W and a maximum PAE of 35% at 10 GHz. The linear gain is 10 dB in Class-B operation [6.198]. The input and output impedance is 50Ω . The bandwidth is 1 GHz with a PAE $\geq 28\%$. The overall package size is $21 \times 12.9 \text{ mm}^2$.

X-Band GaN HEMT Circuits: Flip-Chip Technology

The flip-chip integration approach is favorable for power amplifiers, as low-cost passive carrier substrates with high-thermal conductivity can be combined with low-cost substrates with low-thermal conductivity for the active devices, e.g., [6.152]. A GaN-HEMT-based microwave power amplifier is demonstrated in [6.188] with 14 W of output power using GaN HEMTs grown on sapphire substrates. The active devices are flip-chip bonded on polycrystalline AlN substrates. The amplifier yields a -3 dB-bandwidth between 6–10 GHz with a peak gain of 9 dB. A peak output power of 14 W is reached with a power gain of 4 dB and an associated PAE of 25% at $V_{DS} = 25$ V. A power density of

6.4 W mm^{-1} at 6 GHz at an operation voltage $V_{\text{DS}} = 39 \text{ V}$ in pulsed-operation is reached in a 50 W AlGaN/GaN HEMT power amplifier [6.187]. The output periphery is $W_g = 8 \text{ mm}$, while the output load reported amounts to 7Ω . Again, a flip-chip technology on AlN carrier substrate is applied. GaN HEMTs grown on sapphire substrates for microwave power amplification and integrated in flip-chip technology are demonstrated in [6.186]. Metal resistors are made by Ti with SiN dielectric. MIM capacitors are realized by Au with SiN dielectric. Maximum output power levels $P_{\text{out}} = 7.6 \text{ W}$ at 4 GHz are reached with a periphery $W_g = 6 \text{ mm}$. A broadband amplifier reaches output power levels of 1.6–3.2 W between 3 and 9 GHz with a gate width $W_g = 1 \text{ mm}$.

X-Band GaN Monolithic Integrated Circuits

The monolithic integration of GaN HFETs at X-band frequencies (8.2–12.4 GHz) is very desirable in order to avoid losses in circuit performance with respect to efficiency and bandwidth. GaN MMICs with PAE = 40% are expected [6.140]. Losses occur when long bond wires or bumps are used, as mentioned, e.g., in [6.148]. Further, long bond wires introduce additional uncertainty for the realization of advanced circuit concepts, such as harmonic termination.

Microstrip Transmission-Line X-Band MMICs

A microstrip line passive environment is the technology of choice for the integration of GaN HFETs, due to reduced losses and smaller chip size relative to coplanar-waveguide approaches. While the process complexity is increased with the application of a backend process, standard design, and layout optimization flows can be used, based on microstrip transmission-lines [6.12, 6.28, 6.88, 6.167]. Chip-area reduction is the ultimate requirement for cost reduction also for GaN technology [6.49]. This can be most effectively performed in microstrip-line technology. As one of the first GaN MMICs in microstrip transmission-line technology on s.i. SiC, a dual-stage GaN HEMT MMIC is produced yielding pulsed-output power levels $P_{\text{out}} \geq 20 \text{ W}$ at 9 GHz, as given in [6.26]. The associated power gain and PAE amount to 14 dB and 20%, respectively.

Recent progress of GaN MMIC technology development in X-Band is reported, e.g., in [6.139]. As a general tendency, single-minded performance targets have been modified to also meet reliability and reproducibility targets, e.g., with respect to the choice of power densities. Further, the efficient operation of GaN HEMTs at Q-band (33–50 GHz) is enforced [6.139], which is also beneficial for the efficiency targets at lower frequencies. At the same time, GaN HEMT solid-state devices with a bandwidth of over one decade between 2 and 20 GHz, output power levels of $\geq 100 \text{ W}$, and efficiencies of $\geq 30\%$ are proposed. Further reports of GaN microstrip transmission-line MMICs are given, e.g., in [6.99, 6.148, 6.170, 6.171]. The dual-stage designs in [6.148, 6.170]

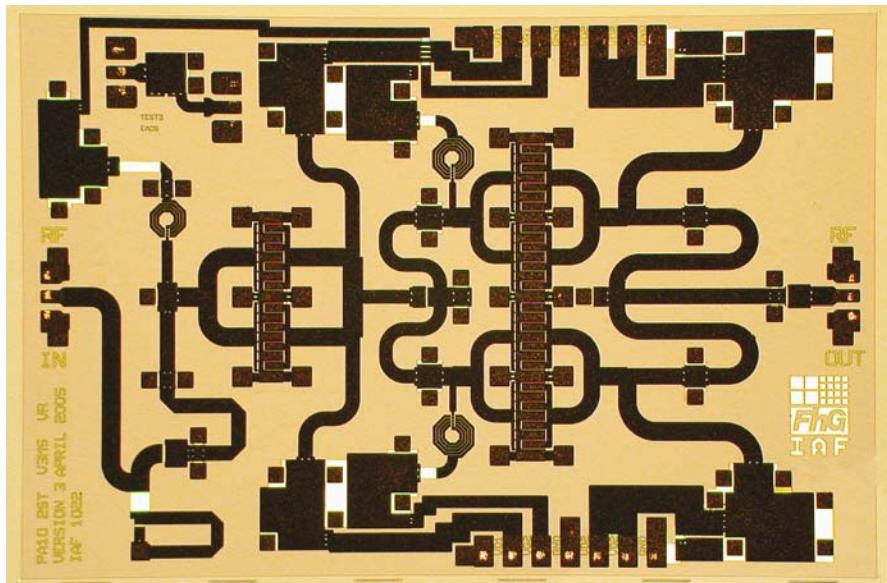


Fig. 6.4. Chip image of a dual-stage high-power amplifier in microstrip transmission-line technology, chip size $4.5\text{ mm} \times 3\text{ mm}$

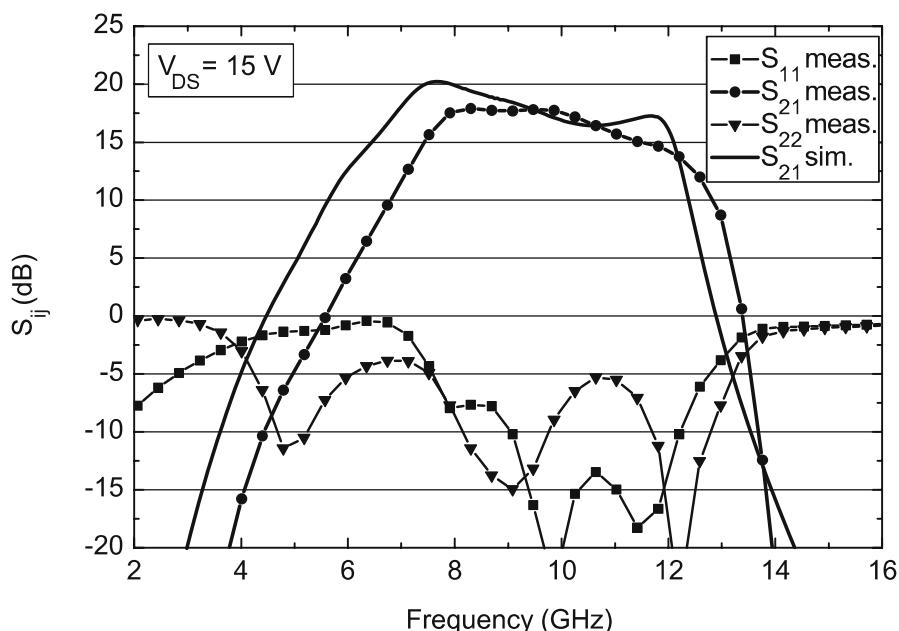


Fig. 6.5. S-parameters of the AlGaN/GaN HEMT MMIC amplifier in microstrip transmission-line technology

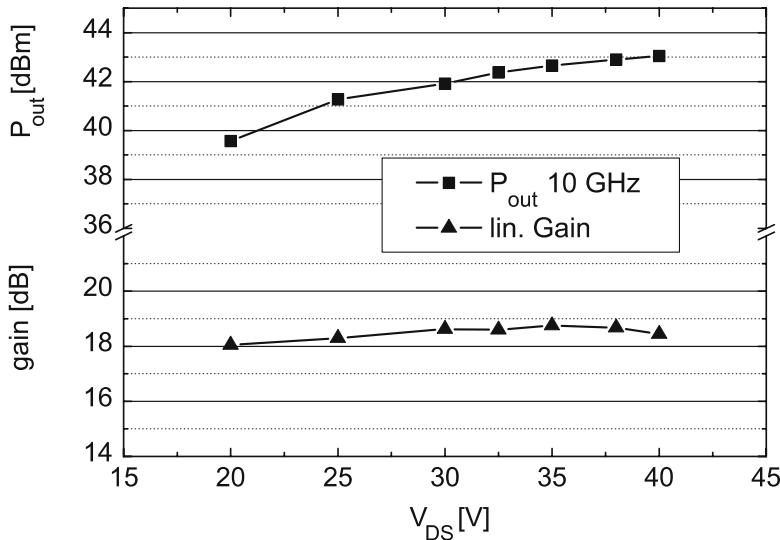


Fig. 6.6. Pulsed-output power and linear gain at 10 GHz as a function of V_{DS}

deliver output power levels of 20 W with a linear gain of 18 dB at $V_{DS} = 40$ V. For a second MMIC with 6 mm gate periphery, an output power at -1 dB compression beyond 14 W is achieved. The saturated output power is 22.4 W. The chip size is 4.5×3 mm 2 for the dual-stage, and 2.75×2.5 mm 2 for the single-stage device. Module integration of such X-band MMIC transmitter chains including an X-band driver amplifier is described, e.g., in [6.149]. Output power levels of 30 W at X-band are reached with the combination of two chips in the output stage. The thermal management and integration of such chips is of ultimate importance, see Chapter 8.

An X-Band Amplifier Example

The example is derived from [6.170, 6.171]. Fig. 6.4 gives the chip image of an X-band MMIC on s.i. SiC substrate. The chip size is 4.5×3 mm 2 . The device technology is based on a gate length $l_g = 300$ nm. The design is tweaked to achieve the desired gain level at the upper edge of the frequency band, in this case 12 GHz. The forced matching in the input network of the first stage ensures gain flatness over the band. Interstage matching is performed with particular emphasis to the maximum input drive needs of the second amplifier stage over the full frequency band. Fig. 6.5 gives the S-parameters measured in cw-mode of the microstrip MMIC at $V_{DS} = 15$ V. Both a broad matching and a broad amplification S_{21} can be observed. This is a typical property of GaN X-band MMICs, sometimes even independent of the design methodology. The S-parameters are well reproduced by the simulation, performed with an optimized LS-model. The gain at the higher band edge increases with the

increase of $V_{DS} > 15$ V. Fig. 6.6 gives the measured pulsed-output power as a function of operation bias V_{DS} . The figure shows the increase of the power gain and output power with V_{DS} up to 40 V.

Coplanar-Waveguide Transmission-Line MMICs

From a processing perspective, coplanar-waveguide MMIC amplifiers can be realized more simply, since no backside process is required as compared to the microstrip approach, e.g., [6.9, 6.10, 6.169]. A coplanar-waveguide X-band linear power amplifier GaN HEMT MMIC is reported in [6.191]. The chip size is 6×1.5 mm 2 . An output power of 36 dBm at 8 GHz is reached and yields an intermodulation distortion IM_3 of -35 dBc at 1 MHz offset and 34% of associated PAE. Single-stage coplanar-waveguide power amplifier MMICs yielding output power levels of 39 dBm with an associated PAE of 33% and a linear gain of 10 dB at 10 GHz are presented in [6.9]. The chip size is increased for this coplanar chips, partly due to the need to connect the ground plane on the front side of the wafer. The device does not use the full set of passive lumped components for matching. A chip size of 4×6.2 mm 2 is reported in [6.9]. A very compact coplanar MMIC design of a power amplifier reported in [6.81] delivers up to 16 W of output power at 8 GHz at an operation bias $V_{DS} = 28$ V. The chip size is 2.2×3.3 mm 2 in this case. The efficiency for this dual-stage MMIC is as high as 30%. The input and interstage matching are performed on small-signal level, whereas the output stage is matched to load-pull measurements.

Coplanar MMIC Example

The MMIC example is based on the considerations in [6.10, 6.169]. Fig. 6.7 gives the chip image of a dual-stage high-power amplifier in coplanar transmission-line technology. The chip size is 4.5×3 mm 2 . During the design phase a multistep procedure is used. Load-pull simulations of the power cells are performed with respect to gain, efficiency, and output power at a compression level given by the application. With respect to stability the load reflection is selected to have sufficient margin to the unstable region where the small-signal gain would be larger than the maximum MSG/MAG. In a further design step, the matching networks of output, input, and interstage are designed. The power combining structures are included in this analysis and are part of the networks. The interstage network transforms the output load of the first stage into the input network of the second stage. Sufficient gain flatness is achieved by designing the interstage network for best match near the upper edge of the operation frequency. Stability analysis is performed according to [6.118]. Further, 2.5D- and 3D-EM-simulations need to be performed for more complicated structures and their application in the layout even for coplanar structures [6.37, 6.68, 6.168]. Fig. 6.8 gives the measured S-parameters of the coplanar amplifier in cw-mode. In general, the very broadband performance of the X-band amplifiers can be observed for the

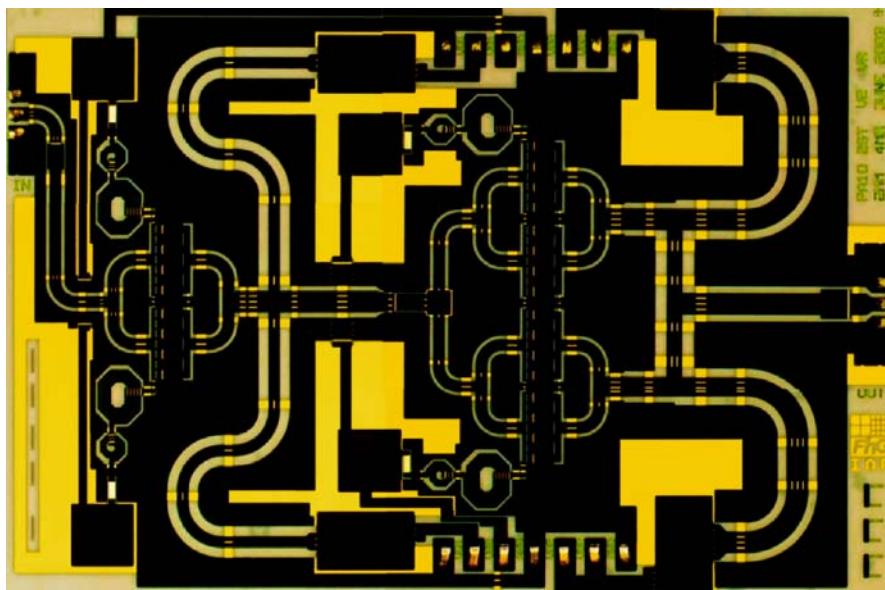


Fig. 6.7. Chip image of a dual-stage coplanar high-power amplifier, chip size $4.5 \times 3 \text{ mm}^2$

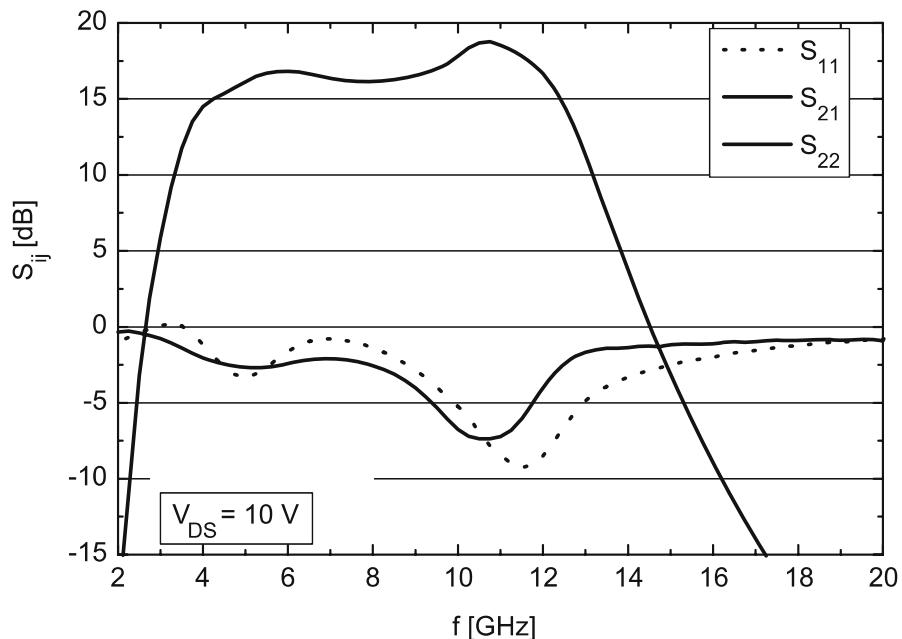


Fig. 6.8. S-parameters of a coplanar AlGaN/GaN HEMT MMIC X-band amplifier at $V_{DS} = 10 \text{ V}$

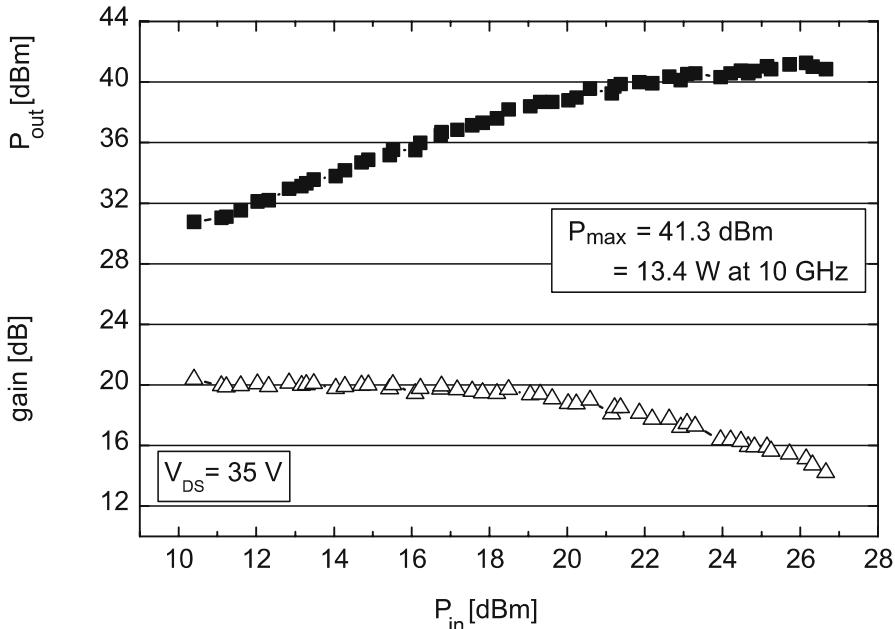


Fig. 6.9. Pulsed-output power and gain at 10 GHz and $V_{DS} = 35$ V

S₂₁. Fig. 6.9 gives the measured pulsed-output power and gain at 10 GHz. The MMIC delivers 13 W of saturated output power, which is equivalent to a power density of 3.3 W mm^{-1} at 10 GHz to a load of 50Ω . Given the maturity of the technology, which is inferior to GaAs, the longterm advantages of GaN MMICs become visible. Further design considerations will be analyzed in Sect. 6.2.6.

6.2.6 Design, Impedance Levels, and Matching Networks

Matching and biasing of GaN HEMTs can be based on well-established techniques used for matching and power combining of GaAs devices, e.g., [6.6]. The realization of typical MMIC functions in GaN circuits, such as biasing and RF-matching, is very similar to that for GaAs. MIM capacitor values and resistors are very similar; however, as will be discussed in Chapter 8, the lumped elements have to be matched to the increased voltage and power levels. This also includes the design rules, which have to be matched to increased power levels, increased electric fields, and higher thermal dissipation. RF-stability considerations of MMICs are discussed, e.g., in [6.118, 6.199]. Nyquist plots of the transfer functions can be used to completely characterize stability of an RF-amplifier. This is important as the (in-)stability circles of the GaN HEMTs are very close to the optimum matching loads. For an example of this property, see, e.g., [6.170].

GaN HEMT Circuits: Design Techniques

The intrinsic properties of wide bandgap GaN FETs are promising and have been repeatedly mentioned [6.121]. However, the use of appropriate design techniques is of critical importance to make use of these intrinsic material properties in circuits. Several examples for the extraction of optimum output load impedances of GaN HEMTs have been reported, e.g., [6.195]. For a GaN/AlGaN HFET power cell with a gate periphery of 1 mm on sapphire substrate, an optimum load of 32Ω and a output capacitance $C_{ds} = 0.32 \text{ pF mm}^{-1}$ are mentioned for an operation bias $V_{DS} = 27 \text{ V}$. A more exact analysis of a 1 mm cell in X-band is given in [6.170]. The frequency-dependent distinction is made between the optimum load for output power, gain, and efficiency. The optimum impedance at 10 GHz of a 1.2 mm cell is $R_{opt} = 35 \Omega$ for maximum power and $R_{opt} = 78 \Omega$ for optimum PAE. A more systemized approach based on LS-models was already detailed in Chapter 5. A simple resistive load can be approximated by the Cripps-approach [6.29]:

$$R_{opt} = \frac{V_{DS}}{0.5 \cdot I_{pp}}. \quad (6.5)$$

V_{DS} and I_{pp} are the quiescent operation bias and the maximum drain current-swing (peak-to-peak) values in linear operation. Based on the operation voltage and input power, the modified Cripps-load can be calculated from a set of equations, which includes also the compensation of the output capacitance, as detailed in [6.29]. The load derived from this modified Cripps-approach can be used as a principle approximation for the verification of simulation results obtained by a large-signal model for frequencies up to about 12 GHz [6.170]. Above this frequency, the impact of the layout and associated impedance transformation becomes dominating.

Advanced Circuit Design Techniques

Circuit design of GaN circuits is similar to that of any other material system, such as GaAs. The tasks for device layout and circuit design include:

- Impedance transformation
- Selection of input matching, output matching, and relative bandwidth [6.88]
- Interstage matching
- Harmonic matching [6.25]
- Area reduction

A first pass design strategy for the use in GaAs X-band MMICs is described, e.g., in [6.167]. Such a strategy includes transistor size selection, characterization of the transistors at high power-level conditions, large-signal parameter extraction, broadband matching techniques, and layout; see [6.6]. Power design and power combining techniques have been described, e.g., in [6.6].

Matching techniques for narrowband and broadband designs require detailed analysis with respect to relative bandwidth, PAE, gain, linearity, and output power. Table 6.3 compares several properties (see also [6.6]) and examples of the application of matching techniques for GaN FETs. No amplifier concept or matching technique is found ideal for all applications, especially for broadband. The most profound trade-offs are among bandwidth, efficiency, and linearity, as seen in Table 6.3. The small-signal conjugate matching is widely used for input and output. However, it is not ideal for power matching due to the difference of R_{opt} for linear gain and output power, especially at high power levels due to the impact of harmonics [6.158]. Quarter-wavelength matching-approaches are attractive in general, as transmission-line elements can be easily used to emulate lumped components [6.195], especially for higher frequencies, while they yield additional advantages, such as half-wavelength transparency [6.30]. The decision, whether lumped-RCL elements or transmission-line elements are used, is based on the frequency and area available to place and fold extended transmission-line elements, especially at lower frequencies. Balanced (0–180°) amplifiers are typically used for simple high-bandwidth designs with increased output power, easy and reliable matching, and intrinsic redundancy. Examples for GaN-based PA designs are found in [6.113], for GaN HEMT low-noise designs, see [6.114]. Push–pull configurations can be used to increase efficiencies while maintaining good bandwidth, as performed with GaN HEMTs, e.g., in [6.53, 6.73, 6.100]. Feedback is used in various forms essentially to improve bandwidth at the upper band edge and the linearity of the design. A DC to 5 GHz design is presented based on feedback inductances [6.23].

Harmonic tuning is typically used to increase the efficiency [6.24, 6.25, 6.30]. As shown in Table 6.3 the termination has a limiting effect on the bandwidth unless very specific techniques are used [6.53].

For overall verification of the passive component models for MMIC layout, 3D- or 2.5D-electromagnetic simulations are typically used to verify the combination of the passive and active elements and their models, e.g., [6.148]. This allows a very precise prediction of the transmission-line elements, as reported in [6.33]. This is especially useful for nonlinear transmission-lines [6.105]. Sensitivity analysis towards process variations completes the design strat-

Table 6.3. Reported matching techniques for GaN FETs and different criteria

Matching	PAE	Bandwidth	Linearity	P_{out}	Gain	Ref.
Small-signal	+	0	++	0	++	[6.81]
Balanced	+	+		+	++	[6.113]
Feedback	--	++		0	+	[6.113, 6.114]
Distributed	--	++		+	+	[6.93]
LCR $\lambda/4$ transmission	-		++	+	0	[6.195]
Harmonic tuning	++	-	0	+	+	[6.24, 6.25]
Push–Pull	++	0	+	++	++	[6.53, 6.73]

egy [6.6, 6.89]. The sensitivity analysis is typically based on the variation of a variety of small-signal parameters and the inclusion of their intrinsic correlation into the analysis [6.89]. Newer methodologies for the design and integration approach for MMICs have been suggested, e.g., in [6.102]. The co-integration of MEMS for tunable impedance-matched networks is suggested. An X-band GaN HEMT power amplifier design using an artificial neural network modeling technique for the active GaN HFET is presented in [6.94]. A neural network is trained and used to model S-parameters of the device under specific operation conditions. This technique is considered quick, while the underlying device physics is omitted and no extraction of a model is necessary. The drawback is the lack of direct control of the extracted parameters. Transmitter design techniques have been described, e.g., in [6.88]. It is suggested that node architectures based on solid-state power amplifiers multiply output power while maintaining gain and efficiency. Traveling-wave-tube (TWT) replacement is considered as one application of multichip MMIC solutions [6.4]. It is discussed whether GaN MMICs significantly reduce the number of MMICs needed for this purpose and enable TWT replacement. As an example, pulsed-output power levels of 500 W and even 880 W have been realized with efficiencies of 50% in L-band and S-band [6.100, 6.108], based on GaN HEMT amplifiers. The device concepts employ four dies of devices integrated in one package in a push–pull concept. This example shows that GaN HEMTs simplify the architectures for a given output power.

6.2.7 Broadband GaN Highly Linear Amplifiers

GaN devices are extremely useful for broadband high-power high-efficiency amplification because of their high impedance levels and their high-gain device characteristics. Corresponding GaAs devices typically provide gate widths of up to $W_g = 16$ mm with power levels of 10 W [6.98]. Several GaN-based hybrid and MMIC-broadband amplifiers have been suggested in the literature, e.g., in [6.74, 6.82, 6.87, 6.93, 6.186]. LCR-matched power amplifiers are given in [6.195]. AlGaN/GaN HEMTs on sapphire substrates and flip-chip mounting on AlN passive substrates are used. A four-way Wilkinson combiner structure is used to match flip-chip devices with 4 mm of total gate periphery. The measured output power amounts to 8.5 W at 8 GHz when biased at $V_{DS} = 16$ V. Another amplifier delivers an output power of 35 dBm between 4 and 8 GHz, i.e., for a relative bandwidth of 50%. A cascode delay-matched power amplifier between 2 and 8 GHz is presented in [6.87], which yields 5 W of output power at 6 GHz, 1.35 W at 8 GHz, and a small-signal bandwidth between 1 and 9 GHz. A demonstration of a high-efficiency nonuniform monolithic GaN HEMT distributed amplifier is given in [6.93]. A four-stage dual-cascode concept is used for the gain cells in order to have a high gain-bandwidth product. The chip size is 2.5×1.4 mm². Power levels of ≥ 1 W are achieved between 3 and 12 GHz with a maximum of 3 W at 8 GHz. The maximum PAE is 25% at 3 GHz.

Ku-Frequency Band (14-18 GHz) MMIC Amplifiers

The Ku-frequency band is used for both civil and military applications requiring bandwidth, linearity, and efficiency [6.105]. Multi octave III-N device amplifiers with bandwidths between 2 and 20 GHz and efficiencies $\geq 30\%$ are proposed, see [6.139]. Broadband reference MMICs based on GaAs HFETs are reported, e.g., for the frequency band 6–18 GHz, in [6.7, 6.85, 6.105]. The output power levels amount to ≥ 5 W in saturation and efficiencies beyond 22% with 12 dB of gain. The chip size is 5.8×5.8 mm². A GaN K-band linear amplifier in coplanar transmission-line technology on sapphire substrate is reported in [6.116]. A 3 dB bandwidth of 4.5 GHz is obtained with more than 10 dB gain between 20 and 24.5 GHz. A Ku-band dual-stage MMIC power amplifier with a 6 mm output periphery and a 3 mm wide driver stage yields a pulsed-output power of 24 W at 16 GHz [6.130]. The associated gain is 12.8 dB with a PAE of 22%. The supply voltage is 31 V. A packaged Ku-band MMIC amplifier in microstrip line technology on s.i. SiC is given in [6.150], which demonstrates the very good linearity of these amplifiers. The dual-stage microstrip transmission-line design operates between 9 and 19 GHz with a small-signal gain of 13 dB. The IMD3 is better than -30 dBc up to associated output power levels of 26 dBm. A 6–16 GHz linearized amplifier in microstrip-transmission-line technology on s.i. SiC substrate is described in [6.74] realized in quarter-micron GaN gate technology. A push-pull concept is used for the amplifier. Active FET nonlinear generators are used to achieve an improvement in carrier-over-intermodulation C/I-ratio of 8 dB. The output power level is 10 W. More recently, across the multi octave bandwidth 2–15 GHz, average cw-output power levels and associated PAE of 5.5 W and 25% are obtained [6.48]. Again a nonuniform distributed topology with five transistors is used in microstrip transmission-line technology. Maximum output power levels reach 6.9 W with 32% PAE at 7 GHz. The chip size is 4.45×2.26 mm². Similar results between 4 and 18 GHz are obtained in [6.105] in coplanar technology. However, the output power results are obtained in pulsed-operation with a duty cycle of only 5% with a gate width $W_g = 2$ mm. As another example, Fig. 6.10 gives the chip image of a single-stage broadband linear power amplifier in coplanar technology on s.i. SiC substrate. Five GaN HEMT cascode GaN HEMTs with $l_g = 150$ nm are combined in a traveling-wave structure. Fig. 6.11 gives the measured S-parameters S_{ij} of the MMIC amplifier. The amplifier provides a small-signal gain of ≥ 8 dB between 1 and 20 GHz in a cascode device concept. The gate biases are $V_{GS} = -3.5$ V for the first gate and $V_{GS} = 2$ V for the second gate. This and other recent examples [6.48, 6.105] demonstrate the outstanding gain bandwidth and power capabilities of GaN HFETs for multi octave broadband applications.

6.2.8 GaN Mm-wave Power Amplifiers

GaN HEMTs are also very attractive for mm-wave operation from 30 GHz to at least 100 GHz [6.133] due to the material properties discussed in Chap-

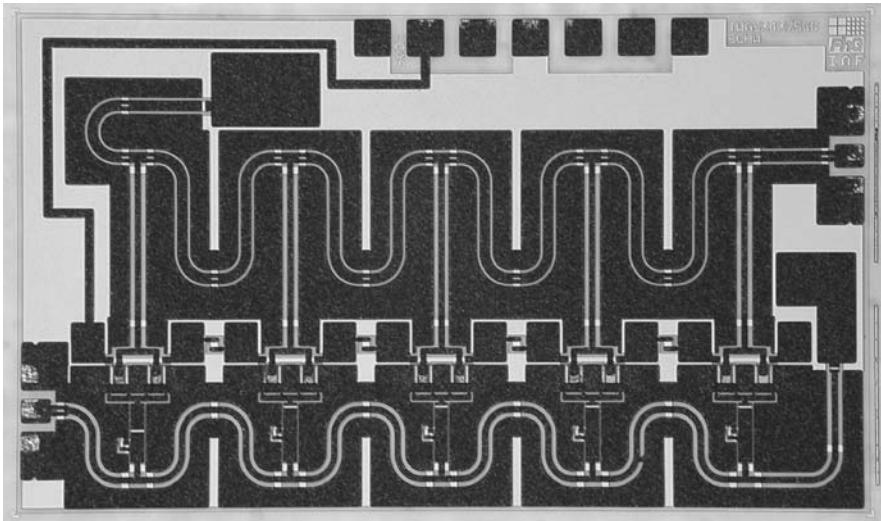


Fig. 6.10. Chip image of a single-stage broadband linear amplifier using cascodes

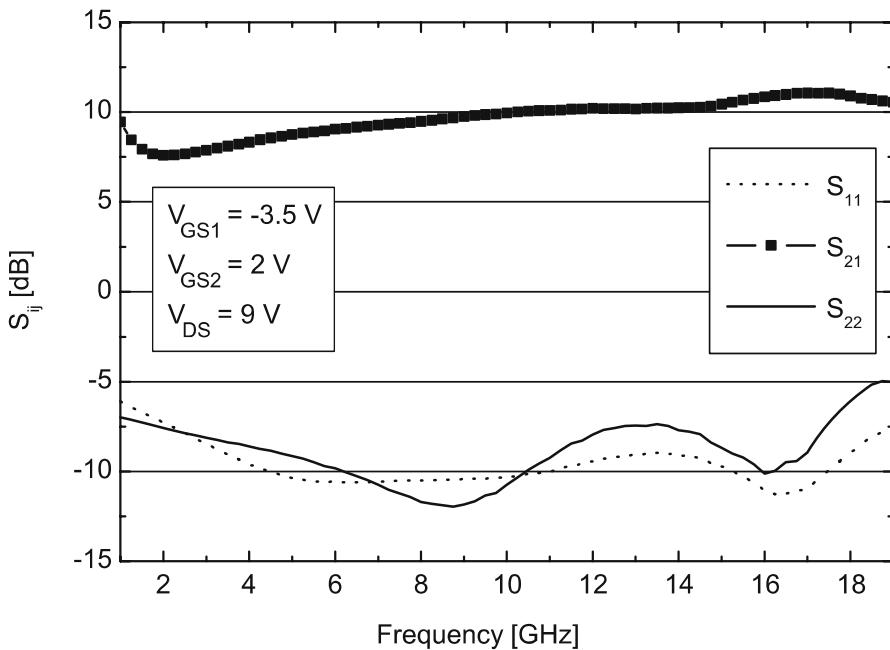


Fig. 6.11. S-parameters of the single-stage cascode amplifier

ter 2. For high frequency operation, e.g., at 30 GHz [6.168], 40 GHz [6.132], or even 80 GHz [6.106], the impedance situation changes dramatically. For a GaN

HEMT with small gate width of 100–300 µm with several hundred Ohms of intrinsic output impedance at 2 GHz, the layout transformation leads to a real output impedance of $\leq 50 \Omega$ with a high inductive contribution, as is shown in Fig. 5.30 in Chapter 5. The complex impedance of a device with $8 \times 60 \mu\text{m}$ gate width at 30 GHz yields $6.6 + i 20.3 \Omega$ [6.168]. Double heterojunction devices are suggested for improved pinch-off of short channel devices [6.106]. The intrinsic impedance is 110Ω . Power gain levels of 7–8 dB per stage are targeted for mm-wave operation [6.140]. Interstage matching at mm-wave frequencies is thus a critical requirement to obtain sufficient power gain to 50Ω impedance [6.168] at mm-wave frequencies. Very different impedance levels from the output of the first amplifier stage to the input of the second stage have to be matched similar to GaAs PHEMTs. The main distinction for the passive mm-wave design for GaN are relaxed design rules for high-power high-voltage operation, which at the same time reduce losses and minimize chip area. On the passive side mm-wave libraries of coplanar transmission-line elements have to be extracted similar to those for GaAs PHEMT, e.g., including the verification with 3D-EM simulation [6.55, 6.168]. Design using microstrip transmission-lines at mm-wave frequencies yields reduced source inductances [6.31], reduced area consumption [6.70], while the passive technology requires a higher amount of EM-simulations [6.70]. The use of microstrip transmission technology helps to suppress higher-order modes within the substrates [6.137] for mm-wave operation.

6.3 Robust GaN Low-Noise Amplifiers

In addition to the outstanding power performance, GaN HEMTs are promising candidates for robust low-noise applications. The low-noise performance of GaN HFETs is currently slightly inferior to that of GaAs PHEMTs, GaAs metamorphic, or InP HEMTs [6.57] for the same gate length [6.60, 6.132]. However, GaN HEMTs provide enormous advantages in terms of linearity [6.123], bandwidth [6.5], and robustness [6.123, 6.142] up to input power levels of $\geq 1 \text{ W}$.

6.3.1 State-of-the-Art of GaN Low-Noise Amplifiers

A number of examples for GaN LNA MMIC and hybrid LNAs are available. On the GaN HFET device level, minimum noise figures $N_{F,\min} = 0.4 \text{ dB}$ at 6 GHz and 0.7 dB at 10 GHz are reported with associated gain levels $G_{\text{ass}} = 14 \text{ dB}$ and 11 dB , respectively [6.60]. Similar noise figures of 0.5 dB in the same frequency range (7–10 GHz) are reached at the full MMIC level using InP HEMT technologies, as reported in [6.57]. A combined low-noise high-power GaN HEMT technology for hybrid circuit approaches is given in [6.131]. Both low-noise operation with 1.7 dB of noise figure and 8.3 dB of associated gain at 8 GHz and power densities of 4.6 W mm^{-1} at $V_{DS} = 25 \text{ V}$

with 40% PAE at 10 GHz are reported. Wideband AlGaN/GaN HEMT low-noise amplifiers for highly survivable receiver electronics are presented in [6.16] using coplanar MMIC technology. A single-stage MMIC device on s.i. SiC substrate yields a noise figure of about 2 dB and a linear gain of 15 dB up to 3 GHz. The devices are subject to RF-stress tests with input power levels of 30 dBm. The output power $P_{-1\text{dB}}$ is ≥ 1 W at 2 GHz. The associated third-order output intercept point (OIP3) is as high as 43 dBm at 2 GHz. C-band GaN HFET LNAs are reported in [6.142] with noise figures of ≤ 2.3 dB between 3 and 7 GHz. The dual-stage MMICs provide an associated gain of 20 dB for the same frequency range. The extrapolated output intercept point (OIP) is 26 dBm at 5 GHz. The devices are subject to input power levels of 36 dBm. A multi octave LNA MMIC from 0.2–8 GHz with ≤ 0.5 dB of noise figure at $V_{\text{DS}} = 12$ V and an output power $P_{-1\text{dB}} = 2$ W is given in [6.83]. The amplifier obtains high linearity with an OIP3 of 43.2–46.5 dBm and $P_{-1\text{dB}}$ of 32.8–33.2 dBm (2 W) between 2 and 6 GHz. The associated PAE at $P_{-1\text{dB}}$ is 28–31%. Further wideband LNAs based on dual-gate GaN technology are presented in [6.5]. A single-stage MMIC delivers 12.5–18 dB of gain and 1.3–2.5 dB noise figure between 1 and 12 GHz. Resistive feedback is used to allow wideband operation. The gate periphery is $W_g = 320 \mu\text{m}$ with a gate length $l_g = 0.2 \mu\text{m}$. The output power of the MMIC is 25 dBm at $V_{\text{DS}} = 10$ V. The device can be driven to a compression level of $P_{-25\text{dB}}$ with a destructive input power level of 38 dBm at 2 GHz. The temperature dependence of a GaN-based HEMT monolithic X-Band LNA between -43°C and 150°C is investigated [6.151]. The LNA noise figure of 3.5 dB at room temperature increases to 5 dB at 150°C . At the same time, the associated gain decreases from 8.5 dB at RT to 5 dB at 150°C and 8 GHz. Investigations of the survivability of AlGaN/GaN HFETs for high-input drive are given in [6.18]. Two catastrophic failure mechanisms are identified. At low drain-source voltages (≤ 10 V), the forward turn-on of the gate diode can exceed the burnout limit, resulting in a sudden failure. Increasing the quiescent V_{DS} increases the peak drain-gate voltage and changes the failure mechanism to gate-drain reverse breakdown.

6.3.2 Examples of GaN MMIC LNAs

Robust GaN HEMT LNA MMICs for X-Band applications have been reported in [6.86]. Some findings in the course of the design and characterization are discussed later.

Single-Stage MMIC Small-Signal and Noise Performance

Fig. 6.12 gives the chip image of the single-stage coplanar design. The chip size is $2 \times 1 \text{ mm}^2$. Fig. 6.13 compares the simulated and measured S-parameters of the amplifier at $V_{\text{DS}} = 7$ V and a drain current $I_D = 150 \text{ mA mm}^{-1}$. The input and output match is better than 10 dB at 10 GHz and a maximum S_{21} of

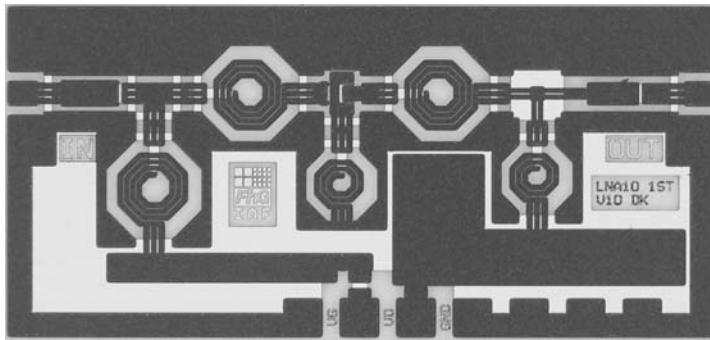


Fig. 6.12. Chip image of a single-stage GaN HEMT low-noise amplifier

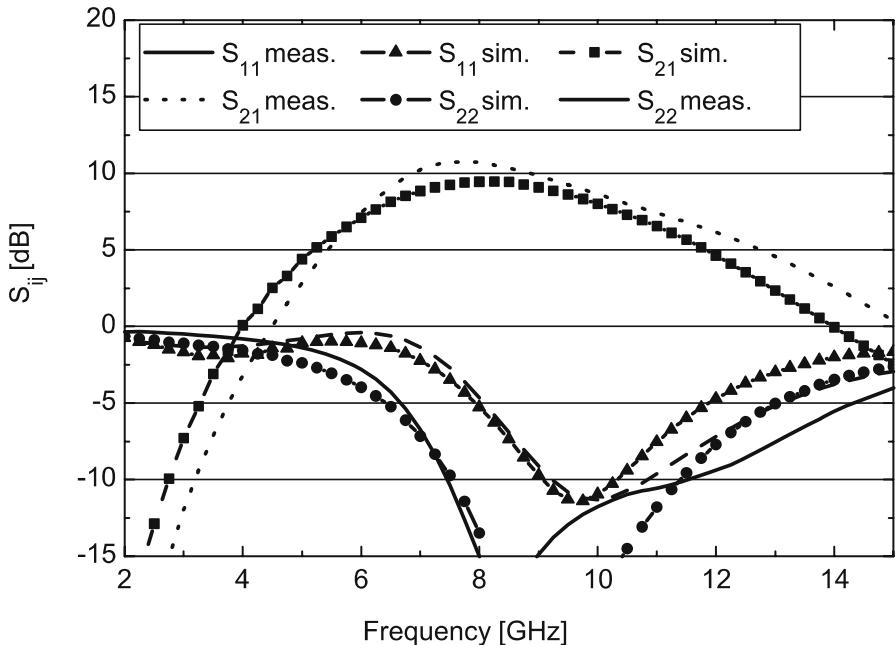


Fig. 6.13. Simulated and measured S-parameters S_{ij} as a function of frequency for a single-stage X-band LNA

10 dB is measured at 8 GHz. Fig. 6.14 provides the measured noise figure N_F of the single-stage design. The measured noise figure at 50Ω is significantly increased relative to the $N_{F,\min}$ of the single FET. This is due to the passive losses in the matching networks.

Small-Signal and Noise Performance of the Dual-Stage MMIC

Multistage MMICs are typical for LNAs, thus Fig. 6.15 compares the simulated and measured S-parameters of a dual-stage amplifier at $V_{DS} = 7$ V for

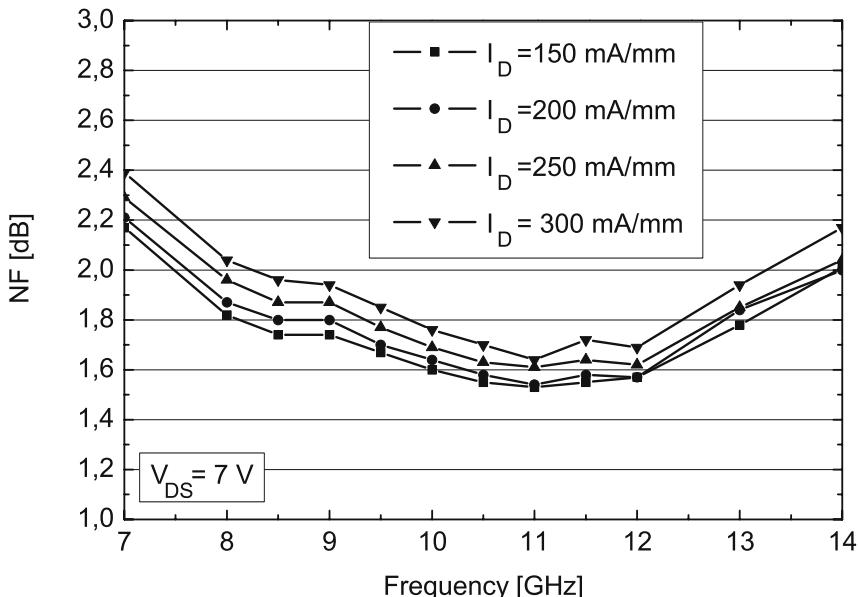


Fig. 6.14. Noise figure N_F of the X-band single-stage LNA as a function of frequency

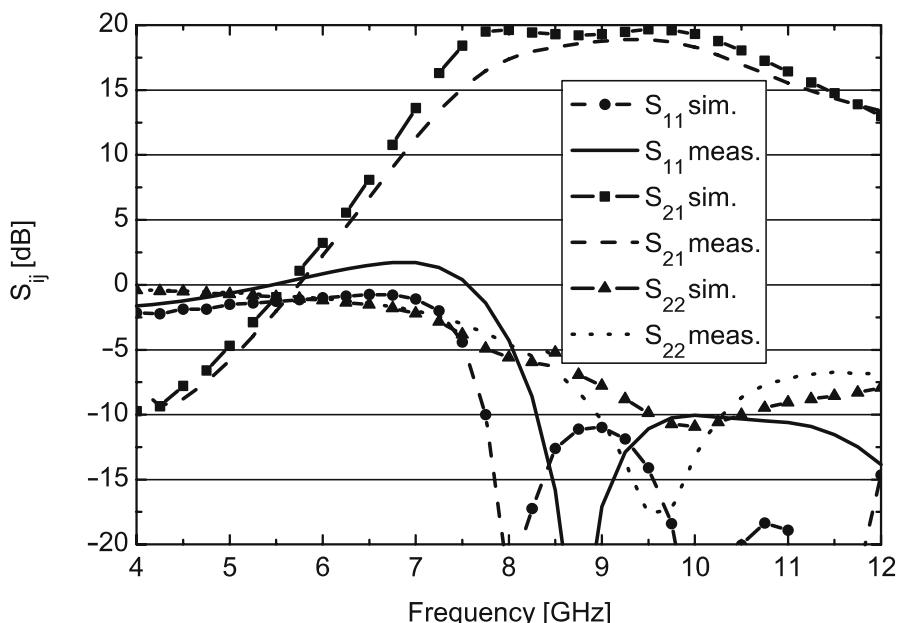


Fig. 6.15. Simulated and measured S-parameters S_{ij} as a function of frequency for the dual-stage X-band LNA

a drain current $I_D = 150 \text{ mA mm}^{-1}$. All drain current levels given are identical for the first and the second amplifier stage. A measured S_{21} of $\geq 18 \text{ dB}$ and a measured input and output match of better than 10 dB are obtained at 10 GHz . The input and output of the devices are matched to the small-signal parameters.

Fig. 6.16 gives the measured noise figure N_F at 10 GHz of the dual stage-design as a function of drain current I_{DS} and operation voltages V_{DS} between 1 and 20 V . The noise figure is nearly constant with V_{DS} while a stronger increase is visible for the increase of the current I_{DS} .

Fig. 6.17 gives the measured noise figure N_F at $V_{DS}=7 \text{ V}$ as a function of frequency for the dual-stage LNA with the drain current as a parameter. A minimum noise figure $N_F = 1.6 \text{ dB}$ is observed for a drain current $I_D = 150 \text{ mA mm}^{-1}$ at 11 GHz . At 10 GHz , the device yields a noise figure of 1.8 dB . The drain current $I_D = 100 \text{ mA mm}^{-1}$ is not considered in Fig. 6.17, as the device did not provide sufficient gain for this bias. Similar operation bias are given in [6.83] for a $2\text{--}8 \text{ GHz}$ MMIC with $V_{DS}=12 \text{ V}/200 \text{ mA}$ for the low power and $V_{DS}=15 \text{ V}/400 \text{ mA}$ for the high-power setting for a 1.2 mm device.

Large-Signal and Intermodulation Measurements

The cw output power measurement of the single-stage LNA for $V_{DS} = 25 \text{ V}$ at 50Ω load at 10 GHz gives a net linear gain of 10 dB , while a maximum cw-PAE of 24% is found. A maximum saturated output power of 26 dBm is measured. The maximum net input power amounts to 23 dBm or 1.66 W mm^{-1} at a compression level of $P_{-7\text{dB}}$. Both the output power and the high-compression level demonstrate the robustness of the GaN LNAs. Intermodulation measurements at both input and output at 10 GHz are given in Fig. 6.18. The output intercept point for two-tone excitation amounts to 27 dBm .

The input intermodulation IIP3-measurement of the single-stage MMIC as a function of V_{GS} - and V_{DS} -bias is given in Fig. 6.19. The V_{GS} -range in Fig. 6.19 covers similar drain current levels, as given in Fig. 6.16. The trade-off between linearity and noise figure can be observed by comparing Fig. 6.19 and Fig. 6.16. Lower noise figures N_F are achieved for reduced operation bias and low currents I_{DS} (Fig. 6.16), whereas the input linearity improves for increased operation bias V_{DS} and for higher current I_{DS} , as shown in Fig. 6.19. Fig. 6.19 clearly shows the combination of high-speed and WBG properties in GaN MMICs, i.e., high-linearity and low-noise figure.

6.4 Oscillators, Mixers, and Attenuators

In addition to their application in amplifiers, the outstanding material properties of III-N devices can be also used for other circuit applications and functions.

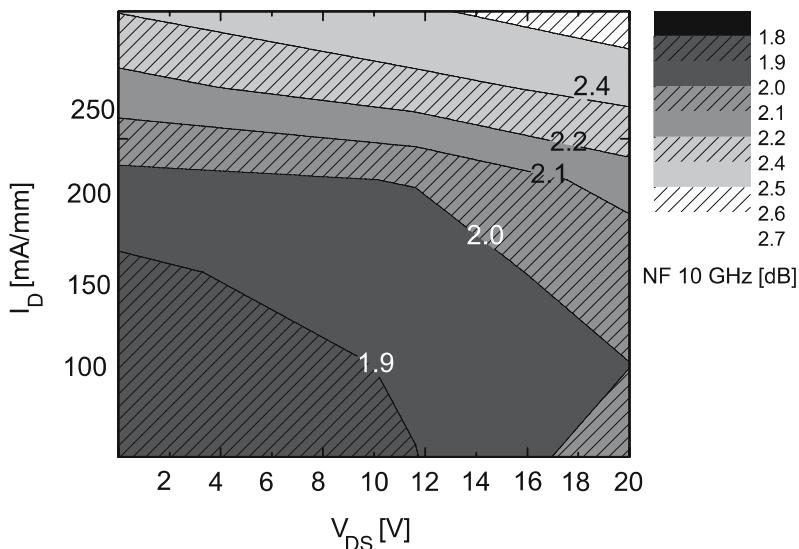


Fig. 6.16. Measured noise figure N_F in dB as a function of I_D and V_{DS} for the dual-stage X-band LNA at 10 GHz

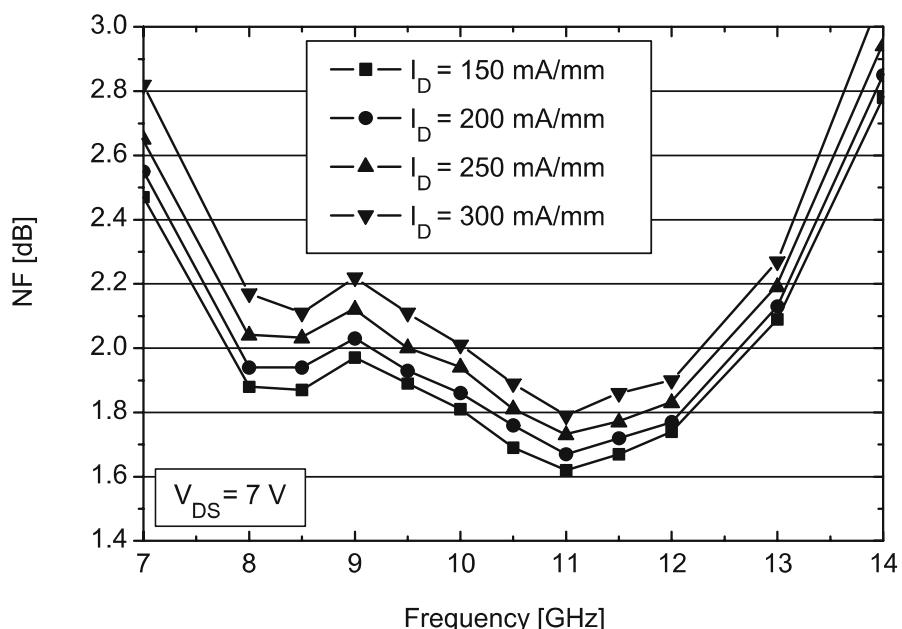


Fig. 6.17. Noise figure N_F of the dual-stage LNA as a function of frequency with the drain current as a parameter

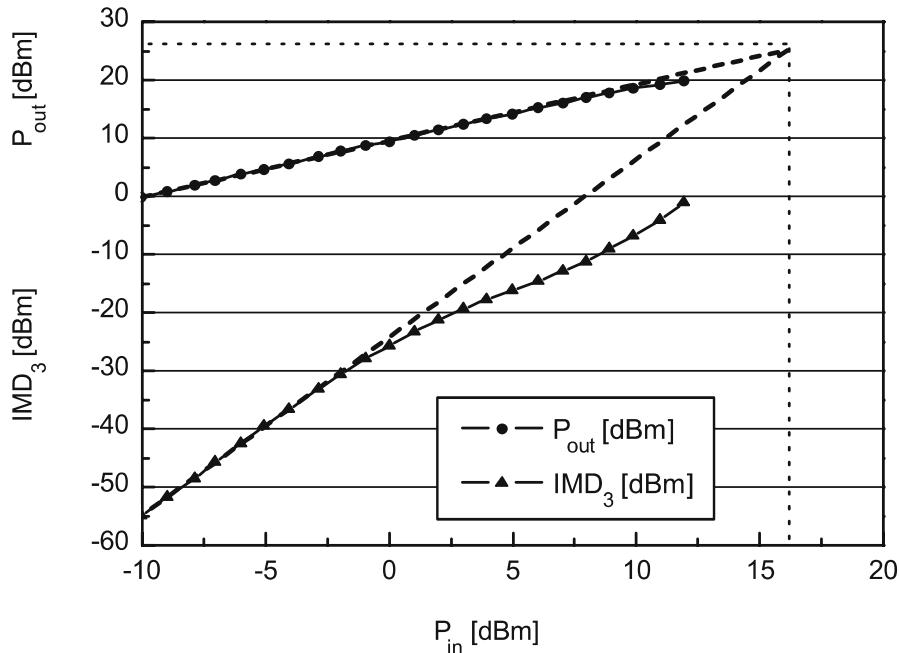


Fig. 6.18. Measured intermodulation distortion IM_3 as a function of input power for the single-stage X-band LNA at 10 GHz

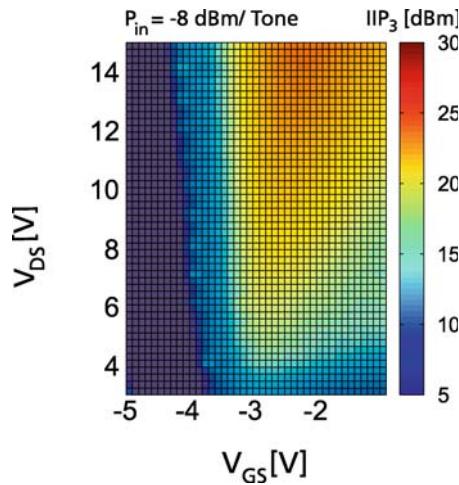


Fig. 6.19. Input intermodulation point IIP₃ as a function of V_{DS} and V_{GS} at 10 GHz

6.4.1 Oscillators

GaN HEMTs are attractive candidates for robust high-power frequency sources, such as voltage controlled oscillators (VCOs), for applications in harsh environments, e.g., [6.50]. The high output-power densities allow MMIC design without the use of an additional output buffer amplifiers, e.g., in [6.72]. An example of a VCO with an output power of 35 dBm between 8.5 and 9.5 GHz is given in [6.72]. Output power densities of 2.1 W mm^{-1} are reached at $V_{DS} = 30 \text{ V}$. The technology uses GaN HEMTs with a gate length $l_g = 150 \text{ nm}$. A common-gate architecture is used as it maximizes device instability. The phase noise is estimated from the spectrum analyzer signal only, which is a critical procedure and thus shall not be detailed here. High-power single-ended Colpitts-type GaN oscillators using field-plated HEMTs are described in [6.194]. Both output power and operation bias can be significantly increased to 1.9 W and $V_{DS} = 40 \text{ V}$ with an output power density of 3.8 W mm^{-1} at 5 GHz. The DC-to-RF-conversion efficiency amounts to 21%, while the measured phase noise at 1 MHz offset from the carrier amounts to -132 dBc . A GaN HFET with $W_g = 4 \times 125 \mu\text{m}$ is used. Similar low-phase noise AlGaN/GaN HEMT oscillators integrated with $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ thin films are given in [6.193]. The high-k material $\text{Ba}_x\text{Sr}_{1-x}\text{TiO}_3$ is integrated for high-Q capacitances at the source and drain side of the devices. Phase-noise levels of -105 dBc at 100 kHz offset from the carrier with output power levels of 20 dBm are given. The DC- to RF-conversion efficiency is 12%. At higher frequencies of 39 GHz, a Q-band oscillator MMIC is presented in [6.90]. An output power of 25 dBm at $V_{DS} = 25 \text{ V}$ is reported at a record low-phase noise level of -120 dBc at 1 MHz offset from the carrier; however, the phase-noise measurement is again performed with a spectrum analyzer, which is very sensitive to locking. Differential GaN oscillators are reported in [6.143]. At an output power level of 23 dBm and 4.16 GHz a second-harmonic-suppression of -45 dB and a third-harmonic-suppression of -70 dB are reached. Initial results for ring oscillators in GaN digital circuits are given in [6.61]. The devices can be operated up to base plate temperatures of 265°C , which shows the suitability for operation of GaN VCOs in harsh environments.

6.4.2 GaN HEMT Mixer Circuits

Any communication system also requires the function of a mixer for frequency upconversion and downconversion. FET mixers are very attractive, as they can be used in active and passive mode, e.g., [6.8]. This allows a choice between conversion gain and conversion loss. The conversion gain is typically traded for the linearity of the mixer. GaN HEMT mixers are more advantageous than GaAs FET mixers, as they promise a higher dynamic range and better mixer linearity [6.2]. GaN high-power mixers with high-conversion gain are attractive candidates for communication systems because they enable the desired output power using a power amplifier with a small number of stages. Resistive mixer concepts using GaN HFETs have been reported repeatedly, e.g.,

in [6.2, 6.71]. A single-ended X-band mixer is presented with a chip size of $1.6 \times 1.3 \text{ mm}^2$ [6.71]. The GaN HFET has a geometry of $0.15 \mu\text{m} \times 1,000 \mu\text{m}$. For an LO-signal of 10 GHz and an RF-signal of 12.4 GHz, the device has a conversion loss of -17 dB . The third-order input intercept point amounts to 40 dBm . This demonstrates the high-output power and linearity capabilities of GaN HFET mixers. C-band linear resistive GaN HFET mixers are described in [6.2]. A GaN HFET with a $10 \times 50 \mu\text{m}$ periphery and a gate length $l_g = 0.7 \mu\text{m}$ are used. The conversion loss of the GaN mixer is 7.3 dB with an local oscillator frequency (LO) of 250 MHz and an intermediate frequency of 4,925 MHz. The linearity is limited by the LO, which suggests that the robustness of the devices further determines mixer linearity. The third-order input intercept point is as high as 36 dBm . Dual-gate mixers provide the advantage of increased gain per chip area. Dual-gate mixers on s.i. SiC substrates are described in [6.156, 6.157]. A $0.7 \mu\text{m} \times 300 \mu\text{m}$ device geometry is used for the realization of a mixer with a maximum output power of 19.6 dBm . The conversion gain is as high as 11 dB at 2 GHz. At 5 GHz, the conversion gain is 5 dB with an associated output power of 13 dBm . Dual-gate mixers for UWB (ultra-wideband) applications with a 2 GHz bandwidth at 24 GHz based on GaN FET on s.i. SiC substrates are presented in [6.156]. A $0.15 \mu\text{m} \times 200 \mu\text{m}$ GaN HEMT is used. The maximum output power amounts to 8.9 dBm . The LO-signal at 24 GHz is modulated by a 0.4 ns pulse at the second gate. The output power from the mixer is found to be sufficient for direct antenna drive in the desired application. Again linearity, bandwidth, and robustness demonstrate the potential of GaN mixers.

6.4.3 Attenuators and Switches

GaN-HFET-based attenuators promise improved power handling while preserving high frequency operation and a wide dynamic range with good linearity. Broadband attenuators based on AlGaN/GaN HEMTs with high dynamic range are presented in [6.1]. The MMIC consists of four FETs in π -configuration, two connected in series, two in shunt-configuration. The MMIC provides an insertion loss of 4 dB , broadband operation from 0 up to 18 GHz, a high dynamic range of 30 dB , and a power handling capability of 15 W mm^{-1} . A simple optically-defined gate $l_g = 1 \mu\text{m}$ gate length is used. The higher operation bias and breakdown capability lead to switches with very good isolation and better large-signal robustness. Based on these properties, also the electrostatic discharge (ESD) capabilities improves. As an example, a typical isolation for GaAs HFET switches is found to be about 30 dB . A GaN FET switch in single-pole-double throw (SPDT) configuration [6.71] yields an isolation of better than 40 dB from near DC to 3 GHz with an insertion loss of better than 1 dB . The compression power $P_{-1\text{dB}}$ of 1 W is achieved with a $400 \mu\text{m}$ device. The third-order intercept point is 46 dBm and correlates well with the expectations.

6.5 Problems

1. What is the estimated impedance advantage of an X-band power cell of 1 mm using a GaN HFET operated at 48 V relative to one using a GaAs PHEMT operated at 8 V?
2. Discuss the area advantage of a GaN MMIC relative to GaAs PHEMT MMIC for the same output power level of 10 W!
3. Calculate the Cripps-load at 2 GHz for an operation voltage of 50 V and 100 V for an output power of 5 W with an $I_{D\max}$ of 700 mA mm^{-1} .
4. Make a guess for the realization of a 100 W power amplifier at 4 GHz with respect to the power cell size. What are your constraints?
5. Which properties make GaN FETs suitable for advanced amplifier concepts?
6. Which device properties make GaN attractive for use in mixers?
7. Do you expect MMICs based on GaN HFETs to provide significantly better phase noise than GaAs PHEMTs? Give arguments!

Reliability Aspects and High-Temperature Operation

In this chapter, III-N-device-specific reliability issues and device failure mechanisms are discussed and analyzed systematically.

7.1 An Overview of Device Testing and of Failure Mechanisms

With the rapid innovation circles of the semiconductor industry, e.g., according to Moore's law [7.92], typical innovation times of 18 months have been maintained for decades now. This fact requires the application of accelerated testing procedures. Typically, extrapolated lifetimes of an electronic device amount to $\geq 10^6$ hours or 114 years at junction temperatures of 125°C.

7.1.1 Description of Device Degradation

The degradation of active electronic devices during operation is typically characterized by two modes. In the first mode, a gradual or parametrical change [7.132] occurs as a function of time of important figures-of-merit, such as drain and gate current I_D and I_G , transconductance g_m , current amplification β , or output power. A second mode is catastrophic failure or sudden total burnout. The latter is included in this testing procedure, as a total failure will also trigger the degradation criterion of choice. Several other application-specific temperature and degradation specifications exist, e.g., for base station applications [7.121] and further communication-, military- [7.107], and satellite-applications [7.6]. Accelerated testing procedures are required in order to timely ensure extrapolated lifetimes of ≥ 20 years at realistic temperatures of operation. Thus, in order to investigate the devices in realistic times scales, temperature accelerated testing is performed at elevated junction temperatures up to 300°C in the GaAs world for both HBT and (H)FETs, e.g., [7.82]. Typical assumptions of this procedure include degradation pro-

cesses that are influenced by mechanisms such as diffusion of metal at the contacts, trap processes, or other processes that yield one-defined activation energy. The degradation is thus accumulated in one quantity. The activation energy is extracted according to

$$E_a = \frac{k}{\log_{10}(e)} \cdot \frac{d \log_{10}(MTTF)}{d(1/T)}. \quad (7.1)$$

From the gradual change of the FOMs, activation energies and median times to failure (MTTFs) can be extracted at a given temperature. The extraction is illustrated in Fig. 7.1. The testing is performed independently for various junction temperatures and the lifetimes extracted are plotted vs. temperature. From the qualified extrapolation, lifetimes can be derived for lower operation temperatures. This extraction procedure needs to be verified, as some degradation mechanisms do not obey accelerated degradation schemes, see, e.g., [7.72]. Other mechanisms are specific to low temperatures [7.86]. Further, some degradation mechanisms may be hidden in the high-temperature acceleration, such as, e.g., low-energy traps, see [7.57]. The criteria for failure applied to the particular data are typically a degradation of the drain current I_D of -5 or -10% [7.121], transconductance, β [7.2], or an output power degradation of ≤ 1 dB [7.79, 7.121], typically even 0.2 dB. From a system point-of-view, even this measure is relatively high, as some system specifications only allow a component degradation of a few percent for the same temperature.

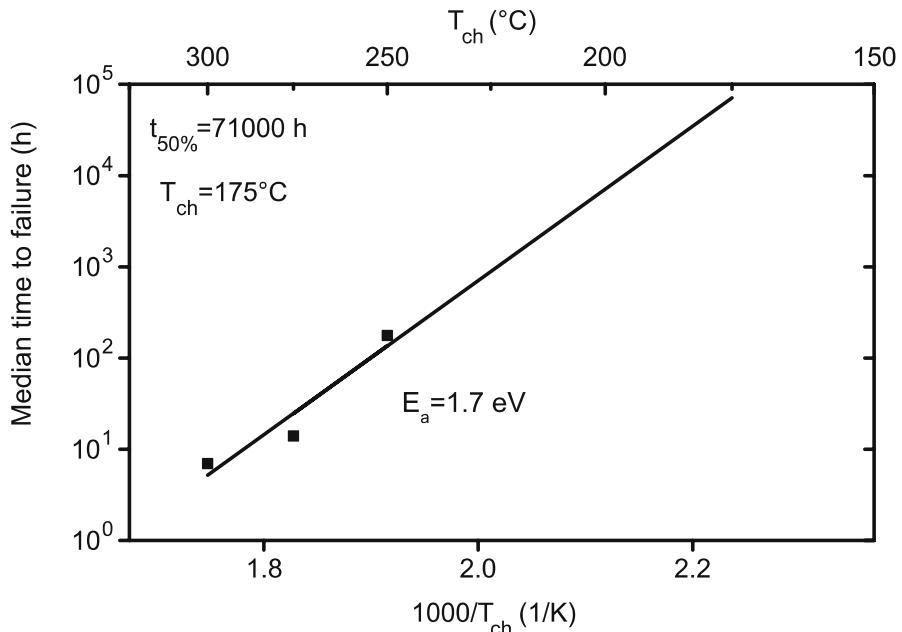


Fig. 7.1. Extraction of the MTTF and activation energy of a GaN HFET [7.33]

The *MTTF* at a given temperature T_L is calculated from the *MTTF* at an elevated junction temperature T [7.110]:

$$MTTF(T_L) = MTTF(T) \cdot \exp\left(\frac{E_a}{k} \cdot \left(\frac{1}{T_L} - \frac{1}{T}\right)\right). \quad (7.2)$$

Fig. 7.1 shows the extraction of the *MTTF* and of the activation energy E_a . Some extraction procedures distinguish between more than one degradation mechanism, e.g., [7.25]. The bandgap energy of the main layers in the semiconductor device is an initial relative measure for interpreting the global quantity activation energy E_a . For GaN with a bandgap energy of 3.4 eV, activation energies of 1.7 eV [7.121] to 1.9 eV [7.102] have been reported. Very low activation energies of GaN devices, such as 0.38 eV, have initially been reported [7.47], which were too low to be of use. In general, based on the higher bandgap of the semiconductors similar or even improved reliability is eventually expected for GaN and other wide bandgap devices as compared to Si [7.137] and to GaAs [7.146] devices. However, this argument of the increase of the bandgap leading to better reliability has to be taken with a grain of salt, as even small bandgap devices, such as InP HEMTs with high In-content in the channel, yield activation energies beyond 1 eV and thus beyond the bandgap energy of the channel, as compiled and stated in [7.23]. Thus, the wide bandgap is beneficial, if

- The main degradation mechanism is related to the absolute bandgap(s)
- The same status of overall process development is achieved
- No additional low-energy mechanism prevail for III-N semiconductors, such as carrier-(de-)trapping or polarization effects

None of these conditions is fully secured for III-N devices. The development of III-N devices for reliability thus focusses on improved dielectrics and interfaces, better contacts (see Chapter 4), and trap-reduced semiconductor materials [7.91], see (Chapter 3). Similarly, a reduced sensitivity of III-N semiconductors toward bandgap-related degradation mechanisms, e.g., radiation damage [7.4] or electrostatic discharge (ESD) [7.121], is expected and also found to be reduced for bulk materials. However, III-N devices strongly rely on interfaces and heteroepitaxy, so that the semiconductor bulk property wide bandgap cannot be fully exploited for the reliability of the devices toward ESD and radiation.

Another way to express reliability is with the help of FIT rates [7.129]. They express the number of failures for an operation time of 10^9 h according to [7.59]

$$1 \text{ FIT} = 1 \text{ failure}/1 \times 10^9 \text{ device hours}. \quad (7.3)$$

Both *MTTF* and FIT rates are naturally related. Some applications may require a different FOM, such as the *MTBF*, the median-time-before-failure [7.57]. The *MTBF* is based on the idea that even the first failure can fully destroy system performance. The extraction of the *MTBF* requires a higher

statistical effort than the extraction of the *MTTF* [7.59] and is thus reported less often.

Device Failure Statistics

Device failure is a statistical process. This process is typically described by a number of statistical functions dependent on the failure mechanism [7.93]. The actual regression and the fitting error distinguishes between different functions, such as the log-normal, the normal function, and the Weibull regression function [7.44]. The log-normal distribution can typically be fitted to the failure distribution of semiconductor devices. The density probability function with the parameters μ and σ reads [7.64] for the log-normal distribution function

$$f(t, \mu, \sigma)_{\text{lognorm}} = \frac{1}{t\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{1}{2} \cdot \left(\frac{\ln(t) - \mu}{\sigma}\right)^2\right), \quad (7.4)$$

while it reads for the normal function

$$f(t, \mu, \sigma)_{\text{norm}} = \frac{1}{\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{(t - \mu)^2}{2\sigma^2}\right). \quad (7.5)$$

The reproducibility of lifetime-test results is a key requirement for the system insertion of electronic devices. This is achieved through the parallel testing of nominally identical devices. The generation of accumulated device hours in excess of 10^5 h is a key requirement [7.44, 7.121] for the verification of the standard deviation of the results achieved. Multiple failure modes have also been analyzed and separated statistically [7.25]. Such a procedure allows the separation of effects and concentration on the most important failure modes, while control of the less demanding failure mode is maintained. In this procedure the device is operated under elevated temperature conditions to analyze early degradation, which is typical of the initial stages of GaN process development [7.108]. The distribution functions f_1 and f_2 of the two failure modes are composed as

$$f = (1 - x) \cdot f_1 + x \cdot f_2. \quad (7.6)$$

Such a procedure can thus be used to separate the infant mortality of devices by burn-in procedures [7.44]. The actual mechanisms of the degradation will now be discussed in the following sections.

7.1.2 Degradation Mechanisms in III-N FETs

III-V HFET degradation is a well-investigated topic [7.24, 7.38, 7.70]. The effects of degradation of GaAs-based (P)HEMTs and of HEMTs based on the InAlAs/InGaAs material system [7.32] are well-known and discussed systematically in the literature. Overview articles can be found, e.g., in [7.38].

Device-performance degradation in general can be classified into two groups, one of which is reversible, including, e.g., simple thermal heating. Most important, however, are nonreversible effects, modifying or destroying device performance irreversibly for the remaining lifetime of the device. Some of these mechanisms are partially reversible, e.g., they can be recovered by light illumination or thermal heating. However, the problems resulting from this behavior make the device quasi-nonreversible for the application. The effects of HFET degradation typically include:

- The shift of the threshold voltage V_{thr} [7.32] and associated thermal runaway [7.1]
- Decrease of maximum drain current I_{Dsat} [7.121]
- Reduction of the DC- and RF-transconductance $g_{\text{m,max}}$ [7.23, 7.24] and similarly of all RF-gain parameters [7.38]
- Increase of the knee voltage under cw- or pulsed-DC-operation [7.29, 7.77, 7.88, 7.91]
- Change of the ideality factor and barrier height of the Schottky contacts [7.24]
- Change, i.e., mostly, but not always, increase of the gate currents and thus reduction of the breakdown voltage [7.22, 7.24, 7.133]

Physically, several nonreversible effects occur during device operation with an impact on reliability. The following effects are discussed for the bulk semiconductor or dielectrics:

- Occupation of traps in the semiconductor caused, e.g., by lattice mismatch of semiconductors and substrates [7.43] such as:
 - Buffer layer trap charging and detrapping [7.51, 7.97]
 - The propagation of substrate-related misfits and other dislocations from the nucleation layer to the surface [7.24]
 - Active semiconductor degradation by hot electrons [7.11, 7.40, 7.87, 7.123] and impact ionization [7.86]
- Relaxation of the material strain [7.61, 7.111]
- Thermal instability of the semiconductor at $\geq 600^\circ\text{C}$ [7.31, 7.36]

At the device contacts the following effects occur:

- Gate contact degradation through:
 - Metal diffusion [7.143]
 - Gate sinking-induced degradation [7.24]
- Spiking of ohmic metals [7.24, 7.42]
- Ohmic contact degradation by:
 - Metal diffusion [7.19, 7.38]
 - Alloy creation [7.8] during operation

Transmission electron microscopy (TEM) cross-section images reveal no significant metal interdiffusion effects at gate and ohmic contacts in AlGaN/GaN HEMTs on s.i. SiC in [7.24]. In general the high annealing temperatures for

III-N devices lead to undefined metal–semiconductor interfaces, as reported in [7.42]. This effect is a reliability concern. Further, the high-annealing temperatures at or beyond the Debye temperatures of III-N semiconductors lead to structural modifications of the semiconductor layers. Most important we find the following degradation effects at the noncontacted or ungated surfaces and interfaces:

- Surface corrosion effects as proposed for GaAs PHEMTs in [7.41, 7.55, 7.138]
- Trap generation and occupation at the interface [7.40, 7.123]
- Degradation of passivation or of the dielectric due to trap charging and detrapping [7.89, 7.102]
- Surface breakdown [7.127]; and related degradation of isolation at mesa and implanted surfaces [7.85]

Further, environmental effects due to ambient gases and fluids have been investigated and include:

- Surface modification by fluorine [7.128] and hydrogen [7.9, 7.21, 7.90]
- Gas absorption at the polar surfaces [7.132]
- Donor or acceptor passivation of dopants by fluorine [7.128]

Further influences arise from radiation damage of various kinds

- Radiation-induced trap creation leading, however, to comparatively small changes in the device DC- and RF-characteristics [7.4].
- Semiconductor material degradation effects for γ -irradiation, while the metal–semiconductor interfaces, such as the Schottky diodes, degrade significantly [7.134].

For III-N devices additional degradation effects have to be considered:

- Change of mechanical stress from the on-wafer bowing of the semiconductor layers relative to the diced, MMIC, or packaging situation [7.62]. This includes:
 - Mechanical effects during the dicing process
 - Influence of the backside process on the frontside performance, e.g., during wafer thinning
- Change of the mechanical stress during die-attach

These effects have a strong impact on the final system application, as any device needs to be diced and mounted.

7.1.3 III-V HBT Device Degradation

III-V HBT reliability has been investigated in a large number of publications for GaAs-HBTs [7.2, 7.14, 7.75, 7.82] and InP-HBTs [7.103]. The most pronounced doping, interface, and contact issues have been solved [7.39] to make the GaAs HBT the most produced III-V electronic RF-device [7.46, 7.48]. The

reliability of GaN-based HBTs is not well-investigated, due to the lack of devices with sufficient gain and overall performance. High-temperature operation of GaN HBTs at 400°C is investigated in a number of publications, e.g., [7.65, 7.147], as high-temperature operation increases the current gain in the existing devices. For III-N HBTs, a similar enumeration holds for the degradation effects in the overall device performance based on GaAs-HBT degradation [7.82]:

- Increase of the base-collector leakage [7.144]
- Instability of the p-doping and its activation in the base layers for npn-devices
- Contact issues due to the p-doping issues at the ohmic contacts

Physically, for III-N devices additional III-N-specific degradation mechanisms are to be expected especially due to the immaturity of the III-N bipolar approach:

- Ohmic contact degradation due to the nonideal ohmic properties for the p-contacts [7.147]
- A modified leakage path due to etch damage [7.144]

At the surfaces and interfaces the following effects are expected based on the remaining device issues:

- Device-passivation degradation
- Degradation of isolation at mesa surfaces [7.144]

With the development of (In)GaN HBTs with better performance, some of these issues will be resolved [7.65], also because of the rapid progress in the GaN HEMT [7.121] and III-N optoelectronic world [7.94].

7.2 Analysis of Nitride-Specific Degradation Mechanisms

Given the large number of publications on III-N electronic devices reviewed in Chapter 2, relatively little reliable and fully consistent data are available for the reliability of GaN devices. This is especially true with respect to increased operation voltages and to the new characteristics such as piezoelectric and spontaneous polarization effects. The few exceptions include the institutions involved in the base station market and military-oriented development, e.g., [7.119, 7.120]. Early reliability data of Cree is discussed in [7.108]. As a general finding, the reproducibility of the results is found insufficient in the early stages of development. Such results have been improved and the progress has continuously been reported, e.g., in [7.102]. This leads to the availability of initial GaN HEMT products [7.115, 7.141]. RFMD reported advances in reliability data in [7.17, 7.114] for their applications for the base station market. A significant stabilization of the device degradation results is found. The consistent evaluation of device reliability of GaN HEMTs by

Nitronex in [7.105, 7.119, 7.121] gives rise to the assumption, that the reliability issues of GaN HFETs can eventually be fully solved. This work is exclusively performed on silicon substrate. Some reliability data devoted to military applications with gate lengths $l_g = 250\text{ nm}$ is given in [7.24]. Focussed ion-beam (FIB) images and SEM investigation show no contact issues after testing. The work specifically stresses the impact of the epitaxial layer structure on the device degradation. For higher frequencies, RF-degradation of small-gate-length GaN devices is discussed, e.g., in [7.13]. As a main finding for the reliability, the current degradation under DC-operation can be correlated with the RF-current degradation under RF-swing. Both current reductions in I_{DS} are found to be similar. In a series of publications [7.43, 7.77, 7.79], researchers at Triquint achieve a number of significant testing results. Effects of the AlGaN/GaN HEMT structure on RF-reliability are discussed in [7.79]. Three issues are stressed: first, the thickness of the AlGaN barrier layer; and second, the application of a GaN cap layer; and, third, the positive impact of a field plate on reliability.

7.2.1 DC-Degradation

DC-degradation experiments at elevated temperatures are the most natural testing routines of the device. Early reliability evaluation of AlGaN/GaN HEMTs grown on s.i. SiC substrate is given, e.g., in [7.78]. The findings include

- Reduction of the transconductance g_m
- Reduction of drain current I_{DSS}
- Change of the Schottky barrier height
- Increase of the on-resistance R_{on}

Electrical bias stress-related degradation of AlGaN/GaN HEMTs is reported in [7.71]. Typical findings for the device after DC-aging include:

- An increase of surface charge and increased transient behavior of the drain current verified by direct surface potential measurements
- A reduction of output power performance after stress [7.78]

The distinction between different stress-bias situations is further very important. Fig. 7.2 gives various bias conditions for testing. High-current I_{DSS} testing, low-current I_{Dq} testing in Class-A/B, and hot pinch-off testing at very high operation bias are typically compared. Pinch-off testing is compared to Class-A biasing, e.g., in [7.123]. In this case, Class-A biasing, or on-state operation of a AlGaN/GaN HFETs with a gate length $l_g = 0.25$ and $0.15\mu\text{m}$ at $V_{DS} = 25\text{ V}$, $P_{DC} = 6\text{ W mm}^{-1}$, is found to result in stronger device degradation than off-state stress at $V_{DS} = 46\text{ V}$ and V_{GS} for pinch-off. Other publications, such as [7.67, 7.88], stress the importance of the off-state testing and Class-B or deep Class-A/B, see Fig. 7.2. A sudden degradation of leakage currents within the first hours of operation is found in [7.67]. Pinch-off testing is performed at a channel temperature $T_{chan} = 150^\circ\text{C}$ for a bias $V_{DS} = 40\text{ V}$.

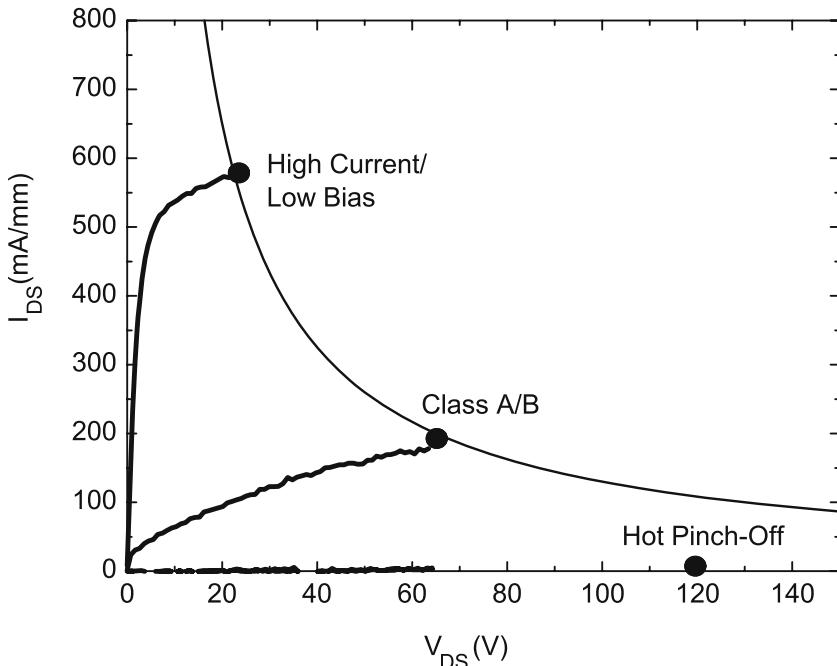


Fig. 7.2. Output characteristics of a GaN HFET with quiescent conditions for aging

and $I_{DQ} = 1.4\%$ of I_{Dmax} and devices with a gate length $l_g = 0.8 \mu\text{m}$. The high-current test is typically found to be less critical, see [7.88]. All these findings are typical, though they do not always necessarily occur in parallel. Step-testing procedures can be applied increasing both bias and temperature with time. Degradation of AlGaN/GaN HEMTs on s.i. SiC under elevated-temperature step-lifetime-testing is further described in [7.24]. The testing starts at a channel temperature $T_{chan} = 150^\circ\text{C}$ with a 15 K step size. The aging is performed for 48 h at each temperature up to 240°C . A strong degradation of the GaN/AlGaN HEMTs is initiated at 195°C . The actual degradation mechanism has not been fully isolated, however, the importance of the material quality on the propagation of the defects from the substrate is stressed. Short-time testing of AlGaN/GaN HEMTs on silicon is also described in [7.7]; however, even under such bias conditions, the devices do not show stable operation, contrary to the good reliability of GaN HEMTs on silicon in [7.121].

Testing Results

As a typical example of an early DC-testing result of an AlGaN/GaN HFET with $W_g = 50 \mu\text{m}$, Fig. 7.3 gives the development of the DC-power density as a function of operation time at $V_{DS} = 20 \text{ V}$ at a backside temperature of 125°C . A degradation of the DC-power is visible, due to the reduction of the current I_{DS} for a given bias $V_{DS}-V_{GS}$ combination. The testing shows

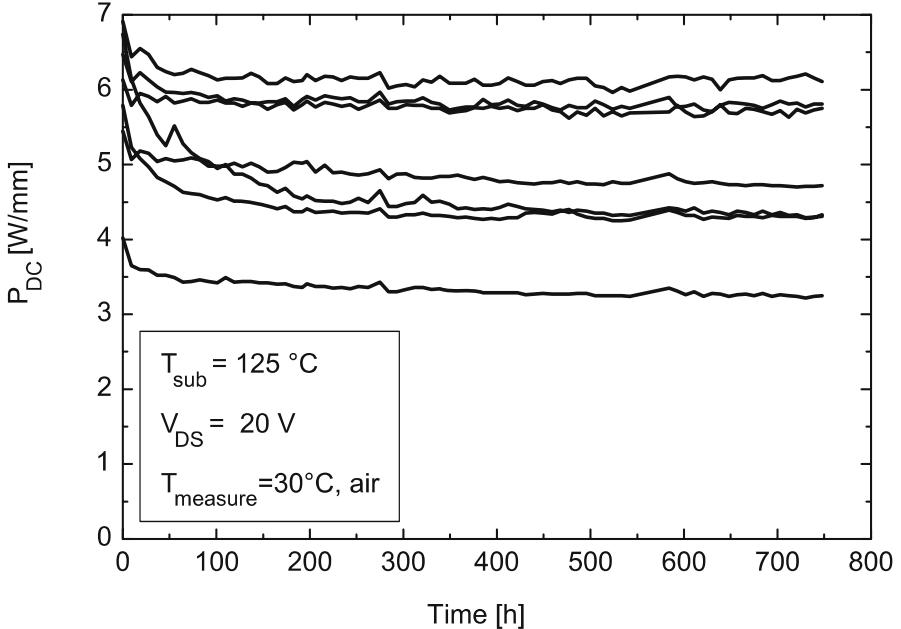


Fig. 7.3. DC-power as a function of time elapsed for GaN HEMTs with $l_g = 300\text{ nm}$ and a gate periphery $W_g = 50\text{ }\mu\text{m}$ [7.33]

a degradation in the first hours of the testing, which spreads the statistical device performance overtime. The device is cycled to room temperature for the DC-measurements. The reduction of the DC-current during aging of AlGaN/GaN HFETs is very similar to the degradation of advanced silicon MOSFETs, e.g., [7.20, 7.98]. This is especially true for the impact of electric fields to the dielectric interface. This can be modeled as an exponential function [7.28, 7.98]:

$$\frac{I(t)}{I_0} = b \cdot t^{-n}. \quad (7.7)$$

A similar expression is derived for the output power degradation in [7.28]:

$$\Delta P_{out} = \frac{I(t)}{I_0} = (1 - b \cdot t^n)^2. \quad (7.8)$$

The data in [7.28] can be correlated to a negative bias temperature instability (NBTI) due to hot carrier injection (HCI), which is very similar to the degradation of Si MOSFETs. This description makes the degradation more predictable. The degradation mechanism in silicon MOSFETs is trap-assisted tunneling through the MOS interface. A similar mechanism at the $\text{SiN}/(\text{Al})\text{GaN}$ interface changes the performance for the GaN HFETs by dynamic trap occupation. The mitigation in [7.98] is performed by changes in the AlGaN/GaN process. To separate device yield from the actual degrada-

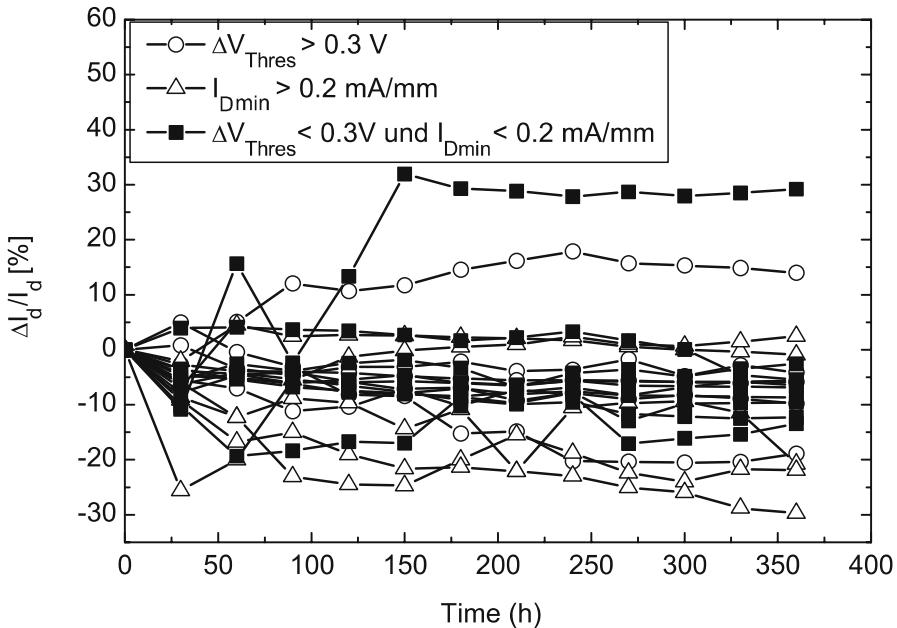


Fig. 7.4. Drain current I_D as a function of time elapsed for GaN HEMTs with $W_g = 50 \mu\text{m}$ and $l_g = 300 \text{ nm}$ [7.33]

tion, Fig. 7.4 gives a typical degradation of the drain current at an elevated substrate temperature in an experiment similar to the one in Fig. 7.3 for a statistical selection of devices. In this set of devices, different modes of behavior are visible. Most of them, however, show a reduction of the drain current and respective power density as a function of time. The devices are sorted according to the derivation from the mean threshold value ΔV_{thr} and the initial value of $I_{D\text{min}}$ prior to aging. For devices, which fulfill the moderate criteria given in the inset, the degradation is more homogenous. Devices with an initially high $I_{D\text{min}}$ degrade stronger than the devices with low $I_{D\text{min}}$. The electrical background of the current degradation mode in Fig. 7.3 and Fig. 7.4 can be manifold:

- The aging translates into a positive shift of the device threshold voltage V_{thr} .
- This current degradation can be caused by an increase of the access resistances R_S and R_D .
- This behavior can be accompanied by a reduction of the transconductance g_m and the maximum current I_{Dsat} .

The most likely explanation in this case is a modification of the critical AlGaN/GaN and AlGaN/SiN interfaces due to carrier (de-)trapping, see [7.63]. This is confirmed by pulsed-DC-measurements prior to and after degradation, which suggest an increase of both the gate- and drain-lag. The latter

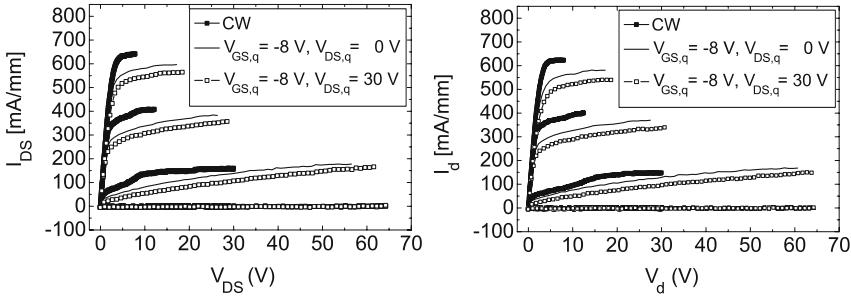


Fig. 7.5. Pulsed-testing of drain prior to (*left*) and after (*right*) aging at $V_{DS} = 120$ V

finding also involves the buffer area of the device, as the drain-lag measurement (see (5.46)) can be influenced by both surface and buffer. As an example, Fig. 7.5 gives the pulsed-drain-lag measurement before and after testing the device at $V_{DS} = 120$ V and pinch-off. The pulse width is 1 μ s at a duty cycle of 0.1%. The cw-measurements are given for reference. Small changes of the output characteristics can be observed despite the high-bias testing. The aging thus leads to changes in the RF-effective IV-characteristics and can be correlated with the output power degradation in some cases, e.g., [7.77]. However, the time constants of the traps created or modified also have to be considered, as traps in III-N semiconductor are sometimes faster than the repetition rate and pulse width of the DC-pulse-testing.

7.2.2 RF-Degradation

RF-degradation testing is an advanced technique to analyze devices under real-operating conditions, typically high-power compression [7.60]. Failure modes in addition to those found during DC-testing can be analyzed, such as forward gate stress and dynamic (de-)trapping. Typical procedures to analyze the shift of the on-currents I_{DSS} and I_{Dq} as a function of time [7.12] while a certain power operation mode is maintained. The power, gain, and PAE changes are monitored in addition. This testing procedure, known from the silicon LDMOS world [7.16], has been applied to GaN HFETs, e.g., at $V_{DS} = 60$ V operation in [7.69]. The I_{Dq} degradation is the most critical failure mode for silicon LDMOS FET operation [7.16] and thus also considered for lifetime evaluation of GaN HFETs for the same application.

Several other testing procedures are available, e.g., [7.113]. For frequencies higher than 2 GHz, RF-reliability of AlGaN/GaN HEMTs grown by MBE on Si substrate is reported in [7.43]. Devices with a gate length $l_g = 300$ nm with a gate field plate are tested at 10 GHz at operation voltages $V_{DS} = 20\text{--}40$ V and $I_{DS} = 200$ mA mm $^{-1}$, i.e., in Class-A/B. The output power of the 4×50 μ m GaN HEMT of 6.2 W mm $^{-1}$ at room temperature does not change after an initial small degradation at $V_{DS} = 40$ V. In a similar experiment the

effects of RF-stress on power characteristics and DC-pulsed-IV characteristics of AlGaN/GaN HEMTs with field plate gates with $l_g = 250$ nm are discussed in [7.77]. The device with the thinnest $\text{Al}_{0.32}\text{Ga}_{0.68}\text{N}$ barrier layer showed the slightest reduction in output power for thicknesses between 13 and 26 nm. Further, the positive impact of a GaN cap layer is mentioned. In addition, comparisons of pulsed-DC-measurements for various quiescent bias and at several stages of the RF-testing are a simple, though very sensitive, methodology for the analysis of the degradation of GaN HFETs. The impact of RF-stress on dispersion and power characteristics of AlGaN/GaN HEMTs is discussed in [7.56]. The saturated drain current I_{Dsat} is reduced after RF-tests at 5 GHz while the output power level is maintained. The dispersion of the transconductance measured between 50 Hz and 100 kHz is found to be nearly unchanged. UV-light-illumination leads to a drain current recovery. The analysis suggests the modification of traps in the gate–drain region as a result of the aging. The monitoring of low-frequency noise in correlation with the effects of RF- and DC-stress on AlGaN/GaN MODFETs is analyzed in [7.135, 7.136]. The principal finding for the impact of RF-stress is a significant shift in the threshold voltage V_{thr} of the GaN HEMT after the stress, while the $1/f$ -noise floor is not strongly affected after stress. As an example of the output power degradation, Fig. 7.6 gives the development of the output power at 10 GHz over 500 h for four AlGaN/GaN HEMTs with $W_g = 0.48$ mm at a $P_{-1\text{dB}}$ power compression operated at $V_{\text{DS}} = 30$ V and class-A/B. A change of output power with time is observed within margins of about 1.5 dB. The behavior can be separated in a decrease of the output power in the first 200 hours, which has been repeat-

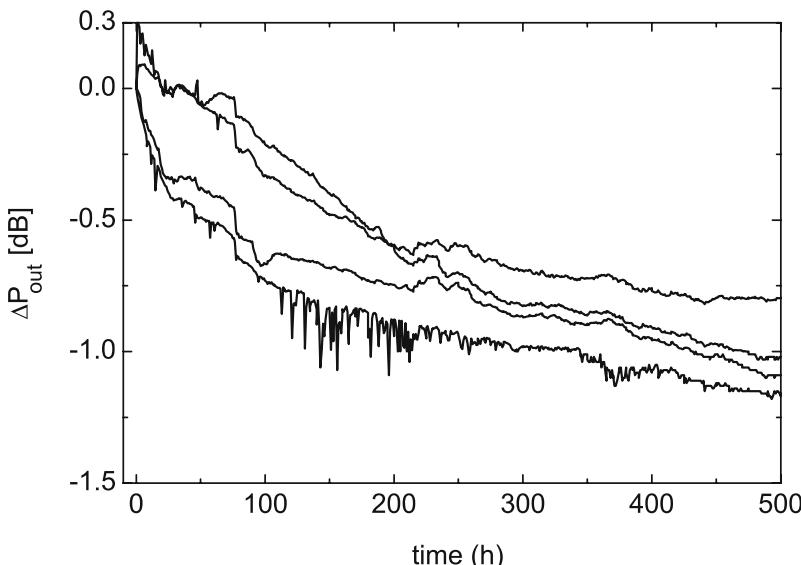


Fig. 7.6. Change of the output power of a GaN HEMT with $l_g = 300$ nm and $W_g = 480 \mu\text{m}$ at 10 GHz vs. time [7.33]

edly presented [7.28] based on the negative bias temperature instability, as discussed with (7.8). It is further noted that some oscillations can occur in the test setup due to the changes of the device over time. The device degradation can be explained by the changes of several of the device characteristics with time:

- A change, i.e., mostly an increase of the knee voltage equivalent to a change of the access resistances
- A change, i.e., mostly a reduction of the maximum drain current $I_{D\text{sat}}$ [7.56]
- A change of the threshold voltage V_{thr} , for NBTI a positive shift, leading to a reduction in output power [7.28]. A negative shift of the threshold voltage leads to an increase of the drain current and output power over time
- A change, i.e., mostly an increase of the minimum or pinch-off current at high V_{DS} voltage [7.56, 7.145]
- A change, i.e., mostly a reduction of the breakdown voltage

The origin of actual changes of the output power and current can now be tracked.

7.3 Failure Analysis

Once the degradation of the terminal characteristics has been analyzed, physical sources for the degradation have to be isolated to mitigate the mechanisms through changes in epitaxial growth and process technology. Fig. 7.7 summarizes possible failure mechanisms in a GaN HFET in a device cross-section. Similar to any other III-V devices, the following issues have been discussed for device failure mechanisms of III-N FETs (for the numbering see Fig. 7.7):

- (3) Dislocation-induced degradation due to the lattice mismatch to the substrate [7.26]
- (3) Defect-induced changes of the minimum drain current $I_{D\text{min}}$ [7.145]
 - (1) Gate sinking [7.32, 7.38]
 - (1) Other changes in the Schottky contacts [7.76]
 - (5) Metal diffusion at ohmic contacts [7.73, 7.76, 7.84]
 - (6) Crystal damage in the highly doped Si doping layer [7.38]
 - (9) Cracking of the semiconductor to the stress and electric (polarization) fields [7.61]
 - (2) Hot-carrier effects, mostly due to high-field gradient for nonoptimized devices [7.38, 7.109, 7.124]
 - (4) (De-)trapping of the surface traps [7.38, 7.126]
 - (7) Changes in the surface morphology [7.67]
 - (8) Environmental effects through gas absorption [7.121]
 - (11) Cracking issues due to the differences in CTEs of the materials in use [7.141]

The effects shown in Fig. 7.7 have already been grouped according to their physical nature.

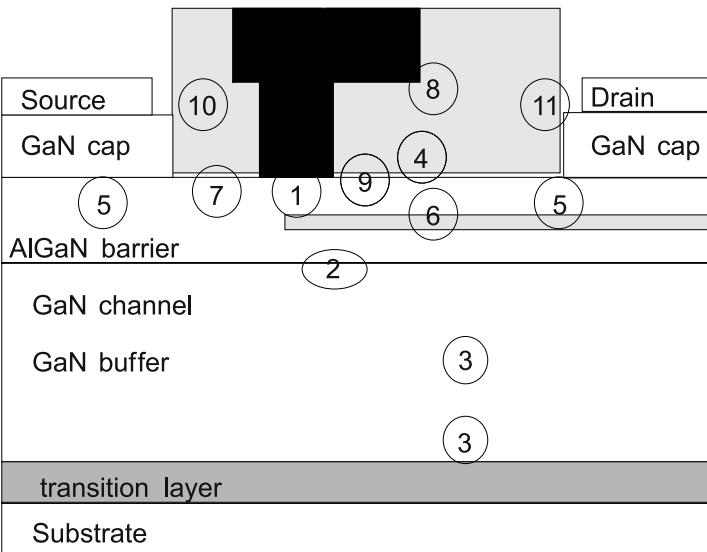


Fig. 7.7. Localized device failure mechanisms in GaN HEMTs on a heterosubstrate

7.3.1 Failure Mechanisms

Sometimes, but not always, the device failure mechanisms can be directly observed. Fig. 7.8 gives an example of a power bar. The breakdown path between two contacts and two gate fingers is optically visible, e.g., [7.76, 7.125]. However, such direct observation examples are not very numerous, as device failure may typically result in partial or total burnout due to high power densities, so that the device cannot be effectively analyzed, see Fig. 7.8. Several examples of failure-related analysis are available. The FIB/SEM/TEM cross-sections in [7.24] allow the analysis related to gate sinking, as is similarly performed for metamorphic devices, e.g., in [7.32, 7.121].

Apart from these classical effects enumerated, polar semiconductors face additional issues. A III-N FET, e.g., on s.i. SiC substrate, is fabricated on a heterosubstrate, resulting in an overall bowing of the wafer, as discussed in Chapter 2. This bow is modified several times during the processing:

- During epitaxy due to the lattice mismatch
- During processing due the metal deposition
- During wafer thinning
- During dicing and packaging

Such mechanical changes may have an impact on the III-N (H)FET performance, which can be dramatic in some cases. A more systematic study of the mechanical strain on the gate current degradation of AlGaN/GaN HFET is discussed in [7.62]. Uniaxial mechanical strain is applied to the device in a specific test jig. The gate current degradation is strongly affected due to

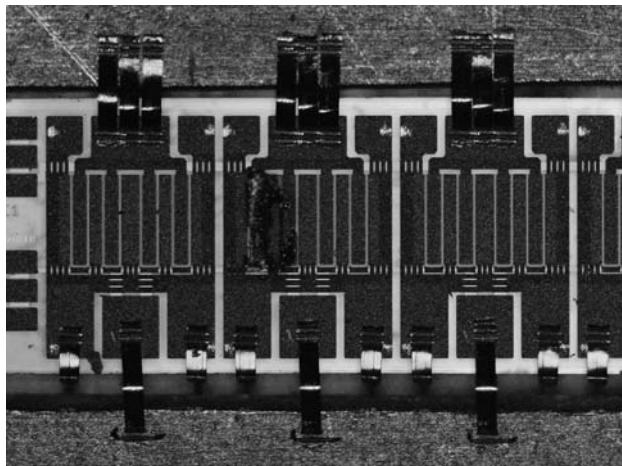


Fig. 7.8. Microscope image of a failed device

the change of the filling of traps in the AlGaN barrier at the drain side of the gate by the mechanical stress. The inverse piezoelectric effect has a similar mechanical effect during electrical stress and is thus related to purely mechanical stress. The related mechanical cracking of the AlGaN barrier layer due to the high polarization fields is described in [7.61]. A step-testing procedure is applied, which repeatedly provides a crack. This mechanical cracking is considered to be based on the piezoelectric properties and the resulting strong tensile strain once a voltage is applied. This principal finding hints to the need to evaluate the full consequences on the polarization in the devices.

Further studies involve impact of the source-gate-access region on reliability, as described in [7.41] similar to findings in other GaAs HFETs [7.122]. The electrostatic interaction of the source with the drain-end of the gate can have a major degrading impact on the effective breakdown voltage of GaN HEMTs.

A simple model for the impact of the gate length dependence of the reliability through thermal effects is given in [7.34]. Based purely on thermal consideration, the reliability drops as a function of gate length l_g . However, the model neglects the significant impact of the change in the hot carrier degradation due to the change of the gate length.

More advanced reliability issues are discussed in [7.141]. These include:

- Oxidation and intermetallic reaction of metals such as Ti, Al, Ni, Au in the ohmic contact
- Ohmic reactivity with the AlGaN
- Ion migration along dielectric surfaces
- Medium-/deep-level electron trap generation at high field
- Stress fracture of interconnect metals
- CTE mismatch of the various metals, dielectrics, and semiconductors

Some of these mechanisms have already been discussed. The ohmic contacts and the adjacent passivation are subject to ohmic oxidation, microcracking, and metal migration along the cracks. This leads to a reduction of the breakdown voltages. Further, the reliability of MIM capacitances is investigated which is limited by trap-assisted band-to-band tunneling. This testing is very similar to the needs of passive elements on GaAs. However, due to the need for increased bias levels and parallel compact integration, the additional testing is needed. The degradation of the drain current of AlGaN/GaN HEMTs with implant isolation at 300°C is detailed in [7.85]. The off-state of the device is not affected, but with the flow of the carriers, a hot-carrier degradation mechanism is effective between gate and drain. In the case of a mesa structure the effect is considered to be suppressed by the reduction of the side gate effect. This means, that two devices in the case of implantation can interact through the incomplete isolation, while the mesa process mitigates the interaction. At the same time, a mesa process can also be critical, as discussed in Chapter 4. Parts of these limiting mechanisms are very process specific and some even trivial, such as metal breakage and CTE issues. However, they all require attention to ensure reliable operation of the full device in the system.

7.3.2 Reliability Case Studies

The effects resulting from the issues mentioned above can be grouped according to the most important failure mechanisms and are detailed here as case studies.

Degradation due to Unstable Contacts

High-contact annealing temperatures at or beyond the Debye temperature of GaN make the device susceptible to uncontrolled metal–semiconductor intermixing in alloys [7.141], uncontrolled chemical reactions [7.141], and uncontrolled interfaces and structures within the semiconductor [7.42]. FIB techniques and scanning tunneling microscope (STEM) images can help to analyze the contacts, as performed in [7.24]. The intermixing at the ohmic contacts leads to several possible reliability issues, such as [7.42]:

- Uncontrolled vertical or lateral diffusion of metal
- Spike structures with locally high current densities
- Reduction of nominally safe distances between contacts

Low-activation energies of only 0.9 eV are found during reliability testing for a more reliable and further developed SiC MESFET process [7.102]. This activation energy is correlated with the degradation of the ohmic contacts, which thus are improved to mitigate the degradation effect. Ohmic contacts are found to be degrading in AlGaN/GaN HFETs, e.g., in [7.141, 7.143]. On the contrary, no significant change of the ohmic metal in AlGaN/GaN HFETs prior to and after the stress test is found in [7.24]. The Ir-based Ohmic contact

in [7.31] is optimized toward specific high-temperature operation at 350°C. Thus, several variants exist to built reliable ohmic contacts. However, also the secondary effects of ohmic contact formation and subsequent microcracking of the passivation have to be considered [7.141]. Low-annealing temperatures may be beneficial to suppress secondary effects, e.g., [7.69].

Schottky contacts have been investigated with regard to reliability in [7.1, 7.54, 7.125], especially at high temperatures [7.12]. The outdiffusion of Pt from the gate is found to be a major reliability concern in [7.60, 7.125]. The generation of an interfacial layer between the semiconductor and the gate contact are found to be the reason for an increase of the Schottky barrier height during stress in [7.121]. The analysis is confirmed by FIB images. Oxygen is found at the interface after aging in [7.60]. The oxide layer is found to be thinner near the gate edge. On the contrary, no metal interdiffusion at the gate contact is observed in [7.24] after DC-step-testing confirmed by STEM imaging. The failure mechanism observed in [7.29] can again be correlated with the oxidation of the AlGaN barrier near the gate after graceful degradation of the device RF-power performance at 10 GHz. Electron energy loss spectroscopy (EELS) maps of nitrogen and oxygen show oxygen at the critical gate–drain edge after aging. No electromigration or gate sinking is observed in the TEM images.

Ni/Au-based gate contacts are optimized and verified with respect to stable operation at channel temperatures of 300°C [7.1]. The optimization procedure is performed at elevated temperatures to guarantee the stability at reduced temperatures. Ni/Au contacts are tested for a gate length $l_g = 0.8 \mu\text{m}$. Initial results provide sudden degradation of the gate contacts in the pinch-off test after some hours, as reported in [7.1, 7.58]. The degradation is correlated with the surface morphology and with the topological distribution of the gate currents. Hexagonal pits from the epitaxial growth are correlated with the increase of gate currents. A threshold level of $20 \mu\text{A mm}^{-1}$ is defined for the reverse leakage at $V_{DS} = 40 \text{ V}$. The change of both reverse and forward gate currents after screening is insignificant at operation bias $V_{DS} = 50 \text{ V}$ and also as a function of temperature.

The forward gate current under high compression or switching is considered a reliability issue by the same group, e.g., [7.67, 7.68]. This contact-related issue is solved by the suggestion of a GaN MISFET on a very similar device structure. However, no full reliability data is provided for this device type.

A trap analysis of these GaN–SiN-MISHEMTs is performed in [7.68]. A detailed pulsed-DC-analysis is performed from various quiescent bias, as detailed in Fig. 7.2 and Fig. 5.8. All quiescent bias are found to be stable. However, for the aggressive quiescent bias at $I_{D\max}$ at $V_{DS} = 50 \text{ V}$ with a dissipated power of 35 W/mm , a strong shift of the threshold voltage V_{thr} and transients of the output characteristics are observed. An improvement of the gate-insulating SiN dielectric is considered to enhance the reliability at high V_{DS} bias and forward-gate current conditions.

Further indirect effects of the gate metallization involve the impact of the gate on the underlying semiconductor through stress and strain. Such stress effects have been mentioned in [7.15].

Device Degradation Due to Changes in the Buffer Layer

The buffer in this study involves all the (insulating) semiconductor layers under the active device structure in the direction of the substrate. The buffer is a very large semiconductor volume relative to the actual active device. The buffer layer stack basically has three functions with physically contradicting demands:

- Compensation for lattice mismatch of various kinds
- Good thermal transport
- Very good electrical isolation at high bias

The simulated field distribution in the buffer is already analyzed in Fig. 4.7 in Chapter 4. We found a very inhomogeneous field distribution, especially at high V_{DS} bias. Thus the control of the trap concentrations and consequent charge control is most crucial for reliability, especially since the exact amount of carriers is stress-dependent. The optimization with respect to epitaxial defects in the buffer targets good electrical isolation [7.51] while maintaining a good surface morphology, i.e., to avoid hexagonal pits [7.67] and other structures. A detailed optimization procedure for reliability improvements is described in [7.51, 7.67]. The optimum defect engineering to be found leads to isolating defects which at the same time have no significant dynamic (de-) trapping behavior at all time range from hours to nanoseconds, even when the buffer is subject to high electric fields. Simulation studies on the impact of traps in AlGaN/GaN HFETs below the channel region are given in [7.45]. Iron buffer codoping has been suggested to enable good buffer isolation [7.53]; however, iron doping is subject to doping diffusion to the upper active device layers during growth and it is also subject to reactor memory which needs careful control. Even once the good isolation is obtained, the long-term stability of the material has to be shown, which has been proven, e.g., in [7.141]. The impact of the buffer engineering on the output power degradation is mentioned in [7.67]. After optimization of the growth conditions, which are not specified, the RF-reliability is enhanced with respect to the I_{Dq} degradation and the output power degradation [7.67]. Defect-induced changes of the minimum drain current on 3-in. s.i. SiC wafers are reported in [7.145]. With the application of a very fine wafer mapping the increase of the minimum current $I_{D\min}$ is correlated with micropipe-induced changes of the epitaxial layers. The abnormal growth on top of the micropipes is analyzed by SEM in cross-sections of the hexagonal pits.

Degradation Due to Unstable Interfaces

Several publications point to the importance of the dielectric/semiconductor and semiconductor/semiconductor interfaces, not only for the mitigation of

interface-related dispersion, but, for very similar reasons, also for the gate leakage suppression and reliability enhancement [7.56, 7.67, 7.76]. The findings include:

- Charge modifications through surface-related techniques during and after device stress, e.g., [7.126]
- Sensitivity to light illumination in a study of the material composition in the barrier in [7.136]
- The impact of interface passivation, e.g., in [7.74, 7.117]
- Changes in the gate leakage currents for devices with an AlN interlayer at the AlGaN/GaN barrier interface [7.27]
- Indiffusion of hydrogen from the passivation in p-layers in optoelectronics devices [7.89]
- Strong changes of the HFETs in photoluminescence and lighting experiments [7.87, 7.91, 7.109]
- The beneficial impact of passivation early in the process on reliability [7.63]
- The positive impact of various field plates on device reliability [7.77]

The means to minimize these effects are mostly technology-based and strongly related to the passivation. The aim of a good and reliable device passivation is to:

- Stabilize the trap density at the dielectric/(Al)GaN interface [7.67]
- Reduce the possibility of creating additional traps [7.123] during operation
- Reduce the gate current (at high temperatures) [7.67]
- To achieve a lateral and vertical field reduction at the interface [7.43, 7.131]

The related hot-carrier degradation has been studied, e.g., in [7.109]. The investigations for GaN MESFETs show stronger degradation for unpassivated devices. Light illumination is used to discriminate the trapping effects at the surface from those in the buffer material. The experiments suggest a modification of the surface in the ungated device access region after hot-electron stress. The impact of the field plate for field engineering for AlGaN/GaN HFETs has been mentioned repeatedly, e.g., [7.77]. The effect of the field-peak reduction along the channel is especially beneficial at the sensitive semiconductor/passivation interface, as the field-related trap creation [7.133] and trap recharging can be reduced. This is especially true for multiple field-plate concepts [7.131]. Several studies are available for the optimization of the field-plate structures for various frequencies, e.g., [7.101]. Surface-related hot-carrier effects in AlGaN/GaN HFETs can be well distinguished from other effects, as the hot-carrier degradation has a negative temperature coefficient, as mentioned in [7.24]. That means this particular degradation reduces at higher ambient temperatures while other, such as diffusion, increase. Thus, despite the strong impact of the interface effects, other material-related effects can be separated [7.24, 7.79]. This concludes the discussion of devices under regular operation.

7.4 Radiation Effects

Wide bandgap semiconductor devices are promising candidates in radiation-harsh environments due to the relatively large bandgap and the reduced probability of current transport via trapping and other defects. A number of investigations have been published with respect to the impact of irradiation on III-N semiconductors. ^{60}Co γ -irradiation effects on n-GaN Schottky diodes are discussed in [7.4, 7.134]. In general, a low susceptibility of the GaN semiconductor to radiation damage is found, whereas the metal/semiconductor interfaces may be the limiting factor because of the trap creation due to irradiation. Further effects of ^{60}Co γ -radiation on DC, RF, and pulsed- I - V characteristics of AlGaN/GaN HEMTs are discussed in [7.4]. The changes of the DC-characteristics are found to increase linearly with the dose of the γ -irradiation. The maximum pulsed-drain-currents I_{Dsat} increase with the irradiation level. In general, a high radiation hardness of GaN is found, while the radiation-induced changes are consistent with induced trap creation. Overviews of relevant traps are given, e.g., in [7.83]. Further γ -irradiation results are given in [7.116]. N-doped GaN layers are compared prior to and after ^{60}Co - γ -irradiation with a radiation doses of 10^{19} cm^{-2} . The slightly doped layer with $n = 10^{17} \text{ cm}^{-3}$ shows a reduction of the carrier concentration, while a heavily doped layer with 10^{18} cm^{-3} yields an increase after irradiation. Annealing at 550°C can recover the original values for mobility and carrier concentration. The annealing behavior of proton-irradiated $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HEMTs on sapphire substrates is discussed in [7.18]. A high proton-irradiation dose 10^{14} cm^{-2} at 1.8 MeV leads to a strong reduction of the transconductance and the saturated current by about 60%. Recovery of the I - V characteristics can be achieved by rapid thermal annealing at 800°C . Further results of proton irradiation on GaN layers are found in [7.50, 7.66]. The photoluminescence spectra after 2 MeV proton irradiation with fluences of up to 10^{16} cm^{-2} show an increased hardness of GaN bulk material as compared to GaAs with respect to displacement damage. This makes the GaN bulk material suitable for space applications. The defects observed after proton irradiation are line defects. Additionally, new traps are introduced, which are not present after He-ion or electron bombardment. A remarkable hardness of GaN material with respect to ion damage is also found in [7.130]. For silicon ion doses of 10^{16} cm^{-2} at energies of 90 keV , the interface is found to be the sink for damage build-up. Reversal of the disorder induced by the ion irradiation through annealing is found difficult. Neutron irradiation on GaAs double heterojunction HEMTs leads to trap creation [7.104]. Deep midgap traps are created, which affect both interfaces and semiconductor layer material. Both mobility and sheet carrier concentration are reduced after neutron irradiation at a dose of $10^{15} \text{ n cm}^{-2}$. Effects of neutron irradiation on Au/GaN Schottky diodes are given in [7.139]. Again a strong radiation hardness is found. Two deep electrical traps, one nitrogen vacancy related and one hydrogen related, are strongly influenced by neutron fluxes. In conclusion, systematic investigations show the

predicted hardness of the wide bandgap semiconductor materials and devices, while device components such as contacts and dielectrics need further specific optimization.

7.5 High-Temperature Operation

The reduced thermal activation due to increased bandgap energies makes wide bandgap devices further promising for high-temperature operation beyond classical operation temperatures. This has been mentioned repeatedly for GaN devices, e.g., in [7.31, 7.36].

Comparison of Electronic Technologies

The maximum temperature for the operation of electronic devices for silicon and GaAs devices is limited. For low-power silicon on insulator (SOI) devices this temperature amounts to about 300°C [7.35]. For GaAs-HFETs, temperatures beyond 400°C are mentioned in [7.112, 7.142]. However, reliability constraints, e.g., of the contacts, lower this temperature for circuit operation to safer regions of operation, e.g., to 150°C, reported in [7.10]. For specific high-temperature operation, circuits allowing up to 250°C [7.49] and 300°C [7.37] have been presented. Techniques for the enhancement of RF-devices for high-temperature operation of GaAs devices are provided, e.g., in [7.95]. The GaAs devices are characterized by S-parameter measurements at elevated temperatures of up to 300°C, and the device changes relative to room temperature are used to modify the circuit design. The changes include increase in breakdown voltage, gain reduction, and shift of the threshold voltage. A typical principal criterion for the high-temperature stability of a semiconductor is the Debye temperature T_{Debye} [7.5]. Values of T_{Debye} are compiled in Table 7.1 for various semiconductors. Based on the comparison in Table 7.1,

Table 7.1. Debye temperatures (given at 300 K) for different semiconductors

Material	T_{Debye} (K)	Ref.
InAs	280	[7.80]
Si	625	[7.114]
GaAs	360	[7.80]
GaN	600	[7.36, 7.106]
AlN	1,150	[7.80]
InN	660	[7.80]
6H-SiC	1,200	[7.80]
4H-SiC	1,300	[7.36]
Diamond	1,860	[7.80]

SiC has been suggested as a genuine high-temperature semiconductor material [7.30]. Various SiC-device types such as MESFETs, MISFETs [7.140], junction FETs [7.30, 7.118, 7.118], and related circuits [7.81] have been suggested for operation temperatures beyond 500°C [7.52]. The maturing SiC-device- and MMIC-technology is a strong competitor to III-N devices, unless the nitride devices can make use of their higher speed performance. Principal high-temperature performance of III-N materials up to 800°C is discussed in [7.36]. AlGaN/GaN HEMTs grown by MOVPE on sapphire substrates are subject to temperature stress of up to 800°C, both in biased and unbiased conditions. Irreversible degradation of the intrinsic active heterostructures is found for operation above 600°C.

III-N Device High-Temperature Operation

The role for wide bandgap semiconductors in high-temperature electronics is discussed in [7.96]. The temperature dependence of device [7.3] and circuit performance as a function of backside temperature, packaging situation, and resulting junction temperature is of critical importance for system performance. On the device level, the importance of:

- The intrinsic carrier concentration
- The pn-junctions
- The thermionic leakage
- The reduction in carrier mobility
- Substrate leakage

are stressed for high-power high-temperature devices. High-temperature performance of AlGaN/GaN HEMTs on s.i. SiC substrates up to backside temperatures of 340°C has been discussed in [7.47]. The devices are found to operate in a stable short-term fashion up to backside temperatures of 250°C. The dissipated power density per area reached with SiC substrates is about 0.6 MW cm⁻². The resistances R_S and R_D , the transconductance g_m , and the saturated current I_{DS} show a nearly linear temperature dependence between room temperature and 300°C. Further high-temperature effects for the RF-power characteristics for channel temperatures between RT and 300°C have been reported [7.1]. A linear gain of 12.3 dB is reported at $T_{chan} = 269^\circ\text{C}$, which decreases nearly linearly by about 2 dB for a temperature change of 100°C at $V_{DS} = 50$ V. The saturated output power at 2.14 GHz decreases also nearly linearly by about 0.7 dB/100°C. The risk of thermal runaway in AlGaN/GaN HFETs is found to be low [7.1], based on a small shift in $V_{GS} \leq 0.01$ V to maintain a stable quiescent current for a channel temperature range of 250°C. The gain parameter variation for a temperature range between -25°C and 125°C is investigated for a variety of GaN technologies in [7.35]. Again, a linear reduction in the temperature of both the saturated drain current I_{DSS} and the transconductance g_m is found. This temperature behavior of GaN HEMTs is compared to GaAs PHEMTs. It is found that

the temperature variation for the GaN devices is smaller than for the GaAs devices. The explanation given is that the saturated velocity v_{sat} in GaN channels is less modified by temperature than in (In)GaAs heterostructures. The high-bandgap energies and the high-heterostructure barriers in III-N devices, i.e., reduction of the thermionic leakage, may also serve as an explanation for this behavior.

Temperature Dependence of Physical Quantities

The intrinsic carrier concentration n_i within different semiconductors can be calculated from the Boltzmann statistics [7.96]:

$$n_i = \sqrt{N_C \cdot N_V} \cdot \exp\left(\frac{-E_g}{2k_B T_L}\right). \quad (7.9)$$

The temperature dependence of the bandgap E_g , of the effective densities of states at the conduction band N_C , and at the valence band N_V are calculated as

$$E_g = E_{g,0} \cdot \frac{\alpha - T_L^2}{\beta + T_L}, \quad (7.10)$$

$$N_C = 2M_C \cdot \left(\frac{2 \cdot \pi \cdot k_B \cdot m_n \cdot T_L}{h^2}\right)^{3/2}, \quad N_V = 2 \cdot \left(\frac{2 \cdot \pi \cdot k_B \cdot m_p \cdot T_L}{h^2}\right)^{3/2}. \quad (7.11)$$

Fig. 7.9 depicts the intrinsic carrier concentrations for various semiconductor materials calculated from (7.10) and (7.11). The differences between conventional materials, such as Si and GaAs, and wide bandgap semiconductors, such as GaN and SiC, are clearly visible. The exponential impact of the energy gap in (7.9) makes the fundamental difference. A requirement for a good high-temperature semiconductor is an intrinsic carrier concentration which is negligible at the operation temperature range relative to the relevant doping concentrations in the device. This reference concentration for III-N devices typically amounts to 10^{16} cm^{-3} . This value of the intrinsic concentration n_i is reached by classical materials such as Si and GaAs, whereas the wide bandgap materials do not reach this intrinsic value n_i even for temperatures of 1,000 K. A similar result can be obtained for the thermionic leakage at the heterointerfaces and contacts. The reverse leakage current at a junction can be calculated as

$$I \simeq A_R \cdot K \cdot T_L^2 \exp\left(\frac{-q \cdot \phi_B}{k_B \cdot T_L}\right). \quad (7.12)$$

Assuming a maximum Schottky barrier height of 90% of the individual bandgap performed by bandgap engineering as a theoretical limit, the leakage currents are compared in Fig. 7.10, normalized to the same leakage of Si at room temperature. Apart from the purely thermionic leakage, further

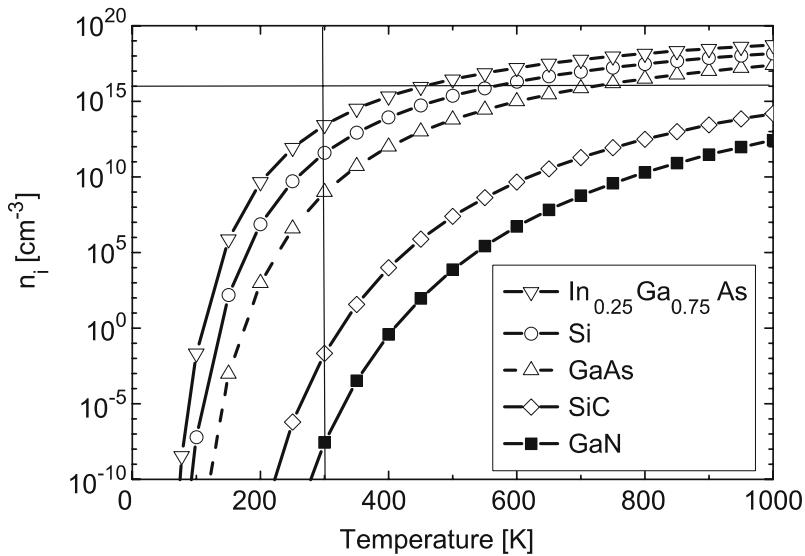


Fig. 7.9. Intrinsic carrier concentration n as a function of lattice temperature T_L for various semiconductors calculated from the Boltzmann statistics

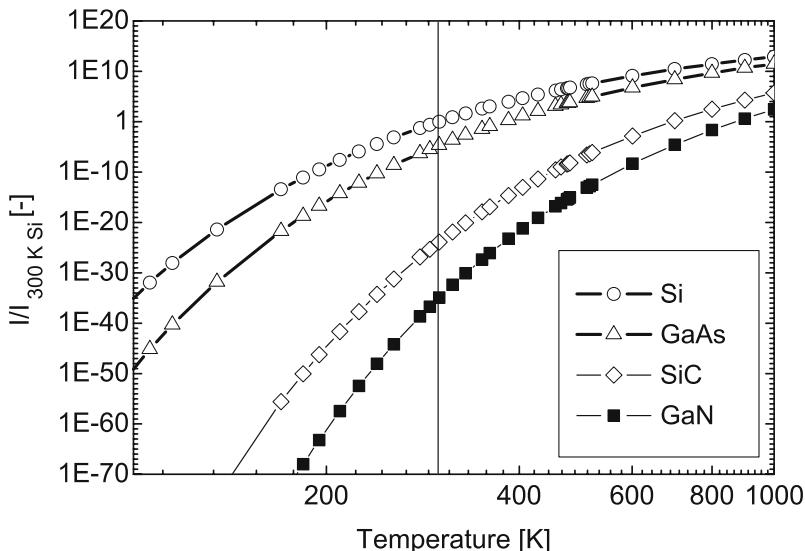


Fig. 7.10. Comparison of barrier leakage of Si, GaAs, GaN, and SiC as a function of lattice temperature T_L

leakage effects have to be considered. A second additional tunneling component is similarly influenced by increased temperature, as reported, e.g., in [7.99, 7.100, 7.148].

Chapter 8 will discuss the exact determination of the temperatures and integration aspects.

7.6 Problems

1. Assume the proposed increase in reliability of a GaN FET relative to an $In_{0.25}Ga_{0.75}As$ channel FET is due only to the increase in bandgap (activation energy at midgap). What is the change in the lifetime at the channel temperature of $125^{\circ}C$?
2. Based on what you know about GaN HFETs, is the assumption of question (1) reasonable? Give arguments!
3. Discuss the most pronounced failure mechanisms of GaN HFETs.
4. What is the most important difference between GaN HFETs and GaAs HEMTs with respect to substrate-related defects? Discuss!
5. Is a Schottky barrier of 90% of the bandgap a realistic assumption? What are the implications?
6. What are additional benefits of large bandgap devices apart from the intrinsic carrier concentrations? Think of traps and the related mechanisms.

Integration, Thermal Management, and Packaging

This chapter describes device and MMIC integration, such as passive coplanar and microstrip circuit techniques, thermal management, and mounting and packaging considerations for state-of-the-art III-N devices and amplifiers.

8.1 Passive MMIC Technologies

So far there are only a few reports with a full description of integrated circuit technologies in microstrip transmission-line technology for GaN HFETs [8.49, 8.74, 8.101, 8.107], contrary to the well-developed GaAs technology [8.60]. Cree demonstrated a fully integrated MMIC process for GaN HEMTs and SiC MESFETs in [8.93, 8.107]. The substrates are thinned to 100 µm. Similar processes are available from NGST [8.39, 8.49] and HRL [8.74] with substrate thicknesses down to 50 µm. A microstrip transmission-line process has been demonstrated by Triquint on HR-silicon substrate. Insulating Si substrates with a resistivity of 30 kΩ cm are used [8.32]. The substrates are also thinned to 100 µm. MIM capacitances with a breakdown voltage of 150 V are reported. Increased integration of GaN devices for base station applications, e.g., in driver amplifiers has been mentioned by RFMD in [8.20, 8.106], similar to the approach using silicon LDMOS for the same application; see [8.108]. Both spiral inductors and MIM- and MIS-capacitors are cointegrated.

8.1.1 Passive Element Technologies

The processing, characterization, and reliability of high-voltage high-power passive elements is of critical importance for GaN and SiC FET MMICs. Transmission-lines, airbridges, resistors, inductances, and MIM and other capacitances have to be hardened for the strict requirements of high-power, high-temperature, and high-voltage operation [8.124].

MIM Capacitances and Inductances

The availability of capacitive lumped elements is a key requirement for matching, DC-blocking, and other design functions on a MMIC. A number of recent publications have described the optimization of capacitances in the GaAs world for high-power operation [8.12, 8.134]. Typically, SiN or SiO_2 are used in various forms [8.11, 8.80, 8.134]. For higher integration, Ta_2O_5 [8.30] can be used in the GaAs world to save area on the wafer. SiN thicknesses in the MIMs down to 25 nm have recently been found useful for GaAs devices [8.12]. A number of other high-k dielectrics have been developed for higher integration of capacitances in silicon IC processes [8.43, 8.44, 8.133]. The higher dielectric constants reduce the area consumption at high integration levels. Specific development is needed for high-voltage operation in MIMs for operation bias of ≥ 50 V. Cree reported the development of reliable MIM capacitances with a size similar to those for GaAs processes, however, with breakdown voltages increased by a factor of 3 [8.124]. The associated lifetime is 10^8 h. Typical breakdown voltages are at least 150 V. An SiO_2/SiN stack with thicknesses of 80/220 nm with an effective $\epsilon_r = 6.7$ and a capacitance per unit area of 200 pF mm^{-2} is given in [8.113].

Fig. 8.1 gives the measurement of the breakdown voltage of an optimized MIM capacitance integrated in a GaN HEMT process. It can be observed that these devices can be operated up to at least 150 V. Fig. 8.2 gives the

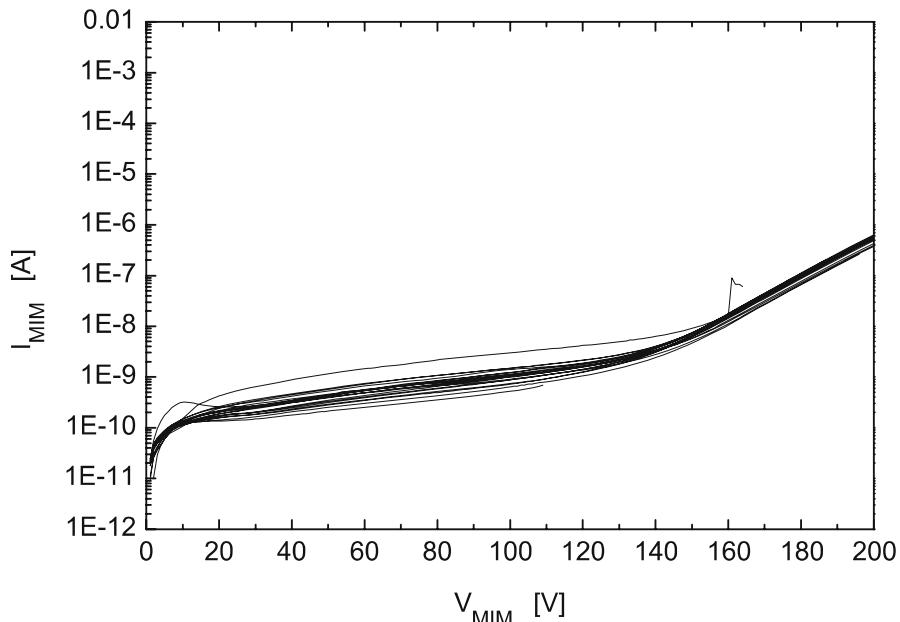


Fig. 8.1. Current–voltage measurement of various MIM capacitances at room temperature

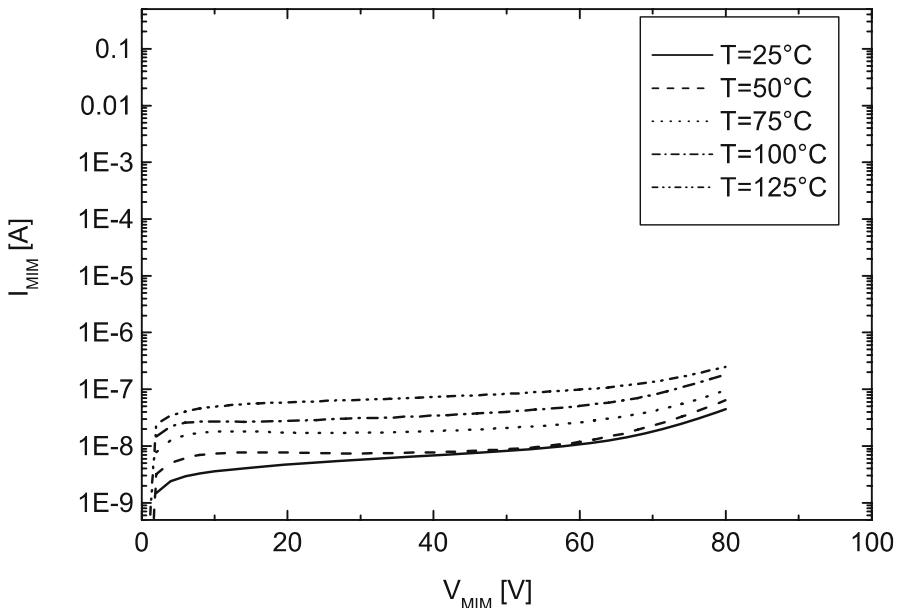


Fig. 8.2. Current–voltage characteristics of a MIM capacitance with the substrate temperature as a parameter

current voltage characteristics of an MIM capacitance for a different area as a function of temperature for a similar structure between 25 and 125°C . We see an increase in the leakage due to the temperature change. High-power operation may heat the passive devices on a MMIC, so an additional breakdown margin is needed, based on the measurements of Fig. 8.2. The substrate quality is important for the quality of the structures on top. Fig. 8.3 gives an example of the impact of a micropipe cluster on an MIM capacitance on s.i. SiC. This issue has been discussed, e.g., in [8.111]. However, the recent improvements in substrate quality have drastically reduced the occurrence of such effects. The high-power levels lead to the increase of the metallization thicknesses. Fig. 8.4 gives an image of a concentrated inductance with a thick galvanic metallization. The high-power operation requires the optimization of both metal thickness and the exact geometry of area-efficient lumped elements for high-voltage operation. This requires air gap adjustment for repeatable manufacturing, as the aspect ratio of thickness and air gap needs to be controllable during processing.

Passive Resistances

Lumped resistances can be integrated in various forms. First of all, ungated semiconductor layers can be used to obtain resistances for which the overall value does not have to be controlled with great precision. This is typically true for high-resistance elements. For higher accuracy and lower resistance,

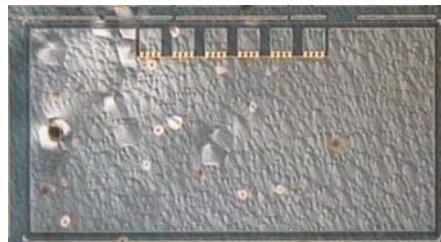


Fig. 8.3. Image of the impact of substrate quality on MIM metallization

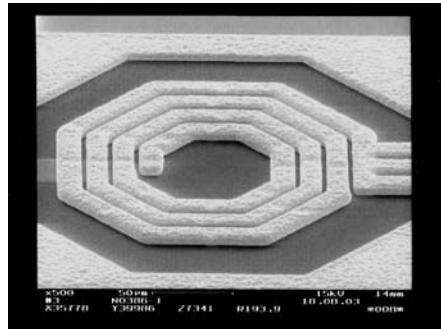


Fig. 8.4. Image of a lumped inductance with thick metallization layer

lumped ohmic resistances are typically integrated as TaN resistors with $25 \Omega \text{ sq}^{-1}$ [8.50] or as NiCr resistors with a resistivity of $50 \Omega \text{ sq}^{-1}$ [8.9] or $100 \Omega \text{ sq}^{-1}$ [8.63]. TaN thin-film resistors for high resistance with $45 \Omega \text{ sq}^{-1}$ and TiN with $45 \Omega \text{ sq}^{-1}$ are reported on s.i. SiC in [8.113]. NiCr resistors with a sheet resistance of $20 \Omega \text{ sq}^{-1}$ are reported by Cree in [8.93] for the integration of GaN HEMTs. Several other processes have been reported, some of which yield a sheet resistance of the NiCr of $50 \Omega \text{ sq}^{-1}$, as is typical for the GaAs MMICs [8.103].

8.1.2 Microstrip Backend Technology

A microstrip transmission-line process on s.i. SiC substrate is rendered complicated due to the extreme material properties of SiC, such as hardness [8.68], chemical inertness, and overall substrate quality of s.i. SiC substrates. A microstrip backend process requires the solution of the following issues, as described in Chapter 4:

- Wafer mounting using an appropriate adhesive [8.76]
- Full wafer thinning [8.68]
- Via-etch
- Metallization
- Wafer removal

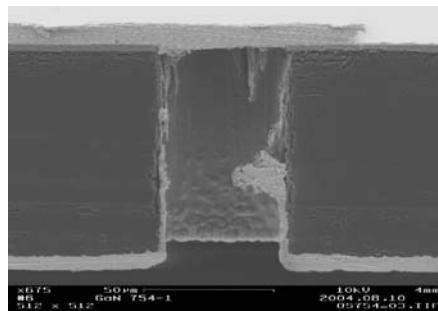


Fig. 8.5. Viaholes in a 100 μm thick s.i. SiC substrate

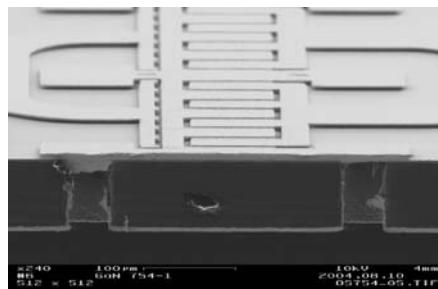


Fig. 8.6. Full power amplifier stage in microstrip transmission-line technology

Cree reported a process with 100 μm thick SiC substrates with 2- and 3-in. diameter and 75 μm diameter via holes in [8.93, 8.124]. Further references to a microstrip process on 3-in. s.i. SiC substrate for Ka-band are given in [8.74]. The thickness of the thinned s.i. SiC substrates is 50 μm in this case [8.74] with a via geometry of 30 \times 30 μm . A thickness of 5 μm for the geometry of the galvanic is reported in [8.29]. The SiC MESFET process in [8.113] yields 100 μm substrate thickness. Fig. 8.5 and Fig. 8.6 give SEM images of viaholes in the output stage of a Gan HFET power amplifier on a 100 μm thick s.i. SiC substrate [8.120]. The viaholes are well covered by metal from the backside, which ensures good grounding of the frontside elements. Further the vertical shape of the viaholes is visible based on the anisotropic etch.

8.2 Integration Issues

Integration of III-N devices and MMICs is a key challenge for the application. [8.42, 8.51, 8.65, 8.67]. GaN devices pose additional problems for system engineers. These integration issues related to GaN-based hybrids and MMICs are:

- Increased power density per die and die area [8.51]
- Increased requirements for performance of conventional heat sinks/thermal contacts, as is discussed in Chapter 7

- DC- and RF-power transmission for increased power levels
- Transparent substrates [8.101]
- Substrates under epitaxial strain
- Increased operation temperatures [8.79].

The electrical issues are discussed in several publications, e.g., in [8.51, 8.101]. Further, assembly issues, such as the processing of optically transparent materials, pose new challenges for automatic packaging equipment, as mentioned in [8.101]. As bowing is a critical issue, the treatment of diced III-N devices under strain through heteroepitaxy is important to ensure reliable device operation. The challenge for increased operation temperatures with respect to packaging, especially in the 300–600°C range is mentioned in [8.79]. Currently operation temperatures similar to those for GaAs modules are being considered for TR-modules for the initial integration of III-N devices; see [8.51]. More specific high-temperature packaging techniques are discussed in [8.95, 8.125]. At these temperature levels, the packaging solutions are typically niche solutions.

Module Integration

Overview articles on transmit/receive (TRX) modules and related technologies for radar and other applications are given in [8.14, 8.42, 8.51, 8.52, 8.65, 8.67]. TRX modules have been under discussion for a long time [8.3, 8.51]; however, cost reduction [8.3, 8.62] and the automatic assembly aspects of a large number of hybrid components have so far restricted their application. TRX-module integration [8.3, 8.51] covers the different functions performed by a multifunction and multichip RF-module, as depicted in Fig. 8.7. This

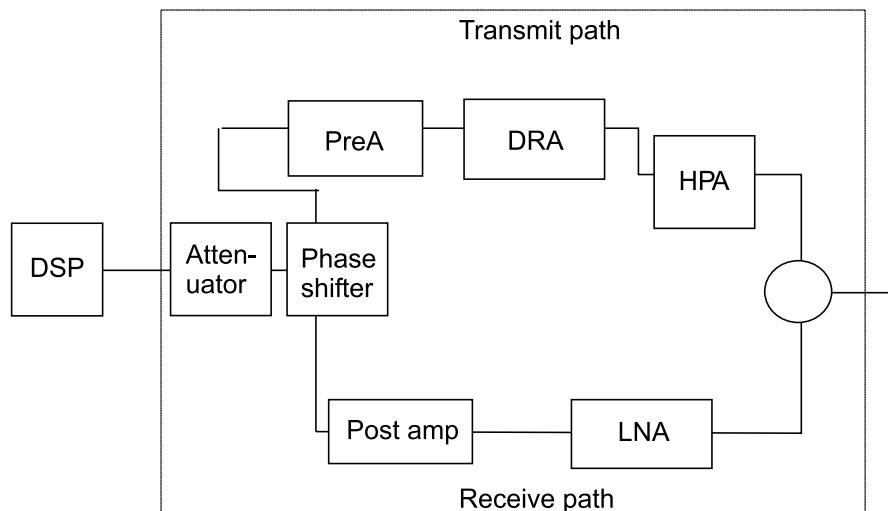


Fig. 8.7. Schematic of the RF-part of a transmit-receive module

includes phase shifting, attenuation, amplification, limiting, and module protection through circulators. The transmit path of a radar TR-module typically involves several driver (DRA) amplifiers and (balanced) high-power amplifiers (HPAs) in the transmit path. The receive path is composed of a limiting function, a low-noise amplifier (LNA), and possibly a second amplifier [8.42]. An overview of architectural aspects and requirements is given in [8.71]. Issues from TRX technology to system aspects and manufacturing aspects such as module calibration and statistics are covered. Trade-offs for the benefits of different module architectures are discussed further, e.g., in [8.3].

8.3 Thermal Management

Thermal management is of ultimate importance to III-N devices, as even very simple estimates can reveal, e.g., [8.36]. Very high channel temperatures are easily reached unless proper packaging and DC-limiting precautions are taken.

8.3.1 Thermal Analysis

Several overviews of thermal analysis of III-N devices are available, e.g., in [8.84, 8.109].

Basic Findings

Thermal analysis of AlGaN/GaN power HFETs is described, e.g., in [8.84]. DC-parameters, noise, and output power are analyzed between 380 and 540 K. The thermal coefficients of several quantities are extracted, as also detailed below. It is found in general that the temperature coefficients of the III-N device terminal quantities are lower than those of GaAs devices, e.g., [8.81]. This means that III-N devices are less sensitive to temperature changes. However, the dissipated power densities per unit area are much higher, which balances or even overcompensates this advantage. This situation is illustrated in Fig. 8.8 in the world map of thermal management, which has been presented in similar fashion in various publications. The increase of the RF-power densities and power levels approximately leads to the same increase in the dissipated power levels. The resulting dissipated power densities per area increase by a factor of 10 for the same application. This means that we change from power densities from $\leq 1 \text{ W mm}^{-2}$ to the range of $1\text{--}10 \text{ W mm}^{-2}$. The main information is hidden in Fig. 8.8. The change of the power density essentially leads passive-conduction cooling-system to their limits and requires solutions beyond, potentially, active cooling solutions.

Determination of Temperatures

Several techniques have been used for analysis of the actual temperature and temperature distributions in the materials and devices. Noninvasive infrared

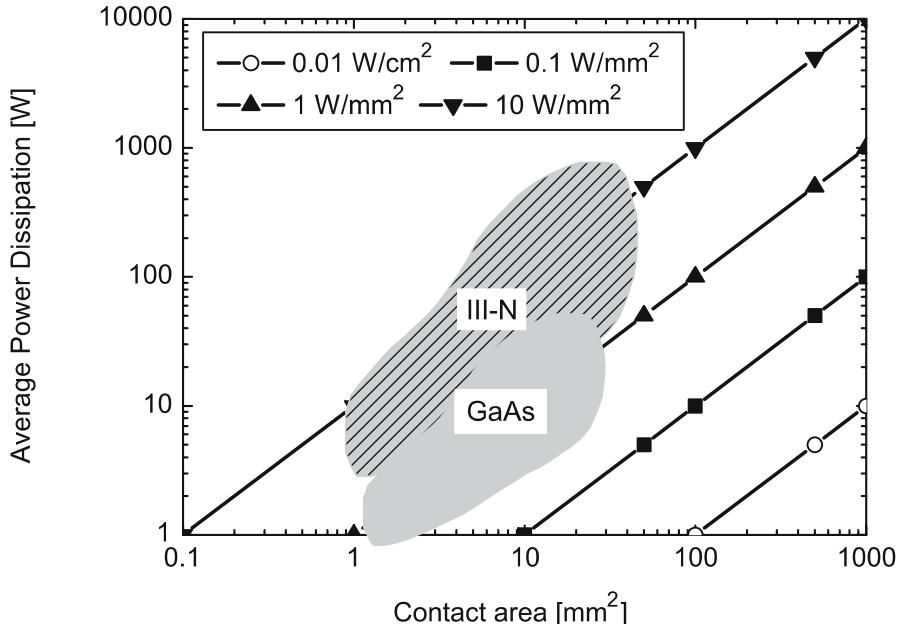


Fig. 8.8. Overview on thermally dissipated power vs. area for different technologies

camera measurements are reported in [8.30, 8.84, 8.109]. An infrared microscope is combined with an on-wafer loadpull setup. The variation of the temperature distribution as a function of input drive power can be monitored. This allows temperature control for realistic operation conditions. Additionally, Raman measurements of the lattice temperature in GaN devices with higher spatial resolution are given in [8.55]. The DUT can be investigated from the frontside and from the backside through the substrate, so that the heat generation can be directly monitored through the optically transparent substrate and the III-N layers. The spatial lateral resolution is submicron, while the depth resolution is $\approx 1\text{ }\mu\text{m}$. Integrated Raman spectroscopy and IR thermography are used in [8.56, 8.96, 8.97]. The IR thermography is used for time-efficient monitoring, e.g., for void control [8.66], with a diffraction-limited resolution of $2\text{--}5\text{ }\mu\text{m}$, while the Raman spectroscopy allows better resolution of the peak temperatures near the gates. The Raman measurements and 3D-thermal simulations of the same structure have been brought to an agreement in the hot spot of the near gate region. Further techniques are presented with the results below. Fig. 8.9 gives the layout of a multifinger high-power GaN HFET. The most important thermal layout parameters, such as the gate-to-gate pitch l_{gg} and the gate width W_g are depicted. Other important parameters are the lateral and vertical boundary conditions.

Fig. 8.10 gives the principal thermal situations for a device. The device can be cooled by three approaches:

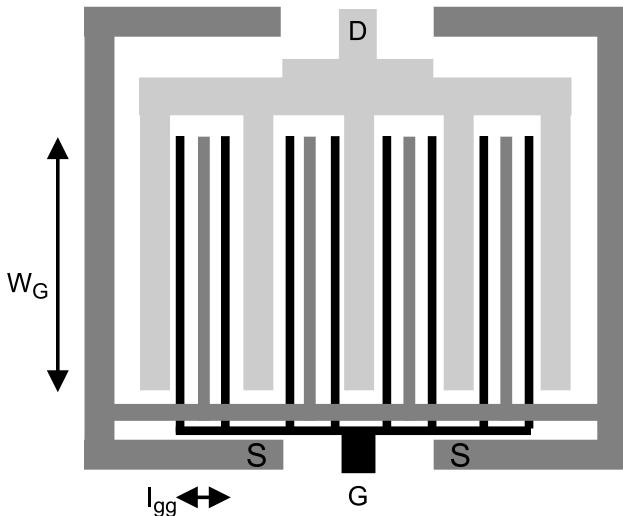


Fig. 8.9. Layout of an eight finger coplanar high-power GaN HFET

1. Purely from the backside
2. Purely from the frontside
3. In a combination of situation (1) and (2)

Based on this insight, Fig. 8.11 depicts a 3D-view of the thermally relevant parameters in a HPA for the most conventional situation (1) in Fig. 8.10. The parameters include:

- The overall extension of the chip ($X \times Y$)
- The thickness of the semiconductor t_{sem}
- The thickness of the substrate t_{sub}
- The thickness of the adhesive or solder t_{ad}
- The submount heat sink material and thickness t_{subm}
- The temperature T_{sub} and temperature distribution at the backside of the substrate
- The gate-to-gate pitch l_{gg}
- The gate width W_g and, with minor impact, the gate length l_g

The determination of the optimized parameters is discussed in Sect. 8.3.2.

8.3.2 Thermal Material Selection and Modeling

A detailed modeling of the relevant thermal parameters is provided in this section for proper thermal analysis. The temperature dependence of the thermal conductivity is modeled according to the exponential law in (2.3) in Chapter 2. A good compilation of models for the temperature of conventional semiconductor materials is given in [8.86]. Parameter values for the models for

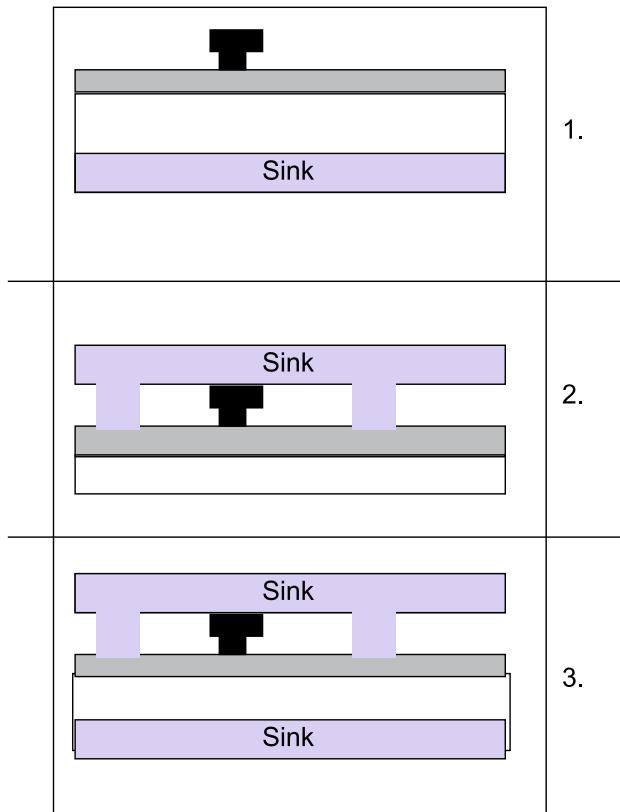


Fig. 8.10. Principal thermal situations

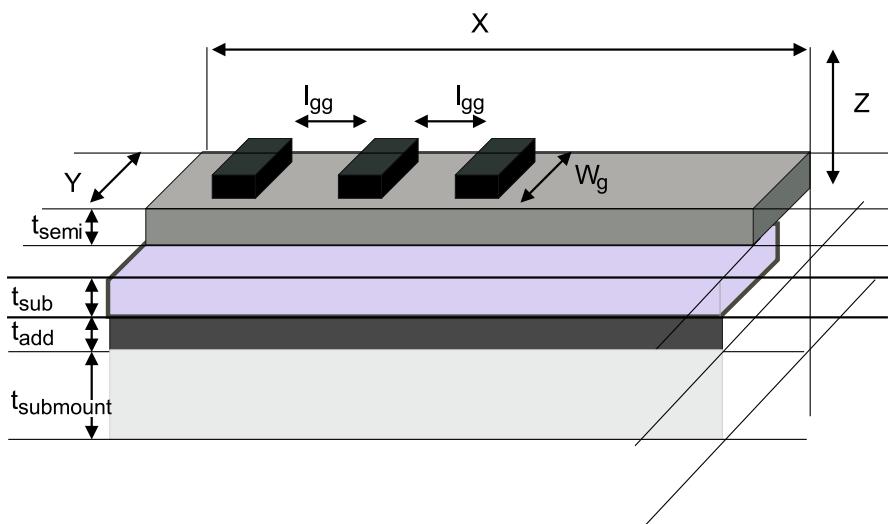


Fig. 8.11. 3D-view of thermally relevant parameters in an HPA

III-N semiconductors are again compiled in Table 8.1 with partial repetitions from Table 2.16. Examples of all relevant parameter values are mentioned, starting from the semiconductor materials, the substrate materials, the sub-mounts, and the adhesives and solders. III-N semiconductors require the development of new heat spreader materials such as copper tungsten, copper diamond, and copper molybdenum with high thermal conductivity, which have a coefficient of thermal expansion (CTE) matched to the typical substrate materials.

Apart from the thermal conductivity the actual choice of the submount material critically depends on the matching of the CTE to the substrate of the semiconductor. Fig. 8.12 gives the world map of packaging materials. Except from natural and synthetic diamond, which has a strong mismatch to SiC, only the composites Cu/W, Cu/Mo, and Cu–diamond yield the proper CTE and a good thermal conductivity suitable to match that of SiC. Most of the pure metals are rather off in CTE. Crystalline AlN is another choice.

Table 8.1. Temperature-dependent thermal properties of III-N semiconductors and packaging materials

	κ_{300} ($\text{W K}^{-1} \text{m}^{-1}$)	α (-)	c_{300} ($\text{J K}^{-1} \text{kg}^{-1}$)	Ref.
Si	125	-1.65	711	[8.104]
GaAs	54	-1.25	322	[8.86]
GaN	160	-0.43	491	[8.36]
AlN crystal.	285	-1.57	748	[8.110]
InN	45	-	325	[8.54]
Si_3N_4	0.96	-	-	[8.36]
s.i. SiC (V-doped)	330–370		715	[8.28,8.36]
6H-SiC	387	-1.49	715	[8.13]
High-purity s.i. SiC	490 c	-1.61	715	[8.22]
Sapphire	28	-1	796	[8.91]
Diamond	1,800–2,500	-1.85	520	[8.70,8.102]
Cu–W (25/75)	230	-	195	[8.25]
Co–Diamond	420, 650	-	-	[8.25,8.135]
Mo–Cu (70/30)	170–210	-	276	
Epoxy	1	-	1000	[8.91]
Silver-filled epoxy	1.9	-	-	[8.25]
Au–Sn	68	-	-	[8.25]
AlN (ceramic)	150	-1.84	770	[8.91]
BeO	250	-	-	[8.70]
Cu	383	-	385	[8.25,8.91]
Au	318	-	129	[8.36]

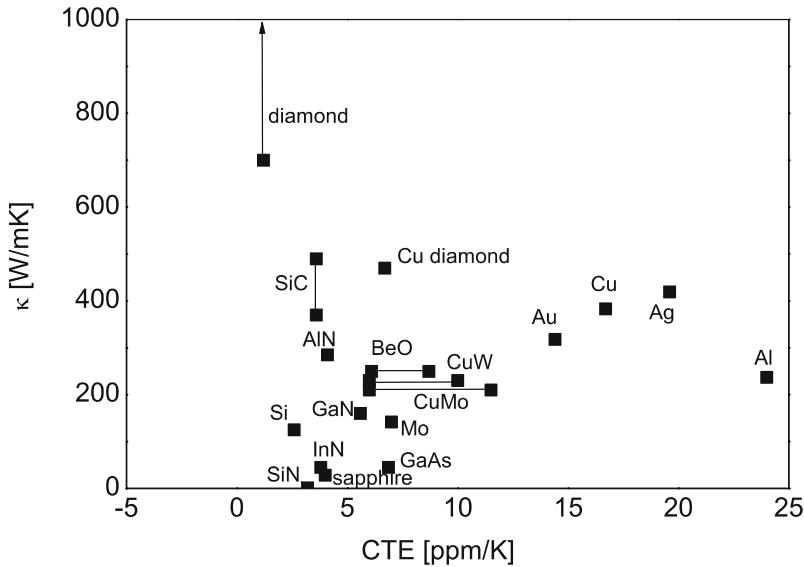


Fig. 8.12. Thermal conductivity as a function of coefficient of thermal expansion (CTE) at RT

Thermal Modeling of Semiconductors

Silicon is a reference for semiconductor materials [8.104] and also serves as a substrate material option for III-N devices [8.109]. The thermal properties of silicon are well investigated. Table 8.1 compares the thermal properties of the most important semiconductors with the properties of materials used in packaging and integration. GaN has a thermal conductivity very similar to that of silicon, thus, it is much better than the κ_{300} of GaAs. The low-temperature thermal conductivity of GaN between 4.2 and 300 K is given in [8.45]. AlN is available in various forms, either crystalline or ceramic. The high-thermal conductivity of the crystalline material is taken from [8.110]. Ceramic AlN is used in HTCC modules and various other substrate technologies, e.g., [8.75]. The thermal conductivity is lower than in crystalline AlN. However, the ceramic AlN still has a conductivity similar to silicon [8.91]. The properties of bulk InN are based on very few measurements only, e.g., [8.54]. InN is not available as a real bulk material, as the lattice mismatch to any substrate is significant. Ternary materials typically have much lower thermal conductivities than the binary semiconductors as measured for $\text{Al}_x\text{Ga}_{1-x}\text{N}$ in [8.64]. The composition dependent modeling is given in (2.8) in Chapter 2.

Modeling of Substrate and Submount Materials

The doping- and polytype dependence of the thermal conductivity of s.i. SiC is critical for precise analysis of the semiconductor substrate, as is pointed

out in [8.5]. High-purity SiC has a different thermal conductivity than (Va-) doped material, as mentioned in [8.5, 8.22, 8.94]. The thermal conductivity is further orientation dependent. Thermal and electrical conductivity and electrical properties of 6H-SiC are given in [8.5, 8.13]. The thermal conductivity is extracted between 300 and 500 K. Further, the thermal conductivity along the *c*-axis is found to be different from the conductivity along the *a*-axis [8.13, 8.36]. The mechanisms of the temperature dependence of the thermal conductivity of silicon carbide are discussed in [8.46] by theoretical separation of the limiting mechanisms. The impact of dislocations on the thermal conductivity at room temperature is mentioned. Dislocation densities of 10^8 cm^{-2} can significantly reduce the outstanding thermal conductivity of SiC to values of typical semiconductor material, such as GaN.

Diamond provides the best thermal conductivity of all materials with values of $1,800\text{--}2,500 \text{ W m}^{-1} \text{ K}^{-1}$, which is an order of magnitude higher than the typical semiconductors and metals [8.102]. CVD diamond has been used for topside heat spreading for high-power InGaP/GaAs HBTs [8.35]. The coating of GaN HEMT with industrial CVD diamond thus is discussed in [8.102]. A low-temperature CVD deposition process has been developed, which requires deposition temperatures $\leq 500^\circ\text{C}$. The reduction of the thermal conductivity for thin layers has to be considered in this case.

Diamond and copper-tungsten micro-packages are described for the integration of GaN HFETs in [8.90]. Both flip-chip and backside cooling with the HFET soldered to diamond are considered. Copper-tungsten has a thermal conductivity similar to AlN and also the CTE can be matched accordingly. Copper-molybdenum is a light material and used for the integration GaAs power MMIC into modules, e.g., [8.69].

The adhesive and submount materials mentioned in Table 8.1 are further discussed below with the packaging examples.

8.3.3 Basic Thermal Findings, Heat Sources, and Thermal Resistances

Basic dependencies of the DC- and RF-device parameters on temperature are given in this section.

Temperature Coefficients

Fig. 8.13 gives the heat dissipation for a power amplifier at a given drain efficiency $\text{DE} = 40\%$ as a function of the operation voltage. The absolute amount of dissipated power is as high as 200 W at $V_{\text{DS}} = 75 \text{ V}$, which means that such a device is thermally limited for a typical area of about $5\text{--}10 \text{ mm}^2$, see Fig. 8.8. The actual mounting situation will decide the channel temperatures.

Table 8.2 gives an overview of the temperature coefficients of device quantities on various substrates and mounting situations. The examples in Table 8.2 suggest that the temperature coefficients of the quantities in GaN FETs are

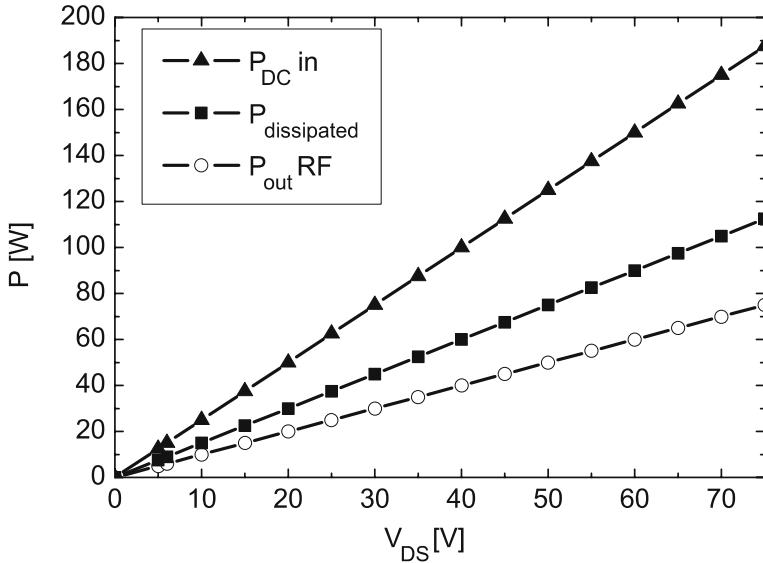


Fig. 8.13. DC-power, dissipated power, and RF-power as a function of V_{DS} operating voltage for an HPA at an assumed PAE of 40%

lower than for comparable GaAs PHEMTs [8.84]. However, as suggested in Fig. 8.8 and Fig. 8.13, the dissipated power levels and power densities per unit gate width and area are much higher than for the GaAs devices with a similar periphery, gate length, and area.

Table 8.2. Temperature coefficients of various HFET DC- and RF-quantities derived within the temperature ranges given

Substrate	Geometry $l_g \times W_g$ (μm)	Quantity	Coefficient	Range T_{sub} (K)	Ref.
GaN/SiC	0.35×250	I_{DSS}	$-14.8 \text{ mA mm}^{-1}/10 \text{ K}$	380–540	[8.84]
GaN/SiC	0.35×250	g_m	$-2 \text{ mS mm}^{-1}/10 \text{ K}$	380–540	[8.84]
GaN/SiC	0.35×250	f_T	$-0.24 \text{ GHz}/10 \text{ K}$	380–540	[8.84]
GaN/SiC	$0.35 \times 1,500$	P_{sat}	$-0.14 \text{ dB}/10 \text{ K}$	300–540	[8.84]
GaN/SiC	0.35×250	$N_{F,\min}$	$0.07/10 \text{ K}$	380–540	[8.84]
GaN/SiC	0.35×250	R_n	$2.6 \Omega/10 \text{ K}$	380–540	[8.84]
GaN/SiC	0.35×250	G_{ass}	$-0.114 \text{ dB}/10 \text{ K}$	380–540	[8.84]
GaN/SiC	$0.8 \times 2,580$	G_{ass}	$-0.23 \text{ dB}/10 \text{ K}$	316–573	[8.2]
GaN/SiC	$0.8 \times 2,580$	P_{sat}	$-0.06 \text{ dB}/10 \text{ K}$	316–573	[8.2]
GaN/SiC	0.3	g_m	$-5 \text{ mS mm}^{-1}/10 \text{ K}$	258–398	[8.2]
GaAs PHEMT	0.2	g_m	$-8.5 \text{ mS mm}^{-1}/10 \text{ K}$	233–423	[8.2]
GaAs PHEMT	1×150	g_m	$-12 \text{ mS mm}^{-1}/10 \text{ K}$	298–423	[8.18]
GaAs PHEMT	1×150	f_T	$-0.6 \text{ GHz}/10 \text{ K}$	298–423	[8.18]
GaAs PHEMT	1×150	P_{sat}	$-0.16 \text{ dB}/10 \text{ K}$	298–423	[8.18]

Thermal Resistances: Approximations

Thermal resistances express the global device temperatures once the dissipated power level is fixed. Several methodologies are available for the experimental and theoretical determination of the thermal resistances for a given mounting situation, e.g., [8.22, 8.36]. A closed-form determination of thermal resistance of GaN HFETs is presented in [8.22, 8.23]. The dependence on the layer thicknesses including host substrate, on the gate-to-gate pitch l_{gg} , on the gate length l_g , and on gate width W_g are considered and verified by finite element simulations. A simple analytical model is given in [8.36]. The thermal conductivities are calculated layer-wise in a column approach starting from the heat sources. This simplified procedure allows a construction of the thermal resistance within 10% of more elaborate simulations or measurements for the examples given. Input parameters are single-finger width W_g , gate-to-gate pitch l_{gg} , and number of gate fingers. This feature is useful if the heat spreading in the upper layers of the stack is sufficient to consider a 1D-problem. The particular influence of the thermal boundary resistance at the GaN/substrate interface to the performance degradation of GaN FETs is discussed in various publications, e.g., in [8.98, 8.118]. These findings are important, as this interface is typically optimized only with respect to electrical needs, such as isolation and dispersion requirements. A similar investigation of the effect of the thermal resistance at the GaN/SiC, GaN/sapphire, and GaN/AlN interface by simulation is provided in [8.33]. The diffuse mismatch approximation is used. The influence of the thermal boundary resistance is particularly important for the SiC substrate, which conducts the heat very well. For SiC, the relative contribution of the boundary to the overall thermal resistance for SiC is higher than for sapphire substrates. Experimental confirmation for the increase of the thermal resistance is provided in [8.98]. Conformal micro-raman thermography is used to determine the temperature at different depths within the device. Full 3D-models based in finite element method will be discussed below with the applications examples.

Self-Heating

Self-heating is the source of channel temperature increase, due to the enormous power levels per dye area in III-N devices. The limiting effects will now be discussed. 3D-thermal simulation of SiC MESFETs coupled with 2D-electrical simulations are reported in [8.10]. It is clearly shown in [8.10] that the heat transfer problem is a full 3D-problem. Thus, thermal effects are included in the simulation for comprehensive device optimization. Power handling limits and degradation of large area AlGaN/GaN RF-HEMTs on sapphire and SiC are discussed in [8.26] based on 3D-thermal simulations. The RF-output power density is correlated with the thermal impedance R_{th} of the device on SiC. The RF-power density reduces nearly linearly from 4 to 2 W mm^{-1} for a increase of R_{th} from 10.5 to 14.5 K mm W^{-1} . The dependence of the thermal impedance R_{th} on gate-gate pitch l_{gg} is discussed for various gate widths W_g .

from 50 to 200 μm . For all gate widths, the thermal impedance reduces by 30% for the variation of the pitch from $l_{\text{gg}} = 20$ to 100 μm . Initial findings on dynamic properties of self-heating in high-power AlGaN/GaN HFETs on sapphire and SiC substrate are discussed in [8.38]. The DC-output characteristics are affected by the self-heating effects after less than 10^{-7} s. After 30 ns during the pulse period there is no reduction of the current with V_{DS} visible on s.i. SiC substrates. On sapphire substrates the thermal impedance is nearly an order of magnitude higher which leads to a higher thermal constants. It is further shown that the thermal impedance of the AlGaN/GaN HFET is mainly affected by the substrate material, as the active semiconductor layers are only about 1.5 μm thin.

Device Optimization Strategies

Device parameters are typically varied with regard to electrical performance. Based on the previous sections, potential thermal parameters for device optimization include:

- Variation of the single-finger length [8.22]
- Variation of the gate–gate spacings or pitch, typically between 20 and 100 μm [8.22, 8.83, 8.109]
- Optimization of the thermal interface from the substrate backside to the metal
- Increase of the chip area and optimization of the distribution of the devices on the chip
- (Microstrip) substrate thickness variation between 400 and 50 μm [8.109]

Minor thermal impact have:

- A variation of the gate lengths [8.22]
- A variation of the semiconductor layers thicknesses, e.g., the buffer layer between 0.5 and 3 μm

These thermal parameters similarly have a strong impact on the electrical performance, so trade-offs need to be evaluated comprehensively and thus examples will now be given.

8.3.4 Backside Cooling

Various mounting techniques have been proposed for semiconductor devices, and very innovative cooling concepts may be required for III-N devices. However, backside cooling is a very good reference for the understanding of the thermal situation. General comparisons of thermal impedances of GaN devices on sapphire, s.i. SiC, and silicon substrates for backside cooling are provided, e.g., in [8.28, 8.58]. GaN HEMTs on s.i. GaN substrates have not been analyzed extensively; however, the thermal situation is very close to the situation of GaN on silicon.

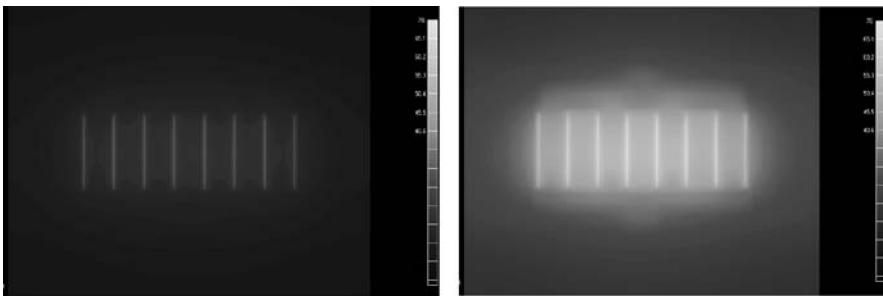


Fig. 8.14. Thermal image of a multifinger FET on SiC (*left*) and sapphire (*right*) substrate, unit (K W^{-1})

Silicon Carbide Substrates

SiC is the material with the highest heat conductivity relative to all other substrate choices except from diamond [8.102]. SiC has some unique properties. Its heat conductivity is approximately metal-like, e.g., compared to Cu or Au, see Table 8.1, [8.13, 8.22, 8.46]. Thus, the heat-spreading properties of a SiC substrate are very good and some thermal arguments known from GaAs or Si need to be revised. Contrary to GaAs and Si, thinning of SiC to 100 or $50\text{ }\mu\text{m}$ does not necessarily improve the overall thermal situation, as explained for diamond and SiC in [8.5, 8.136]. This is only the case if the thermal resistivity of the submount is better than of the SiC substrate. Further, thinning introduces a thermal barrier closer to the active device and may reduce the heat spreading, as the die-attach typically has thermal properties inferior to SiC. Thermal limitations on large-periphery SiC MESFETs, which have a thermal situation similar to GaN HFETs, are discussed in [8.123]. Maximum channel temperatures of 320°C are reached for a device with $W_g = 36\text{ mm}$ gate periphery and 144 gate fingers with $250\text{ }\mu\text{m}$ single-finger gate width. Substrate thickness is $400\text{ }\mu\text{m}$ and the dissipated power $P_{\text{diss}} = 58\text{ W}$. The gate-to-gate pitch l_{gg} is not given.

Infrared and Raman temperature measurements on AlGaN/GaN HFETs on 4H-SiC substrate are given in [8.55, 8.56, 8.96]. The results show operation temperatures of 160°C near the gate finger at a power dissipation level of 20 W mm^{-1} in a $2 \times 50\text{ }\mu\text{m}$ device on a $400\text{ }\mu\text{m}$ -thick SiC substrate. The gate-to-gate pitch is $l_{\text{gg}} = 50\text{ }\mu\text{m}$ and the device is glued to a heat sink with epoxy with a contact area of 15 mm^2 . Such measurements can be used effectively to calibrate the simulated temperature distribution to the real world, typically by means of the assumptions made for the heat source in the simulation. Fig. 8.14 depicts the temperature distribution in a multifinger GaN HFET for both SiC and sapphire substrates. The color code is given on the same scale for the $W_g = 1\text{ mm}$ device with eight fingers. The maximum impedance is 20 K W^{-1} for the SiC and 69 K W^{-1} for SiC for the same substrate thickness. A crucial issue of the thermal simulation is to make sure that the substrate

thickness t_{sub} is greater than the gate-to-gate pitch l_{gg} . If this is not the case, the thermal distribution will be very strongly affected by the boundary condition at the substrate/heat sink interface.

Sapphire Substrates

Careful thermal management for any electronic III-N device is of even greater importance on sapphire substrates, due to the limited thermal conductivity, which is even lower than that of GaAs (see Table 8.1 and Fig. 8.14). Despite the great Vickers hardness, substantial substrate thinning from typically 250–325 μm [8.130] is a requirement. The determination of the channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using a DC-characterization method is presented in [8.58]. A simple estimate of the channel temperature is given based on the threshold voltage shift and the change of the source resistance with temperature. The channel temperature T_{chan} is then derived from the reduction of the drain current with V_{DS} . For a device with $l_{\text{g}} = 0.45 \mu\text{m}$ and $W_{\text{g}} = 50 \mu\text{m}$, a channel temperature $T_{\text{chan}} = 320^\circ\text{C}$ is extracted for sapphire, while only $T_{\text{chan}} = 95^\circ\text{C}$ are extracted for Si substrate. This ratio is a bit too high and reflects some error introduced by this purely electrical method. Thermal findings for GaN HFETs on sapphire substrate further include:

- Thinning of the sapphire substrate to 50 μm , as used for 100 W power operation in a 2 GHz power bar [8.4]
- Generally high-absolute thermal impedances that lead to very high operation temperatures

If we consider only backside cooling, sapphire limits the application of AlGaN/GaN HFETs on sapphire to DC-dissipation power-densities approximately similar to those of GaAs for the same substrate thickness of 50 μm . For other mounting situations, such as flip-chip, sapphire can be a solution, as discussed, e.g., in [8.115].

Silicon Substrates

As a substrate material silicon has a thermal conductivity similar to that of the semiconductor GaN. Thus, it is well suited for power operation; however, it does not supply the same good heat spreading as SiC substrates. Further, the compensation of the high-lattice mismatch introduces an additional heat barrier near the substrate interface. GaN HEMTs on silicon substrates for wireless infrastructure applications are described in [8.109], featuring thermal design and related performance. A good comparison is given for the same nominal device, in this case a $10 \times 200 \mu\text{m}$ device with a gate-to-gate pitch of 25 μm , but with different substrate materials. For the power density of 3 W mm^{-2} , the idealized ratio of the temperature increase is 160 to 75 to 50 K for the comparison sapphire vs. silicon vs. SiC substrate for a base plate temperature of 300 K. The comparison of the thermal impedance is given below. Direct

on-wafer noninvasive thermal monitoring under microwave large-signal conditions are reported in [8.83] for similar GaN HFETs on silicon substrates. A comparison is performed between various ten finger devices with gate finger length of 100, 200, 300, and 400 μm . The gate-to-gate pitch is relaxed from 20 and 50 μm to obtain similar temperatures for the larger devices. The surface temperature observed for the GaN HFET with $W_g = 3 \text{ mm}$ by IR thermography varies between 120 and 200°C simply based on the change of the PAE during the power sweep. The silicon substrates are thinned to 150 μm in this case. This is thicker than for state-of-the-art silicon LDMOS substrates, which are typically thinned to thicknesses below 100 μm .

Comparison of the Substrates

The results for the thermal impedances of the backside cooling for III-N devices on various substrates are compiled in Table 8.3.

The comparison yields the best thermal resistance per unit gate width W_g for SiC, followed by silicon and sapphire. For the flip-chip integration, the thermal resistance is nearly independent of the substrate material. The variation of the results on sapphire substrate from [8.26] is due to a variation of the gate-to-gate pitch l_{gg} between 20 (highest impedance) and 100 μm (lowest impedance).

8.3.5 Flip-Chip Integration

Flip-chip integration is a technology for use in hybrid mounts in several semiconductor technologies, such as silicon [8.53] and GaAs [8.78]. Flip-chip integration of power HEMTs on GaN/SiC technology is discussed in [8.103]. Both

Table 8.3. Comparison of the substrate and mounting configurations

Substrate	Thickness (μm)	Gate width (mm)	Configuration	Impedance	Ref.
SiC	400	1	BS	17 K W^{-1}	[8.94]
SiC	300	0.2	BS	$4\text{--}5 \text{ K mm W}^{-1}$	[8.26]
SiC	100	2	BS	22 K W^{-1}	[8.109]
Sapphire	–	1	BS	65 K W^{-1}	[8.94]
Sapphire	–	0.1	BS, diced	51.7 K mm W^{-1}	[8.115]
Sapphire	300	0.2	BS	$50\text{--}90 \text{ K mm W}^{-1}$	[8.26]
Sapphire	100	2	BS	53 K W^{-1}	[8.26]
Silicon	100	18	BS	$4.25\text{--}4.75 \text{ K W}^{-1}$	[8.109]
Silicon	100	2	BS	37 K W^{-1}	[8.109]
SiC	400	0.1	FC	4.9 K mm W^{-1}	[8.94]
Sapphire	–	1	FC	25 K W^{-1}	[8.94]

BS backside, *FC* flip-chip

electrical and thermal gold bumps are available. In this technology, thermal bumps are used directly within the active devices to remove the heat. Very initial large-periphery AlGaN/GaN MODFETs on sapphire mounted by flip-chip integration are reported in [8.117]. The effect of the thermal improvements by flip-chip bonding is proven by increases in the saturated currents I_{DSS} . Thermal management of AlGaN/GaN HFETs on sapphire substrate using flip-chip bonding with epoxy underfill is described in [8.115]. The passive integration is performed on AlN substrates using gold bumps. The impact of the sapphire substrate to the thermal resistance is found to be reduced, and the heat spreading within the GaN buffer is found to be significant. In this case, a reduction of the thermal impedance of the GaN buffer layer is suggested to optimize performance. Very high RF-power densities of $\geq 5 \text{ W mm}^{-1}$ on sapphire can be reached with small device and by flip-chip integration of GaN devices with a gate width $W_g = 2 \text{ mm}$, as reported in [8.129]. A comparison of conventional and flip-chip bonding of AlGaN/GaN devices by photocurrent measurements is given in [8.94]. The technique allows an absolute temperature calibration of thermal simulations. The thermal resistance for backside-cooled GaN HFETs on sapphire amounts to 65 K W^{-1} , for flip-chip bonding on sapphire to 25 K W^{-1} , and to 17 K W^{-1} for backside-cooled SiC, as also shown in Table 8.2. The gate periphery is $W_g = 10 \times 100 \mu\text{m} = 1 \text{ mm}$. As an example,

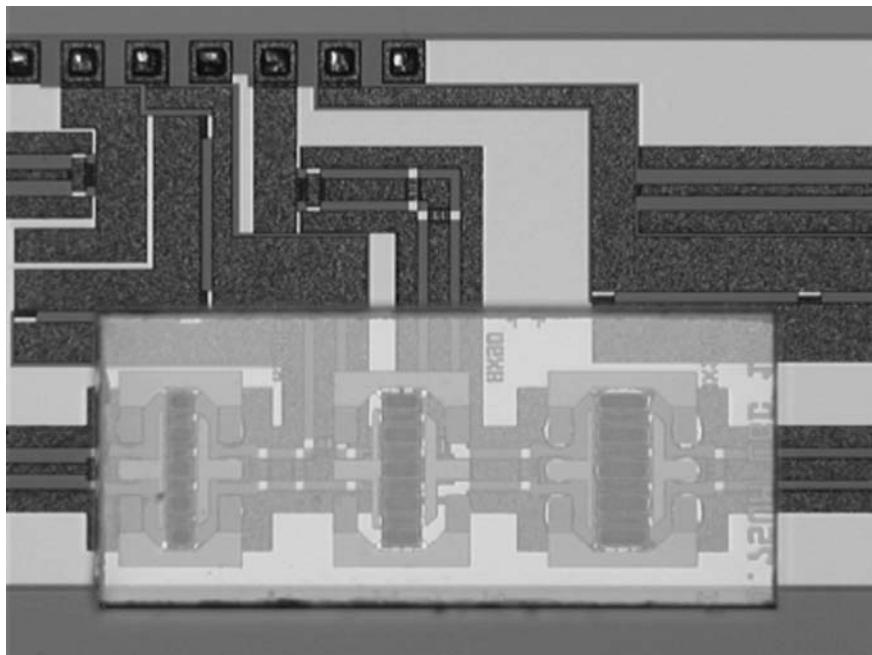


Fig. 8.15. Transparent GaN HEMTs flip-chip mounted on a passive coplanar carrier substrate

Fig. 8.15 gives the image of a GaN HEMTs on s.i. SiC substrate, which is integrated on a passive carrier substrate in coplanar transmission-line technology using gold bumps. The transparent SiC substrate is clearly visible and the bumps between the gate fingers can be seen from the top through the substrate.

Combined Integration Techniques

Even a thermal impedance of 17 K mm W^{-1} for ideally backside-cooled GaN HFETs on SiC may yield high channel temperatures for high-power operation. Thus, the combination of several techniques is discussed by various authors. Fig. 8.10 suggests a combination of frontside and backside cooling. This methodology is the most powerful option; however, at the same time it requires the highest integration effort, and a very careful adaption of the thermal coefficients of expansion is needed. A combination of flip-chip packaging and backside cooling has been suggested for GaN HFETs by RFMD in [8.105] with respect to thermal management for very high-power density operation. The thermal impedances in this case are strongly dependent on the actual thermal path to the heat sink, since isothermal heat sinks cannot easily be realized close to the device on both sides of the devices. A typical integration procedure for such an approach is a backside cooling combined with a flip-chip or ball grid array type of top substrate, as performed for silicon microprocessors [8.6]. Apart from combined flip-chip/backside integration, surface heat conductivity of dielectric material on top of the device can be used. CVD diamond has been proposed as a surface layer [8.102]. It is found that the thermal conductivity of a CVD diamond layer is higher than that of gold, even for very thin diamond layers with only $2\text{ }\mu\text{m}$ thickness.

8.3.6 Dynamic Thermal Effects

The dynamics of thermal processes are highly complex [8.59]. The main issue for thermal management is the determination of the appropriate relaxation mechanisms to describe nonconstant device excitation, compare (5.100) in Chapter 5. The dynamic behavior of device is characterized by complex geometries, temperature dependent material properties, and variations on various orders on spatial and temporal scales [8.127]. For large-scale thermal simulations this complex behavior of the devices is typically reduced to one or two time constants.

Values for the thermal relaxation time constant of the order of 10^{-7} s are mentioned for the thermal relaxation in [8.38]. Similar time constant of 190 ns are reported for AlGaN/GaN HEMTs on silicon [8.57]. These time constants have to be extracted along with the thermal resistance. For the long-term behavior of the thermal response a steady-state thermal behavior is assumed after 20 ms in simulations of silicon devices at low temperatures [8.59]. According to (5.100) the heat capacity becomes the second dominating

material parameter, which is thus compiled in Table 8.1. It can be seen that the heat capacitances of the substrates of choice (SiC, sapphire, and silicon) are very similar. The heat capacitances of the actual semiconductor layers are not considered very important for the optimization, except for the optimization of the overall semiconductor thickness.

The input RF-drive-dependent temperature change of a GaN HFET is monitored by thermal imaging in [8.83]. The thermal distribution is found to be highly fluctuating with time, although steady input power levels are applied. Dynamic thermal effects under pulsed-DC-operation are further discussed in [8.82]. No time constants for the relaxation are given. The impact of the substrate choices sapphire and silicon for GaN HEMTs on the maximum dynamic temperature in pulsed operation is investigated by simulation in [8.131]. The typical analysis for pulsed operation is given for a very high power device in [8.73]. IR images are given for various pulsed widths. Further both power droop of -0.3 dB and phase droop of -3.9° are measured for pulse widths of $200\text{ }\mu\text{s}$ for radar operation.

8.4 Device and MMIC Packaging

Packaging is a critical step for the integration of devices on the hybrid-package and module level. The integration typically includes:

- Wafer dicing
- Die-attach and related void control [8.66]
- Electrical connection including DC- and RF-substrate technology
- Cointegration [8.77]
- Oscillation control
- If needed, hermetic sealing

These steps will now be analyzed in detail for III-N devices.

8.4.1 Dicing

Semiconductor wafer dicing is typically performed by sawing, scribing, cleaving, or by the application of various laser techniques.

Sawing and Scribing

Sawing [8.16] or scribing of GaAs wafers are the typical cost-effective procedures for wafer dicing in industry [8.21,8.122]. Typical issues of dicing are the reduction of ragged edges and gold burrs. Optimization strategies for sawing thus include proper blade selection leading to increased lifetime of the blade. The cutting speed and yield of sawing is not as good as with other dicing techniques. For SiC, sawing is the technique of choice [8.112], whereas sapphire is either diced by a combination of thinning, scribing, and subse-

quent cleaving [8.87], e.g., for optoelectronics, or the substrate is structured or removed by laser lift-off [8.24]. The optimization of scribing includes the stabilization of the tool quality for improved repeatability for high-volume production. For wafers thinner than 150 µm, dicing in general becomes more difficult, e.g., [8.88].

Laser Techniques

Laser dicing techniques are attractive due to the lack of direct physical contact of the tool components with the die. This results in reduced tool wear-out [8.40]. A water-jet-guided laser is suggested for optimized laser cutting of GaAs in [8.88]. In this case, a wavelength of 1,064 nm at 100 W of power is used. The water jet serves as a waveguide and helps to remove debris during the dicing process. UV-laser-assisted scribing of sapphire is discussed in [8.41]. This technique at a wavelength of 255 nm is used to scribe sapphire wafers of 100 µm thickness for III-N LEDs production. Very precise edges are possible with small cuts [8.87]. The technique is presented to overcome the lack of etch techniques for sapphire. A water-jet-guided laser is used for the damage-free dicing of SiC in [8.40]. A 1,064 nm at an average power of 56 W is used with a 40 µm thick water jet. The cutting speed for 380 µm thick substrates can be improved by about 40% relative to sawing. The technique can also be used to scribe SiC wafer with the application of a 532 nm laser and 23 µm thick water jet. Further, the edge quality is improved while the tool does not wear-out, due to the contact-free dicing procedure.

Impact of Dicing

In case of heteroepitaxy and of the lattice mismatch with the substrates, III-N layers have a defined bow after epitaxy, e.g., [8.85]. The pressure dependence of the conductivity in AlGaN/GaN HEMT is investigated in [8.47]. This is important, as the strain is modified on the chip level during dicing. The conductivity in the channel of an AlGaN/GaN HFET shows a linear change of 6.4×10^{-2} mS bar⁻¹ through the application of compressive strain. A similar investigation gives a change of the capacitance 0.86 pF bar⁻¹ for a membrane with a radius of 600 µm for both tensile and compressive strain. This is a strong dependence for an area which is similar to an FET, and the capacitance change is of the order of the total capacitance of an FET with $W_g = 1$ mm. This fact requires a strong control of the dicing changes in III-N devices and MMICs.

8.4.2 Die-Attach

The die-attach is the most important integration step of electronic devices, mostly for thermal reasons. It is composed of a positioning in all three directions (which shall not be discussed here) and an attach step. Several attach processes are available based on either solder or glue processes, e.g., [8.122].

An eutectic solder attach is used in [8.109] for the integration of GaN HEMTs on silicon substrates with an eutectic thickness of $25\text{ }\mu\text{m}$. The die is soldered to a Cu/W package with a thermal conductivity $\kappa = 180\text{ W m}^{-1}\text{ K}^{-1}$. This is a relatively thick eutectic layer, which strongly increases the thermal resistance of the stack. The optimization of the backside metal layer stack is also a subject of GaAs-based backside processes, e.g., [8.21, 8.122]. This includes:

- Precleaning wafer backside [8.21]
- Selection of layer sequences in the die-attach
- Selection of layer thicknesses
- Void reduction

Thermomechanical analysis of gold-based SiC die-attach assembly is described in [8.72]. Again, it is mentioned that the differences in CTE leads to strong mechanical stress to the mounted die, in this case a MEMS pressure sensor. The analysis of the die-attach allows proper compensation of the stress. Void control is typically achieved by removing the semiconductor and optically inspecting the eutectic. Void control of the die-attach can also be performed by thermal imaging, by acoustical microscopy, as performed and reported in [8.66], or by X-ray. Shear tests are performed to investigate the mechanical strength of the bonding. The impact of single voids on the associated temperature increase have been investigated for LDMOS devices, as reported, e.g., in [8.48]. The thermal resistance of the die-attach/solder layer is approximated in a 1D-approach as

$$R_{\text{th}} = \frac{t_{\text{ad}}}{\kappa A}. \quad (8.1)$$

Some thermal conductivities, typical thicknesses of the substrates, die-attach layers, and submount materials relevant to III-N devices are given in Table 8.4. Indium-based solder is typically not suitable for high-power operation, as the melting point of Indium is too low. AuSn solder is a typical die-attach for high-power semiconductors, e.g., [8.122]. Table 8.4 allows a relative comparison of the contributions to the thermal resistance per mm^2 assuming purely 1D-heat transport. It can be seen that the typical solder or glue layers have a critical impact on the overall thermal resistance of the stack. The optimization of the solder includes:

- Metal-material, temperature, and composition selection
- Metal thickness optimization
- Metal stack deposition [8.122] including:
 - Adjustment of the layer thickness to the leaching of Au
 - Solder stop integration to avoid via filling [8.122]
- Backside street integration

After optimization, the thermal conductivity of the eutectic can reach values in the same range as the semiconductor materials. Several effects have to be considered additionally. The so-called via blow-out, i.e., the filling of vias by the solder, is avoided by a stop layer. Such a layer directly develops an oxide,

Table 8.4. Comparison of thermal conductivities for typical materials for packaging

Material	Thickness (μm)	κ_L (W m ⁻¹ K ⁻¹)	Thermal impedance per mm ² (K W ⁻¹)	Ref.
GaN	3	130	0.023	–
SiC	100	370	0.27	–
Silicon	100	150	0.66	–
Sapphire	50	50	1	–
AuSn	20	240	0.083	[8.36]
AuSn	25	–	–	[8.109]
AuGe	20	90	0.22	[8.109]
Epoxy	20	30–60	0.66–0.33	[8.36]
Silver epoxy	20	1.6–7.5	12.5–2.6	[8.36]
Cu–W	1,000	400	2.5	[8.36]
Cu–W	1,500	180	8.3	[8.109]

such as Ti, Ni, and Cr, as reported in [8.122]. Specifically for high-temperature operation, a die-attach scheme for silicon carbide for high-temperature operation at $T_{\text{sub}} = 500^\circ\text{C}$ is reported in [8.17]. SiC diodes are attached to AlN substrates and packages by a specific metal attach scheme.

8.4.3 Package Technology Selection

The selection of the package has a strong impact on the device performance with respect to the system integration. Several optimization steps have been performed on the packages themselves, e.g., [8.70, 8.108]. General aspects of the packaging selection and optimization of hybrid transistors and MMICs include:

- Improved heat removal [8.66, 8.70]
- The need for sealing [8.126]
- The reduction of electrical losses, inductance, and capacitance [8.70]
- Cost reduction [8.62, 8.108]

Recent trends of integration with respect to III-N hybrid devices include:

- Cost reduction of conventional package technology in hybrid integration schemes [8.62]; this includes:
 - Introduction of new organic/plastic technologies replacing ceramic packages [8.1, 8.108]
 - Size reduction [8.128] and increase of packaging efficiency, i.e., reduction of the ratio of package area and semiconductor area [8.27]
- Integration of a number of chips per package [8.14, 8.108]

Initial GaN HFET examples for base station applications have mostly been realized in conventional ceramic packages, e.g., [8.77]. However, ceramic packages are being replaced by organic packages for the competitor LDMOS [8.108]. Recent trends show a similar integration schemes also for GaN HEMTs for base station applications in order to meet similar cost trends [8.116]. For higher frequencies and MMIC integration, [8.27] shows the historical evolution from hybrid transistor integration to multichip MMIC modules and micropackages. Conventional multichip-modules (MCM) concepts are currently applied, as also mentioned for space applications in [8.7]. Low-temperature-cofired-ceramics (LTCC) packaging is a conventional technique of choice, which is used in a variety of module applications, e.g., [8.62]. LTCC-technology is considered to be not very flexible and only cost effective at large production numbers. Further, larger line sizes and tolerances have to be taken into account [8.100]. Several approaches have been pursued to overcome these limitations, e.g., [8.62]. Cost reduction of the LTCC approach can also lead to the use of high-temperature cofired ceramics (HTCC) [8.128], in this case a single 12-layer package. An X-band multichip module including several PA and switch MMICs and ASIC are integrated. HTCC-based MCM packages are typically based on AlN dielectrics and can be used up to 60 GHz [8.75]. The packaging trends further pursued are based on the following technologies:

- Integrated multilayer ceramics modules such as
 - Low-temperature cofired ceramics (LTCC) for frequencies up to 76 GHz [8.7, 8.100, 8.137]
 - High-temperature co-fired ceramics (HTCC) [8.19, 8.128]
 - Photonic bandgap structures [8.137]
- (On the medium timescale) the introduction of
 - System-in-package (SIP) technology [8.7]
 - 3D-integration, as proposed in [8.89, 8.90, 8.132]

An example of the realization of a photonic bandgap structure is given in [8.137]. The LTCC and flip-chip integration of a GaAs MMIC approach is combined with the suppression of undesired modes between the chip ground-plane and the module ground through the use of periodic structures. The SIP approach integrates multiple components, such as GaAs HEMTs, on a high-density interconnect substrate, as performed in [8.121]. TaN and MIM capacitors are cointegrated with GaN HEMTs on AlN passive substrates.

A full 3D-integration of LTCC substrate including μ -ball grid-array (BGA) technology for the stacking on the motherboard is described in [8.90]. A full C-band transceiver including mixer, LNAs based on GaAs MESFET can be integrated by the application of this approach. The LTCC substrates are connected by μ -ball grid-array. Fully 3D-micro-electromagnetic systems (3D MERFS) are described for the integration in [8.31]. The idea of MERFS is based on the fact that there is no millimeterwave analog to the printed circuit board (PCB). Low cost-materials are used to decrease size and weight by an

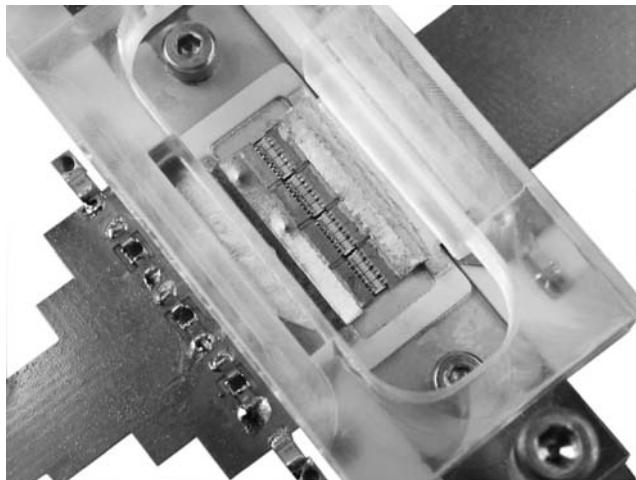


Fig. 8.16. Packaged GaN HEMT in standard ceramic housing

order of magnitude. About 1000 passive conductors and RF-components can be integrated in one substrate.

Thus parallel to the development of the active III-N devices high-performance passive module technologies are being developed increasing packaging density and isolation and line losses at the same time. These integration schemes will be used to integrate GaN RF-devices in future systems.

8.4.4 Thermal Management for Linear Applications

Thermal management is especially critical for linear RF-operation, as linear RF-operation is characterized by high back-off from the highly-efficient saturation point. Thus, the associated efficiency of the operation is much lower than in saturated operation, which leads to increased DC-dissipation and heat generation within the device, see [8.83]. The high-power densities per area of GaN devices aggravate the problem in linear operation, see Fig. 8.8.

Example of a Hybrid AlGaN/GaN HEMT on s.i. SiC

Stages of a base station amplifiers are typical examples for highly linear amplifier [8.77]. The integration task is very similar to the integration of silicon LDMOS or GaAs power FETs for the same application. The typical engineering tasks include:

- Thermal expansion coefficient matching [8.109]
- Bond wire engineering, as described, e.g., in [8.15, 8.70]
- Flange engineering for electrical connection [8.70]
- Cosubstrate integration [8.70]

The integration of a GaN HEMT with a periphery $W_g = 32\text{ mm}$ in a ceramic package is shown in Fig. 8.16. The die is soldered with a AuSn eutectic to a Cu/W submount in a typical LDMOS package. The bonding approach is based on wire bonding in this example and includes no intentional pre-matching. This allows unrestricted broadband and multiband operation. Pre-matching of GaN FETs has also been suggested, e.g., in [8.77]. The internal matching provides input and output impedances of $3-j\ 4\Omega$ at 2.14 GHz for two $W_g = 36\text{ mm}$ GaN HFETs on silicon substrates, integrated in parallel into one ceramic package with single flanges. From a thermal point of view, both eutectic and gate-to-gate pitch l_{gg} have been optimized. The biasing of the transistor is still limited to deep class-A/B in order to reduce the quiescent current I_{Dq} and the associated dissipated power P_{diss} . Further, analog and digital predistortion enable the improvement of both peak and average output power and associated efficiency for given ACLR constraint.

GaN MMIC Integration

GaN MMIC integration includes the following issues, similar to power FET packaging:

- Heat spreading in a limited area
- Individual RF-connection
- Individual DC-connection
- Oscillation control within the cavity of the package [8.37]

The optimization starts on the device level. Specific MMIC-design procedures for the reduction of module costs are given, e.g., in [8.8]. This typically includes size reduction of the MMICs, higher integration with more elaborate passive components, and more compact and thus more risky transmission-line positioning. The latter requires very stable technologies and longstanding design experience on the specific process. MMIC packages are available in several forms as multichip hybrid modules [8.7]. This technology integrates microwave components, RF-feedthrough, and DC-bias/control functions. The multichip modules can be realized in various packaging technologies. Low-cost surface mount device (SMD) packages based on organic materials are available, e.g., in [8.37, 8.119]. They can be used up to frequencies of 40 GHz and even 60 GHz for GaAs FET technologies. The integration requires less than 1 dB of gain at the frequency of 40 GHz . The connection to a printed circuit board (PCB) is critical, and the losses can be minimized to $\leq 0.5\text{ dB}$ at 60 GHz [8.37]. Alumina-based ceramic MMIC packages have been introduced for frequencies up to 40 GHz [8.114]. The package has an air cavity and is leadless. An example of the integration of a coplanar Ka-band driver GaN MMIC on s.i. SiC is depicted in Fig. 8.17. The module is realized in conventional split-block technology. The MMIC is integrated on a subcarrier which is CTE-matched to s.i. SiC. The eutectic solder requires specific optimization with respect to void control and thickness. The DC-supply and DC-oscillation

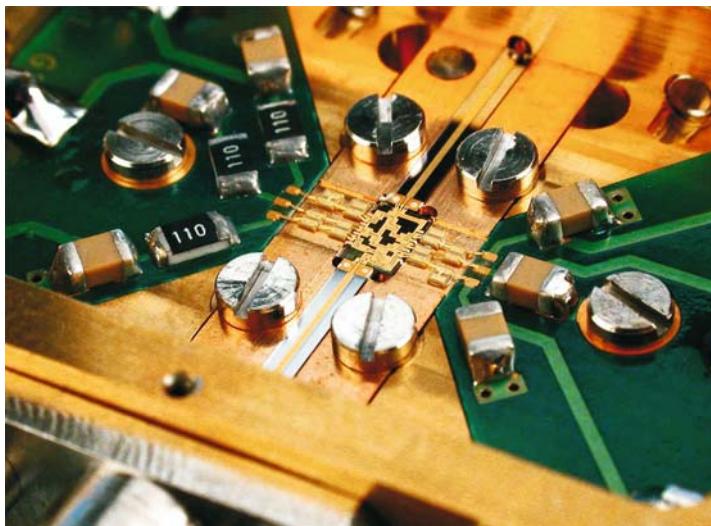


Fig. 8.17. Integrated GaN HEMT Ka-Band driver MMIC in a conventional split-block module

mitigation require new, area-efficient SMD components, which need to support the high-operation bias $V_{DS} = 30\text{ V}$. The module is thermally limited in cw-operation due to the backside cooling. The MMIC requires a quiescent current $I_{Dq} = 150\text{ mA mm}^{-1}$ for suitable gain at Ka-band frequencies, which leads to a power dissipation $P_{diss} = 4.5\text{ W mm}^{-1}$ at $V_{DS} = 30\text{ V}$ for linear communication applications. Both the transition from the coplanar MMIC to the microstrip lines and the submount are visible in Fig. 8.17. Further, the integrated DC-control is visible.

8.4.5 Active Cooling

One basic finding from the previous sections is the thermal limitation of III-N hybrid and MMIC devices, see Fig. 8.8. The thermal limitation of electronics through thermal limitation is already mentioned in [8.138]. Thus, both advanced thermoelectrical cooling layers and embedded microchannel cooler concepts are suggested for the solution of this issue. SiC and silicon are relatively good heat spreaders, so active cooling techniques gain importance for III-N devices.

Thermal management of electronic devices using microchannels enabling local active cooling is described in [8.61]. 3D-microsystem structures are used to build 3D-microfluidic channels near the thermal hot spots of the electronic device. As another option, thermoelectric microcoolers for GaN FETs are described in [8.34]. The idea of microcoolers is to actively cool only the key power devices. Materials such as CVD diamond and AlN are used as substrates for the microcoolers. GaN is suggested to be the material to change

the typical heat dissipation per area of an integrated GaAs device from currently 30 W cm^{-2} (0.3 W mm^{-2} , see Fig. 8.8) to several hundreds W cm^{-2} ($1\text{--}10 \text{ W mm}^{-2}$) for GaN HEMTs with 20 W of output power. This range of power densities is also reached if we consider either the active area or the full chip size as a reference area. New concepts of internal device cooling are also considered. Internal thermoelectric cooling of laser diodes is described in [8.92]. The thermionic effect at the interfaces is used to cool the device. This principle is attractive, since this cooling occurs in or very near the hot spot active region. The procedure is suggested for electronics in [8.138].

8.5 Problems

1. Compare the thermal properties of microstrip and coplanar transmission-line approaches of conventional GaAs FETs to GaN FETs on s.i. SiC.
2. Which mechanical material properties are important for the reliability of flip-chip packaging?
3. What is the principal difference between GaN on SiC substrates and other semiconductors for integration?
4. What is still the main drawback of 3D-integration? Think of both material and economic issues.

Outlook

After about 16 years of outstanding progress in research and development, the challenging III-N material system is about to emerge into the open waters of system introduction. Some great achievements have been made, and others are yet to come: we will see higher operation frequencies, greater wafer formats, still higher output powers, and great results in linearity, efficiency, and bandwidth. However, as the experience of the GaAs devices has proven, a long way is still ahead until full use of material capabilities in subsystems and systems is achieved. Disappointments occur and will continue to arise due to reliability problems on the system level, especially since the proposed high-voltage operation has not been tested on the system-level so far. Further, new mechanisms of degradation at the proposed output power levels will be important, and extremely careful optimization will be necessary to sort out the details. Disappointments will also occur for industrialization, as the emerging markets will not be able to support all business plans. Schumpeter's law of the rise and fall of innovators and competitors will play a dominant role.

In the long run, great progress will be achieved especially for MOD systems in new radars, new electronic countermeasures, and there will be new means in communication and several other civil and military niche applications.

Civil applications in mobile communication will be seen; however, the everlasting silicon is driving down a roadmap of cost reduction at a pace never seen before, and though being technically inferior for some applications, it will keep its share. New applications for 3G and 4G communication systems will be technically possible; however, again the market, customer preferences, and cost issues will decide whether they will evolve. Some great lessons will be learned from the optoelectronic world, where the rise of III-N-based solid-state lighting will lead to a continuous development of materials, substrates, and technologies pushed by a strong consumer market. In an analogy, III-N optoelectronics will challenge the light bulbs, while III-N electronics will challenge the electronic equivalent, the tubes.

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Appendix

Material Properties of Binary Compounds

Table 9.1 in a systematic way compiles the properties of the binary materials.

Table 9.1. Material properties of binary compounds at 300 K

Material	GaN	AlN	InN	SiC 6H
Crystal structure	Wz	Wz	Wz	Wz
Mass density (kg m^{-3})	6,100	3,230	6,810	3,210
Melting temperature (K)	—	3,273	1,373	3,103
Lattice constant a (\AA)	3.189	3.112	3.533	3.073
Lattice constant c (\AA)	5.185	3.982	5.693	—
Thermal expansion (10^{-6} K^{-1}) $\Delta a/a$	5.59	4.2	3.548	4.3
Thermal expansion (10^{-6} K^{-1}) $\Delta c/c$	3.17	5.3	5.760	4.7
Static ϵ_r	9.5	8.5	15.3	9.66
RF- ϵ_r	5.47	4.77	8.4	6.70
Eff. e^- -mass (m/m_0)	0.2	0.314	0.11	0.2
Bandgap ($E_{g,\text{r}}$) (eV) 300 K	3.434	6.22	0.8	3.0
Bandgap 2nd valley E_g (eV)	—	6.9	—	—
Bandgap 3rd valley E_g (eV)	—	—	—	—
Intervalley separation (eV)	1.5	2.5	1.1	—
Sound velocity (m s^{-1})	5×10^3	1×10^4	5×10^3	—
Phonon energy $\hbar \cdot \omega_{\text{LO}}(\text{meV})$	91.2	99.2	89	—
Piezoelectric constant h_{pz} (cm^{-2})	0.5	0.55	0.3	—
Electron mobility 300 K ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	1,400	683	100	260
Hole mobility 300 K ($\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$)	170	14	—	100
v_{sat} electrons (10^7 cm s^{-1})	1.9	2.16	1.32	2
Thermal conductivity ($\text{W K}^{-1} \text{ cm}^{-1}$)	1.3	2.85	0.38	3.7
Specific heat ($\text{J K}^{-1} \text{ kg}^{-1}$)	491	748	325	670

References of Chapter 2

- 2.1. V. Adivarahan, M. Gaevski, W. Sun, H. Fatima, A. Kouymov, S. Saygi, G. Simin, J. Yang, M. Khan, A. Tarakji, M. Shur, R. Gaska, IEEE Electron Device Lett. **24**, 541 (2003)
- 2.2. A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S. Ryu, J. Zhang, in *Device Research Conference*, State College, PA, 2006, pp. 155–158
- 2.3. I. Akasaki, H. Amano, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 7.2, pp. 222–230
- 2.4. I. Akasaki, H. Amano, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 1.4, pp. 30–34
- 2.5. M. Akita, S. Kishimoto, K. Maezawa, T. Mizutani, Electron. Lett. **36**, 1736 (2000)
- 2.6. J. Albrecht, P. Ruden, S. Binari, M. Ancona, IEEE Trans. Electron Devices **47**, 2031 (2000)
- 2.7. E. Alekseev, D. Pavlidis, Solid-State Electron. **44**, 245 (2000)
- 2.8. E. Alekseev, D. Pavlidis, Solid-State Electron. **44**, 941 (2000)
- 2.9. S. Allen, J. Milligan, Comp. Semicond. **9**, 25 (2003)
- 2.10. O. Ambacher, M. Eickhoff, A. Link, M. Hermann, M. Stutzmann, F. Bernardini, V. Fiorentini, Y. Smorchkova, J. Speck, U. Mishra, W. Schaff, V. Tilak, L. Eastman, Phys. Stat. Sol. C **0**, 1878 (2003)
- 2.11. O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, R. Dimitrov, A. Mitchell, M. Stutzmann, J. Appl. Phys. **87**, 334 (2000)
- 2.12. O. Ambacher, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999)
- 2.13. K. Andersson, V. Desmaris, J. Eriksson, N. Roersman, H. Zirath, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 1303–1306
- 2.14. T. Anderson, D. Barrett, J. Chen, W.T. Elkington, E. Emorhokpor, A. Gupta, C. Johnson, R. Hopkins, C. Martin, T. Kerr, E. Semenas,

- A. Souzis, C. Tanner, M. Yonanathan, I. Zwieback Material Science Forum, **457–460**, 75 (2004),
- 2.15. Y. Ando, W. Contrata, N. Samoto, H. Miyamoto, K. Matsunaga, M. Kuzuhara, K. Kunihiro, K. Kasahara, T. Nakayama, Y. Takahashi, N. Hayama, Y. Ohno, IEEE Trans. Electron Devices **47**, 1965 (2000)
- 2.16. Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, M. Kuzuhara, in *IEDM Technical Digest*, Washington DC, 2001, pp. 381–384
- 2.17. A. Anwar, S. Wu, R. Webster, IEEE Trans. Electron Devices **48**, 567 (2001)
- 2.18. A.P. Zhang, L. Rowland, E. Kaminsky, J. Tucker, J. Kretchmer, A. Allen, J. Cook, B. Edward, Electron. Lett. **39**, 245 (2003)
- 2.19. L. Ardaravicius, A. Matulionis, J. Liberis, O. Kipriyanovic, M. Ramonas, L. Eastman, J. Shealy, A. Vertiatchikh, Appl. Phys. Lett. **83**, 4038 (2003)
- 2.20. S. Arulkumaran, M. Miyoschi, T. Egawa, H. Ishikawa, T. Jimbo, IEEE Electron Device Lett. **24**, 497 (2003)
- 2.21. D. As, D. Schikora, A. Greiner, M. Lübbbers, J. Mimkes, K. Lischka, Phys. Rev. B **54**, R11118 (1996)
- 2.22. P. Asbeck, E. Yu, S. Lau, G. Sullivan, J.V. Hove, J. Redwing, Electron. Lett. **33**, 1230 (1997)
- 2.23. P. Asbeck, E. Yu, S. Lau, W. Sun, X. Dang, C. Shi, Solid-State Electron. **44**, 211 (2000)
- 2.24. M. Aust, A. Sharma, A. Chau, A. Gutierrez-Aitken, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 809–812
- 2.25. C. Bae, C. Krug, G. Lucovsky, A. Chakraborty, U. Mishra, J. Appl. Phys. **96**, 2674 (2003)
- 2.26. A. Baliga, IEEE Electron Device Lett. **10**, 455 (1989)
- 2.27. Z. Bandic, E. Piquette, P. Bridger, R. Beach, T. Kuech, T. McGill, Solid-State Electron. **42**, 2289 (1998)
- 2.28. H. Bang, T. Mitani, S. Nakashima, H. Sazawa, K. Hirata, M. Kosaki, H. Okumura, J. Appl. Phys. **100**, 114502 (2006)
- 2.29. A. Barker, M. Illegems, Phys. Rev. B **7**, 743 (1973)
- 2.30. J. Barker, D. Ferry, D. Koleske, R. Shul, J. Appl. Phys. **97**, 063705 (2005)
- 2.31. A. Barnes, D. Hayes, M. Uren, T. Martin, R. Balmer, D. Wallis, K. Hilton, J. Powell, W. Phillips, A. Jimenez, E. Munoz, M. Kuball, S. Rajasingam, J. Pomeroy, N. Labat, N. Malbert, P. Rice, A. Wells, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 2.32. J. Beintner, Y. Li, A. Knorr, D. Chidambarrao, P. Voigt, R. Divakaruni, P. Pöchmüller, G. Bronner, IEEE Electron Device Lett. **25**, 259 (2004)
- 2.33. K. Bejtka, R. Martin, I. Watson, S. Ndiale, M. Leroux, Appl. Phys. Lett. **89**, 191912 (2006)
- 2.34. E. Bellotti, F. Bertazzi, M. Goano, J. Appl. Phys. **101**, 3706 (2007)
- 2.35. E. Bellotti, B. Doshi, K. Brennan, J. Albrecht, P. Ruden, J. Appl. Phys. **85**, 916 (1999)
- 2.36. F. Bernardini, V. Fiorentini, D. Vanderbilt, Phys. Rev. B **56**, R10024 (1997)
- 2.37. U. Bhapkar, M. Shur, J. Appl. Phys. **82**, 1649 (1997)
- 2.38. A. Bhuiyan, A. Hashimoto, A. Yamamoto, J. Appl. Phys. **94**, 2779 (2003)
- 2.39. S. Binari, K. Ikossi-Anastasiou, J. Roussos, D. Parl, D. Koleske, A. Wickenden, R. Henry, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, St. Louis, 2000, pp. 201–204

- 2.40. S. Binari, J. Redwing, G. Kelner, W. Kruppa, IEEE Electron Device Lett. **33**, 242 (1997)
- 2.41. J. Blevins, in *Proceedings of the International Conference on the GaAs Manufacturing Technology*, Miami, 2004, pp. 287–290
- 2.42. C. Bolognesi, A. Kwan, D. DiSanto, in *IEDM Technical Digest*, San Francisco, 2002, pp. 685–688
- 2.43. K. Boutros, B. Luo, Y. Ma, G. Nagy, J. Hacker, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 93–95
- 2.44. K. Boutros, M. Regan, P. Rowell, D. Gotthold, R. Birkhahn, B. Brar, in *IEDM Technical Digest*, Washington DC, 2003, pp. 981–982
- 2.45. K. Boutros, W. Luo, K. Shinohara, in *Device Research Conference*, Santa Barbara, 2005, pp. 183–184
- 2.46. N. Braga, R. Mickevicius, R. Gaska, X. Hu, M. Shur, M. Khan, G. Simin, J. Yang, J. Appl. Phys. **95**, 6409 (2004)
- 2.47. N. Braga, R. Mickevicius, V. Rao, W. Fichtner, R. Gaska, M. Shur, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 149–152
- 2.48. N. Braga, R. Mickevicius, M. Shur, R. Gaska, M. Shur, M. Khan, G. Simin, in *IEDM Technical Digest*, San Francisco, 2004, pp. 815–818
- 2.49. K. Brennan, E. Bellotti, M. Farahmand, J. Haralson, P. Ruden, J. Albrecht, A. Sutandi, Solid-State Electron. **44**, 195 (2000)
- 2.50. K. Brennan, E. Bellotti, M. Farahmand, H. Nilsson, P. Ruden, Y. Zhang, IEEE Trans. Electron Devices **47**, 1882 (2000)
- 2.51. J. Brinkhoff, A. Parker, in *Workshop Applied Radio Science*, Hobart, 2004, pp. 1–8
- 2.52. J. Brown, W. Nagy, S. Singhal, S. Peters, A. Chaudhari, T. Li, R. Nichols, R. Borges, P. Rajagopal, J. Johnson, R. Therrien, A. Hanson, A. Vescan, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1347–1350
- 2.53. T. Brozek, J. Szmida, A. Jabubowski, A. Olszyna, Diamond Relat. Mater. **3**, 720 (1994)
- 2.54. W. Bryden, T. Kistenmacher, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 3.3, pp. 117–121
- 2.55. G. Bu AND D. Ciplys AND M. Shur AND L.J. Schowalter AND S. Schjman AND R. Gaska, IEEE Trans. Ultrason. Ferroelec. Frequency Control, **53**, 251 (2006)
- 2.56. C. Bulutay, Semicond. Sci. Technol. **17**, L59 (2002)
- 2.57. E. Burgemeister, W. von Muench, E. Pettenpaul, J. Appl. Phys. **50**, 5790 (1979)
- 2.58. J. Burm, K. Chu, W. Schaff, L. Eastman, M. Khan, Q. Chen, J. Yang, M. Shur, IEEE Electron Device Lett. **18**, 141 (1997)
- 2.59. R. Caverly, N. Drozdovski, C. Joye, M. Quinn, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 131–134
- 2.60. S. Cha, Y. Chung, M. Wojtowicz, I. Smorchkova, B. Allen, J. Yang, R. Kagiwada, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 829–832
- 2.61. A. Chakraborty, B. Haskell, S. Keller, J. Speck, S. Denbaars, S. Nakamura, U. Mishra, Jpn. J. Appl. Phys. **44**, L173 (2005)

- 2.62. Q. Chen, J. Yang, R. Gaska, M. Khan, M. Shur, G. Sullivan, A. Sailor, J. Higgins, A. Ping, I. Adesida, IEEE Electron Device Lett. **19**, 44 (1998)
- 2.63. L. Cheng, I. Sankin, N. Merret, J. Casady, W. Draper, W. King, V. Bondarenko, M. Mazzola, J. Casady, in *Device Research Conference*, State College, PA, 2006, pp. 159–160
- 2.64. V. Chin, T. Tansley, T. Osotchan, J. Appl. Phys. **75**, 7365 (1994)
- 2.65. V. Chin, B. Zou, T. Tansley, X. Li, J. Appl. Phys. **77**, 6064 (1995)
- 2.66. A. Chini, D. Buttari, R. Coffie, S. Heikmann, S. Keller, U. Mishra, Electron. Lett. **40**, 73 (2004)
- 2.67. A. Chini, D. Buttari, R. Coffie, L. Shen, S. Heikman, A. Chakraborty, S. Keller, U. Mishra, IEEE Electron Device Lett. **25**, 229 (2004)
- 2.68. A. Chini, R. Coffie, G. Meneghesso, E. Zanoni, D. Buttari, S. Heikman, S. Keller, U. Mishra, Electron. Lett. **39**, 625 (2003)
- 2.69. A. Chini, J. Wittich, S. Heikman, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **25**, 229 (2004)
- 2.70. S. Chiu, A. Anwar, S. Wu, IEEE Trans. Electron Devices **47**, 662 (2000)
- 2.71. L. Chkhartishvili, J. Solid-State Chem. **177**, 395 (2004)
- 2.72. T. Chow, R. Tyagi, IEEE Trans. Electron Devices **41**, 1481 (1994)
- 2.73. K. Chu, P. Chao, M. Pizzella, R. Actis, D. Meharry, K. Nichols, R. Vaudo, X. Xu, J. Flynn, J. Dion, G. Brandes, IEEE Electron Device Lett. **25**, 596 (2004)
- 2.74. E. Chumbes, J. Smart, T. Prunty, J. Shealy, IEEE Trans. Electron Devices **48**, 416 (2001)
- 2.75. R. Clarke, J. Palmour, Proc. IEEE **90**, 987 (2002)
- 2.76. I. Cohen, T. Zhu, L. Liu, M. Murphy, M. Pophristic, M. Pabisz, M. Gottfried, B. Shelton, B. Peres, A. Ceruzzi, R. Stall, in *IEEE APEC*, Austin, 2005, pp. 311–314
- 2.77. P.T. Coleridge, R. Stoner, R. Flechter, Phys. Rev. B, **39**, 1120 (1989)
- 2.78. Compound Semiconductor, Epigress Licenses HTCVD Technology from Oktemic. Comp. Semicond. **6**, (2002)
- 2.79. Compound Semiconductor, Cap Wireless to use GaN Chips in X-Band Amplifiers. Comp. Semicond. **11**, (2005)
- 2.80. Compound Semiconductor, Hitachi Confirms 3-Inch GaN Substrate, Eyes 4-Inch. Comp. Semicond. **11**, (2007)
- 2.81. Compound Semiconductor, Cree Announces 40 W GaN Amplifier, First GaN MMIC. Comp. Semicond. **6**, 15 (2000)
- 2.82. T. Cook, C. Fulton, W. Meccouch, R. Davis, G. Lucovsky, R. Nemanich, J. Appl. Phys. **94**, 3949 (2003)
- 2.83. Cree, Silicon Carbide Substrates and Epitaxy: Product Specifications (2007), <http://www.cree.com>
- 2.84. A. Dadgar, M. Neuburger, F. Schulze, J. Bäsing, A. Krtschil, I. Daumiller, M. Kunze, K. Günther, H. Witte, A. Diez, E. Kohn, A. Krost, Phys. Stat. Sol. A **202**, 832 (2005)
- 2.85. I. Daumiller, M. Seyboth, C. Kirchner, M. Kamp, E. Kohn, in *Device Research Conference*, Denver, 2000, pp. 1–2
- 2.86. V. Davydov, A. Klochikhin, V. Emtsev, D. Kurdyukov, S. Ivanov, V. Verkshin, F. Bechstedt, J. Furthmüller, J. Aderhold, J. Graul, A. Mudryi, H. Harima, A. Hashimoto, A. Yamamoto, E. Haller, Phys. Stat. Sol. B **234**, 787 (2002)

- 2.87. C.V. de Walle, J. Neugebauer, C. Stampfl, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.1, pp. 275–280
- 2.88. M. DeLisio, B. Deckmann, C. Cheung, S. Martin, D. Nakhla, E. Hartmann, C. Rollison, J. Pacetti, J. Rosenberg, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 83–86
- 2.89. G. Dimitrakopulos, P. Komninou, T. Karakostas, R. Pond, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 7, pp. 321–378
- 2.90. R. Dimitrov, A. Mitchell, L. Wittmer, O. Ambacher, M. Stutzmann, J. Hilsenbeck, W. Rieger, Jpn. J. Appl. Phys. **38**, 4962 (1999)
- 2.91. M. Drechsler, D. Hofmann, B. Meyer, T. Detchprohm, H. Amano, I. Akasaki, Jpn. J. Appl. Phys. **34**, L1178 (1995)
- 2.92. M. Drory, J. Ager, T. Suski, I. Grzegory, S. Porowski, J. Appl. Phys. **69**, 4044 (1996)
- 2.93. D. Ducatteau, A. Minko, V. Hoel, E. Morvan, E. Delos, B. Grimbert, H. Lahreche, P. Bove, C. Gaquiere, J. DeJaeger, S. Delage, IEEE Electron Device Lett. **27**, 7 (2006)
- 2.94. D. Dumka, C. Lee, H. Tserng, P. Saunier, M. Kumar, Electron. Lett. **40**, 1023 (2003)
- 2.95. N. Dyakonova, A. Dickens, M. Shur, R. Gaska, Electron. Lett. **34**, 1699 (1998)
- 2.96. L. Eastman, V. Tilak, J. Smart, B. Green, E. Chumbes, R. Dimitrov, H. Kim, O. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. Schaff, J. Shealy, IEEE Trans. Electron Devices **48**, 479 (2001)
- 2.97. L. Eastman. Personal Communication, 2002
- 2.98. L. Eastman, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 2273–2275
- 2.99. J. Edgar, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 1.2, pp. 7–21
- 2.100. J. Edgar (ed.), *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series (IEE INSPEC, London, 1994)
- 2.101. J. Edgar, S. Strite, I. Akasaki, H. Amano, C. Wetzel (eds.), *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series (IEE INSPEC, London, 1999)
- 2.102. G. Ellis, J. Moon, D. Wong, M. Micovic, A. Kurdoglian, P. Hashimoto, M. Hu, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 153–156
- 2.103. E. Emorhokpor, T. Kerr, I. Zwieback, W. Elkington, M. Dudley, T. Anderson, J. Chen, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 139–142
- 2.104. J. Ender, H. Wilden, U. Nickel, R. Klemm, A. Brenner, T. Eibert, D. Nuessler, in *Proceedings of European Radar Conference*, Amsterdam, 2004, pp. 113–116
- 2.105. T. Ericson, Proc. IEEE **90**, 1077 (2002)
- 2.106. K. Evans, Comp. Semicond. **10**, (2004)
- 2.107. S. Evans, N. Giles, L. Haliburton, G. Slack, S. Schujman, L. Schowalter, Appl. Phys. Lett. **88**, 062112 (2006)

- 2.108. W. Fan, M. Li, T. Chong, J. Xia, *J. Appl. Phys.* **79**, 188 (1996)
- 2.109. D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, J. Johnson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.3
- 2.110. M. Farahmand, K. Brennan, *IEEE Trans. Electron Devices* **46**, 1319 (1999)
- 2.111. M. Farahmand, K. Brennan, *IEEE Trans. Electron Devices* **47**, 493 (2000)
- 2.112. M. Farahmand, K. Brennan, E. Gebara, D. Heo, Y. Suh, J. Laskar, *IEEE Trans. Electron Devices* **45**, 1844 (2001)
- 2.113. M. Farahmand, C. Garetto, E. Bellotti, K. Brennan, M. Goano, E. Ghillino, G. Ghione, J. Albrecht, P. Ruden, *IEEE Trans. Electron Devices* **48**, 535 (2001)
- 2.114. T. Fehlberg, G. Umana-Membreno, B. Nener, G. Parish, C. Gallinat, G. Koblmüller, S. Rajan, S. Bernardis, J. Speck, *Jpn. J. Appl. Phys.* **45**, L1090 (2006)
- 2.115. A. Fischer, H. Kühne, H. Richter, *Phys. Rev. Lett.* **73**, 2712 (1994)
- 2.116. G. Fischer, in *IEEE Wireless and Microwave Technology Conference*, Clearwater, 2004, p. FD-1
- 2.117. M. Fischetti, *IEEE Trans. Electron Devices* **38**, 634 (1991)
- 2.118. M. Fischetti, S. Laux, *IEEE Trans. Electron Devices* **38**, 650 (1991)
- 2.119. N. Fitzer, A. Kuligk, R. Redmer, M. Städele, S. Goodnick, W. Schattke, *Semicond. Sci. Technol.* **19**, S206 (2004)
- 2.120. D. Florescu, V. Asnin, F. Pollack, *Comp. Semicond.* **7**, 62 (2001)
- 2.121. B. Foutz, S. O'Leary, M. Shur, L. Eastman, *J. Appl. Phys.* **85**, 7727 (1999)
- 2.122. S. Fu, Y. Chen, *Appl. Phys. Lett.* **85**, 1523 (2004)
- 2.123. D. Gaskill, L. Rowland, K. Doverspike, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 3.2, pp. 101–116
- 2.124. G. Gauthier, Y. Mancuso, F. Murgadella, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Paris, 2005, pp. 361–364
- 2.125. J. Gillespie, R. Fitch, N. Moser, T. Jenkins, J. Sewell, D. Via, A.C.A. Dabiran, P. Chow, A. Osinsky, M. Mastro, D. Tsvetkov, V. Soukhovcev, A. Usikov, V. Dmitriev, B. Luo, S. Pearton, F. Ren, *Solid-State Electron.* **47**, 1859 (2003)
- 2.126. J. Gillespie, G. Jessen, G. Via, A. Crespo, D. Langley, M. Aumer, H. Henry, D. Thomson, D. Partlow, in *Proceedings of the International Conference GaAs Manufacturing Technology*, Austin, 2007, pp. 73–76
- 2.127. M. Goano, E. Bellotti, E. Ghillino, C. Garetto, G. Ghione, K. Brennan, *J. Appl. Phys.* **88**, 6476 (2000)
- 2.128. M. Goano, E. Bellotti, E. Ghillino, G. Ghione, K. Brennan, *J. Appl. Phys.* **88**, 6467 (2000)
- 2.129. J. Grajal, F. Calle, J. Pedros, T. Palacios, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 387–390
- 2.130. B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, L. Eastman, *IEEE Electron Device Lett.* **21**, 268 (2000)
- 2.131. B. Green, H. Henry, J. Selbee, R. Lawrence, K. Moore, J. Abdou, M. Miller, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 706–709

- 2.132. B. Green, V. Tilak, V. Kaper, J. Smart, J. Shealy, L. Eastman, IEEE Trans. Microwave Theory Tech. **51**, 618 (2003)
- 2.133. B. Green, V. Tilak, S. Lee, H. Kim, J. Smart, K. Webb, J. Shealy, L. Eastman, IEEE Trans. Microwave Theory Tech. **49**, 2486 (2001)
- 2.134. D. Grider, J. Smart, R. Vetur, M. Young, J. Dick, B. Delayney, Y. Yang, T. Mercier, S. Gibb, C. Palmer, B. Hosse, K. Leverich, N. Zhang, J. Shealy, M. Poulton, B. Sousa, D. Schnaufer, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 101–102
- 2.135. V. Gubaniv, E. Pentaleri, C. Fong, B. Klein, Phys. Rev. B **56**, 13077 (1997)
- 2.136. E. Gusev et al., in *IEDM Technical Digest*, San Francisco, 2004, pp. 79–82
- 2.137. A. Hanser, L. Liu, E. Preble, D. Tsetkov, M. Tutor, N. Williams, K. Evans, Y. Zhou, D. Wang, C. Ahyi, C. Tin, J. Williams, M. Park, D. Storm, D. Katzer, S. Binari, J. Roussos, J. Mittereder, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 67–70
- 2.138. S. Harada, M. Kato, K. Suzuki, M. Okamoto, T. Yatsuo, K. Fukuda, K. Arai, in *IEDM Technology Digest*, San Francisco, 2006, pp. 1–4
- 2.139. G. Harris (ed.), in *Properties of Silicon Carbide*, No. 13 in EMIS Data reviews Series (IEE INSPEC, London, 1995)
- 2.140. J. Heffernan, M. Kauer, S. Hooper, V. Bousquet, K. Johnson, Phys. Stat. Sol. C **1**, 2668 (2004)
- 2.141. R. Hickman, J. van Hove, P. Chow, J. Klaassen, A. Wowchack, C. Polley, D. King, F. Ren, C. Abernathy, S. Pearton, K. Jung, H. Cho, J. LaRoche, Solid-State Electron. **44**, 377 (2000)
- 2.142. M. Higashiwaki, T. Mimura, T. Matsui, IEEE Electron Device Lett. **27**, 719 (2006)
- 2.143. M. Higashiwaki, T. Mimura, T. Matsui, Jpn. J. Appl. Phys. **45**, L843 (2006)
- 2.144. M. Hirose, Y. Takada, M. Kuraguchi, T. Sasaki, K. Tsuda, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 163–166
- 2.145. C. Hobbs, Leonardo, R. Fonseca, A. Knizhnik, V. Dhandapani, S. Samavedam, W. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, M. Lovejoy, R. Rai, E. Hebert, H. Tseng, S. Anderson, B. White, P. Tobin, IEEE Trans. Electron Devices **51**, 971 (2004)
- 2.146. D. Holec, P.M.F.J. Costa, M. Kaspers, C. Humphreys, J. Cryst. Growth **303**, 314 (2007)
- 2.147. H. Hommel, H. Feldle, in *Proceedings of the European Radar Conference*, Amsterdam, 2004, pp. 121–124
- 2.148. Honeywell International, Honeywell Sapphire Products (2007) <https://www51.honeywell.com/sm/em/products-applications/opto-electro-materials.html>
- 2.149. A. Hori, H. Nakaoka, H. Umimoto, K. Yamashita, M. Takase, N. Shimizu, B. Mizuno, S. Odanaka, in *IEDM Technical Digest*, Washington DC, 1994, pp. 485–488
- 2.150. Y. Hsin, H. Hsu, C. Chuo, J. Chyi, IEEE Electron Device Lett. **22**, 501 (2001)
- 2.151. X. Hu, J. Deng, N. Pala, R. Gaska, M. Shur, C. Chen, J. Yang, G. Simin, M. Khan, J. Rojo, L. Schowalter, Appl. Phys. Lett. **82**, 1299 (2003)
- 2.152. J. Huang, M. Hattendorf, M. Feng, D. Lambert, B. Shelton, M. Wong, U. Chowdhury, T. Zhu, H. Kwon, R. Dupuis, IEEE Electron Device Lett. **22**, 157 (2001)

- 2.153. T. Hussain, A. Kurdoghlian, P. Hashimoto, W. Wong, M. Wetzel, J. Moon, L. McCray, M. Micovic, in *IEDM Technical Digest*, Washington DC, 2001, pp. 581–584
- 2.154. J. Ibbetson, P. Fini, K. Ness, S. DenBaars, J. Speck, U. Mishra, *Appl. Phys. Lett.* **77**, 250 (2000)
- 2.155. D. Ingram, Y. Chen, J. Kraus, B. Brunner, B. Allen, H. Yen, K. Lau, in *Radio Frequency Integrated Circuit Symposium Digest*, Anaheim, 1999, pp. 95–98
- 2.156. T. Inoue, Y. Ando, H. Miyamoto, T. Nakayama, Y. Okamoto, K. Hataya, M. Kuzuhara, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1649–1652
- 2.157. T. Inoue, Y. Ando, H. Miyamoto, T. Nakayama, Y. Okamoto, K. Hataya, M. Kuzuhara, *IEEE Trans. Microwave Theory Tech.* **53**, 74 (2004)
- 2.158. H. Ishida, Y. Hirose, T. Murata, A. Kanda, Y. Ikeda, T. Matsuno, K. Inoue, Y. Uemoto, T. Tanaka, T. Egawa, D. Ueda, in *IEDM Technical Digest*, Washington DC, 2003, pp. 583–586
- 2.159. H. Jacobsen, J. Birch, R. Yakimova, M. Syvajarvi, J. Bergman, A. Ellison, T. Tuomi, E. Janzen, *J. Appl. Phys.* **91**, 6354 (2002)
- 2.160. H. Jang, C. Jeon, K. Kim, J. Kim, S. Bae, J. Lee, J. Choi, J. Lee, *Appl. Phys. Lett.* **81**, 1249 (2002)
- 2.161. P. Javorka, A. Alam, N. Nastase, M. Marso, H. Hardtdegen, M. Heuken, H. Lüth, P. Kordos, *Electron. Lett.* **37**, 1364 (2001)
- 2.162. P. Javorka, A. Alam, M. Wolter, A. Fox, M. Marso, M. Heuken, H. Lüth, P. Kordos, *Electron. Lett.* **23**, 4 (2002)
- 2.163. D. Jenkins, J. Dow, *Phys. Rev. B* **39**, 3317 (1989)
- 2.164. G. Jessen, R. Fitch, J. Gillespie, G. Via, N. Moser, M. Yannuzzi, A. Crespo, J. Sewell, R. Dettmer, T. Jenkins, R. Davis, J. Yang, M. Khan, S. Binari, *IEEE Electron Device Lett.* **24**, 677 (2003)
- 2.165. G. Jessen, J. Gillespie, G. Via, A. Crespo, D. Langley, J. Wasserbauer, F. Faili, D. Francis, D. Babic, F. Ejekam, S. Guo, I. Eliashevich, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 271–274
- 2.166. A. Jimenez, D. Buttari, D. Jena, R. Coffie, S. Heikman, N. Zhang, L. Shen, E. Calleeja, E. Munoz, J. Speck, U. Mishra, *IEEE Electron Device Lett.* **23**, 306 (2002)
- 2.167. E. Johnson, *RCA Rev.* **26**, 163 (1965)
- 2.168. J. Johnson, J. Gao, K. Lucht, J.W.C. Strautin, J. Riddle, T. Therrien, P. Rajagopal, J. Roberts, A. Vescan, J. Brown, A. Hanson, S. Singhal, R. Borges, E. Piner, K. Linthicum, *Proc. Elec. Soc.* **7**, 405 (2004)
- 2.169. J. Johnson, E. Piner, A. Vescan, R. Therrien, Rajagopal, J. Roberts, J. Brown, J. Brown, K. Linthicum, *IEEE Electron Device Lett.* **25**, 459 (2004)
- 2.170. R. Jones, K. Yu, S. Li, W. Walukiewicz, J. Ager, E. Haller, H. Lu, W. Schaff, *Phys. Rev. Lett.* **96**, 125505–1 (2006)
- 2.171. K. Joshin, T. Kikkawa, in *Device Research Conference*, Long Beach, 2005, pp. 173–176
- 2.172. K. Joshin, T. Kikkawa, H. Hayashi, T. Maniwa, S. Yokokawa, M. Yokoyama, N. Adachi, M. Takikawa, in *IEDM Technical Digest*, Washington DC, 2003, pp. 983–985
- 2.173. Y. Kamo, T. Kunii, H. Takeuchi, Y. Yamamoto, M. Totsuka, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, T. Oku, A. Inoue, T. Nanjo, H. Chiba,

- M. Suita, T. Oishi, Y. Abe, Y. Tsuyama, R. Shirahana, H. Ohtsuka, K. Iyomasa, K. Yamanaka, M. Hieda, M. Nakayama, T. Ishikawa, T. Takagi, K. Marumoto, Y. Matsuda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 495–498
- 2.174. M. Kanamura, T. Kikkawa, J. Joshin, in *IEDM Technical Digest*, San Francisco, 2004, pp. 799–802
- 2.175. B. Kang, S. Kim, F. Ren, J. Johnson, R. Therrien, P. Rajagopal, J. Roberts, E. Piner, K. Linthicum, S. Chu, K. Baik, B. Gila, C. Abernathy, S. Pearton, *Appl. Phys. Lett.* **85**, 2962 (2004)
- 2.176. B. Kang, F. Ren, B. Gilla, C. Abernathy, S. Pearton, *Appl. Phys. Lett.* **84**, 1123 (2004)
- 2.177. M. Kanoun, S. Goumri-Said, G. Merad, J. Cibert, H. Aourag, *Semicond. Sci. Technol.* **19**, 1220 (2004)
- 2.178. M. Kanoun, A. Merad, G. Merad, J. Cibert, H. Aourag, *Solid-State Electron.* **48**, 1601 (2004)
- 2.179. M. Kao, C. Lee, R. Hajji, P. Saunier, H. Tserng, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 627–630
- 2.180. V. Kaper, V. Tilak, H. Kim, R. Thompson, T. Prunty, J. Smart, L. Eastman, J. Shealy, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 251–254
- 2.181. M. Kariya, S. Nitta, S. Yamaguchi, H. Amano, I. Akasaki, *Jpn. J. Appl. Phys.* **38**, L984 (1999)
- 2.182. S. Karmalkar, N. Satyan, D. Sathaiya, *IEEE Electron Device Lett.* **27**, 87 (2006)
- 2.183. S. Karmalkar, N. Soudabi, *IEEE Trans. Electron Devices* **53**, 2430 (2006)
- 2.184. K. Kasahara, H. Miyamoto, Y. Ando, Y. Okamoto, T. Nakayama, M. Kuzuhara, in *IEDM Technical Digest*, San Francisco, 2002, pp. 677–680
- 2.185. O. Katz, A. Horn, J. Salzmann, *IEEE Trans. Electron Devices* **50**, 2002 (2003)
- 2.186. O. Katz, D. Mistele, B. Meyler, G. Bahir, J. Salzman, in *IEDM Technical Digest*, San Francisco, 2004, pp. 1035–1038
- 2.187. O. Katz, D. Mistele, B. Meyler, G. Bahir, J. Salzmann, *Electron. Lett.* **40**, 1304 (2004)
- 2.188. S. Keller, Y. Wu, G. Parish, N. Ziang, J. Xu, B. Keller, S. DenBaars, U. Mishra, *IEEE Trans. Electron Devices* **48**, 552 (2001)
- 2.189. R. Kemerley, H. Wallace, M. Yoder, *Proc. IEEE* **90**, 1059 (2002)
- 2.190. M. Khan, A. Bhattacharai, J. Kuznia, D. Olson, *Appl. Phys. Lett.* **63**, 1214 (1993)
- 2.191. M. Khan, X. Hu, G. Simin, A. Lunev, J. Yang, R. Gaska, M. Shur, *IEEE Electron Device Lett.* **21**, 63 (2000)
- 2.192. M. Khan, M. Shur, G. Simin, *Phys. Stat. Sol. A* **200**, 155 (2003)
- 2.193. M. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. Shur, R. Gaska, X. Hu, A. Tarakji, *IEEE Trans. Microwave Theory Tech.* **51**, 624 (2003)
- 2.194. R. Kiefer, R. Quay, S. Müller, K. Köhler, F. van Raay, B. Raynor, W. Pletschen, H. Massler, S. Ramberger, M. Mikulla, G. Weimann, in *Proceedings of the Lester Eastman Conference High Performance Devices*, Newark, 2002, pp. 502–504
- 2.195. T. Kikkawa, T. Maniwa, H. Hayashi, M. Kanamura, S. Yokokawa, M. Nishi, N. Adachi, M. Yokoyama, Y. Tateno, K. Joshin, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1347–1350

- 2.196. T. Kikkawa, E. Mitani, K. Joshin, S. Yokokawa, Y. Tateno, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami Beach, 2004, pp. 97–100
- 2.197. T. Kikkawa, M. Nagahara, N. Adachi, S. Yokokawa, S. Kato, M. Yokoyama, M. Kanamura, Y. Yamaguchi, N. Hara, K. Joshin, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 167–170
- 2.198. T. Kikkawa, M. Nagahara, T. Kimura, S. Yokokawa, S. Kato, M. Yokoyama, Y. Tateno, K. Horino, K. Domen, Y. Yamaguchi, N. Hara, K. Joshin, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1815–1818
- 2.199. C. Kim, I. Robinson, J. Myoung, K. Shim, M. Yoo, K. Kim, *Appl. Phys. Lett.* **69**, 2358 (1996)
- 2.200. J. Kim, B. Gila, C. Abernathy, G. Chung, F. Ren, S. Pearton, *Solid-State Electron.* **47**, 1487 (2003)
- 2.201. D. Kimball, P. Draxler, J. Jeong, C. Hsia, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, P. Asbeck, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 89–92
- 2.202. D. Kimball, J. Jeong, P. Draxler, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, P. Asbeck, *IEEE Trans. Microwave Theory Tech.* **54**, 3848 (2006)
- 2.203. S. King, R. Nemanich, R. Davis, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. C1.3, pp. 500–505
- 2.204. L. Kirste, S. Müller, R. Kiefer, R. Quay, K. Köhler, N. Herres, *Mater. Sci. Eng. B* **9**, 8 (2006)
- 2.205. K. Köhler, J. Wiegert, H.P. Menner, M. Maier, L. Kirste, *J. Appl. Phys.* **103**, 023706 (2008)
- 2.206. E. Kohn, I. Daumiller, P. Schmid, N. Nguyen, C. Nguyen, *Electron. Lett.* **35**, 1022 (1999)
- 2.207. E. Kohn, J. Kusterer, A. Denisenko, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 901–904
- 2.208. G. Koley, V. Tilak, L. Eastman, M. Spencer, *J. Appl. Phys.* **90**, 337 (2001)
- 2.209. G. Koley, V. Tilak, L. Eastman, M. Spencer, *IEEE Trans. Electron Devices* **50**, 886 (2003)
- 2.210. N. Kolias, T. Kazior, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 2.211. J. Kolnik, I.H. Oguzman, K.F. Brennan, R. Wang, P.P. Ruden, Y. Wang, *J. Appl. Phys.* **78**, 1033 (1995)
- 2.212. J. Kolnik, I. Oguzman, K. Brennan, R. Wang, P. Ruden, *J. Appl. Phys.* **81**, 726 (1997)
- 2.213. T. Komachi, T. Takayama, M. Imamura, in *IEDM Technical Digest*, San Francisco, 2006, pp. 915–918
- 2.214. J. Komiak, W. Kong, P. Chao, K. Nicols, in *IEEE International Microwave Symposium Digest*, Anaheim, 1999, pp. 947–950
- 2.215. K. Kong, B. Nguyen, S. Nayak, M. Kao, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 232–235
- 2.216. D. Kotchetkov, J. Zou, A. Balandin, D. Florescu, F. Pollak, *J. Electron. Mater.J. Electron. Mater.* **79**, 4316 (2001)
- 2.217. A. Koudymov, X. Hu, K. Simin, M. Ali, J. Yang, M. Khan, *IEEE Electron Device Lett.* **23**, 449 (2002)

- 2.218. P. Kozodoy, H. Xing, S. DenBaars, U. Mishra, A. Saxler, R. Perrin, S. Elhamri, W. Mitchel, *J. Appl. Phys.* **87**, 1832 (2000)
- 2.219. M. Krämer, R. Hoskesn, B. Jakobs, J. Kwaspfen, E. Suijker, A. de Hek, F. Karouta, L. Kaufmann, in *Proceedings of the European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 75–78
- 2.220. D. Krausse, R. Quay, R. Kiefer, A. Tessmann, H. Massler, A. Leuther, T. Merkle, S. Müller, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 71–74
- 2.221. S. Kret, P. Ruterana, C. Delamarre, T. Benabbas, P. Dluzewski, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 9, pp. 439–488
- 2.222. S. Krukowski, M. Leszczynski, S. Porowski, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 1.4, pp. 21–28
- 2.223. S. Krukowski, A. Witek, J. Adamczyk, J. Jun, M. Bockowski, I. Gregory, B. Lucznik, G. Nowak, M. Wroblewski, A. Presz, S. Gierlotka, S. Stelmach, B. Palosz, S. Porowski, P. Zinn, *J. Phys. Chem. Solids*, **59**, 289 (1998)
- 2.224. Y. Kumagai, T. Nagashima, A. Koukitu, *Jpn. J. Appl. Phys.* **46**, L389 (2007)
- 2.225. K. Kumakura, T. Makimoto, N. Kobayashi, *Jpn. J. Appl. Phys.* **39**, L337 (2000)
- 2.226. V. Kumar, G. Chen, S. Guo, B. Peres, I. Adesida, in *Device Research Conference*, Santa Barbara, 2005, pp. 61–62
- 2.227. V. Kumar, J. Lee, A. Kuliev, R. Schwindt, R. Birkhahn, D. Gotthold, S. Guo, B. Albert, I. Adesida, *Electron. Lett.* **39**, 1609 (2003)
- 2.228. V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M. Khan, I. Adesida, *IEEE Electron Device Lett.* **23**, 455 (2002)
- 2.229. K. Kunihiro, K. Kasahara, Y. Takahashi, Y. Ohno, *IEEE Electron Device Lett.* **20**, 608 (1999)
- 2.230. J. Kuzmik, *IEEE Electron Device Lett.* **22**, 510 (2001)
- 2.231. J. Kuzmik, *Semicond. Sci. Technol.* **17**, 540 (2002)
- 2.232. J. Kuzmik, J. Carlin, T. Kostopoulos, G. Konstantinidis, A. Georgakilas, D. Pogany, in *Device Research Conference*, Santa Barbara, 2005, pp. 57–58
- 2.233. M. Kuzuhara, H. Miyamoto, Y. Ando, T. Inoue, Y. Okamoto, T. Nakayama, *Phys. Stat. Sol. A* **200**, 161 (2003)
- 2.234. D. Lambert, D. Lin, R. Dupuis, *Solid-State Electron.* **44**, 253 (2000)
- 2.235. W. Lambrecht, B. Segall, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 5.2, pp. 163–166
- 2.236. W. Lambrecht, B. Segall, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 4.3, pp. 135–140
- 2.237. W. Lambrecht, B. Segall, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 4.2, pp. 129–134
- 2.238. W. Lambrecht, B. Segall, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 4.4, pp. 141–150

- 2.239. J. LaRoche, B. Luo, F. Ren, K. Baik, D. Stodilka, B. Gila, C. Abernathy, S. Pearton, A. Usikov, D. Tsevtkov, V. Soukhouveev, G. Gainer, A. Rechnikov, V. Dimitriev, G. Chen, C. Pan, J. Chyi, Solid-State Electron. **48**, 193 (2004)
- 2.240. C. Lee, P. Saunier, J. Yang, M. Khan, IEEE Electron Device Lett. **24**, 616 (2003)
- 2.241. C. Lee, H. Wang, J. Yang, L. Witkowski, M. Muir, P. Saunier, M. Khan, Electron. Lett. **38**, 924 (2002)
- 2.242. S. Lee, H. Jeong, S. Bae, H. Choi, J. Lee, Y. Lee, IEEE Trans. Electron Devices **48**, 524 (2001)
- 2.243. M. Leszczynski, T. Suski, H. Teisseyre, P. Perlin, I. Grzegory, J. Jun, S. Porowski, T. Moustakas, J. Appl. Phys. **76**, 4909 (1994)
- 2.244. M. Levinstein, S. Rumyantsev, M. Shur (eds.), *GaN, AlN, InN, BN, SiC, SiGe: Properties of Advanced Semiconductor Materials* (Wiley, New York, 2001)
- 2.245. J. Li, K. Nam, M. Nakarmi, J. Lin, H. Jiang, Appl. Phys. Lett. **83**, 5163 (2003)
- 2.246. Q. Li, A. Polyakov, M. Skowronski, M. Roth, M. Fanton, D. Snyder, J. Appl. Phys. **96**, 411 (2004)
- 2.247. S. Li, K. Yu, J. Wu, R. Jones, W. Walukiewicz, J. Ager, W. Shan, E. Haller, H. Lu, W. Schaff, Phys. Rev. B **71**, 161201 (2005)
- 2.248. P. Lim, B. Schineller, O. Schön, K. Heime, M. Heuken, J. Cryst. Growth **205**, 1 (1999)
- 2.249. C. Lin, H. Liu, C. Chu, H. Huang, Y. Wang, C. Liu, C. Chang, C. Wu, C. Chang, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 165–168
- 2.250. Y. Lin, Q. Ker, C. Ho, H. Chang, F. Chien, J. Appl. Phys. **94**, 1819 (2003)
- 2.251. Y. Lin, S. Koa, C. Chan, S. Hsu, Appl. Phys. Lett. **90**, 142111 (2007)
- 2.252. K. Linkenheil, H. Ruob, W. Heinrich, in *Proceedings of the European Microwave Conference*, Amsterdam, 2004, pp. 1561–1564
- 2.253. D. Litvinov, C. Taylor, R. Clarke, Diamond Relat. Mater. **7**, 360 (1998)
- 2.254. B.T. Liu, Appl. Phys. A, **86**, 539 (2007)
- 2.255. W. Liu, A. Balandin, Appl. Phys. Lett. **85**, 5230 (2004)
- 2.256. B.T. Liu, C.W. Liu, Optical Comm., **274**, 361 (2007)
- 2.257. D. Look, Mater. Sci. Eng. B **80**, 383 (2001)
- 2.258. D. Look, J. Sizelove, Phys. Rev. Lett. **82**, 1237 (1999)
- 2.259. D. Look, J. Sizelove, S. Keller, Y. Wu, U. Mishra, S. DenBaars, Solid-State Commun. **102**, 297 (1997)
- 2.260. S. Loughin, R. French, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 6.2, pp. 175–189
- 2.261. W. Lu, V. Kumar, E. Piner, I. Adesida, IEEE Trans. Electron Devices **50**, 1069 (2003)
- 2.262. W. Lu, J. Yang, M. Khan, I. Adesida, IEEE Trans. Electron Devices **48**, 581 (2001)
- 2.263. M. Ludwig, C. Buck, F. Coromina, M. Suess, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1619–1622
- 2.264. C. Luo, D. Clarke, J. Dryden, J. Electron. Mater. **30**, 138 (2001)
- 2.265. B. Luther, S. Wolter, S. Mohney, Sensors Actuators B **56**, 164 (1999)
- 2.266. M. Lyons, C. Grondahl, S. Daoud, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1673–1676

- 2.267. X. Ma, T. Sudarshan, J. Electron. Mater. **33**, 450 (2004)
- 2.268. A. Maekawa, T. Yamamoto, E. Mitani, S. Sano, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 722–725
- 2.269. T. Makimoto, K. Kumakura, N. Kobayashi, in *Proceedings of the International Workshop on Nitride Semiconductors*, Nagoya, 2000, pp. 969–972
- 2.270. T. Makimoto, K. Kumakura, N. Kobayashi, in *International Conference on Solid-State Devices and Materials*, Tokyo, 2003, pp. 134–135
- 2.271. T. Makimoto, Y. Yamauchi, K. Kumakura, Appl. Phys. Lett. **84**, 1964 (2004)
- 2.272. Y. Mancuso, P. Gremillet, P. Lacomme, in *Proceedings of the European Microwave Conference*, Paris, 2005, pp. 817–820
- 2.273. C. Martin, T. Kerr, W. Stepko, T. Anderson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 291–294
- 2.274. E. Martin, J. Jimenez, M. Chafai, Solid-State Electron. **42**, 2309 (1998)
- 2.275. G. Martin, A. Botchkarev, A. Rockett, H. Morkoc, Appl. Phys. Lett. **68**, 2541 (1996)
- 2.276. K. Matocha, T. Chow, R. Gutmann, IEEE Trans. Electron Devices **52**, 6 (2005)
- 2.277. K. Matocha, R. Gutmann, T. Chow, IEEE Trans. Electron Devices **50**, 1200 (2003)
- 2.278. T. Matsuoka, H. Okamoto, M. Nakao, H. Harima, E. Kurimoto, Appl. Phys. Lett. **81**, 1246 (2002)
- 2.279. T. Matsuoka, H. Okamoto, M. Nakao, H. Harima, H. Takahata, H. Mitate, S. Mizuno, Y. Uchiyama, T. Makimoto, in *International Conference on the Solid-State Development and Materials*, Tokyo, 2003, pp. 132–133
- 2.280. J. Matthews, A. Blakeslee, J. Cryst. Growth **27**, 118 (1974)
- 2.281. A. Matulionis, J. Liberis, L. Ardaravicius, M. Ramonas, I. Matulioniene, J. Smart, Semicond. Sci. Technol. **17**, L9 (2002)
- 2.282. L.S. McCarthy, Dissertation, University of California Santa Barbara, Santa Barbara, 2001
- 2.283. L. McCarthy, I. Smorchkova, H. Xing, P. Kozodoy, P. Fini, J. Limb, D. Pulfrey, J. Speck, M. Rodwell, S. DenBaars, U. Mishra, IEEE Trans. Electron Devices **48**, 543 (2001)
- 2.284. F. Medjdoub, J. Carlin, M. Gonschorek, E. Feltin, M. Py, D. Ducatteau, C. Gaquiere, N. Grandjean, E. Kohn, in *IEDM Technical Digest*, San Francisco, 2006, p. 35.7
- 2.285. R. Mehandru, B. Luo, B. Kang, J. Kim, F. Ren, S. Pearton, C. Pan, G. Chen, J. Chyi, Solid-State Electron. **48**, 351 (2004)
- 2.286. C. Meng, G. Liao, J. Chen, in *IEEE International Microwave Symposium Digest*, Anaheim, 1999, pp. 1777–1780
- 2.287. W. Meng, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 1.3, pp. 22–29
- 2.288. W. Menninger, R. Benton, M. Choi, J. Feicht, U. Hallsten, H. Limburg, W. McGahey, Z. Xiaoling, IEEE Trans. Electron Devices **52**, 673 (2005)
- 2.289. M. Micovic, P. Hashimoto, M. Hu, I. Milosavljevic, J. Duval, P. Willadsen, A. Kurdoghlian, P. Deelman, J. Moon, A. Schmitz, M. Delaney, in *IEDM Technical Digest*, San Francisco, 2004, pp. 807–810
- 2.290. M. Micovic, A. Kurdoghlian, H. Moyer, P. Hashimoto, A. Schmitz, I. Milosavljevic, P. Willadsen, W. Wong, J. Duvall, M. Hu, M. Wetzel,

- D. Chow, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 173–176
- 2.291. M. Micovic, A. Kurdhoglian, P. Hashimoto, M. Hu, M. Antcliffe, P. Willadsen, W. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel, D. Chow, in *IEDM Technical Digest*, San Francisco, 2006 pp. 425–428
- 2.292. M. Micovic, A. Kurdoghlian, A. Janke, P. Hashimoto, P. Wong, D. Moon, J. McCray, C. Nguyen, IEEE Trans. Electron Devices **48**, 591 (2001)
- 2.293. J. Milligan, J. Henning, S. Allen, A. Ward, P. Parikh, R. Smith, A. Saxler, Y. Wu, J. Palmour, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 15–18
- 2.294. J. Milligan, J. Henning, S. Allen, A. Ward, J. Palmour, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.2
- 2.295. A. Minko, V. Hoel, G. Dambrine, C. Gaquiere, J. DeJaeger, Y. Cordier, F. Semond, F. Natali, J. Massies, H. Lahreche, L. Wedzikowski, R. Langer, P. Bove, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 67–70
- 2.296. A. Minko, V. Hoel, S. Lepilliet, G. Dambrine, J. DeJaeger, Y. Cordier, F. Semond, F. Natali, J. Massies, IEEE Electron Device Lett. **25**, 167 (2004)
- 2.297. A. Minko, V. Hoel, E. Morvan, B. Grimbart, A. Soltani, E. Delos, D. Ducatteau, C. Gaquière, D. Theron, J.C.D. Jaeger, H. Lahreche, L. Wedzikowski, R. Langer, P. Bove, IEEE Electron Device Lett. **25**, 453 (2004)
- 2.298. J. Miragliotta, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 6.3, pp. 190–194
- 2.299. J. Miragliotta, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 6.4, pp. 195–199
- 2.300. O. Mishima, K. Era, J. Tanaka, S. Yamaoka, Appl. Phys. Lett. **53**, 962 (1988)
- 2.301. U. Mishra, P. Parikh, Y. Wu, Proc. IEEE **90**, 1022 (2002)
- 2.302. U. Mishra, Y. Wu, B. Keller, S. Keller, S. Denbaars, IEEE Trans. Microwave Theory Tech. **46**, 756 (1998)
- 2.303. D. Mistele, O. Katz, A. Horn, G. Bahir, J. Salzmann, Semicond. Sci. Technol. **20**, 972 (2005)
- 2.304. E. Mitani, M. Aojima, A. Maekawa, S. Sano, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 213–216
- 2.305. E. Mitani, M. Aojima, S. Sano, in *Proceedings of the European Microwave Integrated Circuits Conference*, Munich, 2007, pp. 176–179
- 2.306. M. Miyazaki, S. Miyazaki, Y. Yanase, T. Ochiai, T. Shigematsu, Jpn. J. Appl. Phys. **34**, 6303 (1995)
- 2.307. K. Mkhoyan, J. Silcox, E. Alldredge, N. Ashcroft, H. Lu, W. Schaff, L. Eastman, Appl. Phys. Lett. **82**, 1407 (2003)
- 2.308. T. Mnatsakanov, M. Levinstein, L. Pomortseva, S. Yurkov, G. Simin, M. Khan, Solid-State Electron. **47**, 111 (2003)
- 2.309. Y. Mochida, T. Takano, H. Gambe, in *IEDM Technical Digest*, Washington DC, 2001, pp. 14–21
- 2.310. P. Moens, F. Bauwens, J. Baele, K. Vershinin, E.D. Backer, E.S. Narayanan, M. Tack, in *IEDM Technical Digest*, San Francisco, 2006, pp. 919–922

- 2.311. C. Monier, F. Ren, J. Han, P. Chang, R. Shul, K. Lee, A. Zhang, A. Baca, S. Pearton, IEEE Trans. Electron Devices **48**, 427 (2001)
- 2.312. J. Moon, M. Micovic, P. Janke, P. Hashimoto, W. Wong, R. Widman, L. McCray, A. Kurdoghlian, C. Nguyen, Electron. Lett. **37**, 528 (2001)
- 2.313. J. Moon, D. Wong, M. Antcliffe, P. Hashimoto, M. Hu, P. Willadsen, M. Micovic, H. Moyer, A. Kurdhoglian, P. MacDonald, M. Wetzel, R. Bowen, in *IEDM Technical Digest*, San Francisco, 2006, pp. 423–424
- 2.314. K. Mori, Y. Sakai, S. Tsuji, H. Asao, K. Seino, H. Hirose, T. Takagi, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1661–1664
- 2.315. H. Morkoc, *Nitride Semiconductors and Devices*, No. 32 in Springer Series in Materials Science (Springer, Berlin Heidelberg New York, 1999)
- 2.316. S. Müller, J. Sumakeris, M. Brady, R. Glass, H. Hobgood, J. Jenny, R. Leonard, D. Malta, M. Paisley, A. Powell, V. Powell, V. Tsetkov, S. Allen, M. Das, J. Palmour, C. Carter, Eur. Phys. J. Appl. Phys. **27**, 29 (2004)
- 2.317. J. Muth, J. Lee, I. Shmagin, R. Kolbas, H. Casey, B. Keller, U. Mishra, S. DenBaars, Appl. Phys. Lett. **71**, 2572 (1997)
- 2.318. M. Nagahara, T. Kikkawa, N. Adachi, Y. Tateno, S. Kato, M. Yokoyama, S. Yokogama, T. Kimura, Y. Yamaguchi, N. Hara, K. Joshin, in *IEDM Technical Digest*, San Francisco, 2002, pp. 693–696
- 2.319. W. Nagy, S. Singhal, R. Borges, W. Johnson, J. Brown, R. Therrien, A. Chaudhari, A. Hanson, J. Riddle, S. Booth, P. Rajagopal, E. Piner, K. Linthicum, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 483–486
- 2.320. D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, K. Takatori, Nature **430**, 1009 (2004)
- 2.321. N. Nakamura, MRS Bulletin **23**, 37 (1998)
- 2.322. S. Nakamura, Diamond Relat. Mater. **5**, 496 (1996)
- 2.323. S. Nakamura, S. Chichibu (eds.), *Introduction to Nitride Semiconductor Blue Lasers and Light Emitting Diodes* (Taylor & Francis, London New York, 2000)
- 2.324. S. Nakamura, G. Fasol, *The Blue Laser Diode* (Springer, Berlin Heidelberg New York, 1997)
- 2.325. S. Nakamura, M. Senoh, T. Mukai, Appl. Phys. Lett. **62**, 2390 (1993)
- 2.326. S. Nakamura, M. Senoh, S. Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, Y. Sugimoto, Appl. Phys. Lett. **68**, 3269 (1996)
- 2.327. M. Neuburger, I. Daumiller, T. Zimmermann, M. Kunze, G. Koley, M. Spencer, A. Dadgar, A. Krtschil, A. Krost, E. Kohn, Electron. Lett. **39**, 1614 (2003)
- 2.328. J. Newey, Comp. Semicond. **8**, (2002)
- 2.329. H.M. Ng, D. Doppalapudi, T.D. Moustakas, N.G. Weimann, L.F. Eastman, Appl. Phys. Lett., **73**, 821, (1998)
- 2.330. J. Nikaido, T. Kikkawa, S. Yokokawa, Y. Tateno, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.1
- 2.331. O. Nilsson, H.H. Mehling, R. Horn, J. Fricke, R. Hofmann, S. Müller, R. Eckstein, D. Hofmann, High Temp. High Press. **29**, 73 (1997)
- 2.332. M. Nishijima, T. Murata, Y. Hirose, M. Hikita, N. Negoro, H. Sakai, Y. Uemoto, K. Inoue, T. Tanaka, D. Ueda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 299–302
- 2.333. Nitronex, Nitronex Issued Patent, Demos 120 W Device (2003), <http://compoundsemiconductor.net/articles/news/7/10/1/1>

- 2.334. T. Nomura, H. Kambayashi, M. Masuda, S. Ishii, N. Ikeda, J. Lee, S. Yoshida, IEEE Trans. Electron Devices **53**, 2908 (2006)
- 2.335. Northrop Grumman Space Technology, Data sheet: ALH444 1–12 GHz Low Noise Amplifier (2005), <http://www.velocium.com>
- 2.336. S. Nuttinck, S. Pinel, E. Gebara, J. Laskar, M. Harris, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Munich, 2003, pp. 213–215
- 2.337. R. Oberhuber, G. Zandler, P. Vogl, Appl. Phys. Lett. **73**, 818 (1998)
- 2.338. G. O'Clock, M. Duffy, Appl. Phys. Lett. **23**, 55 (1973)
- 2.339. I. Oguzman, E. Bellotti, K. Brennan, J. Kolnik, R. Wang, P. Ruden, J. Appl. Phys. **81**, 7827 (1997)
- 2.340. I. Oguzman, K. Brennan, J. Kolnik, R. Wang, P. Ruden, in *MRS Symposium*, vol. 395, 1st International Conference on Nitride Semiconductor, Boston, 1996, pp. 733–738
- 2.341. Y. Ohno, M. Kuzuhara, IEEE Trans. Electron Devices **48**, 517 (2001)
- 2.342. K. Okamoto, H. Ohta, S. Chichibu, J. Ichihara, H. Takasu, Jpn. J. Appl. Phys. **46**, L187 (2007)
- 2.343. Y. Okamoto, Y. Ando, K. Hataya, H. Miyamoto, T. Nakayama, T. Inoue, M. Kuzuhara, Electron. Lett. **39**, 1474 (2003)
- 2.344. Y. Okamoto, Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, M. Kuzuhara, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004 pp. 1351–1354
- 2.345. Y. Okamoto, Y. Ando, H. Miyamoto, T. Nakayama, T. Inoue, M. Kuzuhara, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 225–228
- 2.346. Y. Okamoto, A. Wakejima, Y. Ando, T. Nakayama, K. Matsunaga, H. Miyamoto, Electron. Lett. **42**, 283 (2006)
- 2.347. Y. Okamoto, A. Wakejima, K. Matsunaga, Y. Ando, T. Nakayama, K. Kasahara, K. Ota, Y. Murase, K. Yamanoguchi, T. Inoue, H. Miyamoto, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 491–494
- 2.348. S. O'Leary, B. Foutz, M. Shur, U. Bhapkar, L. Eastman, J. Appl. Phys. **83**, 826 (1998)
- 2.349. S. O'Leary, B. Foutz, M. Shur, U. Bhapkar, L. Eastman, Solid-State Commun. **105**, 621 (1998)
- 2.350. J. Orton, C. Foxon, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.5, pp. 300–305
- 2.351. J. Orton, C. Foxon, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.4, pp. 294–299
- 2.352. K. Osamura, S. Naka, Y. Murakami, J. Appl. Phys. **46**, 3432 (1975)
- 2.353. C. Oxley, Solid-State Electron. **48**, 1197 (2004)
- 2.354. T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. DenBaars, J. Speck, U. Mishra, IEEE Electron Device Lett. **26**, 781 (2005)
- 2.355. T. Palacios, N. Fichtenbaum, S. Keller, S. Denbaars, U. Mishra, in *Device Research Conference*, State College, PA, 2006, pp. 99–100
- 2.356. V. Palankovski, R. Quay, *Analysis and Simulation of Heterostructure Devices* (Springer, Wien New York, 2004)
- 2.357. V. Palankovski, S. Selberherr, in *Proceedings of the European Conference on High Temperature Electronics*, Berlin, 1999, pp. 25–28

- 2.358. V. Palankovski, S. Vitanov, R. Quay, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 107–110
- 2.359. J. Palmour, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 4–7
- 2.360. J. Palmour, A. Agarwal, S. Ryu, M. Das, J. Sumakeris, A. Powell, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.1
- 2.361. J. Palmour, J. Milligan, J. Henning, S. Allen, A. Ward, P. Parikh, R. Smith, A. Saxler, M. Moore, Y. Wu, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 555–558
- 2.362. J. Palmour, S. Sheppard, R. Smith, S. Allen, W. Pribble, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IEDM Technical Digest*, Washington DC, 2001, pp. 385–388
- 2.363. A. Panda, D. Pavlidis, E. Alekseev, IEEE Trans. Electron Devices **48**, 820 (2001)
- 2.364. P. Parikh, Y. Wu, M. Moore, P. Chavarkar, U. Mishra, B. Neidhard, L. Kehias, T. Jenkins, in *Lester Eastman Conference on Abstract Book*, Newark, 2002, pp. 56–57
- 2.365. S. Pearton, C. Abernathy, B. Gila, F. Ren, J. Zavada, Y. Park, Solid-State Electron. **48**, 1965 (2002)
- 2.366. R. Pierobon, S. Buso, M. Citron, G. Meneghesso, G. Spiazzi, E. Zanoni, in *11th Hetero Structure Technical Work*, Padova, 2001, pp. 57–58
- 2.367. E. Piner, S. Singhal, P. Rajagopal, R. Therrien, J. Roberts, T. Li, A. Hanson, J. Johnson, I. Kizilyalli, K. Linthicum, in *IEDM Technical Digest*, San Francisco, 2006, pp. 411–414
- 2.368. A. Ping, Q. Chen, J. Yang, M. Khan, I. Adesida, IEEE Electron Device Lett. **19**, 54 (1998)
- 2.369. J. Piprek (ed.), *Nitride Semiconductor Devices: Principles and Simulation* (Wiley-VCH, Weinheim, 2007)
- 2.370. K. Ploog, O. Brandt, J. Vac. Sci. Technol. A **16**, 1609 (1998)
- 2.371. A. Polian, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 1.3, pp. 11–20
- 2.372. A. Polian, M. Grimsditch, I. Grzegory, J. Appl. Phys. **79**, 3343 (1996)
- 2.373. S. Pugh, D. Dugdale, S. Brand, R. Abram, J. Appl. Phys. **86**, 3768 (1999)
- 2.374. D. Pulfrey, S. Fathpour, IEEE Trans. Electron Devices **48**, 597 (2001)
- 2.375. R. Quay, K. Hess, R. Reuter, M. Schlechtweg, T. Grave, V. Palankovski, S. Selberherr, IEEE Trans. Electron Devices **48**, 210 (2001)
- 2.376. R. Quay, R. Kiefer, F. van Raay, H. Massler, S. Ramberger, S. Müller, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, in *IEDM Technical Digest*, San Francisco, 2002, pp. 673–676
- 2.377. R. Quay, A. Tessmann, R. Kiefer, R. Weber, F. van Raay, M. Kuri, M. Riessle, H. Massler, S. Müller, M. Schlechtweg, G. Weimann, in *IEDM Technical Digest*, Washington DC, 2003, pp. 567–570
- 2.378. R. Quay, F. van Raay, A. Tessmann, R. Kiefer, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings WOCSDICE*, Venice, 2007, pp. 349–352
- 2.379. S. Rajan, H. Xing, S. DenBaars, U. Mishra, D. Jena, Appl. Phys. Lett. **84** 1591 (2004)

- 2.380. M. Ramonas, A. Matulionis, L. Rota, *Semicond. Sci. Technol.* **18**, 219 (2003)
- 2.381. R. Reeber, K. Wang, *MRS Internet J. Nitride Semicond. Res.* **6**, 3 (2001)
- 2.382. F. Ren, C. Abernathy, J.V. Hove, P. Chow, R. Hickman, J. Klaasen, R. Kopf, H. Cho, K. Jung, J.L. Roche, R. Wilson, J. Han, R. Shul, A. Baca, S. Pearton, *MRS Internet J. Nitride Semicond. Res.* **3**, 41 (1998)
- 2.383. F. Ren, J. Han, R. Hickman, J.V. Hove, P. Chow, J. Klaasen, J. LaRoche, K. Jung, H. Cho, X. Cao, S. Donovan, R. Kopf, R. Wilson, A. Baca, R. Shul, L. Zhang, C. Willison, C. Abernathy, S. Pearton, *Solid-State Electron.* **44**, 239 (2000)
- 2.384. M. Rosker, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 13–16
- 2.385. M. Rosker, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 1.2
- 2.386. M. Rosker, in *IEEE RF IC Symposium Digest*, Honolulu, 2007, pp. 159–162
- 2.387. P. Roussel, *Comp. Semicond.* **9**, 20 (2003)
- 2.388. T. Ruemenapp, D. Peier, in *11th International Symposium on High-Voltage Engineering*, London, 1999, pp. 4.373–4.376
- 2.389. P. Ruterana, M. Albrecht, J. Neugebauer (eds.), *Nitride Semiconductors: Handbook on Materials and Device* (Wiley-VCH, Weinheim, 2003)
- 2.390. P. Ruterana, A. Sanchez, G. Nouet, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 8, pp. 379–438
- 2.391. F. Sacconi, A.D. Carlo, H. Morkoc, *IEEE Trans. Electron Devices* **48**, 450 (2001)
- 2.392. F. Sacconi, A. Di Carlo, F. Della Sala, P. Lugli, in *Proceedings of the European GaAs Related Compounds on Application Symposium GAAS*, Paris, 2000, pp. 620–623
- 2.393. T. Sadi, R. Kelsall, N. Pilgrim, *IEEE Trans. Electron Devices* **53**, 2892 (2006)
- 2.394. W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, T. Domon, I. Omura, M. Yamaguchi, in *IEDM Technical Digest*, Washington DC, 2005, pp. 586–589
- 2.395. W. Saito, I. Omura, T. Domon, K. Tsuda, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 253–256
- 2.396. W. Saito, I. Omura, T. Ogura, H. Ohashi, *Solid-State Electron.* **48**, 1555 (2004)
- 2.397. W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, in *IEDM Technical Digest*, Washington DC, 2003, pp. 587–590
- 2.398. W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, Y. Saito, I. Omura, M. Yamaguchi, in *IEDM Technical Digest*, Washington DC, 2007, pp. 869–873
- 2.399. R. Sandhu, M. Wojtowicz, I. Smorchkova, M. Barsky, R. Tsai, J. Yang, H. Wang, M. Khan, in *Device Research Conference*, Santa Barbara, 2002, pp. 27–28
- 2.400. B. Santic, *Semicond. Sci. Technol.* **18**, 219 (2003)
- 2.401. P. Saunier, in *Proceedings of European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 543–546
- 2.402. J. Schalwig, G. Müller, M. Eickhoff, O. Ambacher, M. Stutzmann, *Sensors Actuators B* **87**, 425 (2002)
- 2.403. L. Schowalter, S. Schujman, W. Liu, M. Goorsky, M. Wood, J. Granusky, F. Shahedipour-Sandvik, *Phys. Stat. Sol. A* **203**, 1667 (2006)

- 2.404. L. Schowalter, G. Slack, J. Whitlock, K. Morgan, S. Schujman, B. Raghothamachar, M. Dudley, K. Evans, Phys. Stat. Sol. C **0**, 1997 (2003)
- 2.405. M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, H. Leier, in *Proceedings Diamond*, Porto, 2000, pp. 744–749
- 2.406. S. Selberherr, *Analysis and Simulation of Semiconductor Devices* (Springer, Wien New York, 1984)
- 2.407. Sensor Electronic Technologies, SET Wins Contract for Device R&D on AlN. Comp. Semicond. **8**, (2004)
- 2.408. C. Sevik, C. Bulutay, Semicond. Sci. Technol. **19**, S188 (2004)
- 2.409. P. Shah, D. Smith, T. Griffin, K. Jones, S. Sheppard, IEEE Trans. Electron Devices **47**, 308 (2000)
- 2.410. W. Shan, J. Ager, K. Yu, W. Walukiewicz, E. Haller, M. Martin, W. McKinney, W. Yang, J. Appl. Phys. **85**, 8505 (1999)
- 2.411. A. Shanware, J. McPherson, M. Visokay, J. Chambers, A. Rotondaro, H. Bu, M. Bevan, R. Khamankar, L. Colombo, in *IEDM Technical Digest*, Washington DC, 2001, pp. 137–140
- 2.412. J. Shealy, J. Smart, M. Poulton, R. Sadler, D. Grider, S. Gibb, B. Hosse, B. Sousa, D. Halchin, V. Steel, P. Garber, P. Wilkerson, B. Zaroff, J. Dick, T. Mercier, J. Bonaker, M. Hamilton, C. Greer, M. Isenhour, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 243–246
- 2.413. B. Shelton, D. Lambert, J. Huang, M. Wong, U. Chowdhury, T. Zhu, H. Kwon, Z. Weber, M. Benarama, M. Feng, R. Dupuis, IEEE Trans. Electron Devices **48**, 490 (2001)
- 2.414. L. Shen, S. Heikman, B. Moran, R. Coffie, N. Zhang, D. Buttari, I. Smorchkova, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **22**, 457 (2001)
- 2.415. K. Shenai, R. Scott, B. Baliga, IEEE Trans. Electron Devices **36**, 1811 (1989)
- 2.416. S. Sheppard, K. Doverspike, W. Pribble, S. Allen, J. Palmour, L. Kehias, T. Jenkins, IEEE Electron Device Lett. **20**, 161 (1999)
- 2.417. J. Sheu et al., J. Phys. Condens. Mater. **14**, R657 (2002)
- 2.418. M. Shin, R. Trew, Electron. Lett. **31**, 498 (1995)
- 2.419. M. Shur, *GaAs Devices and Circuits* (Plenum, New York, 1987)
- 2.420. M. Shur, A. Bykhovski, R. Gaska, Solid-State Electron. **44**, 205 (2000)
- 2.421. M. Shur, R. Gaska, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 137–140
- 2.422. M. Shur, M. Khan, MRS Bulletin **22**, 44 (1997)
- 2.423. E. Sichel, J. Pankove, J. Phys. Chem. Solids **38**, 333 (1977)
- 2.424. SiCrystal AG, Silicon Carbide Product Specification (2004), <http://www.sicrystal.com>
- 2.425. G. Simin, X. Hu, A. Tarakji, J. Zhang, A. Koudymov, S. Saygi, J. Yang, A. Khan, M. Shur, R. Gaska, Appl. Phys. Lett. **40**, L1142 (2001)
- 2.426. G. Simin, A. Koudymov, H. Fatima, J. Zhang, J. Yang, M. Khan, X., A. Tarakji, R. Gaska, M. Shur, IEEE Electron Device Lett. **23**, 458 (2002)
- 2.427. R. Singh, J. Cooper, M. Melloch, T. Chow, J. Palmour, IEEE Trans. Electron Devices **49**, 665 (2002)
- 2.428. G. Slack, R. Tanzilli, R. Pohl, J. Vandersande, J. Phys. Chem. Solids **48**, 641 (1987)
- 2.429. L. Smith, R. Davis, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 10.3, pp. 288–292

- 2.430. I. Smorchkova, M. Wojtowicz, R. Sandhu, R. Tsai, M. Barsky, C. Namba, P. Liu, R. Dia, M. Truong, D. Ko, J. Wang, A. Khan, IEEE Trans. Microwave Theory and Tech. **51**, 665 (2003)
- 2.431. I. Smorchkova, M. Wojtowicz, R. Sandhu, R. Tsai, M. Barsky, C. Namba, P. Liu, R. Dia, M. Truong, D. Ko, J. Wang, A. Khan, in *IEDM Technical Digest*, Washington DC, 2001, pp. 17.5.1–17.5.3
- 2.432. J. Song, D. Leem, S. Kim, J. Kwak, O. Nam, Y. Park, T. Seong, Solid-State Electron. **48**, 1597 (2004)
- 2.433. M. Spencer, J. Palmour, C. Carter, IEEE Trans. Electron Devices **49**, 940 (2002)
- 2.434. G. Spiazzini, S. Buso, M. Citron, M. Corradini, R. Pierobon, IEEE Trans. Power Electron. **18**, 1249 (2003)
- 2.435. D. Storm, D. Katzer, S. Binari, B. Shanabrook, X. Xu, D. McVey, R. Vaudo, G. Brandes, Electron. Lett. **40**, 1226 (2004)
- 2.436. D. Streit, A. Gutierrez-Aitken, M. Wojtowicz, R. Lai, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 5–8
- 2.437. S. Strite, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 9.5, pp. 272–275
- 2.438. C. Suh, Y. Dora, N. Fichtenbaum, L. McCarthy, S. Keller, U. Mishra, in *IEDM Technical Digest*, San Francisco, 2006, pp. 911–913
- 2.439. G. Sullivan, M. Chen, J. Higgins, J. Yang, Q. Chen, R. Pierson, B. McDermott, IEEE Electron Device Lett. **19**, 198 (1998)
- 2.440. K. Sundaram, M. Deen, W. Brown, R. Sah, E. Poindexter, D. Misra (ed.), *Silicon Nitride and Silicon Dioxide Thin Insulating Films* (Electrochemical Society, 1999)
- 2.441. M. Suzuki, T. Uenoyama, A. Yanase, Phys. Rev. B **52**, 8132 (1995)
- 2.442. M. Suzuki, T. Uenoyama, A. Yanase, Phys. Rev. B **58**, 10064 (1998)
- 2.443. S. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley, New York, 1981)
- 2.444. K. Takagi, K. Masuda, Y. Kashiwabara, H. Sakurai, K. Matsushita, S. Takatsuka, H. Kawasaki, Y. Takada, K. Tsuda, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 265–268
- 2.445. H. Takaya, K. Miyagi, K. Hamada, in *IEDM Technical Digest*, San Francisco, 2006, pp. 923–927
- 2.446. T. Tanaka, Y. Koji, T. Meguro, Y. Otoki, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 295–298
- 2.447. O. Tang, K. Duh, S. Liu, P. Smith, W. Kopp, T. Rogers, D. Richard, in *GaAs IC Symposium Technical Digest*, Orlando, 1996, pp. 115–118
- 2.448. T. Taniguchi, J. Tanaka, O. Mishima, T. Ohsawa, S. Yamaoka, Appl. Phys. Lett. **62**, 576 (1993)
- 2.449. T. Tansley, in *Properties of Group III Nitrides*, No. 11 in EMIS Data reviews Series, ed. by J. Edgar (IEE INSPEC, London, 1994), Sect. 1.5, pp. 35–40
- 2.450. T. Tansley, C. Foley, J. Appl. Phys. **59**, 3241 (1986)
- 2.451. T. Tansley, E. Goldys, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), pp. 123–128
- 2.452. T. Tansley, E. Goldys, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 4.5, pp. 135–136

- 2.453. T. Tansley, E. Goldys, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 4.4, pp. 129–134
- 2.454. F. Temcamani, P. Pouvil, O. Noblanc, C. Brylinski, P. Bannelier, B. Darges, J. Prigent, in *IEEE International Microwave Symposium Digest*, Phoenix, 2001, pp. 641–644
- 2.455. D. Theron, C. Gaquiere, J. de Jaeger, S. Delage, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 547–550
- 2.456. R. Therrien, S. Singhal, W. Nagy, J. Marquart, A. Chaudhari, K. Linthicum, J. Johnson, A. Hanson, J. Riddle, P. Rajagopol, B. Preskenis, O. Zhitova, J. Williamson, I. Kizilyalli, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 710–713
- 2.457. V. Tilak, B. Green, V. Kaper, H. Kim, T. Prunty, J. Smart, J. Shealy, L. Eastman, *IEEE Electron Device Lett.* **22**, 504 (2001)
- 2.458. V. Tilak, K. Matocha, P. Sandvik, *Phys. Stat. Sol. A* **3**, 548 (2006)
- 2.459. N. Tipirneni, A. Koudymov, V. Adivaharan, J. Yang, G. Simin, M. Khan, *IEEE Electron Device Lett.* **27**, 716 (2006)
- 2.460. L. Tolbert, B. Ozpinecci, S. Islam, M. Chinthaivali, in *IASTED International Conference on Power and Energy Systems*, Palm Springs, 2003, pp. 317–321
- 2.461. A. Tomchenko, G. Harmer, B. Marquis, J. Allen, *Sensors Actuators B* **93**, 126 (2003)
- 2.462. R. Trew, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1811–1814
- 2.463. R. Trew, Proc. IEEE **90**, 1032 (2002)
- 2.464. R. Trew, *IEEE Trans. Electron Devices* **52**, 638 (2005)
- 2.465. R. Trew, M. Shin, V. Gatto, *Solid-State Electron.* **41**, 1561 (1997)
- 2.466. Triquint Semiconductor, Advanced Product Information TGA2505 (2006), <http://www.triquint.com>
- 2.467. Triquint Semiconductors, Triquint Semiconductor and Lockheed Martin Announce Advanced Gallium Nitride Process with Improved Power, Efficiency, Stability (2003), <http://www.triquint.com/investors/press/dspPressRelease.cfm?pressid=174>
- 2.468. Triquint Semiconductors, 6.5 Watt Ku Band Power Amplifier (2004), <http://www.triquint.com>
- 2.469. D. Ueda, T. Murata, M. Hikita, S. Nakazawa, M. Kuroda, H. Ishida, M. Yanagihara, K. Inoue, T. Ueda, Y. Uemoto, T. Tanaka, T. Egawa, in *IEDM Technical Digest*, Washington DC, 2005, pp. 377–380
- 2.470. H. Ueda, M. Suimoto, T. Uesugi, T. Kachi, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 37–41
- 2.471. Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, in *IEDM Technical Digest*, San Francisco, 2006, pp. 907–910
- 2.472. Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, M. Li, T. Ueda, T. Tanaka, D. Ueda, in *IEDM Technical Digest*, Washington DC, 2007, pp. 861–864
- 2.473. N. Ui, S. Sano, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 718–721
- 2.474. United Monolithic Semiconductors, Data sheet: 7–13 GHz Low Noise Amplifier (2000), <http://www.ums-gaas.com>

- 2.475. C. van de Walle, J. Neugebauer, C. Stampfl, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. 8.1, pp. 275–280
- 2.476. F. van Raay, R. Quay, R. Kiefer, H. Walcher, O. Kappeler, M. Seelmann-Eggebert, S. Müller, M. Schlechtweg, G. Weimann, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS 2005*, Paris, pp 373 - 376
- 2.477. T. Veal, P. Jefferson, L. Piper, C. McConville, T. Joyce, P. Chalker, L. Con-sidine, H. Lu, W. Schaff, Appl. Phys. Lett. **89**, 202110 (2006)
- 2.478. N. Vellas, C. Gaquiere, Y. Guhel, M. Werquin, D. Ducatteau, B. Boudart, J. Jaeger, Z. Bougrioua, M. Germain, M. Leys, S. Borghs, in *Proceedings of the European GaAs Related Compound Application Symposium on GAAS*, Milano, 2002, pp. 25–28
- 2.479. A. Vescan, R. Dietrich, A. Wieszt, A. Schurr, H. Leier, E. Piner, J. Redwing, Electron. Lett. **36**, 1234 (2000)
- 2.480. R. Vetur, PhD thesis, University of California Santa Barbara, Santa Barbara, 2000
- 2.481. R. Vetur, J. Shealy, D. Green, J. McKenna, J. Brown, S. Gibb, K. Leverich, P. Garber, M. Poulton, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 714–717
- 2.482. R. Vetur, Y. Wei, D. Green, S. Gibb, T. Mercier, K. Leverich, P. Garber, M. Poulton, J. Shealy, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 487–490
- 2.483. R. Vetur, N. Zhang, S. Keller, U. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001)
- 2.484. F. Villard, J. Pringent, E. Morvan, C. Dua, C. Brylinski, F. Temcamani, P. Pouvil, IEEE Trans. Microwave Theory Tech. **51**, 1129 (2003)
- 2.485. I. Vurgaftman, J. Meyer, J. Appl. Phys. **94**, 3675 (2003)
- 2.486. I. Vurgaftman, J. Meyer, L. Ram-Mohan, J. Appl. Phys. **89**, 5815 (2001)
- 2.487. A. Wakejima, K. Matsunaga, Y. Okamoto, Y. Ando, T. Nakayama, T. Kasahara, H. Miyamoto, Electron. Lett. **41**, 1004 (2005)
- 2.488. A. Wakejima, K. Matsunaga, Y. Okamoto, Y. Ando, T. Nakayama, H. Miyamoto, Electron. Lett. **41**, 1371 (2005)
- 2.489. D. Walker, X. Zhang, A. Saxler, P. Kung, J. Xu, M. Razeghi, Appl. Phys. Lett. **70**, 949 (1997)
- 2.490. C. Wang, L. Yu, S. Lau, E. Yu, W. Kim, A. Botchkarev, H. Morkoc, Appl. Phys. Lett. **72**, 1211 (1998)
- 2.491. K. Watanabe, T. Taniguchi, H. Kanda, Phys. Stat. Sol. A **201**, 2561 (2004)
- 2.492. M. Weber, L. Tirino, K. Brennan, IEEE Trans. Electron Devices **50**, 2202 (2003)
- 2.493. N. Weimann, L. Eastman, D. Doppalapudi, H. Ng, T. Moustakas, J. Appl. Phys. **83**, 3656 (1998)
- 2.494. C. Weitzel, in *IEDM Technical Digest*, San Francisco, 1998, pp. 51–54
- 2.495. C. Weitzel, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 285–288
- 2.496. R. Wentorf, J. Chem. Phys. **36**, 1990 (1994)
- 2.497. R. Wentzcovitch, K. Chang, M. Cohen, Phys. Rev. B **34**, 1071 (1986)
- 2.498. C. Wetzel, T. Takeuchi, H. Amago, I. Akasaki, Phys. Rev. B **61**, 2159 (2000)

- 2.499. C. Wood, D. Jena (eds.), *Polarization Effects in Semiconductors* (Springer, New York, 2008)
- 2.500. M. Wraback, H. Shen, J. Carrano, T. Li, J. Campbell, M. Schurman, I. Ferguson, *Appl. Phys. Lett.* **76**, 1155 (2000)
- 2.501. J. Wu, W. Walukiewicz, K. Yu, J. Ager, E. Haller, H. Lu, W. Schaff, *Appl. Phys. Lett.* **80**, 4741 (2002)
- 2.502. Y. Wu, Dissertation, University of California Santa Barbara, Santa Barbara, 1997
- 2.503. Y.-F. Wu, S. Wood, R. Smith, S. Sheppard, S.T. Allen, P. Parikh, J. Milligan, in *IEDM Technical Digest*, San Francisco, 2006, pp. 419–421
- 2.504. Y. Wu, D. Kapolnek, J. Ibbetson, P. Parikh, B. Keller, U. Mishra, *IEEE Trans. Electron Devices* **48**, 586 (2001)
- 2.505. Y. Wu, B. Keller, P. Fini, J. Pusl, M. Le, N. Nguyen, C. Nguyen, D. Widman, S. Keller, S. Denbaars, U. Mishra, *Electron. Lett.* **33**, 1742 (1997)
- 2.506. Y. Wu, B. Keller, S. Keller, D. Kapolnek, S. Denbaars, U. Mishra, *IEEE Electron Device Lett.* **17**, 455 (1996)
- 2.507. Y. Wu, B. Keller, S. Keller, N. Nguyen, M. Le, C. Nguyen, T. Jenkins, L. Kehias, S. Denbaars, U. Mishra, *IEEE Electron Device Lett.* **18**, 438 (1997)
- 2.508. Y. Wu, M. Moore, A. Saxler, T. Wisleder, U.K. Mishra, P. Parikh, in *IEDM Technical Digest*, Washington DC, 2005, pp. 583–585
- 2.509. Y. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, A. Burk, in *IEDM Technical Digest*, Washington DC, 2007, pp. 405–408
- 2.510. Y. Wu, M. Moore, A. Saxler, P. Smith, P. Chavarkar, P. Parikh, in *IEDM Technical Digest*, Washington DC, 2003, pp. 579–581
- 2.511. Y. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh, in *Device Research Conference*, State College, PA, 2006, pp. 151–152
- 2.512. Y. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, P. Parikh, *IEEE Electron Device Lett.* **25**, 117 (2004)
- 2.513. H. Xing, P. Chavarkar, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **24**, 141 (2003)
- 2.514. H. Xing, D. Jena, M. Rodwell, U. Mishra, *IEEE Electron Device Lett.* **24**, 4 (2003)
- 2.515. H. Xu, C. Sanabria, A. Chini, S. Keller, U. Mishra, R. York, *IEEE Microw. Wireless Compon. Lett.* **14**, 262 (2004)
- 2.516. I. Yaacov, Y. Seck, U. Mishra, S. DenBaars, *J. Appl. Phys.* **95**, 2073 (2004)
- 2.517. S. Yamakawa, S. Aboud, M. Saraniti, S. Goodnick, *Semicond. Sci. Technol.* **19**, S475 (2004)
- 2.518. T. Yamamoto, E. Mitani, K. Inoue, M. Nishi, S. Sano, in *Proceedings of the European Microwave Integrated Circuits Conference* Munich, 2007, pp 173–175
- 2.519. K. Yamanaka, K. Iyomasa, H. Ohtsuka, M. Nakayama, Y. Tsuyama, T. Kunii, Y. Kano, T. Takagi, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 241–244
- 2.520. K. Yamanaka, K. Mori, K. Iyomasa, H. Ohtsuka, M. Nakayama, Y. Kamo, Y. Isota, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1251–1254
- 2.521. H. Ye, G. Wicks, P. Fauchet, *Appl. Phys. Lett.* **74**, 711 (1999)
- 2.522. Y. Yeo, T. Chong, M. Li, *J. Appl. Phys.* **83**, 1429 (1996)
- 2.523. Y. Yeo, T. Chong, M. Li, W. Fan, *J. Appl. Phys.* **84**, 1813 (1998)

- 2.524. I. Yonenaga, MRS Internet J. Nitride Semicond. Res. **7**, 6 (2002)
- 2.525. E. Yu, G. Sullivan, P. Asbeck, C. Wang, D. Qiao, S. Lau, Appl. Phys. Lett. **71**, 2794 (1997)
- 2.526. H. Yu, L. McCarthy, S. Rajan, S. Keller, S. DenBaars, J. Speck, U. Mishra, IEEE Electron Device Lett. **26**, 283 (2005)
- 2.527. T. Yu, K. Brennan, IEEE Trans. Electron Devices **50**, 315 (2003)
- 2.528. A. Zhang, L. Rowland, E. Kaminsky, J. Kretchmer, V. Tilak, A. Allen, B. Edward, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 251–254
- 2.529. A. Zhang, L. Rowland, E. Kaminsky, J. Tucker, R. Beaupre, J. Kretchmer, J. Garrett, A. Vertiatchikh, G. Koley, H. Cha, A. Allen, J. Cook, J. Foppes, B. Edward, J. Electron. Mater. **32** 437 (2003)
- 2.530. H. Zhang, E. Miller, E. Yu, C. Poblenz, J. Speck, Appl. Phys. Lett. **84**, 4644 (2004)
- 2.531. L. Zhang, L. Lester, A. Baca, R. Shul, P. Chang, C. Wilson, U. Mishra, S. DenBaars, J. Zolper, IEEE Trans. Electron Devices **47**, 507 (2000)
- 2.532. F. Zhao, I. Perez-Wurfl, H. Chih-Fang, J. Torvik, B. Zeghbroek, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 2035–2038
- 2.533. B. Zhou, K. Butcher, X. Li, T. Tansley, Solid-State Electron. **41**, (1997)
- 2.534. T. Zimmermann, M. Neuburger, M. Kunze, I. Daumiller, A. Denisenko, A. Dadgar, A. Krost, E. Kohn, IEEE Electron Device Lett. **25**, 450 (2004)
- 2.535. J. Zolper, Wide Bandgap Semiconductor RF Electronics Technology, MTO Industry Briefing, Sept. 2001
<http://www.compoundsemiconductor.net/cws/article/magazine/11332>

References of Chapter 3

- 3.1. A. Alam, O. Schön, B. Schineller, M. Heuken, H. Jürgensen, Phys. Stat. Sol. A **180**, 109 (2000)
- 3.2. O. Ambacher J. Physics D **31**, 2653 (1998)
- 3.3. B. Ansell, L. Harrison, C. Foxon, J. Harris, T. Cheng, Electron. Lett. **36**, 1237 (2000)
- 3.4. J. Antoszewski, M. Gracey, J. Dell, L. Farone, T. Fisher, G. Parish, Y. Wu, U. Mishra, J. Appl. Phys. **87**, 3900 (2000)
- 3.5. J. Ao, T. Wang, D. Kikuta, Y. Liu, S. Sakai, Y. Ohno, Jpn. J. Appl. Phys. **42**, 1588 (2003)
- 3.6. A. Armstrong, A. Arehart, B. Moran, S. DenBaars, U. Mishra, J. Speck, S. Ringel, Appl. Phys. Lett. **84**, 374 (2004)
- 3.7. S. Arulkumaran, M. Miyoshi, T. Egawa, H. Ishikawa, T. Jimbo, IEEE Electron Device Lett. **24**, 497 (2003)
- 3.8. S. Arulkumaran, M. Sakai, T. Egawa, H. Ishikawa, T. Jimbo, T. Shibata, K. Asai, S. Sumiya, Y. Kuraoka, M. Tanaka, O. Oda, Appl. Phys. Lett. **81**, 1131 (2002)
- 3.9. R. Balmer, K. Hilton, K. Nash, M. Uren, D. Wallis, D. Lee, A. Wells, M. Missous, T. Martin, Semicond. Sci. Technol. **19**, L65 (2004)
- 3.10. J. Bardwell, Y. Liu, H. Tang, J. Webb, S. Rolfe, J. Lapointe, Electron. Lett. **39**, 564 (2003)
- 3.11. A. Barnes, D. Hayes, M. Uren, T. Martin, R. Balmer, D. Wallis, K. Hilton, J. Powell, W. Phillips, A. Jimenez, E. Munoz, M. Kuball, S. Rajasingam, J. Pomeroy, N. Labat, N. Malbert, P. Rice, A. Wells, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 3.12. J. Bernat, R. Pierobon, M. Marso, J. Flynn, G. Brandes, G. Meneghesso, E. Zanoni, P. Kordos, Phys. Stat. Sol. C **2**, 2676 (2005)
- 3.13. J. Bernat, M. Wolter, M. Marso, J. Flynn, G. Brandes, P. Kordos, Electron. Lett. **40**, 78 (2004)
- 3.14. A. Bhuiyan, A. Hashimoto, A. Yamamoto, J. Appl. Phys. **94**, 2779 (2003)
- 3.15. Z. Bougrioua, M. Azize, P. Lorenzini, M. Laügt, H. Haas, Phys. Stat. Sol. A **202**, 536 (2005)
- 3.16. P. Bove, H. Lahreche, J. Thuret, F. Letertre, B. Faure, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 4.3

- 3.17. O. Brandt, R. Muralidharan, P. Waltereit, A. Thamm, A. Trambert, H. von Kiedrowski, K. Ploog, *Appl. Phys. Lett.* **75**, 4019 (1999)
- 3.18. E. Brazel, M. Chain, V. Narayananamurti, *Appl. Phys. Lett.* **74**, 2367 (1999)
- 3.19. C. Buchheim, R. Goldhahn, G. Gobsch, K. Tonisch, V. Cimalla, F. Niebelshütz, O. Ambacher *Appl. Phys. Lett.* **92**, 013510 (2008)
- 3.20. C. Buchheim, A. Winzer, R. Goldhahn, G. Gobsch, O. Ambacher, A. Link, M. Eickhoff, M. Stutzmann, *Thin Film Solids* **450**, 155 (2004)
- 3.21. C. Bulutay, B. Ridley, N. Zakhleniuk, *Phys. Rev. B* **62**, 15754 (2000)
- 3.22. E. Calleja, F. Sanchez, D. Basak, M. Sanchez-Garcia, E. Munoz, I. Izpura, F. Calle, J. Tijero, J. Sanchez-Rojas, *Phys. Rev. B* **55**, 4689 (1997)
- 3.23. P. Cantu, S. Keller, U. Mishra, S. DenBaars, *J. Appl. Phys.* **82**, 3683 (2003)
- 3.24. H. Chen, R. Feenstra, J. Northrup, J. Neugebauer, D. Greve, *MRS Internet J. Nitride Semicond. Res.* **6**, 11 (2001)
- 3.25. A. Chini, R. Coffie, G. Meneghesso, E. Zanoni, D. Buttari, S. Heikman, S. Keller, U. Mishra, *Electron. Lett.* **39**, 625 (2003)
- 3.26. A. Chini, S. Rajan, M. Wong, Y. Fu, J. Speck, U. Mishra, in *Device Research Conference*, Santa Barbara, 2005, pp. 63–64
- 3.27. A. Chini, J. Wittich, S. Heikman, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **25**, 55 (2004)
- 3.28. Y. Choi, M.P.H. Cha, B. Peres, M. Spencer, L. Eastman, *IEEE Trans. Electron Devices* **53**, 2926 (2006)
- 3.29. E. Chumbes, A. Schremer, J. Smart, Y. Wang, N. MacDonalds, D. Hogue, J. Komiak, S. Lichwalla, R. Leoni, J. Shealy, *IEEE Trans. Electron Devices* **48**, 420 (2001)
- 3.30. R. Coffie, D. Buttari, S. Heikmann, S. Keller, A. Chini, L. Shen, U. Mishra, *IEEE Electron Device Lett.* **23**, 588 (2002)
- 3.31. O. Contreras, F. Ponec, J. Christen, A. Dadgar, A. Krost, *Appl. Phys. Lett.* **81**, 4712 (2002)
- 3.32. Y. Cordier, F. Semond, P. Lorenzini, N. Grandjean, F. Natali, B. Damilano, J. Massies, V. Hoel, A. Minko, N. Vellas, C. Gaquiere, J. Jaeger, B. Dessertene, S. Cassette, M. Surrugue, D. Adam, J. Grattepain, R. Aubry, S. Delage, *J. Cryst. Growth* **251**, 811 (2003)
- 3.33. A. Corrion, C. Poblenz, P. Waltereit, T. Palacios, S. Rajan, U. Mishra, J. Speck, *IEICE Trans. Electron.* **E89**, 906 (2006)
- 3.34. A. Dadgar, A. Strittmatter, J. Bläsing, M. Poschenrieder, O. Contreras, P. Veit, T. Riemann, F. Bertram, A. Reiher, A. Krtschil, A. Diez, T. Hempel, T. Finger, A. Kasic, M. Schubert, D. Bimberg, F. Ponce, J. Christen, A. Krost, *Phys. Stat. Sol. B* **0**, 1583 (2003)
- 3.35. E. Danielsson, C. Zetterling, M. Östling, A. Nikolaev, I. Nikitina, V. Dmitriev, *IEEE Trans. Electron Devices* **48**, 444 (2001)
- 3.36. R. Davis, A. Roskowski, E. Preble, J. Speck, B. Heying, J. Freitas, E. Glaser, W. Carlos, *Proc. IEEE* **90**, 993 (2004)
- 3.37. Y. Dikme, M. Fieger, F. Jessen, A. Szymakowski, H. Kalisch, J. Woitok, P. van Gemmern, P. Javorka, M. Marso, R. Jansen, M. Heuken, *Phys. Stat. Sol. C* **0**, 2385 (2003)
- 3.38. W. Doolittle, S. Kang, A. Brown, *Solid-State Electron.* **44**, 229 (2000)
- 3.39. L. Eastman, V. Tilak, J. Smart, B. Green, E. Chumbes, R. Dimitrov, H. Kim, O. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. Schaff, J. Shealy, *IEEE Trans. Electron Devices* **48**, 479 (2001)

- 3.40. L. Eastman, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 2273–2275
- 3.41. C. Elsass, T. Mates, B. Heying, C. Poblenz, P. Fini, P. Petroff, S. DenBaars, J. Speck, *Appl. Phys. Lett.* **77**, 3167 (2000)
- 3.42. D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, J. Johnson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.3
- 3.43. E. Faraclas, S. Islam, A. Anwar, *Solid-State Electron.* **48**, 1849 (2004)
- 3.44. Q. Fareed, R. Gaska, J. Mickevicius, G. Tamulaitis, M. Shur, M. Khan, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, pp. 301–305
- 3.45. Z. Feng, S. Cai, K. Chen, K. Lau, *IEEE Electron Device Lett.* **26**, 870 (2006)
- 3.46. M. Fieger, Y. Dikme, F. Jessen, H. Kalisch, A. Noculak, A. Szymakowski, P.V. Gemmern, B. Faure, C. Richtarch, F. Letertre, M. Heuken, R. Jansen, *Phys. Stat. Sol. C* **2**, 2607 (2005)
- 3.47. J. Flynn, D. Keogh, F. Tamweber, M. Chriss, J. Redwing, in *WBG Semiconductors Workshop*, Copper Mountain, 2000, pp. n.a.
- 3.48. J. Flynn, H. Xin, J. Dion, E. Hutchins, H. Antunes, L. Corso, R.V. Egas, G. Brandes, *Phys. Stat. Sol. C* **0**, 2327 (2003)
- 3.49. S. Fu, Y. Chen, *Appl. Phys. Lett.* **85** 1523 (2004)
- 3.50. A. Georgakilas, H. Ng, P. Komminou, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 3, pp. 107–192
- 3.51. P. Gibart, B. Beaumont, P. Vennegues, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 2, pp. 45–106
- 3.52. J. Gillespie, R. Fitch, N. Moser, T. Jenkins, J. Sewell, D. Via, A.C.A. Dabiran, P. Chow, A. Osinsky, M. Mastro, D. Tsvetkov, V. Soukhovcev, A. Usikov, V. Dmitriev, B. Luo, S. Pearton, F. Ren, *Solid-State Electron.* **47**, 1859 (2003)
- 3.53. N. Gmeinwieser, K. Engl, P. Gottfriedsen, U. Schwarz, J. Zweck, W. Wegscheider, S. Miller, H. Lugauer, A. Leber, A. Weimar, A. Lell, V. Härlé, *J. Appl. Phys.* **96**, 3666 (2004)
- 3.54. W. Götz, N. Johnson, D. Bour, C. Chen, H. Liu, C. Kuo, W. Imler, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 443–454
- 3.55. W. Götz, N. Johnson, M. Bremser, R. Davis, *Appl. Phys. Lett.* **69**, 2379 (1996)
- 3.56. W. Götz, N. Johnson, C. Chen, H. Liu, C. Kuo, W. Imler, *J. Appl. Phys.* **68**, 3144 (1996)
- 3.57. D. Green, , S. Gibb, B. Hosse, R. Vetur, D. Grider, J. Smart, *J. Cryst. Growth* **285**, 3144 (2004)
- 3.58. P. Grudowski, A. Holmes, C. Eiting, R. Dupuis, *J. Appl. Phys.* **69**, 3626 (1996)
- 3.59. A.D. Hanser, R.F. Davis in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. B2.2, pp. 386–395

- 3.60. P. Hansen, Y. Strausser, A. Erickson, E. Tarsa, P. Kozodoy, E. Brazel, J. Ibbetson, U. Mishra, V. Narayananamurti, S. DenBaars, J. Speck, *Appl. Phys. Lett.* **72**, 2247 (1998)
- 3.61. A. Hanson, S. Stockman, G. Stillman, *IEEE Electron Device Lett.* **13**, 504 (1992)
- 3.62. T. Hashizume, *J. Appl. Phys.* **94**, 431 (2003)
- 3.63. S. Heikman, S. Keller, S. DenBaars, U. Mishra, *Appl. Phys. Lett.* **81**, 439 (2002)
- 3.64. S. Heikman, PhD thesis, University of California Santa Barbara, Santa Barbara, 2002
- 3.65. E. Henriksen, S. Syed, Y. Ahmadian, M. Manfra, K. Baldwin, A. Sergent, R. Molnar, H. Stormer, *Appl. Phys. Lett.* **86**, 252108 (2005)
- 3.66. B. Heying, R. Averbeck, L. Chen, E. Haus, H. Riechert, J. Speck, *J. Appl. Phys.* **88**, 1855 (2000)
- 3.67. B. Heying, I. Smorchkova, C. Poblenz, C. Elsass, P. Fini, S. DenBaars, U. Mishra, J. Speck, *Appl. Phys. Lett.* **77**, 2885 (2000)
- 3.68. A. Hierro, A. Arehart, B. Heying, M. Hansen, U. Mishra, S. DenBaars, J. Speck, S. Ringel, *Appl. Phys. Lett.* **80**, 805 (2002)
- 3.69. A. Hierro, A. Arehart, B. Heying, M. Hansen, J. Speck, U. Mishra, S. Denbaars, S. Ringel, *Phys. Stat. Sol. B* **228**, 309 (2001)
- 3.70. M. Higashiwaki, S. Anantathanasarn, N. Negoro, E. Sano, H. Hasegawa, K. Kumakura, T. Makimoto, *Jpn. J. Appl. Phys.* **43**, L1147 (2004)
- 3.71. M. Higashiwaki, T. Matsui, *Jpn. J. Appl. Phys.* **41**, L540 (2002)
- 3.72. M. Higashiwaki, T. Matsui, *Jpn. J. Appl. Phys.* **43**, L768 (2004)
- 3.73. M. Higashiwaki, T. Matsui, *J. Cryst. Growth* **252**, 128 (2003)
- 3.74. M. Higashiwaki, T. Matsui, *J. Cryst. Growth* **251**, 494 (2003)
- 3.75. M. Higashiwaki, T. Matsui, *Jpn. J. Appl. Phys.* **43**, L1147 (2004)
- 3.76. M. Higashiwaki, T. Matsui, *J. Cryst. Growth* **269**, 162 (2004)
- 3.77. M. Higashiwaki, T. Matsui, *Jpn. J. Appl. Phys.* **44**, L475 (2005)
- 3.78. T. Inoue, T. Nakayama, Y. Ando, M. Kosaki, H. Miwa, K. Hirata, T. Uemura, H. Miyamoto, *IEEE Trans. Electron Devices* **55**, 483 (2008)
- 3.79. P. Javorka, A. Alam, M. Wolter, A. Fox, M. Marso, M. Heuken, H. Lüth, P. Kordos, *Electron. Lett.* **23**, 4 (2002)
- 3.80. D. Jena, A. Gossard, U. Mishra, *J. Appl. Phys.* **88**, 4734 (2000)
- 3.81. D. Jena, A. Gossard, U. Mishra, *Appl. Phys. Lett.* **76**, 1707 (2000)
- 3.82. D. Jena, I. Smorchkova, A. Gossard, U. Mishra, *Phys. Stat. Sol. B* **228**, 617 (2001)
- 3.83. C. Jeon, J. Lee, J. Lee, IEEE Electron Device Lett. **25**, 120 (2004)
- 3.84. G. Jessen, J. Gillespie, G. Via, A. Crespo, D. Langley, J. Wasserbauer, F. Faili, D. Francis, D. Babic, F. Ejekam, S. Guo, I. Eliashevich, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 271–274
- 3.85. S. Jia, Y. Dikme, D. Wang, K. Chen, K. Lau, M. Heuken, *IEEE Electron Device Lett.* **26**, 130 (2005)
- 3.86. M. Johnson, Z. Yu, J. Brown, N. El-Masry, J. Cook, J. Schetzina, *J. Electron. Mater.* **28**, 295 (1999)
- 3.87. M. Kamp, H. Riechert in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. B2.8, pp. 426–439

- 3.88. S. Karpow, Y. Kovalchuck, V. Myachin, Y. Pogorelskii, *J. Cryst. Growth* **129**, 563 (1993)
- 3.89. D. Katzer, S. Binari, D. Storm, J. Roussos, B. Shanabrook, E. Glaser, *Electron. Lett.* **38**, 1740 (2002)
- 3.90. D. Katzer, D. Storm, S. Binari, J. Roussos, B. Shanabrook, E. Glaser, *J. Cryst. Growth* **253**, 481 (2003)
- 3.91. D. Katzer, D. Storm, S. Binari, B. Shanabrook, A. Torabi, L. Zhou, D. Smith, *J. Vac. Sci. Technol. B* **23**, 1204 (2005)
- 3.92. S. Keller, G. Parish, P. Fini, S. Heikman, C. Chen, N. Zhang, S. DenBaars, U. Mishra, Y. Wu, *J. Appl. Phys.* **86**, 5850 (1999)
- 3.93. S. Keller, R. Vetry, G. Parish, S. DenBaars, U. Mishra, *Appl. Phys. Lett.* **78**, 3088 (2001)
- 3.94. S. Keller, Y. Wu, G. Parish, N. Ziang, J. Xu, B. Keller, S. DenBaars, U. Mishra, *IEEE Trans. Electron Devices* **48**, 552 (2001)
- 3.95. D. Kelly, C. Brindle, C. Kemerling, M. Stuber, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 200–203
- 3.96. T. Kikkawa, K. Imanishi, M. Kanamura, K. Joshin, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 77–80
- 3.97. T. Kikkawa, T. Maniwa, H. Hayashi, M. Kanamura, S. Yokokawa, M. Nishi, N. Adachi, M. Yokoyama, Y. Tateno, K. Joshin, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1347–1350
- 3.98. T. Kikkawa, M. Nagahara, T. Kimura, S. Yokokawa, S. Kato, M. Yokoyama, Y. Tateno, K. Horino, K. Domen, Y. Yamaguchi, N. Hara, K. Joshin, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1815–1818
- 3.99. A. Kikuchi, R. Bannai, K. Kishino, *Phys. Stat. Sol. A* **188**, 187 (2001)
- 3.100. L. Kirste, S. Moller, R. Kiefer, R. Quay, K. Köhler, N. Herres, *Appl. Surf. Science* **253**, 209 (2006)
- 3.101. W. Knap, E. Borovitskaya, M. Shur, L. Hsu, W. Walukiewicz, E. Frayssinet, P. Lorenzini, N. Grandjean, C. Skierbiszewski, P. Prystawko, M. Leszczynski, I. Grzegory, *Appl. Phys. Lett.* **80**, 1228 (2002)
- 3.102. K. Köhler, S. Müller, N. Rollbihler, R. Kiefer, R. Quay, G. Weimann, in *Proceedings of the International Symposium on Compound Semiconductors*, Lausanne, 2003, pp. 235–238, ed. by M. Illegems
- 3.103. D. Koleske, R. Henry, M. Twigg, J. Culbertson, S. Binari, A. Wickenden, M. Fatemi, *Appl. Phys. Lett.* **80**, 4372 (2002)
- 3.104. N. Kolias, T. Kazior, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 3.105. P. Kozodoy, PhD thesis, University of California Santa Barbara, Santa Barbara, 1999
- 3.106. P. Kozodoy, Y. Smorchkova, M. Hansen, H. Xing, S. DenBaars, U. Mishra, A. Saxler, R. Perrin, W. Mitchel, *Appl. Phys. Lett.* **75**, 2444 (1999)
- 3.107. J. Kuzmik, A. Kostopoulos, G. Konstantinidis, J. Carlin, A. Georgakilas, D. Pogany, *IEEE Trans. Electron Devices* **53**, 422 (2006)
- 3.108. R. Langer, B. Faure, A. Boussagol, P. Bove, H. Lahreche, A. Wilk, J. Thuret, F. Letertre, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, p. 4E
- 3.109. J. LaRoche, B. Luo, F. Ren, K. Baik, D.D. Stodilka, B. Gila, C. Abernathy, S. Pearton, A. Usikov, D. Tsevtkov, V. Soukhovoev, G. Gainer, A. Rechnikov, V. Dimitriev, G. Chen, C. Pan, J. Chyi, *Solid-State Electron.* **48**, 193 (2004)

- 3.110. M. Lee, J. Sheu, Y. Su, S. Chang, W. Lai, G. Chi, IEEE Electron Device Lett. **25**, 593 (2004)
- 3.111. W. Lee, N.J. Ryou, J. Limb, R. Dupuis, D. Hanser, E. Preble, N. Williams, K. Evans, Appl. Phys. Lett. **90**, 093509 (2007)
- 3.112. C. Li, I. Bhat, R. Wang, J. Seiler, J. Electron. Mater. **33**, 481 (2004)
- 3.113. T. Li, R. Campion, C. Foxon, S. Rushworth, L. Smith, J. Cryst. Growth **251**, 499 (2003)
- 3.114. J. Liu, Y. Zhou, R. Chu, Y. Cai, K. Chen, K. Lau, IEEE Electron Device Lett. **26**, 145 (2005)
- 3.115. J. Liu, Y. Zhou, J. Zhu, K. Lau, K. Chen, IEEE Electron Device Lett. **27**, 10 (2006)
- 3.116. J. Liu, Y. Zhou, J. Zhu, Y. Cai, K. Lau, K. Chen, IEEE Trans. Electron Devices **54**, (2007)
- 3.117. K. Liu, T. Tezukab, S. Sugitab, Y. Watarib, Y. Horikoshib, Y. Sua, S. Changa J. Cryst. Growth **263**, 400 (2004)
- 3.118. D. Look, Phys. Stat. Sol. B **228**, 293 (2001)
- 3.119. D. Look, Z. Fang, L. Polenta, MRS Internet J. Nitride Semicond. Res. **5**, W10.5 (2000)
- 3.120. D. Look, J. Sizelove, Phys. Rev. Lett. **82**, 1237 (1999)
- 3.121. H. Lu, I. Bhat, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 497–502
- 3.122. N. Maeda, T. Saitoh, K. Tsubaki, T. Nishida, K. Kobayashi, Phys. Stat. Sol. B **216**, 727 (1999)
- 3.123. M. Maestro, D. Tsvetkov, V. Soukhovoev, A. Usikov, V. Dmitriev, B. Luo, F. Ren, K. Baik, S. Pearton, Solid-State Electron. **47**, 1075 (2003)
- 3.124. M. Manfra, N. Weimann, Y. Bayens, P. Roux, D. Tennant, Electron. Lett. **39**, 694 (2003)
- 3.125. M. Manfra, N. Weimann, O. Mitrofanov, T. Wächtler, D. Tennant, Phys. Stat. Sol. A **200**, 175 (2003)
- 3.126. K. Matsushita, H. Sakurai, H. Kawasaki, Y. Takada, T. Sasaki, K. Tsuda, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 4.2
- 3.127. L. McCarthy, I. Smorchkova, H. Xing, P. Fini, S. Keller, J. Speck, S. DenBaars, M. Rodwell, U. Mishra, Appl. Phys. Lett. **78**, 2235 (2001)
- 3.128. L.S. McCarthy, PhD thesis, University of California Santa Barbara, Santa Barbara, 2001
- 3.129. G. Meneghesso, C. Ongaro, E. Zanoni, C. Brylinski, M. di Forte-Poisson, V. Hoel, J. de Jaeger, R. Langer, H. Lahreche, P. Bove, J. Thorpe, in *IEDM Technical Digest*, Washington DC, 2007, pp. 807–810
- 3.130. F. Medjdoub, N. Sarazin, M. Tordjman, M. Magis, M. di Forte-Poisson, M. Knez, E. Delos, C. Gaquiere, S. Delage, E. Kohn, Electronics Lett. **43** 691 (2007)
- 3.131. M. Micovic, P. Hashimoto, M. Hu, I. Milosavljevic, J. Duval, P. Willadsen, A. Kurdoghlian, P. Deelman, J. Moon, A. Schmitz, M. Delaney, in *IEDM Technical Digest*, San Francisco, 2004, pp. 807–810
- 3.132. M. Micovic, A. Kurdoghlian, P. Janke, P.H.D. Wong, J. Moon, L. McCray, C. Nguyen, IEEE Trans. Electron Devices **48**, 591 (2001)
- 3.133. E. Miller, D. Schaadt, E. Yu, X. Sun, L. Brillson, P. Waltereit, J. Speck, J. Appl. Phys. **94**, 7611 (2003)

- 3.134. E. Miller, E. Yu, P. Waltereit, J. Speck, *Appl. Phys. Lett.* **84**, 535 (2004)
- 3.135. A. Minko, V. Hoel, S. Lepilliet, G. Dambrine, J. DeJaeger, Y. Cordier, F. Semond, F. Natali, J. Massies, *IEEE Electron Device Lett.* **25**, 167 (2004)
- 3.136. M. Miyoshi, M. Sakai, S. Arulkumaran, H. Ishikawa, T. Egawa, M. Tanaka, O. Oda, *Jpn. J. Appl. Phys.* **43**, 7939 (2004)
- 3.137. E. Monroy, N. Gogneau, F. Enjalbert, F. Fossard, D. Jalabert, E. Bellet-Amalric, L. Dang, B. Daudin, *J. Appl. Phys.* **94**, 3121 (2003)
- 3.138. H. Morkoc, *Nitride Semiconductors and Devices*, Springer Series in Materials Science, vol. 32 (Springer, Berlin Heidelberg New York, 1999)
- 3.139. S. Müller, K. Köhler, R. Kiefer, R. Quay, M. Baeumler, L. Kirste, *Phys. Stat. Sol. C* **2**, 2639 (2005)
- 3.140. T. Murata, M. Hikita, Y. Hirose, Y. Uemoto, K. Inoue, T. Tanaka, D. Ueda, *IEEE Trans. Electron Devices* **52**, 1042 (2005)
- 3.141. N. Nakamura, in *MRS Bulletin*, Warrendale, 1998, pp. 1145–1156
- 3.142. S. Nakamura, S. Chichibu (eds.), *Introduction to Nitride Semiconductor Blue Lasers and Light Emitting Diodes* (Taylor & Francis, London New York, 2000)
- 3.143. S. Nakamura, N. Iwasa, M. Senoh, T. Mukai, *Jpn. J. Appl. Phys.* **228**, 309 (2001)
- 3.144. S. Nakamura, T. Mukai, M. Senoh, *J. Appl. Phys.* **71**, 5543 (1992)
- 3.145. Y. Nakano, J. Suda, T. Kimoto, *Phys. Stat. Sol. C* **2**, 2208 (2005)
- 3.146. Y. Nanishi, Y. Saito, T. Yamaguchi, M. Hori, F. Matsuda, T. Araki, A. Suzuki, T. Miyajima, *Phys. Stat. Sol. A* **200**, 202 (2003)
- 3.147. Y. Nasishi, Y. Saito, T. Yamaguchi, *Jpn. J. Appl. Phys.* **42**, 2549 (2003)
- 3.148. J. Neugebauer, C. Van de Walle *Appl. Phys. Lett.* **68**, 1829 (1996)
- 3.149. S. Newstead, R. Kubiak, E. Parker, *J. Cryst. Growth* **81**, 49 (1987)
- 3.150. H. Ng, D. Doppalapudi, D. Korakakis, R. Singh, T. Moustakas, *J. Cryst. Growth* **189–190**, 349 (1998)
- 3.151. N. Okamoto, K. Hoshino, N. Hara, M. Takikawa, Y. Arakawa, *J. Cryst. Growth* **272**, 278 (2004)
- 3.152. Y. Okamoto, K. Takahashi, H. Nakamura, Y. Okada, M. Kawabe, *Phys. Stat. Sol. A* **180**, 59 (2000)
- 3.153. T. Palacios, A. Chakraborty, S. Heikmann, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **27**, 13 (2006)
- 3.154. T. Palacios, A. Chakraborty, S. Keller, S. DenBaars, U. Mishra, in *Device Research Conference*, Santa Barbara, 2005, pp. 181–182
- 3.155. T. Palacios, L. Shen, S. Keller, A. Chakraborty, S. Heikman, D. Buttari, S. DenBaars, U. Mishra, *Phys. Stat. Sol. A* **22**, 837 (2005)
- 3.156. N. Pan, J. Elliot, M. Knowles, D. Vu, K. Kishimoto, J. Twynam, H. Sato, M. Fresina, G. Stillman, *IEEE Electron Device Lett.* **19**, 115 (1998)
- 3.157. G. Parish, PhD thesis, University of California Santa Barbara, Santa Barbara, 1999
- 3.158. C. Park, Y. Park, H. Lee, I. Yoon, T. Kang, H. Cho, J. Oh, K. Wang, *Jpn. J. Appl. Phys.* **44**, 1722 (2005)
- 3.159. T. Paskova, V. Darakchieva, E. Valcheva, P. Paskov, I. Ivanov, B. Monemar, T. Böttcher, C. Roder, D. Hommel, *J. Electron. Mater.* **33**, 389 (2004)
- 3.160. S. Pearton, J. Zolper, R. Shul, F. Ren, *J. Appl. Phys.* **86**, 1 (1999)
- 3.161. A. Petersson, A. Gustafsson, L. Samuelson, S. Tanaka, Y. Aoyagi, *MRS Internet J. Nitride Semicond. Res.* **7**, (2002)
- 3.162. C. Poblenz, P. Waltereit, S. Rajan, S. Heikman, U. Mishra, J. Speck, *J. Vac. Sci. Technol. B* **22**, 1145 (2004)

- 3.163. C. Poblenz, P. Waltereit, S. Rajan, U.K. Mishra, J.S. Speck, P. Chin, I. Smorchkova, B. Heying, *J. Vac. Sci. Technol. B* **23**, 1562 (2005)
- 3.164. A. Polyakov, N. Smirnov, A. Govorkov, A. Shlensky, S. Pearton, *J. Appl. Phys.* **95**, 5591 (2004)
- 3.165. A. Ptak, L. Holbert, L. Ting, C. Schwartz, M. Moldovan, N. Giles, T. Myers, P. van Lierde, C. Tian, R. Hockett, S. Mitha, A. Wickenden, D. Koleske, R. Henry, *Appl. Phys. Lett.* **79**, 2740 (2001)
- 3.166. S. Rajan, P. Waltereit, C. Poblenz, S. Heikman, D. Green, J. Speck, U. Mishra, *IEEE Electron Device Lett.* **25**, 247 (2004)
- 3.167. J. Redwing, T. Kuech in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. B2.7, pp. 416–425
- 3.168. J. Redwing, M. Tischler, J. Flynn, S. Elhamri, M. Ahoujja, R. Newrock, W. Mitchel, *Appl. Phys. Lett.* **69**, 963 (1996).
- 3.169. F. Ren, J. Zolper *Wide Energy Bandgap Electronic Devices* (World Scientific, New Jersey, 2003)
- 3.170. M. Reshchikova, H. Morkoc, *J. Appl. Phys.* **97**, 061301–1 (2005)
- 3.171. M. Rudziski, P. Hageman, A. Grzegorczyk, L. Macht, T. Rödle, H. Jos, P. Larsen, *Phys. Stat. Sol. C* **2**, 2141 (2005)
- 3.172. P. Ruterana, M. Albrecht, J. Neugebauer (eds.), *Nitride Semiconductors: Handbook on Materials and Device* (Wiley-VCH, Weinheim, 2003)
- 3.173. P. Ruterana, M. Morales, F. Gourbilleau, P. Singh, M. Drago, T. Schmidling, U. Pohl, W. Richter, *Phys. Stat. Sol. A* **202**, 781 (2005)
- 3.174. M. Sakai, T. Egawa, M. Hao, H. Ishikawa, *Jpn. J. Appl. Phys.* **43**, 8019 (2004)
- 3.175. W. Schaff, L. Hai, H. Jeonghyun, W. Hong, in *Proc. IEEE/Cornell Conf. High Perf. Devices*, Ithaca, 2000, pp. 225–231
- 3.176. F. Scholz, Progress in Crystal Growth and Characterization of Materials, **35**, 243 (1997))
- 3.177. F. Schwierz, V. Polyakov, in *Proc. Intl. Solid-State Integrated Circuit Technology ICSICT* Shanghai, 2006, pp. 845–848
- 3.178. D. Segev, C. Van de Walle, *Europhys. Lett.* **76**, 305 (2006)
- 3.179. F. Semond, B. Damilano, P. Lorenzini, S. Vezian, N. Grandjean, M. Leroux, J. Massies, *Appl. Phys. Lett.* **75**, 82 (1999)
- 3.180. F. Semond, P. Lorenzini, N. Grandjean, J. Massies, *Appl. Phys. Lett.* **78**, 335 (2001)
- 3.181. I. Shalish, L. Kronik, G. Segal, Y. Shapira, Y. Rosenwaks, U. Tisch, J. Salzman, *Phys. Rev. B.*, **59**, 9748 (1999)
- 3.182. L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. DenBaars, U. Mishra, *J. Electron. Mater.* **33**, 422 (2004)
- 3.183. L. Shen, S. Heikman, B. Moran, R. Coffie, N. Zhang, D. Buttari, I. Smorchkova, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **22**, 457 (2001)
- 3.184. B. Simpkins, E. Yu, P. Waltereit, J. Speck, *J. Appl. Phys.* **94**, 1448 (2003)
- 3.185. J. Smart, A. Schremer, N. Weimann, O. Ambacher, L. Eastman, J. Shealy, *Appl. Phys. Lett.* **75**, 388 (1999)
- 3.186. I. Smorchkova, E. Haus, B. Heying, P. Kozodoy, P. Fini, J. Ibbetson, S. Keller, S. DenBaars, J. Speck, U. Mishra, *Appl. Phys. Lett.* **76**, 718 (2000)

- 3.187. A. Sozza, C. Dua, E. Morvan, M. diForte Poisson, S. Delage, F. Rampazzo, A. Tazzoli, F. Danesin, G. Meneghesso, E. Zanoni, A. Curutchet, N. Malbert, N. Labat, B. Grimbert, J.D. Jaeger, in *IEDM Technical Digest*, Washington DC, 2005, pp. 590–593
- 3.188. M. Steen, M. Sheldon, R. Bresnahan, T. Bird, D. Gotthold, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.5
- 3.189. J. Suda, Y. Nakano, T. Kimoto, MRS Symposium **831**, 471 (1999)
- 3.190. B. Sverdlov, A. Botchkarev, G. Martin, A. Salvador, H. Morkoc, S. Tsien, D. Smith, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 175–180
- 3.191. H. Takeuchi, Y. Yamamoto, Y. Kamo, T. Oku, M. Nakayama, *The European Physical Journal B* **52**, 311 (2006)
- 3.192. T. Tanaka, Y. Koji, T. Meguro, Y. Otoki, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 295–298
- 3.193. T. Tanaka, K. Takano, H. Fujikura, T. Mishima, Y. Kohji, H. Kamogawa, T. Meguro, Y. Otoki, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 4.1
- 3.194. H. Tang, J. Webb, *Appl. Phys. Lett.* **74**, 2373 (1999)
- 3.195. E. Tengborn, M. Rummukainen, F. Tuomisto, K. Saarinen, M. Rudzinski, P. Hageman, P. Larsen, A. Nordlund, *Appl. Phys. Lett.* **89**, 091905 (2006)
- 3.196. A. Thamm, O. Brandt, J. Hilsenbeck, R. Lossy, K.H. Ploog, in *Procedings of the International Symposium on Compound Semiconductors*, Monterey, 2000, pp 455–460
- 3.197. V. Tilak, B. Green, V. Kaper, H. Kim, T. Prunty, J. Smart, J. Shealy, L. Eastman, *IEEE Electron Device Lett.* **22**, 504 (2001)
- 3.198. A. Trassoudaine, R. Cadoret, E. Aujol, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 4, pp. 193–240
- 3.199. R. Underwood, PhD thesis, University of California Santa Barbara, Santa Barbara, 1999
- 3.200. M. Uren, T. Martin, B. Hughes, K. Hilton, A. Wells, R. Balmer, D.H.A. Keir, D. Wallis, A. Piddock, M. Missous, *Phys. Stat. Sol. A* **194**, 468 (2002)
- 3.201. R. Vandersmissen, J. Das, W. Ruythooren, J. Derluyn, M. Germain, D. Xiao, D. Schreurs, G. Borghs, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.3
- 3.202. C. Van de Walle, C. Stampfl, J. Neugebauer, *J. Cryst. Growth* **189/190**, 505 (1998)
- 3.203. C. Van de Walle, J. Neugebauer, C. Stampfl, in *Properties, Processing and Applications of GaN Nitride and Related Semiconductors*, No. 23 in EMIS Data reviews Series, ed. by J. Edgar et al. (IEE INSPEC, London, 1999), Sect. A8.2, pp. 275–280
- 3.204. A. Vescan, J. Brown, J. Johnson, R. Therrien, T. Gehrke, P. Rajagopal, J. Roberts, S. Singhal, W. Nagy, R. Borges, E. Piner, K. Linthicum, *Phys. Stat. Sol. C* **0**, 52 (2002)
- 3.205. P. Waltereit, S. Lim, M. McLaurin, J. Speck, *Phys. Stat. Sol. A* **194**, 524 (2002)
- 3.206. P. Waltereit, C. Poblenz, S. Rajan, F. Wu, U.K. Mishra, and J.S. Speck, *Jpn. J. Appl. Phys.* **43** L1520 (2004)

- 3.207. C. Wang, L. Yu, S. Lau, E. Yu, W. Kim, A. Botchkarev, H. Morkoc, *Appl. Phys. Lett.* **72**, 1211 (1998)
- 3.208. D. Wang, S. Jia, K. Chen, K. Lau, Y. Dikme, P. van Gemmern, Y. Lin, H. Kalisch, R. Jansen, M. Heuken, *J. Appl. Phys.* **97**, 56103 (2005)
- 3.209. S. Wang, S. Chang, K. Uang, B. Liou, in *Device Research Conference*, Santa Barbara, 2005, pp. 59–60
- 3.210. N. Watanabe, H. Yokoyama, M. Hiroki, Y. Oda, T. Kobayashi, T. Yagi, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 257–260
- 3.211. J. Webb, H. Tang, J. Bardwell, S. Rolfe, Y. Liu, J. Lapointe, P. Marshall, T. MacElwee, *Phys. Stat. Sol. A* **188**, 271 (2001)
- 3.212. J. Webb, H. Tang, J. Bardwell, P. Coleridge, *Phys. Stat. Sol. A* **176**, 243 (1999)
- 3.213. J. Webb, H. Tang, J. Bardwell, P. Coleridge, *Appl. Phys. Lett.* **78**, 3845 (2001)
- 3.214. J. Webb, H. Tang, J. Bardwell, Y. Liu, J. Lapointe, T. MacElwee, *Phys. Stat. Sol. A* **194**, 439 (2002)
- 3.215. T. Weeks, M. Bremser, K. Ailey, E. Carlson, W. Perry, R. Davis *Appl. Phys. Lett.* **67**, 401 (1995)
- 3.216. N. Weimann, M. Manfra, S. Chakraborty, D. Tennant, *IEEE Electron Device Lett.* **23**, 691 (2002)
- 3.217. N. Weimann, M. Manfra, T. Wächtler, *IEEE Electron Device Lett.* **24**, 57 (2003)
- 3.218. A. Wickenden, D. Koleske, R. Henry, R. Gorman, J. Culbertson, M. Twigg, *J. Electron. Mater.* **28**, 301 (1999)
- 3.219. A. Wickenden, D. Koleske, R. Henry, R. Gorman, M. Twigg, M. Fatemi, J. Freitas, W. Moore, *J. Electron. Mater.* **29**, 21 (2000)
- 3.220. A. Winzer, R. Goldhahn, G. Gobsch, A. Dadgar, A. Krost, O. Weidemann, M. Stutzmann, M. Eickhoff, *Appl. Phys. Lett.*, **88**, 4101 (2006)
- 3.221. M. Wojtowicz, B. Heying, P.C.I. Smorchkova, R. Sandhu, T. Block, M. Aumer, D. Thomson, D. Partlow, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, p. 299
- 3.222. Y. Wu, B. Keller, P. Fini, S. Keller, T. Jenkins, L. Kehias, S. Denbaars, U. Mishra, *IEEE Electron Device Lett.* **19**, 50 (1998)
- 3.223. L. Wu, W. Meyer, F. Auret, *Phys. Stat. Sol. A* **201**, 2277 (2004)
- 3.224. Y. Wu, M. Moore, A. Abrahamsen, M. Jacob-Mitos, P. Parikh, S. Heikman, A. Burk, in *IEDM Technical Digest*, Washington DC, 2007, pp. 405–408
- 3.225. F. Yam, Z. Hassan, *Superlattices and Microstructures*, **43**, 1 (2008)
- 3.226. A. Yamamoto, T. Shin-ya, T. Sugiura, A. Hashimoto, *J. Cryst. Growth* **189–190**, 461 (1998)
- 3.227. F. Yang, J. Hwang, Y. Yang, K. Chen, J. Wang, *Jpn. J. Appl. Phys.* **41**, L1321 (2002)
- 3.228. T. Yuasa, Y. Ueta, Y. Tsuda, A. Ogawa, M. Taneya, K. Takao, *Jpn. J. Appl. Phys.* **38**, L703 (1999)
- 3.229. J. Zimmer, G. Chandler, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 129–132

References of Chapter 4

- 4.1. V. Adivarahan, M. Gaevski, M. Islam, B. Zhang, Y. Deng, M. Khan, IEEE Trans. Electron Devices **55**, 495 (2008)
- 4.2. V. Adivarahan, A. Koudymov, S. Rai, J. Yang, G. Simin, M. Khan, in *Device Research Conference*, Santa Barbara, 2005, pp. 177–178
- 4.3. V. Adivarahan, J. Yang, A. Koudymov, G. Simin, M. Khan, IEEE Electron Device Lett. **26**, 535 (2005)
- 4.4. V. Agarwal, D. Rawal, H. Vyas, J. Electrochem. Soc. **152**, G567 (2005)
- 4.5. Y. Ando, Y. Okamoto, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Kuzuhara, in *IEDM Technical Digest*, Washington DC, 2003, pp. 563–566
- 4.6. Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, M. Kuzuhara, in *IEDM Technical Digest*, Washington DC, 2001, pp. 381–384
- 4.7. Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, M. Kuzuhara, IEEE Electron Device Lett. **24**, 289 (2003)
- 4.8. Y. Ando, A. Wakejima, Y. Okamoto, T. Nakayama, K. Ota, K. Yamanoguchi, Y. Murase, K. Kasahara, K. Matsunaga, T. Inoue, H. Miyamoto, in *IEDM Technical Digest*, Washington DC, 2005, pp. 576–579
- 4.9. J. Ao, D. Kikuta, N. Kubota, Y. Naoi, Y. Ohno, IEEE Electron Device Lett. **24**, 500 (2003)
- 4.10. C. Bae, C. Krug, G. Lucovsky, A. Chakraborty, U. Mishra, J. Appl. Phys. **96**, 2674 (2004)
- 4.11. K. Ban, H. Hong, D. Noh, T. Seong, J. Song, D. Kim, Semicond. Sci. Technol. **20**, 921 (2005)
- 4.12. J. Bardwell, I. Foulds, B. Lamontagne, H. Tang, J. Webb, P. Marshall, S. Rolfe, J. Stapledon, J. Vac. Sci. Technol. A **18**, 750 (2000)
- 4.13. J. Bardwell, I. Foulds, J. Webb, H. Tang, J. Electron. Mater. **28**, 1071 (1999)
- 4.14. J. Bardwell, S. Haffouz, W. McKinnon, C. Storey, H. Tang, G. Sproule, D. Roth, R. Wang, Electrochem. Solid-State Lett. **10**, H46 (2007)
- 4.15. D. Basak, M. Verdu, M. Montojo, M. Sanchez-Garcia, F. Sanchez, E. Munoz, E. Calleja, Semicond. Sci. Technol. **12**, 1654 (1997)
- 4.16. F. Benkhelifa, R. Kiefer, S. Müller, F. van Raay, R. Quay, R. Sah, M. Mikulla, G. Weimann, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.4

- 4.17. J. Bernat, P. Javorka, A. Fox, M. Marso, H. Lüth, P. Kordos, Solid-State Electron. **47**, 2097 (2003)
- 4.18. S. Binari, H. Dietrich, G. Kelner, L. Rowland, K. Doverspike, D. Gaskill, Electron. Lett. **30**, 909 (1994)
- 4.19. S. Binari, H. Dietrich, G. Kelner, L. Rowland, K. Doverspike, D. Wickenden, J. Appl. Phys. **78**, 3008 (1995)
- 4.20. S. Binari, K. Ikossi, J. Roussos, W. Kruppa, D. Park, H. Dietrich, D. Koleske, A. Wickenden, R.L. Henry, IEEE Trans. Electron Devices **48**, 465 (2001)
- 4.21. S. Binari, P. Klein, T. Kazior, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1823–1826
- 4.22. S. Binari, W. Kruppa, H. Dietrich, G. Kelner, A. Wickenden, J. Freitas, Solid-State Electron. **41**, 1549 (1997)
- 4.23. K. Boutros, M. Regan, P. Rowell, D. Gotthold, B. Brar, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 23–26
- 4.24. S. Bradley, A. Young, L. Brillson, M. Murphy, W. Schaff, L. Eastman, IEEE Trans. Electron Devices **48**, 412 (2001)
- 4.25. N. Braga, R. Mickevicius, V. Rao, W. Fichtner, R. Gaska, M. Shur, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 149–152
- 4.26. H. Brech, W. Brakensiek, D. Burdeaux, W. Burger, C. Dragon, G. Formicone, B. Pryor, D. Rice, in *IEDM Technical Digest*, Washington DC, 2003, pp. 359–362
- 4.27. D. Buttari, A. Chini, G. Meneghesso, E. Zanoni, P. Chavarkar, R. Coffie, N. Zhang, S. Heikman, L. Shen, H. Xing, C. Zheng, U. Mishra, IEEE Electron Device Lett. **23**, 118 (2002)
- 4.28. D. Buttari, A. Chini, G. Meneghesso, E. Zanoni, B. Moran, S. Heikman, N. Zhang, L. Shen, R. Coffie, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **23**, 76 (2002)
- 4.29. D. Buttari, A. Chini, T. Palacios, R. Coffie, L. Shen, H. Xing, S. Heikman, L. McCarthy, A. Chakraborty, S. Keller, U. Mishra, Appl. Phys. Lett. **83**, 4779 (2003)
- 4.30. Y. Cai, Y. Zhou, K. Chen, K. Lau, IEEE Electron Device Lett. **26**, 435 (2005)
- 4.31. P. Chabert, J. Vac. Sci. Technol. B **19**, 212 (2001)
- 4.32. P. Chabert, N. Proust, J. Perrin, R. Boswell, Appl. Phys. Lett. **76**, 2310 (2000)
- 4.33. C. Chen, S. Keller, G. Parish, R. Vetry, P. Kozodoy, E. Hu, S. DenBaars, U. Mishra, Y. Wu, Appl. Phys. Lett. **73**, 3147 (1998)
- 4.34. K. Cheng, J. Lee, J. Lyding, Y. Kim, Y. Kim, K.P. Suh, IEEE Electron Device Lett. **22**, 188 (2001)
- 4.35. M. Chertouk, M. Dammann, K. Köhler, G. Weimann, IEEE Electron Device Lett. **21**, 97 (2000)
- 4.36. R. Cheung, S. Withanage, R. Reeves, S. Brown, I. Ben-Yaacov, C. Kirchner, M. Kamp, Appl. Phys. Lett. **74**, 3185 (1999)
- 4.37. A. Chini, D. Buttari, R. Coffie, S. Heikmann, S. Keller, U. Mishra, Electron. Lett. **40**, 73 (2004)
- 4.38. A. Chini, D. Buttari, R. Coffie, L. Shen, S. Heikman, A. Chakraborty, S. Keller, U. Mishra, IEEE Electron Device Lett. **25**, 229 (2004)
- 4.39. A. Chini, J. Wittich, S. Heikman, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **25**, 55 (2004)

- 4.40. H. Cho, K. Lee, B. Gila, C. Abernathy, S. Pearton, F. Ren, Solid-State Electron. **47**, 1597 (2003)
- 4.41. H. Cho, K. Lee, B. Gila, C. Abernathy, S. Pearton, F. Ren, Solid-State Electron. **47**, 1757 (2003)
- 4.42. H. Cho, P. Leeungsawarat, D. Hays, S. Pearton, S. Chu, R. Strong, C. Zetterling, M. Östling, Appl. Phys. Lett. **76**, 739 (2000)
- 4.43. H. Cho, C. Vartuli, C. Abernathy, S. Donovan, S. Pearton, R. Schul, J. Han, Solid-State Electron. **42**, 2277 (1998)
- 4.44. H. Chou, T. Lee, S. Huang, H. Weng, M. Tsai, J. Lee, M. Chertouk, D. Tu, P. Chao, C. Wu, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Scottsdale, 2003, p. 10.2
- 4.45. C. Chu, C. Yu, Y. Wang, J. Tsai, F. Lai, S. Wang, Appl. Phys. Lett. **77**, 3423 (2000)
- 4.46. E. Chumbes, J. Smart, T. Prunty, J. Shealy, in *IEDM Technical Digest*, San Francisco, 2000, pp. 385–388
- 4.47. R. Coffie, D. Buttari, S. Heikmann, S. Keller, A. Chini, L. Shen, U. Mishra, IEEE Electron Device Lett. **23**, 588 (2002)
- 4.48. R. Coffie, L. Shen, G. Parish, A. Chini, D. Buttari, S. Heikman, S. Keller, U. Mishra, Electron. Lett. **39**, 1419 (2003)
- 4.49. X. Dang, E. Yu, E. Piner, B. McDermott, J. Appl. Phys. **90**, 1357 (2001)
- 4.50. Y. Dora, A. Chakraborty, S. Heikman, L. McCarthy, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **7**, 529 (2006)
- 4.51. Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **27**, 713 (2006)
- 4.52. Y. Dora, C. Suh, A. Chakraborty, S. Heikman, S. Chandrasekarana, V. Mehrotra, U. Mishra, in *Device Research Conference*, Santa Barbara, 2005, pp. 191–192
- 4.53. D. Dumka, C. Lee, H. Tserng, P. Saunier, M. Kumar, Electron. Lett. **40**, 1023 (2003)
- 4.54. R. Dupuis, C. Eiting, P. Grundowski, H. Hsia, Z. Tang, D. Becher, H. Kuo, G. Stillman, M. Feng, J. Electron. Mater. **28**, 319 (1999)
- 4.55. L. Eastman, V. Tilak, J. Smart, B. Green, E. Chumbes, R. Dimitrov, H. Kim, O. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. Schaff, J. Shealy, IEEE Trans. Electron Devices **48**, 479 (2001)
- 4.56. C. Eddy, B. Molnar, J. Electron. Mater. **28**, 314 (1999)
- 4.57. A. Edwards, J. Mittereder, S. Binari, D. Katz, D. Storm, J. Roussos, IEEE Electron Device Lett. **26**, 225 (2005)
- 4.58. T. Egawa, G. Zhao, H. Ishikawa, M. Umeno, T. Jimbo, IEEE Trans. Electron Devices **48**, 603 (2001)
- 4.59. A. Endoh, Y. Yamashita, K. Ikeda, M. Higashiwaki, K. Hikosaka, T. Matsui, S. Hiyamizu, T. Mikura, Jpn. J. Appl. Phys. **43**, 2255 (2004)
- 4.60. A. Endoh, Y. Yamashita, K. Ikeda, M.H.A. Hikosaka, T. Matsui, S. Hiyamizu, T. Mimura, Jpn. J. Appl. Phys. **43**, 2255 (2004)
- 4.61. D. Fanning, L. Witkowski, J. Stidham, H. Tserng, M. Muir, P. Saunier, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, San Diego, 2002, pp. 83–86
- 4.62. D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, J. Johnson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.3

- 4.63. G. Franz, Phys. Stat. Sol. A **159**, 137 (1997)
- 4.64. M. Fu, V. Sarvepalli, R. Singh, C. Abernathy, X. Cao, S. Pearton, J. Sekhar, Solid-State Electron. **42**, 2335 (1998)
- 4.65. B. Gaffey, L. Guido, X. Wang, T. Ma, IEEE Trans. Electron Devices **48**, 458 (2001)
- 4.66. D. Gao, M. Wijesundara, C. Carraro, R. Howe, R. Maboudian, J. Vac. Sci. Technol. B **22**, 513 (2004)
- 4.67. B. Gila, J. Kim, B. Luo, A. Onstine, W. Johnson, F. Ren, C. Abernathy, S. Pearton, Solid-State Electron. **47**, 2139 (2003)
- 4.68. J. Gillespie, A. Crespo, R. Fitch, G. Jessen, D. Langley, N. Moser, D. Via, M. Williams, M. Yannuzzi, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.2
- 4.69. S. Golka, W. Schrenk, G. Strasser, in *Proceedings of German Microwave Forum*, Vienna, 2005, pp. 189–192
- 4.70. D. Gotthold, S. Guo, R. Birkhahn, B. Albert, D. Florescu, B. Peres, J. Electron. Mater. **33**, 408 (2004)
- 4.71. J. Graff, E. Schubert, A. Osinsky, in *Proceedings of IEEE/Cornell Conference on High Performance Devices*, Ithaca, 2000, pp. 28–32
- 4.72. B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, L. Eastman, IEEE Electron Device Lett. **21**, 268 (2000)
- 4.73. J. Grenko, C. Reynolds, R. Schlessner, K. Bachmann, Z. Rietmeier, R. Davis, Z. Sitar, MRS Internet J. Nitride Semicond. Res. **9**, (2004)
- 4.74. R. Grundbacher, R. Lai, M. Nishimoto, T. Chin, Y. Chen, M. Barsky, T. Block, D. Streit, IEEE Electron Device Lett. **20**, 517 (1999)
- 4.75. J. Guo, F. Pan, M. Feng, R. Guo, P. Chou, C. Chang, J. Appl. Phys. **80**, 1623 (1996)
- 4.76. Q. Guo, O. Kato, A. Yoshida, J. Electrochem. Soc. **139**, 2008 (1992)
- 4.77. E. Haberer, C.H. Chen, A. Abare, M. Hansen, S. DenBaars, L. Coldren, U. Mishra, E. Hu, Appl. Phys. Lett. **76**, 3941 (2000)
- 4.78. P. Hacke, T. Detchprohm, K. Hiramatsu, N. Sawaki, Appl. Phys. Lett. **63**, 2676 (1993)
- 4.79. M. Hampson, S. Shen, R. Schwindt, R. Price, U. Chowdhury, M. Wong, T. Zhu, D. Yoo, R. Dupuis, M. Feng, IEEE Electron Device Lett. **25**, 238 (2004)
- 4.80. P. Hansen, L. Shen, Y. Wu, A. Stonas, Y. Terao, S. Heikman, D. Buttari, T. Taylor, S. DenBaars, U. Mishra, R. York, J. Speck, J. Vac. Sci. Technol. B **22**, 2479 (2004)
- 4.81. W. Hanson, R. Borges, J. Brown, J. Cook, T. Gehrke, J. Johnson, K. Linthicum, S. Peters, E. Piner, P. Rajagopal, J. Robert, S. Singhal, R. Therrien, A. Vescan, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 107–110
- 4.82. P. Hartlieb, R. Davies, R. Nemanich, in *Nitride Semiconductors: Handbook on Materials and Device*, ed. by P. Ruterana, M. Albrecht, J. Neugebauer (Wiley-VCH, Weinheim, 2003), Chap. 10, pp. 491–523
- 4.83. T. Hashizume, J. Kotani, H. Hasegawa, Appl. Phys. Lett. **84**, 4884 (2004)
- 4.84. T. Hashizume, S. Ootomo, H. Hasegawa, Appl. Phys. Lett. **83**, 2952 (2003)
- 4.85. T. Hashizume, S. Ootomo, T. Inakagi, H. Hasegawa, J. Vac. Sci. Technol. B **21**, 1828 (2003)
- 4.86. T. Hattori, G. Nakamura, S. Nomura, T. Ichise, A. Masuda, H. Matsumura, in *GaAs IC Symposium Technical Digest*, Anaheim, 1997, pp. 78–80

- 4.87. N. Hefyene, S. Cristoloveanu, G. Ghibaudo, P. Gentil, Y. Moriyasu, T. Morishita, M. Matsui, A. Yasujima, Solid-State Electron. **44**, 1711 (2000)
- 4.88. H. Hendriks, J. Crites, G. D'Urso, R. Fox, T. Lepkowski, B. Patel, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Las Vegas, 2001, pp. 181–184
- 4.89. M. Higashiwaki, N. Hirose, T. Matsui, IEEE Electron Device Lett. **26**, 139 (2005)
- 4.90. M. Higashiwaki, N. Hirose, T.M.A. Mimura, J. Appl. Phys. **100**, 033714 (2006)
- 4.91. M. Higashiwaki, T. Matsui, Jpn. J. Appl. Phys. **44**, L475 (2005)
- 4.92. M. Higashiwaki, T. Matsui, Jpn. J. Appl. Phys. **45**, L1111 (2006)
- 4.93. M. Higashiwaki, T. Matsui, T. Mimura, in *Device Research Conference*, State College PA, 2006, pp. 149–150
- 4.94. M. Higashiwaki, T. Matsui, T. Mimura, IEEE Electron Device Lett. **27**, 16 (2006)
- 4.95. M. Higashiwaki, T. Mimura, T. Matsui, IEEE Trans. Electron Devices **54**, 1566 (2007)
- 4.96. M. Hikita, M. Yanagihara, K. Nakazawa, H. Ueno, Y. Hirose, T. Ueda, Y. Uemoto, T. Tanaka, D. Ueda, T. Egawa, IEEE Trans. Electron Devices **52**, 1963 (2005)
- 4.97. J. Hilsenbeck, Dissertation, Technische Universität Karlsruhe, 2001
- 4.98. J. Hilsenbeck, F. Lenk, R. Lossy, J. Würfl, K. Köhler, H. Obloh, in *Proceedings of the International Symposium on Compound Semiconductors*, Monterey, 2000, pp. 351–356
- 4.99. J. Hilsenbeck, W. Rieger, E. Neubauer, W. John, G. Tränkle, J. Würfl, A. Ramakrishnan, H. Obloh, Phys. Stat. Sol. A **176**, 183 (1999)
- 4.100. J. Hilsenbeck, W. Rieger, J. Würfl, R. Dimitrov, O. Ambacher, in *Proceedings of the International Symposium on Compound Semiconductors*, Berlin, 1999, pp. 507–510
- 4.101. J. Hong, J. Lee, C. Vartuli, J. Mackenzie, S. Donovan, C. Abernathy, R. Crockett, S. Pearton, J. Zolper, Solid-State Electron. **41**, 681 (1997)
- 4.102. S. Hsu, D. Pavlidis, in *GaAs IC Symposium Technical Digest*, San Diego, 2003, pp. 119–122
- 4.103. H. Huang, C. Kao, J. Tsai, C. Yu, C. Chu, J. Lee, S. Kuo, C. Lin, H. Kuo, S. Wang, Mater. Sci. Eng. B **107**, 237 (2004)
- 4.104. J. Hwang, W. Schaff, B. Green, H. Cha, L. Eastman, Solid-State Electron. **48**, 363 (2004)
- 4.105. J. Ibbetson, P. Fini, K. Ness, S. DenBaars, J. Speck, U. Mishra, Appl. Phys. Lett. **77**, 250 (2000)
- 4.106. S. Inaba, K. Okano, S. Matsuda, M. Fujiwara, A. Hokazono, K. Adachi, K. Ohuchi, H. Suto, H. Fukui, T. Shimizu, S. Mori, H. Oguma, A. Murakoshi, T. Itani, T. Iinuma, T. Kudo, H. Shibata, S. Taniguchi, T. Matsushita, S. Magoshi, Y. Watanabe, M. Takayanagi, A. Azuma, H. Oyamatsu, K. Suguro, Y. Katsumata, Y. Toyoshima, H. Ishiuchi, in *IEDM Technical Digest*, Washington DC, 2001, pp. 641–644
- 4.107. K. Inoue, Y. Ikeda, H. Masato, T. Matsuno, K. Nishii, in *IEDM Technical Digest*, Washington DC, 2001, pp. 577–580
- 4.108. Y. Irokawa, J. Kim, F. Ren, K. Baik, B. Gila, C. Abernathy, S. Pearton, C. Pan, G. Chen, J. Chyi, S. Park, Solid-State Electron. **48**, 827 (2004)

- 4.109. J. Izpura, *Semicond. Sci. Technol.* **17**, 1293 (2002)
- 4.110. C. Jeon, H. Jang, J. Lee, *Appl. Phys. Lett.* **82**, 391 (2003)
- 4.111. C. Jeon, J. Lee, *J. Appl. Phys.* **95**, 698 (2004)
- 4.112. C. Jeong, D. Kim, K. Kim, G. Yeom, *Jpn. J. Appl. Phys.* **41**, 6206 (2002)
- 4.113. G. Jessen, R. Fitch, J. Gillespie, G. Via, N. Moser, M. Yannuzzi, A. Crespo, R. Dettmer, T. Jenkins, in *GaAs IC Symposium Technical Digest*, San Diego, 2003, pp. 277–279
- 4.114. J. Johnson, J. Gao, K. Lucht, J. Williamson, C. Strautin, J. Riddle, R. Therrien, P. Rajagopal, J. Roberts, A. Vescan, J. Brown, A. Hanson, S. Singhal, R. Borges, E. Piner, K. Linthicum, *Proc. Electrochem. Soc.* **7**, 405 (2004)
- 4.115. J. Johnson, A. Zhang, W. Luo, F. Ren, S. Pearton, S. Park, Y. Park, J. Chyi, *IEEE Trans. Electron Devices* **49**, 32 (2002)
- 4.116. H. Kambayashi, T. Wada, N. Ikeda, S. Yoshida, in *GaN, AlN, InN and Related Materials*, ed. by M. Kuball, T. Myers, J. Redwing, T. Mukai. Materials Research Society Symposium Proceedings vol. 892, Warrendale PA, 2006, p. FF05-03
- 4.117. Y. Kamo, T. Kunii, H. Takeuchi, Y. Yamamoto, M. Totsuka, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, T. Oku, A. Inoue, T. Nanjo, H. Chiba, M. Suita, T. Oishi, Y. Abe, Y. Tsuyama, R. Shirahana, H. Ohtsuka, K. Iyomasa, K. Yamanaka, M. Hieda, M. Nakayama, T. Ishikawa, T. Takagi, K. Marumoto, Y. Matsuda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 495–498
- 4.118. M. Kanamura, T. Kikkawa, T. Iwai, K. Imanishi, T. Kubo, K. Joshin, in *IEDM Technical Digest*, Washington DC, 2005, pp. 572–575
- 4.119. B. Kang, R. Mehandru, S. Kim, F. Ren, R. Fitch, J. Gillespie, N. Moser, G. Jessen, T. Jenkins, R. Dettmer, D. Via, A. Crespo, B. Gila, R. Abernathy, S. Pearton, *Appl. Phys. Lett.* **84**, 4635 (2004)
- 4.120. S. Karmalkar, U. Mishra, *IEEE Trans. Electron Devices* **48**, 73 (2001)
- 4.121. T. Kato, K. Hayashi, Y. Sasaki, T. Kato, *IEEE Trans. Electron Devices* **34**, 753 (1987)
- 4.122. H. Kawai, M. Hara, F. Nakamura, S. Imanaga, *Electron. Lett.* **34**, 592 (1998)
- 4.123. H. Kawaura, T. Sakamoto, T. Baba, Y. Ochiai, J. Fujita, J. Sone, *IEEE Trans. Electron Devices* **47**, 856 (2000)
- 4.124. S. Keller, Y. Wu, G. Parish, N. Ziang, J. Xu, B. Keller, S. DenBaars, U. Mishra, *IEEE Trans. Electron Devices* **48**, 552 (2001)
- 4.125. F. Khan, B. Roof, I. Adesida, *J. Electron. Mater.* **3**, 212 (2001)
- 4.126. R. Kiefer, R. Quay, S. Müller, K. Köhler, F. van Raay, B. Raynor, W. Pletschen, H. Massler, S. Ramberger, M. Mikulla, G. Weimann, in *Proceedings of Lester Eastman Conference on High Performance Devices*, Newark, 2002, pp. 502–504
- 4.127. T. Kikkawa, M. Nagahara, T. Kimura, S. Yokokawa, S. Kato, M. Yokoyama, Y. Tateno, K. Horino, K. Domen, Y. Yamaguchi, N. Hara, K. Joshin, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1815–1818
- 4.128. T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tateno, Y. Yamaguchi, N. Hara, K. Joshin, P. Asbeck, in *IEDM Technical Digest*, Washington DC, 2001, pp. 585–588
- 4.129. B. Kim, J. Lee, H. Park, Y. Park, T. Kim, *J. Electron. Mater.* **27**, L32 (1997)
- 4.130. H. Kim, J. Lee, W. Lu, *Phys. Stat. Sol. A* **202**, 841 (2005)
- 4.131. H. Kim, R. Thompson, V. Tilak, T. Prunty, J. Shealy, L. Eastman, *IEEE Electron Device Lett.* **24**, 421 (2003)

- 4.132. J. Kim, F. Ren, B. Gila, C. Abernathy, S. Pearton, *Appl. Phys. Lett.* **82**, 739 (2003)
- 4.133. J. Kim, J. Je, J. Lee, Y. Park, T. Kim, I. Jung, B. Lee, J. Lee, *J. Electron. Mater.* **30**, L8 (2001)
- 4.134. S. Kim, B. Bang, F. Ren, J. D'Entremont, J. Blumenfeld, T. Cordock, S. Pearton, *J. Electron. Mater.* **33**, 477 (2004)
- 4.135. P. Klein, S. Binari, J. Freitas, A. Wickenden, *J. Appl. Phys.* **88**, 2843 (2000)
- 4.136. P. Klein, S. Binari, K. Ikosso-Anastasiou, A. Wickenden, D. Koleske, R. Henry, D. Katzer, *Electron. Lett.* **37**, 661 (2001)
- 4.137. Y. Knafo, I. Toledo, I. Hallakoun, J. Kaplun, G. Bunin, T. Baksht, B. Hadad, Y. Shapira, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.4
- 4.138. E. Kohn, in *Proceedings of SODC*, Nanjing, 2000, pp. 13–16
- 4.139. G. Koley, V. Tilak, L. Eastman, M. Spencer, *IEEE Trans. Electron Devices* **50**, 886 (2003)
- 4.140. N. Kolias, T. Kazior, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 4.141. P. Kordos, J. Bernat, D. Gregusova, M. Marso, H. Lüth, *Semicond. Sci. Technol.* **21**, 67 (2006)
- 4.142. P. Kordos, J. Bernat, M. Marso, H. Lüth, F. Rampazzo, G. Tamiazzo, R. Pierobon, G. Meneghesso, *Appl. Phys. Lett.* **86**, 253511 (2005)
- 4.143. A. Koudymov, V. Adivarahan, J. Yang, G. Simin, M. Khan, *IEEE Electron Device Lett.* **26**, 704 (2005)
- 4.144. A. Koudymov, G. Simin, M. Khan, A. Tarakji, R. Gaska, M. Shur, *IEEE Electron Device Lett.* **24**, 680 (2003)
- 4.145. P. Kozodoy, J. Ibbetson, H. Mar, P. Fini, S. Keller, J. Speck, S. DenBaars, U. Mishra, *Appl. Phys. Lett.* **73**, 975 (1998)
- 4.146. O. Krüger, C. Scholz, R. Grundmüller, H. Wittrich, P. Wolter, J. Würfl, G. Tränkle, in *Euro-Med. Symposium on Laser Induced Breakdown Spectroscopy*, Crete, 2003, p. 22
- 4.147. S. Kucheyev, J. Williams, S. Pearton, *Mat.Sci.Eng. R* **33**, 51 (2001)
- 4.148. V. Kumar, J. Lee, A. Kuliev, R. Schwindt, R. Birkhahn, D. Gotthold, S. Guo, B. Albert, I. Adesida, *Electron. Lett.* **39**, 1609 (2003)
- 4.149. V. Kumar, W. Lu, F. Khan, R. Schwindt, A. Kuliev, J.Y.M. Khan, I. Adesida, in *IEDM Technical Digest*, Washington DC, 2001, pp. 573–576
- 4.150. V. Kumar, W. Lu, R. Schwindt, A. Kuliev, G. Simin, J. Yang, M. Khan, I. Adesida, *IEEE Electron Device Lett.* **23**, 455 (2002)
- 4.151. T. Kunii, M. Totsuka, Y. Kamo, Y. Yamamoto, H. Takeuchi, Y. Shimada, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, S. Nakatsuka, A. Inoue, T. Oku, T. Nanjo, T. Oishi, T. Ishikawa, Y. Matsuda, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 197–200
- 4.152. B. Lee, S. Jung, J. Lee, Y. Park, M. Paek, K. Cho, *Semicond. Sci. Technol.* **16**, 471 (2001)
- 4.153. C. Lee, P. Saunier, H. Tserng, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 177–180
- 4.154. C. Lee, H. Kao, *Appl. Phys. Lett.* **76**, 2364 (2000)
- 4.155. J. Lee, D. Liu, H. Kim, W. Lu, *Solid-State Electron.* **48**, 1855 (2004)
- 4.156. J. Lee, K. Chang, I. Lee, S. Park, *J. Electrochem. Soc.* **147**, 1859 (2000)
- 4.157. J. Lee, C. Huh, D. Kim, S. Park, *Semicond. Sci. Technol.* **18**, 530 (2003)

- 4.158. H. Leier, A. Wieszt, R. Bethasch, H. Tobler, A. Vescan, R. Dietrich, A. Schurr, H. Sledzik, J. Birbeck, R. Balmer, T. Martin, in *Proceedings of European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, London, 2001, pp. 49–52
- 4.159. B. Leung, N. Chan, W. Fong, C. Zhu, S. Ng, H. Lui, K. Tong, C. Surya, L. Lu, W. Ge, IEEE Trans. Electron Devices **49**, 314 (2003)
- 4.160. C. Lin, W. Wang, P. Lin, C. Lin, Y. Chang, Y. Chan, IEEE Electron Device Lett. **26**, 710 (2005)
- 4.161. M. Lin, Z. Fan, Z. Ma, L. Allen, H. Morkoc, Appl. Phys. Lett. **64**, 887 (1994)
- 4.162. M. Lin, Z. Ma, F. Huang, Z. Fan, L. Allen, H. Morkoc, Appl. Phys. Lett. **64**, 1003 (1994)
- 4.163. Q. Liu, S. Lau, Solid-State Electron. **42**, 677 (1998)
- 4.164. T. Lodhi, J. McMonagle, R. Davis, D. Brookbanks, S. Combe, M. Clausen, M.F. O'Keefe, A. Collar, J. Atherton, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 125–128
- 4.165. R. Lossy, P. Heymann, J. Würfl, N. Chaturvedi, S. Müller, K. Köhler, in *Proceedings of European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Milano, 2002, pp. 23–27
- 4.166. R. Lossy, J. Hilsenbeck, J. Würfl, K. Köhler, H. Obloh, Phys. Stat. Sol. A **188**, 263 (2001)
- 4.167. R. Lossy, A. Liero, O. Krüger, J. Wüerl, G. Tränkle, Phys. Stat. Sol. C **3**, 482 (2005)
- 4.168. R. Lossy, A. Liero, J. Würfl, G. Tränkle, in *IEDM Technical Digest*, Washington DC, 2005, pp. 580–582
- 4.169. B. Luo, R. Mehandru, J. Kim, F. Ren, B. Gila, A. Onstine, C. Abernathy, S. Pearton, D. Gotthold, R. Birkhan, B. Peres, R. Fitch, N. Moser, J. Gillispie, G. Jessen, T. Jenkins, M. Yannuzzi, G. Via, A. Crespo, Solid-State Electron. **47**, 1781 (2003)
- 4.170. B. Luo, R. Mehandru, J. Kim, F. Ren, B. Gila, A. Onstine, C. Abernathy, S. Pearton, D. Gotthold, R. Birkhan, B. Peres, R. Fitch, N. Moser, J. Gillispie, G. Jessen, T. Jenkins, M. Yannuzzi, G. Via, A. Crespo, Solid-State Electron. **48**, 355 (2004)
- 4.171. B. Luo, R. Mehandru, J. Kim, F. Ren, B. Gila, A. Onstine, C. Abernathy, S. Pearton, R. Fitch, J. Gillespie, R. Dellmer, T. Jenkins, J. Sewell, D. Via, A. Crespo, Solid-State Electron. **46**, 2185 (2002)
- 4.172. L. Ma, K. Adeni, C. Zeng, Y. Jin, K. Dandu, Y. Saripalli, M. Johnson, D. Barlage, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 105–109
- 4.173. T. Makimoto, Y. Yamauchi, K. Kumakura, Appl. Phys. Lett. **84**, 1964 (2004)
- 4.174. K. Matocha, R. Gutmann, T. Chow, IEEE Trans. Electron Devices **50**, 1200 (2003)
- 4.175. L. McCarthy, I. Smorchkova, H. Xing, P. Kozodoy, P. Fini, J. Limb, D. Pulfrey, J. Speck, M. Rodwell, S. DenBaars, U. Mishra, IEEE Trans. Electron Devices **48**, 543 (2001)
- 4.176. G. Meneghesso, A. Chini, E. Zanoni, M. Manfredi, M. Pavesi, B. Boudart, C. Gaquiere, in *IEDM Technical Digest*, San Francisco, 2000, pp. 389–392
- 4.177. G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. Mishra, C. Canali, E. Zanoni, IEEE Trans. Electron Devices **51**, 1554 (2004)

- 4.178. D. Meyer, J. Flemish, J. Redwing, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 305–308
- 4.179. S.D. Meyer, C. Charbonniaud, R. Quere, M. Campovecchio, R. Lossy, J. Würfl, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 455–458
- 4.180. M. Micovic, A. Kurdhoghlian, H. Moyer, P. Hashimoto, A. Schmitz, I. Milosavljevic, P. Willadsen, W. Wong, J. Duvall, M. Hu, M. Wetzel, D. Chow, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 173–176
- 4.181. J. Mileham, S. Pearton, C. Abernathy, J. MacKenzie, R. Shul, S. Kilcoyne, *Appl. Phys. Lett.* **67**, 1119 (1995)
- 4.182. M. Minsky, M. White, E. Hu, *Appl. Phys. Lett.* **68**, 1531 (1996)
- 4.183. N. Miura, T. Oishi, T. Nanjo, M. Suita, Y. Abe, T. Ozeki, H. Ishikawa, T. Egawa, *IEEE Trans. Electron Devices* **51**, 297 (2004)
- 4.184. T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, K. Maezawa, *IEEE Trans. Electron Devices* **50**, 2015 (2003)
- 4.185. J. Moon, D. Wong, T. Hussain, M. Micovic, P. Deelmann, H. Ming, M. Antcliffe, C. Ngo, P. Hashimoto, L. McCray, in *Device Research Conference*, Santa Barbara, 2002, pp. 23–24
- 4.186. J. Moon, S. Wu, D. Wong, I. Milosavljevic, A. Conway, P. Hashimoto, M. Hu, M. Antcliffe, M. Micovic, *IEEE Electron Device Lett.* **26**, 348 (2005)
- 4.187. T. Mori, M. Kase, K. Hashimoto, M. Kojima, T. Sugii, in *IEDM Technical Digest*, Washington DC, 2003, pp. 623–626
- 4.188. H. Morkoc, *Nitride Semiconductors and Devices*. Springer Series in Materials Science, vol. 32 (Springer, Berlin Heidelberg New York, 1999)
- 4.189. H. Morkoc, *Nitride Semiconductors and Devices*. Springer Series in Materials Science, vol. 32 (Springer, Berlin Heidelberg New York, 1999) Chap. 6
- 4.190. Z. Mouffak, N. Medelci-Djezzar, C. Boney, A. Bensaoula, L. Trombetta, *MRS Internet J. Nitride Semicond. Res.* **8**, 7 (2003)
- 4.191. T. Murata, M. Hikita, Y. Hirose, Y. Uemoto, K. Inoue, T. Tanaka, D. Ueda, *IEEE Trans. Electron Devices* **52**, 1042 (2005)
- 4.192. S. Nakamura, M. Senoh, T. Mukai, *Appl. Phys. Lett.* **62**, 2390 (1993)
- 4.193. T. Nanjo, N. Miura, T. Oishi, M. Suita, Y. Abe, T. Ozeki, S. Nakatsuka, A. Inoue, T. Ishikawa, Y. Matsuda, H. Ishikawa, T. Egawa, *Jpn. J. Appl. Phys.* **43**, 1925 (2004)
- 4.194. M. Neuburger, J. Allgaier, T. Zimmermann, I. Daumiller, M. Kunze, R. Birkhahn, D. Gotthold, E. Kohn, *IEEE Electron Device Lett.* **25**, 256 (2004)
- 4.195. G. Neumark, I. Kuskovsky, H. Jiang (eds.), *Wide Bandgap Light Emitting Materials and Devices* (Wiley-VCH, Weinheim, 2007)
- 4.196. M. Nishijima, T. Murata, Y. Hirose, M. Hikita, N. Negoro, H. Sakai, Y. Uemoto, K. Inoue, T. Tanaka, D. Ueda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 299–302
- 4.197. K. Nishizono, M. Okada, M. Kamei, D. Kikuta, K. Tominaga, Y. Ohno, J. Ao, *Appl. Phys. Lett.* **84**, 3996 (2004)
- 4.198. S. Nuttinck, S. Pinel, E. Gebara, J. Laskar, M. Harris, in *Proceedings of European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Munich, 2003, pp. 213–215
- 4.199. T. Oishi, N. Miura, M. Suita, T. Nanjo, Y. Abe, T. Ozeki, *J. Appl. Phys.* **94**, 1662 (2003)

- 4.200. T. Palacios, E. Snow, Y. Pei, A. Chakraborty, S. Keller, S. DenBaars, U.K. Mishra, in *IEDM Technical Digest*, Washington DC, 2005, pp. 787–789
- 4.201. S. Pearton, J. Zolper, R. Shul, and F. Ren, *J. Appl. Phys.* **86**, 1 (1999)
- 4.202. S. Pearton, C. Abernathy, B. Gila, F. Ren, J. Zavada, Y. Park, *Solid-State Electron.* **48**, 1965 (2002)
- 4.203. S. Pearton, C. Abernathy, C. Vartuli, *Solid-State Electron.* **42**, 2269 (1998)
- 4.204. S. Pearton, R. Shul, F. Ren, *MRS Internet J. Nitride Semicond. Res.* **5**, 11 (2000)
- 4.205. A. Ping, D. Selvanathan, C. Youtsey, E. Piner, J. Redwing, I. Adesida, *Electron. Lett.* **35**, 2141 (1999)
- 4.206. A. Polyakov, N. Smirnov, A. Govorkov, K. Baik, S. Pearton, B. Luo, F. Ren, J. Zavada, *J. Appl. Phys.* **94**, 3960 (2003)
- 4.207. S. Rajan, P. Waltereit, C. Poblenz, S. Heikman, D. Green, J. Speck, U. Mishra, *IEEE Electron Device Lett.* **25**, 247 (2004)
- 4.208. C. Ramesh, V. Reddy, C. Choi, *Mater. Sci. Eng. B* **112**, 30 (2004)
- 4.209. E. Readinger, J. Robinson, S. Mohney, R. Therrien, *Semicond. Sci. Technol.* **20**, 389 (2005)
- 4.210. V. Reddy, S. Kim, J. Song, T. Seong, *Solid-State Electron.* **48**, 1563 (2004)
- 4.211. F. Ren, J. Han, R. Hickman, J.V. Hove, P. Chow, J. Klaasen, J. LaRoche, K. Jung, H. Cho, X. Cao, S. Donovan, R. Kopf, R. Wilson, A. Baca, R. Shul, L. Zhang, C. Willison, C. Abernathy, S. Pearton, *Solid-State Electron.* **44**, 239 (2000)
- 4.212. F. Ren, J. Lothian, S. Pearton, C. Abernathy, C. Vartuli, J. Mackenzie, R. Wilson, R. Karlicek, *J. Electron. Mater.* **26**, 1287 (1997)
- 4.213. P. Roussell, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 231–232
- 4.214. P. Ruterana, M. Albrecht, J. Neugebauer (eds.), *Nitride Semiconductors: Handbook on Materials and Device* (Wiley-VCH, Weinheim, 2003)
- 4.215. D. Sahoo, R. Lal, H. Kim, V. Tilak, L. Eastman, *IEEE Trans. Electron Devices* **50**, 1163 (2003)
- 4.216. W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Otmura, T. Ogura, *IEEE Trans. Electron Devices* **52**, 159 (2005)
- 4.217. W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, *IEEE Trans. Electron Devices* **53**, 356 (2006)
- 4.218. W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Omura, *Jpn. J. Appl. Phys.* **43**, 2239 (2004)
- 4.219. J. Schalwig, G. Müller, U. Karrer, M. Eickhoff, O. Ambacher, M. Stutzmann, L. Görgens, G. Dollinger, *Appl. Phys. Lett.* **80**, 1222 (2002)
- 4.220. R. Schul, C. Willison, M. Bridges, J. Han, J. Lee, S. Pearton, C. Abernathy, J. Mackenzie, S. Donovan, *Solid-State Electron.* **42**, 2269 (1998)
- 4.221. J. Shealy, in *GaAs-IC Symposium Short Course: Emerging Technologies from Defense to Commercial*, San Diego, 2003
- 4.222. J. Shealy, in *CSIC-IC Symposium Short Course: Emerging Technologies from Defense to Commercial*, Palm Springs, 2005
- 4.223. J. Sheats, B. Smith (eds.), *Microlithography: Science and Technology* (Marcel Dekker, New York, 1998)
- 4.224. B. Shelton, D. Lambert, J. Huang, M. Wong, U. Chowdhury, T. Zhu, H. Kwon, Z. Weber, M. Benarama, M. Feng, R. Dupuis, *IEEE Trans. Electron Devices* **48**, 490 (2001)

- 4.225. L. Shen, R. Coffie, D. Buttari, S. Heikman, A. Chakraborty, A. Chini, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **25**, 7 (2004)
- 4.226. J. Sheu, Y. Su, G. Chi, P. Koh, M. Jou, C. Chang, C. Liu, W. Hung, Appl. Phys. Lett. **74**, 2340 (1999)
- 4.227. S. Sheu, J. Liou, C. Huang, IEEE Trans. Electron Devices **45**, 326 (1998)
- 4.228. K. Shiojima, D. McInturff, J. Woodall, P. Grudowski, C. Eiting, R. Dupuis, J. Electron. Mater. **28**, 228 (1999)
- 4.229. E. Silkowski, Y. Yeo, R. Hengehold, M. Khan, T. Lei, K. Evans, C. Cerny, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 813–818.
- 4.230. G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. Khan, M. Shur, R. Gaska, Appl. Phys. Lett. **79**, 2651 (2001)
- 4.231. D. Siriex, D. Barataud, R. Sommet, O. Noblanc, Z. Ouarch, C. Brylinski, J. Teyssier, R. Quere, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 765–768
- 4.232. S. Sivakumar, in *IEDM Technical Digest*, San Francisco, 2006, pp. 985–988
- 4.233. D. Stocker, E. Schubert, J. Redwing, Appl. Phys. Lett. **73**, 2654 (1998)
- 4.234. S. Strite, P. Epperlein, A. Dommann, A. Rockett, R. Broom, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 795–800.
- 4.235. Y. Su, S. Chang, T. Kuan, C. Ko, J. Webb, W. Lan, Y. Cherng, S. Chen, Mater. Sci. Eng. B **110**, 260 (2004)
- 4.236. C.S. Suh, A. Chini, Y. Fu, C. Poblenz, J.S. Speck, U.K. Mishra, in *Device Research Conference*, State College PA, 2006, pp. 163–166
- 4.237. Y. Sun, L. Eastman, IEEE Trans. Electron Devices **52**, 1689 (2005)
- 4.238. K. Suzue, S. Mohammad, Z. Fan, W. Kim, O. Aktas, A. Botchkarev, H. Morkoc, J. Appl. Phys. **80**, 4467 (1996)
- 4.239. H. Takenaka, D. Ueda, IEEE Trans. Electron Devices **43**, 238 (1996)
- 4.240. K. Tan, D. Streit, R. Dia, S. Wang, A. Han, P. Chow, T. Trinh, P. Liu, J. Velebir, H. Yen, IEEE Electron Device Lett. **12**, 213 (1991)
- 4.241. W. Tan, P. Houston, G. Hill, R. Airey, P. Parbook, J. Electron. Mater. **33**, 400 (2004)
- 4.242. W. Tan, M. Uren, P. Houston, R. Green, R. Balmer, T. Martin, IEEE Electron Device Lett. **27**, 1 (2006)
- 4.243. R. Therrien, S. Singhal, J. Johnson, W. Nagy, R. Borges, A. Chaudhari, A. Hanson, A. Edwards, J. Marquart, P. Rajagopal, C. Park, I. Kizilyalli, K. Linthicum, in *IEDM Technical Digest*, Washington DC, 2005, pp. 568–571
- 4.244. R. Thompson, V. Kaper, T. Prunty, J. Shealy, in *GaAs IC Symposium Technical Digest*, San Diego, 2003, pp. 298–300
- 4.245. R. Thompson, T. Prunty, V. Kaper, J. Shealy, IEEE Trans. Electron Devices **51**, 292 (2004)
- 4.246. V. Tilak, B. Green, H. Kim, R. Dimitrov, J. Smart, W. Schaff, J. Shealy, L. Eastman, in *Proceedings of the International Symposium Compound Semiconductors*, Monterey, 2000, pp. 357–363
- 4.247. J. Torvik, J. Pankove, B.V. Zeghbroeck, IEEE Trans. Electron Devices **46**, 1326 (1999)
- 4.248. D. Tossell, K. Powell, M. Bourke, Y. Song, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, St. Louis, 2000, pp. 79–82

- 4.249. S. Trassaert, B. Boudart, C. Gaquiere, D. Theron, Y. Crosnier, F. Huet, M. Poisson, *Electron. Lett.* **35**, 1386 (1999)
- 4.250. H. Tseng, C. Capasso, J. Schaeffer, E. Hebert, P. Tobin, D.C. Gilmer, D. Triyoso, M.E. Ramon, S. Kalpat, E. Luckowski, W. Taylor, Y. Jeon, O. Adetutu, R. Hegde, R. Noble, M. Jahanbani, C.E. Chemali, B. White, in *IEDM Technical Digest*, San Francisco, 2004, pp. 821–824
- 4.251. Y. Uemoto, D. Shibata, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai, N. Batta, M. Li, T. Ueda, T. Tanaka, D. Ueda, in *IEDM Technical Digest*, Washington DC, 2007, pp. 861–864
- 4.252. M. Uren, T. Martin, M. Kuball, J. Hayes, B. Hughes, K. Hilton, R. Balmer, in *IMS Workshop Wide Bandgap Technologies*, Seattle, 2002
- 4.253. M. Uren, K. Nash, R. Balmer, T. Martin, E. Morvan, N. Caillas, S. Delage, D. Ducatteau, B. Grimbert, J. de Jaeger, *IEEE Trans. Electron Devices* **53**, 395 (2006)
- 4.254. I. Usov, N. Parikh, D. Thomson, R. Davis, *MRS Internet J. Nitride Semicond. Res.* **7**, 1 (2002)
- 4.255. F. van Raay, R. Quay, R. Kiefer, W. Fehrenbach, W. Bronner, M. Kuri, F. Benkhelifa, H. Massler, S. Müller, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings of European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Paris, 2005, pp. 233–236
- 4.256. C. Varmazis, G. D'Urso, H. Hendricks, *Semiconduct. Int.* **23**, 87 (2000)
- 4.257. C. Vartuli, S. Pearton, C. Abernathy, J.M. Kenzie, M. Lovejoy, R. Shul, J. Zolper, A. Baca, M. Hagerott-Crawford, K. Jones, F. Ren, *Solid-State Electron.* **41**, 531 (1997)
- 4.258. H. Venugopalan, S. Mohney, *Appl. Phys. Lett.* **73**, 1242 (1998)
- 4.259. G. Verzellesi, R. Pierobon, F. Rampazzo, G. Meneghesso, A. Chini, U. Mishra, C. Canali, E. Zanoni, in *IEDM Technical Digest*, San Francisco, 2002, pp. 689–692
- 4.260. R. Vetur, PhD thesis, University of California Santa Barbara, Santa Barbara, 2000
- 4.261. R. Vetur, Y. Wu, P.T. Fini, G. Parish, S. Keller, S. DenBaars, U. Mishra, in *IEDM Technical Digest*, San Francisco, 1998, pp. 55–58
- 4.262. R. Vetur, N. Zhang, S. Keller, U. Mishra, *IEEE Trans. Electron Devices* **48**, 560 (2001)
- 4.263. G. Via, S. Binary, D. Judy, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 19–22
- 4.264. A. Wakejima, K. Ota, K. Matsunaga, M. Kuzuhara, *IEEE Trans. Electron Devices* **50**, 1983 (2003)
- 4.265. R. Wang, Y. Cai, C. Tang, K. Lau, K. Chen, *IEEE Electron Device Lett.* **27**, 793 (2005)
- 4.266. W. Wang, Y. Li, C. Lin, Y. Chan, G. Chen, J. Chyi, *IEEE Electron Device Lett.* **25**, 52 (2004)
- 4.267. W. Wang, C. Lin, P. Lin, C. Lin, F. Huang, Y. Chan, G. Chen, J. Chyi, *IEEE Electron Device Lett.* **25**, 763 (2004)
- 4.268. W. Wang, P. Lin, C. Lin, C. Lin, Y. Chan, *IEEE Electron Device Lett.* **26**, 5 (2005)
- 4.269. X. Wang, L. He, *J. Electron. Mater.* **27**, 1272 (1998)
- 4.270. A. Ward, in *IMS Workshop WFI GaN Device and Circuit Reliability*, Honolulu, 2007

- 4.271. O. Weidemann, M. Hermann, G. Steinhoff, H. Wingbrant, A. Spetz, M. Stutzmann, M. Eickhoff, *Appl. Phys. Lett.* **83**, 773 (2003)
- 4.272. J. Wu, J. del Alamo, K. Jenkins, in *IEDM Technical Digest*, San Francisco, 2000, pp. 477–481
- 4.273. J. Wu, J. Scholvin, J.D. Alamo, *IEEE Trans. Electron Devices* **48**, 2181 (2001)
- 4.274. Y. Wu, PhD thesis, University of California Santa Barbara, Santa Barbara, 1997
- 4.275. Y. Wu, B. Keller, P. Fini, S. Keller, T. Jenkins, L. Kehias, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **19**, 50 (1998)
- 4.276. Y. Wu, M. Moore, T. Wisleder, P. Chavarkar, U. Mishra, P. Parikh, in *IEDM Technical Digest*, San Francisco, 2004, pp. 1078–1079
- 4.277. Y. Wu, S. Keller, P. Kozodoy, B. Keller, P. Parikh, D. Kapolnek, S. DenBaars, U. Mishra,
- 4.278. Y. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh, in *Device Research Conference*, State College PA, 2006, pp. 151–152
- 4.279. Y. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, P. Parikh, *IEEE Electron Device Lett.* **25**, 117 (2004)
- 4.280. Y. Wu, A. Saxler, M. Moore, T. Wisleder, U. Mishra, P. Parikh, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 170–172
- 4.281. H. Xing, P. Chavarkar, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **24**, 141 (2003)
- 4.282. H. Xing, S. DenBaars, U. Mishra, *J. Appl. Phys.* **97**, 113703 (2005)
- 4.283. H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, U. Mishra, *IEEE Electron Device Lett.* **25**, 161 (2004)
- 4.284. H. Xing, L. McCarthy, S. Keller, S. DenBaars, U. Mishra, in *Proceedings of the International Symposium Compound Semiconductors*, Monterey, 2000, pp. 365–369
- 4.285. Y. Liu, J. Bardwell, S. McAlister, S. Rolfe, H. Tang, J. Webb, *J. Appl. Phys.* **96**, 2674 (2004)
- 4.286. E. Young, H. Hendriks, G. Rojano, R. Baskaran, T. Ritzdorf, J. Klocke, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, San Diego, 2002, pp. 180–183
- 4.287. C. Youtsey, I. Adesida, G. Bulman, *Electron. Lett.* **33**, 245 (1997)
- 4.288. C. Youtsey, I. Adesida, L. Romano, G. Bulman, *Appl. Phys. Lett.* **72**, 560 (1999)
- 4.289. H. Yu, L. McCarthy, S. Rajan, S. Keller, S. DenBaars, J. Speck, U. Mishra, *IEEE Electron Device Lett.* **26**, 283 (2005)
- 4.290. H. Yu, L. McCarthy, H. Xing, P. Waltereit, L. Shen, S. Keller, S. DenBaars, J. Speck, U. Mishra, *Appl. Phys. Lett.* **85**, 5254 (2004)
- 4.291. L. Yu, L. Jia, D. Qiao, S. Lau, J. Li, J. Lin, H. Jiang, *IEEE Trans. Electron Devices* **50**, 500 (2003)
- 4.292. L. Yu, D. Qiao, Q. Xing, S. Lau, K. Boutros, J. Redwing, *Appl. Phys. Lett.* **73**, 238 (1998)
- 4.293. H.V. Zeijl, L. Nanver, in *Solid-State Circuits Technical Conference*, Beijing, 1998, pp. 98–101
- 4.294. N. Zhang, S. Keller, F. Parish, S. Heikman, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **21**, 373 (2000)

- 4.295. N. Zhang, B. Moran, S. DenBaars, U. Mishra, X. Wang, T. Ma, in *IEDM Technical Digest*, Washington DC, 2001, pp. 589–592
- 4.296. C. Zhu, W. Fong, B. Leung, C. Cheng, C. Surya, IEEE Trans. Electron Devices **48**, 1225 (2001)
- 4.297. J. Zolper, M. Crawford, A. Howard, S. Pearton, R. Abernathy, C. Vartuli, C. Yuan, R. Stall, J. Ramer, S. Hersee, R. Wilson, in *MRS Symposium*, First International Conference on Nitride Semiconductors, vol. 395, Boston, 1996, pp. 801–806.
- 4.298. J. Zolper, R. Shul, A. Baca, R. Wilson, S. Pearton, R. Stall, Appl. Phys. Lett. **68**, 2273 (1996)

References of Chapter 5

- 5.1. A. Alabadelah, T. Fernandez, A. Mediavilla, B. Nauwelaers, A. Santarelli, D. Schreurs, A. Tazon, P. Traverso, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Amsterdam, 2004, pp. 191–195
- 5.2. K. Anderson, C. Fager, J. Pedro, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1159–1162
- 5.3. Y. Ando, A. Cappy, K. Marubashi, K. Onda, H. Miyamoto, M. Kuzuhara, *IEEE Trans. Electron Devices* **44**, 1367 (1997)
- 5.4. Y. Ando, W. Contrata, N. Samoto, H. Miyamoto, K. Matsunaga, M. Kuzuhara, K. Kunihiro, K. Kasahara, T. Nakayama, Y. Takahashi, N. Hayama, Y. Ohno, *IEEE Trans. Electron Devices* **47**, 1965 (2000)
- 5.5. I. Angelov, L. Bengtsson, M. Garcia, in *IEEE International Microwave Symposium Digest*, Orlando, 1995, pp. 1515–1518
- 5.6. I. Angelov, L. Bengtsson, M. Garcia, *IEEE Trans. Microw. Theory Tech.* **44**, 1664 (1996)
- 5.7. I. Angelov, V. Desmaris, K. Dynefors, P. Nilsson, N. Rorsman, H. Zirath, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Paris, 2005, pp. 309–312
- 5.8. I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, H. Zirath, in *IEEE International Microwave Symposium Digest*, Anaheim, 1999, pp. 525–528
- 5.9. I. Angelov, H. Zirath, *Electron. Lett.* **28**, 129 (1992)
- 5.10. I. Angelov, H. Zirath, N. Rorsman, *IEEE Trans. Microw. Theory Tech.* **40**, 2258 (1992)
- 5.11. I. Angelov, H. Zirath, N. Rorsman, in *IEEE International Microwave Symposium Digest*, San Diego, 1994, pp. 1571–1574
- 5.12. F. Benkhelifa, R. Kiefer, S. Müller, F. van Raay, R. Quay, R. Sah, M. Mikulla, G. Weimann, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.4
- 5.13. J. Bernat, M. Wolter, M. Marso, J. Flynn, G. Brandes, P. Kordos, *Electron. Lett.* **40**, 78 (2004)
- 5.14. M. Berroth, R. Bosch, *IEEE Trans. Microw. Theory Tech.* **38**, 891 (1990)
- 5.15. U. Bhapkar, M. Shur, *J. Appl. Phys.* **82**, 1649 (1997)
- 5.16. S. Binari, P. Klein, T. Kazior, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1823–1826

- 5.17. J.R. Black, IEEE Trans. Electron Devices **16**, 338 (1969)
- 5.18. C. Bolognesi, A. Kwan, D. DiSanto, in *IEDM Technical Digest*, San Francisco, 2002, pp. 685–688
- 5.19. F. Bonani, G. Ghione, M. Pirola, C. Naldi, in *IEDM Technical Digest*, Washington DC, 1993, pp. 101–104
- 5.20. F. Bonani, G. Ghione, M. Pirola, C. Naldi, in *GaAs IC Symposium Technical Digest*, Philadelphia, 1994, pp. 141–144
- 5.21. S. Boumaiza, F. Ghannouchi, IEEE Trans. Microw. Theory Tech. **51**, 2427 (2003)
- 5.22. H. Bousbia, D. Barataud, G. Neveux, T. Gasseling, J. Nebus, J. Tessier, in *IEEE International Microwave Symposium Digest*, San Franscisco, 2006, pp. 1452–1455
- 5.23. R. Brady, G. Valdivia, T. Brazil, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 593–596
- 5.24. B. Brar, K. Boutros, R. deWarnes, V. Tilak, R. Shealy, L. Eastman, in *Proceedings of Lester Eastman Conference on High Performance Devices*, Newark, 2002, pp. 487–491
- 5.25. J. Brinkhoff, A. Parker, IEEE Trans. Microw. Theory Tech. **51**, 1045 (2003)
- 5.26. J. Brinkhoff, A. Parker, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 799–802
- 5.27. J. Brinkhoff, A. Parker, in *Workshop Application Radio Science*, Hobart, 2004, pp. 1–8
- 5.28. J. Brinkhoff, A. Parker, M. Leung, IEEE Trans. Microw. Theory Tech. **51**, 2523 (2003)
- 5.29. B. Bunz, A. Ahmed, G. Kompa, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS* Paris, 2005, pp. 649–652
- 5.30. P. Cabral, J. Pedro, N. Carvalho, IEEE Trans. Microw. Theory Tech. **52**, 2585 (2004)
- 5.31. Y. Cai, Y. Zhou, K. Chen, K. Lau, in *Device Research Conference*, Santa Barbara, 2005, pp. 179–180
- 5.32. N. Carvalho, J. Pedro, W. Jang, M. Steer, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 801–805
- 5.33. C. Chen, M. Deen, Y. Cheng, M. Matloubian, IEEE Trans. Electron Devices **48**, 2884 (2001)
- 5.34. C. Chen, R. Coffie, K. Krishnamurthy, S. Keller, M. Rodwell, U. Mishra, IEEE Electron Device Lett. **21**, 549 (2000)
- 5.35. Y. Chen, R. Coffie, W. Luo, M. Wojtowicz, I. Smorchkova, B. Heying, Y. Kim, M. Aust, A. Oki, in *IEEE International Microwave Symposium Digest*, Honolulu, 1998, pp. 137–140
- 5.36. S. Chiu, A. Anwar, S. Wu, IEEE Trans. Electron Devices **47**, 662 (2000)
- 5.37. Y. Chou, D. Leung, R. Lai, R. Grundbacher, M. Barsky, Q. Kan, R. Tsai, M. Wojtowicz, D. Eng, L. Tran, T. Block, P. Liu, M. Nishimoto, A. Oki, IEEE Electron Device Lett. **24**, 378 (2003)
- 5.38. . Colvin, S. Bhatia, K. O, IEEE J. Solid-State Circuits **34**, 1339 (1999)
- 5.39. A. Conway, P. Asbeck, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 605–608
- 5.40. A. Conway, Y. Zhao, P. Asbeck, M. Micovic, J. Moon, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 499–502

- 5.41. S. Cripps, in *IEEE International Microwave Symposium Digest*, Boston, 1983, pp. 221–223
- 5.42. G. Crupi, D. Xiao, D. Schreurs, E. Limiti, A. Caddemi, W. De Raedt, M. Germain, *IEEE Trans. Microw. Theory Tech.* **54**, 3616 (2006)
- 5.43. W. Curtice, *IEEE Trans. Microw. Theory Tech.* **28**, 448 (1980)
- 5.44. W. Curtice, in *IMS Workshop WMG: Solid-State Power Invades the Tube Realm*, Honolulu, 2007
- 5.45. W. Curtice, R. Camisa, *IEEE Trans. Microw. Theory Tech.* **32**, 1573 (1984)
- 5.46. A. Curutchet, N. Malbert, N. Labat, A. Touboul, C. Gaquiere, A. Minko, M. Uren, *Microelectron. Reliab.* **43**, 1713 (2003)
- 5.47. G. Dambrine, A. Cappy, F. Heliodore, E. Playez, *IEEE Trans. Microw. Theory Tech.* **36**, 1151 (1988)
- 5.48. N. de Carvalho, J. Pedro, *IEEE Trans. Microw. Theory Tech.* **47**, 2364 (1999)
- 5.49. N. de Carvalho, J. Pedro, *IEEE Trans. Microw. Theory Tech.* **50**, 2090 (2002)
- 5.50. D. DiSanto, C. Bolognesi, *IEEE Trans. Electron Devices* **53**, 2914 (2006)
- 5.51. S. Doo, P. Roblin, G. Jessen, R. Fitch, J. Gillespie, N. Moser, A. Crespo, G. Simpson, J. King, *IEEE Microw. Wireless Compon. Lett.* **16**, 681 (2006)
- 5.52. P. Draxler, J. Jeong, C. Hsia, S. Lanfranco, W. Nagy, K. Linthicum, L. Larsson, P. Asbeck, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1549–1552
- 5.53. P. Draxler, S. Lafranco, D. Kimball, C. Hsia, J. Jeong, J. van de Sluis, P. Asbeck, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1534–1537
- 5.54. L. Eastman, V. Tilak, J. Smart, B. Green, E. Chumbes, R. Dimitrov, H. Kim, O. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. Schaff, J. Shealy, *IEEE Trans. Electron Devices* **48**, 479 (2001)
- 5.55. J. Evans, G. Amarasingha, *IEEE Trans. Electron Devices* **44**, 1148 (1997)
- 5.56. C. Fager, J. Pedro, N. de Carvalho, H. Zirath, *IEEE Trans. Microw. Theory Tech.* **50**, 2834 (2002)
- 5.57. P. Fedorenko, J. Kenney, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1453–1456
- 5.58. G. Fischer, in *IEEE Wireless and Microwave Technology Conference*, Clearwater, 2004, p. FD-1
- 5.59. M. Foisy, P. Jeroma, G. Martin, in *IEEE International Microwave Symposium Digest*, Albuquerque, 1992, pp. 251–254
- 5.60. H. Fukui, *IEEE Trans. Electron Devices* **26**, 1032 (1979)
- 5.61. J. Golio, M. Miller, G. Maracas, D. Johnson, *IEEE Trans. Electron Devices* **37**, 1217 (1990)
- 5.62. B. Green, K. Chu, E. Chumbes, J. Smart, J. Shealy, L. Eastman, *IEEE Electron Device Lett.* **21**, 268 (2000)
- 5.63. B. Green, H. Kim, K. Chu, H. Lin, V. Tilak, J. Shealy, J. Smart, L. Eastman, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 237–241
- 5.64. F. De Groote, O. Jardel, J. Verspecht, D. Barataud, J. Teyssier, R. Quere, in *Proc. ARFTG Microwave Measurement Symposium*, Washington DC, 2005
- 5.65. W. Ho, C. Surya, K. Tong, W. Kim, A. Botcharev, H. Morkoc, *IEEE Trans. Electron Devices* **46**, 1099 (1999)
- 5.66. F.N. Hooge, *IEEE Trans. Electron Devices* **41**, 1926 (1994)
- 5.67. S. Hsu, P. Valizadeh, D. Pavlidis, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 85–88

- 5.68. M. Ida, K. Kurishima, N. Watanabe, T. Enoki, in *IEDM Technical Digest*, Washington DC, 2001, pp. 776–779
- 5.69. S. Islam, A. Anwar, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 267–270
- 5.70. S. Islam, A. Anwar, *IEEE Trans. Microw. Theory Tech.* **14**, 853 (2004)
- 5.71. S. Islam, A. Anwar, *IEEE Trans. Electron Devices* **49**, 710 (2004)
- 5.72. R. Jansen, A. Smymakowski, M. Bahn, A. John, C. Rieckmann, A. Noculak, S. Chalermwisutkul, D. Klümper, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Forth Worth, 2004
- 5.73. O. Jardel, F. de Groote, C. Charbonniaud, T. Reveyrand, J. Teyssier, R. Quere, D. Floriot, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 601–604
- 5.74. O. Jardel, F. De Groote, T. Reveyrand, J.C. Jacquet, C. Charbonniaud, J. Teyssier, D. Floriot, R. Quere, *IEEE Trans. Microw. Theory Tech.* **55**, 2660 (2007)
- 5.75. A. Jarndal, G. Kompa, *IEEE Trans. Microw. Theory Tech.* **53**, 3440 (2005)
- 5.76. A. Jarndal, G. Kompa, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1423–1426
- 5.77. A. Jarndal, G. Kompa, **54**, 2830 (2007)
- 5.78. M. Je, H. Shin, *IEEE Electron Device Lett.* **24**, 183 (2003)
- 5.79. K. Jeon, Y. Kwon, S. Hong, *IEEE Microw. Guided Wave Lett.* **7**, 78 (1997)
- 5.80. J. Johnson, J. Gao, K. Lucht, J.W.C. Strautin, J. Riddle, T. Therrien, P. Rajagopal, J. Roberts, A. Vescan, J. Brown, A. Hanson, S. Singhal, R. Borges, E. Piner, K. Linthicum, *Proc. Electron. Soc.* **7**, 405 (2004)
- 5.81. S. Karmalkar, N. Satyan, D. Sathaiya, *IEEE Electron Device Lett.* **27**, 87 (2006)
- 5.82. O. Katz, G. Bahir, J. Salzmann, *IEEE Trans. Electron Devices* **37**, 2250 (1990)
- 5.83. T. Kikkawa, K. Imanishi, M. Kanamura, K. Joshin, in *Proceedings International Conference GaAs Manufacturing Technology*, San Diego, 2002, pp. 171–174
- 5.84. T. Kikkawa, T. Maniwa, H. Hayashi, M. Kanamura, S. Yokokawa, M. Nishi, N. Adachi, M. Yokoyama, Y. Tateno, K. Joshin, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1347–1350
- 5.85. T. Kikkawa, M. Nagahara, T. Kimura, S. Yokokawa, S. Kato, M. Yokoyama, Y. Tateno, K. Horino, K. Domen, Y. Yamaguchi, N. Hara, K. Joshin, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1815–1818
- 5.86. D. Kimball, P. Draxler, J. Jeong, C. Hsia, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, P. Asbeck, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 89–92
- 5.87. E. Kohn, I. Daumiller, M. Kunze, M. Neuburger, M. Seyboth, T. Jenkins, J. Sewell, J. Norstand, Y. Smorchkova, U. Mishra, *IEEE Trans. Microw. Theory Tech.* **51**, 634 (2003)
- 5.88. A. Koudymov, G. Simin, M. Khan, A. Tarakji, R. Gaska, M. Shur, *IEEE Electron Device Lett.* **24**, 680 (2003)
- 5.89. H. Ku, M. McKinley, J. Kenney, *IEEE Trans. Microw. Theory Tech.* **50**, 2843 (2002)
- 5.90. K. Ku, J. Kenney, in *IEEE International Microwave Symposium Digest*, Phoenix, 2003, pp. 799–802

- 5.91. D. Kuksenkov, H. Temkin, R. Gaska, J. Yang, IEEE Electron Device Lett. **19**, 222 (1998)
- 5.92. K. Kunihiro, Y. Ohno, IEEE Trans. Electron Devices **43**, 1336 (1996)
- 5.93. J. Kuzmik, S. Bychikhin, M. Neuburger, A. Dadgar, A. Krost, E. Kohn, D. Pogany, IEEE Trans. Electron Devices **52**, 1698 (2005)
- 5.94. J. Lee, D. Liu, Z. Lin, W. Lu, J. Flynn, G. Brandes, Solid-State Electron. **47**, 2081 (2003)
- 5.95. J. Lee, K. Webb, IEEE Trans. Microw. Theory Tech. **52**, 2 (2004)
- 5.96. K. Lee, A. Dabiran, P. Chow, A. Osinsky, S. Pearton, F. Ren, Solid-State Electron. **48**, 37 (2004)
- 5.97. K. Lee, A. Dabiran, A. Osinsky, P. Chow, S. Pearton, F. Ren, Solid-State Electron. **47**, 1501 (2003)
- 5.98. S. Lee, K. Webb, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1415–1418
- 5.99. S. Lee, K. Webb, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1057–1060
- 5.100. S. Lee, K. Webb, V. Tilak, L. Eastman, IEEE Trans. Microw. Theory Tech. **51**, 1567 (2003)
- 5.101. H. Leier, A. Wieszt, R. Bethasch, H. Tobler, A. Vescan, R. Dietrich, A. Schurr, H. Sledzik, J. Birbeck, R. Balmer, T. Martin, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, London, 2001, pp. 49–52
- 5.102. R. Leoni III, J. Bao, J. Bu, X. Du, M. Shirokov, J. Hwang, IEEE Trans. Electron Devices **47**, 498 (2000)
- 5.103. M. Li, Y. Wang, Electron Devices **55**, 261 (2008)
- 5.104. T. Li, R. Joshi, R. del Rosario, IEEE Trans. Electron Devices **49**, 1511 (2002)
- 5.105. C. Lin, W. Wang, P. Lin, C. Lin, Y. Chang, Y. Chan, IEEE Electron Device Lett. **26**, 710 (2005)
- 5.106. T. Liu, S. Boumaiza, F. Ghannouchi, IEEE Trans. Microw. Theory Tech. **53**, 3578 (2005)
- 5.107. W. Liu, *Handbook of III-V Heterojunction Bipolar Transistors* (Wiley, New York, 1998)
- 5.108. Y. Liu, R. Trew, G. Bilbro, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 597–600
- 5.109. W. Lu, V. Kumar, E. Piner, I. Adesida, IEEE Trans. Electron Devices **50**, 1069 (2003)
- 5.110. S. Manohar, A. Narayanan, A. Keerti, A. Pham, J. Brown, R. Borges, K. Linthicum, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 449–452
- 5.111. A. Materka, T. Kacprzak, IEEE Trans. Microw. Theory Tech. **33**, 129 (1985)
- 5.112. K. Matocha, T. Chow, R. Gutmann, IEEE Trans. Electron Devices **52**, 6 (2005)
- 5.113. N. Matsunaga, M. Yamamoto, Y. Hatta, H. Masuda, IEEE Trans. Electron Devices **50**, 1194 (2003)
- 5.114. L. McCarthy, PhD thesis, University of California Santa Barbara, Santa Barbara, 2001
- 5.115. L. McCarthy, L. Smorchkova, P. Fini, M. Rodwell, J. Speck, S. DenBaars, U. Mishra, Electron. Lett. **38**, 144 (2002)

- 5.116. P. McGovern, J. Benedikt, P. Tasker, J. Powell, K. Hilton, J. Glasper, R. Balmer, T. Martin, M. Uren, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 503–506
- 5.117. P. McGovern, D. Williams, P. Tasker, J. Benedikt, J. Powell, K. Hilton, R. Balmer, T. Martin, M. Uren, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 825–828
- 5.118. E. Mengistu, G. Kompa, in *Proceedings of the European Microwave Integrated Circuits Conference*, Manchester, 2006, pp. 292–295
- 5.119. T. Merkle, A. Tessmann, S. Ramberger, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 453–456
- 5.120. S.D. Meyer, C. Charbonniaud, R. Quere, M. Campovecchio, R. Lossy, J. Würfl, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 455–458
- 5.121. T. Mizutani, H. Makihara, M. Akita, Y. Ohno, S. Kishimoto, K. Maezawa, *Jpn. J. Appl. Phys.* **42**, 424 (2003)
- 5.122. T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, K. Maezawa, *IEEE Trans. Electron Devices* **50**, 2015 (2003)
- 5.123. N. Moll, M. Hueschen, A. Fischer-Colbrie, *IEEE Trans. Electron Devices* **35**, 879 (1988)
- 5.124. J. Moon, M. Micovic, A. Kurdoghlian, P. Janke, P.H.W. Wong, L. McCray, *Electron. Lett.* **38**, 1358 (2002)
- 5.125. T. Nass, D. Wiegner, U. Seyfried, W. Templ, S. Weber, S. Woerner, P. Klose, R. Quay, F. van Raay, H. Walcher, H. Massler, M. Seelmann-Eggebert, O. Kappeler, R. Kiefer, in *Joint Symposium on Opto- and Microelectronic Devices and Circuits*, Duisburg, 2006, pp. 133–136
- 5.126. A. Nidhi, T. Palacios, A. Chakraborty, S. Keller, U. Mishra, *IEEE Electron Device Lett.* **27**, 877 (2006)
- 5.127. J. Nikaido, T. Kikkawa, E. Mitani, S. Yokokawa, Y. Tateno, in *Proceedings of International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, pp. 97–100
- 5.128. S. Nuttinck, S. Pinel, E. Gebara, J. Laskar, M. Harris, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Munich, 2003, pp. 213–215
- 5.129. S. Nuttinck, E. Gebara, J. Laskar, H. Harris, *IEEE Trans. Microw. Theory Tech.* **49**, 2413 (2001)
- 5.130. C. Oxley, M. Uren, *IEEE Trans. Electron Devices* **52**, 165 (2005)
- 5.131. T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S. DenBaars, U. Mishra, *IEEE Trans. Electron Devices* **52**, 2117 (2005)
- 5.132. A. Parker, J. Scott, J. Rathmell, M. Sayed, in *IEEE International Microwave Symposium Digest*, San Francisco, 1996, pp. 1707–1710
- 5.133. A. Parker, J. Rathmell, *IEEE Trans. Microw. Theory Tech.* **49**, 2105 (2001)
- 5.134. A. Parker, J. Rathmell, *IEEE Trans. Microw. Theory Tech.* **51**, 588 (2003)
- 5.135. A. Parker, J. Rathmell, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 803–806
- 5.136. A. Parker, J. Scott, *Electron. Lett.* **29**, 1961 (1993)
- 5.137. J. Pedro, N. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits* (Artech House, Boston, 2003)
- 5.138. R. Pengelly, in *Proceedings of Wireless and Microwave Technology Conference*, Clearwater, 2004, pp. RC-5

- 5.139. J. Peransin, P. Vignaud, D. Rigaud, L. Vandamme, IEEE Trans. Electron Devices **37**, 2250 (1990)
- 5.140. M. Pospieszalski, IEEE Trans. Microw. Theory Tech. **37**, 1340 (1989)
- 5.141. W. Pribble, in *IMS Workshop WMG: High Power Device Characterization and Modeling*, Honolulu, 2007
- 5.142. W. Pribble, S. Sheppard, R. Smith, S. Allen, J. Palmour, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IMS Workshop Wide Bandgap Technologies*, Seattle, 2002
- 5.143. G. Qu, A. Parker, in *IEEE International Microwave Symposium Digest*, Baltimore, 1998, pp. 745–748,
- 5.144. R. Quay, K. Hess, R. Reuter, M. Schlechtweg, T. Grave, V. Palankovski, S. Selberherr, IEEE Trans. Electron Devices **48**, 210 (2001)
- 5.145. A. Rashmi, A. Kranti, S. Haldar, M. Gupta, R. Gupta, IEEE Trans. Microw. Theory Tech. **51**, 607 (2003)
- 5.146. P. Regoliosi, A. Reale, A.D. Carlo, P. Romanini, M. Peroni, C. Lanzieri, A. Angelini, M. Pirola, G. Ghione, IEEE Trans. Electron Devices **53**, 182 (2006)
- 5.147. R. Reuter, M. Agethen, U. Auer, S. van Waasen, D. Peters, W. Brockerhoff, F. Tegude, IEEE Trans. Microw. Theory Tech. **45**, 977 (1997)
- 5.148. R. Reuter, F. Tegude, in *IEEE International Microwave Symposium Digest*, Boston, 1998, pp. 137–140
- 5.149. P. Roblin, H. Rohdin, *High-Speed Heterostructure Devices* (Cambridge University Press, Cambridge, 2002)
- 5.150. M. Rodwell, M. Urteaga, T. Mathew, D. Scott, D. Mensa, Q. Lee, J. Guthrie, Y. Betser, S. Martin, R. Smith, S. Jaganathan, S. Krishnan, S. Long, R. Pullela, B. Agarwal, U. Bhattacharya, L. Samoska, M. Dahlstrom, IEEE Trans. Electron Devices **48**, 2606 (2001)
- 5.151. H. Rohdin, P. Roblin, IEEE Trans. Electron Devices **33**, 664 (1986)
- 5.152. D. Root, in *Proceedings of IEEE International Midwest Symposium Circuits and Systems*, Dayton, 2001, pp. 768–772
- 5.153. D. Root, S. Fan, in *IEEE International Microwave Symposium Digest*, Albuquerque, 1992, pp. 255–258
- 5.154. D. Root, M. Iwamoto, J. Wood, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 279–282
- 5.155. D. Root, in *Proceedings of European Microwave Conference*, Cannes, 1994, pp. 854–859
- 5.156. D. Root, M. Pirola, S. Fan, W. Anklam, A. Cognata, IEEE Trans. Microw. Theory Tech. **41**, 2211 (1993)
- 5.157. S. Rumyantsev, N. Pala, M. Shur, E. Borovitskaya, A. Dimitriev, M. Levenshtein, R. Gaska, M. Khan, J. Yang, X. Hu, G. Simin, IEEE Trans. Electron Devices **48**, 530 (2001)
- 5.158. F. Sacconi, A. Di Carlo, F. Della Sala, P. Lugli, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Paris, 2000, pp. 620–623
- 5.159. C. Sanabria, A. Chakraborty, H. Xu, M. Rodwell, U. Mishra, R. York, IEEE Electron Device Lett. **27**, 19 (2005)
- 5.160. C. Sanabria, X. Hongtao, T. Palacios, A. Chakraborty, S. Heikman, U. Mishra, R. York, IEEE Trans. Microw. Theory Tech. **53**, 762 (2005)
- 5.161. M. Schlechtweg, Dissertation, Universität Kassel, 1989

- 5.162. I. Schmale, G. Kompa, in *Proceedings of European Microwave Conference*, Munich, 1999, pp. 258–261
- 5.163. D. Schreurs, J. Verspecht, B. Nauwelaers, A.V. de Capelle, M. VanRossum, in *Proceedings of European Microwave Conference*, Tel Aviv, 1997, pp. 921–926
- 5.164. D. Schreurs, J. Verspecht, E. Vandamme, N. Vellas, C. Gaquiere, M. Germain, G. Borghs, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 447–450
- 5.165. D. Schreurs, J. Wood, N. Tufillaro, D. Usikov, L. Barford, D. Root, in *IEDM Technical Digest*, San Francisco, 2000, 819–822
- 5.166. M. Seelmann-Eggebert, T. Merkle, F. van Raay, R. Quay, M. Schlechtweg, *IEEE Trans. Microw. Theory Tech.* **55**, 195 (2007)
- 5.167. K. Shenai, R. Scott, B. Baliga, *IEEE Trans. Electron Devices* **36**, 1811 (1989)
- 5.168. K. Shinohara, Y. Yamashita, A. Endoh, I. Watanabe, K. Hikosaka, T. Matsui, T. Mimura, S. Hiyamizu, *IEEE Electron Device Lett.* **25**, 241 (2004)
- 5.169. M. Shur, *GaAs Devices and Circuits* (Plenum, New York, 1987)
- 5.170. F. Sischka, *The Curtice Mesfet Model* (Agilent Technologies, Böblingen, Germany, 2001)
- 5.171. H. Statz, H. Haus, R. Pucel, *IEEE Trans. Electron Devices* **21**, 549 (1974)
- 5.172. J. Stenarson, M. Garcia, I. Angelov, H. Zirath, *IEEE Trans. Microw. Theory Tech.* **47**, 2358 (1999)
- 5.173. Y. Su, S. Wei, R. Wang, S. Chang, C. Ko, T. Kuan, *IEEE Electron Device Lett.* **24**, 622 (2003)
- 5.174. T. Suemitsu, K. Shiojima, T. Makimura, N. Shigekawa, *Jpn. J. Appl. Phys.* **44**, L211 (2005)
- 5.175. H. Sun, C. Bolognesi, *Appl. Phys. Lett.* **90**, 123505 (2007)
- 5.176. W. Sutton, D. Pavlidis, H. Lahreche, B. Damilano, R. Langer, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Munich, pp. 209–212, 2003
- 5.177. S. Sze, *Physics of Semiconductor Devices*, 2nd edn. (Wiley, New York, 1981)
- 5.178. T. Takano, Y. Oishi, T. Maniwa, H. Hayashi, T. Kikkawa, K. Araki, *Microw. Opt. Tech. Lett.* **45**, 551 (2005)
- 5.179. P. Tasker, J. Braunstein, in *IEEE International Microwave Symposium Digest*, Orlando, 1995, pp. 611–614
- 5.180. P. Tasker, B. Hughes, *IEEE Electron Device Lett.* **10**, 291 (1989)
- 5.181. R. Therrien, S. Singhal, J. Johnson, W. Nagy, R. Borges, A. Chaudhari, A. Hanson, A. Edwards, J. Marquart, P. Rajagopal, C. Park, I. Kizilyalli, K. Linthicum, in *IEDM Technical Digest*, Washington DC, 2005, 568–571
- 5.182. J. Tirado, J. Sanchez-Rojas, J. Izpura, *IEEE Trans. Electron Devices*, **54**, 410 (2007)
- 5.183. S. Trassaert, B. Boudart, C. Gaquiere, D. Theron, Y. Crosnier, F. Huet, M. Poisson, *Electron. Lett.* **35**, 1386 (1999)
- 5.184. R. Trew, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1811–1814
- 5.185. R. Trew, Y. Liu, W. Kuang, R. Vetry, J. Shealy, *IEEE Trans. Microw. Theory Tech.* **54**, 2061 (2006)
- 5.186. R. Trew, Y. Liu, H. Yin, G. Bilbro, J. Shealy, R. Vetry, P. Garber, M. Poulton, in *IEEE International Microwave Symposium Digest*, San Franscisco, 2006, pp. 643–646
- 5.187. T. Turlington, *Behavioral Modeling of Nonlinear RF and Microwave Devices*, (Artech House, Boston and London, 2000)

- 5.188. N. Ui, Y. Tajima, in *IMS Workshop WMG: High Power Device Characterization and Modeling*, Honolulu, 2007
- 5.189. S. Vainshtein, V. Yuferev, J. Kostamovaara, IEEE Trans. Electron Devices **50**, 1988 (2003)
- 5.190. F. van Raay, R. Quay, R. Kiefer, H. Massler, M. Schlechtweg, G. Weimann, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 451–454
- 5.191. L.K.J. Vandamme, IEEE Trans. Electron Devices **41**, 2176 (1997)
- 5.192. N. Vellas, C. Gaquiere, F. Bue, Y. Guhel, B. Boudart, J. de Jaeger, M. Poisson, IEEE Electron Device Lett. **23**, 246 (2002)
- 5.193. A. Vertiatchikh, L. Eastman, Electron. Lett. **39**, 876 (2003)
- 5.194. A. Vertiatchikh, L. Eastman, IEEE Electron Device Lett. **24**, 535 (2003)
- 5.195. R. Vetary, N. Zhang, S. Keller, U. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001)
- 5.196. S. Vitusevich, M. Petrychuk, S. Danylyuk, A. Kurakin, N. Klein, A. Belyaev, Phys. Stat. Sol. A **202**, 816 (2005)
- 5.197. D. Wandrei, Y. Tajima, in *IMS Workshop WMG: High Power Device Characterization and Modeling*, Honolulu, 2007
- 5.198. C. Wang, C. Zhu, G. Zhang, L. Li, IEEE Trans. Electron Devices **50**, 1145 (2003)
- 5.199. J.W. Lee, S. Lee, K.J. Webb, in *IEEE International Microwave Symposium Digest*, Phoenix, 2001, pp. 679–682
- 5.200. A. Wieszt, R. Dietrich, J. Lee, A. Vescan, H. Leier, E. Piner, J. Redwing, H. Sledzik, in *Proceedings of the European Gallium Arsenide Other Compound Semiconductors Application Symposium GAAS*, Paris, 2000, pp. 260–263
- 5.201. J. Wood, D. Root, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 685–688
- 5.202. Y. Wu, P. Chavarkar, M. Moore, P. Parikh, U. Mishra, in *IEDM Technical Digest*, Washington DC, 2001, pp. 951–953
- 5.203. Y. Wu, P. Chavarkar, M. Moore, P. Parikh, U. Mishra, in *IEDM Technical Digest*, San Francisco, 2002, 697–699
- 5.204. Y. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh, in *Device Research Conference*, State College, PA, 2006, pp. 151–152
- 5.205. Y. Wu, A. Saxler, M. Moore, R. Smith, S. Sheppard, P. Chavarkar, T. Wisleder, U. Mishra, P. Parikh, IEEE Electron Device Lett. **25**, 117 (2004)
- 5.206. H. Xing, P. Chavarkar, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **24**, 141 (2003)
- 5.207. H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, U. Mishra, IEEE Electron Device Lett. **25**, 161 (2004)
- 5.208. H. Xing, D. Green, L. McCarthy, I. Smorchkova, P. Chavarkar, T. Mates, S. Keller, S. DenBaars, J. Speck, U. Mishra, in *Bipolar Circuits Technology Meeting*, Minneapolis, 2001, pp. 125–130
- 5.209. J. Xu, W. Yin, J. Mao, IEEE Microw. Wireless Compon. Lett. **17**, 55 (2007)
- 5.210. S. Yamakawa, S. Aboud, M. Saraniti, S. Goodnick, Semicond. Sci. Technol. **19**, S475 (2004)
- 5.211. N. Zhang, B. Moran, S. DenBaars, U. Mishra, X. Wang, T. Ma, in *IEDM Technical Digest*, Washington DC, 2001, pp. 589–592

References of Chapter 6

- 6.1. E. Alekseev, S. Hsu, D. Pavlidis, in *Proceedings of European Microwave Conference*, Paris, 2000, pp. 1–4
- 6.2. K. Andersson, V. Desmaris, J. Eriksson, N. Roersman, H. Zirath, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 1303–1306
- 6.3. P. Asbeck, J. Mink, T. Itoh, G. Haddad, *Microw. J.* **42**, 22 (1999)
- 6.4. H. Ashoka, J. Ness, A. Robinson, M. Gourlay, J. Logan, P. Woodhead, D. Reuther, in *IEEE International Microwave Symposium Digest*, Baltimore, 1998, pp. 1149–1153
- 6.5. M. Aust, A. Sharma, Y. Chen, M. Wojtowicz, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 89–92
- 6.6. I. Bahl, in *International Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits*, Duisburg, 1994, pp. 71–91
- 6.7. A. Barnes, M. Moore, M. Allenson, in *IEEE International Microwave Symposium Digest*, Denver, 1997, pp. 1429–1432
- 6.8. W. Baumberger, *IEEE J. Solid-State Circuits* **29**, 1244 (1994)
- 6.9. A. Behtash, H. Tobler, F. Berlec, H. Leyer, V. Ziegler, B. Adelseck, T. Martin, R. Balmer, D. Pavlidis, R. Jansen, M. Neuburger, H. Schumacher, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1657–1660
- 6.10. F. Benkhelifa, R. Kiefer, S. Müller, F. van Raay, R. Quay, R. Sah, M. Mikulla, G. Weimann, in *Proceedings of International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.4
- 6.11. A. Bessemoulin, R. Quay, S. Ramberger, H. Massler, M. Schlechtweg, *IEEE J. Solid-State Circuits* **38**, 1433 (2003)
- 6.12. W. Bösch, J. Mayock, M. O’Keefe, J. McMonagle, in *IEEE International Radar Conference*, Arlington, 2005, pp. 22–26
- 6.13. H. Brech, W. Brakensiek, D. Burdeaux, W. Burger, C. Dragon, G. Formicone, B. Pryor, D. Rice, in *IEDM Technical Digest*, Washington DC, 2003, pp. 359–362
- 6.14. D. Bryant, K. Salzmann, R. Hudgens, in *IEEE International Microwave Symposium Digest*, Atlanta, 1993, pp. 1373–1376
- 6.15. J. Cha, J. Kim, B. Kim, J. Lee, S. Kim, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 533–536

- 6.16. S. Cha, Y. Chung, M. Wojtowicz, I. Smorchkova, B. Allen, J. Yang, R. Kagiwada, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 829–832
- 6.17. T. Chang, W. Wu, J. Lin, S. Jang, F. Ren, S. Pearton, R. Fitch, J. Gillespie, *Microw. Opt. Tech. Lett.* **49**, 1152 (2007)
- 6.18. Y. Chen, R. Coffie, W. Luo, M. Wojtowicz, I. Smorchkova, B. Heying, Y. Kim, M. Aust, A. Oki, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 307–310
- 6.19. Y. Chen, C. Wu, C. Pao, M. Cole, Z. Bardai, L. Hou, T. Midford, in *GaAs IC Symposium Technical Digest*, San Diego, 1995, pp. 281–284
- 6.20. H. Chireix, *Proc. IRE* **23**, 1370 (1935)
- 6.21. K. Cho, W. Kim, J. Kim, S. Stapleton, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1895–1899
- 6.22. J. Choi, J. Yim, J. Yang, J. Kim, J. Cha, B. Kim, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 81–84
- 6.23. Y. Chung, S. Cai, W. Lee, Y. Lin, C. Wen, K. Wang, T. Itoh, *Electron. Lett.* **37**, 1199 (2001)
- 6.24. Y. Chung, C. Hang, S. Cai, Y. Qian, C. Wen, K. Wang, T. Itoh, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 433–436
- 6.25. P. Colantonio, F. Giannini, R. Giofre, E. Limiti, A. Serino, M. Peroni, P. Romanini, C. Proietti, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 673–676
- 6.26. Compound Semiconductor, *Comp. Semicond.* **6**, 15 (2000)
- 6.27. J. Conlon, N. Zhang, M. Poulton, J. Shealy, R. Vetry, D. Green, J. Brown, S. Gibb, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 85–88
- 6.28. A. Couturier, S. Heckmann, V. Serru, T. Huet, P. Chaumas, J. Fontecave, M. Camiade, J.P. Viaud, S. Piotrowicz, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 813–816
- 6.29. S. Cripps, in *IEEE International Microwave Symposium Digest*, Boston, 1983, pp. 221–223
- 6.30. S. Cripps, *RF Power Amplifiers for Wireless Communications* (Artech House, Boston London, 1999)
- 6.31. A. Darwish, K. Boutros, B. Luo, B. Huebschman, E. Viveiros, H. Hung, *IEEE Trans. Microw. Theory Tech.* **54**, 4456 (2006)
- 6.32. D. Dawson, in *IMS Workshop WMG: Solid-State Power Invades the Tube Realm*, Honolulu, 2007
- 6.33. A. de Hek, P. Hunneman, M. Demmler, A. Hülsmann, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Munich, 1999, pp. 276–280
- 6.34. I. Dettmann, E. Chigaeva, L. Wu, M. Berroth, in *EEEfCOM Workshop*, Ulm, June 2005
- 6.35. M. Drinkwine, T. Winslow, D. Miller, D. Conway, B. Raymond, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 187–190
- 6.36. W. Eckl, B. Friedel, G. Fischer, H. Schenkel, in *IMS Workshop Advances in GaN-based Device and Circuit Technology: Modeling and Applications*, Fort Worth, 2004
- 6.37. M. Engels, R. Jansen, in *IEEE International Microwave Symposium Digest*, Atlanta, 1993, pp. 757–760

- 6.38. D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, J. Johnson, in *Proceedings of International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.3
- 6.39. H. Finlay, R. Jansen, J. Jenkins, I. Eddison, IEEE Trans. Microw. Theory Tech. **36**, 961 (1988)
- 6.40. G. Fischer, in *IEEE Wireless and Microwave Technology Conference*, Clearwater, 2004, p. FD-1
- 6.41. R. Freitag, H. Henry, E. Lee, M. Pingor, H. Salvo, 160 W MODAR Wind Shear Detection/Weather System. IEEE Trans. Microw. Theory Tech. **43**, 1703 (1995)
- 6.42. J. Gajadharsing, O. Bosma, P. van Westen, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 529–532
- 6.43. N.L. Gallou, J. Villemazet, B. Cogo, J. Cazaux, A. Mallet, L. Lapierre, in *Proceedings of European Microwave Conference*, Munich, 2003, pp. 273–276
- 6.44. S. Gao, S. Sanabria, H. Xu, S. Long, S. Heikman, U. Mishra, R. York, IEE Proc. Microw. Ant. Propag. **153**, 259 (2006)
- 6.45. S. Gao, H. Xu, S. Heikman, U. Mishra, R. York, in *Asia Pacific Microwave Conference*, Suzhou, 2005
- 6.46. S. Gao, H. Xu, S. Heikman, U. Mishra, R. York, IEEE Microw. Wireless Compon. Lett. **16**, 28 (2006)
- 6.47. S. Gao, H. Xu, U. Mishra, R. York, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 259–262
- 6.48. J. Gassmann, P. Watson, L. Kehias, G. Henry, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 615–618
- 6.49. E. Griffin, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 709–712
- 6.50. G. Soubercaze-Pun, J.G. Tartarin, L. Bary, J. Rayssac, E. Morvan, B. Grimbert, S. Delage, J. DeJaeger, J. Graffeuil, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 747–750
- 6.51. K. Gupta, R. Garg, I. Bahl, P. Bhartia, *Microstrip Lines and Slotlines*. (Artech House, Boston London, 1996)
- 6.52. U. Gustavsson, Master thesis, Orebro University, 2006
- 6.53. C. Hang, Y. Qian, T. Itoh, in *IEEE International Microwave Symposium Digest*, Phoenix, 2001, pp. 1079–1082
- 6.54. G. Hanington, P. Chen, P. Asbeck, L. Larson, IEEE Trans. Microw. Theory Tech. **47**, 1471 (1999)
- 6.55. W. Haydl, A. Tessmann, K. Züfle, H. Massler, T. Krems, L. Verwelen, J. Schneider, in *Proceedings of European Microwave Conference Prague*, 1996, pp. 996–1000
- 6.56. W. Heinrich, IEEE Trans. Microw. Theory Tech. **41**, 45 (1993)
- 6.57. M. Heins, J. Carroll, M. Kao, J. Delaney, C. Campbell, in *IEEE International Microwave Symposium Digest*, Forth Worth, 2004, pp. 149–152
- 6.58. S. Hong, Y. Woo, I. Kim, J. Kim, J. Moon, H. Kim, J. Lee, B. Kim, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1247–1250
- 6.59. S. Hsu, P. Valizadeh, D. Pavlidis, J. Moon, M. Micovic, D. Wong, T. Hussain, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 85–88
- 6.60. T. Hussain, A. Kurdoghlian, P. Hashimoto, W. Wong, M. Wetzel, J. Moon, L. McCray, M. Micovic, in *IEDM Technical Digest*, Washington DC, 2001, pp. 581–584

- 6.61. T. Hussain, M. Micovic, T. Tsien, M. Delaney, D. Chow, A. Schmitz, P. Hashimoto, D. Wong, J. Moon, M. Hu, J. Duvall, D. McLaughlin, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 25–27
- 6.62. A. Huttunen, R. Kaunisto, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1437–1440
- 6.63. A. Inoue, A. Ohta, S. Goto, T. Ishikawa, Y. Matsuda, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1947–1950
- 6.64. M. Iwamoto, A. Jayaraman, G. Hanington, P. Chen, A. Bellora, W. Thornton, L. Larson, P. Asbeck, Electron. Lett. **36**, 1010 (2000)
- 6.65. K. Iyomasa, K. Yamanaka, K. Mori, H. Noto, H. Ohtsuka, M.N.S. Yoneda, Y. Kamo, Y. Isota, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1255–1258
- 6.66. B. Jacobs, B. van Straaten, M. Kramer, F. Karouta, P. de Hek, E. Suijker, R. van Dijk, Proc. MRS **693**, 629 (2001)
- 6.67. A. Jayaraman, P. Chen, G. Hanington, L. Larson, P. Asbeck, IEEE Microw. Guided Wave Lett. **8**, 121 (1998)
- 6.68. A. John, R. Jansen, in *IEEE International Microwave Symposium Digest*, San Francisco, 1996, pp. 745–748
- 6.69. Y. Kamo, T. Kunii, H. Takeuchi, Y. Yamamoto, M. Totsuka, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, T. Oku, A. Inoue, T. Nanjo, H. Chiba, M. Suita, T. Oishi, Y. Abe, Y. Tsuyama, R. Shirahana, H. Ohtsuka, K. Iyomasa, K. Yamanaka, M. Hieda, M. Nakayama, T. Ishikawa, T. Takagi, K. Marumoto, Y. Matsuda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 495–498
- 6.70. K. Kong, B. Nguyen, S. Nayak, M. Kao, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 232–235
- 6.71. V. Kaper, R. Thompson, T. Prunty, J. Shealy, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1145–1148
- 6.72. V. Kaper, V. Tilak, H. Kim, R. Thompson, T. Prunty, J. Smart, L. Eastman, J. Shealy, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 251–254
- 6.73. O. Kappeler, R. Quay, F. van Raay, R. Kiefer, R. Reiner, H. Walcher, S. Müller, M. Mikulla, M. Schlechtweg, G. Weimann, D. Wiegner, U. Seyfried, W. Templ, in *IEDM Technical Digest*, Washington DC, 2005, pp. 385–386
- 6.74. A. Katz, M. Kubak, G. DeSalvo, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1364–1367
- 6.75. A. Kawano, N. Adachi, Y. Tateno, S. Mizuno, N. Ui, J. Nikaido, S. Sano, in *Asia Pacific Microwave Conference*, Suzhou, 2005
- 6.76. D. Keogh, J. Li, A. Conway, D. Qiao, S. Raychaudhuri, P. Asbeck, Int. J. High Speed Electron. Systems **14**, 831 (2004)
- 6.77. L. Khan, Proc. IRE **40**, 803 (1952)
- 6.78. T. Kikkawa, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 17–20
- 6.79. D. Kimball, P. Draxler, J. Jeong, C. Hsia, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, P. Asbeck, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 89–92
- 6.80. D. Kimball, J. Jeong, C. Hsia, P. Draxler, P. Asbeck, D. Choi, W. Pribble, R. Pengelly, in *IEEE Radio and Wireless Symposium*, San Diego, 2006, pp. n.a.

- 6.81. H. Klockenhoff, R. Behtash, J. Würfl, W. Heinrich, G. Tränkle, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1846–1849
- 6.82. K. Kobayashi, Y.C. Chen, I. Smorchkova, R. Tsai, M. Wojtowicz, A. Oki, in *Radio Frequency Integrated Circuit Symposium Digest*, Honolulu, 2007, pp. 585–588
- 6.83. K. Kobayashi, Y. Chen, I. Smorchkova, R. Tsai, M. Wojtowicz, A. Oki, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 619–622
- 6.84. J. Komiak, W. Kong, P. Chao, K. Nicols, in *GaAs IC Symposium Technical Digest*, Orlando, 1996, pp. 111–114
- 6.85. J. Komiak, W. Kong, K. Nicols, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 905–907
- 6.86. D. Krausse, R. Quay, R. Kiefer, A. Tessmann, H. Massler, A. Leuther, T. Merkle, S. Müller, C. Schwörer, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 71–74
- 6.87. K. Krishnamurthy, S. Keller, U. Mishra, M. Rodwell, S. Long, in *GaAs IC Symposium Technical Digest*, Seattle, 2000, pp. 33–36
- 6.88. B. Kruger, in *IEEE International Radar Conference*, Annapolis, 1998, pp. 227–232
- 6.89. P. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs* (Artech House, Boston London, 1989)
- 6.90. A. Lan, M. Wojtowicz, I. Smorchkova, R. Coffie, R. Tsai, B. Heying, M. Truong, F. Fong, M. Kintis, C. Namba, A. Oki, T. Wong, *IEEE Microw. Wireless Compon. Lett.* **16**, 425 (2006)
- 6.91. L. Larson, P. Asbeck, D. Kimball, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 1–4
- 6.92. J. Lee, L. Eastman, K. Webb, *IEEE Trans. Microw. Theory Tech.* **51**, 2243 (2003)
- 6.93. S. Lee, B. Green, K. Chu, K. Webb, L. Eastman, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 549–552
- 6.94. S. Lee, B. Cetiner, H. Torpi, S. Cai, J. Li, K. Alt, Y. Chen, C. Wen, K. Wang, T. Itoh, *IEEE Trans. Electron Devices* **48**, 495 (2001)
- 6.95. Y.S. Lee, Y.H. Jeong, *IEEE Microw. Wireless Compon. Lett.* **17**, 622 (2007)
- 6.96. J. Lees, J. Benedikt, K. Hilton, J. Powell, R. Balmer, M. Uren, T. Martin, P. Tasker, *Electron. Lett.* **41**, 1284 (2005)
- 6.97. B. Levush, in *IMS Workshop WMG: Solid-State Power Invades the Tube Realm*, Honolulu, 2007
- 6.98. C. Lin, H. Liu, C. Chu, H. Huang, Y. Wang, C. Liu, C. Chang, C. Wu, C. Chang, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 165–168
- 6.99. G. Ma, Q. Chen, O. Tornblad, T. Wei, C. Ahrens, R. Gerlach, in *IEDM Technical Digest*, Washington DC, 2005, pp. 361–364
- 6.100. A. Maekawa, T. Yamamoto, E. Mitani, S. Sano, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 722–725
- 6.101. L. Maloratsky, *Microwave & RF* **39**, 79 (2000)
- 6.102. E. Martinez, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 7–10

- 6.103. J. Martins, P. Cabral, N. Carvalho, J. Pedro, IEEE Trans. Microw. Theory Tech. **54**, 4432 (2006)
- 6.104. P. McGovern, D. Williams, P. Tasker, J. Benedikt, J. Powell, K. Hilton, R. Balmer, T. Martin, M. Uren, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 825–828
- 6.105. D. Meharry, R. Lendner, K. Chu, L.G.K. Beech, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 631–634
- 6.106. M. Micovic, A. Kurdoghlian, P. Hashimoto, M. Hu, M. Antcliffe, P. Willadsen, W. Wong, R. Bowen, I. Milosavljevic, A. Schmitz, M. Wetzel, D. Chow, in *IEDM Technical Digest*, San Francisco, 2006, pp. 425–428
- 6.107. M. Micovic, A. Kurdoghlian, A. Janke, P. Hashimoto, P. Wong, D. Moon, J. McCray, C. Nguyen, IEEE Trans. Electron Devices **48**, 591 (2001)
- 6.108. E. Mitani, in *IMS Workshop WSG: Solid-State Power Invades the Tube Realm*, Honolulu, 2007
- 6.109. E. Mitani, H. Haematsu, S. Yokogawa, J. Nikaido, Y. Tateno, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 183–186
- 6.110. W. Nagy, J. Brown, R. Borges, S. Singhal, IEEE Trans. Microw. Theory Tech. **51**, 660 (2003)
- 6.111. Y. Nanishi, H. Miyamoto, A. Suzuki, H. Okumura, N. Shibata, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 45–48
- 6.112. R. Negra, T. Chu, M. Helaoui, S. Boumaizs, G. Hegazi, F. Ghannouchi, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 795–798
- 6.113. M. Neuburger, M. Kunze, I. Daumiller, T. Zimmermann, A. Dadgar, A. Krost, S. Hettich, F. Gruson, H. Schumacher, E. Kohn, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 111–114
- 6.114. M. Neuburger, M. Kunze, I. Daumiller, T. Zimmermann, A. Dadgar, A. Krost, S. Hettich, F. Gruson, H. Schumacher, E. Kohn, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 225–228
- 6.115. C. Nguyen, M. Micovic, D. Wong, A. Kurdoghlian, P. Hashimoto, P. Janke, L. McCray, J. Moon, in *GaAs IC Symposium Technical Digest*, Seattle, 2000, pp. 11–14
- 6.116. M. Nishijima, T. Murata, Y. Hirose, M. Hikita, N. Negoro, H. Sakai, Y. Uemoto, K. Inoue, T. Tanaka, D. Ueda, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 299–302
- 6.117. T. Ogawa, T. Iwasaki, H. Maruyama, K. Horiguchi, M. Nakayama, Y. Ikeda, H. Kurebayashi, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 537–540
- 6.118. M. Ohtomo, IEEE Trans. Microw. Theory Tech. **41**(6–7), 495 (1993)
- 6.119. Y. Okamoto, A. Wakejima, K. Matsunaga, Y. Ando, T. Nakayama, K. Kasahara, K. Ota, Y. Murase, K. Yamanoguchi, T. Inoue, H. Miyamoto, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 491–494
- 6.120. V. Paidi, S. Xie, R. Coffie, B. Moran, S. Heikman, S. Keller, A. Chini, S. DenBaars, U. Mishra, S. Long, M. Rodwell, IEEE Trans. Microw. Theory Tech. **51**, 643 (2003)

- 6.121. J. Palmour, S. Sheppard, R. Smith, S. Allen, W. Pribble, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IEDM Technical Digest*, Washington DC, 2001, pp. 385–388
- 6.122. R. Pantocha, IEEE Trans. Microw. Theory Tech. **37**, 1675 (1989)
- 6.123. P. Parikh, Y. Wu, M. Moore, P. Chavarkar, U. Mishra, B. Neidhard, L. Kehias, T. Jenkins, in *Lester Eastman Conference High Performance Devices*, Newark, 2002, pp. 56–57
- 6.124. R. Pengelly, in *Proceedings of Wireless and Microwave Technology Conference*, Clearwater, 2004, pp. RC-5
- 6.125. P. Piel, M. Miller, B. Green, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1363–1366
- 6.126. S. Piotrowicz, E. Chartier, J. Jaquet, D. Floriot, J. Coupat, C. Framery, P. Eudeline, P. Auxemery, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1527–1530
- 6.127. G. Ponchak, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Munich, 1999, pp. 414–417
- 6.128. G. Ponchak, Z. Schwartz, S. Alterovitz, A. Downey, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 41–44
- 6.129. M.J. Poulton, W. Leverich, J. Shealy, R. Vetry, J. Brown, D. Green, S. Gibb, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1327–1330
- 6.130. W. Pribble, J. Palmour, S. Sheppard, R. Smith, S. Allen, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1819–1822
- 6.131. T. Quach, R. Fitch, J. Gillespie, T. Jenkins, R. Neidhard, E. Nykiel, G. Via, P. Watson, J. Wiedemann, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 103–106
- 6.132. R. Quay, R. Kiefer, F. van Raay, H. Massler, S. Ramberger, S. Müller, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, in *IEDM Technical Digest*, San Francisco, 2002, pp. 673–676
- 6.133. R. Quay, F. van Raay, A. Tessmann, R. Kiefer, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings WOCSDICE*, Venice, 2007, pp. 349–352
- 6.134. F. Raab, IEEE Trans. Microw. Theory Tech. **45**, 2007 (1997)
- 6.135. F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, N. Sokal, IEEE Trans. Microw. Theory Tech. **50**, 814 (2002)
- 6.136. F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, N. Sokal, High Freq. Electron. **2**, 22 (2003)
- 6.137. V. Radisic, C. Pobanz, H. Ming, M. Micovic, M. Wetzel, P. Janke, M. Yu, C. Ngo, D. Dawson, M. Matloubian, in *Radio Frequency Integrated Circuits Symposium Digest*, Boston, 2000, pp. 43–46
- 6.138. M. Riaziat, R. Majidi-Ahy, I. Feng, IEEE Trans. Microw. Theory Tech. **38**, 245 (1990)
- 6.139. M. Rosker, H. Dietrich, C. Bozada, A. Hung, G. Via, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 41–45
- 6.140. M. Rosker, in *IEEE RF IC Symposium Digest*, Honolulu, 2007, pp. 159–162
- 6.141. A. Royet, B. Cabon, O. Rozeau, T. Ouisse, T. Billon, IEE Proc. Microw. Ant. Propag., **149**, 253 (2002)

- 6.142. M. Rudolph, R. Behtash, K. Hirche, J. Würfl, W. Heinrich, G. Tränkle, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1899–1902
- 6.143. C. Sanabria, X. Hongtao, S. Heikman, U. Mishra, R. York, IEEE Microw. Wireless Compon. Lett. **15**, 463 (2005)
- 6.144. H. Sano, K. Otobe, Y. Tateno, N. Adachi, S. Mizuno, A. Kawano, J. Nikaido, S. Sano, in *Asia Pacific Microwave Conference*, Suzhou, 2005
- 6.145. M. Schlechtweg, W. Haydl, A. Bangert, J. Braunstein, P. Tasker, L. Verweyen, H. Massler, W. Bronner, A. Hülsmann, K. Köhler, IEEE J. Solid-State Circuits **31**, 1426 (1996)
- 6.146. D. Schmelzer, S. Long, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 96–99
- 6.147. C. Schöllhorn, W. Zhao, M. Morschbach, E. Kasper, IEEE Trans. Electron Devices **50**, 740 (2003)
- 6.148. P. Schuh, R. Leberer, H. Sledzik, M. Oppermann, B. Adelseck, H. Brugger, R. Behtash, H. Leier, R. Quay, R. Kiefer, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 726–729
- 6.149. P. Schuh, R. Leberer, H. Sledzik, M. Oppermann, B. Adelseck, H. Brugger, R. Quay, M. Mikulla, G. Weimann, in *Proceedings of European Microwave Integrated Circuits Conference*, Manchester, 2006, pp. 241–244
- 6.150. P. Schuh, R. Leberer, H. Sledzik, D. Schmidt, M. Oppermann, B. Adelseck, H. Brugger, R. Quay, F. van Raay, M. Seelmann-Eggebert, R. Kiefer, W. Bronner, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1324–1327
- 6.151. R. Schwindt, V. Kumar, O. Aktas, J. Lee, I. Adesida, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 201–203
- 6.152. K. Seemann, S. Ramberger, A. Tessmann, R. Quay, J. Schneider, M. Riessle, H. Walcher, M. Kuri, R. Kiefer, M. Schlechtweg, in *Proceedings of European Microwave Conference*, Munich, 2003, pp. 383–386
- 6.153. S. Sheppard, B. Pribble, R. Smith, A. Saxler, S. Allen, J. Milligan, R. Pengelly, in *Proceedings of International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 175–178
- 6.154. S. Sheppard, W. Pribble, D. Emerson, Z. Ring, R. Smith, S. Allen, J. Palmour, in *Device Research Conference*, Denver, 2000, pp. 37–38
- 6.155. H. Shimawaki, H. Miyamoto, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 377–380
- 6.156. K. Shiojima, T. Makimura, T. Kosugi, T. Suemitsu, N. Shigekawa, M. Hiroki, H. Yokoyama, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1331–1334
- 6.157. K. Shiojima, T. Makimura, T. Kosugi, S. Sugitani, N. Shigekawa, H. Ishikawa, T. Egawa, Electron. Lett. **40**, 775 (2004)
- 6.158. D. Snider, IEEE Trans. Electron Devices **14**, 851 (1967)
- 6.159. M. Südow, K. Andersson, N. Billström, J. Grahn, H. Hjelmgren, J. Nilsson, P. Nilsson, J. Stahl, H. Zirath, N. Rorsman, IEEE Trans. Microw. Theory Tech. **54**, 4072 (2006)
- 6.160. Y. Takada, H. Sakurai, K. Matsushita, K. Masuda, S. Takatsuka, M. Kuraguchi, T. Suzuki, M. Hirose, H. Kawasaki, K. Takagi, K. Tsuda, IEICE Tech. Rep. **105**, 39 (2005)

- 6.161. K. Takagi, K. Masuda, Y. Kashiwabara, H. Sakurai, K. Matsushita, S. Takatsuka, H. Kawasaki, Y. Takada, K. Tsuda, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 265–268
- 6.162. T. Takagi, M. Mochizuki, Y. Tarui, Y. Itoh, S. Tsuji, Y. Mitsui, IEICE Trans. Electron. **E78-C**, 936 (1995)
- 6.163. R. Therrien, A. Chaudhari, S. Singhal, C. Snow, A. Edwards, C. Park, W. Nagy, J. Johnson, A. Hanson, K. Linticum, I. Kizilyalli, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 635–638
- 6.164. R. Therrien, W. Nagy, I. Kizilyalli, RF Design, 27 (2007)
- 6.165. N. Ui, H. Sano, S. Sano, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1259–1262
- 6.166. N. Ui, S. Sano, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 718–721
- 6.167. F. van den Bogaart, A. de Hek, in *IEE Tutorial Colloquium on Design of RFICs and MMICs*, London, 1997, pp. 8/1–8/6
- 6.168. M. van Heiningen, F. van Vliet, R. Quay, F. van Raay, M. Seelmann-Eggebert, in *Proceedings of European Microwave Integrated Circuits Conference*, Manchester, 2006, pp. 75–78
- 6.169. F. van Raay, R. Quay, R. Kiefer, F. Benkhelifa, B. Raynor, W. Pletschen, M. Kuri, H. Massler, S. Müller, M. Dammann, M. Mikulla, M. Schlechtweg, G. Weimann, IEEE Microw. Wireless Compon. Lett. **15**, 460 (2005)
- 6.170. F. van Raay, R. Quay, R. Kiefer, W. Bronner, M. Seelmann-Eggebert, M. Schlechtweg, M. Mikulla, G. Weimann, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1368–1371
- 6.171. F. van Raay, R. Quay, R. Kiefer, W. Fehrenbach, W. Bronner, M. Kuri, F. Benkhelifa, H. Massler, S. Müller, M. Mikulla, M. Schlechtweg, G. Weimann, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 233–236
- 6.172. F. van Rijs, S. Theeuwen, in *IEDM Technical Digest*, San Francisco, 2006, pp. 205–208
- 6.173. B. Vassilakis, A. Cova, in *Asia Pacific Microwave Conference*, Suzhou, 2005
- 6.174. B. Vassilakis, A. Cova, W. Veitschegger, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 3–7
- 6.175. N. Vellas, C. Gaquiere, Y. Guhel, M. Werquin, F. Bue, R. Aubry, S. Delage, F. Semond, J. Jaeger, IEEE Electron Device Lett. **23**, 461 (2002)
- 6.176. G. Vendelin, *Design of Amplifiers and Oscillators by the S-Parameter Method* (Wiley, New York, 1982)
- 6.177. R. Vetry, J. Shealy, D. Green, J. McKenna, J. Brown, S. Gibb, K. Leverich, P. Garber, M. Poulton, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 714–717
- 6.178. J. Vincent, D. van der Merve, in *IEEE AFRICON*, Stellenbosch, 1996, pp. 749–752
- 6.179. A. Wakejima, T. Asano, T. Hirano, M. Funabashi, K. Matsunaga, IEEE J. Solid-State Circuits **40**, 2054 (2005)
- 6.180. A. Wakejima, K. Matsunaga, Y. Okamoto, Y. Ando, T. Nakayama, H. Miyamoto, Electron. Lett. **41**, 1371 (2005)
- 6.181. A. Wakejima, K. Matsunaga, Y. Okamoto, K. Ota, Y. Ando, T. Nakayama, H. Miyamoto, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1360–1363

- 6.182. F. Wang, A. Yang, D. Kimball, K. Larson, P. Asbeck, IEEE Trans. Microw. Theory Tech. **53**, 1244 (2005)
- 6.183. R. Wang, M. Cole, in *GaAs IC Symposium Technical Digest*, Orlando, 1996, pp. 111–114
- 6.184. M. Werquin, C. Gaquiere, Y. Gubel, N. Vellas, D. Theron, B. Boudart, V. Hoel, M. Germain, J.D. Jaeger, S. Delage, Electron. Lett. **41**, 46 (2005)
- 6.185. P. White, T. O'Leary, in *GaAs IC Symposium Technical Digest*, San Diego, 1995, pp. 277–280
- 6.186. W. Wu, B. Thibeault, J. Xu, R. York, S. Keller, B. Keller, U. Mishra, in *Device Research Conference*, Santa Barbara, 1999, pp. 50–51
- 6.187. Y. Wu, P. Charvarkar, M. Moore, P. Parikh, B. Keller, U. Mishra, in *IEDM Technical Digest*, San Francisco, 2000, pp. 375–376
- 6.188. Y. Wu, D. Kapolnek, J. Ibbetson, P. Parikh, B. Keller, U. Mishra, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 963–965
- 6.189. Y. Wu, M. Moore, A. Saxler, T. Wisleder, P. Parikh, in *Device Research Conference*, State College, PA, 2006, pp. 151–152
- 6.190. Y. Wu, A. Chin, K.H. Shih, C.C. Wu, C. Liao, S. Pai, C. Chi, IEEE Electron Device Lett. **21**, 442 (2000)
- 6.191. S. Xie, V. Paidi, R.C.A. Heikman, B. Moran, A. Chini, S. DenBaars, U. Mishra, S. Long, M. Rodwell, IEEE Microw. Wireless Compon. Lett. **13**, 284 (2003)
- 6.192. S. Xie, V. Paidi, S. Heikman, L. Shen, A. Chini, U. Mishra, M. Rodwell, S. Long, Int. J. High Speed Electron. Systems **14**, 847 (2004)
- 6.193. H. Xu, S. Sanabria, N. Pervez, S. Keller, U. Mishra, R. York, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2002, pp. 1509–1512
- 6.194. H. Xu, S. Sanabria, N. Pervez, S. Keller, U. Mishra, R. York, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1345–1348
- 6.195. J. Xu, S. Keller, G. Parish, S. Heikman, U. Mishra, R. York, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 959–962
- 6.196. S. Xu, K. Gan, G. Samudra, Y. Liang, J. Sin, IEEE Trans. Electron Devices **47**, 1980 (2000)
- 6.197. T. Yamamoto, T. Kitahara, S. Hiura, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1263–1266
- 6.198. T. Yamamoto, E. Mitani, K. Inoue, M. Nishi, S. Sano, in *Proceedings of the European Microwave Integrated Circuits Conference* Munich, 2007, pp. 173–176
- 6.199. K. Yamanaka, K. Iyomasa, H. Ohtsuka, M. Nakayama, Y. Tsuyama, T. Kunii, Y. Kamo, T. Takagi, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 241–244
- 6.200. K. Yamanaka, K. Mori, K. Iyomasa, H. Ohtsuka, M. Nakayama, Y. Kamo, Y. Isota, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 1251–1254
- 6.201. M. Yu, M. Matloubian, P. Petre, L.R. Hamilton, R. Bowen, M. Lui, H. Sun, C. Ngo, P. Janke, D. Baker, R. Robertson, IEEE J. Solid-State Circuits **34**, 1212 (1999)
- 6.202. J. Zolper, Wide Bandgap Semiconductor RF Electronics Technology, MTO Industry Briefing, Sept. 2001,
<http://www.compoundsemiconductor.net/cws/article/magazine/11332>

References of Chapter 7

- 7.1. N. Adachi, Y. Tateno, S. Mizuno, A. Kawano, J. Nikaido, S. Sano, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 507–510
- 7.2. M. Adlerstein, J. Gering, IEEE Trans. Electron Devices **47**, 434 (2000)
- 7.3. M. Akita, S. Kishimoto, T. Mizutani, IEEE Electron Device Lett. **22**, 376 (2001)
- 7.4. O. Aktas, A. Kuliev, V. Kumar, R. Schwindt, S. Toshkov, D. Costescu, J. Stubbins, I. Adesida, Solid-State Electron. **48**, 471 (2004)
- 7.5. N. Ashcroft, N. Mermin, *Solid-State Physics* (Saunders College, Fort Worth, 1976)
- 7.6. A. Barnes, A. Boetti, L. Marchand, J. Hopkins, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 5–12
- 7.7. J. Bernat, M. Wolter, P. Javorka, A. Fox, M. Marso, P. Kordos, Solid-State Electron. **48**, 1825 (2004)
- 7.8. R. Blanchard, A. Cornet, J. del Alamo, IEEE Electron Device Lett. **21**, 424 (2001)
- 7.9. R. Blanchard, M. Sommerville, J.D. Alamo, K. Duh, P. Chao, IEEE Trans. Electron Devices **47**, 1560 (2000)
- 7.10. J.D. Blauwe, D. Wellekens, G. Groeseneken, L. Haspeslagh, J.V. Houdt, L. Deferm, H. Maes, IEEE Trans. Electron Devices **45**, 2466 (1998)
- 7.11. M. Borgarino, R. Menozzi, Y. Baeyens, P. Cova, F. Fantini, IEEE Trans. Electron Devices **45**, 366 (1998)
- 7.12. K. Boutros, W. Luo, B. Brar, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2006, pp. n.a.
- 7.13. K. Boutros, P. Rowell, B. Brar, in *Proceedings of the International Reliability Physics Symposium*, Phoenix, 2004, pp. 577–578
- 7.14. N. Bovolon, R. Schultheis, J. Müller, P. Zwicknagl, E. Zanoni, IEEE Electron Device Lett. **19**, 469 (1998)
- 7.15. N. Braga, R. Mickevicius, V. Rao, W. Fichtner, R. Gaska, M. Shur, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 149–152
- 7.16. H. Brech, W. Brakensiek, D. Burdeaux, W. Burger, C. Dragon, G. Formicone, B. Pryor, D. Rice, in *IEDM Technical Digest*, Washington DC, 2003, pp. 359–362

- 7.17. J. Brown, S. Lee, D. Lieu, J. Martin, R. Vetry, M. Poulton, J. Shealy, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 303–306
- 7.18. S. Cai, Y. Tang, R. Li, Y. Wei, L. Wong, Y. Chen, K. Wang, M. Chen, Y. Zhao, R. Schrimpf, J. Keay, K. Galloway, IEEE Trans. Electron Devices **47**, 304 (2000)
- 7.19. C. Canali, F. Magistral, M. Sangalli, C. Tedesco, E. Zanoni, G. Castellaneta, F. Marchetti, in *Proceedings of the International Reliability Physics Symposium*, Cardiff, 1991, pp. 206–213
- 7.20. P. Cappelletti, R. Bez, A. Modelli, A. Visconti, in *IEDM Technical Digest*, San Francisco, 2004, pp. 489–492
- 7.21. P. Chao, W. Hu, H. DeOrio, A. Swanson, W. Hoffmann, W. Taft, IEEE Electron Device Lett. **18**, 441 (1997)
- 7.22. H. Chiu, T. Yeh, S. Yang, M. Hwu, Y. Chan, IEEE Trans. Electron Devices **50**, 1532 (2003)
- 7.23. Y. Chou, D. Leung, R. Lai, R. Grundbacher, M. Barsky, Q. Kan, R. Tsai, M. Wojtowicz, D. Eng, L. Tran, T. Block, P. Liu, M. Nishimoto, A. Oki, IEEE Trans. Electron Devices **24**, 378 (2003)
- 7.24. Y. Chou, D. Leung, I. Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo, Q. Kan, R. Lai, P. Liu, D. Eng, A. Oki, Microelectron. Reliab. **44**, 1033 (2004)
- 7.25. A. Christou, P. Tang, J.M. Hu, IEEE Trans. Electron Devices **39**, 2229 (1992)
- 7.26. K. Chu, P. Chao, M. Pizzella, R. Actis, D. Meharry, K. Nichols, R. Vaudo, X. Xu, J. Flynn, J. Dion, G. Brandes, IEEE Electron Device Lett. **25**, 596 (2004)
- 7.27. R. Coffie, Y. Chen, P. Smorchkova, Y.C. Chou, M. Wojtowicz, A. Oki, in *Proceedings International Reliability Physics Symp.*, San Jose, 2006, pp 99–102
- 7.28. R. Coffie, Y. Chen, P. Smorchkova, B. Heying, W. Sutton, Y.C. Chou, W.B. Luo, M. Wojtowicz, A. Oki, in *Proceedings International Reliability Physics Symp.*, Phoenix, 2007, pp 568–571
- 7.29. A. Conway, M. Chen, P. Hashimoto, P. Willadsen, M. Micovic, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 99–102
- 7.30. J. Cooper Jr., M. Melloch, R. Singh, A. Agarwal, J. Palmour, IEEE Trans. Electron Devices **49**, 658 (2002)
- 7.31. A. Dabiran, A. Osinsky, P. Chow, R. Fitch, J. Gillespie, N. Moser, T. Jenkins, J. Sewell, D. Via, A. Crespo, J. LaRoche, F. Ren, S. Pearton, in *Proceedings of High Temperature Electronics Conference*, Santa Fe, 2006, pp. 329–333
- 7.32. M. Dammann, A. Leuther, R. Quay, M. Meng, H. Konstanzer, W. Jantz, M. Mikulla, Microelectron. Reliab. **44**, 939 (2004)
- 7.33. M. Dammann, Personal Communication, 2007
- 7.34. A.M. Darwish, A. Bayba, H. Hung, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 311–314
- 7.35. A. Darwish, B. Hübschman, R.D. Rosario, E. Viveiros, H. Hung, in *Compound Semiconductor IC Symposium Technical Digest*, Palm Springs, 2005, pp. 145–148
- 7.36. I. Daumiller, C. Kirchner, M. Kamp, K. Ebeling, E. Kohn, IEEE Electron Device Lett. **20**, 448 (1999)
- 7.37. P. de Jong, G. Meijer, A. van Roermund, IEEE J. Solid-State Circuits **33**, 1999 (1998)

- 7.38. J. del Alamo, A. Villanueva, in *IEDM Technical Digest*, San Francisco, 2004, pp. 1019–1022
- 7.39. M. die Forte-Poisson, S. Delage, S. Cassette, Mater. Sci. Semicond. Process. **4**, 503 (2001)
- 7.40. D. Dieci, G. Sozzi, R. Menozzi, E. Tediosi, C. Lanzieri, C. Canali, IEEE Trans. Electron Devices **48**, 1929 (2001)
- 7.41. D. DiSanto, C. Bolognesi, Electron. Lett. **41**, 503 (2005)
- 7.42. Y. Dora, A. Chakraborty, S. Heikman, L. McCarthy, S. Keller, S. DenBaars, U. Mishra, IEEE Electron Device Lett. **7**, 529 (2006)
- 7.43. D. Dumka, C. Lee, H. Tserng, P. Saunier, Electron. Lett. **40**, 1554 (2004)
- 7.44. R. Esfandiari, T. O'Neill, T. Lin, R. Kono, IEEE Trans. Electron Devices **37**, 1174 (1990)
- 7.45. M. Faqir, A. Chini, G. Verzellesi, F. Fantini, F. Rampazzo, G. Meneghesso, E. Zanoni, J. Bernat, P. Kordos, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2007, pp. 25–31
- 7.46. M. Fresina, M. Logue, J. Fendrich, T. Rogers, in *Proceedings of the International Symposium on GaAs and Related Compounds*, Baltimore, 2001, pp. 203–222
- 7.47. R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. Khan, M. Shur, IEEE Electron Device Lett. **18**, 494 (1997)
- 7.48. A. Geissberger, M. Fresina, L. Kapitan, C. Baratt, K. Tan, M. Hoppe, D. Streit, T. Block, M. Lammert, A. Oki, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 1999, p. 5.7
- 7.49. D. Gogl, H. Fiedler, M. Spitz, B. Parmentier,
- 7.50. S. Goodmann, F. Auret, F. Koschnick, J. Spaeth, B. Beaumont, P. Gibart, MRS Internet J. Nitride Semicond. Res. **4S1**, G6.12 (1999)
- 7.51. D. Green, S. Gibb, B. Hosse, R. Vetary, D. Grider, J. Smart, J. Cryst. Growth **272**, 285 (2004)
- 7.52. C. Hatfield, G. Bilbro, S. Allen, J.W. Palmour,
- 7.53. S. Heikman, S. Keller, S. DenBaars, U. Mishra, Appl. Phys. Lett. **81**, 439 (2002)
- 7.54. J. Hilsenbeck, E. Neubauer, J. Würfl, G. Tränkle, H. Obloh, Electron. Lett. **36**, 980 (2000)
- 7.55. T. Hisaka, Y. Nogami, H. Sasaki, A. Hasuike, N. Yoschida, K. Hayashi, T. Sonoda, A. Villanueva, J. del Alamo, in *GaAs IC Symposium Technical Digest*, San Diego, 2003, pp. 67–70
- 7.56. S. Hsu, P. Valizadeh, D. Pavlidis, in *GaAs IC Symposium Technical Digest*, Monterey, 2002, pp. 85–88
- 7.57. A. Immorlica, in *IMS Workshop WFI: GaN Device and Circuit Reliability*, Honolulu, 2007
- 7.58. Y. Inoue, S. Masuda, M. Kanamura, T. Ohki, K. Makiyama, N. Okamoto, K. Imanishi, T. Kikkawa, N. Hara, H. Shigematsu, K. Joshin, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 639–642
- 7.59. JEDEC, *Guidelines for GaAs MMIC and FET Life Testing* (Electronic Industries Association, Washington DC, 1993), JEP118
- 7.60. J. Jimenez, U. Chowdhury, M. Kao, A. Balistreri, C. Lee, P. Saunier, P. Chao, W. Hu, K. Chu, A. Immorlica, J. del Alamo, J. Joh, M. Shur, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2006, pp. n.a.
- 7.61. J. Joh, J. del Alamo, in *IEDM Technical Digest*, San Francisco, 2006, pp. 415–418

- 7.62. J. Joh, L. Xia, J.A. del Alamo, in *IEDM Technical Digest*, Washington DC, 2007, pp. 385–388
- 7.63. J. Johnson, J. Gao, K. Lucht, J. Williamson, C. Strautin, J. Riddle, R. Therrien, P. Rajagopal, J. Roberts, A. Vescan, J. Brown, A. Hanson, S. Singhal, R. Borges, E. Piner, K. Linthicum, Proc. Electrochem. Soc. **7**, 405 (2004)
- 7.64. A. Jordan, Microelectron. Reliab. **18**, 267 (1978)
- 7.65. D. Keogh, P. Asbeck, T. Chung, J. Limb, D. Yoo, J. Ryou, W. Lee, W. Lee, S. Chen, R. Dupuis, Electron. Lett. **42**, 661 (2006)
- 7.66. S. Khanna, J. Webb, A. Houdayer, C. Carloni, IEEE Trans. Nucl. Sci. **47**, 2322 (2000)
- 7.67. T. Kikkawa, K. Imanishi, M. Kanamura, K. Joshin, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, San Diego, 2002, pp. 171–174
- 7.68. T. Kikkawa, M. Kanamura, T. Ohki, K. Imanishi, K. Makiyama, N. Okamoto, N. Hara, K. Joshin, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 91–94
- 7.69. T. Kikkawa, T. Maniwa, H. Hayashi, M. Kanamura, S. Yokokawa, M. Nishi, N. Adachi, M. Yokoyama, Y. Tateno, K. Joshin, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1347–1350
- 7.70. H. Kim, V. Tilak, B. Green, H. Cha, J. Smart, J. Shealy, L. Eastman, in *Proceedings of the International Reliability Physics Symposium*, Nara, 2001, pp. 214–218
- 7.71. G. Koley, H. Kim, L. Eastman, M. Spencer, Electron. Lett. **39**, 1217 (2003)
- 7.72. B. Kopp, T. Axness, C. Moore, in *IEEE International Microwave Symposium Digest*, Denver, 1997, pp. 583–586
- 7.73. T. Kunii, M. Totsuka, Y. Kamo, Y. Yamamoto, H. Takeuchi, Y. Shimada, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, S. Nakatsuka, A. Inoue, T. Oku, T. Nanjo, T. Oishi, T. Ishikawa, Y. Matsuda, IEEE JEDEC, 137 (2003)
- 7.74. T. Kunii, M. Totsuka, Y. Kamo, Y. Yamamoto, H. Takeuchi, Y. Shimada, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, S. Nakatsuka, A. Inoue, T. Oku, T. Nanjo, T. Oishi, T. Ishikawa, Y. Matsuda, in *Compound Semiconductor IC Symposium Technical Digest*, Monterey, 2004, pp. 197–200
- 7.75. K. Kurishima, S. Yamahata, H. Nakajima, H. Ito, N. Watanabe, IEEE Electron Device Lett. **19**, 303 (1998)
- 7.76. J. Kuzmik, D. Pogany, E. Gornik, P. Javorka, P. Kordos, Solid-State Electron. **48**, 271 (2004)
- 7.77. C. Lee, H. Tserng, L. Witkowski, P. Saunier, S. Guo, B. Albert, R. Birkhan, G. Munns, Electron. Lett. **40**, 1547 (2004)
- 7.78. C. Lee, L. Witkowski, M. Muir, H. Tserng, P. Saunier, H. Wang, J. Yang, M. Khan, in *Proceedings of IEEE Lester Eastman Conference on High Performance Devices*, Newark, 2002, pp. 436–442
- 7.79. C. Lee, L. Wittkowski, H. Tserng, P. Saunier, R. Birkhahn, D. Olson, D. Olson, G. Munns, S. Guo, B. Albert, Electron. Lett. **41**, 155 (2005)
- 7.80. M. Levinstein, S. Rumyantsev, M. Shur (eds.), *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe* (Wiley, New York, 2001)
- 7.81. C. Li, J. Duster, K.T. Kornegay, IEEE Electron Device Lett. **24**, 72 (2003)
- 7.82. W. Liu, IEEE Trans. Electron Devices **43**, 220 (1996)
- 7.83. D. Look, Phys. Stat. Sol. B **228**, 293 (2001)
- 7.84. P. Maaskant, M. Akhter, J. Lambkin, L. Considine, IEEE Trans. Electron Devices **48**, 1822 (2001)

- 7.85. K. Matsushita, S. Teramoto, H. Sakurai, Y. Takada, J. Shim, H. Kawasaki, K. Tsuda, K. Takagi, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 87–90
- 7.86. G. Meneghesso, E.D. Bortoli, A. Paccagnella, E. Zanoni, C. Canali, IEEE Electron Device Lett. **16**, 336 (1995)
- 7.87. G. Meneghesso, T. Grave, M. Manfredi, M. Pavesi, C. Canali, E. Zanoni, IEEE Trans. Electron Devices **47**, 2 (2000)
- 7.88. G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, E. Zanoni, IEEE Trans. Electron Devices **53**, 2932 (2006)
- 7.89. M. Meneghini, L. Trevisanello, S. Levada, G. Meneghesso, G. Tamiazzo, E. Zanoni, T. Zahner, U. Zehnder, V. Härtle, U. Strauß, in *IEDM Technical Digest*, Washington DC, 2005, pp. 1009–1012
- 7.90. S. Mertens, J. del Alamo, IEEE Trans. Electron Devices **49**, 1849 (2002)
- 7.91. J. Mittereder, S. Binari, P. Klein, J. Roussos, D. Katzer, D. Storm, D. Koleske, A. Wickenden, R. Henry, Appl. Phys. Lett. **83**, 1650 (2003)
- 7.92. G. Moore, in *IEEE International Solid-State Circuits Conference*, vol. XLVI, San Francisco, 2003, pp. 20–23
- 7.93. F. Mu, C. Tan, M. Xu, IEEE Trans. Electron Devices **48**, 2740 (2001)
- 7.94. S. Nakamura, G. Fasol, *The Blue Laser Diode* (Springer, Berlin Heidelberg New York, 1997)
- 7.95. R. Narasimhan, L. Sadwick, R. Hwu, IEEE Trans. Electron Devices **46**, 24 (1999)
- 7.96. P. Neudeck, R. Okojie, L. Chen, Proc. IEEE **90**, 1065 (2002)
- 7.97. J. Nikaido, T. Kikkawa, E. Mitani, S. Yokokawa, Y. Tateno, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, pp. 97–100
- 7.98. A. Oki, in *IMS Workshop WSG: Solid-State Power Invades the Tube Realm*, Honolulu, 2007
- 7.99. J. Osvald, J. Kuzmik, G. Konstantinidis, P. Lobotka and A. Georgakilas Microelectronic Engineering, **81**, 181, (2005)
- 7.100. S. Oyama, T. Hashizume, H. Hasegawa Applied Surface Science **190**, 322 (2002)
- 7.101. V. Palankovski, S. Vitanov, R. Quay, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 107–110
- 7.102. J. Palmour, J. Milligan, J. Henning, S. Allen, A. Ward, P. Parikh, R. Smith, A. Saxler, M. Moore, Y. Wu, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 555–558
- 7.103. N. Pan, J. Elliott, M. Knowles, D. Vu, K. Kishimoto, J. Twynam, H. Sato, M. Fresina, G. Stillman, IEEE Electron Device Lett. **19**, 115 (1998)
- 7.104. M. Papastamatiou, N. Arpatzianis, G. Papaioannou, C. Papastergiou, A. Christou, IEEE Trans. Electron Devices **44**, 364 (1997)
- 7.105. E. Piner, S. Singhal, P. Rajagopal, R. Therrien, J. Roberts, T. Li, A. Hansson, J. Johnson, I. Kizilyalli, K. Linthicum, in *IEDM Technical Digest*, San Francisco, 2006, pp. 411–414
- 7.106. J. Piprek (ed.), *Nitride Semiconductor Devices: Principles and Simulation* (Wiley-VCH, Weinheim, 2007)
- 7.107. G. Ponchak, S.K.H. Ho-Chung, in *Digest of IEEE Microwave Millimeter-Wave Monolithic Circuits Symposium*, San Diego, 1994, pp. 69–72

- 7.108. W. Pribble, S. Sheppard, R. Smith, S. Allen, J. Palmour, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IMS Workshop on Wide Bandgap Technologies*, Seattle, 2002
- 7.109. F. Rampazzo, R. Pierobon, D. Pacetta, C. Gaquiere, D. Theron, B. Boudart, G. Meneghesso, E. Zanoni, *Microelectron. Reliab.* **44**, 1375 (2004)
- 7.110. P. Roblin, H. Rohdin, *High-Speed Heterostructure Devices* (Cambridge University Press, Cambridge, 2002)
- 7.111. P. Saunier, C. Lee, A. Balistreri, D. Dumka, J. Jimenez, H. Tseng, Y. Kao, P. Chao, K. Chu, A. Souzis, I. Eliashevich, S. Guo, J. del Alamo, J. Joh, M. Shur, in *Device Research Conference*, South Bend, 2007, pp. 35–36
- 7.112. P. Schmid, K.M. Lipka, J. Ibbetson, N. Nguyen, U. Mishra, L. Pond, C. Weitzel, E. Kohn, *IEEE Electron Device Lett.* **19**, 225 (1998)
- 7.113. R. Shaw, D. Sanderlin, J. DeJulio, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2007, pp. 3–20
- 7.114. J. Shealy, in *CSIC-IC Symposium Short Course: Emerging Technologies from Defense to Commercial*, Palm Springs, 2005
- 7.115. S. Sheppard, B. Pribble, R. Smith, A. Saxler, S. Allen, J. Milligan, R. Pen-gelly, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 175–178
- 7.116. N. Shmidt, D. Davydov, V. Emtsev, I. Krestnikov, A. Lebedev, W. Lundin, D. Poloskin, A. Sakharov, A. Usikov, A. Osinsky, *Phys. Stat. Sol. B* **216**, 533 (1999)
- 7.117. G. Simin, V. Adivarahan, J. Yang, A. Koudymov, S. Rai, M. Khan, *Electron. Lett.* **41**, 774 (2005)
- 7.118. R. Singh, D. Capell, M. Das, L. Lipkin, J.W. Palmour, *IEEE Trans. Electron Devices* **50**, 471 (2003)
- 7.119. S. Singhal, A. Chaudhari, A. Hanson, J. Johnson, R.T.P. Rajagopal, T. Li, C. Park, A. Edwards, E. Piner, I. Kizilyalli, K. Linthicum, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2006, pp. 21–24
- 7.120. S. Singhal, A. Hanson, A. Chaudhari, P. Rajagopal, T. Li, J. Johnson, W. Nagy, R. Therrien, C. Park, A. Edwards, E. Piner, K. Linthicum, I. Kizilyalli, in *Reliability of Compound Semiconductors Workshop*, San Antonio, 2006
- 7.121. S. Singhal, T. Li, A. Chaudhari, A. Hanson, R. Therrien, J. Johnson, W. Nagy, J. Marquart, P. Rajagopal, J. Roberts, E. Piner, I. Kizilyalli, K. Linthicum, *Microelectron. Reliab.* **46**, 1247 (2006)
- 7.122. M.H. Sommerville, J.D. Alamo, P. Saunier, *IEEE Trans. Electron Devices* **45**, 1883 (1998)
- 7.123. A. Sozza, C. Dua, E. Morvan, M. diForte Poisson, S. Delage, F. Rampazzo, A. Tazzoli, F. Danesin, G. Meneghesso, E. Zanoni, A. Curutchet, N. Malbert, N. Labat, B. Grimbert, J.D. Jaeger, in *IEDM Technical Digest*, Washington DC, 2005, pp. 590–593
- 7.124. A. Sozza, C. Dua, E. Morvan, B. Grimber, S. Delage, *Microelectron. Reliab.* **45**, 1617 (2005)
- 7.125. A. Sozza, C. Dua, E. Morvan, B. Grimbert, V. Hoel, S. Delage, N. Chatuverdi, R. Lossy, J. Wuerfl, *Microelectron. Reliab.* **44**, 1369 (2004)
- 7.126. A. Stopel, A. Khramtsov, O. Katz, S. Solodky, T. Baksht, Y. Knafo, M. Leibovitch, Y. Shapira, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 14.19

- 7.127. T. Sudarshan, G. Gradinaru, J. Yang, M. Khan, *Electron. Lett.* **34**, 927 (1998)
- 7.128. T. Suemitsu, Y. Fukai, H. Sugiyama, K. Watanabe, H. Yokoyama, *Microelectron. Reliab.* **42**, 47 (2002)
- 7.129. B. Surridge, J. Law, B. Oliver, W. Pakulski, H. Strackholder, M. Abou-Khalil, G. Bonneville, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, San Diego, 2002, p. 3A
- 7.130. H. Tan, J. Williams, C. Yuan, S. Pearton, in *MRS Symposium*, Boston, 1996, pp. 807–811
- 7.131. R. Therrien, S. Singhal, J. Johnson, W. Nagy, R. Borges, A. Chaudhari, A. Hanson, A. Edwards, J. Marquart, P. Rajagopal, C. Park, I. Kizilyallı, K. Linthicum, in *IEDM Technical Digest*, Washington DC, 2005, pp. 568–571
- 7.132. V. Tilak, M. Ali, V. Cimalla, V. Manivannan, P. Sandvik, J. Fedison, O. Ambacher, D. Merfeld, in *Proceedings of Materials Research Society Symposium*, Warrendale, 2004, pp. 593–597
- 7.133. R. Trew, Y. Liu, W. Kuang, G. Bilbro, in *Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 103–106
- 7.134. G. Umana-Membreno, J. Dell, G. Parish, B. Nener, L. Faraone, U. Mishra, *IEEE Trans. Electron Devices* **50**, 2326 (2003)
- 7.135. P. Valizadeh, D. Pavlidis, in *GaAs IC Symposium Technical Digest*, San Diego, 2003, pp. 78–81
- 7.136. P. Valizadeh, D. Pavlidis, *IEEE Trans. Electron Devices* **52**, 1933 (2005)
- 7.137. R. Versari, A. Pieracci, *IEEE Trans. Electron Devices* **46**, 1228 (1999)
- 7.138. A. Villanueva, J.A. del Alamo, T. Hisaka, T. Ishida in *IEDM Technical Digest*, Washington DC, 2007, pp. 393–396
- 7.139. C. Wang, J. Vac. Sci. Technol. B **20**, 1821 (2002)
- 7.140. X.W. Wang, W. Zhu, X. Guo, T. Ma, J. Tucker, M. Rao, in *IEDM Technical Digest*, Washington DC, 1999, pp. 209–212
- 7.141. A. Ward, in *IMS Workshop WFI GaN Device and Circuit Reliability*, Honolulu, 2007
- 7.142. C. Wilson, A. O'Neill, S. Baier, J. Nohava, *IEEE Trans. Electron Devices* **43**, 201 (1996)
- 7.143. J. Würfl, J. Hilsenbeck, E. Nebauer, G. Tränkle, H. Obloh, W. Österle, *Microelectron. Reliab.* **40**, 1689 (2000)
- 7.144. H. Xing, P. Chavarkar, S. Keller, S. DenBaars, U. Mishra, *IEEE Electron Device Lett.* **24**, 141 (2003)
- 7.145. F. Yamaki, K. Ishii, M. Nishi, H. Haematsu, Y. Tateno, H. Kawata, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 95–98
- 7.146. B. Yang, W. Li, E. Casterline, in *Proceedings of the International Symposium on GaAs and Related Compounds*, Seattle, 2000, pp. 53–61
- 7.147. S. Yoshida, J. Suzuki, *J. Appl. Phys.* **85**, 7931 (1999)
- 7.148. L. Yu, Q. Liu, Q. Quao, S. Lau, J. Redwing, *J. Appl. Phys.* **84**, 2099 (1998)
- 7.149. E. Zanoni, G. Meneghesso, G. Verzellesi, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, in *IEDM Technical Digest*, Washington DC, 2007, pp. 381–384

References of Chapter 8

- 8.1. Z. Aboush, J. Benedikt, J. Priday, P. Tasker, in *10th High Frequency Post-graduate Student Colloquium*, University of Leeds, 2005, p. WE4B4
- 8.2. N. Adachi, Y. Tateno, S. Mizuno, A. Kawano, J. Nikaido, S. Sano, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 507–510
- 8.3. A. Agrawal, R. Clark, J. Komiak, in *IEEE International Microwave Symposium Digest*, San Francisco, 1996, pp. 995–999
- 8.4. Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, M. Kuzuhura, in *IEDM Technical Digest*, Washington DC, 2001, pp. 381–384
- 8.5. A. Angelini, M. Furno, F. Cappelluti, F. Bonani, M. Pirola, G. Ghione, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 145–148
- 8.6. I. Anjoh, A. Nishimura, S. Eguchi, IEEE Trans. Electron Devices **45**, 743 (1998)
- 8.7. A. Barnes, A. Boetti, L. Marchand, J. Hopkins, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 5–12
- 8.8. K. Beilenhoff, P. Quentin, S. Tranchant, O. Vaudescal, M. Parisot, H. Daembkes, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Milano, 2002, pp. 331–334
- 8.9. F. Benkhelifa, R. Kiefer, S. Müller, F. van Raay, R. Quay, R. Sah, M. Mikulla, G. Weimann, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.4
- 8.10. K. Bertilsson, C. Harris, H. Nilsson, Solid-State Electron. **48**, 2103 (2004)
- 8.11. R. Bolam, V. Ramachandran, D. Coolbaugh, K. Watson, IEEE Trans. Electron Devices **50**, 941 (2003)
- 8.12. M. Brophy, A. Torrejon, S. Petersen, K. Avala, L. Liu, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Scottsdale, 2003, p. 4.1
- 8.13. E. Burgemeister, W. von Muench, E. Pettenpaul, J. Appl. Phys. **50**, 5790 (1979)
- 8.14. A. Cetronico, M. Cicolani, M. Comparini, U.D. Marcantonio, R. Giordani, L. Maresciali, in *Proceedings of European Microwave Conference*, Paris, 2005, p. 4

- 8.15. A. Chandrasekhar, S. Stoukatch, S. Brebels, J. Balachandran, E. Beyne, W. de Raedt, B. Nauwelaers, A. Poddar, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Munich, 2003, pp. 427–430
- 8.16. E. Chang, R. Dean, J. Proctor, R. Elmer, K. Pande, IEEE Trans. Semiconductor Manufacturing **4**, 66 (1991)
- 8.17. L. Chen, G. Hunter, P. Neudeck, in *MRS Symposium*, San Francisco, 2000, pp. T8.10.1–6
- 8.18. H. Chiu, S. Yang, Y. Chan, IEEE Trans. Microw. Theory Tech. **48**, 2210 (2001)
- 8.19. M. Comparini, C. Leone, P. Montanucci, M. Tursini, in *Proceedings of European Microwave Conference*, Milano, 2002, pp. 57–60
- 8.20. J. Conlon, N. Zhang, M. Poulton, J. Shealy, R. Vetry, D. Green, J. Brown, S. Gibb, in *IEEE Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 85–88
- 8.21. T. Daly, J. Fender, B. Duffin, M. Kottke, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Scottsdale, 2003, p. 10.6
- 8.22. A. Darwish, A. Bayba, H. Hung, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 2039–2042
- 8.23. A. Darwish, A. Bayba, H. Hung, IEEE Trans. Microw. Theory Tech. **52**, 2611 (2004)
- 8.24. A. David, T. Fujii, B. Moran, S. Nakamura, S. DenBaars, C. Weisbuch, H. Benisty Appl. Phys. Lett. **88**, 133514 (2006)
- 8.25. H. Davidson, N. Coletta, J. Kerns, D. Makowiecki, in *Proceedings of the Electronic Components and Technology Conference*, Las Vegas, 1995, pp. 538–541
- 8.26. R. Dietrich, A. Wieszt, A. Vescan, H. Leier, R. Stenzel, W. Klix, Solid-State Electron. **47**, 123 (2003)
- 8.27. C. Drevon, in *IEE Seminar of Packaging and Interconnects at Microwave and mm-Wave Frequencies*, London, 2000, pp. 8/1–8/4
- 8.28. L. Eastman, V. Tilak, J. Smart, B. Green, E. Chumbes, R. Dimitrov, H. Kim, O. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. Schaff, J. Shealy, IEEE Trans. Electron Devices **48**, 479 (2001)
- 8.29. G. Ellis, J. Moon, D. Wong, M. Micovic, A. Kurdoghlian, P. Hashimoto, M. Hu, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 153–156
- 8.30. M. Elta, A. Chu, L. Mahoney, R. Cerretani, W. Courtney, IEEE Electron Device Lett. **3**, 127 (1982)
- 8.31. J. Evans, in *IEEE Compound Semiconductor IC Symposium Technical Digest*, San Antonio, 2006, pp. 211–214
- 8.32. D. Fanning, L. Witkowski, C. Lee, D. Dumka, H. Tserng, P. Saunier, W. Gaiewski, E. Piner, K. Linthicum, J. Johnson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 8.3
- 8.33. K. Filippov, A. Balandin, MRS Internet J. Nitride Semicond. Res. **8**, (2003)
- 8.34. J. Fleuriol, A. Borshchevsky, M. Ryan, W. Phillips, E. Kolawa, T. Kacisch, R. Ewell, in *Proceedings of the International Conference on Thermoelectrics*, Dresden, 1997, pp. 641–645
- 8.35. D. Floriot, J. Jacquet, E. Chartier, J. Coupat, P. Eudeline, P. Auxemery, H. Blanck, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 541–544

- 8.36. J. Freeman, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 2039–2042
- 8.37. J. Galiere, J. Valard, E. Estebe, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 591–594
- 8.38. R. Gaska, A. Osinsky, J. Yang, M. Shur, *IEEE Electron Device Lett.* **19**, 89 (1998)
- 8.39. J. Gassmann, P. Watson, L. Kehias, G. Henry, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 615–618
- 8.40. S. Green, D. Perrottet, B. Richerzhagen, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 145–148
- 8.41. E. Gu, C. Jeon, H. Choi, G. Rice, M. Dawson, E. Illy, M. Knowles, *Thin Solid Films*, **453/454**, 26 (2004)
- 8.42. H. Hommel, H. Feldle, in *Proceedings of European Radar Conference*, Amsterdam, 2004, pp. 121–124
- 8.43. H. Hu, C. Zhu, Y. Lu, M. Li, B. Cho, W. Choi, *IEEE Electron Device Lett.* **23**, 514 (2002)
- 8.44. H. Hu, C. Zhu, X. Yu, A. Chin, M. Li, B.J. Cho, D. Kwong, P. Foo, M.B. Yu, X. Liu, J. Winkler, *IEEE Electron Device Lett.* **24**, 60 (2003)
- 8.45. A. Jezowski, B. Danilchenko, M. Bockowski, I. Grzegory, S. Kukowski, T. Suski, T. Paszkiewicz, *Solid-State Commun.* **128**, 69 (2003)
- 8.46. R. Joshi, P. Neudeck, C. Fazi, *J. Appl. Phys.* **88**, 265 (2000)
- 8.47. B. Kang, S. Kim, F. Ren, J. Johnson, R. Therrien, P. Rajagopal, J. Roberts, E. Piner, K. Linthicum, S. Chu, K. Baik, B. Gila, C. Abernathy, S. Pearton, *Appl. Phys. Lett.* **85**, 2962 (2004)
- 8.48. D. Katsis, J. vanWyk, *IEEE Trans. Compon. Pack. Technol.* **29**, 127 (2006)
- 8.49. K. Kobayashi, Y. Chen, I. Smorchkova, R. Tsai, M. Wojtowicz, A. Oki, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 619–622
- 8.50. J. Komiak, W. Kong, K. Nicols, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 905–907
- 8.51. A. Kopp, M. Borkowski, G. Jerinic, *IEEE Trans. Microw. Theory Tech.* **50**, 827 (2002)
- 8.52. B. Kopp, in *IEEE International Microwave Symposium Digest*, Boston, 2000, pp. 705–708
- 8.53. A. Kowalczyk, V. Alder, C. Amir, F. Chiu, C.P. Chng, W.J.D. Lange, Y. Ge, S. Ghosh, T.C. Hoang, B. Huang, S. Kant, Y.S. Kao, C. Khieu, S. Kumar, L. Lee, A. Liebermensch, X. Liu, N.G. Malur, A.A. Martin, H. Ngo, S. Oh, I. Orginos, L. Shih, B. Sur, M. Tremblay, A. Tzeng, D. Vo, S. Zambare, J. Zong, *IEEE J. Solid-State Circuits* **36**, 1609 (2001)
- 8.54. S. Kukowski, A. Witek, J. Adamczyk, J. Jun, M. Bockowski, I. Grzegory, B. Lucznik, G. Nowak, M. Wroblewski, A. Presz, S. Gierlotka, S. Stelmach, B. Palosz, S. Porowski, P. Zinn, *J. Phys. Chem. Solids* **59**, 289 (1998)
- 8.55. M. Kuball, J. Hayes, M. Uren, T. Martin, J. Birbeck, R. Balmer, B. Hughes, *IEEE Electron Device Lett.* **23**, 7 (2002)
- 8.56. M. Kuball, A. Sarua, H. Ji, M. Uren, R. Balmer, T. Martin, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1339–1342
- 8.57. J. Kuzmik, S. Bychikhin, M. Neuburger, A. Dadgar, A. Kroft, E. Kohn, D. Pogany, *IEEE Trans. Electron Devices* **52**, 1698 (2005)

- 8.58. J. Kuzmik, P. Javorka, A. Alam, M. Marso, M. Heuken, P. Kordos, IEEE Trans. Electron Devices **49**, 1496 (2002)
- 8.59. F.D. la Hidalga, M. Deen, E. Gutiérrez, IEEE Trans. Electron Devices **47**, 1098 (2000)
- 8.60. P. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs* (Artech House, Boston London, 1989)
- 8.61. J. Laskar, S. Nuttinck, S. Pinel, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 217–220
- 8.62. L. Lecheminoux, N. Gosselin, in *IEEE International Electronics Manufacturing Technology Symposium*, San Jose, 2003, pp. 255–260
- 8.63. D. Leung, Y. Chou, C. Wu, R. Kono, J. Scarpulla, R. Lai, M. Hoppe, D. Streit, in *Radio Frequency Integrated Circuits Symposium Digest*, Anaheim, 1999, pp. 153–156
- 8.64. W. Liu, A. Balandin, Appl. Phys. Lett. **85**, 5230 (2004)
- 8.65. M. Ludwig, C. Buck, F. Coromina, M. Suess, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1619–1622
- 8.66. M. Mahalingam, E. Mares, in *IEEE International Microwave Symposium Digest*, Phoenix, 2001, pp. 2199–2202
- 8.67. Y. Mancuso, P. Gremillet, P. Lacomme, in *Proceedings of European Microwave Conference*, Paris, 2005, pp. 817–820
- 8.68. C. Martin, T. Kerr, W. Stepko, T. Anderson, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 291–294
- 8.69. S. Marsh, J. Clifton, K. Vanner, J. Cockrill, I. Davies, in *Proceedings International Symp. Elec. Dev. for Microwave and Optoelectronic Applications EDMO*, London, 1997, pp. 169–174
- 8.70. S. McCarthy, P. Smith, J. Walker, N. Padfield, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 1023–1026
- 8.71. D. McQuiddy, R. Gassner, P. Hull, J. Mason, J. Bedinger, Proc. IEEE **79**, 308 (1991)
- 8.72. K. Meyyappan, P. McCluskey, L. Chen, IEEE Trans. Devices Mater. Rel. **3**, 152 (2003)
- 8.73. E. Mitani, M. Aojima, A. Maekawa, S. Sano, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 213–216
- 8.74. M. Micovic, A. Kurdoghlian, H. Moyer, P. Hashimoto, A. Schmitz, I. Milosavjevic, P. Willadesn, W. Wong, J. Duvall, M. Hu, M. Delaney, D. Chow, in *IEEE International Microwave Symposium Digest*, Fort Worth, 2004, pp. 1653–1656
- 8.75. J. Mizoe, S. Amano, T. Kuwabara, T. Kaneko, K. Wada, A. Kato, K. Sato, M. Fujise, in *IEEE International Microwave Symposium Digest*, Anaheim, 1999, pp. 475–478
- 8.76. J. Moore, A. Smith, D. Nguyen, S. Kulkarni, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Miami, 2004, pp. 175–178
- 8.77. W. Nagy, S. Singhal, R. Borges, W. Johnson, J. Brown, R. Therrien, A. Chaudhari, A. Hanson, J. Riddle, S. Booth, P. Rajagopal, E. Piner, K. Linthicum, in *IEEE International Microwave Symposium Digest*, Long Beach, 2005, pp. 483–486

- 8.78. T. Nakatsuka, J. Itoh, T. Yoshida, M. Nishitsuji, T. Uda, O. Ishikawa, IEEE J. Solid-State Circuits **33**, 1284 (1998)
- 8.79. P. Neudeck, R. Okojie, L. Chen, Proc. IEEE **90**, 1065 (2002)
- 8.80. C. Ng, K. Chew, S. Chu, IEEE Electron Device Lett. **24**, 506 (2003)
- 8.81. S. Nuttinck, B. Banerjee, S. Venkataraman, J. Laskar, M. Harris, in *IEEE International Microwave Symposium Digest*, Philadelphia, 2003, pp. 221–223
- 8.82. S. Nuttinck, E. Gebara, J. Laskar, B. Wagner, M. Harris, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 921–924
- 8.83. S. Nuttinck, R. Mukhopadhyay, C. Loper, S. Singhal, M. Harris, J. Laskar, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 79–82
- 8.84. S. Nuttinck, B. Wagner, B. Banerjee, S. Venkataraman, E. Gebara, J. Laskar, H. Harris, IEEE Trans. Microw. Theory Tech. **51**, 2445 (2003)
- 8.85. Y. Ohno, M. Kuzuhara, IEEE Trans. Electron Devices **48**, 517 (2001)
- 8.86. V. Palankovski, S. Selberherr, in *Proceedings of European Conference on High Temperature Electronics Conference*, Berlin, 1999, pp. 25–28
- 8.87. J. Park, P. Sercel, Comp. Semicond. **48**, 517 (2002)
- 8.88. D. Perrottet, A. Spiegel, S. Amorosi, B. Richerzhagen, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 14.16
- 8.89. N. Pham, P. Sarro, K. Ng, J.N. Burghartz, IEEE Trans. Electron Devices **48**, 1756 (2001)
- 8.90. S. Pinel, S. Chakraborty, M. Roellig, R. Kunze, S. Mandal, H. Liang, C. Lee, R. Li, K. Lim, G. White, M. Tentzeris, J. Laskar, in *IEEE International Microwave Symposium Digest*, Seattle, 2002, pp. 1553–1556
- 8.91. S. Pinel, A. Marty, J. Tasselli, J. Bailbe, E. Beyne, R.V. Hoof, S. Marco, J. Morante, O. Vendier, M. Huan, IEEE Trans. Compon. Pack. Technol. **25**, 244 (2002)
- 8.92. K. Pipe, R. Ram, A. Shakouri, IEEE Photonics Technol. Lett. **14**, 433 (2002)
- 8.93. W. Pribble, S. Sheppard, R. Smith, S. Allen, J. Palmour, T. Smith, Z. Ring, J. Sumakeris, A. Saxler, J. Milligan, in *IMS Workshop Wide Bandgap Technologies*, Seattle, 2002
- 8.94. P. Regoliosi, A.R.A.D. Carlo, P. Romanini, M. Peroni, C. Lanzieri, A. Angelini, M. Pirola, G. Ghione, IEEE Trans. Electron Devices **53**, 182 (2006)
- 8.95. L. Sadwick, J. Chern, R. Nelson, R. Hwu, in *Proceedings of the High Temperature Electronics Conference*, Santa Fe, 2006, pp. 377–379
- 8.96. A. Sarua, H. Ji, M. Kuball, M. Uren, T. Martin, K. Hilton, R. Balmer, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Vancouver, 2006, pp. 179–182
- 8.97. A. Sarua, H. Ji, M. Kuball, M. Uren, T. Martin, K. Hilton, R. Balmer, IEEE Trans. Electron Devices **53**, 2438 (2006)
- 8.98. A. Sarua, J. Hangfeng, K. Hilton, D. Wallis, M. Uren, T. Martin, M. Kuball, IEEE Trans. Electron Devices **54**, 3152 (2007)
- 8.99. C. Schaffauser, O. Vendier, S. Forestier, F. Michard, D. Geffroy, C. Drevon, J. Villemazet, J. Cazaux, S. Delage, J. Roux, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Paris, 2005, pp. 537–540
- 8.100. F. Schmückle, A. Jentzsch, W. Heinrich, J. Butz, M. Spinnler, in *IEEE International Microwave Symposium Digest*, Phoenix, 2001, pp. 1903–1906

- 8.101. P. Schuh, R. Leberer, H. Sledzik, D. Schmidt, M. Oppermann, B. Adelseck, H. Brugger, R. Quay, F. van Raay, M. Seelmann-Eggebert, R. Kiefer, W. Bronner, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1324–1327
- 8.102. M. Seelmann-Eggebert, P. Meisen, F. Schaudel, P. Koidl, A. Vescan, H. Leier, Diamond Relat. Mater. **10**, 744 (2001)
- 8.103. K. Seemann, S. Ramberger, A. Tessmann, R. Quay, J. Schneider, M. Riessle, H. Walcher, M. Kuri, R. Kiefer, M. Schlechtweg, in *Proceedings of European Microwave Conference*, Munich, 2003, pp. 383–386
- 8.104. S. Selberherr, *Analysis and Simulation of Semiconductor Devices* (Springer, Wien New York, 1984)
- 8.105. J. Shealy, in *GaAs-IC Symposium Short Course: Emerging Technologies from Defense to Commercial*, San Diego, 2003
- 8.106. J. Shealy, in *CSIC-IC Symposium Short Course: Emerging Technologies from Defense to Commercial*, Palm Springs, 2005
- 8.107. S. Sheppard, W. Pribble, D. Emerson, Z. Ring, R. Smith, S. Allen, J. Milligan, J. Palmour, in *Proceedings of IEEE/Cornell Conference on High Performance Devices*, Ithaca, 2000, pp. 232–236
- 8.108. C. Shih, J. Sjöström, R. Bagger, P. Anderson, Y. Yu, G. Ma, Q. Chen, T. Aberg, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 889–892
- 8.109. S. Singhal, J. Brown, R. Borges, E. Piner, W. Nagy, A. Vescan, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Milano, 2002, pp. 37–40
- 8.110. G. Slack, R. Tanzilli, R. Pohl, J. Vandersande, J. Phys. Chem. Solids **48**, 641 (1987)
- 8.111. M. Spencer, J. Palmour, C. Carter, IEEE Trans. Electron Devices **49**, 940 (2002)
- 8.112. N. Stath, V. Högle and J. Wagner Materials Science and Engineering B **80**, 224 (2001)
- 8.113. M. Südow, K. Andersson, N. Billström, J. Grahn, H. Hjelmgren, J. Nilsson, P. Nilsson, J. Stahl, H. Zirath, N. Rorsman, IEEE Trans. Microw. Theory Tech. **54**, 4072 (2006)
- 8.114. Y. Suh, D. Richardson, A. Dardello, S. Mahon, J. Harvey, in *Proceedings of European Microwave Conference*, Paris, 2005, pp. 545–548
- 8.115. J. Sun, H. Fatima, A. Koudymov, A. Chitnis, X. Hu, H. Wang, J. Zhang, G. Simin, J. Yang, M. Khan, IEEE Electron Device Lett. **24**, 375 (2003)
- 8.116. R. Therrien, A. Chaudhari, S. Singhal, C. Snow, A. Edwards, C. Park, W. Nagy, J. Johnson, A. Hanson, K. Linticum, I. Kizilyalli, in *IEEE International Microwave Symposium Digest*, Honolulu, 2007, pp. 635–638
- 8.117. B. Thibeault, B. Keller, Y. Wu, P. Fini, U. Mishra, C. Nguyen, N. Nguyen, M. Le, in *IEDM Technical Digest*, Washington DC, 1997, pp. 569–572
- 8.118. V. Turin, A. Balandin, Electron. Lett. **40**, 81 (2004)
- 8.119. M. van Heijningen, J. Priday, in *Proceedings of European Microwave Conference*, Amsterdam, 2004, pp. 357–360
- 8.120. F. van Raay, R. Quay, R. Kiefer, W. Bronner, M. Seelmann-Eggebert, M. Schlechtweg, M. Mikulla, G. Weimann, in *IEEE International Microwave Symposium Digest*, San Francisco, 2006, pp. 1368–1371

- 8.121. R. Vandersmissen, J. Das, W. Ruythooren, J. Derluyn, M. Germain, D. Xiao, D. Schreurs, G. Borghs, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, New Orleans, 2005, p. 13.3
- 8.122. C. Varmazis, G. D'Urso, H. Hendricks, *Semiconduct. Int.* **23**, 87 (2000)
- 8.123. F. Villard, J. Prigent, E. Morvan, C. Dua, C. Brylinski, F. Temcamani, *IEEE Trans. Microw. Theory Tech.* **51**, 1129 (2003)
- 8.124. A. Ward, in *IMS Workshop WFI GaN Device and Circuit Reliability*, Honolulu, 2007
- 8.125. M. Watts, in *Proceedings of High Temperature Electronics Conference*, Santa Fe, 2006, pp. 371–376
- 8.126. M. Werner, W. Fahmer, *IEEE Trans. Ind. Electron.* **48**, 249 (2001)
- 8.127. J. Wilson, P. Raad, *Int. J. Heat Mass Transf.* **47**, 3707 (2004)
- 8.128. M. Winser, in *Proceedings of European Microwave Conference*, Paris, 2005, pp. 493–496
- 8.129. Y Wu, D. Kapolnek, J. Ibbetson, P. Parikh, B. Keller, U. Mishra, *IEEE Trans. Electron Devices* **48**, 586 (2001)
- 8.130. Y. Wu, B. Keller, S. Keller, D. Kapolnek, S. Denbaars, U. Mishra, *IEEE Electron Device Lett.* **17**, 455 (1996)
- 8.131. J. Xu, W. Yin, J. Mao, *IEEE Microw. Wireless Compon. Lett.*, **17**, 55 (2007)
- 8.132. L. Xue, C. Liu, H. Kim, S. Kim, S. Tiwari, *IEEE Trans. Electron Devices* **50**, 601 (2003)
- 8.133. M. Yang, C. Huang, A. Chin, C. Zhu, M. Li, D. Kwong, *IEEE Electron Device Lett.* **24**, 306 (2003)
- 8.134. B. Yeats, *IEEE Trans. Electron Devices* **45**, 939 (1998)
- 8.135. T. Young, *Surface and Coatings Technology* **202**, 1208 (2007)
- 8.136. J. Zimmer, G. Chandler, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Austin, 2007, pp. 129–132
- 8.137. A. Ziroff, M. Nalezinski, W. Menzel, in *Proceedings of European GaAs and Related Compounds Application Symposium GAAS*, Amsterdam, 2004, pp. 491–494
- 8.138. J. Zolper, in *Proceedings of the International Conference on GaAs Manufacturing Technology*, Scottsdale, 2003, p. 1.2

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Progress In RF Device Modeling: From MESFETs To GaN PHEMTs

BY YUSUKE TAJIMA, PH.D.,
AURIGA MEASUREMENT SYSTEMS

A Brief History Of RF Device Modeling

Gallium arsenide (GaAs) field-effect transistor (FET) modeling activities began in the 1980s. In those days, engineers worked in an environment that was quite different from the one engineers work in today. All computational work was done on main-frame computers (IBM and VAX), which were considerably slower than today's PCs. Large-signal simulators were not yet available. Modeling engineers had to write their own software to solve harmonic balance equations. In fact, the term "harmonic balance" itself was a new concept for many electrical engineers!

In 1980, the first empirical model of a GaAs FET was presented by Walter Curtice¹, who demonstrated a waveform output of an amplifier in the time

domain using SPICE simulation. A few months later in 1981, Yusuke Tajima et al presented a paper² in which, using their own empirical model, amplifier and oscillator performance was simulated in the frequency domain. Simulations of P_{in} versus P_{out} performance and load pull contours (*Figure 1*) were demonstrated in their paper, signifying the first time that modeling and simulation techniques were used to demonstrate RF characteristics in forms that RF engineers are familiar with today. The simulation program was primitive — later called “piecemeal 0th order harmonic balance” — and the conversion was terrible. By 1985, A. Materka³ and Curtice⁴ revealed their own models and frequency domain analysis using a much-improved harmonic balance program. These three (Tajima, Materka, and Curtice) models are still available in Agilent Technologies' Advanced Design System (ADS) software, but their value is more historical than practical for modern-day devices.

These engineers had a difficult time achieving agreement between model simulation and measurement data. The discrepancy was sometimes very large. Some tried to compromise the model by inserting artificial components, dispersive elements, but this just led to more discrepancy in other characteristics.

The basis of all of these models, as described in Materka's paper, was that “the large-signal device properties were governed primarily by the transistor DC characteristics.” This approach, however, turned out to be too simplistic. In 1990, A. Platzker, Y. Tajima, and other engineers from Raytheon first showed that the IV (current-voltage) relation that controlled RF trajectory could be very different from DC characteristics. They developed a “pulsed IV measurement system”⁵ and measured instantaneous IV curves when the device was biased up to different operating conditions (*Figure 2*). The pulsed IV

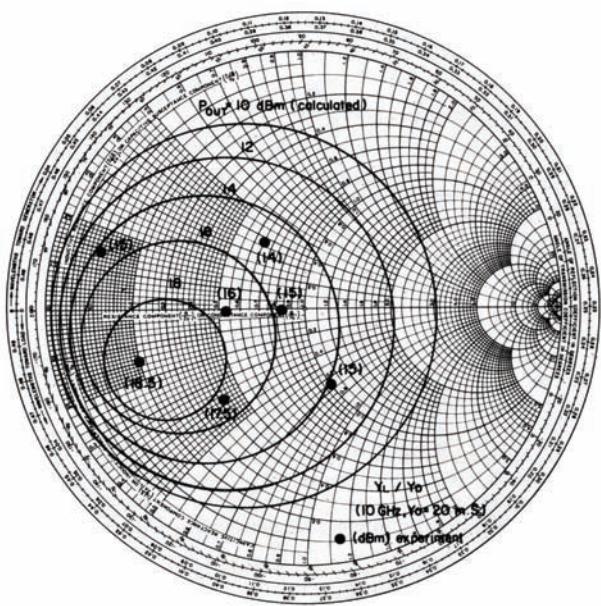


FIGURE 1: FIRST SIMULATED LOAD PULL CONTOURS ON LOAD ADMITTANCE CHART ALONG WITH EXPERIMENTAL DATA IN DOTS.²

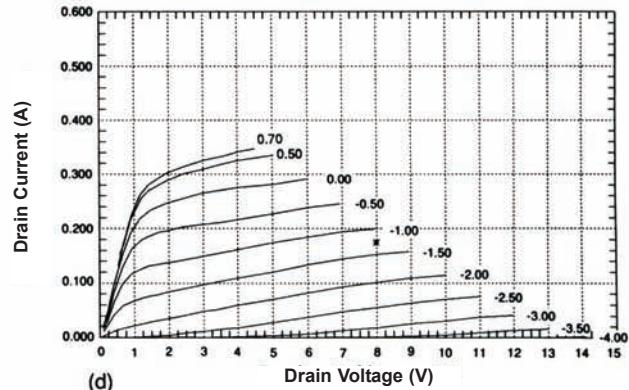
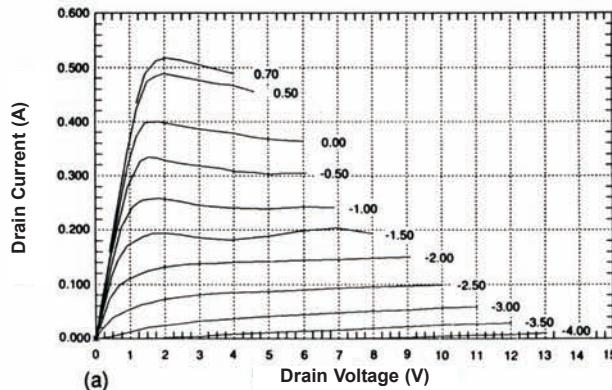


FIGURE 2: FIRST PULSED IV DATA OF A GAAS FET – WITH A BIAS AT OVD AND OVG (A), AND WITH A BIAS AT 8VD AND -1.25VG (D) – SHOWING A LARGE BIAS DEPENDENCY OF IV CHARACTERISTICS.⁵ SUCCESSFUL SIMULATION RESULTS WERE OBTAINED WHEN IV CURVES WERE MODELED WITH A BIAS APPLIED (D).

curves were not only very different from DC IV curves, but varied with bias points. When the pulsed IV curves measured from the amplifier bias condition were used in the model, the agreement between the model simulation and measured data was greatly improved, accurately predicting output power, efficiency, and small-signal gain, which was previously difficult to achieve. Various companies, including Accent, Agilent, Auriga Measurement Systems, and Keithly Instruments, have since commercialized pulsed IV systems.

In the 1990s, various simulation tools started providing harmonic balance analysis capability. For the first time, large-signal simulation became available to the vast majority of circuit design engineers. New models were introduced that offered more sophistication in their parameters, including capacitor (C_{gs} , C_{gd} , C_{ds}) dependency on gate and drain voltages. EEs of GaAs high electron mobility transistor (EEHEMT) and Angelov models, which are quite common today, were also introduced in the 1990s.

However, the dependency of capacitors on two terminal voltages (V_{gs} , V_{ds}) led to a breakdown on the charge conservation law and resulted in the nonphysical conduction current through capacitances. Figures 3 and 4 show extracted C_{gs} and C_{gd} from PHEMT (pseudomorphic high electron mobility transistor) S-parameter measurement, illustrating the dependency on both V_{gs} and V_{ds} . Various authors discussed the issue of charge conservation and introduced new restrictions on the capacitance models. A proposal to add a transcapacitance element in the model to maintain the charge conservation was made by D. Root⁶. EEHEMT and Angelov models do not satisfy the charge conservation law. With these models, when two-voltage dependency on the capacitors

C_{gs} (pF) vs. V_{gs} with V_{ds} as a parameter

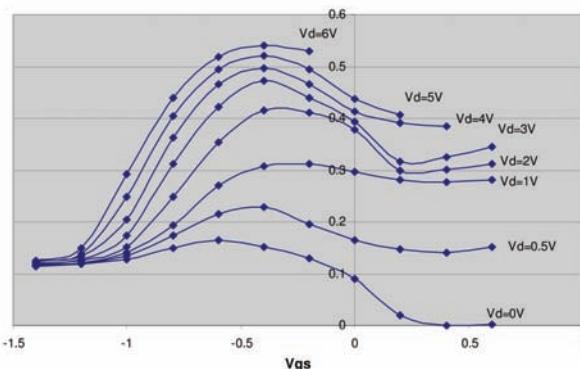


FIGURE 3: CGS DEPENDENCY ON VGS AND VDS (PHEMT).

C_{dg} vs. V_{dg} with V_{gs} as parameter (data)

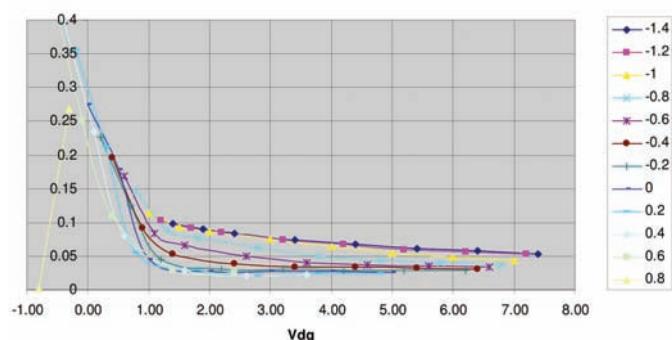


FIGURE 4: CDG DEPENDENCY ON VDG (=VDS-VGS) AND VGS (PHEMT).

is specified, users must be aware that the non-physical conduction current may start to flow through the gate terminal. Many new models have been introduced to correct this problem.

Developing More Accurate Modeling Techniques

The recent introduction of new device types, as well as stringent efficiency and linearity requirements from new systems, is necessitating more accurate modeling techniques. The behavior modeling technique — where raw S-parameters at a large number of bias points are stored as a database and use the S-parameter set as a function of the terminal voltages to simulate large-signal performance — has made steady progress in recent years, especially with the introduction of artificial neural networks. Various

authors report accurate simulation results for adjacent channel power ratio (ACPR) and error vector magnitude (EVM).

However, this approach has not acquired general acceptance yet, due to the fact that the model is not very portable to different sites and is not very scalable to other sizes or temperatures.

Traditional empirical modeling approaches, where a set of equations is used to represent device characteristics, are still the preferred approach for many design environments. Equations are becoming more sophisticated in order to accurately handle different types of devices — such as PHEMTs, gallium nitride (GaN) devices, and enhancement-mode devices — over a wide range of voltages. The model developed at Auriga uses almost 100 parameters, which is large compared to the classical models of the 1980s. On the other hand, it is minuscule compared to behavior models where thousands of data points must be handled. Empirical models are easy to port, easy to scale for the size and temperature, and easy to simulate the bias point change under drive.

When 100 parameters are involved — most of them to be determined from measured data — model extraction requires a great deal of number crunching

and extraction, which cannot be executed without the help of a smart extraction program. If the extraction is not programmed with intelligence, the model may not be useable. We also have to make certain that the data is accurate and well de-embedded. In other words, the modeling must be supported by good data and an intelligent extraction program.

A Current Approach To Large-Signal Modeling

The procedure for large-signal modeling that is being adopted at Auriga is as follows:

- De-embedding circuit file definition:* S2P files have to be defined to represent the circuits between the system reference planes and device ports. This can be done either by calculation or measurement of standards. All the device S2P files will be de-embedded using the de-embedding files.
- DC IV curve measurement:* This is to determine the voltage and current range to be tested in the subsequent tests.
- DC diode measurement:* This is to determine the diode parameters between gate to source and gate to drain.
- ColdFET measurement and extraction of parasitic component values:* FETs are measured with $V_d=0$ with varying forward gate current. Parasitic component values are determined through this data.
- S-parameter measurement and extraction of small-signal model:* S-parameters are measured with varying bias points — sometimes more than 100 — to cover RF trajectory. From extracted equivalent circuit models, voltage dependency of capacitances (C_{gs} , C_{ds} , C_{gd}) is derived.
- Pulsed IV measurement and IV model extraction:* Pulsed IV data is taken from the operating bias point. IV model parameters are extracted from the data.
- Load pull measurement:* Optional load pull measurements are carried out to obtain verification data and are compared to the simulated results using the model. Load pull data are taken with a single tone, two tones, or other modulated signals.

By completing these steps, all necessary model parameters are derived. These model parameter extraction steps require the Auriga ModelStation program to handle the large amount of data and large number of parameters to be extracted.

Figures 5 and 6 show examples of successful model extraction of a GaN PHEMT device. The device, Eudyna's EGN010MK, has a bias voltage at

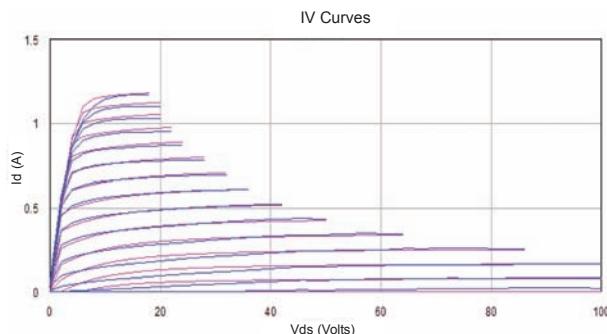


FIGURE 5: PULSED IV CHARACTERISTICS ($V_{BIAS} = 50$ V, $V_{PULSE} = 0$ TO 100 V) WERE MODELED USING THE AURIGA MODEL. OTHER VOLTAGE-DEPENDENT PARAMETERS SUCH AS C_{GS} , C_{GD} , AND C_{DS} WERE DERIVED FROM S-PARAMETER MEASUREMENT OVER 100 BIAS POINTS.

50 V. *Figure 5* shows measured pulsed IV data compared to modeled IV curves, demonstrating excellent agreement. *Figure 6* shows measured P_{in} vs. P_{out} and power-added efficiency of the packaged device compared to the simulated results using Applied Wave Research's Microwave Office (MWO) and Agilent's ADS where the extracted model is installed. Results from both simulators are identical and very close to the measured data.

Remaining Hurdles To Overcome

RF device models are not yet perfect. The following paragraphs will discuss some of the remaining challenges that need to be addressed.

In many applications today, devices are biased near class B rather than class AB. This makes modeling more difficult, because the model parameters are changing rapidly at this bias point. Data must be taken at much finer voltage steps

near a r pinch-off to capture the rapid changes in parameters. As such, model equations must have an added feature to represent the subtle variations near a r pinch-off,

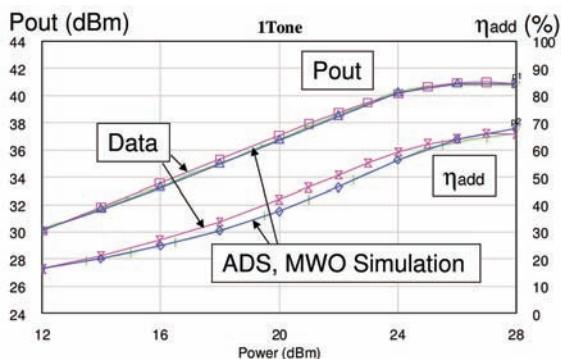


FIGURE 6: PIN VS. POUT AND ASSOCIATED POWER-ADDED EFFICIENCY WAS CALCULATED USING ADS AND MICROWAVE OFFICE, WITH IDENTICAL RESULTS. SIMULATED RESULTS ARE COMPARED TO THE ACTUAL MEASUREMENTS IN THIS FIGURE.

while still maintaining the global agreements over a wide range of bias points.

There is also a growing need for models of very large devices in the output power (RF) range of 50 W to 200 W. These devices must be measured as accurately as the smaller devices; however, the device impedance is much lower and the heat dissipation is much higher. S-parameters will have to be measured under pulsed bias from the nominal bias voltages to maintain isothermal conditions, and the device will have to be mounted in fixtures for measurement, rather than using an RF probing technique. The fixtures need to be low loss and well calibrated for de-embedding. These are not easy tasks.

Scaling device models from a small device to a large one will alleviate some of the issues associated with modeling large devices — if the scaling can be done accurately. However, larger devices inherently

have various parasitic elements related to additional structure to combine unit cells. Not all of these cells are operated at the same amplitude and phase, resulting in a loss of performance.

Techniques for modeling RF devices have made great strides since 1980. However, we still have a long way to go to satisfy all the needs of circuit and system engineers.

References

1. W.R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 28, No. 5, May 1980, pp. 448-456.
2. Y. Tajima, B. Wrona, and K. Mishima, "GaAs FET Large-Signal Model and Its Application to Circuit Designs," *IEEE Transactions on Electron Devices*, Vol. 28, No. 2, February 1981, pp. 171-175.
3. A. Materka and T. Kacprzak, "Computer Calculation of Large-Signal GaAs FET Amplifier Characteristics," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 33, No. 2, February 1985, pp. 129-135.
4. W.R. Curtice, and M. Ettenburg, "A Non-linear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 33, No. 12, 1985, pp. 1383-1394.
5. A. Platzker, A. Palevski, S. Nash, W. Struble, and Y. Tajima, "Characterization of GaAs Devices by a Versatile Pulse IV Measurement System," *IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, May 1990, pp. 1137-1140.
6. D.E. Root, from the 1999 Asia-Pacific Microwave Conference Workshop (WS2) Modeling and Characterization of Microwave Devices and Packages, Singapore.

About The Author

Yusuke Tajima received his B.S. and Ph.D. degrees in electronics engineering from Tokyo University in 1970 and 1980 respectively. He continued his research and developmental work at Toshiba Central Lab in Japan and then at the Raytheon Research Division in Massachusetts. He has contributed to many innovations in microwave devices, circuit designs, and characterization methods.

In 2000, Dr. Tajima became general manager of ACCO USA, responsible for the U.S. operations of ACCO (France). Since 2004, he has served as the director of modeling and design for Auriga Measurement Systems, overseeing the company's business unit focused on modeling and design. ●

Practical Design Comparison Between High-Power GaAs MESFET and GaN HEMT

By Ivan Boshnakov
Aerial Facilities Ltd.

This comparison of transistor technologies uses two similar amplifier designs to provide an accurate evaluation of their differences

applications. They offer higher power density and higher voltage operation, which in turn are associated with much lower parasitic capacitances and much higher load-line dynamic resistance, and hence wider bandwidth applications. Of the two kinds the GaN HEMTs offer higher gain performance.

This article compares the performance of a 10W GaAs MESFET which has been very popular for years and a new 10W GaN HEMT, by describing the practical design of 10W Class A amplifier stages with each of the two transistors.

The Comparative Design Problem

The comparative designs were provoked by the fact that both of the selected transistors are Eudyna products (the FLL120MK GaAs MESFET and the EGN010MK GaN HEMT) and that they exhibit very similar output power performance. Their metal-ceramic cases are also the same. Nonlinear models are also available for both transistors. The model for FLL120MK was purchased for a modest price from Modelithics. There was already an indication that this model is well behaved [1]. The model for the EGN010MK is available free from Eudyna and was developed by Auriga Measurement Systems.

By simply looking at the data sheets it is obvious that the GaN transistor is useful to much higher frequencies. The comparative

In the recent years wide bandgap transistors, such as SiC MESFETs and GaN HEMTs, have appeared on the market for high power RF/microwave

designs though are done at around 2GHz searching to maximize the bandwidth and the gain for each transistor at the same output power (P_{1dB}).

The design procedures are very similar to the ones described in [2] and [3]. As was done then, two CAD programs—MultiMatch Amplifier Design Wizard and Microwave Office—were again used in tandem.

The GaAs MESFET Design

The nonlinear model of FLL120MK was used first in Microwave Office to evaluate the maximum P_{1dB} that could be achieved. This was done by using the tuners in the same way as described in [2]. That showed a maximum P_{1dB} of 40.5 dBm at around 2 GHz (bias point: 10V, 2.2A).

Having a nonlinear model it would be possible to follow a design procedure similar to the one in [2], which started with extracting the optimum P_{1dB} output impedances for a number of frequencies by using the tuner at the output, and then using these impedances in MultiMatch to synthesize a network to provide them. That network could then be brought back into Microwave Office to check and tune the performance.

However, it was decided that because the performance would be a compromise between bandwidth and P_{1dB} , a procedure similar to the one in [3] should be used. This design procedure uses the Power Parameters [4, 5, 3] of MultiMatch which provide flexibility and versatility when looking for optimum P_{1dB} performance in a desired bandwidth.

In order to follow this procedure, an S -parameters data file was generated first by using the nonlinear model in Microwave

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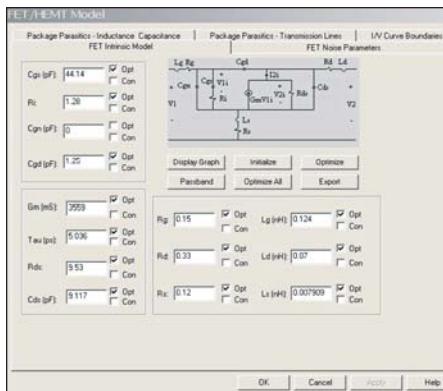


Figure 1 . GaAs MESFET linear model.

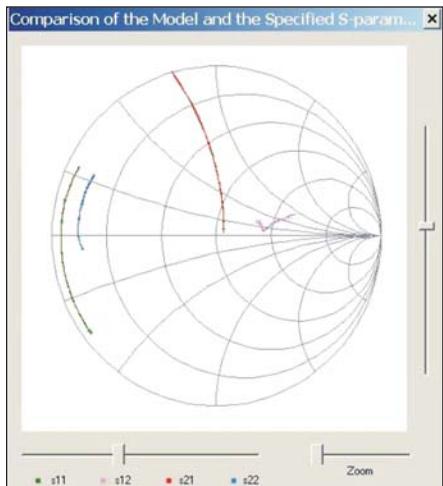


Figure 2 . Graph showing the result of the fitting.

Office. This file was then used in MultiMatch to fit a linear model to the S -parameters, which together with defined I/V Curve Boundaries and bias point, allows MultiMatch to calculate the power performance. The model fitted is used to generate the required Power Parameters. Figures 1 and 2 show the component values of the fitted linear model and graphs of the S -parameters of the model and the measured S -parameters. Note the tight fit between the two sets of S -parameters.

The model extraction was done inside the Transistor/Device Modification Module of MultiMatch. The model fitting was followed by a general analysis of the capabilities of the

Frequency (GHz)	k	MAG (dB)	MSG (dB)	G_a (dB)	G_w (dB)	G_T (dB)
100.0000E-3	0.08	infinity	32.65	29.19	34.55	24.39
151.2341E-3	0.12	infinity	30.65	26.13	30.95	21.04
199.2583E-3	0.15	infinity	29.45	23.93	28.56	18.73
301.3467E-3	0.23	infinity	27.65	20.49	24.97	15.21
397.0388E-3	0.31	infinity	26.42	18.15	22.58	12.85
499.6184E-3	0.38	infinity	25.44	16.20	20.60	10.88
600.4581E-3	0.46	infinity	24.61	14.63	19.01	9.30
791.1329E-3	0.60	infinity	23.39	12.30	16.64	6.96
908.0980E-3	0.68	infinity	22.77	11.14	15.47	5.80
995.5313E-3	0.75	infinity	22.39	10.38	14.69	5.03
1.14270	0.85	infinity	21.74	9.24	13.52	3.90
1.19650	0.90	infinity	21.55	8.86	13.13	3.52
1.31170	0.96	infinity	21.10	8.12	12.36	2.78
1.37340	1.00	20.56	20.56	7.75	11.98	2.41
1.43790	1.04	19.36	19.36	7.38	11.60	2.05
1.50560	1.09	18.63	18.63	7.02	11.23	1.69
1.57640	1.13	18.01	18.01	6.66	10.85	1.34
1.65050	1.17	17.49	17.49	6.31	10.48	1.00
1.72820	1.22	16.95	16.95	5.96	10.11	0.66
1.80950	1.26	16.46	16.46	5.62	9.75	0.32
1.89460	1.29	16.01	16.01	5.28	9.39	-0.00
1.98370	1.34	15.53	15.53	4.94	9.03	-0.32
2.07700	1.38	15.08	15.08	4.62	8.68	-0.62
2.17470	1.41	14.66	14.66	4.30	8.33	-0.92
2.27700	1.45	14.24	14.24	4.00	7.99	-1.19
2.38410	1.48	13.82	13.82	3.70	7.66	-1.45
2.49620	1.51	13.41	13.41	3.41	7.33	-1.70
2.61360	1.53	13.01	13.01	3.13	7.02	-1.93
2.73650	1.54	12.63	12.32	2.88	6.72	-2.12
2.86520	1.56	12.26	12.26	2.64	6.44	-2.29
3.00000	1.57	11.87	11.87	2.41	6.16	-2.44

Table 1 . GaAs MESFET k -factor and gain.

transistor. The results are shown in Tables 1 and 2.

Before anything else first the stability of the amplifier stage should be considered. In this case, because the transistor k -factor (Table 1) shows unconditional stability (>1) above about 1.4 GHz, it was decided to synthesize the output and input networks first and then add an input shunt resistor, at an appropriate place, to take care of the instability at the lower frequencies.

Table 2 shows the maximum Output Power ($P_{o\text{-max}}$) obtainable before the intrinsic output current or

voltage starts to clip. This power is a close estimate of the maximum $P_{1\text{dB}}$ of the transistor, but more importantly the output impedance and the Load-Pull Contours for this unclipped $P_{o\text{-max}}$ are the same as those for $P_{1\text{dB}\text{-max}}$ [6, 7, 4, 5]. Normally P_o simulated by MultiMatch should be slightly lower than the actual $P_{1\text{dB}}$ or the $P_{1\text{dB}}$ simulated with a nonlinear model. At the $P_{1\text{dB}}$ point on the compression curve there is already some clipping. Table 1 also shows the optimum impedance ($Z_{L\text{-opt}}$) at which $P_{o\text{-max}}$ ($P_{1\text{dB}\text{-max}}$) is achieved and the associated maxi-

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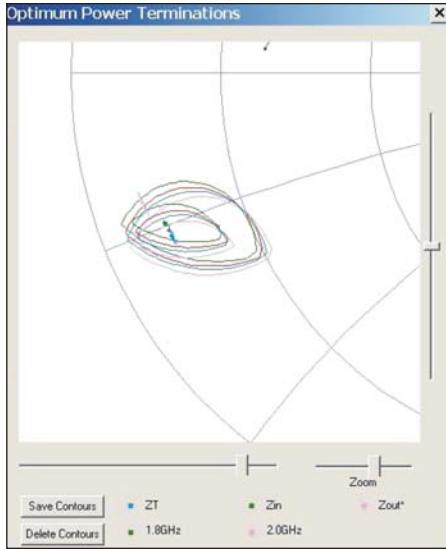


Figure 3 . GaAs MESFET load-pull vointours for P_o/P_{1dB} .

mum power gain ($G_{p\text{-max}}$). $G_{p\text{-max}}$ is the power gain of the transistor when its output is matched for $P_{o\text{-max}}$ and its input for maximum input Return Loss (RL_{in}).

The next few steps of the design procedure follow closely the procedure described in [1]. It was decided to try and see what P_o could be achieved in the frequency band of 1.8-2 GHz. The MultiMatch command for synthesis of a network which provides the optimum impedance for $P_{o\text{-max}}$ was invoked and that starts an impedance set-up wizard. One of the steps of the wizard's procedure shows in graphical form (Fig. 3) the Load-Pull contours of P_o (P_{1dB}). The blue line in the middle of the ellipsoids represents the optimum impedances ($Z_{L\text{-opt}}$) at which $P_{o\text{-max}}$ is achieved. The ellipsoid contours are spaced and grouped for 1 dB and 2 dB less power. The different colour of each individual contour in each group represents a different frequency. (The magenta line shown represents the impedances for maximum gain. If these impedances are presented to the output of the transistor then the gain will be the maximum possible, but P_o will be more than 2 dB less than the maxi-

Frequency (GHz)	Load Termination (ohm)	Output Power (dBm)	Power Gain (dB)
1.43790	3.65	-j3.87	39.669
1.50560	3.62	-j4.11	39.665
1.57640	3.59	-j4.36	39.661
1.65050	3.57	-j4.64	39.656
1.72820	3.54	-j4.93	39.650
1.80950	3.65	-j5.32	39.660
1.89460	3.90	-j5.79	39.668
1.98370	3.47	-j5.98	39.630
2.07700	3.45	-j6.40	39.622
2.17470	3.43	-j6.85	39.612
2.27700	3.42	-j7.35	39.602
2.38410	3.41	-j7.90	39.590

Table 2 . $Z_{L\text{-opt}}$, P_o and G_p .

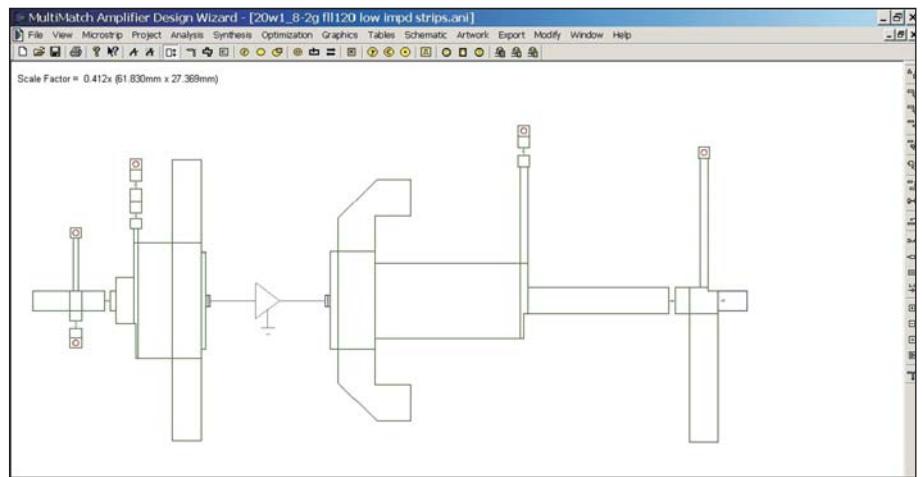


Figure 4 . The first MultiMatch layout solution for the GaAs MESFET stage.

mum.) The purpose of this wizard is to set the target impedance for the synthesis which in this case was set to be $Z_{L\text{-opt}}$.

A number of iterations were then run in the network synthesis module of MultiMatch with different main-line (series) impedances to arrive at the highest P_o with the most tolerance insensitive network behavior. This capability of MultiMatch to provide immediate tolerance sensitivity evaluation of the multiple synthesis choices presented to the designer is a strong advantage. It increases the chances very substantially that the design iteration will be successful

when a yield analysis is done at the end of the full design cycle. The chosen solution of the synthesis session was transferred to the analysis module where the analysis showed P_o just 0.3-0.5 dB lower than $P_{o\text{-max}}$. The input matching network was synthesized next and Figure 4 shows the resulting layout of the MultiMatch solution.

This layout was translated into Microwave Office schematic and layout, and then, as described in [3], electromagnetic analysis and tuning were attempted to compensate for the effects of the microstrip discontinuities. When this design was done,

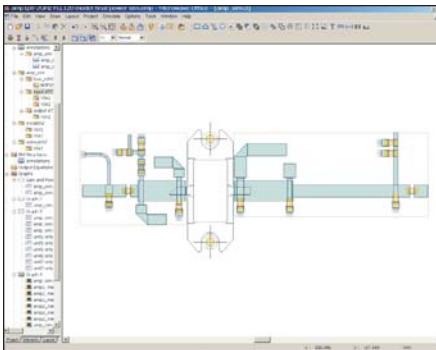


Figure 5 . Final GaAs MESFET stage layout.

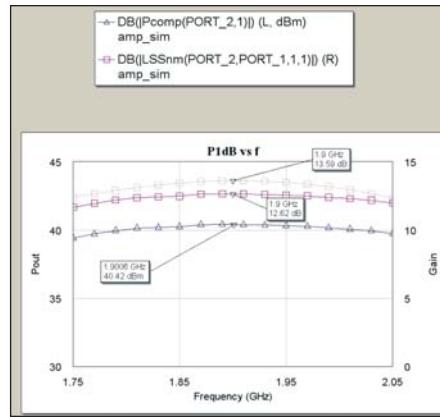


Figure 6 . P_{1dB} simulation.

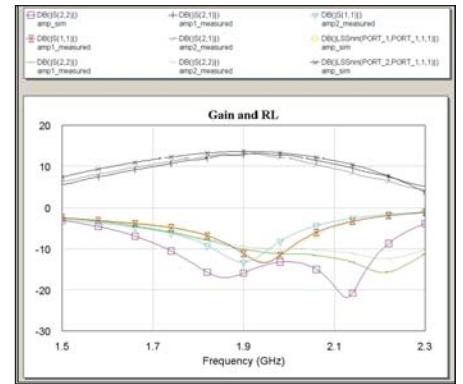


Figure 7 . Gain and R_L comparison.

MultiMatch discontinuities models were of the closed-form type based on models from the literature and they could not fully compensate for the discontinuities effects of this very high dimensions ratio layout which is typically necessary with high power amplifiers. In this case it turned out that the discontinuities effects could not be tuned out for the whole bandwidth of 1.8-2 GHz. This bandwidth is more than twice wider in percentage than the design bandwidth in [3] (2.1-2.2 GHz).

It was obvious that the solution of the problem should be sought in reducing the width of the main-line (series) microstrip lines, although this would bring more tolerance sensitivity. The widest lines were set to be 3 mm because in Microwave Office the standard electromagnetically solved discontinuity X-models range allows width to height ratios (W/H) up to 4.0. W is the microstrip line width and H is the substrate height which in this case is 0.762 mm (30 mil) with $\epsilon_r = 3.88$. The newly synthesized MultiMatch design showed good performance and when translated into Microwave Office only very minor tuning was necessary for optimum performance. Because the discontinuities X-models were used it was decided not to perform an electromagnetic simulation of the layout. Figure 5 shows the layout of this design iteration in Microwave Office and Figure 6 shows the simulated

P_{1dB}.

Two test units were built and measured. Figure 7 shows the comparison between the simulated and measured performance for Gain and R_L.

The somewhat different output R_L did not affect the P_{1dB} measured performance. It was startlingly the same as the simulated P_{1dB}. The simulated Output IP3 is 55.5 dBm and the measured values are 55.8 dBm and 58 dBm for the two different units which is also a very close agreement.

The designed stage was used to design a balanced stage to which a balanced 5W driver was added to realize a 20W Class A amplifier with very high linearity performance (OIP3 = 58 dBm). It has consistently come out of production without any necessity to tune.

It should be mentioned here that substrate specific X-models for wider lines could have been generated using the X-model development facility provided in Microwave Office, and then more iterations could be run between MultiMatch and Microwave Office to see if there was not a solution with wider main-line (series) lines (lower characteristic impedances) which would still work for the 1.8-2 GHz bandwidth, but would also provide less tolerance sensitivity. This of course would have taken more design time.

At the time of writing this paper

MultiMatch acquired a new discontinuity modeling module in which substrate specific models can be developed by the user in a similar manner as the X-model facility of Microwave Office. For the MultiMatch discontinuities model development though, a third party 2.5D electromagnetic simulator has to be used and instead of a data base to be filled as in Microwave Office, coefficients for polynomial curve fits of the components in pre-determined equivalent circuits must be provided. It is the Microwave Office X-models facility that provides in the fastest manner the information for the MultiMatch discontinuity models.

The MultiMatch discontinuity modeling module has already been tested up to 50 GHz. It is a time consuming operation to produce substrate specific discontinuity models, but when it is done it is usually not necessary to run multiple iterations between MultiMatch and Microwave Office to compensate for the discontinuities effects.

The GaN HEMT Design

The design of the stage with the GaN HEMT proceeded in a very similar manner though with some important differences. First, simulations with the nonlinear model using tuners in Microwave Office showed maximum P_{1dB} of 40.6 dBm. Then S-parameters file was generated and in MultiMatch linear model was fit-

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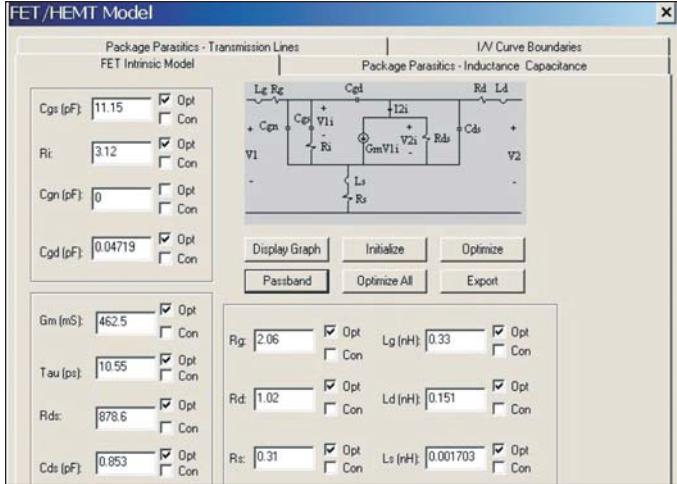


Figure 8 · GaN HEMT linear model.

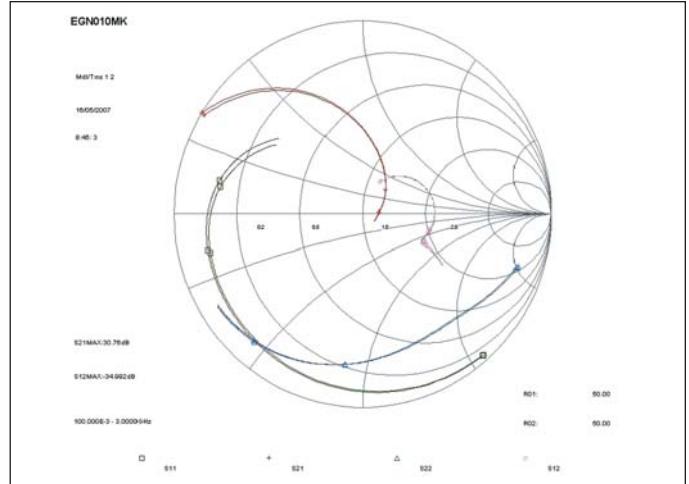


Figure 9 · GaN HEMT S-parameters vs. linear model.

ted to the S-parameters (Figures 8 and 9).

The parasitic capacitances in the linear model have much smaller values than the GaAs MESFET ones and the parasitic drain-source resistor is much bigger. The optimum intrinsic load (across the voltage-current generator), R_{L-opt} , of the GaN HEMT is about 100 ohm while the GaAs MESFET one is about 4.5 ohm (calculated by the Load-line method). All of this indicates that the GaN HEMT will have much wider bandwidth performance. The general capabilities analysis (Table 3) indicates that this transistor has much higher gain capabilities, but that comes at the price of substantial instability—the k -factor is bigger than one only between 3 and 4 GHz. So the next step was to use the MultiMatch modification network synthesis capability to design a network at the input of the transistor that would, before everything, provide unconditional stability at all frequencies, but also would simultaneously level the gain, reduce the input miss-match and consequently widen the bandwidth and provide tolerance insensitivity of the performance of the stage. It should be obvious that such a network would contain resistors. With an initial guess about the bandwidth capabilities of the transis-

Frequency (GHz)	k	MAG (dB)	MSG (dB)	G_a (dB)	G_w (dB)	G_T (dB)
100.0000E-3	0.04	infinity	37.05	36.67	43.15	30.61
300.0000E-3	0.13	infinity	32.31	30.07	33.50	26.50
500.0000E-3	0.22	infinity	30.09	26.05	28.86	22.85
700.0000E-3	0.30	infinity	28.65	23.33	25.65	19.98
799.9999E-3	0.35	infinity	28.07	22.27	24.33	18.75
1.00000	0.44	infinity	27.14	20.52	22.04	16.62
1.20000	0.53	infinity	26.37	19.16	20.08	14.82
1.40000	0.62	infinity	25.71	18.07	18.36	13.29
1.60000	0.71	infinity	25.14	17.21	16.84	12.00
1.80000	0.79	infinity	24.60	16.53	15.48	10.92
2.00000	0.87	infinity	24.09	16.00	14.26	10.04
2.20000	0.94	infinity	23.59	15.61	13.16	9.33
2.40000	0.99	infinity	23.09	15.36	12.19	8.79
2.60000	1.03	21.49	21.49	15.22	11.32	8.41
2.80000	1.06	20.54	20.54	15.19	10.55	8.15
3.00000	1.08	19.81	19.81	15.26	9.88	8.02
3.20000	1.07	19.27	19.27	15.39	9.31	7.99
3.40000	1.07	18.79	18.79	15.54	8.83	8.00
3.60000	1.05	18.44	18.44	15.63	8.45	8.02
3.80000	1.03	18.20	18.20	15.55	8.16	7.99
4.00000	1.01	18.26	18.26	15.18	7.97	7.88
4.20000	0.98	infinity	18.14	14.45	7.90	7.65
4.40000	0.95	infinity	17.61	13.37	7.95	7.32
4.60000	0.92	infinity	17.08	12.05	8.12	6.94
4.80000	0.89	infinity	16.56	10.60	8.45	6.55
5.00000	0.86	infinity	16.06	9.12	8.96	6.15
5.20000	0.84	infinity	15.58	7.66	9.70	5.72
5.40000	0.81	infinity	15.11	6.26	10.72	5.15
5.50000	0.80	infinity	14.88	5.58	11.37	4.75

Table 3 · GaN HEMT k -factor and gain.

High Frequency Design

COMPARING GaAs/GaN

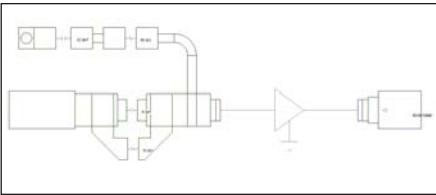


Figure 10 . GaN HEMT modification network.

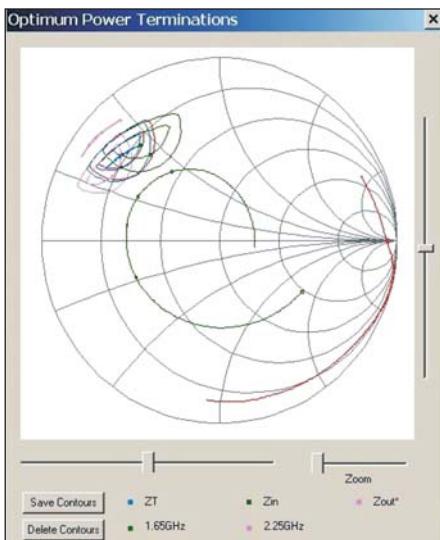


Figure 11 . GaN HEMT load-pull contours for P_{1dB} .

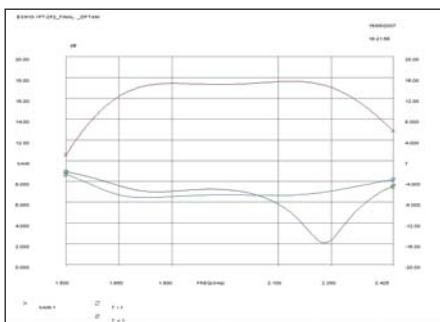


Figure 12 . GaN HEMT G_p and R_L .

tor of 1.6-2.3 GHz such a modification network was synthesized and Figure 10 shows it in layout form.

Table 4 presents the results of the capabilities analysis, this time of the entire circuit of Figure 10. The table shows the optimum load (Z_{L-opt}) for the maximum pre-clipped output power $P_{o,max}$, $P_{o,max}$ itself, and the associated maximum $G_{p,max}$.

DMS—Stage Z_L , P_o and Gain (P_{oM}):

Frequency (GHz)	Load Termination (ohm)	Output Power (dBm)	Power Gain (dB)
1.60000	10.99	+j23.83	39.976
1.70000	10.48	+j23.07	39.981
1.80000	9.86	+j22.12	39.971
1.90000	8.91	+j20.31	39.969
2.00000	8.41	+j19.34	39.962
2.10000	7.98	+j18.48	39.952
2.20000	7.55	+j17.53	39.940
2.30000	7.17	+j16.60	39.929

Table 4 . GaN HEMT Z_{L-opt} , P_o and G_p .

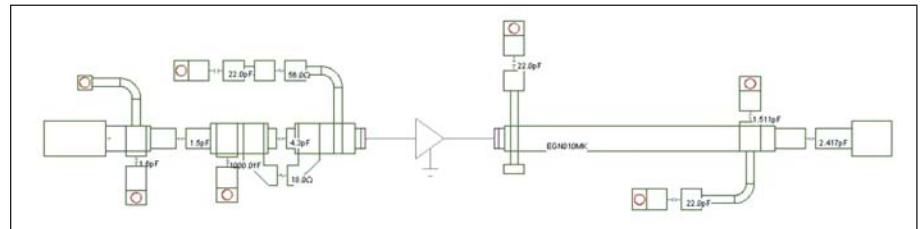


Figure 13 . GaN HEMT stage MM layout.

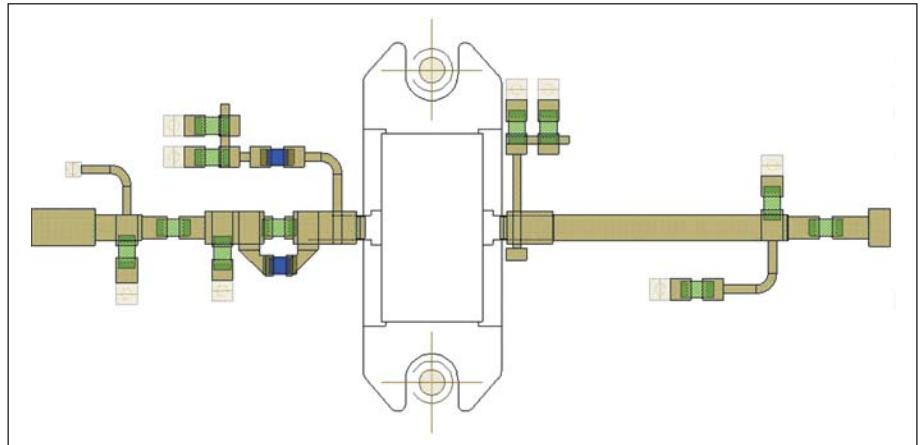


Figure 14 . GaN HEMT stage MWO layout.

Then the output network was synthesized by searching for a bandwidth in which P_o would be no more than 0.5 dB less than $P_{o,max}$ of Table 4. This was achieved for 1.7-2.2 GHz which is also a very useful frequency range covering all the cell/mobile phone frequency bands. Figure 11 presents the GaN HEMT Load-Pull contours for the 1.7-2.2 GHz band-

width. The blue line again was the targeted by the synthesis Z_{L-opt} .

Figure 12 presents the G_p and the input and output R_L after the input matching network was added. Figure 13 shows the layout in MultiMatch, and Figure 14 shows it after it was transferred into Microwave Office. As it can be seen, the series microstrip lines have much higher characteristic

impedances, which reflects the much higher transistor impedances and the wider bandwidth that can be achieved compared to the GaAs MESFET case.

The circuit in Microwave Office was very slightly tuned and it simulated P_{1dB} of better than 40.2 dB over the 1.7-2.2 GHz bandwidth (Figure 15). Figure 16 compares the G_p and R_L between the simulated and the measured performance of the first two test units that were built. No tuning was applied to the test units.

The simulated gain is about 1.5 dB higher than the measured values but with the same shape. It was even 2 dB higher before the operational temperature in the nonlinear model was adjusted up by a whole 30°C to counter for the non-perfect heat-sinking of the test units. Also the measured output IP3 in this case is 49.5 dBm while the simulated output IP3 of 58 dBm is overly optimistic. It is

difficult to establish the reason for these differences without more data.

What is important though is that the measured P_{1dB} of both units again came charmingly on top of the simulated P_{1dB} . So as a whole, the combination of the nonlinear model and the design approach provided in effect a first-time-right design. Figure 17 shows a photograph of one of the GaN HEMT test units. The GaAs MESFET test units look very similar.

Summary and Conclusions

As expected the GaN HEMT showed much broader bandwidth and higher gain capabilities. The GaAs MESFET though showed exceptionally good linearity. It is as if it has a linearizer integrated in its structure. The relatively poor linearity performance of the GaN HEMT in a Class A amplifier realization is not necessarily a bad thing. The non-impres-

sive third-order distortion levels could possibly correspond to a gradual gain compression curve which together with the much lower parasitics would allow for very good and easy to achieve pre-distortion type linearization. The lower parasitics are really of great advantage when the GaN HEMTs are used in the heavy nonlinear switch-mode amplifier applications (E, D, F) and for envelope biased Class AB applications, both of which are providing exceptional efficiency. The latter ones are also easily linearized by digital pre-distortion. There are already numerous technical and scientific publications on these matters. There is a great excitement in the industry about utilizing the advantages the wide bandgap transistors are offering. Mass product applications are coming, competition is boiling up and hopefully the current high cost of the GaN transistors will come down soon.

High Frequency Design

COMPARING GaAs/GaN

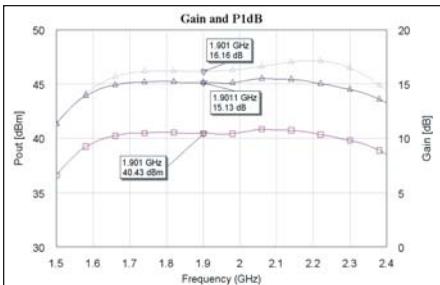


Figure 15 . GaN HEMT stage MWO simulated $P_{1\text{dB}}$:

The GaAs MESFET nonlinear model used is very good. The GaN HEMT model is good enough for this application. With the SiC and GaN microwave transistors that have come recently on the market most of the transistor manufacturers are finally warming up to the necessity of providing good and really usable nonlinear models. There are also companies like Modelithics and Auriga Measurement Systems that provide modeling services.

Once again as in [2] and [3] it was shown that the dedicated to amplifier design MultiMatch with its unique Power Parameters and practical real life network synthesis capabilities guarantees first-time-right and optimum performance designs in very short design cycles. It should be emphasized though that MultiMatch is really effective if the users have a thorough understanding of amplifier and matching network basics and are determined to develop superior products. It is not a design tool for Dummies! Even for experienced amplifier designers, MultiMatch, with its unique amplifier synthesis design approach, will provide insights and solutions which are impossible when using just a general simulator/optimizer type software programs. At the same time the software also provides a path for inexperienced users with good fundamental knowledge to learn and realize quickly practical and effective amplifier designs.

Microwave Office was an integral

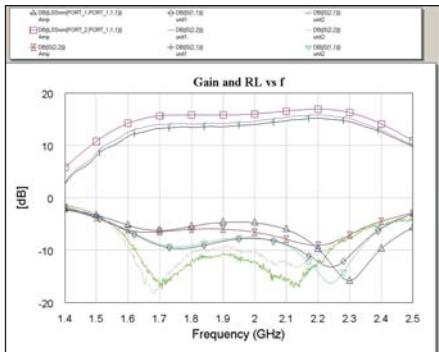


Figure 16 . GaN HEMT stage simulated and measured G_p and R_L .

part of the design procedures described here. As a general RF/microwave simulator it is very user-friendly and with its open design environment it provides easy interoperability with third-party design tools. As one of the very broad range of interconnected RF/microwave electronic design automation products of AWR its solutions can be integrated and used further in the simulations for the development of more complex systems.

References

1. Sonoko Akamatsu, Charles Baylis, and Larry Dunleavy, "Accurate Simulation Models Yield High-Efficiency Power Amplifier Design," *IEEE Microwave Magazine*, December 2005.
 2. Ivan Boshnakov, Jon Divall, "Tandem RF software programs streamline the design of power amplifiers," website feature on *Planet Analog*, and *Microwave Engineering Europe*, December 2002, <http://www.mwee.com/features/showArticle.jhtml?articleID=12802301>.
 3. Ivan Boshnakov, "First time right design of Class A power amplifiers using the novel power parameters," *Microwave Engineering Europe*, February 2005, <http://i.cmpnet.com/mwee/archive/feb05/mwee0205p30.pdf>
 4. MultiMatch Amplifier Design Wizard, Stellenbosch: Ampsa (Pty) Ltd.; <http://www.ampsap.com>.

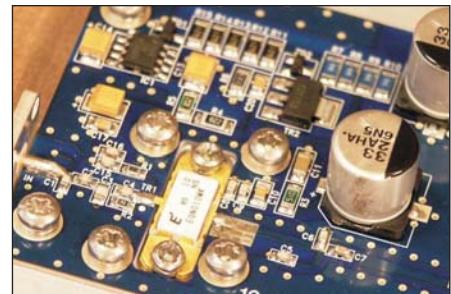


Figure 17 . GaN HEMT test unit photo.

5. Abrie, Pieter L.D., *Design of RF and Microwave Amplifiers and Oscillators*, Artech House, 2000, ISBN 0-89006-797-X
 6. Cripps, S.C., "A Theory for the Prediction of GaAs Load-Pull Power Contours," *IEEE-MTT-S Int'l. Microwave Symposium Digest*, 1983, pp 221-223.
 7. Cripps, S.C., *RF Power Amplifiers for Wireless Communications*, Artech House, 1999, ISBN 0-89006-989-I.

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A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs

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(Invited Paper)

Abstract—Gallium-nitride power transistor (GaN HEMT) and integrated circuit technologies have matured dramatically over the last few years, and many hundreds of thousands of devices have been manufactured and fielded in applications ranging from pulsed radars and counter-IED jammers to CATV modules and fourth-generation infrastructure base-stations. GaN HEMT devices, exhibiting high power densities coupled with high breakdown voltages, have opened up the possibilities for highly efficient power amplifiers (PAs) exploiting the principles of waveform engineered designs. This paper summarizes the unique advantages of GaN HEMTs compared to other power transistor technologies, with examples of where such features have been exploited. Since RF power densities of GaN HEMTs are many times higher than other technologies, much attention has also been given to thermal management—examples of both commercial “off-the-shelf” packaging as well as custom heat-sinks are described. The very desirable feature of having accurate large-signal models for both discrete transistors and monolithic microwave integrated circuit foundry are emphasized with a number of circuit design examples. GaN HEMT technology has been a major enabler for both very broadband high-PAs and very high-efficiency designs. This paper describes examples of broadband amplifiers, as well as several of the main areas of high-efficiency amplifier design—notably Class-D, Class-E, Class-F, and Class-J approaches, Doherty PAs, envelope-tracking techniques, and Chireix outphasing.

Index Terms—Broadband, gallium nitride (GaN), high efficiency, monolithic microwave integrated circuit (MMIC), power amplifier (PAs), power transistor, silicon carbide.

I. INTRODUCTION

WIDE-BANDGAP semiconductor technology for high-power microwave devices has matured rapidly over the last several years as evidenced by the fact that AlGaN/GaN HEMTs have been available as commercial-off-the-shelf (COTS) devices since 2005. The material properties of GaN compared to competing materials are presented in Table I. AlGaN/GaN HEMTs possess high breakdown voltage, which allows large drain voltages to be used, leading to high output impedance per watt of RF power, resulting in easier matching and lower loss matching circuits. The high

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TABLE I
MATERIAL PROPERTIES OF MICROWAVE SEMICONDUCTORS [1]

Material	Mobility, μ , $\text{cm}^2/\text{V}\cdot\text{s}$	Dielectric Constant, ϵ	Bandgap, E_g , eV	Break down field, E_b $10^6\text{V}/\text{cm}$	BFOM Ratio	Tmax, $^{\circ}\text{C}$
Si	1300	11.9	1.12	0.3	1.0	300
GaAs	5000	12.5	1.42	0.4	9.6	300
4H-SiC	260	10	3.2	3.5	3.1	600
GaN	1500	9.5	3.4	2	24.6	700

BFOM is Baliga's figure of merit for power transistor performance ($\mu \cdot \epsilon \cdot E_g^3$)

TABLE II
IMPACT OF GaN ON PA CONCEPTS

Concept	Silicon	GaN on SiC
Class E/F/J	Low f_T , moderate breakdown voltage	High f_T , high breakdown voltage
Doherty	Low off-state impedance, high output capacitance	High off-state impedance, low output capacitance
LINC	Large non-linear output capacitance	Small non-linear output capacitance
EER/ET	Poor amplitude to phase modulation conversion, moderate bandwidth	Good amplitude to phase modulation conversion, large bandwidth
Digital Pre-Distortion	High thermal time constant, moderate bandwidth	Low thermal time constant, large bandwidth

sheet charge leads to large current densities and transistor area can be reduced resulting in high watts per millimeter of gate periphery. The high saturated drift velocity leads to high saturation current densities and watts per unit gate periphery. In turn, this leads to lower capacitances per watt of output power. Low output capacitance and drain-to-source resistance per watt also make GaN HEMTs suitable for switch-mode amplifiers.

Research and development of GaN HEMTs gained considerable momentum in the late 1990s and early 2000s when it became possible to reproducibly grow high-quality 4H-SiC substrates [2], [3]. In particular, GaN HEMT technologies have had a significant impact on various power amplifier (PA) concepts, as outlined in Table II [4] where a comparison is made between silicon LDMOSFETs (the “incumbent” technology for many applications) and GaN on SiC HEMTs.

High total RF powers from GaN HEMT transistors over a wide frequency range have been reported for single die up to several hundred watts [5], [6]. However, these high power densities, in terms of watts per millimeter, also present extreme power dissipation demands on both the transistor layouts, as

well as the semiconductor substrates. Fortunately, the high thermal conductivity of SiC substrates ($>330 \text{ W/m} \cdot \text{K}$) allows these high power densities to be efficiently dissipated for realistic drain efficiencies, preventing the extreme channel temperatures that would result due to self-heating with other substrate technologies. For example, a commercially available 120-W discrete transistor (Cree CGH40120F) operating at 28 V will generate 120 W of continuous wave (CW) RF power, and at its saturated output power, has a drain efficiency of 65%. With a rated CW thermal resistance of $1.5 \text{ }^{\circ}\text{C/W}$, the dissipated power is 64 W with a channel temperature rise of $96 \text{ }^{\circ}\text{C}$ allowing the device to comfortably operate at baseplate temperatures in excess of $100 \text{ }^{\circ}\text{C}$. The effective pulsed thermal resistances of such devices are also lower (dependent on pulselwidth and duty factor)—this aspect will be covered in Section IX.

In summary, GaN offers a rugged and reliable technology capable of high-voltage and high-temperature operation. This opens up many industrial, defense, medical, and commercial applications that can be targeted by GaN.

II. OVERVIEW OF TECHNOLOGY

Early progress on GaN/AlGaN HEMT technology in the 1990s was concentrated on three main areas, including improving epitaxial layer material quality, selecting the best substrate materials, and developing unit processes (e.g., [7]). Many of the advances in hetero-epitaxy of GaN and AlGaN were based on early metal–organic chemical vapor deposition (MOCVD) work in the field of opto-electronics [8]. However, both molecular beam epitaxy (MBE) and MOCVD growth methods were perceived as viable for GaN-based electronics devices [9], [10]. Most of the advancements in epitaxial growth were first achieved on sapphire due to its availability, but commercial ventures for GaN HEMT devices have all adopted either Si as a “low-cost” substrate or semi-insulating 6H- or 4H-SiC for superior high-power performance and thermal management. State-of-the-art power levels have been demonstrated on SiC substrates with total output powers of 800 W at 2.9 GHz [6] and over 500 W at 3.5 GHz [11].

The performance benefits for these devices are remarkable due to their ability to make heterostructures in a material system that also supports high breakdown fields. This has provided the key components necessary for high breakdown voltage and high transconductance device results as the technology advanced in the mid 1990s [10]. Clear understanding of the phenomenon of 2DEG carrier densities greater than $1 \times 10^{13}/\text{cm}^2$ was achieved after strain- and polarization-induced charges were clearly explained [11]. Subsequent device structure and processing enhancements led to the first results of passivated GaN HEMTs with results showing the clear thermal advantage of using SiC as a substrate instead of sapphire for high total RF power [14] and [15].

The epilayers for Cree commercial HEMTs are grown by MOCVD in a high-volume reactor on 100-mm semi-insulating 4H silicon carbide (SI 4H-SiC) substrates that are cut on-axis. The epitaxial growth process is highly reproducible and in production for several years, in part due to the funding on the Defense Advanced Research Projects Agency (DARPA) Wide Bandgap Semiconductor (WBGS) Program that was initiated

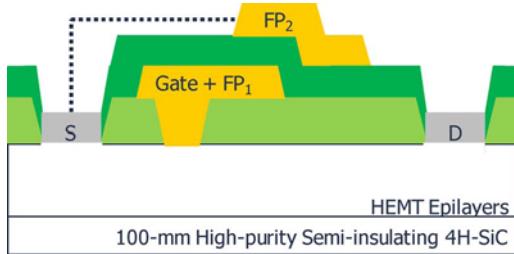


Fig. 1. Schematic cross section of the AlGaN/AlN/GaN HEMT RF structure showing integrated first field plate and source-connected second field plate.

in 2002 [16]. Typical structures comprise an AlN nucleation layer, $1.4 \mu\text{m}$ of Fe-doped insulating GaN, approximately 0.6 nm of an AlN barrier layer, and a 25-nm cap layer of undoped $\text{Al}_{0.22}\text{Ga}_{0.78}\text{N}$. This nominal layer thickness and mole fraction yield sheet electron concentrations in the range of 8 to $10 \times 10^{12}/\text{cm}^2$, but due to the AlN interlayer has the strong advantage of electron mobilities near $2000 \text{ cm}^2/\text{V} \cdot \text{s}$ at room temperature [17]. The channel sheet resistance is about 335Ω per square.

As shown in the schematic cross section of Fig. 1, the device is fabricated with ohmic contacts that are formed directly on the top AlGaN layer. Device isolation is achieved using nitrogen implants to achieve a planar structure [18]. Gate electrodes are formed by recessing through a first SiN dielectric to the AlGaN and then depositing Ni/Pt/Au metallization. Very strong peak electric fields occur at the drain-side edge of the metal semiconductor junction in this lateral device. The optimized device includes a lateral extension of the gate electrode on the drain side to provide an elegant integration of field shaping with the gate metallization. The gate footprint is offset to reduce source resistance and increase gate-to-drain breakdown voltage. The gate length of the device is nominally $0.4 \mu\text{m}$, and the gate-to-drain spacing is about $3 \mu\text{m}$. After a second passivation, a source connected second field plate is fabricated to provide further electric field shaping at the highest drain voltages and to reduce gate to drain feedback capacitance of the device [19], [20]. The 1-mA/mm (gate current) breakdown voltage of this structure exceeds 150 V. Unit cell devices exhibit CW on-wafer output power levels of 4–5 W/mm when measured on a load–pull bench at 28 V and 3.5 GHz. The gate connected second field plate together with integrated first field plate has become the most widespread device structure in the industry for RF applications below 20 GHz.

Microwave monolithic circuit demonstrations were an early goal of those developing the technology. Besides Cree Inc., a number of other GaN MMIC foundries provide similar technologies such as Triquint, Raytheon, and Hughes Research Laboratories. After the basic transistor device is completed, standard passive components such as metal–insulator–metal (MIM) capacitors, thin-film resistors, and through-wafer slot vias are utilized in the Cree Inc. process to achieve high-performance versatile monolithic microwave integrated circuit (MMIC) products (Fig. 2). The MIM capacitors have been developed to support peak voltages greater than 100 V. SiC substrate vias has allowed the straightforward implementation of the amplifier circuits without the need of cumbersome

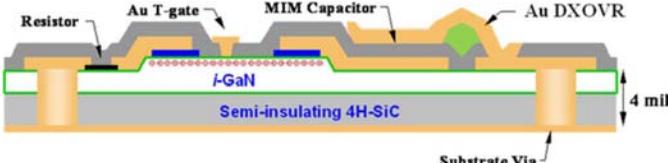


Fig. 2. Schematic cross section of typical GaN HEMT MMIC process.

coplanar waveguide grounding schemes. Specifically, slot vias are implemented in the 100- μm -thick SiC substrates to simplify layout and increase gain. Three types of resistors are available: nichrome thin film with 12- Ω/square resistance and two “bulk” GaN resistors with 70- and 400- Ω/square resistance. Bulk GaN resistor layers are covered by thick dielectric insulators, enabling metal crossovers. A 0.4- μm gate-length 28-V process provides 4.5 W/mm of gate periphery for circuits between dc to 8 GHz, while a 0.25- μm gate-length 40-V process provides 7 W/mm of gate periphery between dc and 18 GHz.

III. GaN HEMT LARGE-SIGNAL MODELING

Field-effect transistor (FET) models have a long history. In Shockley’s original FET work, a physical representation was derived to predict operation of the junction field-effect transistor (JFET). Models have evolved from this point to describe and design new field-effect devices and to facilitate their various uses. There have been many new device structures and circuits produced over the 60 years that have passed since Shockley’s work, as well as an equally impressive list of modeling approaches. This branching of FET lineage has been driven by both military and civilian radar and communication system needs. In addition, various types of device models have been developed depending on application. An area of intense focus for both device and model development has been that of high-efficiency PAs. System cost is driven by prime power and cooling requirements and improved efficiency is the key to reducing these costs. Improved power devices, along with proper measurements and models, have driven an increase in performance; hence, the focus of the presently described review.

Recently, most effort in PA design has been focused on GaAs pseudomorphic HEMTs (pHEMTs), Si LDMOSFETs, and GaN HEMTs. Models have been developed and adapted to these devices and share many common features because they are all field-effect structures. The focus of this study is to provide an example of this adaptation to the development of GaN HEMT models for MMIC and RF integrated circuit (RFIC) design. There have been excellent overviews of the state of modeling over the years. One recent example is by Dunleavy *et al.* [21]. The intent of this section of this paper is to present one possible solution to the modeling/design problem as applied to the GaN HEMT while acknowledging that there are many other viable solutions.

There are two general approaches to HEMT (or other active device) modeling. One is table based, the best known of which has been developed by Root. The table data can either be measured or simulated using 2-D physical simulators. An extension

of this work appears in [22]. A more recent version of this approach is the new X -parameter model formulation, which is based on significant small- and large-signal measurements [23]. This approach can be very accurate, but requires intensive measurement resources. To improve accuracy, the entire simulation space must be mapped using both large- and small-signal measurements including load-pull and linearity. It is certainly desirable to have the largest possible measurement database from which to extract and verify any model, but these measurements can be time consuming and expensive. A properly formulated model based on physical equations allows a reduction in required measurements without a significant loss in accuracy.

The second approach involves the description of the active device by closed-form physical equations, the parameters of which can be extracted from measured data. This is the approach chosen to support Cree Inc. device models and reported here. There has been much work over the past 60 years on this topic, ramping significantly with the advent of the GaAs MESFET in the late 1970s. The model described here uses various formulations, from published work, combined in such a way as to allow parameter extraction using a minimal set of measurements. An added aspect to the model development is verification using an extensive library of MMIC amplifier designs up to 20 GHz, as well as a large number of hybrid circuits using packaged devices. The model was originally developed specifically for MMIC design, thus allowing continuous improvements as MMICs were developed, measured, and simulations verified.

The starting point for the HEMT model is the drain current formulation. The basis for the $I_D(V_G, V_D)$ function is very similar to the formulation given by Statz *et al.* [24]. A common feature in the drain formulation of this model and other notable versions [25], [26] is the drain voltage saturation parameter

$$I_D \sim \tanh(\alpha * V_D).$$

A variant of this function is included in the present model together with a gate voltage parameter similar to that in [25]. Another feature, using work from [26], has proven useful in modeling drain current variations near pinch-off as

$$I_D \sim \beta(V_D - V_{DS0}).$$

A feature common to these drain current formulations, which caused an issue early in the work, was the lack of a gate voltage saturation mechanism. The original intent would be to limit channel current with forward gate conduction. This proved somewhat problematic in practice, particularly when high compression is used in high-efficiency PAs. The hyperbolic tangent function, ubiquitous in modeling, proved helpful in saturating $I_D(V_G)$. A well-known application is found in the Angelov (or Chalmers) model [27]. A deficiency in this approach became apparent in fitting GaN HEMT devices for both linearity and efficiency predictions. As shown in [24], the GaAs MESFET (and in the GaN HEMT as well) drain current obeys a square-law dependence on gate voltage near pinch-off. This can be approximated with a high-order polynomial argument within the tanh function, but this is difficult to fit and has shown convergence problems. Furthermore, compression both at pinch-off and open channel necessarily share characteristics

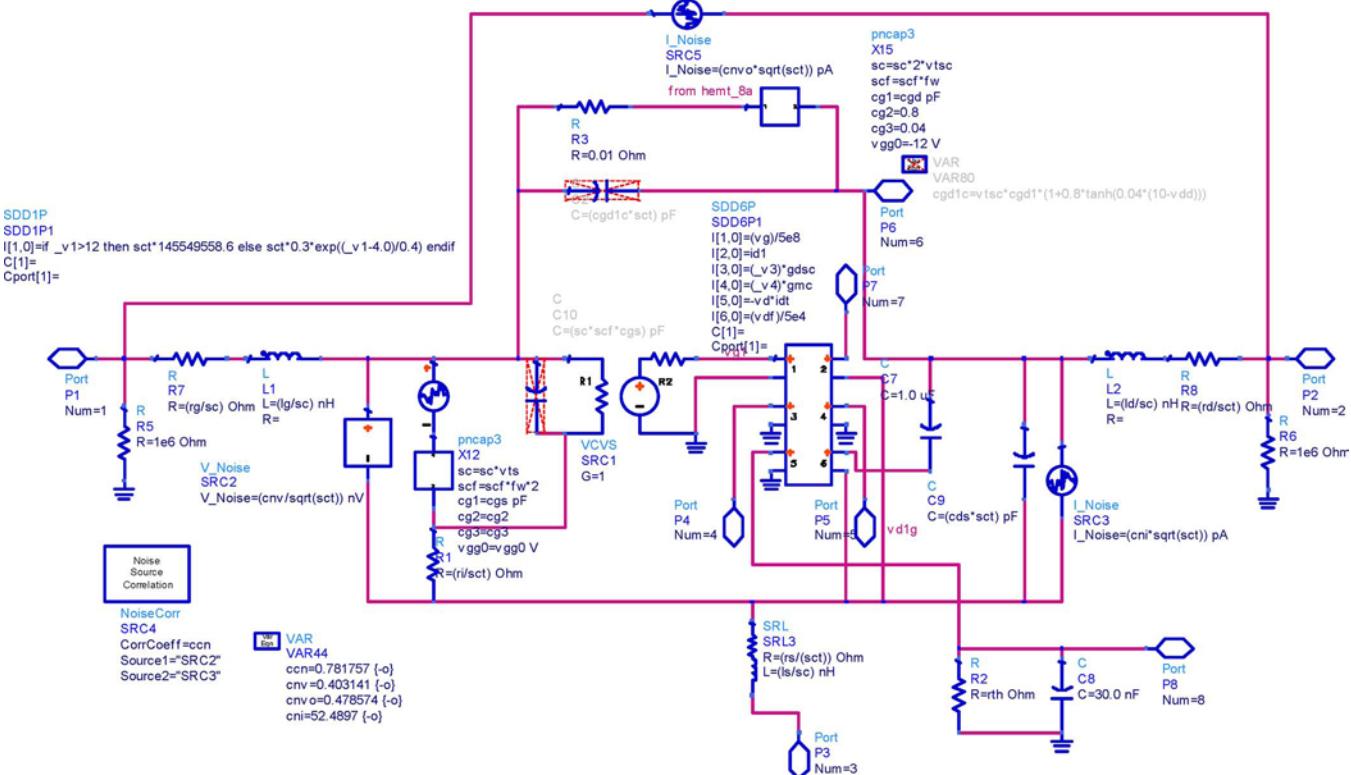


Fig. 3. HEMT SDD model schematic.

in the Angelov formulation. Experience did not show good fits either in linearity or high levels of compression. A reasonable solution for this problem has been proposed by Fager *et al.* [28] and the gate voltage compression expression allows the $G_M(V_G)$ function to be tailored separately from the square-law pinch-off allowing compression in a controlled and continuous manner.

The $I_D(V_G, V_D)$ characteristic also involves trapping and dispersive effects. Many device models are formulated to fit both transconductance and output conductance dispersion, as well as knee collapse, which is common in high-breakdown high-voltage devices. The Cree Inc. model uses the dc knee voltage as controlled by the α parameter to fit the observed RF knee without explicit fitting of the dc knee. This has not proven to be an issue in drain current prediction, nor has transconductance dispersion been shown to be a particular problem with GaN HEMT devices. Observations have shown output conductance dispersion to be an issue for self-consistent fits from small to large-signal operation. The solution for this problem has been found in the work of Jeon *et al.* [29]. Adding a small-signal perturbation to the $I_D(V_G, V_D)$ function separates the small-signal output conductance from the drain current slope providing a good fit over the range of input power.

The HEMT model schematic is shown in Fig. 3. This shows the drain current implemented in Agilent's Advanced Design System as a symbolically defined device (SDD). The overall structure is based on the standard 13-element small-signal FET model. Although there have been many corrections and additions to this model since development of the GaAs MESFET, the standard 13-element model is straightforward to fit and

lends itself well to simple voltage-dependent capacitance models. Inspection of the schematic shows that both C_{GS} and C_{GD} are functions of the terminal voltages and implemented as gate charge formulations. There is also a gate forward conduction diode based on the standard exponential characteristic. Proper modeling of forward conduction is essential to the prediction of over-compressed operation, particularly in the case of broadband amplifiers. Improvement of convergence dictates that the exponential function must be limited. In this case, some arbitrarily large hard limit can be chosen with detriment to convergence properties. The C_{GS} and C_{GD} voltage functions use the tanh function similar to Fager *et al.* [28]. Extensive modeling and load-pull fits show that C_{DS} does not need to dynamically vary with drain voltage, but should scale as drain voltage is changed for the wide-bandgap HEMT device.

The model as shown in Fig. 3 also includes noise calculation, is dependent on a dynamic thermal model based on channel dissipated power [30], and can be scaled for various unit cell configurations, as well as for parallel operation. The four noise sources represent the drain current noise and thermal noise from the FET internal resistances. Input and output noise is found to be correlated for the GaN HEMT. The model is partially based on the work of Lazaro *et al.* [31], as well as an empirical study of noise data [32]. The implementation as correlated noise sources simplifies the transition to a Verilog-A [33] translation used to develop models for both Agilent's ADS and AWR's Microwave Office simulators. The thermal model is based on a single-pole configuration, which provides for scaling as a function of dc dissipated power. Additional detailed thermal modeling can be performed using finite-element simulators and an

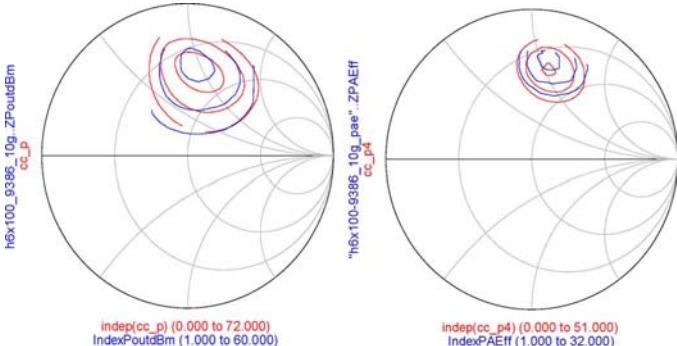


Fig. 4. Measured versus modeled load–pull contours (output power: left; PAE: right).

equivalent thermal resistance is defined for the electro-thermal model. Thermal resistance calculations can also be calculated analytically as demonstrated by Darwish *et al.* [34]. Thermal calculations are essential for GaN HEMT amplifier design due to the high dissipated power associated with high drain bias.

The model parameters are extracted from measured *S*-parameters over a range of bias values, as well as measured load–pull data. The thermal degradation has been characterized using pulsed on-wafer measurements and equates to 0.01 dBm per °C in output power. As previously discussed, the model is self-consistent over power and fits measurements over a large dynamic range. All model development was based on a two-fingered 720- μ m device and has been scaled successfully to a total gate periphery of 48 mm. The model fits *S*-parameters up to 20 GHz and a typical load–pull fit at 10 GHz is shown in Fig. 4.

The power contours are in 0.5-dB steps from 33.5 to 34.5 dBm and power-added efficiency (PAE) contours are in 10% steps from 30% to 50%. Extracting model parameters over the full range of *S*-parameters up to 20 GHz and at least two load–pull frequencies, typically 3.5 and 10 GHz, provide accurate results for both narrowband and broadband designs up to 20 GHz with narrowband power levels in excess of 100 W. Packaged model parameters have also been developed to support discrete transistors using the same intrinsic model used for MMIC PA design.

IV. BRIEF DESCRIPTION OF AMPLIFIER CLASSES

GaN HEMT technology has not only opened up a resurgence in the investigation of various PA classes such as D, E, and F, but has also led to investigations into new modes of operation such as Class J [35], [36]. In general, there has been a lot of attention given to “waveform engineering” in the last few years [37], [38]—this has undoubtedly been due to the fact that GaN HEMT devices allow voltage and current swings on the drains of the devices that can far exceed other RF power semiconductor technologies. Table III gives a basic summary of the theoretical maximum efficiencies that can be provided by various amplifier classes. In practice, the maximum efficiencies will be lower because of a number of reasons [39]: conductance losses, V_{KNEE} losses, passive component losses, and discharge losses.

TABLE III
THEORETICAL MAXIMUM EFFICIENCIES OF VARIOUS CLASS PAs

Class	A	B	C	D	E	F	J
Efficiency, %	50	78.5	100	100	100	100	78.5

V. BROADBAND AMPLIFIER EXAMPLES

Since GaN HEMTs have high-power densities and low input and output capacitances per watt of RF output power, compared to most other microwave semiconductors, they have become useful devices to achieve high powers over broad bandwidths. A variety of circuit approaches have been demonstrated over a range of power levels, frequencies and terminating impedances—these include distributed (traveling wave), lossy match, and gate-to-drain feedback. Three of the most popular applications have been in software-defined radios, broadband jammers, and instrumentation amplifiers. In the latter case, relatively large power levels are required for such applications as automotive electromagnetic compatibility (EMC) testing—multiple baluns for power combining are often used to achieve wide bandwidths at high power levels.

Cree Inc. has been developing GaN products for the past six years. All of these devices are based on a 0.4- μ m gate-length process and range in complexity from discrete unmatched transistors for wideband applications to multichip hybrid assemblies and packaged MMICs. An example of a discrete GaN HEMT for a very broadband amplifier application is the CGH40006S. This device is an unmatched transistor suitable for use in broadband applications, either as an output stage in military communication handheld radios or as a driver in counter IED jamming amplifiers. The challenge at this power level was to design an amplifier that would cover from 2 through 6 GHz. The transistor is housed in a plastic surface mount quad-flat no-leads (QFN) package. This package approach presents two key challenges: thermal management and electrical design to 6 GHz. The thermal design challenge was solved by placing the QFN packaged part on top of an array of filled vias. The vias were filled with conductive epoxy. The thermal conductivity of such epoxy-filled vias, although not as high as copper-plated vias, is sufficient. Simulations of the thermal stack were made using finite-element analysis (FEA) software (Fig. 5). Initial thermal simulations were performed at 4 W/mm (of gate periphery) of power dissipation to ensure that the channel temperature remained under 225 °C when operating at a case temperature of 85 °C.

Consideration was also given to the surface temperature of the die as the plastic of the QFN package is in direct contact with the transistor. From simulation it was determined that the surface of the die would be 30 °C lower than the peak channel temperature. The target power dissipation was then used as a design goal in the electrical simulations. Using the thermal engine of the large-signal model, it was possible to optimize the circuit’s electrical performance for best thermal performance. The electrical design challenge of the amplifier was caused by the source inductance of the via array and its impact on the performance of the final circuit. It was determined, during the design process that the launch of the RF signal from the printed circuit board to the package was critical. The use of a ground–signal–ground

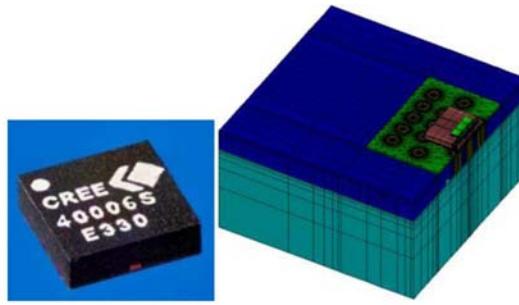


Fig. 5. Use of FEA tools to design a via array for best thermal management (top left: QFN package; top right: half of QFN package on via array; bottom left: temperature profile of QFN packaged transistor).

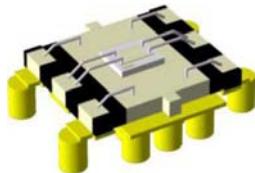


Fig. 6. Layout view of CGH40006S with associated via array and GSG feed structure.

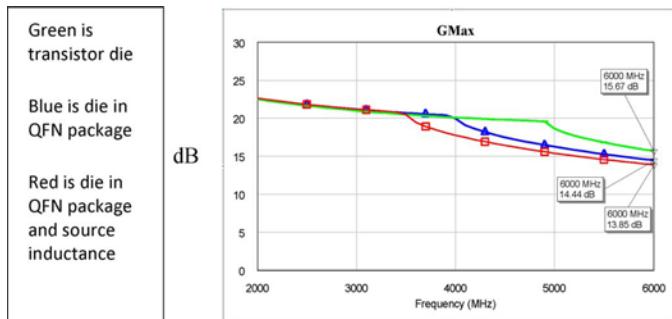


Fig. 7. Effects of source inductance and GSG feed on G_{MAX} .

(GSG) launch reduced the effect of source inductance on the maximum available gain of the device above 4 GHz.

The breakpoint in G_{MAX} is extended from 3.5 to 5 GHz, resulting in an increase in gain of 2 dB at 6 GHz (Figs. 6 and 7). The via array was modeled using a layout-driven simulation approach in Microwave Office. The circuit design approach was to synthesize matching circuits to match simulated source and load-pull impedances derived from the large-signal model. Fig. 8 indicates that matching to the input of this device was more complex than matching to the output. This is often the case with broadband circuit designs using GaN HEMTs.

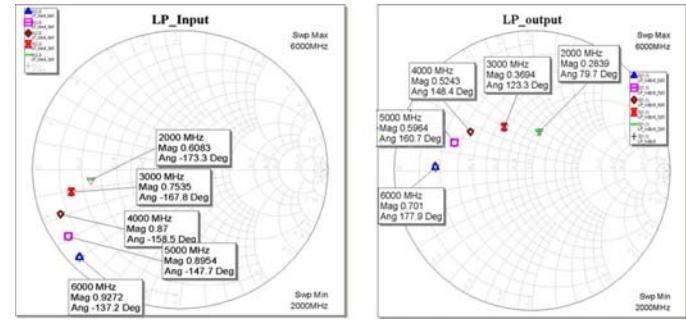


Fig. 8. Simulated optimum source and load impedances for CGH40006S.

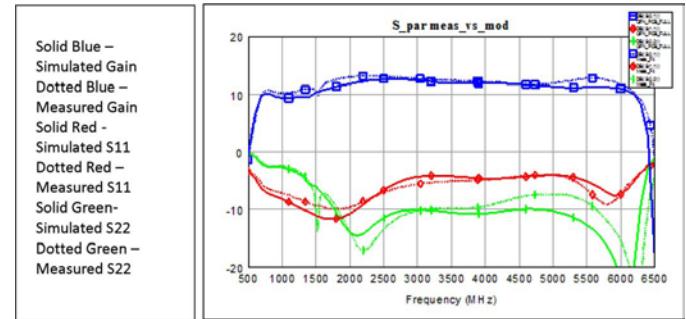


Fig. 9. Measured versus simulated small-signal performance of the CGH40006S in a broadband reference design.

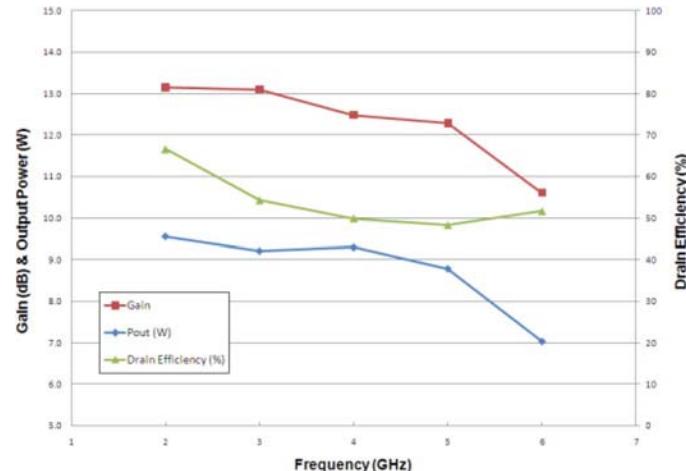


Fig. 10. Large-signal performance of the CGH40006S in a broadband reference design.

Excellent correlation was shown between measured and simulated circuit performances (Fig. 9) demonstrating the accuracy of the large-signal model. Furthermore, with careful layout driven techniques, a more complex and time-consuming 3-D analysis of the via array was not necessary.

Fig. 10 shows the measured large-signal performance of the complete amplifier (Fig. 11) over 2–6 GHz. Power gain is maintained at greater than 11 dB with 7-W minimum output power and drain efficiencies of greater than 50%.

Lin *et al.* [40] have used both the distributed and feedback approaches to design a range of commercial amplifiers covering saturated power levels up to 40 dBm over frequency ranges covering from 30 to 4000 MHz. Fig. 12 shows a comparison be-

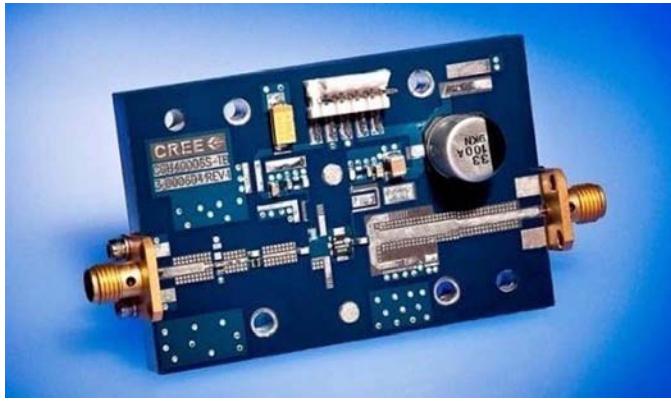


Fig. 11. Photograph of CGH40006S in a 2–6-GHz broadband reference design.

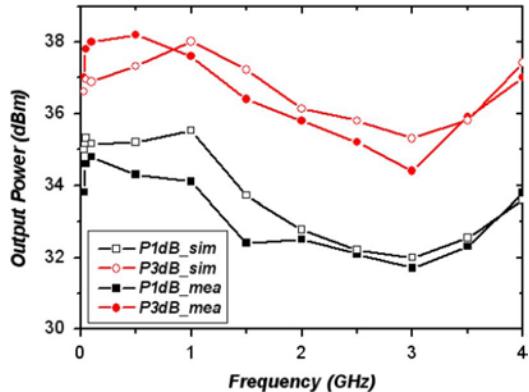


Fig. 12. Measured and simulated output power for broadband feedback amplifier [40].

tween measured and large-signal modeled results for one of the feedback amplifiers.

Carrubba *et al.* [41] recently demonstrated a novel, highly efficient, and broadband RF PA operating in “continuous class-F” mode. The introduction and experimental verification of this new PA mode demonstrated that it is possible to maintain expected output performance, both in terms of efficiency and power, over a very wide bandwidth. Using recently established continuous Class-F theory, an output matching network was designed to terminate the first three harmonic impedances. This resulted in a PA delivering an average drain efficiency of 74% and average output power of 10.5 W for an octave bandwidth between 0.55–1.1 GHz. Fig. 13 shows the practical implementation of the PA, while Fig. 14 shows the comparison between measurements and simulations.

VI. HIGH EFFICIENCY PA EXAMPLES

Much recent work has been achieved in the area of high-efficiency PA design using GaN HEMTs for a variety of classes of operation. This paper provides a number of circuit examples, but is, by no means, an exhaustive source of recent multiple designs.

Class D: Lin and Fathy [42] have demonstrated a Class-D amplifier using Cree CGH40010F transistors. A 50–550-MHz wideband GaN HEMT PA with over 20-W output power and

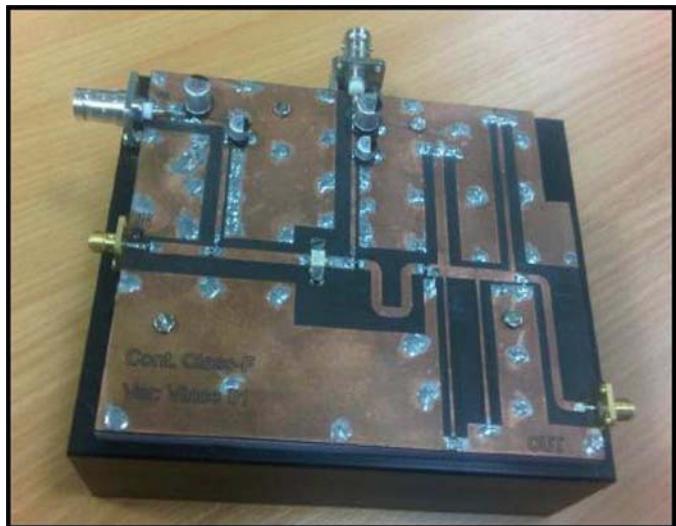


Fig. 13. Continuous Class-F mode PA [41].

63% drain efficiency was successfully developed. The wideband PA utilized two GaN HEMTs and operated in a push–pull voltage mode—Class D. The design was based on a large-signal simulation to optimize the PA’s output power and efficiency. To assure wideband operation, a coaxial line impedance transformer was used as part of the input matching network; a wideband 1:1 ferrite loaded balun and low-pass filters were utilized on the amplifier’s output instead of the conventional serial harmonic termination. Peak voltage swing on the drains of the transistors is 55 V (well within the breakdown voltage of the process). The practical implementation of the amplifier is shown in Fig. 15 and measured results are shown in Fig. 16.

Class E: Shi *et al.* [43] have developed a very compact highly efficient 65-W wideband GaN Class-E PA. Optimum Class-E loading conditions were achieved over a broad frequency range using a wideband design and implementation approach using bond-wire inductors and MOS/MIM capacitors. The amplifier output network schematic is shown in Fig. 17. A photograph of the implementation is presented in Fig. 18, showing the employment of Cree 14.4-mm GaN die. The PA operates from 1.7 to 2.3 GHz with a power gain of 12.3 ± 0.9 dB, while providing an output power of 42–65 W with a PAE ranging from 63% to 72%. The total area of the amplifier including bias networks is only 20 mm × 20 mm.

Class-E Doherty: Combining the advantages of Class-E and Doherty PA (DPA) operations has resulted in some of the highest PAEs at backed-off power levels reported to date. For example, Choi *et al.* [44] have described work on a two-way Doherty amplifier employing Class-E single-ended circuits for both the carrier and peaking amplifiers. The individual amplifiers, utilizing Cree CGH40010F transistors, were optimally matched at fundamental, second, and third harmonics using transmission lines on Taconic substrates (with dielectric constant of 2.6) to provide PAEs from 58% to 76% with output powers from 39.6 to 41.2 dBm and gains from 8.3 to 14.3 dB across 2.7–3.1 GHz. The switching Doherty amplifier consists of a carrier amplifier, peaking amplifier, broadband Wilkinson divider, offset lines, and output combiner. Fig. 19 shows the

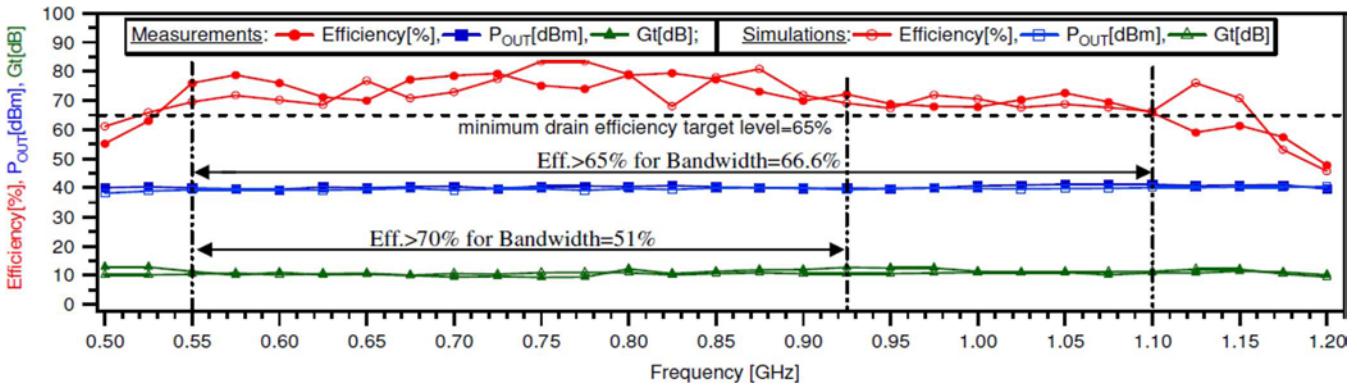


Fig. 14. Measured and simulated performance of continuous Class-F PA [41].

fabricated PA where the input divider uses multiple sections to minimize the effect of Class-E load conditions. Linearity of the amplifier was not a major concern since the application was for multifunction radar. PAE and drain efficiency at 6-dB back-off were 63% and 73%, respectively (Fig. 20).

Class-E Chireix Outphasing: A Chireix outphasing PA is a promising candidate to work around classical linearity-efficiency tradeoffs and is based on linear amplification using nonlinear components (LINC). In an out-phasing transmitter, a complex modulated input signal is split into two signals with constant amplitude and a relative phase difference, corresponding to the time-varying envelope of the original input signal. The two branch signals are amplified by switch-mode power amplifiers (SMPAs). After combining both branch signals at the outputs of these SMPAs, an amplified replica of the original input signal results. Unfortunately, due to the nonisolating properties of the combiner, a time-varying reactive load modulation exists at the output of both SMPAs. To mitigate this unwanted load modulation, Chireix compensation elements are placed at the input ports of the power combiner. This creates an efficiency peak at a specified power back-off level, resulting in an improved average PA efficiency. The Chireix outphasing combiner is usually based on quarter-wave transmission lines and can be found in many publications on outphasing PAs. The Chireix compensation elements are either lumped or can be incorporated in the combiner. There are, however, some drawbacks to the classical Chireix combiner. The efficiency not only depends on the outphasing angle, but also on frequency since both the Chireix compensation elements and the quarter-wave lines are frequency dependent. Class-B, Class-D, and Class-F implementations have traditionally been used in the branch PAs, but recently Class-E has been identified as an even better candidate, demonstrating higher efficiency over a wider dynamic range [45].

Transformers can convert a single-ended load into a floating load. However, a lumped-element transformer is difficult to implement for high powers at RF frequencies. Coupled lines can be used to combine the outputs as in a Marchand balun. Van der Heijden *et al.* [46] have fabricated an outphasing SMPA with a Class-E Chireix coupled-line combiner. Fig. 21 shows the schematic of the amplifier. The Class-E PA switches were realized with commercially available Cree GaN HEMT transistor die. Since the GaN stages need to be driven with pulse-wave

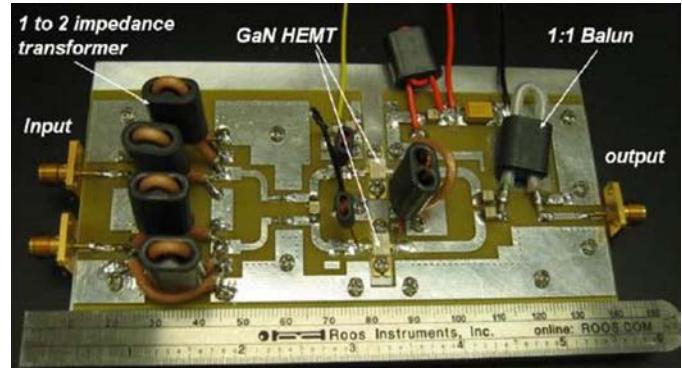
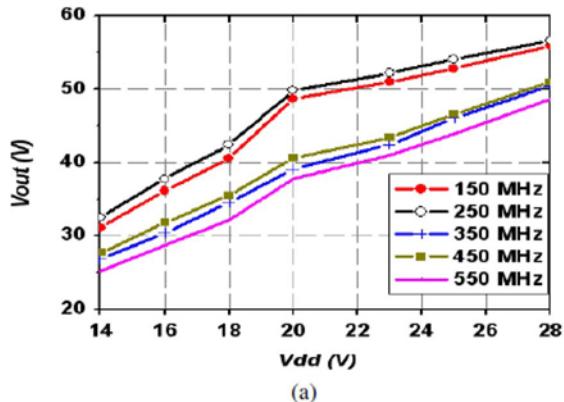


Fig. 15. Practical implementation of Class-D UHF PA [42].

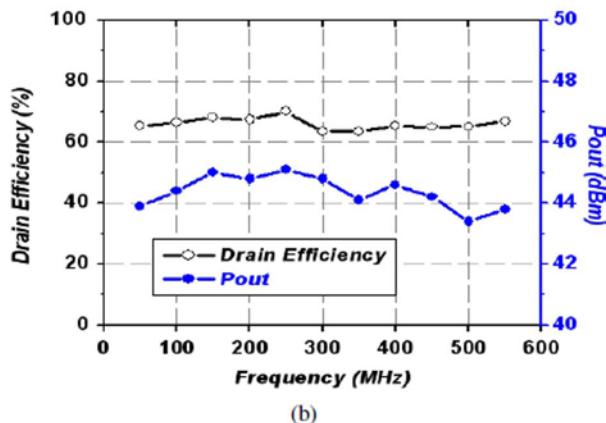
signals (to obtain the highest efficiency), a high-voltage CMOS driver topology was used in a 65-nm process. Fig. 22 shows a close-up of the CMOS-GaN SMPA lineup. Fig. 23 shows drain efficiency, total lineup efficiency, and power gain as a function of output power. At 10-dB back-off, the drain efficiency is 65% and the total lineup efficiency is 44%. At 8-dB back-off, the drain efficiency is 70% and the total lineup efficiency is 53%. The drain efficiency at 10-dB back-off is comparable to what has been published for a three-way GaN DPA, but with wider bandwidth capability.

Class-F: A wide range of both Class-F and inverse Class-F PAs have been described in the literature. Typical of these is the PA design produced by Schelmzer and Long [47]. In a Class-F amplifier, the output matching network must absorb the C_{DS} of the HEMT and the interconnect inductance while providing the correct fundamental and harmonic resistances at the intrinsic drain of the transistor. It is beneficial if the matching network can be tuned to different values of R_L so the amplifier can be designed for different supply voltages, especially for GaN transistors, which can be matched to a range of impedances due to their high breakdown voltage.

Fig. 24 illustrates a matching network that can accomplish this. Two separate bond-wires are used at the drain pad. This allows the bond-wire inductance to be incorporated into the quarter-wavelength drain bias transmission line giving the lowest even harmonic impedances at the drain. Z_2 , θ_2 , and Z_3 can be tuned to absorb C_{DS} and L_{BW} and simultaneously present a real impedance at the fundamental, R_L , and a very



(a)



(b)

Fig. 16. Measured performance of Class-D PA [42].

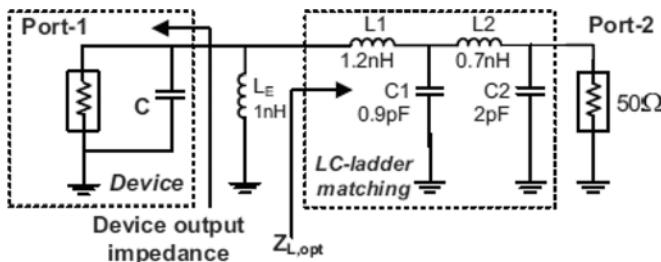


Fig. 17. Class-E output matching network for compact PA [43].

high real impedance at the third harmonic. Effectively, both matching networks terminate the second, third, and fourth harmonics and some of the higher order even harmonics as well.

The output matching network topology is a particularly good fit for the GaN transistor used (Cree CGH60015D, 3.6-mm gatewidth transistor) having a C_{DS} of about 0.9 pF. The output matching network was capable of tuning R_L from 25 to 120 Ω while maintaining a high third harmonic impedance and realizable transmission-line impedance.

The amplifier was constructed on a low-loss printed-circuit-board substrate with gold-plated traces mounted to a copper carrier. The GaN HEMT was directly mounted to the copper carrier and used wire-bond interconnects. Fig. 25 shows a photograph of the amplifier. The amplifier was tested at 2 GHz where only the fundamental frequency component was measured for the results. The amplifier had a peak PAE of 85.5% with an output power of 16.5 W with a drain bias voltage of 42.5 V. The peak

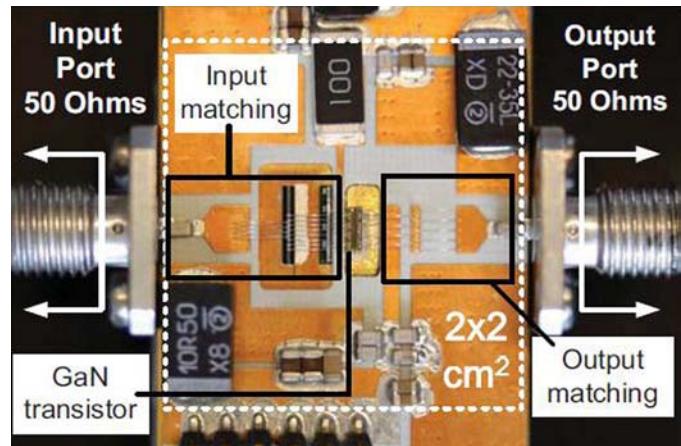


Fig. 18. Practical implementation of compact Class-E PA [43].

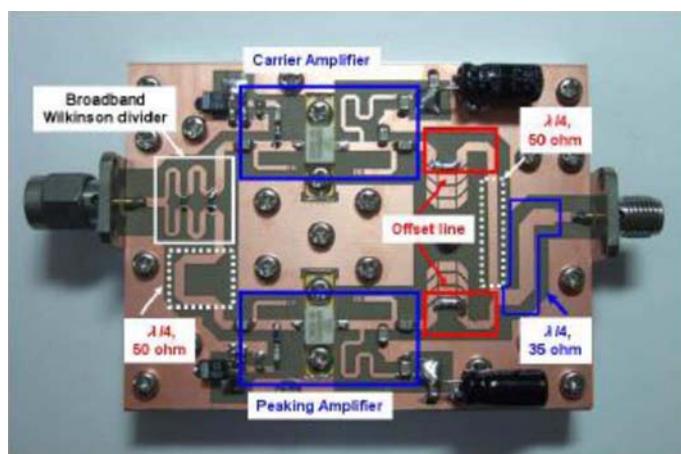


Fig. 19. Practical implementation of Class-E DPA [44].

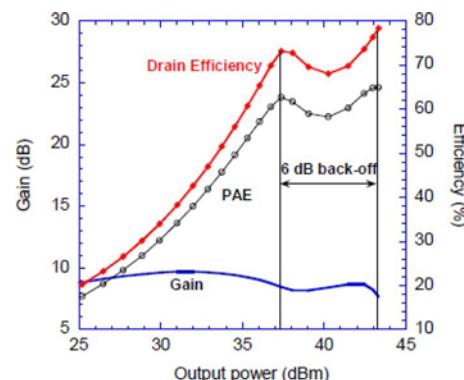


Fig. 20. Gain and efficiency of Class-E DPA [44].

gain was 15.8 dB, and it had a compressed gain at peak PAE of 13.0 dB. The peak drain efficiency was 91%.

Class-J: Moon *et al.* [36] have presented the theory of operation of Class-J PAs with linear and nonlinear output capacitors (C_{OUT}). The efficiency of a Class-J amplifier is enhanced by the nonlinear capacitance because of harmonic generation from the nonlinear C_{OUT} , especially the second-harmonic voltage component. This harmonic voltage allows the reduction of the phase difference between the fundamental voltage and current components from 45° to less than 45° while maintaining a

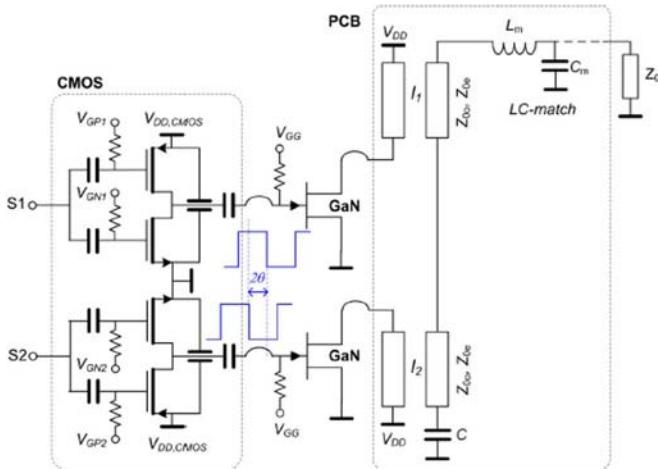


Fig. 21. Schematic of Class-E Chireix coupled line outphasing PA [46].

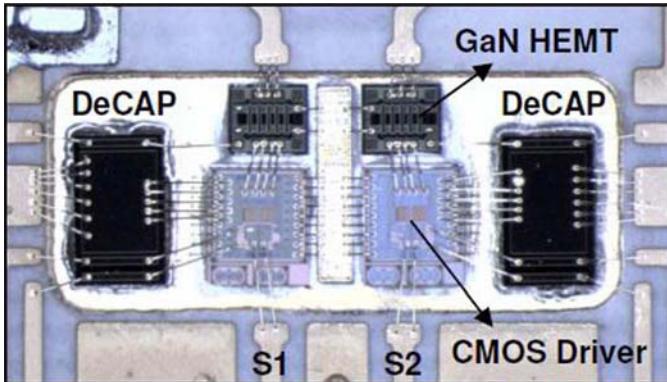


Fig. 22. Close-up photograph of CMOS driven Class-E GaN HEMTs [46].

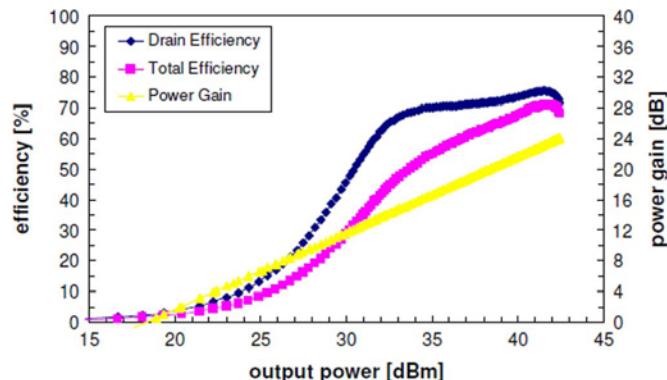


Fig. 23. Power gain, drain, and total lineup efficiencies of Class-E Chireix outphasing PA [46].

half-sinusoidal shape. Therefore, a Class-J amplifier with the nonlinear C_{OUT} can deliver larger output power and higher efficiency compared with a linear C_{OUT} . The Class-J amplifier can be further optimized by employing a so-called saturated PA, a recently reported amplifier type presented by the same authors. The phase difference of that proposed PA is zero. Like the Class-J amplifier, the PA uses a nonlinear C_{OUT} to shape the voltage waveform with a purely resistive fundamental load impedance at the current source, which enhances the output power and efficiency. A highly efficient amplifier based on

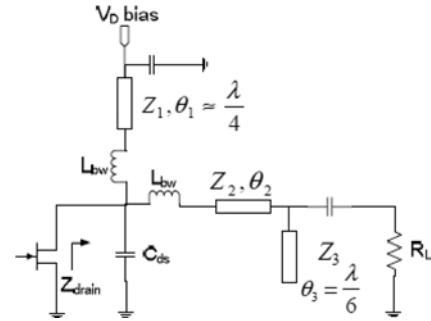


Fig. 24. Output matching network for Class-F PA [47].

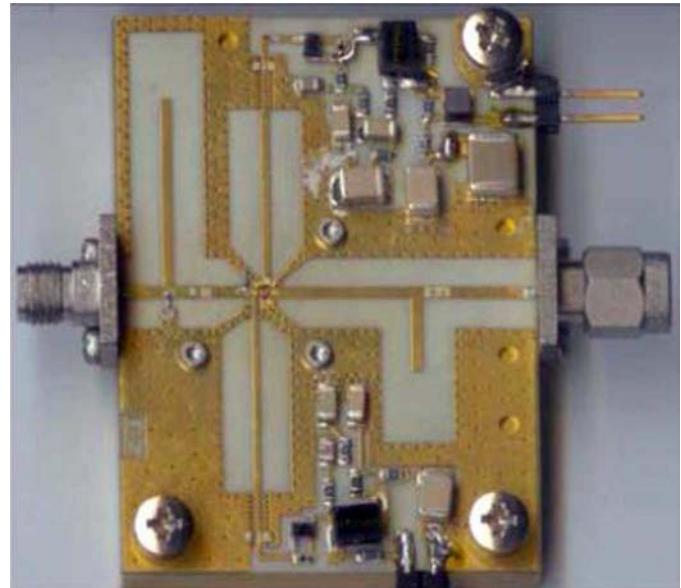


Fig. 25. Practical implementation of bare die GaN HEMT Class-F PA [47].

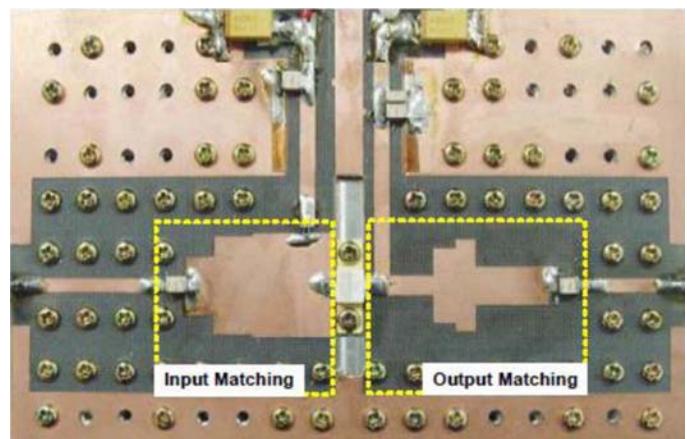


Fig. 26. Practical implementation of Class-J PA [36].

the saturated PA was designed using a Cree CGH40010F GaN HEMT at 2.14 GHz (Fig. 26). It provided a PAE of 77.3% at a saturated power of 40.6 dBm (11.5 W).

DPAs: There has been a very large body of work completed on high-efficiency DPAs over the last few years. This paper will only describe a few examples, but there are various approaches

TABLE IV
VARIOUS TYPES OF DPA CONFIGURATIONS

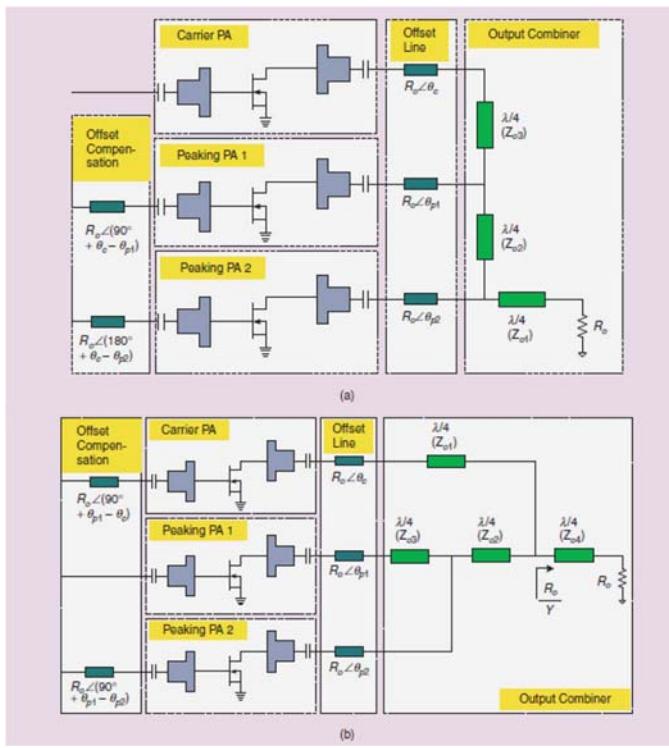


Fig. 27. Two different types of three-stage DPAs [48].

covering “conventional” two-way, N -way, and N -stage, asymmetrical (both unequal power division and unequal transistor peripheries), as well as different classes of operation for carrier and peaking amplifiers.

Kim *et al.* have provided an extensive overview of DPA design specifically employing GaN HEMTs [48]. Of particular interest is the description of various three-way approaches shown schematically in Fig. 27. There are two kinds of three-stage DPA architectures, as shown in Fig. 27(a) and (b). Fig. 27(a) is a widely known structure. The topology is a parallel combination of one DPA used as a carrier PA with an additional peaking PA. The first peaking PA modulates the load of the carrier PA initially and the second peaking PA modulates the load of the previous Doherty stage at a higher power. The topology in Fig. 27(b) is a parallel combination of one carrier PA and one DPA used as a peaking PA. Both the three-stage and the three-way architectures use three PA units, but the two peaking PAs are turned on sequentially in the three-stage DPA instead of simultaneously like a multistage amplifier. Thus, three peak efficiency points are formed: at the two turn-on points and at the peak power. In the three-way structure, the peaking PAs are turned on simultaneously, similar to N -way power combining. To achieve proper load modulation, the three-way DPA requires two quarter-wavelength transmission lines, but the three-stage DPAs require three and four quarter-wavelength transmission lines, respectively. A comparison of the achievable efficiencies of various types of DPAs is shown in Table IV.

To implement the three-stage DPA, a Class-AB mode PA was designed at 2.655 GHz using Cree’s CGH40045F GaN HEMT devices. A simple method to overcome the problem of incomplete load modulation due to unequal currents in the carrier and

802.16 WiMAX with 8.5 dB PAPR		
N-Way	Back-off, dB	Average Drain Efficiency, %
2 way	-6	59
3 way	-9.54	61.2
Three-Stage Type 1		
1:2:2	-4.44/-9.54	69.8
1:2:3	-6/-9.54	69.4
1:3:3	-4.87/-12	70.5
1:3:4	-6/-12	71
Three-Stage Type 2		
1:1:1	-6/-9.54	69.4
1:2:2	-6/-13.98	70.1
2:3:3	-6/-12	71

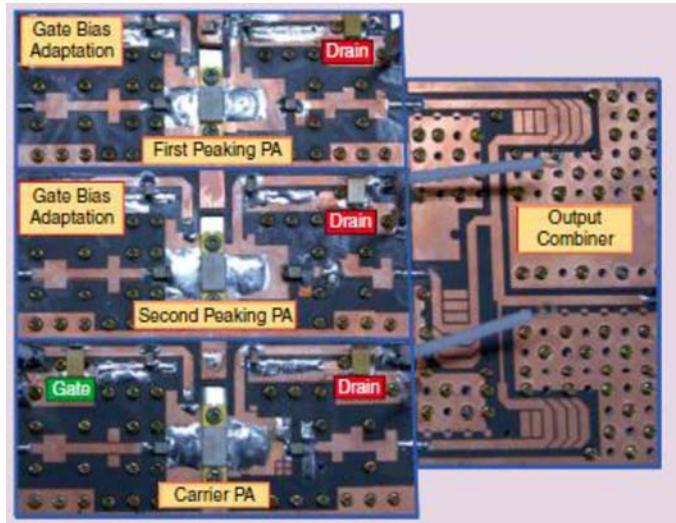


Fig. 28. Practical implementation of three-stage DPA [48].

peaking amplifiers was to control the gate bias of the peaking PAs. Gate bias control of the DPA is also often employed for accurate intermodulation cancellation. Gate bias control of the peaking PA was also used for performance optimization, that is, to simultaneously achieve high efficiency at the backed-off input power, as well as at high peak powers. In this example, the quiescent bias current of the carrier PA was 55 mA, and the PA delivered 64.6% drain efficiency at an output power of 46.4 dBm. The implemented PA with 1:1:1 ratio is shown in Fig. 28. The measured efficiency is illustrated in Fig. 29(a). This amplifier was employed for amplification of an 802.16e Mobile WiMAX signal with 7.8-dB peak-to-average power ratio (PAPR). Fig. 29(b) shows the measured efficiency of the envelope-tracking three-stage DPA with and without gate bias adaptation.

Grebennikov [49] described a novel high-efficiency four-stage DPA architecture convenient for practical implementation in base-station applications for modern communication standards. Each PA was based on a 25-W Cree GaN HEMT device with the transmission-line load network corresponding to an inverse Class-F mode approximation. In a CW operation

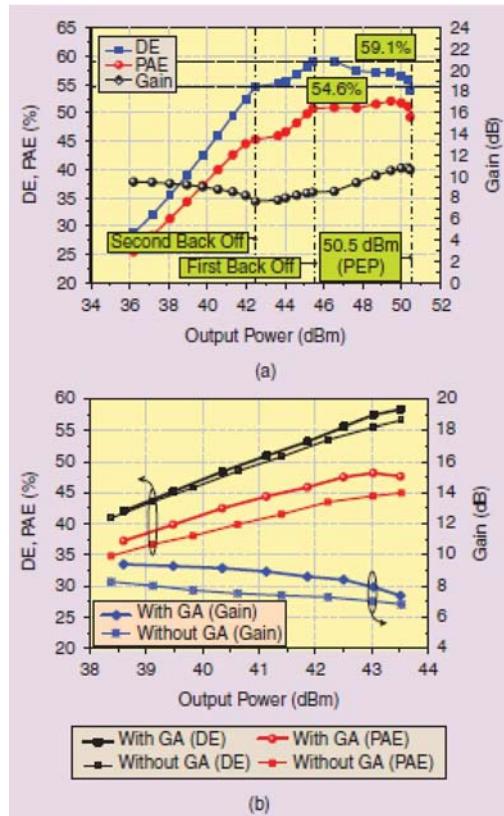


Fig. 29. (a) Gain and efficiency of DPA versus output power. (b) Gain, output power, and efficiencies of DPA with and without gate bias adaptation [48].

mode with the same bias voltage for each transistor, an output power of 50 dBm with a drain efficiency of 77% was achieved at a supply voltage of 34 V. In a single-carrier W-CDMA operation mode with a PAPR of 6.5 dB, a high drain efficiency of 61% was achieved at an average output power of 43 dBm, with ACLR1 measured at a -31 -dBc level. The Doherty configuration is shown in Fig. 30 and affords high efficiency to be maintained over a wide region of back-off conditions.

In theory, three-way DPA implementations can offer even better efficiencies in power back-off operation, which is highly desirable when dealing with single or multiple (unclipped) W-CDMA channels or modern fourth-generation (4G) signals with high crest factors. Unfortunately, practical three-way DPA implementations rarely meet their expectations due to their complicated implementation. To overcome these implementation issues and enable reproducible, as well as very efficient N -way Doherty amplifiers, the use of mixed-signal techniques was recently proposed to establish digital input control of the individual amplifier cells [50]. This approach facilitates the independent optimization of the amplifier-cell drive conditions for maximum efficiency. Neo *et al.* [51] had previously employed Si LDMOS transistors in the PAs, but have extended this concept to demonstrate the capabilities with GaN HEMT transistors. The system setup for the three-way DPA is shown in Fig. 31.

The system is calibrated to maximize the backed-off power efficiency by adjusting the relative input phases of the three signals, as well as optimizing performance as a function of the

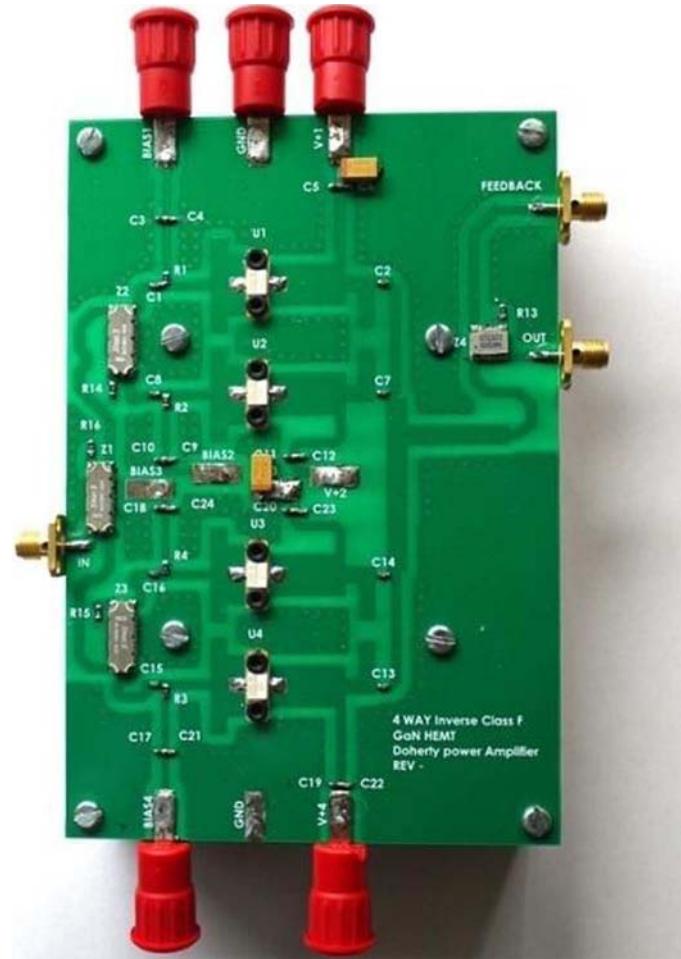


Fig. 30. Four-way DPA implementation [49].

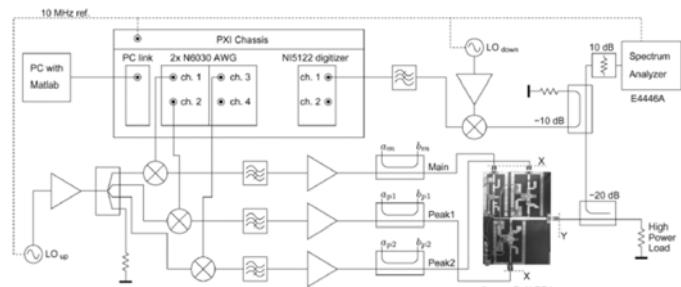


Fig. 31. Schematic diagram of three-way mixed-signal DPA [50].

relative sizes of the transistors used in the carrier and peaking amplifiers. Fig. 32 also shows the normalized measured PAE of a 45-W Class-B GaN amplifier, which utilized an identical device as applied in the peak 1 amplifier. It is interesting to see that at maximum output powers, both the DPA, as well as the Class-B amplifier using the same device technology reach a maximum PAE of almost 70%, confirming the close to ideal operation of the DPA design at full power. Note that the PAE of the Class-B GaN amplifier decreases proportionally to the square of the back-off power, whereas the GaN three-way DPA demonstrates very high efficiency throughout the entire back-off range of 12 dB. At the 12-dB back-off point, the GaN three-way DPA provides three times higher PAE than the Class-B amplifier

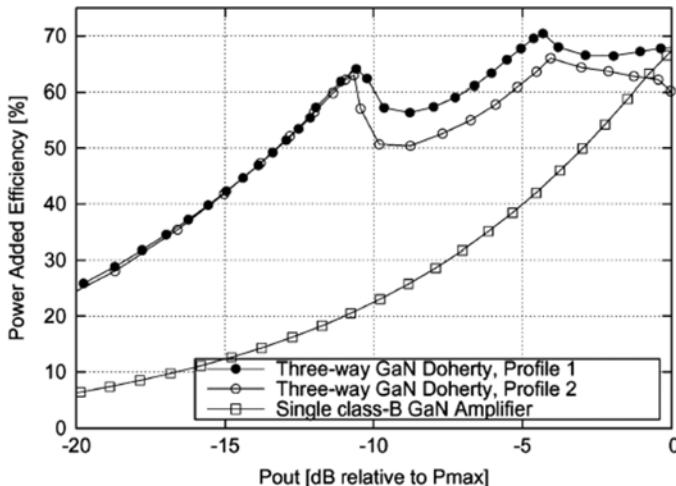


Fig. 32. Measured PAE of three-way DPA versus output power under two different mixed-signal conditions when compared to a single-ended Class-B amplifier [50].

for CW signals, indicating the very high efficiency potential of the three-way DPA for complex modulated signals with a high PAPR. The CW performance of the three-way GaN DPA was characterized and optimized using software control, yielding a measured performance of: 68% PAE at 50 dBm (full power), 70.4% at 45 dBm (first back-off point), and 64% at 38 dBm (second back-off point), while the measured transducer power gain was greater than 10 dB at all times. To demonstrate that this exceptional high-efficiency performance could be effectively utilized for practical base-station operation, the GaN three-way DPA was driven by a W-CDMA signal with a crest factor of 11.5 dB. Using a dedicated memory-effect compensating pre-distortion algorithm, the resulting measured PAE for this signal was 53% at an average power of 38.5 dBm, while meeting all linearity specifications. This was the highest PAE performance ever reported for any PA operating with a W-CDMA signal without using crest factor reduction techniques (at the time of the publication in 2008).

Envelope Tracking (ET) PAs: The high-voltage operation of GaN HEMTs is particularly attractive for ET techniques that are used to maintain high efficiencies over a wide range of operating drain voltages under saturated power conditions. Over the last few years there have been a variety of reported results on ET-based amplifiers using a variety of RF semiconductor technologies such as Si LDMOSFET, GaAs HVHBT, and GaN HEMT [52], [53], [54].

Yamaki *et al.* [5] have described an optimized GaN device consisting of a single-die HEMT with 43 mm of gate periphery together with internal matching circuits in a package. The package size is 13.2 mm × 21.0 mm. In order to realize high efficiencies, the authors implemented an inverse Class-F PA with harmonic terminations with output-matching networks inside the package. A single GaN HEMT die has advantages in terms of simplicity and cost effectiveness. The authors processed two types of GaN HEMT (A and B). The gate periphery and length were 43 mm and 0.6 μ m for 200-W output power, respectively. The gate electrode consisted of Ni/Au, and SiN

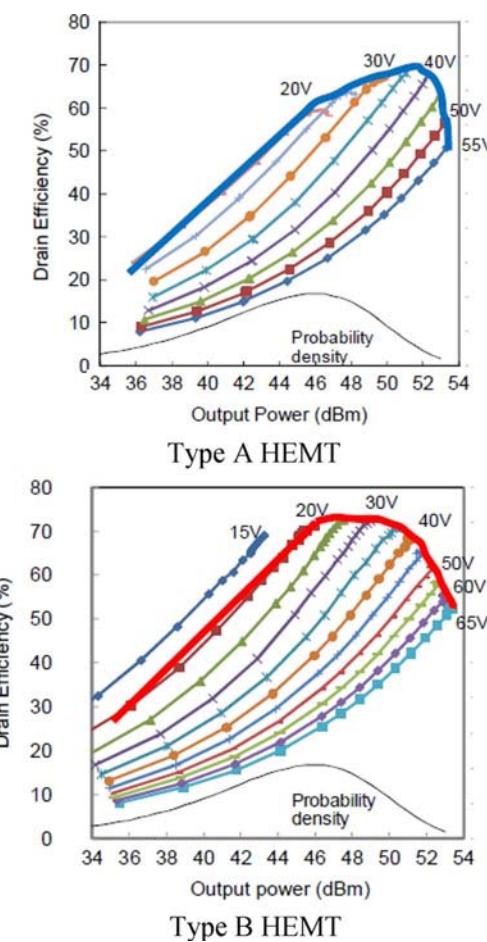


Fig. 33. Drain efficiency versus output power for GaN HEMTs A and B [5].

passivation was deposited on the GaN cap layer using plasma CVD. The structure of GaN HEMT (A) was “conventional,” which had already been manufactured as the commercially available EGN21C210I2D. The electrode structure and AlGaN electron supply layer of GaN HEMT (B) was changed to improve breakdown voltage to greater than 300 V allowing safe drain voltage operation under ET up to 65 V.

Fig. 33 shows the drain efficiency measured at various drain voltages as a function of output power at 2.14 GHz together with a probability density function (PDF) of the W-CDMA signal. The bold line on the efficiency curves represents the operating point of the ET system. As shown in Fig. 33(a), the drain efficiency of the GaN HEMT (A) device was more than 65% over a 30 V ($P_{out} = 49.2$ dBm) to 40 V (52.7 dBm) drain bias range with a maximum drain efficiency of 68%. When a W-CDMA signal with 7-dB PAPR is used in this case, the drain efficiency of the GaN HEMT (A) device decreased significantly below the average power. As shown in Fig. 33(b), the drain efficiency of the GaN HEMT (B) device was more than 65% over a 15-V ($P_{out} = 42.5$ dBm) to 45-V (51.5 dBm) drain bias range with maximum drain efficiency of 72.5%. This result indicated that the GaN HEMT (B) device provided 65% efficiency over a wide range of powers (9 dB) as a result of the high-voltage operation and the improved C_{DS} characteristics.

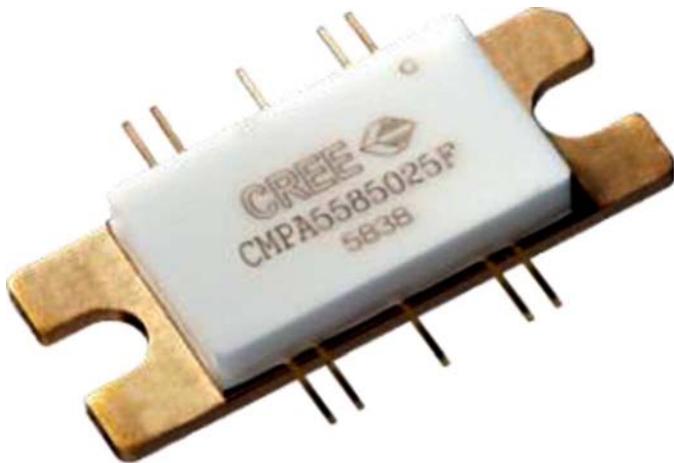


Fig. 34. CMPA5585025F shown in custom developed ten-lead 50- Ω package with dedicated bias leads.

VII. MONOLITHIC PA EXAMPLES

SiC is an excellent semi-insulating material, which allows it to be used for low-loss transmission lines and lumped elements (see Table I for properties of SiC) in addition to active devices such as HEMTs. Thus, GaN on SiC monolithic integrated circuits have become a popular platform for a range of circuits including wideband PAs. The first example is of a commercially available GaN HEMT MMIC, the CMPA5585025F, from Cree Inc. This MMIC is a packaged two-stage amplifier for satellite communications applications. The MMIC covers both the commercial, 5.8–7.2 GHz, and military, 7.9–8.4 GHz, frequency allocations. The availability of this packaged GaN HEMT MMIC has increased significantly state-of-the-art performance in terms of efficiency, gain, and power. In comparison, an internally matched GaAs FET only covers one band of interest. Target RF output power at 85 °C case temperature, assuming a copper–tungsten composite package flange, was 25 W (CW). The efficiency and power gain targets were 40% PAE and 15–20 dB, respectively, across the frequency bands. A new multilead package was also developed for the MMIC, which can be used for a complete range of MMICs. The availability of commercially available packages for high-power large-area MMICs is somewhat limited. Most high power packages have relatively poor thermal conductivities and only have a single input and output RF lead. To take full advantage of a high-performance MMIC, it is very desirable to have multiple dedicated bias leads on either side of the RF leads to optimally distribute bias voltages to the MMIC (Fig. 34). This is an important design consideration since dc-bias networks often affect the overall stability of the amplifier—especially when working with high-power high-gain MMICs enclosed within small form factors. Each lead is also provides RF impedance of 50 Ω operating to 15 GHz or so. This package also has the advantage of superior thermal conductivity as the flange material is 1:3:1 CPC (see Table V) enabling the packaged MMIC to be used to full case temperature without any de-rating of its linear output power.

The MMIC was characterized for its linear performance under offset quadrature phase shift keyed (OQPSK) modulation. The linearity specification requires spectral purity

TABLE V
COMMONLY USED MATERIALS FOR THERMAL MANAGEMENT OF
GaN HEMT TRANSISTORS AND MMICS

	CuW-10 10%Cu 90%W	CuMoCu 30%Cu 70%Mo	CMC Cu/Mo/Cu 1:1:1	CPC Cu/CuMo/Cu 1:4:1	Alumina
Thermal Conductivity, W/mK	197	190	260	220	35
Coefficient of Thermal Expansion, ppm/K	8	7.65	7.1	7.5 to 8.5	5.4
		Super CMC Cu/Mo multilayers	Aluminum Diamond/Silver Diamond		
Thermal Conductivity, W/mK		370		>500/800	
Coefficient of Thermal Expansion, ppm/K		6 to 10		7.5<10	

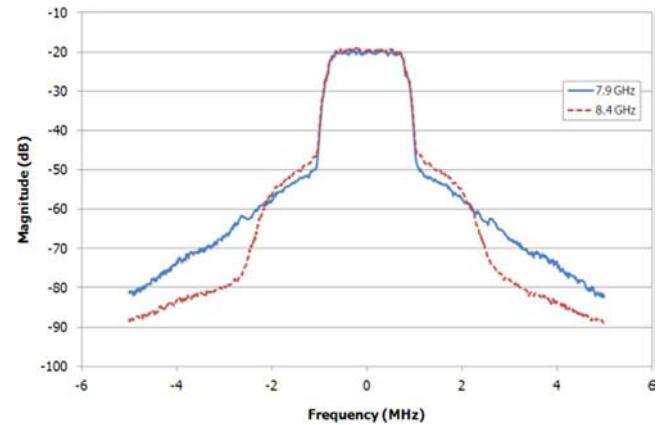


Fig. 35. CMPA5585025F spectral mask under 1.6-Ms/s OQPSK at 15-W average output power.

measurements at a spectral offset of one symbol from the center frequency, i.e., for a 1.6-Ms/s signal rate, the spectral mask is measured at 1.6-MHz offset from the center of the carrier. At this frequency, the spectral emissions are required to be less than -25 dBc. The multiple bias leads of the package allow for large video bandwidths to be supported. This allows compliance with the inevitable increase in data that satellite communications systems will have to handle in the near future.

Fig. 35 shows the spectral mask of the CMPA5585025F at both 7.9 and 8.4 GHz. At these frequencies, the PAE is 25%—over twice that of an internally matched discrete GaAs FET. GaN HEMTs have adequate linearity when biased in Class A/B, whereas GaAs FETs are biased in Class A and are operated typically at 10 dB below their 1-dB compression point. Consequently the PAEs for the latter devices are usually less than 10%. Also, due to their low power densities, GaAs FETs also have large gate peripheries to achieve the required output power, which lead to devices with very high output capacitance with power gains of only 6 dB or so. The GaN MMIC described here typically provides 20-dB gain at its rated linear output power across both *C*- and *X*-bands. A summary of performance is shown in Fig. 36.

Distributed MMIC Amplifier Design Example: A dc–6-GHz distributed MMIC amplifier (Cree CMPA0060025F) was designed using the nonlinear model-based design process described earlier [55]. The distributed (traveling wave) amplifier

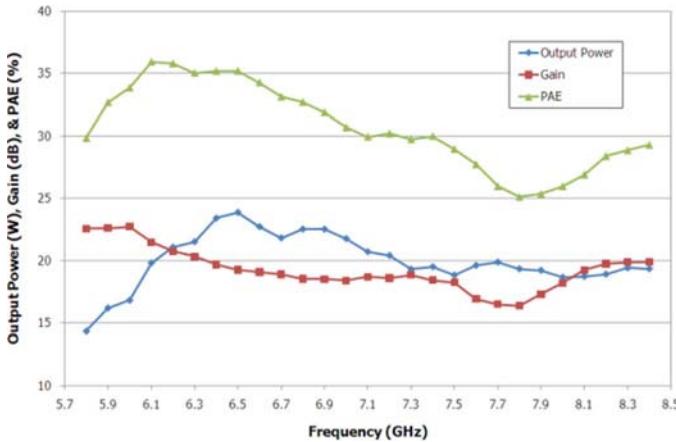


Fig. 36. CMPA5585025F output power, gain, and PAE at rated linear output power under 1.6-Ms/s OQPSK modulation.

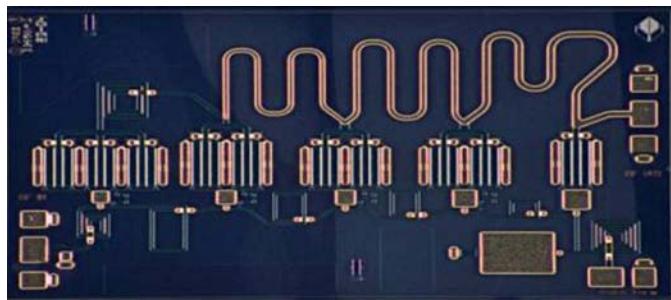


Fig. 37. Cascode NDPA MMIC.

is particularly useful in low-pass multioctave applications. The power and efficiency limitations for a reactively match amplifier are governed by the Bode–Fano power-bandwidth limit and by passive circuit losses. For very high-power levels, these limits dictate a maximum drain voltage based on a load-line match over the required bandwidth. In principle, the reactive elements of the active devices can be absorbed into the gate and drain synthetic transmission lines of a distributed topology with the limitations being gate line cutoff frequency and loss along the drain line [56]. A further complication in the design of power distributed amplifiers is that of device load-line match over the required band. Using standard distributed design techniques, some active devices may actually sink power in parts of the band.

To achieve high efficiency from the distributed amplifier, a nonuniform approach is used in the design of the output transmission line where the characteristic impedance changes cell by cell and the output reverse termination is eliminated [57]. Proper design of the gate and drain lines and resizing of the individual cells will establish a reasonable load-line impedance for each cell.

Other issues affecting nonuniform distributed power amplifier (NDPA) performance include output line loss, drain–gate feedback, and drain voltage level required to provide power to a $50\text{-}\Omega$ load. Each of these design problems can be reduced by using a balanced cascode configuration for individual cells [58]. The cascode configuration exhibits significantly reduced feedback and output conductance compared to a single common-

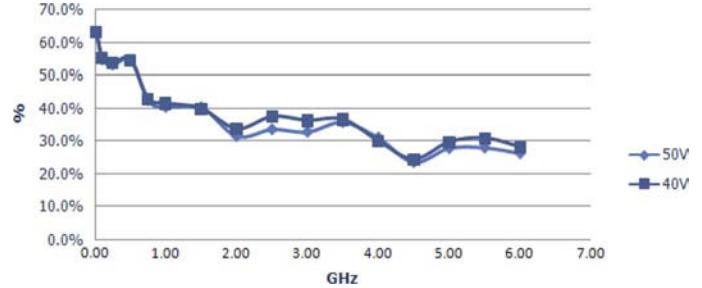


Fig. 38. Drain efficiency versus frequency at $P_{IN} = 32 \text{ dBm}$ for NDPA MMIC.

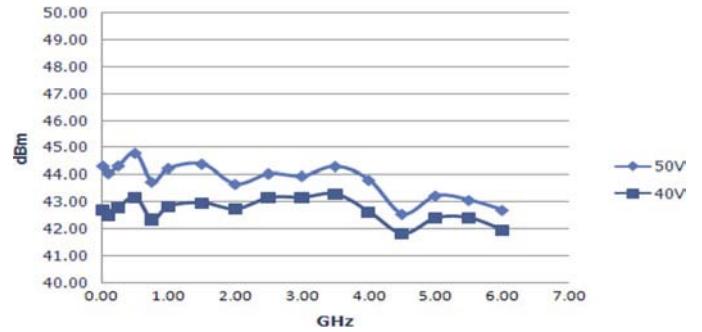


Fig. 39. Output power at $P_{IN} = 32 \text{ dBm}$ for NDPA MMIC.

source stage. With the common-source and common-gate stages balanced as shown in [58], the drain voltage can be increased as much as twofold without incurring breakdown issues.

Although device breakdown would support operation of the cascode cell up to a drain voltage of 80 V, the design becomes thermally limited. For CW operation, experience shows that 4–5 W/mm is the limit of dissipated power to maintain channel temperatures $<200^\circ\text{C}$. The dynamic self-heating feature of the nonlinear model is crucial for predicting this operation. For the five-stage design example shown in Fig. 37, this limit is a drain voltage of 50 V. This should give an output power into $50\text{-}\Omega$ of

$$P_{OUT} = V_D^2 / (1.414 * 50) = 25 \text{ W.}$$

The measured performance of this amplifier is shown in Figs. 38 and 39. The amplifier produces 25 W of RF power up to 6 GHz with approximately 30% PAE. This shows that the cascode cell NDPA can be designed with a high-efficiency load line over a decade bandwidth.

VIII. VERY HIGH PAs

The majority of existing radar systems utilize technologies such as klystrons, magnetrons, or traveling-wave tube amplifiers (TWTAs) for their PAs. As end users demand more capability and operability for radar systems, they have been in search of more reliable cost-effective highly efficient, yet small-sized radar PAs. There have been two major independent approaches to overcome these challenges and to meet the needs—the first approach is to provide a miniaturized traveling-wave tube (TWT) to help make radar system smaller; the other approach is based on solid-state PAs using GaAs MESFETs or Si bipolar transistors. More recently, GaN HEMTs have become a very promising technology for small-size



Fig. 40. Practical implementation of 1-kW S-band GaN HEMT PA [59].

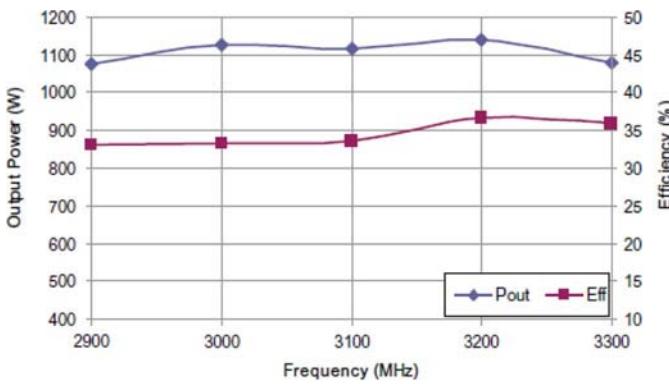


Fig. 41. Measured output power and total line-up efficiency of 1-kW S-band PA [59].

high-efficiency PAs in the kilowatt range. Kwack *et al.* [59], for example, have described the design and manufacture of multistage *S*-band 1-kW pallets consisting of a pre-driver stage, driver stage, and four combined 300-W units. Fig. 40 shows detail of the complete 1-kW pallet.

As shown in Fig. 41, the SSPA successfully achieved output powers above 1 kW from 2900 to 3300 MHz. The efficiency of the whole PA, including the bias circuits, was about 34%. The output power was measured at the midpoint of the pulselength (100 ms with a 10% duty factor), and the efficiency was calculated using the peak current value during the pulse. During the pulse, the output power overshoots at the beginning of the pulse, and then gradually comes down with time, which is defined as power droop (the main cause of power droop being the thermal degradation of performance in the particular semiconductor technology, which for GaN is considerably better than either GaAs or Si due to the superior thermal conductivity of SiC).

IX. THERMAL MANAGEMENT AND PACKAGING

A systematic and consistent approach to the thermal modeling and measurement of GaN on SiC HEMT power transistors has been described [60]. Since the power density of such multilayered wide bandgap structures and assemblies can be very

high compared with other transistor technologies, the application of such an approach to the prediction of operating channel temperatures (and hence, product lifetime) is important. Both CW and transient (i.e., pulsed and digitally modulated) thermal resistances were calculated for a range of transistor structures and sizes as a function of power density, pulse length, and duty factor and compared with measured channel temperatures and RF parameters. The resulting thermal resistance values have then been imported into new “self-heating” large-signal models so that transistor channel temperatures and the resulting effects on RF performance such as gain, output power, and efficiency can be determined during the amplifier design phase.

GaN HEMT devices place considerable onus on the type of packaging used to house them because of the relatively high RF power density and resulting dissipated heat density from the die. Table V shows some of the commonly available materials used for commercial transistor packages that are suitable for many GaN HEMT devices. The most popular materials used today are copper–tungsten copper–molybdenum–copper, and copper–copper–molybdenum–copper. These materials not only have good thermal expansion coefficient matches to SiC, but also to the alumina ceramic materials most often employed for lead frames. All flange materials also need to have stable properties with regard to temperature, e.g., bowing and flatness, as well as suitable low surface roughness after plating allowing efficient, and void free die attach usually employing AuSn eutectic solder pre-forms.

PAEs for relatively narrowband CW PAs employing GaN can be high (typically greater than 60%), but in certain cases (such as high-frequency ultra-broadband MMICs), efficiencies can be in the low 20% region. In these cases, more exotic materials are required for die mounting such as aluminum diamond or silver diamond composites [61], [62], which have thermal conductivities two to three times that of copper-based materials. Such increases in thermal conductivity have a marked effect on the operating channel temperature of the transistors—typically lowering the temperature by 25% or so (thus, if with Cu–Mo–Cu the $T_{CHANNEL}$ was 200 °C it will be reduced to 150 °C (using silver diamond)).

For pulsed applications, the situation is quite different. With almost an infinite number of pulselength and duty cycle combinations, an effective way of communicating the thermal resistance θ_{jc} versus time is essential. The best approach is plotting θ_{jc} versus time in a semi-log scale for several duty cycles. In order to perform transient thermal analysis, density and specific heat material properties must be used in addition to thermal conductivity for time constant calculations of each material. The density and specific heat values used are listed in Table VI.

Fig. 42 shows the transient thermal response of a 28.8-mm gatewidth GaN HEMT device in a 60-mil-thick CMC package dissipating 8 W/mm of power at 10%, 20%, 50% duty cycles. The transient response shows two distinct slopes of resistance versus time prior to full thermal saturation at approximately 400 ms. These two slopes can be attributed to the different transient thermal properties of the die and package. Fig. 43 shows how performing a transient thermal analysis with the same die, but mounted into a 40-mil-thick CuW package has the same thermal response during the first 100 ms, but is significantly

TABLE VI
MATERIAL PROPERTIES FOR TRANSIENT THERMAL ANALYSIS

Material	Density (gm/cm ³)	Specific Heat (J/KgC)
GaN	6.1	490
SiC	3.1	681
Au	19.32	126
AuSn	14.5	150
Cu	8.3	385
Mo	10.3	250

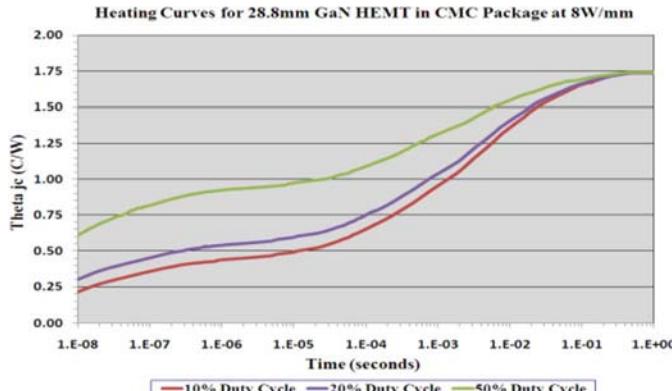


Fig. 42. Thermal resistance versus time for a 28.8-mm gatewidth GaN HEMT.

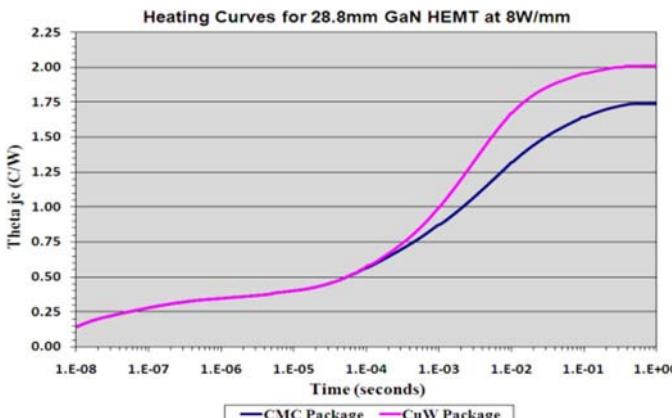


Fig. 43. Transient response of 28.8-mm gatewidth GaN HEMT in two different packages.

different after this point. The thermal resistance increase of the device with the CuW package can be explained by the slower thermal response of the material.

X. ROBUSTNESS

GaN HEMTs have been shown to survive output voltage standing-wave ratio (VSWR) mismatches well compared to Si LDMOSFETs and GaAs FETs. This can result in eliminating or simplifying protection circuitry and reducing field failure rates. The robustness is directly linked to the ability of the devices to handle large voltage and current swings for both transmitted and reflected RF power, as well as to deal with increased heat dissipation. Most GaN transistors are specified to withstand a 10:1 output mismatch VSWR at fully rated output power. For example, Quay *et al.* [63] have described a series of mismatch

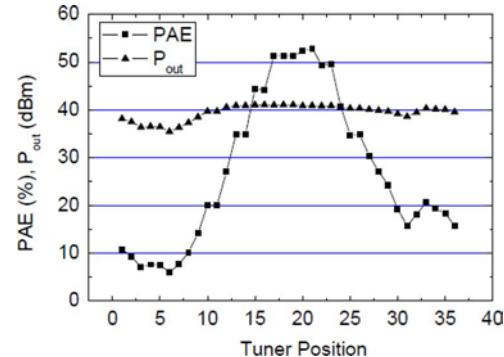


Fig. 44. Output power and PAE of nominal 30-W PA versus 10:1 VSWR mismatch [63].

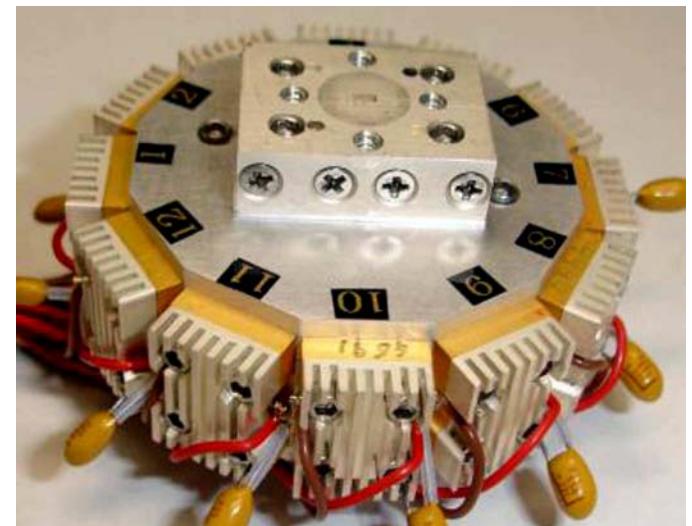


Fig. 45. Twelve 95-GHz GaN HEMT MMIC modules in a low-loss radial line combiner arrangement.

stress testing on a nominal 30-W device operating at 50 V under 10:1 VSWR. Fig. 44 shows the resultant degradation in output power and PAE as a function of output tuner position. The PAE, under certain tuner positions, can be as low as 7% with a corresponding drop in RF power to 4 W with a maximum channel temperature of 278 °C—even so the device did not fail.

XI. OTHER DEVELOPMENTS

Although commercially available GaN HEMT transistors and MMICs today are concentrated at frequencies below 18 GHz, a considerable amount of work has been achieved at much higher frequencies, indicating the potential for short gate-length devices. For example, Micovic *et al.* [64] have reported promising results for MMIC PAs at 88 GHz. The authors used $4 \times 37.5 \mu\text{m}$ wide devices having a gate length of $0.15 \mu\text{m}$ as the basic unit cell building blocks. The devices had extrinsic peak transconductances exceeding 360 mS/mm at $V_{DS} = 10 \text{ V}$, I_{DSS} of 0.8 A/mm , I_{MAX} of 1.2 A/mm , f_T exceeding 90 GHz, and f_{MAX} exceeding 200 GHz. Three-stage MMIC PAs had small-signal gains of 19.6 dB at 84 GHz. The peak power of a MMIC-based module was 842 mW at a drain bias of 14 V and a frequency of 88 GHz. Associated PAE of the

module at peak output power was 14.8% with associated gain of 9.3 dB. The output power of the module exceeded 560 mW over 84–95 GHz. Schellenberg *et al.* [65] have produced a solid-state PA with an output power of 5.2 W at 95 GHz and greater than 3 W over the 94–98.5-GHz band employing such MMICs. The results were achieved by combining 12 of the MMICs in a low-loss radial line combiner network, as shown in Fig. 45.

XII. CONCLUSION

This paper has attempted to give a broad review of GaN HEMTs in terms of their wide-bandgap advantages over other semiconductor technologies. An overview of a typical AlGaN/GaN on SiC manufacturing technology was followed with a review of small- and large-signal models allowing the accurate design of both hybrid and monolithic circuits. An extensive description of various examples of broadband and high-efficiency PAs was given and followed by comments on thermal management and robustness. GaN HEMT technologies and applications have been and continue to be some of the most challenging and exciting in the RF and microwave industry [66].

ACKNOWLEDGMENT

The authors would like to thank numerous colleagues and coworkers for their successful work on wide-bandgap transistors, hybrid, and MMIC PAs. Acknowledgements are made particularly to those referenced authors that have provided examples of PAs covering a wide range of frequencies and power levels.

REFERENCES

- [1] *RF and Microwave Semiconductor Handbook*, M. Golio, Ed.. Boca Raton, FL: CRC, 2003, ch. 3, p. 3.
- [2] D. Hobgood, M. Brady, W. Brixius, G. Fechko, R. Glass, D. Hennishall, J. Jenny, R. Leonard, D. Malta, S. G. Muller, V. Tsvetkov, and C. Carter, "Status of large diameter SiC crystal growth for electronic and optical applications," *Silicon Carbide Rel. Mater.*, 1999 (Part I), *Mater. Sci. Forum*, vol. 338–342, pp. 3–8, 2000.
- [3] S. T. Sheppard, W. L. Pribble, D. T. Emerson, Z. Ring, R. P. Smith, S. T. Allen, J. W. Milligan, and J. W. Palmour, "Technology development for GaN/AlGaN HEMT hybrid and MMIC amplifiers on semi-insulating SiC substrates," in *Proc. IEEE/Cornell High Perform. Devices Conf.*, Ithaca, NY, Aug. 7–9, 2000, pp. 232–236, IEEE Cat. 00CH37122.
- [4] S. McGrath and T. Rodle, "Moving past the hype: Real opportunities for wide bandgap compound semiconductors in RF power markets," *CSManTech On-Line Dig.* 2005. [Online]. Available: <http://www.csmantech.org/Digests/2005/index2005.html>, Paper 1.4
- [5] F. Yamaki, K. Inoue, N. Ui, A. Kawana, and S. Sano, "A 65% drain efficiency GaN HEMT with 200 W peak power for 20 V to 65 V envelope tracking base station amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, Jun. 2011, Flash Drive.
- [6] E. Mitani, M. Aojima, A. Maekawa, and S. Sano, "An 800-W AlGaN/GaN HEMT for S-band high-power application," *CSManTech On-Line Dig.* 2007. [Online]. Available: <http://www.csmantech.org/Digests/2007/2007%20Papers/11b.pdf>
- [7] R. Gaka, J. W. Wang, A. Osinsky, Q. Chen, M. A. Khan, A. O. Orlov, G. L. Snider, and M. S. Shur, "Electron transport in AlGaN–GaN heterostructures grown on 6H-SiC substrates," *Appl. Phys. Lett.*, vol. 72, no. 6, pp. 707–709, Feb. 1998.
- [8] B. P. Keller *et al.*, "Metalorganic chemical vapor deposition growth of high optical quality and high mobility GaN," *J. Electron. Mater.*, vol. 24, pp. 1707–1709, Nov. 1995.
- [9] S. Keller *et al.*, "Metalorganic chemical vapor deposition of high mobility AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 86, pp. 5850–5857, Nov. 1999.
- [10] I. P. Smorchkova *et al.*, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," *J. Appl. Phys.*, vol. 86, no. 8, pp. 4520–4526, Oct. 1999.
- [11] Y. F. Wu, S. M. Wood, R. P. Smith, S. Sheppard, S. T. Allen, P. Parikh, and J. Milligan, "An internally-matched GaN HEMT amplifier with 550-watt peak power at 3.5 GHz," in *Int. Electron Devices Meeting*, Dec. 11–13, 2006, pp. 1–3.
- [12] Y. F. Wu *et al.*, "Very high breakdown voltage and large transconductance realized on GaN heterojunction field-effect transistors," *Appl. Phys. Lett.*, vol. 69, pp. 1438–1440, Sep. 1996.
- [13] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzman, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3333, 1999.
- [14] Y. F. Wu, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, pp. 586–590, 2001.
- [15] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 21, no. 6, pp. 268–270, Jun. 2000.
- [16] M. Rosker, "Wide bandgap semiconductor devices and MMICs: A DARPA perspective," in *Int. Compound Semiconduct. Manuf. Technol. Conf.*, New Orleans, LA, Apr. 2005, p. 1.2.
- [17] L. Shen, S. Heikman, B. Moran, R. Coffie, N. Q. Zhang, D. Buttari, I. P. Smorchkova, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/AlN/GaN high-power microwave HEMT," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 457–459, Oct. 2001.
- [18] S. C. Binari, H. B. Dietrich, G. Kelner, L. B. Rowland, K. Doverspike, and D. K. Wickenden, "H, He, and N implant isolation of n-type GaN," *J. Appl. Phys.*, vol. 78, no. 5, pp. 3008–3011, 1995.
- [19] Y. F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," in *64th Device Res. Conf.*, Jun. 2006, pp. 151–152.
- [20] Y. Okamoto, Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki, N. Shibata, and M. Kuzuhara, "Improved power performance for a recessed-gate AlGaN–GaN heterojunction FET with a field-modulating plate," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2536–2540, Nov. 2004.
- [21] L. Dunleavy, C. Baylis, W. Curtice, and R. Connick, "Modeling GaN: Powerful but challenging," *IEEE Microw. Mag.*, pp. 83–96, Oct. 2010.
- [22] J. Wood and D. Root, "A symmetric and thermally-de-embedded nonlinear FET model for wireless and microwave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2004, pp. 35–38.
- [23] J. Verspecht and D. E. Root, "Polyharmonic distortion modeling," *IEEE Microw. Mag.*, no. 3, pp. 44–45, Jun. 2006.
- [24] H. Statz, P. Newman, I. Smith, R. Pucel, and H. Haus, "GaAs FET device and circuit simulation in spice," *IEEE Trans. Electron Devices*, vol. ED-34, no. 2, pp. 160–169, Feb. 1987.
- [25] A. Materka and T. Kacprzak, "Computer calculation of large-signal GaAs FET amplifier characteristics," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-33, no. 2, pp. 129–135, Feb. 1985.
- [26] W. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-33, no. 12, pp. 1383–1393, Dec. 1985.
- [27] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 12, pp. 2258–2266, Dec. 1992.
- [28] C. Fager, J. C. Pedro, N. B. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 12, pp. 2834–2842, Dec. 2002.
- [29] K. Jeon, Y. Kwon, and S. Hong, "A frequency dispersion model of GaAs MESFET for large-signal applications," *IEEE Microw. Guided Wave Lett.*, vol. 7, no. 3, pp. 78–80, Mar. 1997.
- [30] E. Filseth and M. Jachowski, "SPICE extensions dynamically model thermal properties," *EDN*, pp. 169–180, Apr. 1988.
- [31] A. Lazarò, L. Pradell, and J. O'Callaghan, "FET noise-parameter determination using a novel technique based on 50-Ω noise-figure measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 3, pp. 315–324, Mar. 1999.
- [32] L. Dunleavy, 2009, Modelithics Inc., private communication.

- [33] D. Fitzpatrick and I. Miller, *Analog Behavioral Modeling With the Verilog-A Language*. Norwell, MA: Kluwer, 1998.
- [34] A. M. Darwish, A. Bayba, and H. A. Hung, "Thermal resistance calculation of AlGaN/GaN devices," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2611–2620, Nov. 2004.
- [35] N. Tuffy, A. Zhu, and T. J. Brazil, "Class-J RF power amplifier with wideband harmonic suppression," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, Jun. 2011, Flash Drive.
- [36] J. Moon, J. Kim, and B. Kim, "Investigation of a class-J power amplifier with a nonlinear cout for optimized operation," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 11, pp. 2800–2811, Nov. 2010.
- [37] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Norwood, MA: Artech House, 2006.
- [38] P. J. Tasker, "Practical waveform engineering," *IEEE Microw. Mag.*, pp. 65–76, Dec. 2009.
- [39] S. El-Hamamsy, "Design of high efficiency RF class-D power amplifier," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 297–308, May 1994.
- [40] S. Lin, M. Eron, and S. Turner, "Development of broadband amplifier based on GaN HEMTs," in *IEEE Wamicon Conf. Dig.*, Clearwater, FL, Apr. 2011, CD.
- [41] V. Carrubba, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A novel highly efficient broadband continuous class-F RFPA delivering 74% average efficiency for an octave bandwidth," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, Jun. 2011, Flash Drive.
- [42] S. Lin and A. E. Fathy, "A 20 W GaN HEMT VHF/UHF class-D amplifier," in *IEEE Wamicon Conf. Dig.*, Clearwater, FL, Apr. 2011, CD.
- [43] K. Shi, D. A. Calvillo-Cortes, L. C. N. de Vreede, and F. van Rijs, "A compact 65 W 1.7 to 2.3 GHz class-E GaN power amplifier for base-stations," in *Eur. Microw. Conf. Dig.*, Manchester, U.K., Oct. 2011, pp. 542–545.
- [44] G. W. Choi, H. J. Kim, W. J. Hwang, S. W. Shin, J. J. Choi, and S. J. Ha, "High efficiency class-E tuned Doherty amplifier using GaN HEMT," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2009, pp. 925–928.
- [45] T. K. Moushaan and K. M. Faulkner, "Load pull analysis of Chireix outphasing class-E power amplifiers," in *Proc. Asia-Pacific Microw. Conf.*, Dec. 2009, pp. 2180–2183.
- [46] M. P. van der Heijden, M. Acar, J. S. Vromans, and D. A. Calvillo-Cortes, "A 19 W high-efficiency wideband CMOS-GaN class-E chireix RF outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, Jun. 2011, Flash Drive.
- [47] D. Schmelzer and S. I. Long, "A GaN HEMT class F amplifier at 2 GHz with >80% PAE," in *IEEE Compound Semiconduct. IC Symp.*, 2006, pp. 96–99.
- [48] B. Kim, I. Kim, and J. Moon, "Advanced Doherty architecture," *IEEE Microw. Mag.*, vol. 5, pp. 72–86, Aug. 2010.
- [49] A. Grebenikov, "A high-efficiency 100-W four-stage Doherty GaN HEMT power amplifier module for WCDMA systems," in *ARMMS Conf.*, Apr. 2011. [Online]. Available: www.armms.org
- [50] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N. de Vreede, "A high-efficiency 100-W GaN three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 7, pp. 1582–1591, Jul. 2008.
- [51] W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing, and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient N-way Doherty amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 5, pp. 866–879, May 2007.
- [52] P. Draxler, S. Lanfranco, D. Kimball, C. Hsia, J. Jeong, J. Van de Sluis, and P. M. Asbeck, "High efficiency envelope tracking LDMOS power amplifier for W-CDMA," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2006, pp. 1534–1537.
- [53] C. Steinbeiser, T. Landon, G. Burgin, O. Krutko, J. Haley, P. Page, D. Kimball, and P. M. Asbeck, "HVHBT Doherty and envelope tracking PAs for high efficiency WCDMA and WiMAX basestation applications," in *IEEE Power Amplifier Symp.*, Jan. 2009, pp. 57–61.
- [54] A. Cidronali, N. Giovannelli, T. Vlasits, R. Hernaman, and G. Manes, "A 240 W dual-band 870 and 2140 MHz envelope tracking GaN PA designed by a probability distribution conscious approach," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Baltimore, MD, Jun. 2011, Flash Drive.
- [55] S. Wood, C. Platis, D. Farrell, B. Millon, B. Pribble, P. Smith, R. Pengelly, and J. Milligan, "Advances in high power GaN HEMT transistors," *Microw. Eng. Europe*, pp. 2–7, May 2009.
- [56] J. Beyer, S. N. Prasad, R. Becker, J. E. Nordman, and G. K. Hohenwarter, "MESFET distributed amplifier design guidelines," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-32, no. 3, pp. 268–275, Mar. 1984.
- [57] G. Vendelin, A. Pavio, and U. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*. Hoboken, NJ: Wiley, 2005.
- [58] A. Inoue, S. Goto, T. Kunii, T. Ishikawa, and Y. Matsuda, "A high efficiency, high voltage, balanced cascode FET," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2005, pp. 669–672.
- [59] J. Kwack, K. Kim, and S. Cho, "1 kW S-band solid state radar amplifier," in *IEEE Wamicon Conf. Dig.*, Clearwater, FL, Apr. 2011, CD.
- [60] A. Prejs, S. Wood, R. Pengelly, and W. Pribble, "Thermal analysis and its application to high power GaN HEMT amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Boston, MA, Jun. 2009, pp. 917–920.
- [61] K. Loufty, "Aluminum diamond meets cost and technical challenges for removing heat from GaN devices," *Microw. Product Dig.*, pp. 14, 54–60, Jun. 2011.
- [62] O. Vendier *et al.*, "AGAPAC: Advanced GaN package for space," Thales Alenia Space, France. [Online]. Available: http://ec.europa.eu/enterprise/newsroom/cf/_getdocument.cfm?doc_id=6484, O. Vendier, Proj. Coordinator
- [63] R. Quay, M. Musser, F. van Raay, T. Maier, and M. Mikulla, "Managing power density of high-power GaN devices," in *IEEE MTT-S Int. Microw. Symp. Workshop Dig.*, Boston, MA, 2009, pp. 71–86, Workshop Notes WMF "Is GaN ready for system insertion?"
- [64] M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, M. Hu, A. Corrion, A. Fung, R. Lin, L. Samoska, P. Kangaslahti, B. Lambriksen, P. Goldsmith, W. S. Wong, A. Schmitz, P. Hashimoto, P. J. Willadsen, and D. H. Chow, "W-band GaN MMIC with 842 mW output power at 88 GHz," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2010, Flash Drive.
- [65] J. Schellenberg, E. Watkins, M. Micovic, B. Kim, and K. Han, "W-band, 5 W solid-state power amplifier/combiner," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2010, Flash Drive.
- [66] R. Quay, *Gallium Nitride Electronics*, ser. Mater. Sci. Berlin, Germany: Springer, 2008.



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Mr. Pribble has contributed to a number of IEEE Microwave Theory and Techniques Society (IEEE MTT-S) workshops.

APPENDIX II-5

TRANSISTOR MODELS

Nonlinear Modeling of Compound Semiconductor HEMTs

State of the Art

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Abstract — This paper will review the state-of-the-art for modeling compound semiconductor HFETs and HEMTs for microwave power applications. Some simple physics shows why SPICE models, or compact models, cannot contain all aspects of the device operation. Because the models are incomplete, any given model may always be improved and thus, modifiable user-defined compact models are preferred. In particular, Verilog-A coded models are shown to have many desirable features. Minimum modeling requirements for accurate system and circuit simulation are described, as well as present modeling techniques.

Index Terms — Transistors, MODFETs, SPICE, simulation software, power amplifiers.

I. INTRODUCTION

This paper will review some modeling principles and useful techniques for constructing HEMT models for accurate circuit simulation. A more thorough review of present-day modeling techniques for HEMTs and bipolar transistors is given by Curtice [1] and by Root [2].

The models used for circuit simulation are, at best, a simplified approximation of the important physics of the HEMT. The most physical model would be a two or three-dimensional internal model of the device, which includes the charge transport physics for both electrons and holes and their time-domain behavior. Such models have been constructed using the ATLAS program. However, this type of model can only be used for very simple circuits due to the lengthy execution time. The “SPICE” program introduced “compact” models to mimic the important behavior of transistors by permitting efficient simulation of complex transistors circuits. However, the amount of physics in a compact model determines the number of model parameters. Many aspects of transistor behavior are omitted in these models. But, because the model parameters provide currents as an analytical function of applied voltages, extensive look-tables are not needed and the model is very “compact.”

A discussion of the “velocity overshoot” in short gate-length HEMTs will be given to introduce the complexity of the internal physics of the HEMT. Then, the types of HEMT models and coding techniques will be discussed. Because the

models have only limited physical behavior, any given model can always be improved for better performance in any given application. It is therefore important then to work with HEMT models that can be easily modified. A popular approach is the Verilog-A coded model. Coding time is much less than other methods and it can be used in all commercial circuit simulators.

The testing equipment need for parameter extraction for compact models is described. The most import addition to earlier approaches is the use of short-pulse current-voltage measurements with controlled quiescent biasing. This equipment permits evaluation of temperature effects and charge trapping effects, both of which are important in compound semiconductor HEMTs.

II. CHARGE TRANSPORT IN SEMICONDUCTORS

Electron transport in an N-type semiconductor is collision-dominated, like an “electron gas.” Thus, the current produced in a “long” N-type semiconductor with ohmic contacts is proportional to electron mobility and the voltage applied. This is simply, Ohm’s Law! The electron drift velocity is equal to the product of mobility and electric field.

However, HEMTs used for microwave operation have very short gate length and “ballistic” behavior occurs when low energy electrons (with large mobility) are injected into the large electric field under the gate. In this case the product of electron mobility and electric field is a velocity much larger than the steady-state velocity observed in a long sample. As the electron gains energy, its mobility and velocity are reduced. This effect is called “velocity overshoot” and Figure 1 shows an overshoot calculation made for GaN semiconductor [3]. Short gate length produces very large velocity whereas the longer gate length gives steady-state velocity.

The larger velocity causes a shorter gate transit time and a larger F_t for the HEMT. The effect in GaAs and GaN is much stronger than for silicon because the electron mobility is much larger than for silicon.

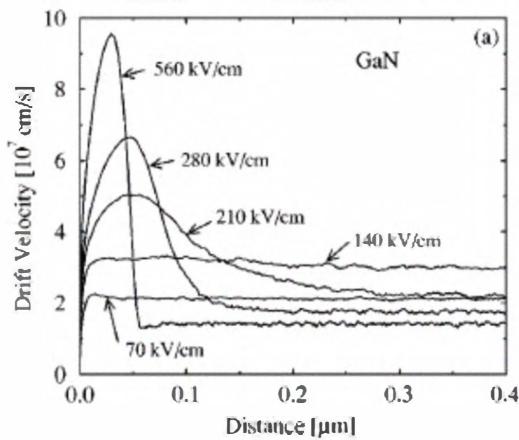


Fig. 1 Calculated electron drift velocity vs. distance for GaN

This effect and trapping effects are not easily reproduced in a compact model. Gate length might be a parameter in the model, but it cannot account for the physics present during a change in velocity overshoot due to a change in gate length. Measurements of the gate and drain currents as functions of voltages will not give enough information to make the model follow the internal physics of the device.

This effect clearly shows why one cannot scale transistor models with gate length. Scaling with gate width is also difficult because of the variation of field and charge across the width. However, scaling by the number of gate fingers is often accurate as long as the parasitic elements are not greatly different.

This example clearly shows external HEMT measurements cannot be used to make a truly physical compact model. In fact, all compact models will behave non-physically in some measurement condition!

III. COMPACT MODELS

C-coded and Verilog-A coded models may be used with many simulators. Often, a simulator will also provide a simpler approach to modeling, such as the Symbolically Defined Device model, or the SDD model in Agilent Technologies' Advance Design System, or ADS. However, models such as the SDD model often do not contain accurate derivative expression and produce convergence problems during simulation. The C-coded model must contain such derivative expressions, whereas, the Verilog-A code need not [4].

A good comparison of C-code and Verilog-A coding is the C_HEMT model for ADS developed by W. R. Curtice Consulting. C-coding requires about 1100 lines of code. Verilog-A coding requires only 210 lines of code. Both

versions run well in ADS. In addition, the same Verilog-A code may be used for producing a model in Microwave Office (AWR) and Spectre (Cadence Design Systems, Inc.) circuit simulators.

An example of the use of C_HEMT model for a GaN/SiC HEMT is shown in Figure 2. Here it is seen that the model provides separate measurement of the total drain current, I_{DS} , and the internal drain-source current without capacitive currents, I_{DS_int} . Figure 3 shows that the model gives good agreement for the tuned GaN amplifier at 10 GHz. Figure 4 shows the dynamic load lines on top of the IV characteristic. The presentation permits understanding of the dynamic operation of the amplifier. Figure 5 shows how the external meter provides far less insight into the dynamic operation.

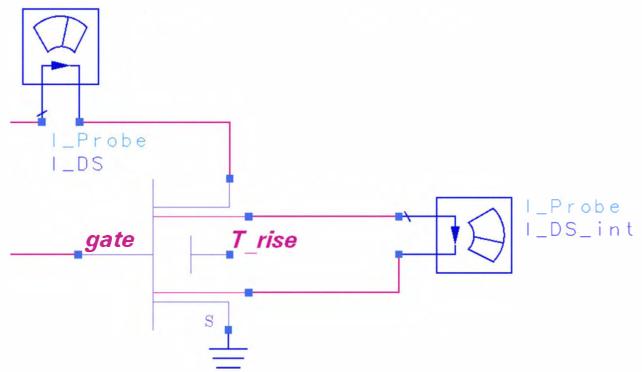


Fig. 2 C_HEMT model with two drain current measurements

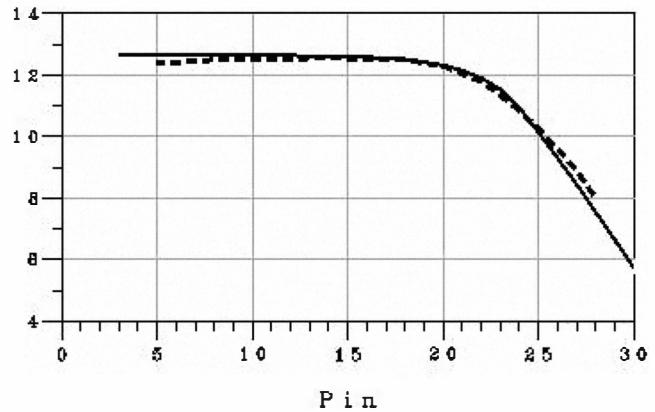


Fig. 3 Gain(dB) for data and model (full curve) for 10 GHz amplifier

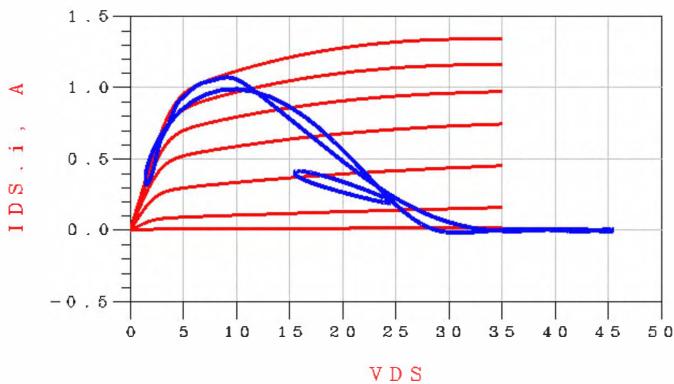


Fig. 4. Dynamic load line for $P_{in} = 10$ and 20 dBm and device IV characteristics using I_{DS_int}

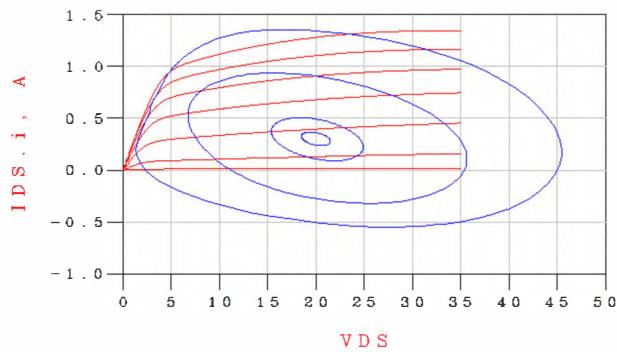


Fig. 5. Dynamic load lines for $P_{in} = 0, 10, 20$ and 30 dBm and device IV characteristics using I_{DS} .

IV. MODELING USING THE VECTOR NETWORK ANALYZER

A large-signal waveform measurement system has been used by several researchers to measure transistor IV characteristics dynamically. Demmler and Tasker [5] have shown such measurements. Wei et al. [6] used such data for model extraction for a GaAs HBT. Curras-Francos [7] clearly explain extraction to a table-based model for a 4×60 μm GaAs HEMT. Schreurs, Verspecht et al. [8] have shown how a model is produced from such data for a GaAs HEMT operating with class B biasing. Their initial extraction is for the Angelov model and then, to extend the useful frequency range, an ANN (Artificial Neural Network) model is constructed.

This technique is still evolving. However, it is not clear that such a model will be as useful as a compact model. It is clear that the vector network-based model is not scalable or easily tailored for improved performance in a specific application. How to deal with pulsed applications, trapping effects and breakdown effects that vary as a function of biasing conditions needs to be addressed. However, the Vector Network measurements are clearly helpful in verification of a model, such as a compact model.

V. COMPACT MODELS CONSTRUCTED USING PULSED IV DATA

The use of a dynamic I-V analyzer, such as DiVA or the Agilent Technologies 85124A, has provided important modeling data in which the heating effects and charge trapping effects are controlled. Pulsed biasing with pulse length less than 1 μs for low duty cycle permits measurement of device currents without appreciable heating effects. Such systems permit separate setting of the quiescent state voltages, that is, the voltage on the device terminals between current pulses. This permits control of the slow state trapping effects during the testing. In many cases, pulsed S-parameter can be measured. Many companies have constructed their own version of such equipment. When this equipment is not available, such pulsed data can be obtained from external vendors.

The HEMT models created using pulsed IV systems are clearly superior to previous methods. The improvement in the model becomes more important for large periphery devices.

Such testing has shown that the RF and DC IV transconductance in GaN HEMTs are often of different values. This occurs due to trapping effects and the model for the device should show the same behavior to be accurate. The popular Angelov model [10] installed in ADS and MWO does not have this ability.

Short pulse IV measurements were used as early as 1985 to characterize the drain-gate breakdown behavior in GaAs MESETs [9]. Present-day equipment is superior to this equipment.

VI. IMPROVING EXISTING MODELS

The Angelov model is available in many simulators. It is electro-thermal but has several deficiencies. One is that the parameters for the gate charge equations are difficult to evaluate. In addition, the ADS2009U2 installed Angelov model does not include drain-gate breakdown. This effect is particularly important in GaAs devices. The model parameters LSBO and VTR relate to increases in the drain-source current caused by increased drain-source voltage and only involve drain and source currents, not gate current. This would have to be corrected for simulation of devices with appreciable breakdown effects.

Rather than start from scratch to correct this, one can start with the Verilog-A version, which is also contained in ADS. In general, one will want to improve or update any existing model that proves useful and accurate. Because of the lack of real physics in a compact model, improvements will continually be desired. A model is, in fact, never finished.

An additional feature of the compact model is that one may perform "what if" simulations. For example, the expected

performance of a 10-finger device can be based upon the model for the 2-finger device. The expected performance obtained if drain-gate capacitance is increased by adding a "field plate" could be predicted, as well as for other changes.

VII. REQUIREMENTS FOR AN ACCURATE HEMT MODEL

The following characteristics are preferred for an acceptable HEMT model:

- a. Good accuracy over the expected range of voltages, frequencies and temperatures
- b. An uncomplicated parameter extraction process with a reasonable number of model parameters
- c. If periphery is larger than 1mm, model must be electro-thermal to include self-heating effects properly
- d. Must include important breakdown effects, such as gate-drain and gate-source breakdown
- e. Must be able to be easily modified by the user
- f. Accurate scaling by the number of fingers is desirable
- g. Include important trapping effects and their dependence upon biasing conditions
- h. For system simulations the model must be able to predict IMD3 accurately (and IMD5, if possible)
- i. Must have good convergence properties in harmonic-balance, envelope and time-domain simulations

transistors," IEEE Trans. on Microwave Theory & Tech., 43, pp 2899-2905, 1995.

- [7] Curras-Francos, "Table-based nonlinear HEMT model extracted from time-domain large-signal measurements," IEEE Trans on Microwave Theory & Tech., Vol. 53, pp1593-1600, 2005.
- [8] Schreurs, Verspecht et al., Straightforward ... device model parameter estimation method based on vector large-signal measurements, IEEE Trans. on Microwave Theory & Tech., Vol. 50, pp. 2315-2319, 2002
- [9] Curtice and Ettenberg, "A Nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," IEEE Trans. on Microwave Theory & Tech., Vol. MTT-33, p.1383-1394, 1985
- [10] Angelov, Zirath and Rorsman, "New empirical nonlinear model for HEMT and MESFET devices," IEEE Trans. Microwave theory & Tech., Vol 40, pp 2258-2266, Dec. 1992.

REFERENCES

- [1] Curtice, *RF and Microwave Handbook*, Second Edition, CRC Press,[Editor] Mike Golio, p 32-1 - 32-25, 2008.
- [2] Root, "Nonlinear FET Modeling Fundamentals and Neural Network Applications," Presented at Advances in Active Device Characterization & Modeling for RF and Microwave, 2007 IEEE MTT-S International Microwave Symposium, Hawaii, June 2007.
- [3] Foutz, O'Leary, Shur and Eastman, Journal of Applied Physics, Vol. 85, No. 11, 1 June 1999.
- [4] The Designer's Guide to Verilog AMS, Kluwer Academic Publishers, Norwell, MA, 2004
- [5] Demmler and Tasker, "A vector correction...," Presented at the workshop on new direction in nonlinear RF and Microwave Characterization, 1996 International Microwave Symposium, 1996.
- [6] Wei et al., "Waveform-based modeling and characterization of microwave power heterojunction

Converting GaAs FET Models For Different Nonlinear Simulators

INTRODUCTION

This paper addresses the issues involved in converting GaAs models for different nonlinear simulators.

There may be slight differences in the way a model is implemented in commercial simulators. These differences can usually be reconciled by consulting the simulator's accompanying documentation, mapping parameters from one simulator to another, recognizing default values of parameters and their effects, and modifying the simulation schematic.

The high frequency output conductance network can be implemented external to the nonlinear model with good results.

Although the same model exists in multiple simulators, each simulator may use slightly different variable names. For example, most GaAs FET models contain a zero bias gate-source junction capacitance. In PSPICE and MDS this capacitance is defined as the variable CGS; in LIBRA and COMPACT it is defined as CGSO. These differences require the user to translate model parameters to conform to the syntax of their specific simulator.

Another example where conversion is necessary is when one simulator implements circuit elements inherent to the nonlinear model, but these elements do not exist in the basic nonlinear model of other simulators. One such instance is with a series RC network shunting the output of the Triquint FET model (TOM) in the Libra simulator. This RC network is integral to the Libra TOM but nonexistent in the MDS and PSPICE simulators. The Libra TOM parameters can be used in PSPICE after some minor conversions.

There are many different GaAs FET models in use today. California Eastern Laboratories (CEL) uses the model that fits the widest range of biases and frequencies possible. In addition, nonlinear models are chosen that are available in most commercial simulators.

GaAs FET MODELS

Three nonlinear GaAs FET models are the Curtice[2], the Statz-Pucel [3], and the TOM (Triquint's Own Model) [4]. The Curtice model was one of the first high frequency nonlinear GaAs FET models to be implemented in commercial simulators. This model does an excellent job of predicting device behavior for a single bias point. For a wide range of biases however, CEL has found that the Curtice model doesn't fit the measured AC and DC performance simultaneously with the same set of model parameters as accurately as the TOM and Statz models. CEL's modeling philosophy is to fit the widest range of biases and frequencies as possible, therefore, the TOM and Statz models are used for our generic multi-bias model.

MODEL DESCRIPTION

There are two major differences between the TOM and Statz models: (1) how the DC drain-source current is modeled, and (2) how the high frequency output conductance is modeled. The DC drain-source current formulation is reviewed. The DC I-V curve equations for the Statz and TOM are implemented the same in the four simulators evaluated and are therefore not reviewed.

Next, the high frequency output conductance model differences are reviewed. Unlike the DC drain-source current, simulator implementations of the high frequency output conductance are different and are therefore included in this review.

DC drain-source current

The Statz DC I-V curves (Figure 1) result in an almost *constant* drain current with increasing drain voltage at lower gate voltages. The TOM in comparison (Figure 2) exhibits an almost *linear increase* in drain current with increasing drain voltage. At higher drain voltages, the I-V curves in the Statz model exhibit an approximate *linear increase* in drain current with respect to drain voltage, while the TOM drain current becomes approximately *constant* with increasing drain voltage.

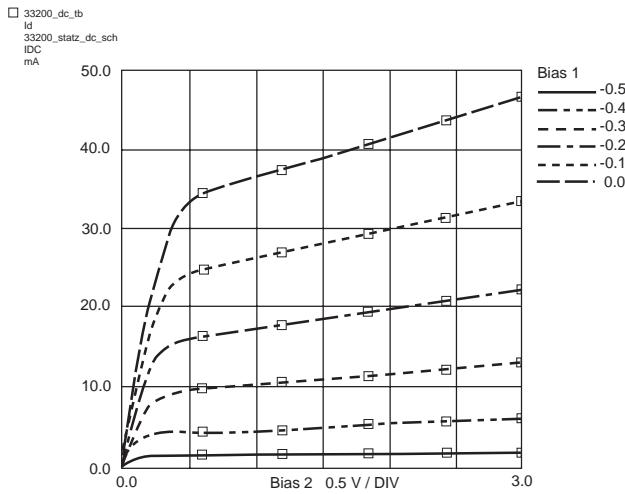


Figure 1. NEC NE33200 Modeled IV curves using the Statz Model.

Model differences can be quantified by scrutinizing how each author formulates the DC drain-source current. Since the Statz and TOM models are modified versions of the Curtice equation, we will first examine the Curtice model DC I-V curve formulation.

The Curtice model defines the drain current with respect to the drain-source and gate-source voltages as:

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (1)$$

where V_{TO} is the threshold voltage, β , λ , and α are model parameters.

The Statz model modifies Curtice's formulation, equation (1), by replacing the more computationally intensive hyperbolic tangent function with a truncated series representation. More importantly, the Statz model changes I_{ds} such that the square-law approximation is only in effect for small $(V_{gs} - V_{TO})$ values. For larger values of $(V_{gs} - V_{TO})$, I_{ds} becomes almost linear.

The Statz I_{ds} equation then becomes:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{\beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) [1 - [1 - (\alpha V_{ds})/3]^3]}{1 + b(V_{gs} - V_{TO})} \quad (2)$$

for $0 < V_{ds} < 3/\alpha$

and:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{\beta(V_{gs} - V_{TO})^2 (1 + \lambda V_{ds})}{1 + b(V_{gs} - V_{TO})} \quad (3)$$

for $V_{ds} \geq 3/\alpha$

where $[1 - [1 - (\alpha V_{ds})/3]^3]$ is the truncated series representation of $\tanh(\alpha V_{ds})$ and β is a model parameter.

The Statz model only fits drain conductance for small ranges of drain current. When larger ranges of drain current are simulated, the Statz model tends to predict a conductance that is too large.

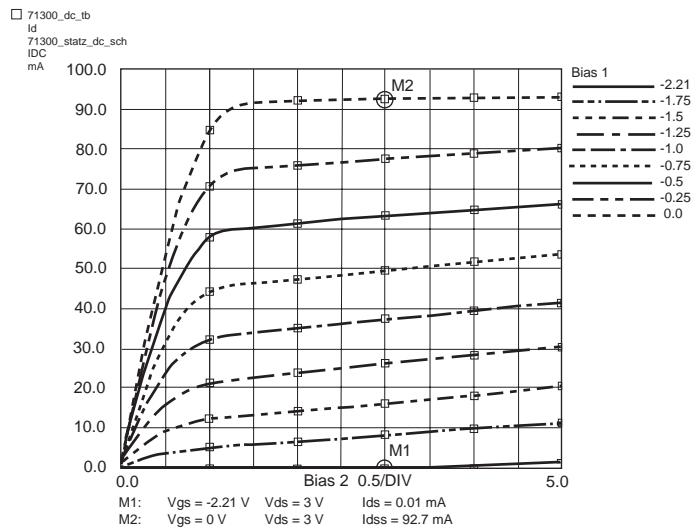


Figure 2. NEC NE71300 Modeled IV Curves using TOM.

TOM recognized the fact that not all device behavior is well predicted by the square-law assumption, so the exponent in the expression $(V_{gs} - V_{TO})^2$ is changed from a constant 2 to the variable Q . For the TOM, the drain-source current becomes:

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^Q [1 - [1 - (\alpha V_{ds})/3]^3] \quad (4)$$

and:

$$I_{ds}(V_{gs}, V_{ds}) = \beta(V_{gs} - V_{TO})^Q \quad \text{for } V_{ds} \geq 3/\alpha \quad (5)$$

with:

$$I_{ds}(V_{gs}, V_{ds}) = \frac{I_{ds0}}{1 + \delta(I_{ds0})(V_{ds})} \quad (6)$$

The TOM also uses a parameter δ to model the decreased drain conductance at low gate-source biases. TOM also allows for scaling of V_{TO} , or pinch-off voltage, to account for drain-source voltage dependence.

How the equations relate to actual device performance is shown above in Figures 1 and 2. These figures show modeled I-V curves derived from the above equations. The models match actual device measurements quite well. Figure 1 is a model of the NEC NE33200 I-V curves using the Statz model. Figure 2 is a model of the NEC NE71300 I-V curves using TOM. Both models are those implemented by the HP-EEsof Series IV Libra simulator.

High Frequency Output Conductance Model

The high frequency output conductance model for the Statz and TOM models is best illustrated by examining the schematics in Figure 3 and Figure 4. For the Statz model of Figure 3, the drain-source series RC network (CRF and RC) provides a correction to the AC output conductance at a specific bias condition. To implement a full bias range model, the RC network is tuned at a bias in the middle of the bias range. In the TOM, Figure 4, the drain-source RC network (Cbs and Rdb) controls the frequency when the

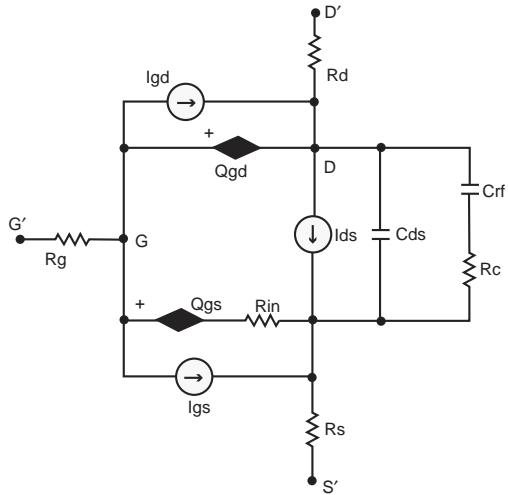


Figure 3. Statz Model Schematic, Libra Series IV.

current source I_{db} becomes a factor. As with the Statz model, TOM is tuned to the measured data in the middle of the device's bias range.

Simulator Implementation

The ability to specify the high frequency output conductance is not programmed in all simulator models. To determine if the Statz model or TOM you are using in your simulator has this compensation built in, inspect the nonlinear model simulator documentation.

If the compensation is not programmed into the simulator model, you can implement the output conductance by adding the RC network as and external resistor and capacitor as shown in Figure 6. The components RDB and CBS in Figure 6 represent this external compensation. PSPICE and MDS are two of the nonlinear simulators that do not have the output conductance programmed into their TOM.

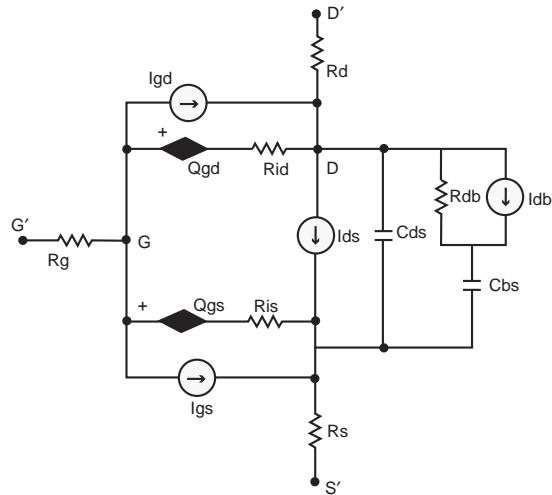


Figure 4. TOM Schematic, Libra Series IV.

OUTPUT CONDUCTANCE CONVERSION

The following example shows how to convert *Libra Series IV* TOM into *PSPICE* TOM. This example uses the NE71300 L to K band low noise N-Channel GaAs MESFET device. This is a 280 μ m gate width by 0.3 μ m gate length device with a typical noise figure of 0.6 dB and an associated gain of 14 dB at 4 GHz. The maximum drain to source voltage is 5.0 V and the maximum drain current is 10 mA typical and 30 mA maximum.

Figure 4 shows the schematic for the basic TOM. Note the presence of Rdb and CBS from the drain to the source. Figure 5 shows the LIBRA Series IV schematic for the TOM. Note that while there is no external Rdb and CBS in the schematic, the model variables RDB and CBS are present in the listing of variables in Figure 5. This shows

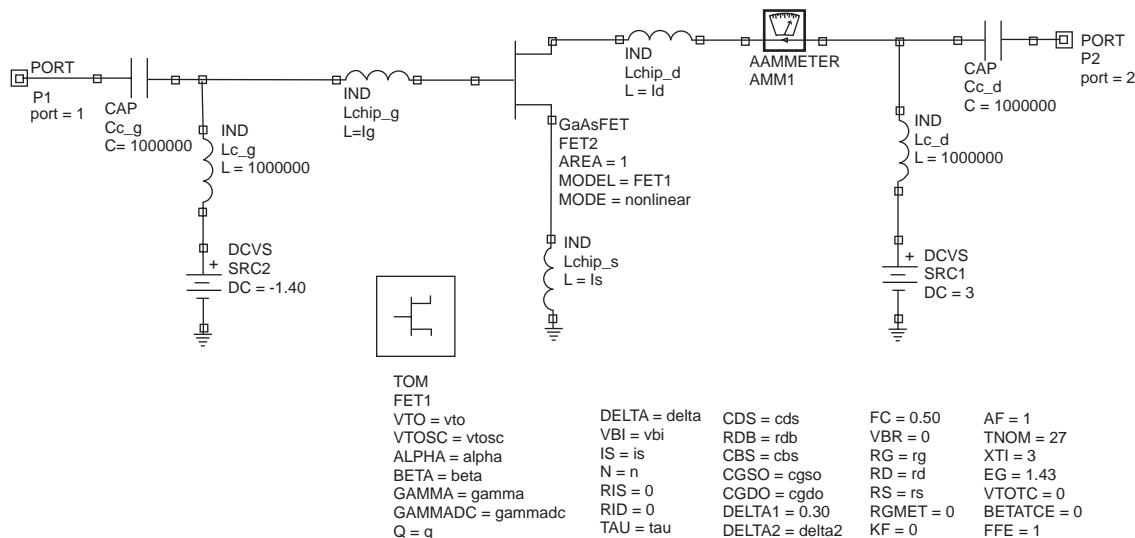


Figure 5. Libra Series IV Schematic with Internal RC Network.

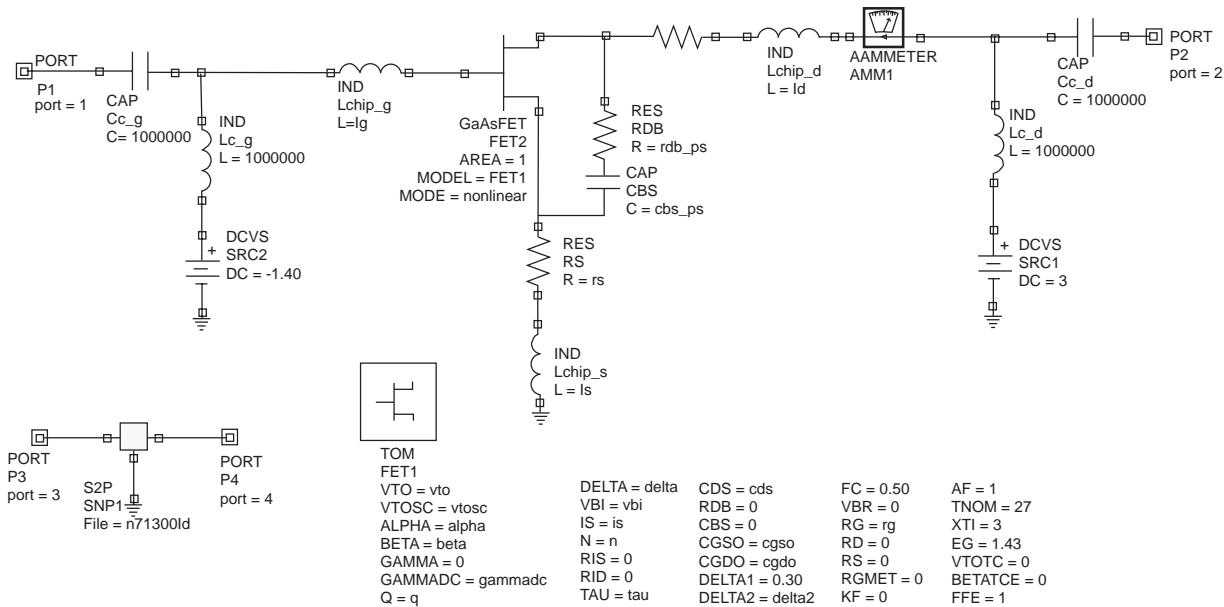


Figure 6. Libra Series IV Schematic with External Network.

conclusively that the output conductance is programmed into Libra's TOM.

If using a simulator that doesn't have the compensation programmed into the model, add RDB and CBS as external circuit components, as shown in Figure 6. Figure 6 uses the Libra simulator, therefore, RDB, CBS, RD and RS are set to 0 in the programmed list of model variables because these parameters are added externally as components.

Comparison Of Internal Compensation To External Compensation

Figures 7 through 10 show a comparison of implementing the high frequency output conductance control externally. In the following figures, \square is the CEL measured data, \circ is the results using the schematic with the internal compensation (Figure 5) and Δ is the results using the schematic with external compensation (Figure 6).

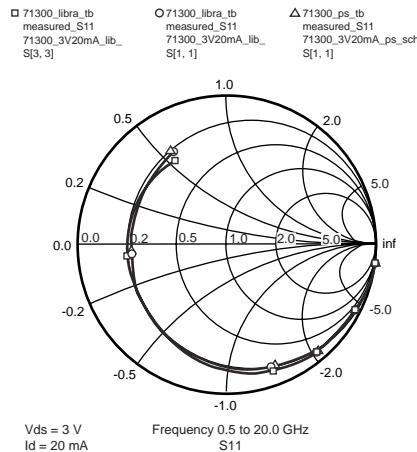


Figure 7. S11 Compensation Comparison.

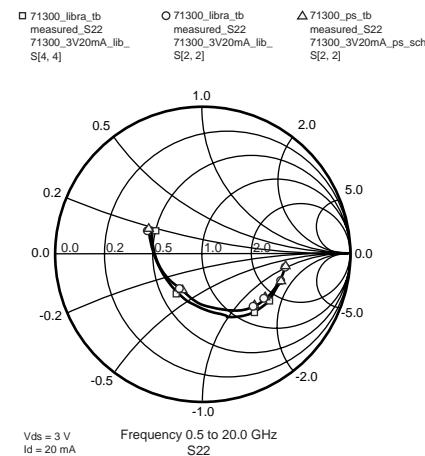


Figure 8. S22 Compensation Comparison.

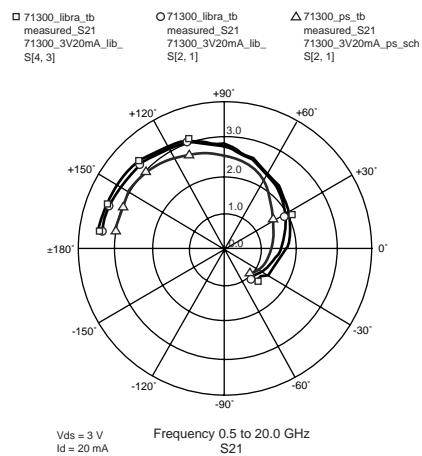


Figure 9. S21 Compensation Comparison.

LIBRA PARAMETERS	DEFINITION	PSpice PARAMETER[6]
BETA	transconductance parameter or coefficient	BETA
VTO	threshold voltage (called the pinch-off voltage in PSpice)	VTO
ALPHA	current saturation parameter (called the saturation voltage parameter in PSpice)	ALPHA
LAMBDA	output conductance parameter (called channel-length modulation in PSpice)	LAMBDA
THETA	parameter which controls Ids-Vgs characteristic transition from quadratic to linear behavior (called the doping tail extending parameter in PSpice)	B
TAU	transit time under gate (called conduction current delay time in PSpice)	TAU
VBR	gate-drain junction reverse bias breakdown voltage	not implemented
IS	gate junction reverse saturation current (called the gate p-n saturation current in PSpice)	IS
N	gate junction reverse saturation current (called the p-n emission coefficient in PSpice)	N
VBI	built-in gate potential (called the gate p-n potential in PSpice)	VBI
FC	coefficient for forward bias depletion capacitance	FC
RC	used with CRF to model frequency dependent output conductance	not implemented
CRF	used with RC to model frequency dependent output conductance	not implemented
RD	drain ohmic resistance	RD
RG	gate ohmic resistance	RG
RS	source ohmic resistance	RS
RIN	channel resistance	not implemented
CGSO	zero bias gate-source junction capacitance	CGS
CGDO	zero bias gate-drain junction capacitance	CGD
DELTA1	capacitance saturation transition voltage parameter	not implemented
DELTA2	capacitance threshold transition voltage parameter	VDELTA
CDS	drain-source capacitance	CDS
CGS	gate-source capacitance	not implemented
CGD	gate-drain capacitance	not implemented
KF	flicker noise coefficient	KF
AF	flicker noise exponent	AF
XTI	temperature exponent for saturation current	XTI
EG	energy gap or band gap voltage	EG
VTOTC	VTO temperature coefficient	VTOTC
BETATCE	BETA exponential temperature coefficient	BETATCE
FFE	flicker noise frequency exponent	not implemented
not implemented	gate p-n grading coefficient	M
not implemented	capacitance limiting voltage	VMAX

Table 1: Statz Model Parameters.

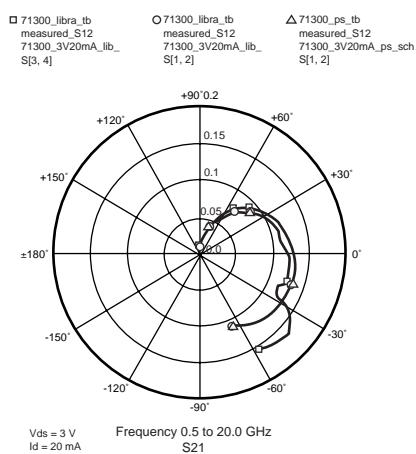


Figure 10. S12 Compensation Comparison.

It can be seen by examining Figure 9 that the gain resulting from the model in Figure 6 is lower than the measured gain and the modeled gain from the schematic in Figure 5. This is due partly to the fact that some simulators do not

implement the AC gamma parameter (GAMMAAC). In addition, when GAMMAAC is set to its default of zero, the value for Rdb (called rdb_ps in Figure 6) must also be adjusted to match S22. In the above example, rdb = 2000 ohms and rrdb_ps = 300 ohms. Table 1 and Table 2 compare the parameters as implemented in HP-EEsof Series IV Libra simulator[5] and MicroSim PSpice[6] for the Statz model (Table 1) and for TOM (Table 2). Figures 7, 8 and 10 indicate that, properly implemented, the external compensation network provides almost identical results for S11, S22 and S12.

CONCLUSIONS

1. The Curtice model is useful when extracting a model at a single bias point.
2. The Statz model is more accurate when the Ids for a device behaves quadratically (square-law approximation) for small values of (V_{gs} - VTO) and linearly for large values of (V_{gs} - VTO).
3. TOM is more accurate when the square-law approximation does not predict device performance well and when the device drain conductance varies with gate-source bias.

LIBRA PARAMETERS	DEFINITION	PSpice Parameter[6]
VTO	threshold voltage (called the pinch-off voltage in PSpice)	VTO
VTOSC	scaleable portion of the threshold voltage	not implemented
ALPHA	current saturation parameter (called the saturation voltage parameter in PSpice)	ALPHA
BETA	transconductance parameter or coefficient	BETA
GAMMA	AC drain pull coefficient	not implemented
GAMMADC	DC drain pull coefficient (called the static feedback parameter in PSpice)	GAMMA
Q	power law exponent	Q
DELTA	output feedback coefficient	DELTA
VBI	built-in gate potential (called the gate p-n potential in PSpice)	VBI
IS	gate junction reverse saturation current (called the gate p-n saturation current in PSpice)	IS
N	gate junction ideality factor (called the gate p-n emission coefficient in PSpice)	N
RIS	source end channel resistance	not implemented
RID	drain end channel resistance	not implemented
TAU	transit time under gate (called conduction current delay time in PSpice)	TAU
CDS	drain-source capacitance	CDS
RDB	dispersion source output impedance	not implemented
CBS	drain-source capacitance	not implemented
CGSO	zero bias gate-source junction capacitance	CGS
CGDO	zero bias gate-drain junction capacitance	CGD
DELTA1	capacitance saturation transition voltage parameter	not implemented
DELTA2	capacitance threshold transition voltage parameter	VDELTA
FC	coefficient for forward bias depletion capacitance	FC
VBR	gate-drain junction reverse bias breakdown voltage	not implemented
RD	drain ohmic resistance	RD
RG	gate ohmic resistance	RG
RS	source ohmic resistance	RS
RGMET	gate metal resistance	not implemented
KF	flicker noise coefficient	KF
AF	flicker noise exponent	AF
XTI	temperature exponent for saturation current	XTI
EG	energy gap or band gap voltage	EG
VTOTC	VTO temperature coefficient	VTOTC
BETATCE	BETA exponential temperature coefficient	BETATCE
FFE	flicker noise frequency exponent	not implemented
not implemented	gate p-n grading coefficient	M
not implemented	capacitance limiting voltage	VMAX

Table 2. TOM Parameters.**REFERENCES**

- [1] J. Michael Golio, Editor, "Microwave MESFETs and HEMTs", Artech House, 1991.
- [2] W.R. Curtice, "A MESFET model for Use in the Design of GaAs Integrated Circuits," IEEE Trans. Microwave Theory Tech., Vol. MTT-28, 1980, pp. 448-456.
- [3] H. Statz, P. Newman, I. Smith, R. Pucel, and H. Haus, "GaAs FET Device and Circuit Simulation in SPICE," IEEE Trans. Electron Devices, Vol. ED-34, 1987, pp. 160-169.
- [4] A. McCamant, G. McCormack, and D. Smith, "An Improved GaAs MESFET Model for Spice," IEEE Microwave Theory Tech., Vol. MTT-38, June 1990, pp. 822-824.
- [5] HP-EESof Microwave & RF Circuit Design Circuit Element Catalog, Vol. 2, February 1994, pp. 13-79 - 13-106.
- [6] Microsim PSpice A/D Circuit Analysis Software Reference Manual, Version 6.3, April 1996, pp. 2-6 - 2-21.

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Modeling GaN: Powerful but Challenging

GaN

Gallium nitride transistor-based power amplifiers (PAs) are currently among the most important technologies impacting high-power transmitter design at microwave frequencies. The high breakdown voltage capability (over 100 V), combined with simultaneous high-current capability (tens of amps) and favorable thermal conductivity of modern aluminum gallium nitride/gallium nitride high-electron mobility transistors (AlGaN/GaN HEMTs) (often more simply referred to as GaN HEMTs) on silicon carbide (SiC) and silicon substrates, has enabled an order-of-magnitude improvement in power density over gallium arsenide (GaAs)-based devices. GaN HEMTs also allow high-power operation at much higher frequencies than silicon laterally diffused metal-oxide-semiconductor field-effect transistors (LDMOS FETs), currently a staple for the cellular base station industry. As GaN technology has developed, first in research laboratories and more recently in multiple commercial device manufacturers, the demand for improved nonlinear models has grown alongside the device process improvements. The need for improved models for GaN is twofold: first, GaN devices have unique nuances in behavior to be addressed; second, there is a desire for improved accuracy to take full advantage of the performance wins to be gained by GaN HEMT performance in the areas of high efficiency and high-power operation.

Such behavioral nuances include trapping effects and associated current-knee collapse (which results in an increase in the knee voltage at which electron velocity saturation occurs) that tends to be more significant for GaN than for GaAs-based HEMTs, as illustrated by Trassaert et al. [1] and Charbonnud et al. [2]. Additional bias dependences have been observed, for example, in the source resistance, as pointed out by Trew et al. [3], and the drain-to-source capacitance, as indicated by Tajima [4]. Subthreshold-valid modeling may be important for designers who wish to operate in Class B, C, D, and E high-efficiency operating modes, for example, and not all models can fit behavior in this region. Specific attention was paid to ensure the Curtice FET (CFET) model [5] is well behaved in this region. Candidate models should be checked for fidelity with respect to measured data for

gate voltages at or below threshold if this operating region will be important for the application. Finally, due in part to the capability of GaN HEMTs to work at higher voltage-current products, there is an increased need for accurate electrothermal modeling. Illustrative work in this area can be found in the works of Camarchia et al. [6] and Casto [7], among many others [2], [7]–[9].

The significant attention placed on nonlinear models is in step with the growing community of designers who are using nonlinear circuit simulators with good success to design and optimize high-power amplifiers. For this simulation-based design community, the success of their PAs, whether for wireless communications or military applications, depends on the accuracy and scalability—with bias, temperature, and geometry—of available nonlinear models for power transistors.

At a top level, one might ask questions like “Nonlinear FET models for PA design have been available for some time now, so why are we still talking about them?” and “Isn’t this a solved problem?” The reality is that the demand and requirements for more accurate nonlinear models in new and existing devices

continues to increase. In fact, it is common knowledge in the industry that the lack of a good nonlinear model can be a significant impediment to having a commercial GaN device considered for new designs.

With this demand has come an accompanying need for advanced model testing. For example, as operating power increases,

thermal issues play a larger role and pulsed measurements are required to either avoid variable self-heating during testing or to help keep the device at a safe temperature during the intended operation. Load-pull measurements are certainly in the category of advanced model testing. These measurements include straightforward single-tone power compression and efficiency optimization, to two-tone and multi-tone distortion testing, amplitude modulation/phase modulation (AM/PM) load-pull and pulsed radio frequency (RF)/pulsed bias load-pull testing. Also, time domain waveform measurements and nonlinear network analyzer measurements are being increasingly applied to the problem of nonlinear power transistor model validation.

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The demand for improved nonlinear models has grown alongside the device process improvements.

Among the considerations for good power transistor models are the overall measurement accuracy, the suitability of the model, and the types of validations executed to test and refine the model. Fixturing and calibration methods/standards play a very important role in achieving an accurate data set to use for models; after all, compact model accuracy starts (and can stop) with data accuracy. In this article, we discuss modeling considerations for GaN HEMT devices and nonlinear modeling techniques that can predict the particular behaviors of GaN devices. We will review several popular compact FET models including commercially available models as well as the in-house models discussed in the next section. This treatment expands the presentation of GaN modeling considerations given at a recent conference [10].

A Tour of GaN HEMT Modeling Work

A review of the microwave device modeling literature reveals that much work has been done in the area of nonlinear modeling in the context of GaN HEMT treatment. Most of this work is targeting accurate measurement-based compact models that can be used for design work. Such models are implemented in simulators variously as C-code, Verilog-A code, and as symbolically defined devices (SDDs) among other coding approaches. Figure 1 shows a nonlinear equivalent circuit topology used in the most recent model by Angelov et al. [11]. As will be explained in the next section, element values and equation fitting

coefficients are extracted or optimized to provide a best fit to various measured data.

Various available GaN HEMT compact models differ somewhat in topological details, but, more significantly, they are distinguished by the equations used to fit the voltage-dependent I_{DS} and the functions used to represent the voltage dependent capacitance or charge representations of C_{gs} , C_{gd} , and C_{ds} . Most popular models have electrothermal models that consist of an equivalent electrical analog thermal resistance R_{therm} and capacitance C_{therm} as depicted in Figure 1. These electrothermal models provide a means to estimate the channel temperature rise due to dc power dissipation. The one shown is a simple single pole model, which can be expanded to address multiple thermal time constants if needed to represent more complex behavior.

To better understand the foundation for GaN HEMT compact models, most of the reported work represents either a straightforward application of compact models originally developed for GaAs metal-semiconductor field-effect transistor (MESFETs) and HEMTs or extensions to and customizations of such models. These well-established models include the original Curtice model [12], the Eesof GaAs HEMT (EEHEMT) model [13], and the original Angelov-Chalmers model [14], which is also referred to as the *Angelov* model or the *Chalmers* model.

The EEHEMT model is itself an extension of the Curtice model. The EEHEMT model separates the dc and ac behavior for a simpler model extraction. However, this makes complex time-dependent thermal effects in the in-between or low-frequency region (where temperature can vary with the ac signal fluctuations) more difficult to characterize. The model reported by Camarchia et al. [6] uses the original Curtice model as the basis for a

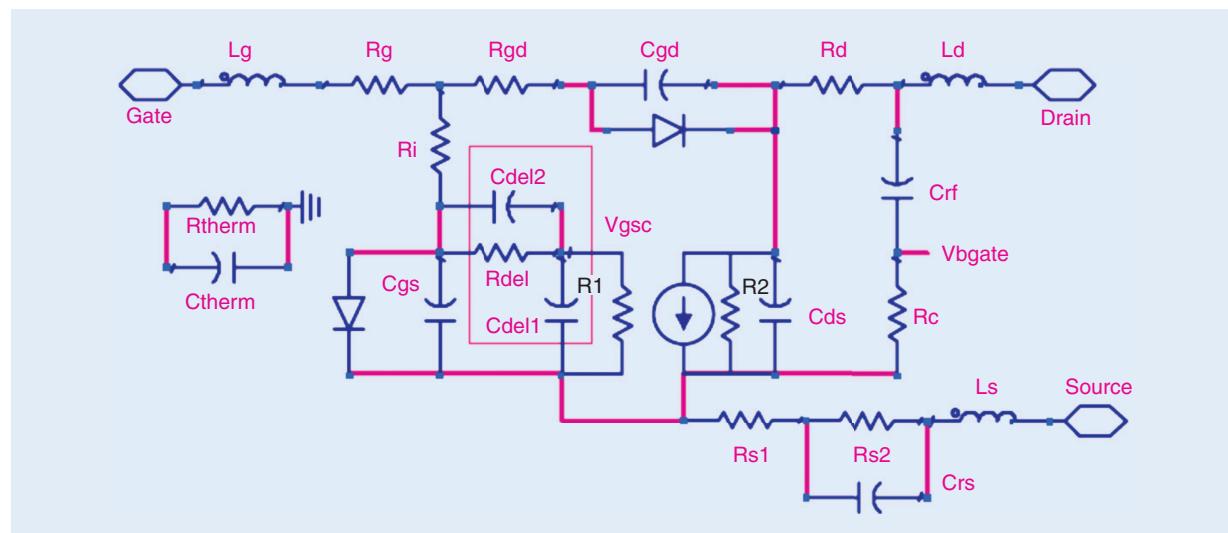


Figure 1. Topology for the Angelov GaN HEMT model [11]. The electrothermal model elements R_{therm} and C_{therm} enable estimation of channel temperature rise due to power dissipation.

comprehensive so-called self-consistent electrothermal model. This model is developed by fitting a behavioral thermal equivalent circuit model to this analysis. Results are shown for a GaN HEMT device, illustrating the impact of improved electrothermal modeling on memory effects such as variations in third-order intermodulation power (IM3) with tone spacing. Kharabi et al. report good success with the EEHEMT model for modeling the RF Micro Devices, Inc. (RFMD) GaN devices [15]. Curtice has expanded considerably on the original model of [12] with present model variations called CFET and C_HEMT (with the most recent versions of these labeled CFET9 and C_HEMT3, as of this writing). These models have specific enhancements that aid with GaN modeling [5]. The separate works of Casto and Dooley [7] and Lee and Webb [8], [9] both report good results using the CFET model for GaN modeling.

Updates have also been made to the original Angelov model and there is now a GaN-specific version (termed *Angelov_GaN*) available in Verilog-A code. This updated model has the topology of Figure 1 and is the basis for the work reported in Angelov, et al. [16] and Angelov, et al. [11]. The *Angelov_GaN* model includes modifications to the I_{ds} model to address improved prediction of harmonics as well as g_m and g_{ds} dispersion. Modifications are also made to better assure charge conservation of capacitance functions. Another model that has been demonstrated to be effective for GaN HEMT modeling is the Auriga model discussed by Tajima [4], which is reported to be a significant expansion to the Angelov model. The original Angelov model has also been used by the authors of this article with good success, and it has also been modified to add bias and geometry scalability. Results from this model will be discussed later.

Among the considerations for good power transistor models are the overall measurement accuracy, the suitability of the model, and the types of validations executed to test and refine the model.

Two models that have used a common but different starting point for their current formulation are that of the in-house model presented by Cabral et al. [17] and the proprietary Cree model, as described by Pengelly et al. [18]. Both of these groups start with the current formulation of Fager et al. [19]. This formulation was originally developed for silicon LDMOS transistors. Cabral et al. provide a compelling example of how Fager's four-region current formulation leads to improved comparison to measured data in terms of the derivatives of the current functions (for example, g_m , g_{m2} , and g_{m3}), when compared to the original Angelov model [14]. Both Pedro et al. and Pengelly et al. report improved third-order intermodulation distortion and spectral spreading prediction with their models compared to the more established MESFET/HEMT formulations.

Nonetheless, the example of Figure 2, which was provided by coauthor Walter Curtice, suggests good results can be achieved for third-order effects, such as IM3 and third harmonic power with the Angelov model. Shown is a comparison to an EEHEMT model for the same device, which, in this particular case, shows improved third harmonic prediction for the Angelov model. However, we will later show a different GaN HEMT example where third-order IM3 was predicted quite acceptably with an EEHEMT model.

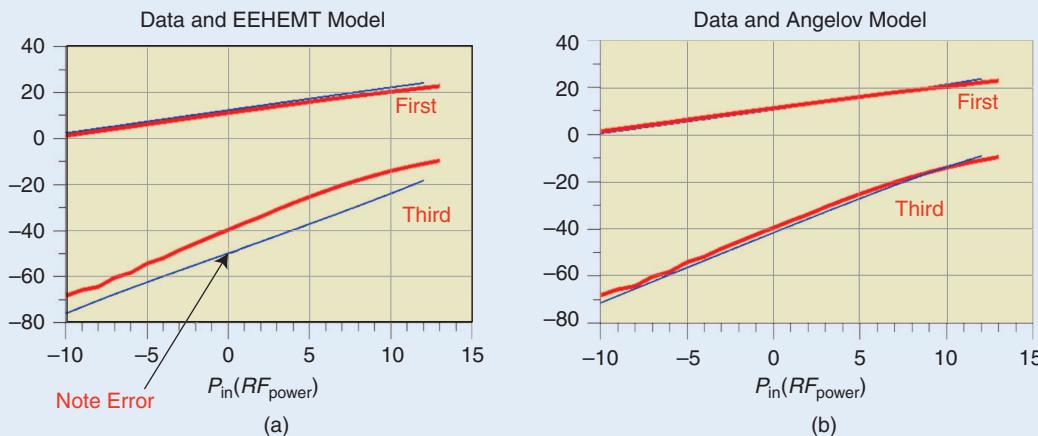


Figure 2. Comparison of fundamental and third harmonic output power for a 1.75-mm GaN HEMT device. (a) EEHEMT model fit. (b) Angelov model fit. Measured data are red and modeled results are blue.

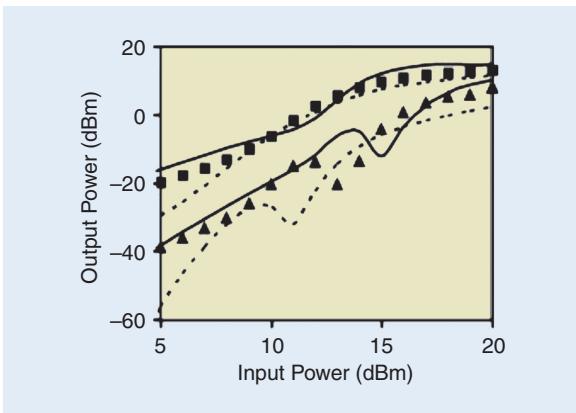


Figure 3. Measured (symbols) third-order (top curve) and fifth-order (bottom curve) intermodulation distortion of a Class-A amplifier under optimum source and load matches at 1.9 GHz versus that simulated with Angelov (—) and EEHEMT (---) models for a GaN MOSHFET device [20].

Another example of an Angelov-based model providing good intermodulation distortion prediction for GaN devices is shown in the work of Deng et al. [20], wherein modifications were made to the Verilog-A code version of the Angelov model to tailor its applicability to metal–oxide–semiconductor heterostructure field-effect transistor (MOSHFET) devices, which are similar to GaN HEMTs with the exception of a thin oxide layer that is introduced as a gate insulator having the positive effect of reducing gate current. Figure 3 shows measured and simulated IM3 and IM5 for a Class AB amplifier based on a modeled GaN MOSHFET device. Simulated results are shown for both the modified Angelov model and an EEHEMT model for the GaN device.

To put the examples of Figures 2 and 3 in some perspective, the work of Pedro et al. [17] specifically

focused on making sure third-order effects were properly modeled. Other models, with appropriate attention, may or may not give acceptable results for third-order distortion and harmonic results. It is misguided to assume that they will without adequate advanced model testing and careful validation at or near the operating region of interest.

Recent publications also include those specifically addressing the often significant trapping effects in GaN HEMTs as well as numerical approaches. Examples of this work include the drain-lag model described by Jardel et al. [21], along with the treatment of Baylis that modified the Angelov current formulation to address quiescent-bias dependent trapping effects [22]. Physics-based numerical modeling approaches [3], [23] have revealed much new understanding of effects that need closer attention, such as breakdown behavior and the aforementioned nonlinearity of the GaN HEMT source resistance.

Table 1 is a summary of various FET models, which includes models that are being used for GaN HEMT transistors. Also included for comparison purposes are selected models used for GaAs MESFET, silicon MOSFET, and LDMOS devices. Models with a larger number of parameters are not necessarily better for a given task, but, generally speaking, are set up with additional parameters to either tie the model more closely to physical process effects, as in the case of the Berkeley Short-Channel IGFET Model (BSIM) type of models [24], or to have increased flexibility in modeling specific ac and dc aspects of the device behavior, as is the case with the EEHEMT model. The following are a few reasons why a lower number of parameters are desirable:

- Model parameter extraction time increases with the number of parameters. A 100-parameter model takes considerably longer to extract than a 50-parameter model.

TABLE 1. Comparison of example FET models used for GaAs, silicon, and GaN FET/HEMT devices.

FET Models	Approx. Number of Parameters	Electrothermal (Rth-Cth) Model	Geometry Scalability Built-In	Original Device Context
Curtice3 [12]	59	No	No	GaAs MESFET
Motorola Electrothermal (MET) [25]	62	Yes	Yes	LD MOSFET
CMC (Curtice/Modelithics/Cree) [26]	55	Yes	Yes	LD MOSFET
BSIMSOI3 [24]	191	Yes	Yes	SOI MOSFET
CFET [5]	48	Yes	Yes	HEMT
EEHEMT [13]	71	No	Yes	HEMT
Angelov [14]	80	Yes	No	HEMT/MESFET
Angelov GaN [11]	90	Yes	No	HEMT
Auriga [4]	100	Yes	Yes	HEMT

- The parameters of a large parameter set model tend to be less physical and more empirical.
- Uncertainty in parameters increases greatly as the number of parameters increases. This can cause poor convergence in optimization routines.

It should also be noted that even though all models shown have temperature dependences built in to the equations, not all have full electrothermal models that address self-heating. Self-heating is caused by average power dissipation in the device. The self-heating varies with dc bias and, at high power, with RF signal levels. Most of the models listed are commercially available as built-in models in microwave circuit simulator, such as Agilent Advanced Design System (ADS) and Applied Wave Research (AWR) Microwave Office. The Angelov model is also available in Verilog-A format in both the original [14] and Angelov_GaN [11] versions. The CFET model can be purchased from W.R. Curtice Consulting as add-on software. The Auriga model may be accessed through commercial model extraction services offered by Auriga Microwave. With the exception of this model, Modelithics offers extraction services for the other models listed. Relatively speaking, the Angelov model parameter extractions tend to be more time-consuming in comparison to EEHEMT and CFET, for which IC-CAP routines are readily available to assist with the extraction process.

Basic Modeling Strategy, Considerations and Issues

The following discussion presents a nonlinear characterization and modeling strategy in the context of addressing some of the specific issues relevant to GaN modeling. A typical test station used to acquire data for model coefficient extraction con-

It should also be noted that even though all models shown have temperature dependences built in to the equations, not all have full electrothermal models that address self-heating.

sists of a wafer probe station, broadband vector network analyzer (VNA), dc and pulsed current voltage ($I-V$) analyzers, and a computer-running software that facilitates at least instrument control and data acquisition if not also model extraction [13]. A typical nonlinear transistor modeling process is outlined in Figure 4. The reader is referred to one of the texts available for more detailed transistor modeling information [27]–[29].

As a first step, $I-V$ and multibias S-parameter measurements (often pulsed) are performed. Understanding trapping effects and their bias dependence is important for successful GaN HEMT modeling. Here judicious application of pulsed $I-V$ techniques is recommended. Pulsed $I-V$ techniques began in the FET modeling context with the groundbreaking work of Platzker et al. [30]. The introduction of commercially available systems greatly facilitated such applications, and pulsed $I-V$ measurements are now used for routine model extractions as well as research. Commercial pulsed $I-V$ measurement systems have been developed by the manufacturers such as

- Agilent Technologies
- Accent Optoelectronics
- Auriga Measurement Systems
- Keithley Instruments
- Focus Microwaves
- AMCAD.

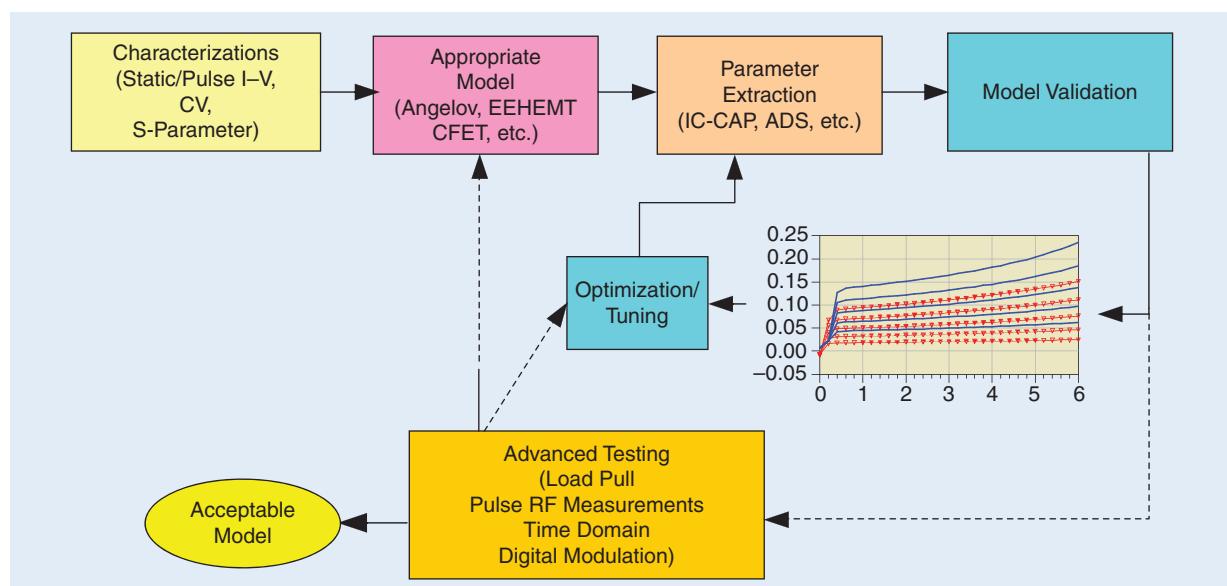


Figure 4. Nonlinear transistor modeling process.

GaN HEMTs often show a significant quiescent-bias dependence in their operating characteristics.

Some of the original systems have been made obsolete by their manufacturer but their systems are still in active use in modeling laboratories. The Auriga AU4750 illustrated on the left side of Figure 5 is an example of a commercially available pulsed I-V test system.

Pulsed I-V analysis has been applied by many to understand trapping effects in III-V devices, including

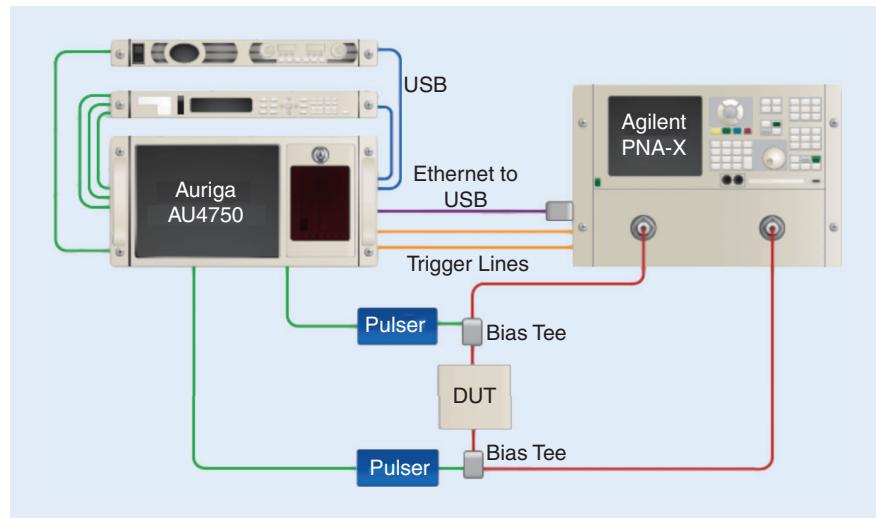


Figure 5. Commercially available setup for pulsed I-V and pulsed S-parameters. (Courtesy Auriga Microwave, used with permission.)

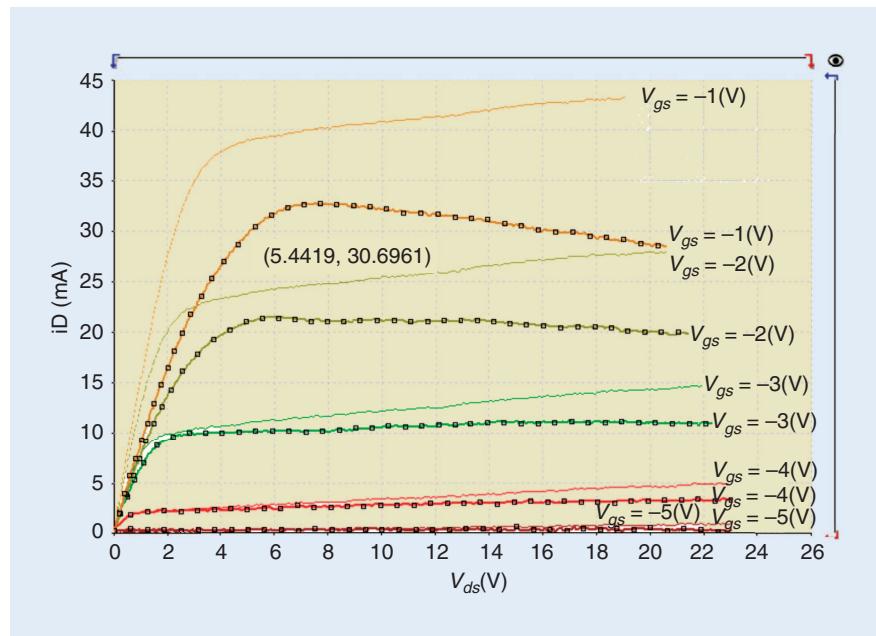


Figure 6. Comparison of pulsed I-V (solid lines without symbols) and static I-V for a GaN HEMT. Pulse conditions were 0.2 μ s pulse width and 1-ms separation with quiescent bias set at $V_{dsq} = 0$, $V_{gsq} = 0$. V_{gs} is varied from -5 to -1 V in 1 V steps.

the original GaN trapping origins and its characterization [1], [31], [32]. For the case of GaN HEMT modeling, pulsed I-V measurements are effective for extracting an isodynamic equation for I_{DS} . The term *isodynamic* is used when thermal and trap conditions are held at values corresponding to the specified quiescent bias condition. This is in comparison to a static I-V measurement, representative of a traditional curve tracer or dc parameter analyzer, where acquisition of each data point is slow enough that traps, if present, and thermal conditions can be different at each of the acquired data points. Figure 6 shows a comparison of pulsed and static I-V measurements for a GaN transistor [22], where the thermal heating effects in the high V_{ds}

* I_{ds} power dissipation region are quite clear in contrast to the isodynamic pulsed I-V data. Typical pulsed I-V conditions might consist of 0.1 to 0.5 μ s pulse widths, separated by time intervals on the order of 1 ms. These data were acquired using an Accent Optoelectronics DiVA instrument.

GaN HEMTs often show a significant quiescent-bias dependence in their operating characteristics. As an illustrative example, pulsed I-V measurements made by Baylis [22] are shown in Figure 7. In this figure, I-V curves from several different values of zero power dissipation quiescent bias conditions are shown. In Figure 7(a), the quiescent drain-to-source voltage V_{dsQ} is held at 0 V while the quiescent gate-to-source voltage V_{gsQ} is varied from -5 V to 0 V. In Figure 7(b), the gate voltage is held at threshold, such that the drain current is zero and the drain voltage (V_{dsQ}) is varied between 0 and 4.5 V. Because the power dissipation (based on the quiescent bias) is zero for all of the measurements, the variations observed in both plots are due only to trapping effects and not thermal effects. Baylis introduced modifications of the original Angelov current equations that allow for such quiescent

bias-dependent trapping effects in I - V curves to be captured in a nonlinear model. It should be mentioned the device represented in Figure 7 is a noncommercial device with significant gate- and drain-dependent trapping. Commercial devices with quality surface passivation will show much less gate-dependent trapping and may show a less pronounced current collapse than illustrated here. Nevertheless, for GaN modeling it is important to make sure that pulsed I - V measurements are used for model fitting with the quiescent bias point to be at or near the desired operating bias point(s).

Zero V_{ds} -biased cold-FET S-parameter measurements are generally performed to assist with nonbias-dependent extrinsic parasitic element determination. Referring to Figure 1, L_d , L_g , and L_s , along with extrinsic resistances and pad capacitances (if present and significant), for example, would all be determined in this way. If the device is packaged, package parasitics will also need to be modeled and de-embedded from the measurements. The same strategy used for LDMOS packaged device modeling [28] can be applied to separate package parasitic and intrinsic device model aspects for GaN HEMTs. Preferably, both chip and packaged versions of the device are available, as it is better to model the intrinsic device using chip-level data.

Capacitance-voltage (CV) behavior is most often derived from multibias, hot-bias S-parameters after extrinsic element effects have been de-embedded from the measured data. The selection of the model will be driven by a number of considerations, including availability of the model and extraction tools in the chosen circuit simulator. For maximum flexibility, one advantage of having a model available as either a symbolically defined device

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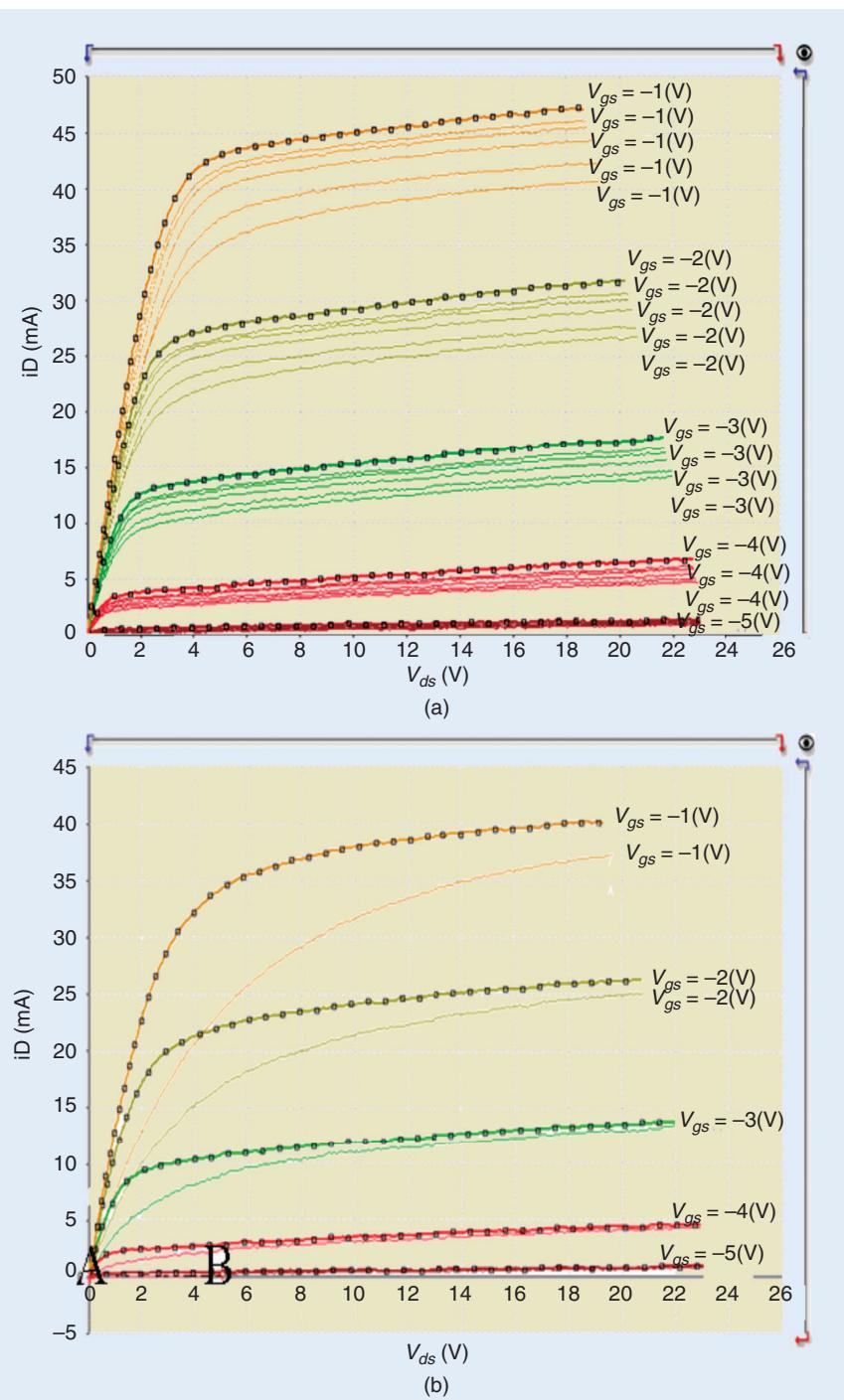


Figure 7. Bias dependent trapping effects for a GaN HEMT. In all cases, the dc power dissipation is zero as pulsing is either from (a) $V_{ds} = 0$ and various V_{gs} values and (b) $V_{gs} <$ pinchoff and varied V_{ds} . Pulse conditions were 0.2- μ s pulse width and 1-ms separation. V_{gs} is varied from -5 to -1 V in 1 V steps.

Pulsed S-parameter measurements additionally can be used to ensure that the correct thermal dependences of the model's capacitance equations are extracted.

or Verilog-A code is that modifications to the model can be made if necessary to better track observed voltage dependences. As powerful as the models described in the prior section can be, compact models are still empirical approximations that cannot fully capture all the effects of a real physical device for all operating regions and conditions [33].

Once the appropriate model is selected, model parameters are extracted using software such as Agilent IC-CAP and/or utilizing a circuit simulator like ADS or AWR Microwave Office. The model is then validated, often with emphasis on the important regions for the targeted application. That is to say, as a general rule, nonlinear models do not necessarily work well globally at all possible quiescent bias conditions. Rather, it is common to focus on a particular operating region when fitting model parameters. For example, for Class E applications, special attention is given to fitting I - V and S-parameters in the threshold and knee regions. As pointed out by Negra et al. [34], a model developed for Class AB may not be effective for Class E/D switched-mode applications. However, the particular model reported by Negra et al. appears to be limited in application to subgigahertz applications. In contrast, we have found that good results can be achieved for modeling Class E type devices by

focusing attention on making sure the model fits well in the threshold (zero current) off and knee on regions with models such as the EEHEMT and the CFET.

Turning attention to the electrothermal circuit of Figure 1, a number of useful measurement techniques to extract thermal resistance and time constants, or thermal capacitance, have been demonstrated for silicon devices that possess minimal trapping effects [35]–[38]. Casto and Dooley [7] applied similar methods to extract an electrothermal model for GaN HEMTs by performing pulsed I - V and S-parameter testing at multiple temperatures and biases and validating results against infrared measurement results. As mentioned earlier, another group has demonstrated the usefulness of numerically based thermal analysis as part of their electrothermal modeling strategy [6].

Pulsed S-parameter measurements additionally can be used to ensure that the correct thermal dependences of the model's capacitance equations are extracted. These differences are caused by self-heating effects as well as electron emission and capture by trap states on the surface and in the substrate of the device. More effort and model complexity is required if the goal is to have a model that can scale accurately with geometry and/or with quiescent bias conditions. As with pulsed I - V measurements, pulsed bias S-parameters are pulsed from one specific quiescent bias point at a time.

When performing pulsed bias/pulsed S-parameters, careful attention needs to be paid to the bias tees used, as the frequency and time-domain step response of the dc bias path can severely limit the pulsed conditions that can be used [39]. Figure 8 shows examples of a pulse response of the dc to RF + dc port of both an example commercial bias

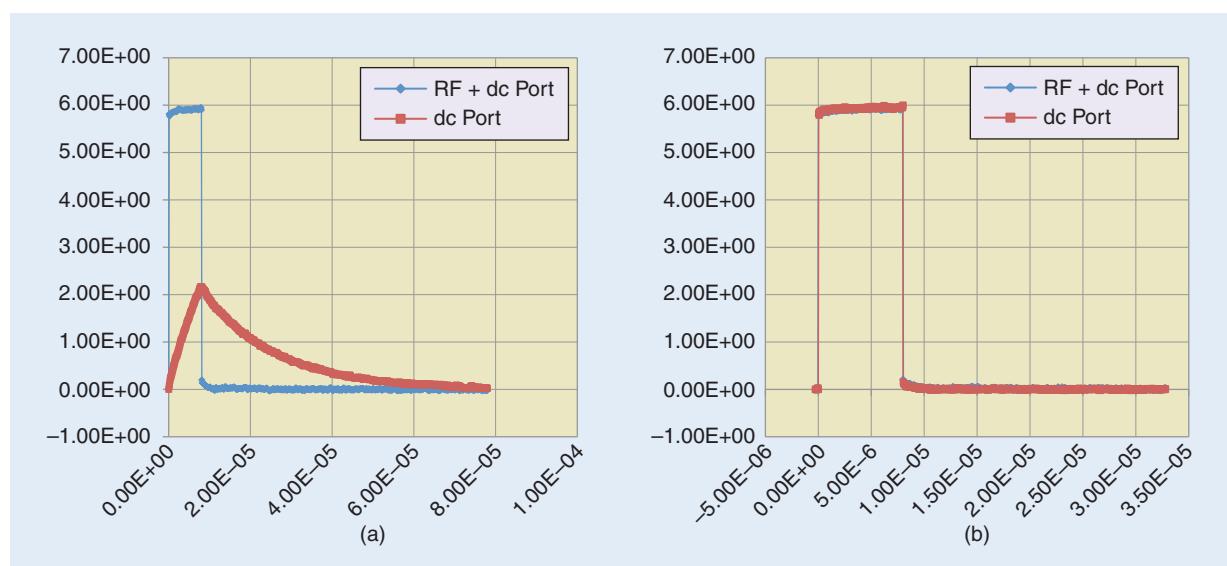


Figure 8. Pulse width 8 μ s and period 80 μ s (10% duty cycle) for (a) a commercial bias tee and (b) a custom in-house bias tee. Note: The y-axis is voltage and x-axis is time in seconds for both plots.

tee [Figure 8(a)] and a custom in-house bias tee [Figure 8(b)]. For pulsed S-parameters, the VNA measurement approach can also limit the measurement dynamic range depending on the pulse width and/or duty cycle [40]–[42].

The commercially available system shown in Figure 5 enables both pulsed I - V and pulsed S-parameter measurements by combining the Auriga AU4750 pulsed I - V system with an Agilent PNA-X network analyzer. An example of a comparison of pulsed and static bias S-parameters for a GaN HEMT made with this system is shown in Figure 9, where the effects of self-heating for the static-bias case are exhibited as a gain drop of about 1–1.5 dB. In addition to addressing self-heating and trapping issues, pulsed S-parameters allow data to be taken in regions where the device may fail due to overheating. While pulsed S-parameters are clearly useful for many large-signal device modeling applications, it should also be noted that the authors have developed nonlinear models over the past several years for a multitude of power devices without the use of pulsed S-parameters. Positive feedback from designers using these models as well as load-pull validations has confirmed the accuracy of the models so derived.

In referring to Figure 4, much of the model parameter extraction and fitting for GaN HEMTs is performed using I - V and S-parameter data and it is the advanced testing area “where the rubber meets the road,” so to speak, for a given application. Application-specific testing that is tailored to the given appli-

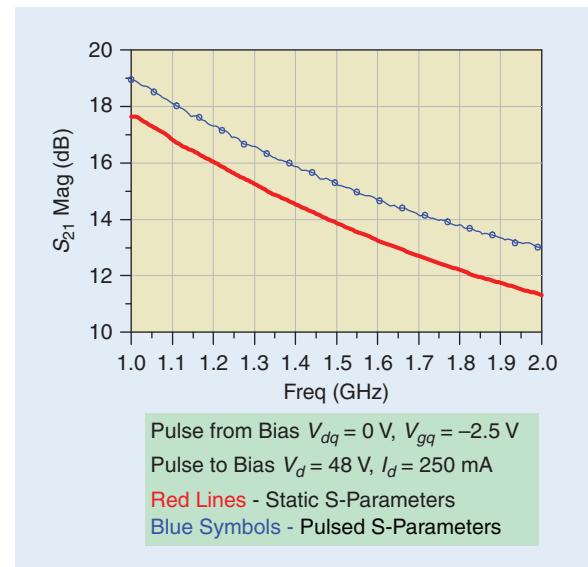


Figure 9. Pulsed S-parameter and static S-parameter comparison for a 10 W GaN HEMT. Pulse conditions: 5 μ s pulse width, 0.1% duty cycle (IF BW = 1/pulse width = ~200 kHz).

cation can help reveal whether the model can meet the demands of the target design type, or help to identify how to further refine the parameter set to make sure the model can be useful for the type of PA design for which it is intended. Single-tone scalar load- and source-pull testing is done at a minimum. Depending on the final circuit application for which the model is intended, load-pull validation requirements may, in

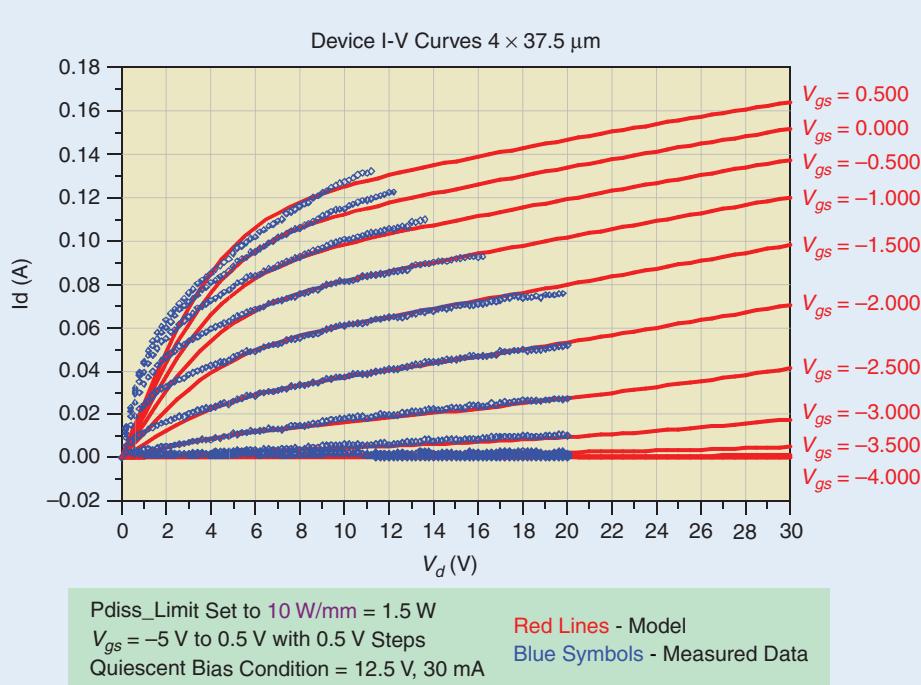


Figure 10. The 25 °C pulsed I - V curves for a 4 × 37.5 μ m GaN HEMT device compared to an extracted EEHEMT model.

many cases, expand to include two-tone linearity testing, harmonic impedance, AM/PM, adjacent channel power ratio, and error vector magnitude as well as time-domain waveform testing. Advanced testing validations of GaN device models these days increasingly are including tests like large-signal network analyzer or nonlinear VNA-measured waveforms tested under varied fundamental and harmonic load-pull conditions.

In summary, a large amount of work has been applied by several groups to develop and test the capabilities of various model topologies and equation sets for use in GaN HEMT modeling. Other areas needing careful attention in extracting trustworthy models for GaN HEMTs include obtaining appropriate and accurate sets of characterization data, with attention paid to thermal and trapping effects, along with extensive large-signal (or advanced testing) validation.

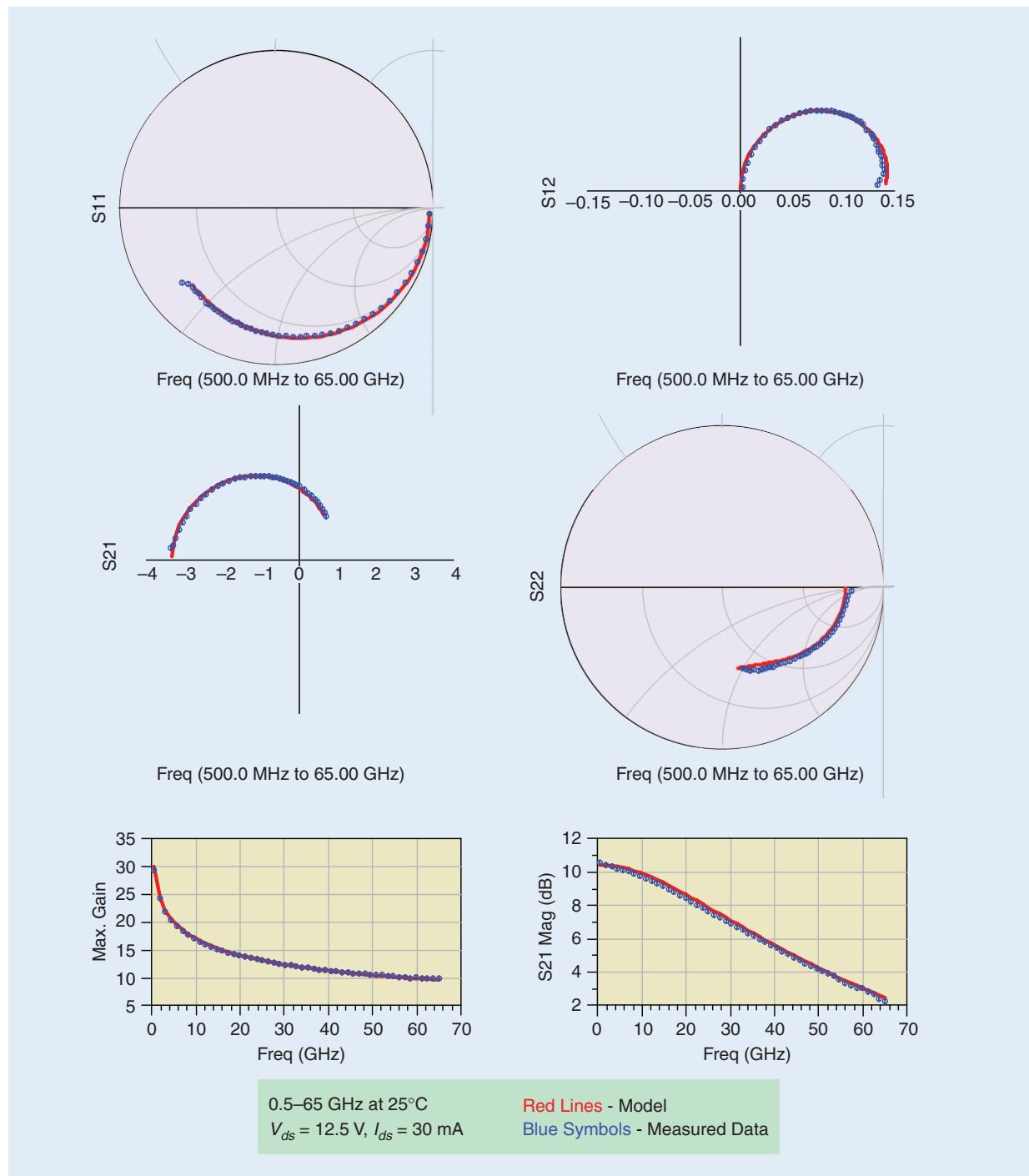


Figure 11. The S-parameter comparison for a $4 \times 37.5 \mu\text{m}$, GaN HEMT device.

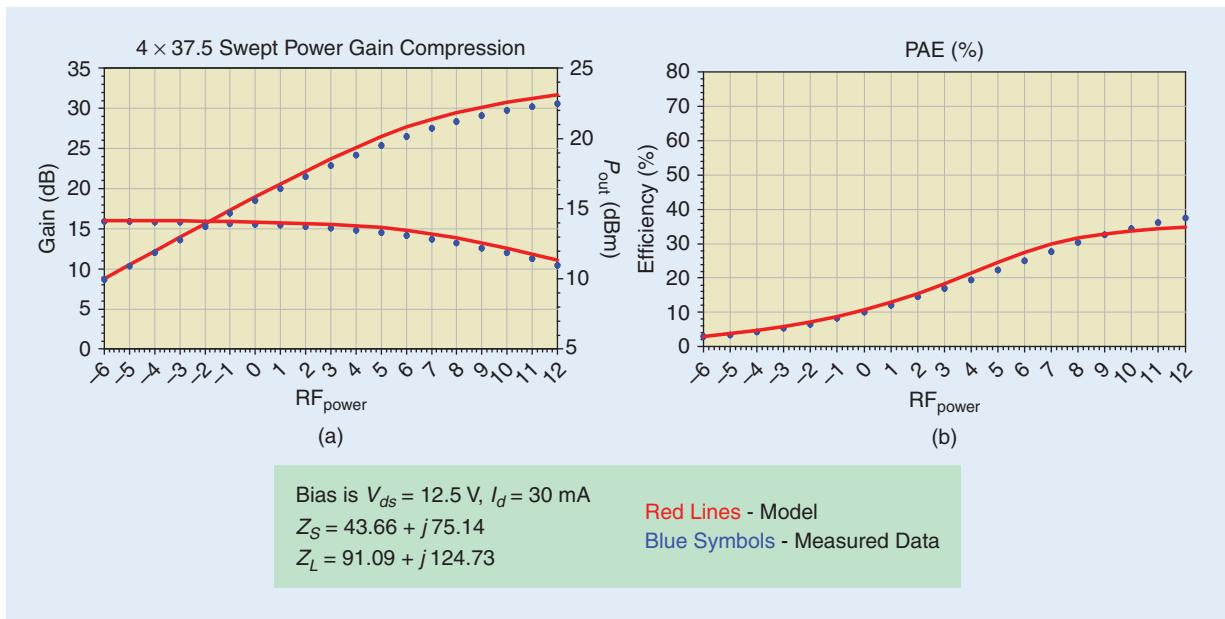


Figure 12. The 17-GHz power-tuned swept-power comparison of an EEHEMT for a $4 \times 37.5 \mu\text{m}$ GaN HEMT device.

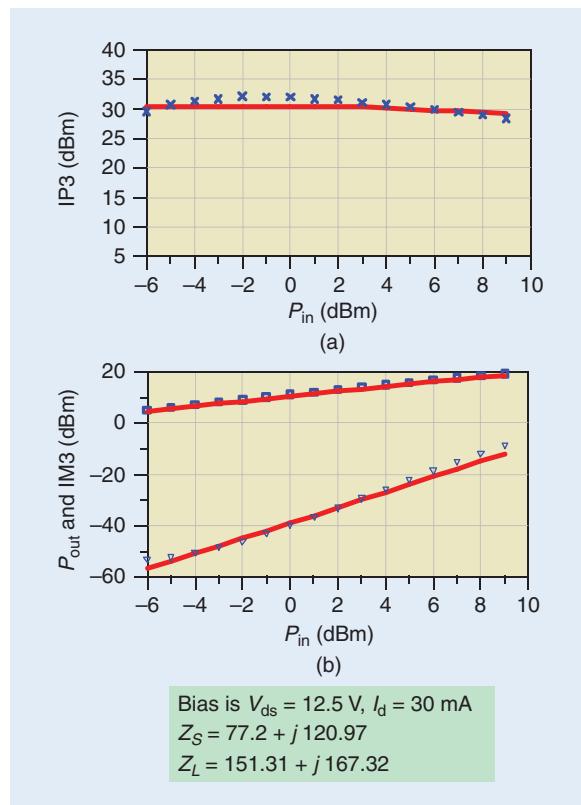


Figure 13. The 17-GHz IP3-tuned swept-power comparison of an extracted EEHEMT model (red line) and measured data (blue symbols) for a $4 \times 37.5 \mu\text{m}$ GaN HEMT device.

Example Modeling Results for GaN HEMT Devices

Next we will turn our attention to several example models for GaN HEMTs of various sizes. All the

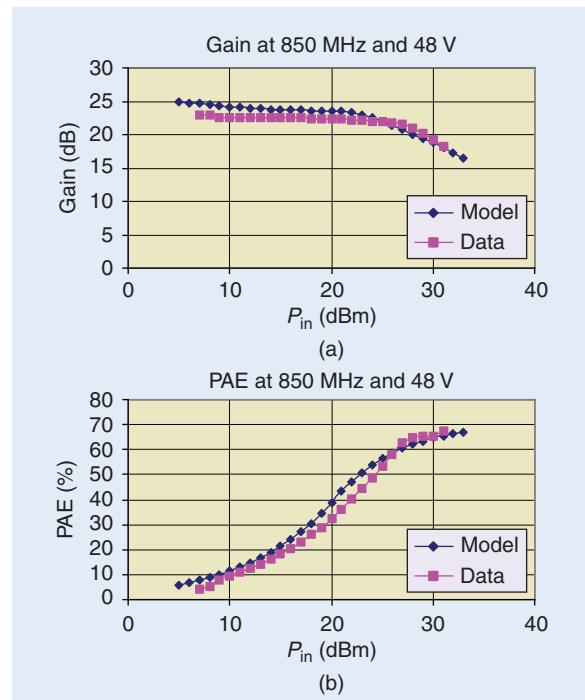


Figure 14. (a) Gain and (b) power-added efficiency (PAE) for a 45-W packaged GaN HEMT versus input power for $f = 850 \text{ MHz}$, $V_{DS} = 48 \text{ V}$, $Z_S = (2.046 + j1.960) \Omega$, and $Z_L = (6.857 + j5.7) \Omega$. This device was modeled with a Curtice FET model.

model examples presented in this section have been extracted by Modelithics, starting with an EEHEMT model example. Figures 10–13 show modeling results for a relatively small $4 \times 37.5 \mu\text{m}$ gate width geometry GaN HEMT chip intended for millimeter-wave applications. Figure 9 shows the $I\text{-}V$ curve is

With the powerful benefits of GaN devices, unique challenges are encountered as a result of trapping effects, related current collapse, high voltages and currents, and corresponding thermal issues.

reasonably well fit to measured data, with some differences observed in the knee region. Figure 11 shows a very good fit for all four S-parameters for this same model through 65 GHz. Figure 12 demonstrates that the model fits single-tone power-swept gain and

efficiency very well after the completion of a load-pull measurement at 17 GHz. Figure 13 indicates that it is possible to obtain good fits to third-order distortion measures with the EEHEMT model. The third-order intercept point (IP3) and third-order intermodulation levels are well predicted by the model extracted for this particular device. Moving on to a much larger device, Figure 14 shows favorable comparisons for an extracted CFET model for a 45-W packaged GaN HEMT device. Shown are swept power gain compression and efficiency comparisons made at optimal termination conditions determined from load-pull testing at 850 MHz.

As a final example, an Angelov model was extracted for a 10-W transistor and scaled to represent a 100-W

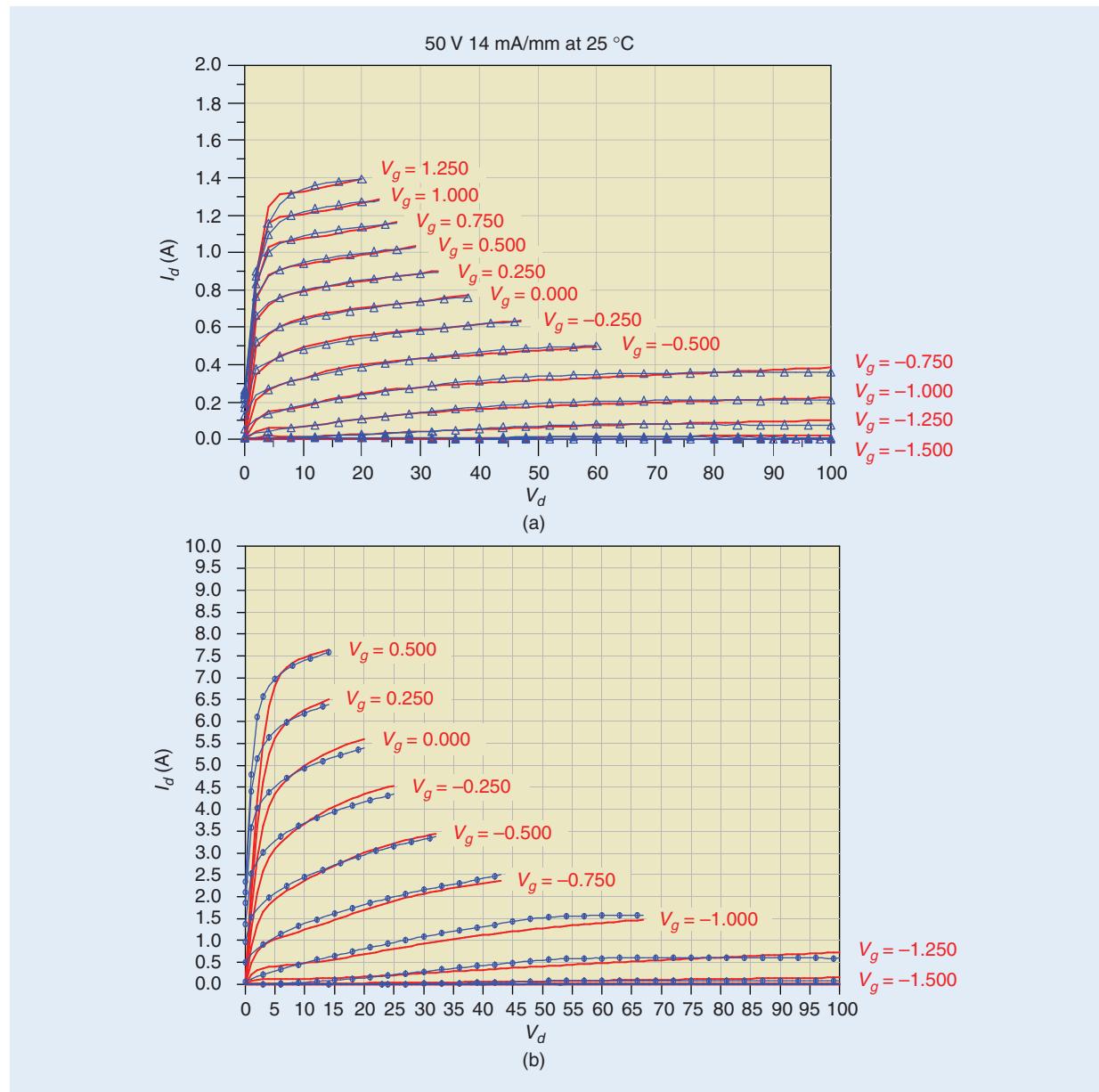


Figure 15. Pulsed I-V measured and simulated data for 10 W and 100 W chip-level GaN devices. Quiescent bias for both pulsed I-V sets is $V_{ds} = 50$ V and $I_{ds} \sim 0$. Pulse width was 0.2 μ s.

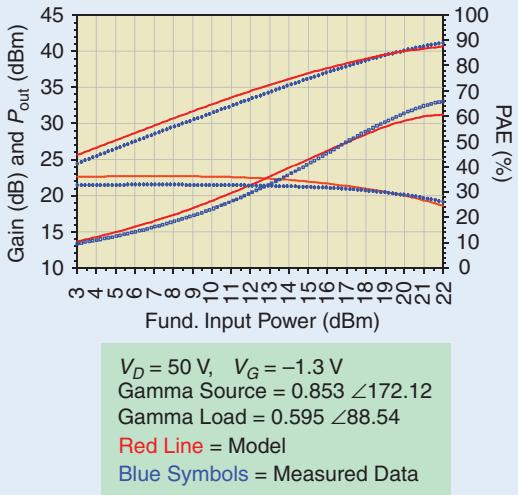


Figure 16. 25 °C power tuned power sweep for the 10 W unit cell GaN transistor measured at 2.14 GHz.

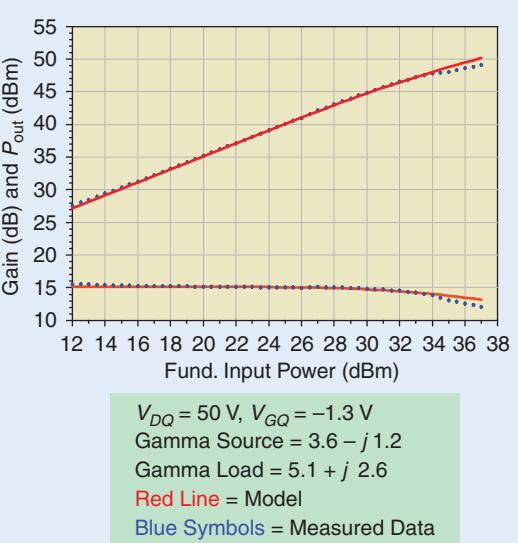


Figure 17. 2.14 GHz swept-power measurement of a 100 W GaN transistor compared to simulations with Modelithics scalable GaN model. Data is taken under pulsed conditions with 80 μs pulse period, 80% duty cycle.

transistor. The model used incorporates in-house quiescent bias and geometry scaling. The same model is used for all results shown, with only a change in scaling factors or quiescent bias included. Figure 15 shows pulsed I - V results for both devices, demonstrating a very good I - V fit over the entire operating region for both data sets. Figure 16 shows power-swept results after load-pull was performed on the 10 W transistor at 30 V, while Figure 17 demonstrates good agreement for simulations compared to pulsed load-pull results for the 100 W GaN data.

Conclusions

With the powerful benefits of GaN devices, unique challenges are encountered as a result of trapping effects, related current collapse, high voltages and currents, and corresponding thermal issues. This article has reviewed recent modeling work focused on addressing GaN modeling challenges along with strategies for successful measurement-based modeling of GaN transistors. The use of pulsed measurements as part of the modeling process, along with sufficiently flexible modeling equations and topologies, is critical for obtaining reliable electrothermal GaN models. In addition to the model extraction measurements of I - V and multiple-bias S-parameter data, large-signal measurements (load-pull, power sweep, linearity, and waveform) are also a critical part of model validation and improvement. Excellent model results can be obtained with suitable in-house models or by using established HEMT models available for popular microwave nonlinear circuit simulators. Examples are shown for accurate GaN models developed using the EEHEMT, CFET, and Angelov modeling templates. A given model's effectiveness will vary with the skills of the measurement and modeling team along with applications and power amplifier operating modes. The successful modeler will be aware of the need for accurate data, carefully applied extraction methodologies, along with the strengths and limitations of available models to obtain the best results for circuit designers.

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References

- [1] S. Trassaert, B. Budart, C. Gaquière, D. Théron, Y. Crosnier, F. Huet, and M. A. Poisson, "Trap effects studies in GaN MESFETs by pulsed measurements," *Electron. Lett.*, vol. 35, no. 16, pp. 1386–1388, Aug. 1999.
- [2] C. Charbonnaud, S. DeMeyer, R. Quere, and J. Teyssier, "Electrothermal and trapping effects characterization of AlGaN/GaN HEMTs," in *Proc. 2003 Gallium Arsenide Applications Symp.*, Munich, Oct. 6–10, 2003, pp. 201–204.
- [3] R. J. Trew, Y. Liu, G. L. Bilbro, W. Kuang, R. Vetury, and J. B. Shealy, "IEEE nonlinear source resistance in high-voltage microwave AlGaN/GaN HFETs," *IEEE Trans. Microwave Theory and Tech.*, vol. 54, no. 5, pp. 1824–1831, May 2006.
- [4] Y. Tajima, "Introduction of new large signal model (LS7) for MESFET family of devices," presented at *Workshop 38th European*

- Microwave Conf.: WFR-15: Advances in Model-based HPA Design*, Amsterdam, The Netherlands, Oct. 2008.
- [5] W. R. Curtice, *User's Guide for the C_FET Model for Agilent's Advanced Design Simulator*. Washington Crossing, PA: W. R. Curtice Consulting, June 2004.
- [6] V. Camarchia, F. Cappelluti, M. Pirola, S. Guerrieri, and G. Ghione, "Self-consistent electrothermal modeling of class A, AB, and B power GaN HEMTs under modulated RF excitation," *IEEE Trans. Microwave Theory and Tech.*, vol. 55, no. 9, pp. 1824–1831, Sept. 2007.
- [7] M.J. Casto and S.R. Dooley, "AlGaN/GaN HEMT temperature-dependent large-signal model thermal circuit extraction with verification through advanced thermal imaging," in *2009 IEEE WAMICON Dig.*, Clearwater, FL, Apr. 2009, pp. 1–5.
- [8] J. Lee, S. Lee, and K. Webb, "Scalable large-signal device model for high power-density AlGaN/GaN HEMT's on SiC," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2001, pp. 679–682.
- [9] J. Lee and K. Webb, "A temperature-dependent nonlinear analytic model for AlGaN–GaN HEMTs on SiC," *IEEE Trans. Microwave Theory and Tech.*, vol. 52, no. 1, pp. 2–9, Jan. 2004.
- [10] C. Baylis, L. Dunleavy, and R. Connick, "Modeling considerations for GaN HEMT devices," in *Proc. 10th IEEE Wireless and Microwave Technology Conf. (WAMICON)* 2009, Apr. 2009, pp. 1–2.
- [11] I. Angelov, K. Andersson, D. Schreurs, D. Xiao, N. Rorsman1, V. Desmaris, M. Sudow, and H. Zirath, "Large-signal modeling and comparison of AlGaN/GaN HEMTs and SiC MESFETs," in *Proc. Asia-Pacific Microwave Conf. 2006*, Dec. 2006, pp. 279–282.
- [12] W. R. Curtice and M. Ettenberg, "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 33, pp. 1383–1393, Dec. 1985.
- [13] Agilent Technologies, *ICCAP Software Documentation*. Palo Alto, CA: Agilent Technologies Inc., 2009.
- [14] I. Angelov, H. Zirath, and N. Rorsman, "A new empirical nonlinear model for HEMT and MESFET devices," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2258–2266, Dec. 1992.
- [15] F. Kharabi, M. J. Poulton, D. Halchin, and D. Green, "A classic nonlinear FET model for GaN HEMT devices," in *Proc. Compound Semiconductor Integrated Circuit Symp.*, Oct. 2007, pp. 1–4.
- [16] I. Angelov, V. Desmaris, K. Dynefors, P. Å. Nilsson, N. Rorsman, and H. Zirath, "On the large-signal modelling of AlGaN/GaN HEMTs and SiC MESFETs," in *Proc. European Gallium Arsenide and Other Semiconductor Application Symp.*, 2005 (EGAAS'05), Oct. 2005, pp. 309–313.
- [17] P. Cabral, J. Pedro, and N. Carvalho, "Nonlinear device model of microwave power GaN HEMTs for high power-amplifier design," *IEEE Trans. Microwave Theory and Tech.*, vol. 52, no. 11, pp. 2585–2592, Nov. 2004.
- [18] R. Pengelly, B. Millon, D. Farrell, B. Pribble, and S. Wood, "Application of non-linear models in a range of challenging GaN HEMT power amplifier designs," presented at *IEEE MTT-S Int. Microwave Symp. Workshop—WMC: Challenges in Model-based HPA Design*, Atlanta, GA, June 2008.
- [19] C. Fager, J. C. Pedro, N. B. de Carvalho, and H. Zirath, "Prediction of IMD in LDMOS transistor amplifiers using a new large-signal model," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 12, pp. 2834–2842, Dec. 2002.
- [20] J. Deng, W. Wang, S. Halder, W. Curtice, J. Hwang, V. Adivarahan, and M. Khan, "Temperature-dependent RF large-signal model of GaN-based MOSFETs," *IEEE Trans. Microwave Theory and Tech.*, vol. 56, no. 12, pp. 2709–2716, Dec. 2008.
- [21] O. Jardel, F. De Groote, C. Charbonniaud, T. Reveyrand, J. P. Teysier, R. Quéré, and D. Floriot, "A drain-lag model for AlGaN/GaN power HEMTs," in *IEEE MTT-S Int. Microwave Symp. Dig.* June 2007, pp. 601–604.
- [22] C. Baylis, "Improved techniques for nonlinear electrothermal FET modeling and measurement validation," Ph.D. dissertation, Univ. South Florida, 2007.
- [23] R. J. Trew, Y. Liu, W. Kuang, H. Yin, G. L. Bilbro, J. B. Shealy, R. Vetary, P. M. Garber, and M. J. Poulton, "RF breakdown and large-signal modeling of AlGaN/GaN HFETs," in *IEEE MTT-S Int. Microwave Symp. Dig.* 2006 June 2006, pp. 643–646.
- [24] *Level 60 UC Berkeley BSIM3-SOI DD model*. (June 2001). [Online]. Available: http://www.ece.uci.edu/docs/hspice/hspice_2001_2-178.html
- [25] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, and E. E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FETs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1999, vol. 2, pp. 419–423.
- [26] W. Curtice, L. Dunleavy, W. Clausen, and R. Pengelly, "New LDMOS model delivers powerful transistor library—Part 1: The CMC model," *High Frequency Electron. Mag.*, pp. 18–25, Oct. 2004.
- [27] W. R. Curtice, "Nonlinear transistor modeling for circuit simulation," in *RF and Microwave Handbook*, 2nd ed., M. Golio and J. Golio, Eds. Boca Raton, FL: CRC, 2008, Ch. 32.
- [28] P. Aaen, J. Pla, and J. Wood, *Modeling and Characterization of RF and Microwave Power FETs*. Cambridge, U.K.: Cambridge Univ. Press, 2007.
- [29] J. Gao, *RF and Microwave Modeling and Measurement Techniques for Field Effect Transistors*. Raleigh, NC: SciTech Publishing, Inc., 2010.
- [30] A. Platzker, A. Palevski, S. Nash, W. Struble, and Y. Tajima, "Characterization of GaAs devices by a versatile pulse IV measurement system," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1990, pp. 1137–1140.
- [31] D. Siriex, D. Barataud, P. Sommet, O. Noblanc, Z. Quarch, C. Brylinski, J. Teyssier, and R. Quere, "Characterization and modeling of nonlinear trapping effects in power SiC MESFETs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 765–768.
- [32] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1554–1561, Oct. 2004.
- [33] W. R. Curtice, "Nonlinear modeling of compound semiconductor HEMTs state of the art," in *IEEE MTT-S Int. Microwave Symp. Dig.* June 2010, pp. 1194–1197.
- [34] R. Negra, T. D. Chut, M. Helaoui, S. Boumaiza, G. M. Hegazit, and E. M. Ghannouchi, "Switch-based GaN HEMT model suitable for highly efficient RF power amplifier design," in *IEEE MTT-S Int. Microwave Symp. Dig.* June 2007, pp. 795–798.
- [35] K. Jenkins and K. Rim, "Measurement of the effect of self-heating in strained-silicon MOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 6, pp. 360–362, June 2002.
- [36] C. Baylis, L. Dunleavy, and J. Daniel, "Direct measurement of thermal circuit parameters using pulsed IV and the normalized difference unit," in *IEEE MTT-S Int. Microwave Symp. Dig.* June 2004, pp. 1233–1236.
- [37] S. Meena, C. Baylis, L. Dunleavy, and M. Marbell, "Duty cycle dependent pulsed IV simulation and thermal time constant model fitting for LDMOS transistors," in *74th ARFTG Symposium Dig.*, Boulder, CO, Dec. 2009.
- [38] C. Baylis, J. Perry, M. Moldovan, R. Marks, II, and L. Dunleavy, "Voltage transient measurement and extraction of power RF MOSFET thermal time constants," in *74th ARFTG Symp. Dig.*, Boulder, CO, Dec. 2009.
- [39] C. Baylis, L. Dunleavy, and W. Clausen, "Design of bias tees for a pulsed-bias, pulsed-RF test system using accurate component models," *Microwave J.*, Oct. 2006.
- [40] L. Betts, "Make accurate pulsed S-parameter measurements," *Microwaves RF Mag.*, Nov. 2003.
- [41] F. Thümmler and T. Bednorz, "Measuring performance in pulsed signal devices: A multi-faceted challenge," *Microwave J.*, Sept. 2007.
- [42] C. Baylis, L. Dunleavy, and J. Martens, "Constructing and benchmarking a pulsed-RF, pulsed-bias S-parameter system," in *ARFTG Symp. Dig.*, Washington, DC, Dec. 2005.



COMPARISON OF NON-LINEAR MESFET MODELS OVER 1-12 GHZ FREQUENCY RANGE¹

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ABSTRACT

This paper is an extension of work done previously on the comparison of non-linear MESFET models [3]. The list of models that are compared includes the Curtice quadratic, Curtice cubic, Statz, Materka, and Advanced Materka models to which the Angelov's model has been added. Furthermore, measurements and model prediction of intermodulation distortion (IMD) are now extended to 12 GHz. The comparison is based on the relative error observed between the measured and simulated DC I-V data, and average error for the model prediction of high frequency gain and IMD. Performance of various models is discussed.

1. INTRODUCTION

GaAs MESFETs are used in a variety of high-frequency and non-linear applications and it is, therefore, very important to model their behavior accurately across a large frequency and bias range. Initial study of DC and ac performance of various models was done in [1] and for non-linear performance in [2]. Different empirical models have been built over the years and various factors, such as gain, are used in comparing the performances of these models. An additional figure of merit is the amount of intermodulation distortion (IMD), which shows the effects of non-linear interactions of signals applied to the device. IMD is also relatively straightforward to measure.

In this work we analyze six models: Curtice quadratic and cubic, Statz, Materka, Advanced Materka and recently added Angelov's model [3-5], which are evaluated across a wide frequency and bias range.

2. MESFET MODELS

The topology of the large-signal MESFET model is common to all the models being investigated, and is shown in Figure 1. The difference among the models is

primarily in the functions that govern the current source I_{ds} and capacitances C_{gd} and C_{gs} .

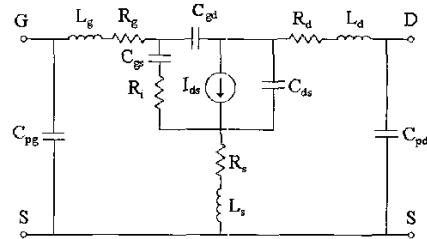


Figure 1. Large-signal model topology.

The extraction of various device parameters is often based on a small-signal equivalent circuit, which is some simplification of the large-signal model. Only the bias variation of different elements has to be modeled, typically by using a set of fitting formulas. The parameters for the formulas are extracted through an optimization procedure.

3. DC AND C-V MEASUREMENTS AND SIMULATIONS

The devices used for our measurements were on-wafer GaAs MESFETs with 300 μ m gate width. The results reported here were obtained from different devices and equipment than the results reported in [3] but the observed characteristics were, in general, very similar to our previous results. The DC measurements were done using HP 4145B parameter analyzer. The S-parameters were measured using Cascade ACP probes connected to Agilent 8722E vector network analyzer in the frequency range from 0.1 to 26.1 GHz. The DC and S-parameters were measured at the following bias points for parameter extraction: V_{ds} (drain voltage)=0V to 3V with a step of 0.2V and 3V to 8V with a step of 1V and V_{gs} (gate voltage)= -2.75V to 0.25V with a step of 0.25V. In addition, a set of "cold FET" measurements ($V_{ds} = 0$) was done.

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The model parameters were extracted using IC-CAP from Agilent [8]. All the models are built-in except for the Angelov's model, which was implemented on IC-CAP as a user defined model. The circuit simulations were carried out on Agilent ADS [9]. The Angelov's model is implemented on ADS using the Symbolically Defined Device (SDD) feature.

The extrinsic parameters R_D , R_G , R_S , L_D , L_G , L_S were obtained after the de-embedding using the procedure given by Dambrine [6]. These parameters are shown in Table 1 and are kept fixed in the subsequent steps.

Table 1. Parasitic resistances and inductances

Parasitics	R_D	R_G	R_S	L_D	L_g	L_s
Value	3.2	1.4	2.1	30.01	26.08	2.76

The intrinsic MESFET parameters were obtained after the de-embedding procedure. The initial DC and C-V parameters were obtained through extraction routines in IC-CAP and typically involved optimization on a subset of measured data. These model parameters were then included into ADS models and were globally optimized by reducing the relative error between the measured and simulated data.

The relative error is used in comparing various DC models and it is calculated from the following:

$$\text{REL. Error} = \sum \frac{|\text{SIMULATED_VALUE} - \text{MEASURED_VALUE}|}{\text{MEASURED_VALUE}} \quad (1)$$

NUMBER_OF_TESTPOINTS

Relative error gives a better representation for errors for the smaller current values. Table 2 contains the average relative error for five gate voltages. Shaded numbers indicate the best result.

Table 2. Relative error for a set of output I-V curves; V_{ds} changes from 0V to 6V.

V_{gs}	Angelov's	Curtice quadratic	Statz
-2.0V	213.96%	256.76%	44.2%
-1.5V	11.03%	21.42%	13.9%
-1.0V	7.105%	8.74%	6.07%
-0.5V	5.96%	6.68%	5.17%
0V	6.95%	8.4%	7.81%

V_{gs}	Curtice cubic	Materka	Advanced Materka
-2.0V	39.18%	207.25%	100%
-1.5V	7.3%	25.14%	8.59%
-1.0V	5.85%	7.82%	5.87%
-0.5V	5.97%	6.74%	5.16%
0V	7.68%	7.77%	6.46%

The best fit is given by Curtice cubic and Advanced Materka, but the differences are not as pronounced as observed before [3]. The Angelov's model does not

provide a good fit for gate voltages near cut-off. We observed somewhat increased knee voltage in the output I-V measurements, which made the accurate fit in the linear region more difficult, resulting in errors higher than previously observed. The source and ramifications of this increase in knee voltage are being investigated.

C_{gd} and C_{gs} were obtained by measuring S-parameters from 100MHz to 26.1GHz and by de-embedding the device so that intrinsic device parameters could be calculated. The C_{gd} and C_{gs} for a particular bias were obtained by averaging their values over the frequency range, but the actual variation of capacitances up to 10GHz was small. This procedure was repeated for $V_{gs} = -2$ to 0V in steps of 0.5V, with V_{ds} swept from 0 to 6V for each V_{gs} . As illustrated in Figure 2, Angelov's model has the best fit to C-V measurements, especially at low values of V_{ds} . Zero bias capacitances were found to be $C_{gd0} = 23$ fF, $C_{gs0} = 520$ fF. In addition, $f_T = 20$ GHz, and $f_{max} > 40$ GHz were deduced from S-parameters.

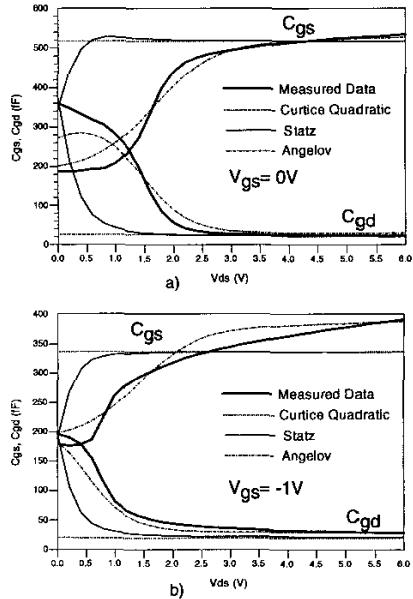


Figure 2. C-V measurements vs. simulation, a) $V_{gs}=0V$, b) $V_{gs}=-1V$.

4. INTERMODULATION DISTORTION

After the non-linear model parameters were extracted and optimized, we next investigated intermodulation distortion (IMD), which is a nonlinear effect occurring when two or more excitation frequencies are applied to the device. Output power is then distributed among the fundamental, second-, third-, fourth-, and higher-order IMD frequencies. In our experiments we applied two excitation frequencies, f_1 and f_2 , separated by 1 MHz. Third-order IMD product (IMD3) will occur at $2f_1-f_2$ and

$2f_2-f_1$. Output power was measured at fundamental and IMD3 frequencies.

We measured IMD at 3 different biases and at eleven different center frequencies. Biases were chosen to represent low-noise, class A, and maximum gain region of operation. Table 3 shows the measurements made for 1.1 GHz. The other center frequency points are as follows: 1.4, 1.7, 2.3, 2.6, 2.9, 4, 5, 7, 9, and 12 GHz.

Table 3: Bias and frequency for IMD measurements

f_1 (GHz)	f_2 (GHz)	V_{gs} (V)	V_{ds} (V)	Bias type
1.1	1.101	0	5	100% I_{dss}
1.1	1.101	-0.9	5	50% I_{dss}
1.1	1.101	-1.7	5	10% I_{dss}

Source power was swept from -20 to +18 dBm in 1 dBm steps and output power was measured at fundamental and IMD3 frequencies using spectrum analyzer. Power losses (cables etc.) were calibrated up to the probe tips.

After obtaining measured data, all models were simulated using the ADS harmonic balance feature to obtain output power at fundamental and IMD3 frequencies. At each frequency and bias point, an average error in dBm between measured and simulated data was calculated over the range of input available powers.

5. MODEL COMPARISON

The various models are compared by plotting the output power P_{out} vs. frequency for 100% I_{dss} , 50% I_{dss} and 10% I_{dss} . Figures 3 and 4 show the plots for the errors between the measured P_{out} at fundamental and IMD3 and the ones obtained from simulations. From the plots we observe that the errors tend to "stabilize" above 5 GHz i.e. there is not much change in errors from one frequency point to another, whereas there are significant changes below 5 GHz. We also observe a sharp increase in errors at 4 GHz. The source of this is under investigation; it could be due to some resonance set up by, e.g., an isolator whose cut-off is at 4 GHz.

From Figure 3 one can qualitatively conclude that Statz model provides the best overall fit, i.e. across the frequency and bias range, for P_{out} (or gain) at fundamental frequency. In the lower frequency range differences between models are less pronounced. At the 10% I_{dss} bias, Curtice Cubic and Angelov's model had significantly larger errors at frequencies larger than 4 GHz.

Figure 4 shows somewhat surprising level of error for IMD3 results. For 100% and 50% I_{dss} bias points, results for different models are reasonably close to each other, but Curtice cubic performs the best. Near cut-off, i.e. at 10% I_{dss} , Advanced Materka and Statz show the best results.

6. CONCLUSIONS

Previous work done on the comparison of the non-linear MESFET models was extended by including the

Angelov's model and extending the measurements and model predictions of the IMD to 1-12 GHz range. In terms of DC fit, all models had similar errors, except near cut-off, where Curtice cubic and Statz model showed significantly better results. C-V curves were best fitted by Angelov's model. When it comes to IMD, at this time it is difficult to establish a single best model for use across the frequency range and bias points, since some models are more accurate but only in a relatively limited range. One model that did show a reasonably uniform accuracy was Statz model. Interestingly, despite having the best fit to C-V curves and very good DC performance, Angelov's model didn't show any remarkable improvement over other models in terms of IMD performance. This may change once we evaluate the performance for the linear bias point, where a better C-V fit at lower V_{ds} voltage may become important.

Ultimately, we want to find the dominant non-linear mechanism for different models. This would shine some light on how to improve the models and potentially also help us understand how to improve the device performance. This study is an initial step toward that goal. Future work will also address reasons for 4 GHz spikes in error, difficulty in matching the linear region of I-V curves, as well as adding more models, such as TOM3.

7. REFERENCES

- [1] Rodriguez, Al-Daas, and Mehzer "Comparison of Nonlinear MESFET Models for Wideband Circuit Design," *IEEE Trans. Electron Devices*, vol. 41, no. 3, March 1994.
- [2] M. Monte et al "Choosing an Optimum Large Signal Model for GaAs MESFETs and HEMTs" *IEEE MTT-S Digest*, 1990.
- [3] E. Sijercic and B. Pejcincovic, "Comparison of Non-linear MESFET Models, *Proc. ICECS 2002*, Dubrovnik, Croatia.
- [4] I. Angelov, H. Zirath, and N. Rorsman, "A New Empirical Nonlinear Model for HEMT and MESFET Devices," *IEEE Trans. MTT*, vol. 40, no. 3, pp. 2258-2266, Dec. 1992.
- [5] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the Chalmers Nonlinear HEMT and MESFET model," *IEEE Trans. MTT*, vol. 44, no. 10, pp. 1664-1674, 1996.
- [6] G. Dambrine et al. "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE Trans. MTT*, vol. 36, no. 7, pp. 1151-1159, July 1988.
- [7] R. Anholt, *Electrical and Thermal Characterization of MESFETs, HEMTs, and HBTs*, Artech House, Boston, 1995.
- [8] HP Eesof (Agilent) "IC-CAP 5.0" manual, HP, June, 1997
- [9] HP Eesof (Agilent) "HP Advanced Design System Essentials," HP, May 1998

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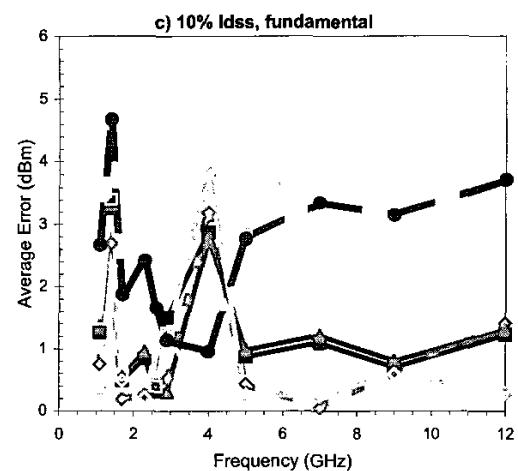
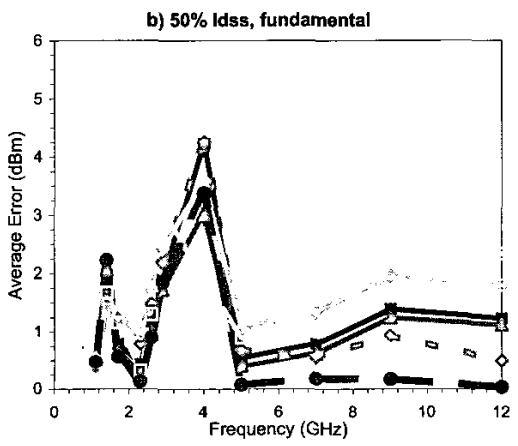
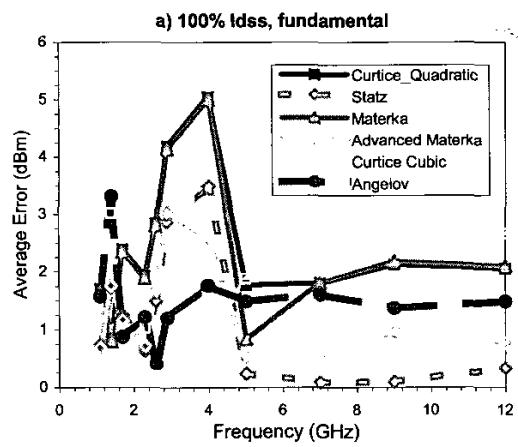


Figure 3. Average error in P_{out} vs. frequency for three bias points: a) 100%, b) 50%, and c) 10% Idss

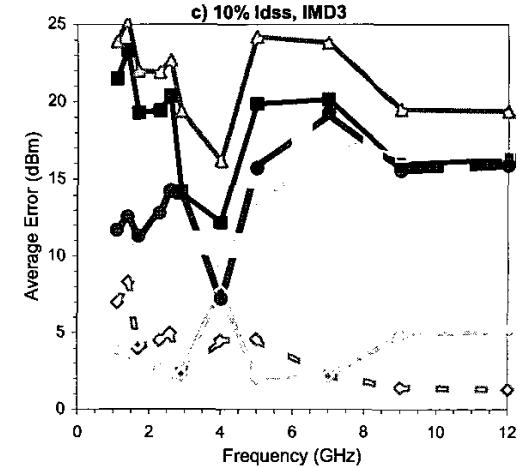
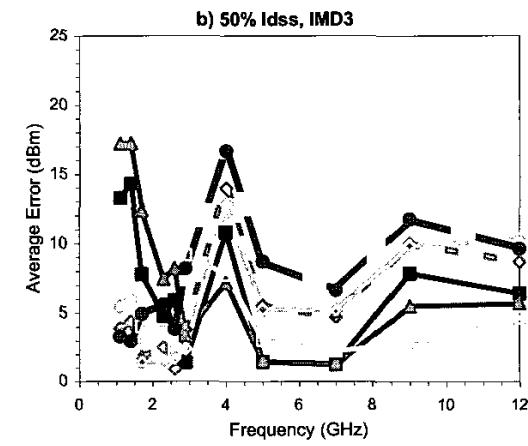
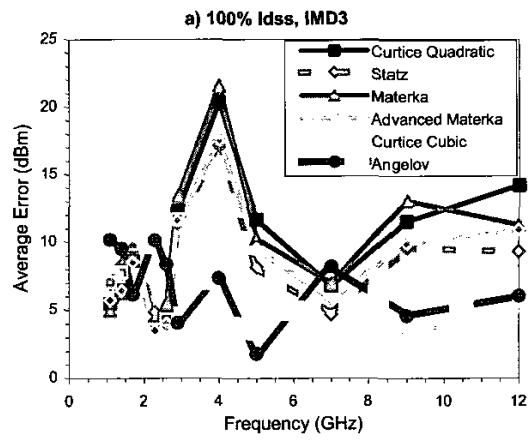


Figure 4. Average error in IMD3 vs. frequency for three bias points: a) 100%, b) 50%, and c) 10% Idss

NONLINEAR MODELLING OF POWER FETs AND HBTs

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Abstract: Large-signal modelling and simulation techniques for microwave and millimeter-wave transistors are described. The relative merits of physical, physics-based and non-linear equivalent circuit models are summarized.

Introduction: Many important microwave and millimeter sub-systems, such as oscillators, power amplifiers and mixers, operate in large-signal modes. Indeed, the key operating parameters of these circuits are functions of the non-linearities present in the circuit. These non-linearities are functions of the magnitudes of the signal currents and voltages present in transistor circuits relative to the bias levels. In practice, non-linear operation may occur at relatively low power levels (a few tens of milliwatts in an amplifier). Individual transistors operating at frequencies above 4 GHz are rarely capable of CW power outputs above 10 Watts, requiring power combining for higher power levels. This in turn implies that the impedance levels at the input and output of the transistor must be compatible with low-loss impedance matching circuits to achieve satisfactory power added efficiencies in power amplifiers. The choice of transistor technology depends on the application and the key operating criteria. At lower frequencies there is a high demand for single-supply high-efficiency circuits in portable commercial communications applications and as a result there is strong interest in using silicon BJT, Si/Ge and AlGaAs/GaAs heterojunction bipolar transistors. In high power applications ($>10W$) below 2 GHz, silicon bipolar transistors are the dominant technology because of their superior thermal properties and well established technology. A recent trend has been towards the requirement for very high linearity in multi-carrier power amplifier circuits at frequencies up to 12 GHz using both bipolar and MESFET technologies. At higher frequencies the emphasis on attaining high output powers at frequencies up to 100 GHz has led to great interest in using pHEMT technology. At all frequencies, a major factor is the cost-effectiveness of the technology and in this respect the well established MESFET satisfies many power amplifier and oscillator requirements at frequencies up to 20 GHz.

The traditional approach to modelling microwave transistors is based almost exclusively on extracting models from direct electrical and RF measurements. This data is used either in the form of 'black-box' parameters (S , y or z) or is manipulated to extract equivalent circuit models with closed-form equations associated with semi-empirical parameter extraction techniques. This approach has been successfully applied to the design of small-signal circuits in both hybrid and monolithic forms at frequencies up to 60 GHz. However, in the case of large-signal circuits, such as power amplifiers, conventional methods require extensive large-signal characterization, which may take the form of load-pull measurements or a combination of DC curve-fits and multiple bias-dependent S parameter measurements to extract the non-linear equivalent circuit model. If the intermodulation performance of the intended circuit is important it will also be necessary to carry out a series of two-tone (or multi-tone) measurements. Many applications specify a wide range of operating temperatures, which may need to require sets of large-signal measurements at a number of temperatures within the specified range. The self-heating of power transistors also implies that the final circuit should take account of the thermal conditions which exist during the large-signal characterisation process. The final large-signal non-linear model is then used in association with non-linear circuit design tools. Experimentally-based modelling techniques are suitable for established, well characterised devices, intended for operation in circuits which are designed within a limited range of operating conditions (frequency range, number of signals, bias,

signal level, impedances and temperature). It is difficult to apply this approach to new devices or custom monolithic circuit designs.

The desire to minimise the cost of the design and development process for new devices and circuits means that predictive models are required, quantitatively defining the device and circuit characteristics prior to fabrication. In these circumstances an empirically-based equivalent circuit model approach is not always appropriate. This large-signal design problem is particularly acute in the case of monolithic circuits where the embedded nature of the transistors makes it very difficult to measure the intrinsic operating characteristics. Furthermore, unlike hybrid microwave integrated circuits, it is extremely difficult to modify monolithic circuits after they are fabricated if they fail to meet the required specification. These challenges have led to the requirement for new techniques capable of dealing with non-linear operation of microwave transistors operating at higher frequencies and in new circuit configurations.

The requirement for accurate non-linear models for microwave transistors and circuits, coupled with the desire to optimize their performance, has led to considerable interest in using physical models to design and improve devices and circuits [1]. Physical models are based on a description of the physical processes which characterise the transistor and circuit. In the case of the active device this requires a description of the carrier transport physics and the associated geometrical and materials properties of the transistor. Physical models should be distinguished from 'physics-based' equivalent circuit models where the element values are obtained from expressions which phenomenologically relate the circuit elements to the device physics. Physics-based equivalent circuit models model can be useful in relating the transistor performance to the geometry and physics of the device, but their application is often limited by the same factors which apply to equivalent circuit models. In particular, even with an extensive set of physical data on the transistor, this type of model requires a detailed set of measurements and empirical fitting factors. Nevertheless, physics-based models provide an attractive means of describing transistors for well characterised fabrication processes and are particularly useful for applications where the device characteristics are very sensitive to the process and the advantages of full physical models are diminished (for example the ideality factor of the junctions in HBTs is strongly dependent on the process and material qualities). An example of a physics-based HBT model is given later in this paper.

Physical models have traditionally been regarded as the domain of device-physicists and researchers, requiring very powerful computers to obtain qualitative results. However, dramatic advances in computer technology over the past decade have brought the computing time and memory requirements of physical models within the realm of the desk-top workstation. This has in turn allowed engineers to apply physical models to complex device structures to develop new types of semiconductor device and enhance established designs. Indeed, physical device simulation software is now commercially available with powerful graphical user interfaces which is capable of representing devices in two- and three-dimensions. The insight provided by physical models and their ability to directly relate the microwave performance of transistors to the geometrical and material properties of the device have made physical models a useful tool for the device engineer. The utility of this approach is being extended to the microwave design engineer with the advent of new faster physical models which provide accurate solutions in time-frames comparable with non-linear equivalent circuit models. This class of model includes the quasi-two-dimensional simulation, described later in this paper.

This paper will review the current trends in nonlinear modelling of microwave power transistors addressing nonlinear equivalent circuit models, physical models and physics-based models.

Nonlinear Equivalent Circuit Models: Equivalent circuit models are relatively straightforward to construct and analyse using well established circuit theory. This is the most widely used type of transistor model and in the case of large-signal models constitutes a mixture of linear and non-linear

elements. There are several stages in developing a comprehensive non-linear power transistor model. There are some differences in the model development for FETs and bipolar transistors. We will initially consider the case of MESFETs and HEMTs. The DC and CV characteristics are required to obtain the input and output characteristics, breakdown voltages, contact/junction ideality factors and static capacitance behaviour. Several types of RF measurement are required to unambiguously de-embed the intrinsic device behaviour [2]. The parasitic elements may be extracted using a series of 'cold' and 'hot' measurements. 'Cold' measurements are performed with the transistor biassed at $V_{DS}=0$ and pinched-off (no current flow) and S parameters are measured over a range of frequencies. A number of low frequency S parameter measurements are usually needed to minimise inductive effects when extracting the pad capacitances. 'Hot' measurements are performed with the gate in forward-bias. The frequency-independent values of the parasitic elements (capacitances, resistances and inductances) associated with packaging, mounting and probing are then extracted by converting the measured data to Z and/or Y parameters. Straightforward analytic expressions relate the real and imaginary parts of the two-port parameters to the parasitic resistances, capacitances and inductances.

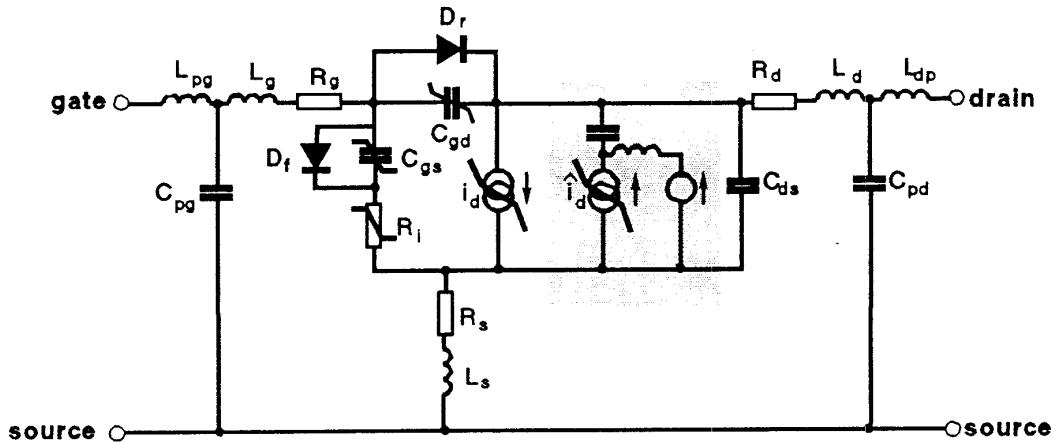


Figure 1 Large-signal equivalent circuit model of a microwave FET (suitable for MESFETs and HEMTs) with elements included to represent dispersion at low frequencies (shaded region).

Following the extraction of the parasitic elements, an extensive set of S parameter measurements is required over a wide range of DC bias conditions. In the case of power transistors this will include the breakdown, pinch-off and gate-forward conditions. It is also necessary to carry out these measurements over a frequency range extending from well below 1 GHz (to account for dispersion) to above the highest harmonic frequency of interest. The bias-dependence of the intrinsic static transconductance and output conductance obtained from the DC results are then compared with the bias-dependent results extracted from the bias-dependent S parameter results. Differences between the two sets of results are used to determine the dispersion (often resulting in an increase in output conductance of up to a factor of $4\times$ over the frequency range 1 Hz to 1 MHz). Dispersion is usually modelled with the addition of a RC network in the output circuit of the FET. More complex models model dispersion by including a network with current and voltage source connected via an inductor and capacitor to the drain and source nodes (Figure 1). At this stage the bias-dependence of the elements is assessed and any weakly dependent elements are set to constant values to simplify the model. The remaining bias-dependent elements are then described using multi-dimensional analytic functions or look-up tables with v_{DS} and v_{GS} as the parameters. The final model is then validated by checking that it accurately represents the measured DC characteristics and S parameters over the full frequency range. In the case of power

transistors it is also necessary to validate the non-linear capabilities of the model by independently comparing the large-signal performance of the model with results obtained from load-pull (or at least a number of power tests). A typical non-linear FET model (suitable for both MESFETs and HEMTs) is shown in Figure 2.

The drain current curve-fit is central to all non-linear FET equivalent circuit models. There are a wide range of formulae available. Some of the most popular expressions are:

$$\begin{aligned}
 & \text{Curtice: } I_{DS} = \beta(V_{DS} - V_{TO})^2 (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) \\
 & \text{Statz: } I_{DS} = \frac{\beta(V_{GS} - V_{TO})^2}{1 + b(V_{GS} - V_{TO})} (1 + \lambda V_{DS}) \tanh(\alpha V_{DS}) \\
 & \text{Materka-Kacprzak: } I_{DS} = \beta \left(1 - \frac{V_{GS}}{V_T} \right)^2 \tanh \left(\frac{\alpha V_{DS}}{V_{GS} - V_T} \right) \quad \text{where } V_T = V_{TO} + \gamma V_{DS}
 \end{aligned} \tag{1}$$

The model parameters $\alpha, \beta, \lambda, \gamma, b$ are fitted to measured data and V_{TO} is the measured threshold voltage.

The gate capacitances are also strong functions of bias and are usually modelled using derivatives of the well known Schottky capacitance function $C(V) = C_0/(I-V/V_{Bi})^m$. Among the most popular capacitance models is the Statz model:

$$\begin{aligned}
 C_{gs} &= \frac{C_{GSO} K_1 K_2}{\left(1 - \frac{V_n}{V_{Bi}} \right)^{0.5}} + C_{gd0} K_3 \\
 C_{gd} &= \frac{C_{GSO} K_1 K_3}{\left(1 - \frac{V_n}{V_{Bi}} \right)^{0.5}} + C_{gd0} K_2
 \end{aligned} \tag{2}$$

where, for $\delta = 0.2$

$$\begin{aligned}
 K1 &= 0.5 \cdot [1 + (V_e - V_{TO}) / [(V_e - V_{TO})^2 + \delta^2]^{0.5}] \\
 K2 &= 0.5 \cdot [1 + (V_{gs} - V_{gd}) / [(V_{gs} - V_{gd})^2 + (1/\alpha)^2]^{0.5}] \\
 K3 &= 0.5 \cdot [1 - (V_{gs} - V_{gd}) / [(V_{gs} - V_{gd})^2 + (1/\alpha)^2]^{0.5}] \\
 V_n &= 0.5 \cdot [V_e + V_{TO} + [(V_e - V_{TO})^2 + \delta^2]^{0.5}] \quad \text{if } V_n < 0.5 \text{ else } V_n = 0.5 \\
 V_e &= 0.5 \cdot [V_{gs} + V_{gd} + [(V_{gs} - V_{gd})^2 + (1/\alpha)^2]^{0.5}] \quad \text{if } 0.5 \cdot [V_e + V_{TO} + [(V_e - V_{TO})^2 + \delta^2]^{0.5}] < 0.5
 \end{aligned}$$

Physics-Based Equivalent Circuit Models: Physics-based equivalent circuit models associate elements with specific physical processes in the active device. In this respect this type of model often appears topologically identical to other equivalent circuit models. However, the fundamental difference between this and the previous class of equivalent circuit model is that the element values in physics-based models are derived from (or attributed to) the physics governing the operation of the device, rather than purely based on fitting parameters to DC and microwave data measured at the 'terminals' of the transistor. Physics-based models are available in varying degrees of complexity. For example, HBTs can be represented by a physics-based equivalent circuit as simple as the Gummel-Poon model in Figure 3 or they can be considered in terms of the very detailed model of Grossman and Chroma's award winning paper [3], with over 40 circuit elements associated with the physics of the device. In the case of GaAs MESFETs and HEMTs, a particularly good overview of physics-based equivalent circuit models is given in Ladbrooke's book [4].

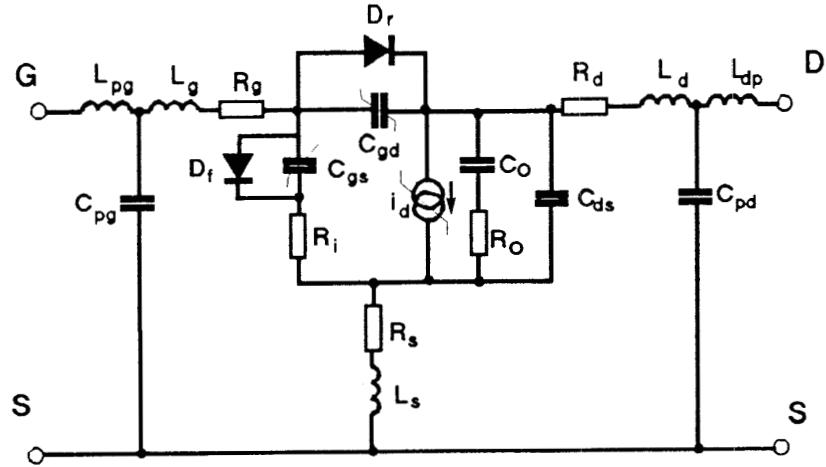


Figure 2 Large-signal model of FET widely used in microwave circuit design.

Most HBT large-signal models are based on either the Ebers-Moll [6] or Gummel-Poon [5] configurations. The Gummel-Poon model, originally developed in 1970, is superior to the basic Ebers-Moll model, remaining valid in the high injection regime and including recombination effects present in the space-charge regions. The basic Gummel-Poon model it is not directly applicable to HBTs, because the base current in HBTs is dominated by surface or bulk depletion layer recombination, rather than hole injection from the base into the emitter. The base current at low current densities is mainly due to surface recombination [7,8,9]. Recombination at the base surface occurs as a result of electrons injected from the emitter. However, the temperature dependence of the equivalent circuit element values suggests that the base current at high current densities is largely attributable to depletion layer recombination. A consequence of this is that the ideality factor of base current is always higher than the ideality factor of the collector current. Furthermore, this results in two regions of increasing current gain with increasing intrinsic base-emitter bias V_{BE} . The two regions of current gain in the HBT are defined by the component of base current that is dominant in each region (surface or bulk recombination). In the case of the classical Gummel-Poon model, the current gain increases initially, flattens and then decreases with increasing V_{BE} . Emitter crowding is negligible in AlGaAs/GaAs HBTs, unlike their silicon homojunction counterparts.

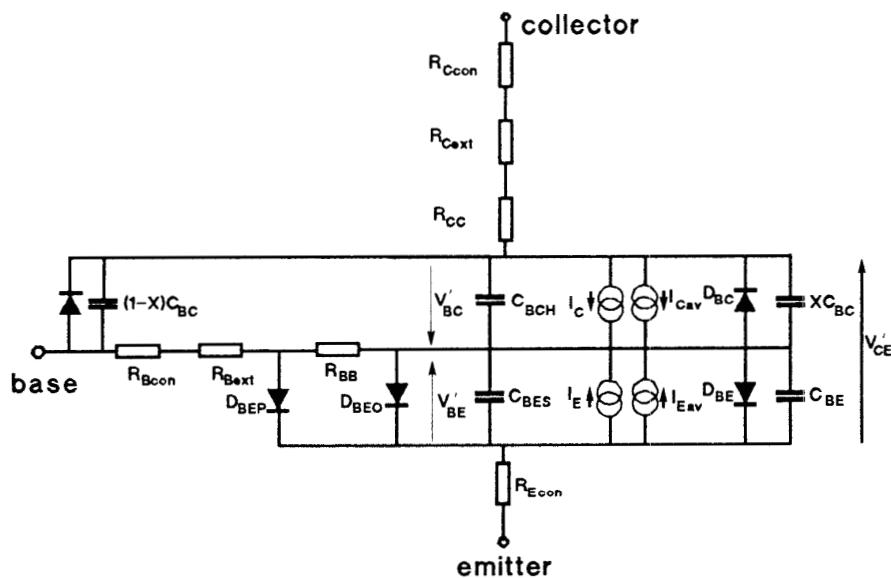


Figure 3 Modified Gummel-Poon model suitable for large-signal HBT simulation

The forward base current has two components - the bulk depletion layer recombination (described by I_{SE} and N_E) and the surface recombination (described by I_{SES} and N_{ES}). The reverse characteristics in HBTs are not necessarily characterized by the same processes as those in the forward direction. In single heterojunction transistors, it is common for the reverse base current ideality factor N_C and emitter current ideality factor N_R to be equal, resulting in a region of relatively constant current gain as a function of emitter current. In practice, the surface recombination base current dominates in reverse operation (I_{SCS}), and the reverse bulk recombination/injection component can be neglected. The surface recombination component typically has an ideality factor in the region of 2. Neutral base recombination is attributable to non-radiative centers in the base layer and is strongly influenced by material quality (and trap density).

All the saturation currents (I_{SE} , I_{SES} , I_{SC} , I_{SCS} , I_S) have a strong temperature dependence [3]. The saturation currents and ideality factors are extracted from Gummel plots (forward and reverse). The collector and emitter current ideality factors N_F and N_R respectively are usually found to be constant with variations in temperature and lie in the range 1.0 to 1.2. In the case of temperature dependent ideality factors, such as the base current ideality factor N_E , the ideality factor is approximated using a linear or quadratic temperature dependence.

Although most of the model parameters are directly related to the physical structure of the HBT, some of the data is highly process-dependent and cannot be accurately determined from closed-form physics-based relationships. In particular, the ideality factors, saturation currents and temperature dependence of these factors varies significantly with the fabrication process. These diode parameters are obtained from measured data and have been found to be consistent from batch to batch for any given process, and can be assumed to be constant for any given design of HBT.

The problem of bending in the Gummel plots at high current levels and the associated problem of obtaining a suitable linear approximation to find I_S and N_F can be overcome by plotting $\log(\beta)$ against $\log(I_c)$ [10]. The use of $\log(I_c)$ as the independent variable corresponds with the use of the intrinsic base-emitter voltage V_{BE} , because the high doping in the base of HBT's eliminates high injection effects. The parameters I_{SE} , N_E , I_{SES} and N_{ES} can be obtained using the $\log(\beta)/\log(I_c)$ characteristics.

The fully expanded equations for the HBT, equivalent to the essentially Gummel-Poon model described earlier, take the form,

$$\begin{aligned}
 I_C &= \frac{I_S}{\beta_F} \left[\exp\left(\frac{V_{BE}}{N_F V_T}\right) - \exp\left(\frac{V_{BC}}{N_R V_T}\right) \right] - \frac{I_S}{\beta_R} \left[\exp\left(\frac{V_{BC}}{N_R V_T}\right) - 1 \right] \\
 &\quad - I_{SC} \left[\exp\left(\frac{V_{BC}}{N_C V_T}\right) - 1 \right] - I_{SCS} \left[\exp\left(\frac{V_{BC}}{N_{CS} V_T}\right) - 1 \right] \\
 I_B &= \frac{I_S}{\beta_F} \left[\exp\left(\frac{V_{BE}}{N_F V_T}\right) - 1 \right] + \frac{I_S}{\beta_R} \left[\exp\left(\frac{V_{BC}}{N_R V_T}\right) - 1 \right] + I_{SC} \left[\exp\left(\frac{V_{BC}}{N_C V_T}\right) - 1 \right] \\
 &\quad + I_{SCS} \left[\exp\left(\frac{V_{BC}}{N_{CS} V_T}\right) - 1 \right] + I_{SE} \left[\exp\left(\frac{V_{BE}}{N_E V_T}\right) - 1 \right] + I_{SES} \left[\exp\left(\frac{V_{BE}}{N_{ES} V_T}\right) - 1 \right]
 \end{aligned} \tag{3}$$

where I_S is the forward collector saturation current, I_{SE} is the saturation current for recombination in the base-emitter space-charge region, I_{SC} is the saturation current for recombination in the base-collector space-charge region, I_{SES} is the saturation current for recombination in the base-emitter surface depletion region, I_{SCS} is the reverse surface depletion region recombination current. The Early effect

is neglected in these equations. The surface recombination currents are included in this formulation for the first time, representing an improvement over the earlier Hafizi model [9].

The collector current is not an instantaneous function of the base current because it takes a finite time for electrons injected at the emitter side of the base to reach the collector. Velocity overshoot can have a significant effect on the transport of carriers in HBTs and plays a significant role in the base-collector space-charge region. Grossman et al developed a model for I_{CC} in the base-collector space-charge region using a simplified velocity profile with two sections. Their model is based on applying the Ramo-Shockley theorem which requires that the collected electron current I_{CC} be the spatial average of the current in the base-collector space charge region. Tiwari [11] develops a collector transport factor to account for dispersion effects due to variation in overshoot with time during switching.

The two main breakdown mechanisms in bipolar junction transistors are avalanche breakdown of the collector-base junction and punch-through breakdown. Punch-through breakdown occurs when the reverse collector-base voltage increases to the point where the collector-base depletion region merges with the emitter-base depletion region. This is not a common mechanism in HBTs. Breakdown in the emitter-base junction only occurs under exceptional reverse-bias conditions and is attributable to Zener breakdown in HBTs. The critical voltage at which avalanche breakdown occurs in bipolar transistors depends on the transistor configuration and on the external circuit.

$$R_{bulk} = \rho \frac{L}{A} = R_s \frac{L}{W} \quad (4)$$

In physics-based models the bulk ohmic resistances may be calculated using the following relationship, where ρ is the resistivity and R_s is the sheet resistance. When current flows through a contact surface, normal to the contact, it is possible to define the vertical contact resistance as $R_{VC} = 1/AG_C$, where A is the area of the contact and G_C is the conductance per unit area of the contact. Vertical contact resistances are important in HBTs to represent the emitter contact and base contact resistance in series with the extrinsic base-collector capacitance. When current flows through a contact in parallel with the contact surface, a lateral contact resistance is defined. This resistance is attributable to both the contact and sheet spreading resistance. In the case of a contact of length L and width W , the lateral contact resistance is given by,

$$R_{LC} = \frac{(R_s/G_C)^{0.5}}{W \tanh(L/L_C)} \quad (5)$$

Here the contact characteristic length $L_C = (1/G_C R_s)^{0.5}$. In the context of these definitions the length is defined in the plane of the device cross-section and the width of the contact is normal to the cross-section (as for gate dimensions in FETs). When a current enters a sheet region of material and leaves normal to the sheet surface (with constant current density), a spreading resistance may be defined. In the case of HBTs spreading resistances occur in the base layer beneath the emitter mesa and in the contact layer beneath the base mesa. In these regions the doping is high and the resistivity low, allowing spreading resistances to accurately represent the behaviour in these regions. The spreading resistance for a region of width W , length L and sheet resistance R_s , for a single contact reduces to $R_{SPR} = R_s L / 3W$. When current enters the region from two sides, as is the case when multiple contacts are present, the spreading resistance is reduced by a factor of four as there are two parallel paths, each of half the length.

The capacitances associated with HBTs are modelled using depletion region approximations and space-charge region charge-storage relationships. The base-collector junction in most HBTs is an abrupt homojunction. The junction consists of the highly doped base and lightly doped collector regions. The

lightly doped collector region interfaces with the highly doped collector contact layer. The base-collector depletion capacitance model consists of two relationships to represent the conditions when the base-collector depletion layer is inside the lightly doped collector and when the depletion layer extends into the highly doped contact layer. In the first case,

$$C_C = \frac{C_{JC}}{\left(1 - \frac{V_{BC}}{V_{JC}}\right)^{M_C}} \quad (6)$$

where M_C is the junction grading coefficient (0.5 for the abrupt base-collector in a HBT). The zero bias base-collector junction capacitance C_{JC} is given by,

$$C_{JC} = A_{coll} \left(\frac{q N_{Dcoll} N_{Abase}}{2 V_{JC} (N_{Abase} + N_{Dcoll})} \right)^{0.5} \quad (7)$$

and V_{JC} is the built-in potential of the junction. The forward-biased base-collector capacitance models are often based on those found in SPICE. The base-emitter, which also consists of two layers is modelled using similar equations to represent the depletion capacitance. Hole storage in the emitter is assumed to be negligible because the heterojunction inhibits the injection of holes into the emitter and the associated capacitance is omitted from the model.

Thermal Equivalent Circuit Models:

Most large-signal transistors (and many small-signal) require thermal models to account for self-heating effects. Returning to the HBT, self-heating generally has a more pronounced effect in GaAs/AlGaAs HBTs than in silicon BJTs because of the lower thermal conductivity of GaAs. Heat dissipation can be largely attributed to a point or line source and has a time constant τ_{TH} in the region of a microsecond. A relatively simple thermal model is shown in Figure 4. The thermal time constant of the device is simulated using the combination $R_{TH}C_{TH}$. The thermal resistance of devices depends on the layout and size of the device as well as mounting and heatsinking arrangements. The thermal resistance of the semiconductor material is itself a function of temperature.

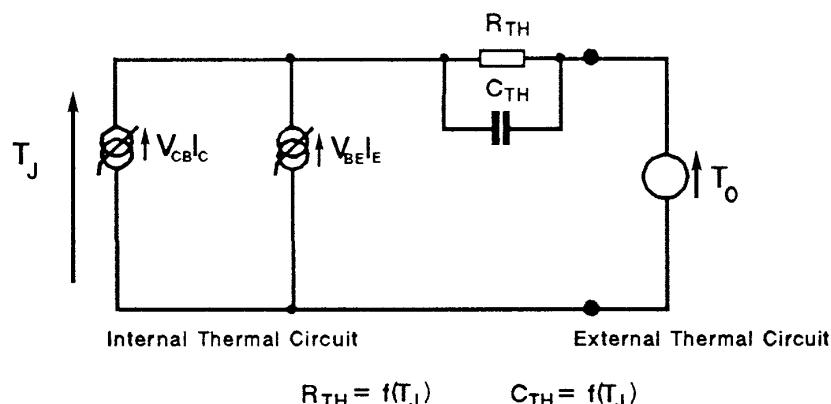


Figure 4. Thermal Model for HBT

The simulated results for a 3×20 micron GaAs/AlGaAs HBT are shown in Figure 5. The simulated S parameters for this device are shown in Figure 6.

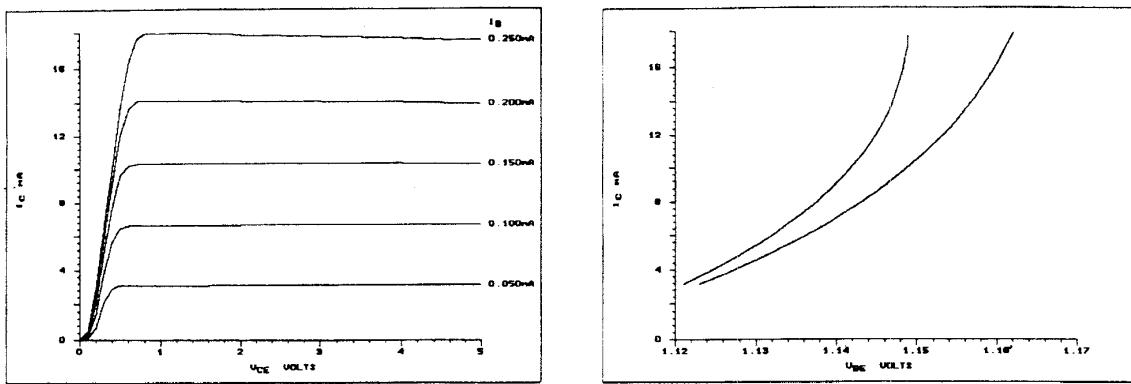


Figure 5 DC characteristics obtained from physics-based equivalent circuit model of a 3×10 micron emitter GaAs/AlGaAs emitter HBT.

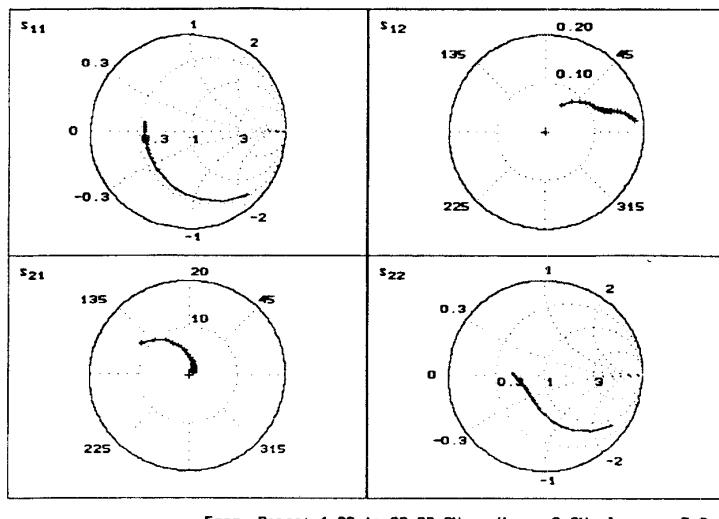


Figure 6 Simulated S parameters for a 3×20 micron emitter GaAs/AlGaAs emitter HBT obtained from physics-based equivalent circuit model .

Physical Models for Microwave Transistors: The interest in using physical models in microwave CAD has been stimulated by the competitive nature of the microwave industry and commercial pressures, requiring cost-effective and high performance designs. Physical semiconductor device models allow the DC, transient and AC characteristics of microwave devices and circuits to be readily extracted. Physical models can be used in association with the same circuit design techniques as with the more familiar equivalent circuit and two-port methods. Time-domain methods are intrinsically compatible with physical models, although the popular harmonic balance can be readily adapted for use with physical models. The influence of thermal effects on the operation of microwave semiconductor devices and circuits can be included in physical models, assisting in the development of thermal management for circuit designs.

Physical models describe the active device in terms of the carrier transport properties and the material and geometrical characteristics, allowing both a physical and electrical description of the device. These types of model are by their nature more complex than equivalent circuit models and normally require numerical methods to obtain solutions to the set of transport equations. They can provide a valuable insight into the operation of semiconductor devices and allows their characteristics to be closely related

to the structure and transport properties. The same model can be used to analyse DC, transient and microwave operation covering both small- and large-signal regimes.

The most commonly used set of carrier transport equations is based on making a series of approximations to the Boltzmann Transport Equation. The most widely used physical models are based on the drift-diffusion approximation. This is a reasonable approximation for devices with relatively large feature sizes, where the carrier transit times far exceed the energy and momentum relaxation times, but is inappropriate for most microwave transistors. In many small-scale devices, such as microwave FETs, the electric field, carrier density gradient and current densities are often very large in magnitude. These high electric fields present lead to substantial carrier heating with the carriers attaining very high energies relative to the equilibrium levels. This results in the carriers experiencing non-equilibrium transport conditions and their velocity may transiently exceed the equilibrium value. In these circumstances it is common for electron velocities to reach values of up to five times the 'steady-state' velocity. A rigorous treatment of the transport in small-scale devices requires the solution of the carrier, momentum and energy conservation equations. The following equations are used to describe hot electron transport for electrons.

The current continuity equation:

$$\frac{\partial n}{\partial t} + \nabla \cdot (nv) = -G \quad (8)$$

The momentum conservation equation:

$$\frac{\partial v}{\partial t} = -\frac{qE}{m^*(w)} - \frac{2}{3nm^*(w)}\nabla(rnw) - \frac{v}{m^*}\nabla(m^*v) + \frac{1}{3n}\nabla(m^*(w)v^2) - \frac{v}{\tau_m(w)} \quad (9)$$

The energy conservation equation:

$$\frac{\partial w}{\partial t} = -qv.E - v.\nabla w - \frac{2}{3n}\nabla\left[\left(nv - \frac{\kappa\nabla}{k}\right)\left(w - \frac{1}{2}m^*(w)v^2\right)\right] - \frac{w - w_0}{\tau_w(w)} \quad (10)$$

The electron energy is given by,

$$w = \frac{1}{2}m^*(w)v^2 + \frac{3}{2}kT_e \quad w_0 = \frac{3}{2}kT_0 \quad (11)$$

where n is the electron density and G is the generation-recombination rate, v is the electron carrier velocity, w is the average electron energy, k is Boltzmann's constant, κ is thermal conductivity of the semiconductor material, T_e is the electron temperature, w_0 is the equilibrium electron energy and T_0 is the lattice temperature. A similar set of equations can be used to describe hole transport. The parameters $m^*(w)$, $\tau_w(w)$, $\tau_m(w)$, are determined from their relationship with the steady-state electric field extracted from Monte Carlo simulations. The non-stationary transport models are available in several degrees of approximation, varying from a full dynamic transport model to a simplified energy-transport model. Although most of the significant factors affecting the carrier dynamics are retained in the simplified models, there are some significant differences in the simulation results between the full transport model and the simplified form [12].

The Poisson equation is used to relate the electric field to the charge,

$$\nabla \cdot (\epsilon_0 \epsilon_r \mathbf{E}) = -q(n - p - N_D^+ + N_A^- - N_T^i) \quad (12)$$

where ϵ_0 is the permittivity of free space, n and p are the electron and hole densities respectively, ϵ_r is the local permittivity of the material, N_D^+ and N_A^- are the ionized donor and acceptor doping densities and N_T^i is the net ionized trap density. The current I is obtained from the electron and hole current densities $J_n = qnv_n$ and $J_p = qpv_p$ respectively, by integrating over a suitable surface surrounding the contact of interest,

$$I = \int_p \left(J_n + J_p + \epsilon_0 \epsilon_r \frac{\partial E}{\partial t} \right) dA \quad (13)$$

In unipolar devices, such as MESFETs, generation-recombination has a negligible role in the normal operating characteristics. However, even in the case of unipolar devices, generation-recombination mechanisms become important in the presence of high electric fields. The onset of breakdown in MESFETs can occur at relatively low bias voltages and in these circumstances a suitable bipolar model which includes generation-recombination is necessary (particularly for large-signal modelling). The generation-recombination rate G has contributions from thermal, impact ionization, Auger, optical and surface generation-recombination processes. Surface recombination is also an important in MESFETs and HBTs. In FETs the differences between steady-state DC and pulsed (fast transient) $I-V$ characteristics and low frequency dispersion associated with g_m and g_d are attributable to the dynamic behaviour of deep level traps in the bulk material and at the surface of GaAs MESFETs [13,14]. The transient behaviour of traps also impacts on the performance of microwave circuits. The 'gate-lag' often seen in transistor power amplifiers operating under pulse conditions is often associated with traps.

The carrier transport processes in semiconductors display a strong temperature dependence which is reflected in the observed terminal current behaviour of devices. Self-heating has a significant impact on parameters such as mobility, generation-recombination and trap occupancy. Furthermore, the non-uniform nature of the temperature distribution contributes to the heat flow in the device, modifying the carrier transport process. This manifests itself in the electrical and microwave characteristics of active devices. An accurate model requires the solution of the heat flow equation which describes the evolution of the temperature distribution within the device,

$$c_L \rho_L \frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa_L \nabla T_L) + H_s \quad (14)$$

where c_L and ρ_L are the specific heat and density of the material, κ_L is the lattice thermal conductivity, H_s is the heat generation and T_L is the lattice temperature. The heat generation is usually obtained by evaluating the scalar product of the electric field E and total conduction current density J ,

$$H_s = \mathbf{J} \cdot \mathbf{E} + qE_g G \quad (15)$$

where E_g is the energy band-gap of the semiconductor and G is the generation-recombination rate. The heat flow equation couples with the carrier transport equations to form a coupled electro-thermal model. The numerical solution of the heat flow equation requires careful consideration to obtain an accurate solution. Ghione et al have suggested that to obtain accurate results for MESFETs, the simulation domain for analysis should be extended horizontally for up to three times the source-drain contact spacing and to a depth of up to ten times the active layer thickness of the device - an area considerably larger than that normally associated with the solution of the transport equations [15].

MESFET's and HEMTs have predominantly two-dimensional electric field and carrier distributions. Two-dimensional simulations have been used extensively to investigate these devices and associated circuits [16,17,18,19,20]. Two-dimensional numerical simulations of HEMTs have been used to characterise their DC and RF properties (for example [21]). Two-dimensional numerical device simulations have demonstrated good accuracy and provide considerable insight into the DC and RF operation of devices (for example [1,16,17]). However, they are still not widely accepted as design tools because of the computer power required to obtain the necessary results.

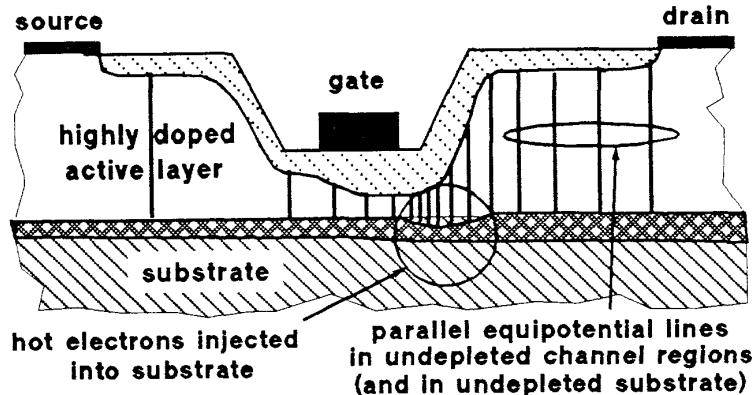


Figure 7. Quasi-two-dimensional FET model

Today, there is an increasing demand for physical models to satisfy industry's demand for advanced design tools aimed at reducing the design time and cost of new devices (the 'right first time' philosophy). The highly efficient quasi-two-dimensional model for FET's provides an attractive alternative to the slower two-dimensional model, overcoming the cpu time constraints of the two-dimensional simulations. Quasi-two-dimensional simulators are ideal for modelling MESFET's [22], dual-gate FET's [23] and HEMTs [24,25]. Careful examination of full two-dimensional simulations reveals that the potential lines are almost parallel in the undepleted active channel and substrate of MESFETs and HEMTs, Figure 7. This implies that the electric field and current flow in these regions is almost one-dimensional. The conducting channel is bounded by surface and gate depletion regions which can vary rapidly in short distances the substrate and active channel interface and must be taken in to account. The semiconductor transport equations are solved in a highly efficient quasi-two-dimensional manner, retaining a two-dimensional description of the active channel, but only requiring a numerical solution of the x -component of the electric field parallel to the surface of the FET.

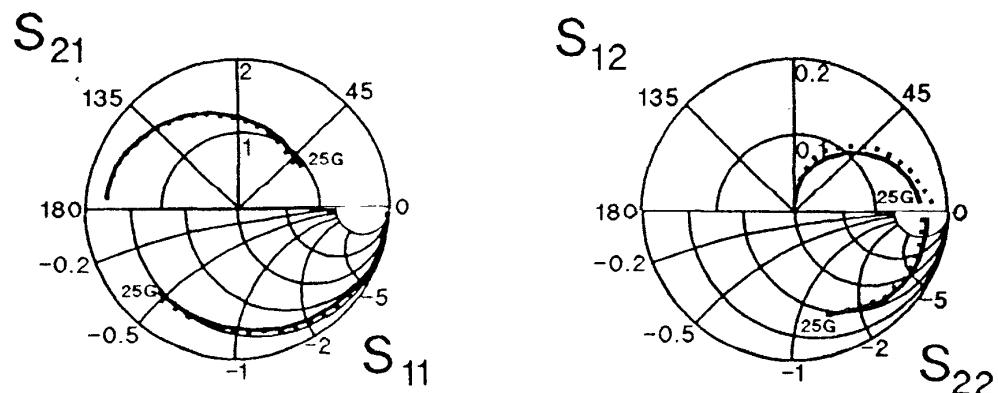


Figure 8. Comparison of microwave S parameters of a 0.5 micron gate length MBE MESFET.

Since the appearance of the first quasi-two-dimensional models (for example [26,27]), the accuracy of these models has been improved by further development of the transport model and better estimation of the two-dimensional channel cross-section [22,23,28,29,30]. Quasi-two-dimensional models have been reported which incorporate hot electron models, charge-control models, heat dissipation, surface and substrate trap representation, breakdown and gate conduction [22,30]. This type of model can be used to predict the operation of devices with parameter spreads and yields prior to fabrication, since the device geometry and material parameters, which play a major role determining spreads and yields, form the basis of the model. This makes the design of new devices systematic and quantitative, minimising uncertainty in the design due to doping profile and fabrication process requirements. The quasi-two-dimensional models provide a relatively rapid solution compared with full two-dimensional models which can be up to 1000 times slower. Microwave S parameters typically require 1 second per frequency for a full CW multi-cycle time-domain and bias-dependent simulation on a typical workstation. Single and two transistor power amplifier circuits have been simulated using a modified harmonic balance scheme, requiring less than 2 seconds per power level below 1dB gain compression (on a typical workstation). Simulated and measured S parameter data for an epitaxial 0.5 micron gate length MESFET is shown in Figure 8. The measured data was obtained using a wafer-prober. The results were obtained directly from the physical model, using the available physical data on the FET, without any additional fitting. Measured and simulated load-pull characteristics for a 0.5 micron gate length power FET, operating at 10 GHz in a Class A amplifier configuration, are shown in Figure 9.

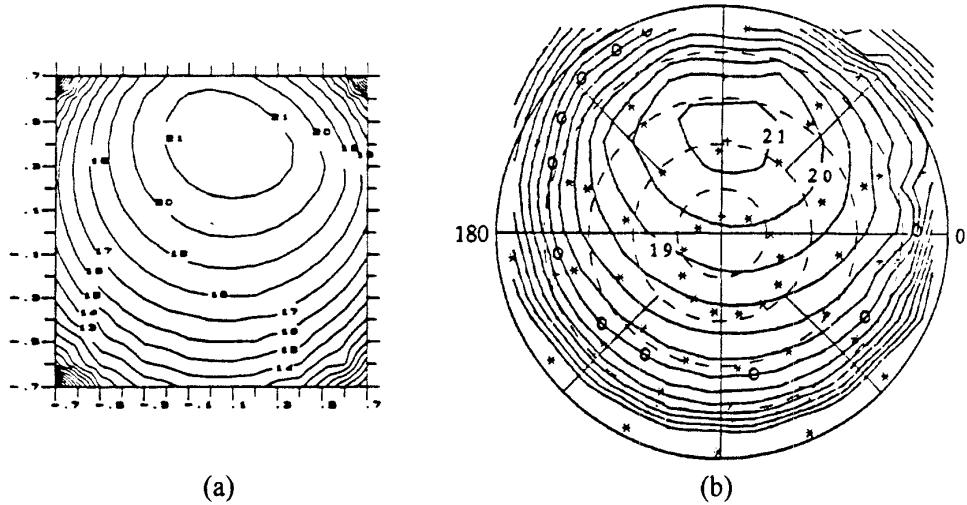


Figure 9 (a) Simulated and (b) measured load-pull characteristics of output power for a 0.5 micron gate length GaAs power MESFET at 1dB gain compression (10 GHz Class A amplifier operation).

The quasi-two-dimensional simulation approach has been successfully extended to modelling AlGaAs/GaAs HEMTs and pseudomorphic HEMTs [24]. Although simplified models are available, a rigorous solution requires the self-consistent solution of the Poisson and Schrödinger equations to obtain a charge control model for the layer structure. This accurately quantifies the sheet electron density attributable to the quantization in the two-dimensional electron gas layer(s) (2DEG) in these transistors. A comparison of measured and simulated transconductance data for a commercial pHEMT device is given in Figure 10.

Physical models can be used in association with established circuit simulators, including time-domain, frequency-domain, harmonic balance and state-variable simulators. The most popular methods utilize time-domain and harmonic-balance techniques. Figure 11 shows the power transfer characteristic of a 38 GHz pHEMT amplifier, simulated using a quasi-two-dimensional model coupled to a highly efficient time-domain simulator [31].

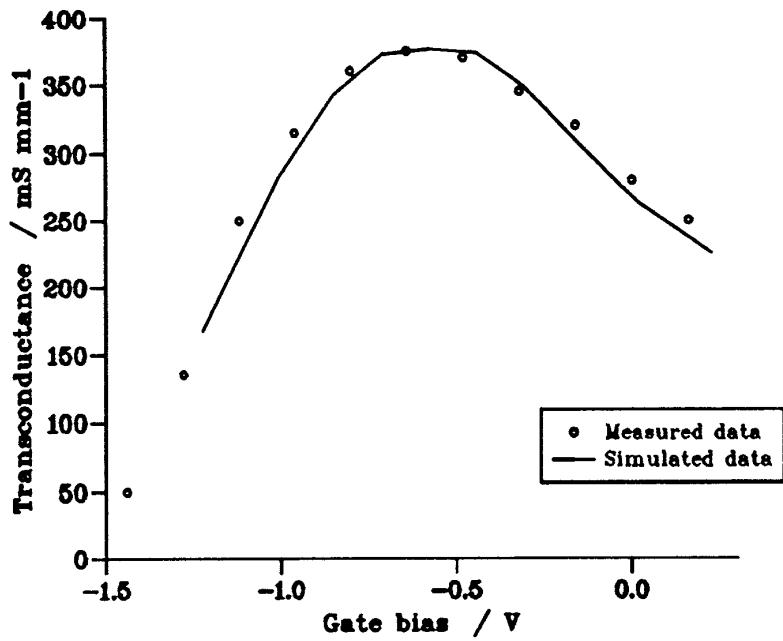


Figure 10. Comparison of simulated and measured transconductance for a commercial pHEMT.

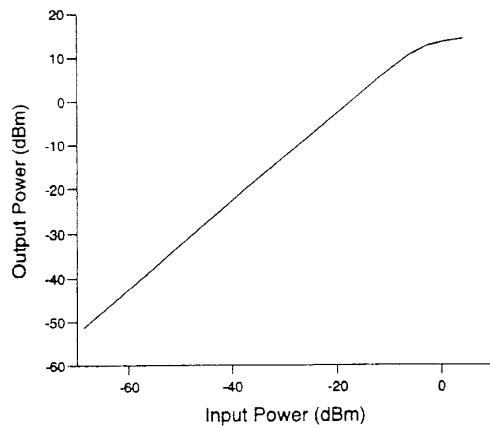


Figure 11 Simulated power transfer characteristic of a 38 GHz pHEMT amplifier obtained using a physical model.

Conclusions: The challenge of modelling the non-linear operation of microwave and millimeter-wave transistors has been met by the development of large-signal models which can now provide a high degree of accuracy. The advent of more powerful computers has increased the interest in using physical models and physics-based models for CAD. The increasing economic pressures to reduce the cost and time required for design cycles can be partly satisfied using predictive physical models to supplement traditional equivalent circuit methods.

References:

- [1] G. Ghione, C.U. Naldi and F. Filicori, "Physical Modeling of GaAs MESFET's in an Integrated CAD Environment: From Device Technology to Microwave Circuit Performance", IEEE Trans. MTT, MTT-37, pp.457-468, March 1989
- [2] G. Dambrine, A. Cappy, F. Heliodore and E. Playez, "A New Method of Determining the FET Small-Signal Equivalent Circuit", IEEE Trans. MTT, Vol. MTT-36, pp.1151-1159, July 1988
- [3] P.C. Grossman and J. Choma Jr., "Large-signal modeling of HBT's Including Self-Heating and Transit Time Effects", IEEE Trans. Microwave Theory and Techniques, Vol. 40, No.3, pp.449-464, March 1992
- [4] P.H. Ladbrooke, *MMIC Design: GaAs FETs and HEMTs*, Artech House 1989
- [5] H. Gummel and H.Poon, "An Integral Charge Control Model of Bipolar Transistors", Bell Sys. Tech. Jnl., Vol. 49, pp.827-852, May 1970.
- [6] J.J. Ebers and J.L. Moll, "Large-Signal Behaviour of Junction Transistors", Proc. IRE, Vol. 42, pp.1761-1772, 1954
- [7] G. Stringfellow, "Effect of surface treatment on recombination velocity and diode leakage current in GaP", J. Vac. Sci. Tech., Vol. 13, No.4, pp.908-913, July-August 1978
- [8] C. Sandroff, R. Nottenburg, J. Bischoff and R. Bhat, "Dramatic enhancement in the gain of GaAs/AlGaAs heterostructure bipolar transistors by surface chemical passivation", Appl. Phys. Lett., Vol. 51, No.1, pp.33-35, July 6, 1987
- [9] M.E. Hafizi, C.R. Crowell and M. Grupen, "The DC Characteristics of GaAs/AlGaAs Heterojunction Bipolar Transistors with Application to Device Modelling", IEEE Trans. Electron Devices, Vol. 37, No.10, pp.2121-2129, 1990
- [10] P.C. Grossman and A. Oki, "A Large-Signal DC Model for GaAs/Ga_{1-x}Al_xAs heterojunction Bipolar Transistors", Bipolar Circuits and Technology Meeting, pp.258-262, September, 1989
- [11] S. Tiwari, *Compound Semiconductor Device Physics*, 1993
- [12] Y. Feng and A. Hintz, "Simulation of Submicrometer GaAs MESFET's Using a Full Dynamic Transport Model", IEEE Trans. Electron Devices, ED-35, pp.1419-1431, September 1988
- [13] K. Horio, H. Yanai and T. Ikoma, "Numerical Simulation of GaAs MESFET's on the Semi-insulating Substrate Compensated by Deep Traps", IEEE Trans. Electron Devices, ED-35, pp.1778-1785, November 1988
- [14] T.M. Barton and C.M. Snowden, "Two-Dimensional Numerical Simulation of Trapping Phenomena in the Substrate of GaAs MESFETs", IEEE Trans. Electron Devices, June 1990
- [15] G.Ghione, P. Golzio P. and C. Naldi, "Self-consistent thermal modelling of GaAs MESFETs: a comparative analysis of power device mountings", Alta Frequenza, Vol. LVII, 7:311-319, 1988
- [16] C.M. Snowden, M.J. Howes and D.V. Morgan, "Large-Signal Modeling of GaAs MESFET Operation", IEEE Trans. Electron Devices, Vol. ED-30, pp.1817-1824, December 1983
- [17] C.M. Snowden, "Computer-Aided Design of MMICs based on Physical Device Models", IEE Proceedings, Vol. 133, Pt. H, No.5, pp. 419-427, October 1986
- [18] C.M. Snowden and D. Loret, "Two-Dimensional Hot Electron Models for Short Gate Length GaAs MESFETs", IEEE Trans. Electron Devices, ED-34, pp.212-223, 1987
- [19] F. Heliodore, M. Lefebvre, G. Salmer and O. El-Sayed, "Two-Dimensional Simulation of Submicrometer GaAs MESFET's: Surface Effects and Optimisation of Recessed Gate Structures", IEEE Trans. Electron Devices, ED-35, pp.824-830, July 1988
- [20] Y. Wada and M. Tomizawa, "Drain Avalanche Breakdown in Gallium Arsenide MESFET's", IEEE Trans. Electron Devices, ED-35, pp.1765-1770, November 1988
- [21] T. Shawki, G. Salmer and O. El-Sayed, "MODFET 2-D Hydrodynamic Energy Modeling: Optimisation of Subquarter-Micron Gate Structures", IEEE Trans. Electron Devices, ED-37, pp.21-30, January 1990
- [22] C.M. Snowden and R.R. Pantoja, "Quasi-Two-Dimensional MESFET Simulations for CAD", IEEE Trans. Electron Devices, ED-36, pp.1564-1574, September 1989
- [23] C. Licurish, M.J. Howes and C.M. Snowden, "A New Model for the Dual-Gate GaAs MESFET", IEEE Trans. MTT, MTT-37, pp.1497-1505, October 1989
- [24] R. Veresegyhazy, R. and C.M. Snowden, "Highly efficient simulation of HEMTs and MESFETs based on quantum mechanics", Proc. Int. Workshop on Computational Electronics, Leeds, 96-100, 1993
- [25] Happy et al "HELENA: A Friendly Software for Calculating the DC, AC and Noise Performance of HEMTs", International Jour. of Microwave and Millimeter-Wave Computer-Aided Engineering, Vol. 3, No.1 pp. 14-28, January 1993
- [26] B. Carnez, A. Cappy, A. Kaszynski, E. Constant and G.Salmer, "Modelling of a Submicrometer Gate Field-effect Transistor Including Effects of Nonstationary Electron Dynamics", J. Appl. Phys., 51, pp.784-790, January 1980
- [27] R.K. Cook, and J. Frey, J., "An efficient technique for two-dimensional simulation of velocity overshoot in Si and GaAs devices", COMPEL, 1, 2:65-87, 1982
- [28] P.A. Sandborn, J.R. East and G.I. Haddad, "Quasi-Two-Dimensional Modeling of GaAs MESFET's", IEEE Trans. Electron Devices, ED-34, pp.985-991, May 1987
- [29] R.B. Darling, "Generalized Gradual Channel Modeling of Field-Effect Transistors", IEEE Trans. Electron Devices, ED-35, pp.2302-2314, December 1988
- [30] C.M. Snowden and R.R. Pantoja, "GaAs MESFET physical models for process-oriented design", IEEE Trans. MTT-40:1401-1409, 1992
- [31] R. Singh and C.M. Snowden, "Large-signal modelling of millimetre-wave HEMTs", Proc. European Microwave Conference, Cannes, 1994