Accurate Small-Signal Modeling of HFET's for Millimeter-Wave Applications

Niklas Rorsman, Mikael Garcia, *Student Member, IEEE,* Christer Karlsson, *Student Member, IEEE,* and Herbert Zirath, *Member, IEEE*

Abstract— **In this paper we discuss the small-signal modeling of HFET's at millimeter-wave frequencies. A new and iterative method is used to extract the parasitic components. This method allows calculation of a π-network to model the heterojunction field-effect transitor (HFET) pads, thus extending the validity of the model to higher frequencies. Formulas are derived to translate this π-network into a transmission line. A new and general cold field-effect transitor (FET) equivalent circuit, including a Schottky series resistance, is used to extract the parasitic resistances and inductances. Finally, a new and compact set of analytical equations for calculation of the intrinsic parameters is presented. The real part of Y_{12} is accounted for in these equations and its modeling is discussed. The accounting of $\mathrm{Re}(Y_{12})$ improves the S-parameter modeling. Model parameters are extracted for an InAlAs/InGaAs/InP HFET from measured S-parameters up to 50 GHz, and the validity of the model is evaluated by comparison with measured data at 75–110 GHz.**

I. Introduction

THE small-signal equivalent circuit of an heterojunction field-effect transitor (HFET) is used in the design of high-speed circuits and characterization of fabrication processes. The small-signal circuit also helps in understanding device physics. Fast and accurate parameter extraction for HFET modeling is hence needed to design, develop, and produce high-yield, low-cost, high-performance monolithic circuits.

The small-signal circuit parameters are extracted either by optimizing the component values to closely fit the measured S-parameters, by using analytical expressions [1]–[3], or by using the frequency independence of the intrinsic components (calculated from analytical expressions) and, through iteration, determining the parasitics [4], [5]. The optimizing method results in a set of component values that depend on the starting values and method of optimization. The most favored direct extraction method was originally presented by Dambrine *et al.* [1] and later modified by Berroth and Bosch [2]. The method uses pinched ($V_{\mathrm{gs}} < V_{\mathrm{po}}$) cold FET ($V_{\mathrm{ds}} = 0$ V) measurements to obtain the parasitic capacitances. Cold FET measurements with a forward-biased gate are used to extract the parasitic inductances and resistances of the device. The intrinsic circuit components are then analytically determined from S-parameters measured under active bias conditions. An alternative method to extract the parasitics was presented by Tayrani *et al.* [4], where the gate is not forward biased to eliminate any gate degradation caused by large gate currents.

In this paper, the HFET's pads are modeled with a π-configured LC-network to extend the validity of the modeling. This network requires a new iterative extraction method for the parasitic resistances and inductances. A Schottky gate series resistances is added to further improve the cold FET modeling. Formulas to translate the π-network to a transmission line are derived. Finally, we investigate the influence of the real part of Y_{12} on the modeling of an active HFET and discuss how to model it. New, exact, and compact equations for calculation of the intrinsic parameters are presented.

We demonstrate the parameter extraction for a lattice-matched InAlAs/InGaAs/InP HFET. S-parameters measured on-wafer up to 50 GHz are used to extract the equivalent circuit parameters. The response of the equivalent circuit is compared with W-band (75–110 GHz) measurements.

II. Device Fabrication and Measurements

HFET's were fabricated on a lattice-matched InAlAs/InGaAs/InP material. The material structure is as follows (from bottom to top): a 500-nm $In_{0.52}Al_{0.48}As$ buffer, a 20-nm $In_{0.53}Ga_{0.47}As$ channel, a 4-nm $In_{0.52}Al_{0.48}As$ spacer, Si-∂-doping ($4 \cdot 10^{12}$ cm^{-2}), a 20-nm $In_{0.52}Al_{0.48}As$ Schottky layer, and a 5-nm $In_{0.53}Ga_{0.47}As$ cap layer. Standard photolithography methods were used to define the mesa and ohmic contact patterns. A phosphoric acid-based etch was used for mesa etching and Au/Ge/Ni ohmic contact metallization was electron beam evaporated. The contacts were then annealed with rapid thermal annealing and the resulting ohmic contact resistivity is 0.15 Ω·mm. Mushroom gates were defined with electron beam lithography and a selective etch was used for recessing. Au/Pt/Ti was evaporated for gate metallization and the resulting gate length is 0.15 μm. A thick metal layer was evaporated on the contacts and finally the HFET's were passivated with a polyimide.

The extrinsic dc transconductance is 400 mS/mm and the saturated drain to source current is 350 mA/mm. The extrapolated maximum frequency of oscillation, $f_{\max}$, is 300 GHz and the transit frequency, f_T, is 110 GHz for a 100-μm device.

III. Models and Equivalent Circuits

A. Determination of FET Extrinsic Components

The modeling of the pads becomes important at millimeterwave frequencies, since the pad models influences the extraction of the intrinsic components. An LC network in an

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L- or a π-configuration is a good model for the pads at low frequencies. Compared to a transmission line, the L- and π-net for our pads are valid up to 17 and 50 GHz, respectively, with an error of 5% in the S-parameter magnitudes. The validity of the model may be extended to higher frequencies by replacing the lumped networks with a loss-less transmission line. The Maclaurin series expansion of the *ABCD* (cascade) matrices of a lossless transmission line and a π-network can be used to determine the equivalent length and characteristic impedance

$$ABCD_{\text{transmission line}} = \begin{bmatrix} 1 - \frac{\omega^2 l^2}{2c^2} & jZ_0\frac{\omega l}{c} \\ \frac{j\omega l}{Z_0 c} & 1 - \frac{\omega^2 l^2}{2c^2} \end{bmatrix} + O(\omega^3) \tag{1}$$

$$ABCD_{\pi-\text{net}} = \begin{bmatrix} 1 - \frac{\omega^2 LC}{2} & j\omega L \\ j\omega C\left(1 - \frac{\omega^2 LC}{4}\right) & 1 - \frac{\omega^2 LC}{2} \end{bmatrix} \tag{2}$$

where c is the speed of light, l is the length of the transmission line, and Z_0 is the characteristic impedance. When L and C have been extracted from cold FET measurements, the equivalent length and characteristic impedance of the pad can be calculated from $l = c\sqrt{LC}$ and $Z_0 = \sqrt{L/C}$.

The total drain-source capacitance for a pinched cold FET is composed of two parts: the pad capacitance, C_{pd}, and the capacitance due to the electrode between the two gate fingers, C_{ds} (Fig. 1). In [1], [2], and [4] the drain-source capacitance is neglected (or assumed to a certain value). C_{ds} is, however, not a negligible part of the total drain-source capacitance for millimeter-wave HFET's, and it is not directly extractable from S-parameters. Neglecting C_{ds} (or assuming an incorrect value) at the extraction of C_{pd} will introduce errors in the following extraction of the intrinsic components. This error may not be apparent, since an error in C_{pd} may be compensated by an incorrect C_{ds} of the active HFET. The error becomes apparent if the gate width dependence of C_{ds} is investigated. Our transistor layout was designed to have almost identical drain and gate pads (Fig. 1), but this is generally not the case. The pad associated capacitances, C_{pd} and C_{pg}, can therefore not generally be set equal. We measured S-parameters for cold FET and pinched HFET's with different gate widths (20–200 μm). Extrapolation of the total drain capacitance to zero gate width gives the drain pad capacitance. Using this method, a drain pad capacitance of 15.5 fF was calculated, which agrees well with the gate pad capacitance of 15.2 fF. The parasitic gate to drain capacitance, C_{pgd} (Fig. 2), has earlier been determined for this HFET layout [5] and was accounted for.

For the extraction of the parasitic resistances and inductances we follow the basic principle in [1] and [4]. We have used the equivalent circuit in Fig. 2 to describe the FET at $V_{\text{ds}} = 0$ V, including both a gate-capacitance, C_g, and a Schottky barrier resistance, R_{dy}. In most other methods either C_g [1] or R_{dy} [4] is assumed to be negligible, making the models valid only at certain gate biases. Using this equivalent circuit we can determine the HFET parasitic components in a wider gate voltage range compared to other methods. Furthermore, we propose that the total gate series resistance is composed of two parts: one part proportional to the gate width,

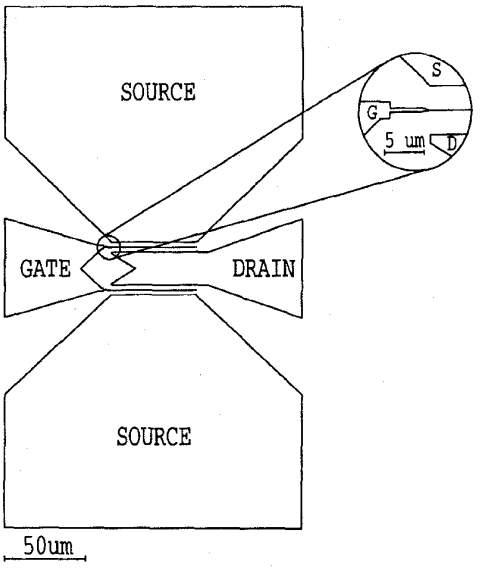


Fig. 1. Layout of the HFET.

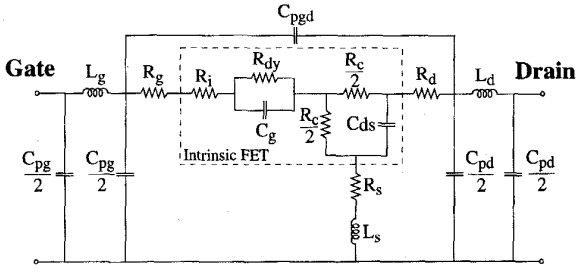


Fig. 2. Equivalent circuit of an HFET at $V_{\text{ds}} = 0$ V.

R_g and one part (Schottky contact series resistance) inversely proportional to the gate width R_i. R_i is often the dominant part of the total gate series resistance for short gate widths and R_g will hence be overestimated if R_i is not taken into account.

For a cold FET with a forward-biased gate for full channel conditions, C_{ds} can be neglected, since its impedance usually is large compared to R_c at this bias. If the parasitic capacitances and inductances have been subtracted, C_{ds} is neglected and the gate length is so short that it can be assumed to be a point contact, the Z-parameters for a cold FET (Fig. 2) are

$$Z_{11} = R_g + R_i + \frac{R_{\text{dy}}}{1 + j\omega C_g R_{\text{dy}}} + \frac{R_c}{2} + R_s + j\omega(L_s + \Delta L_g) \tag{3}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + j\omega L_s \tag{4}$$

$$Z_{22} = R_d + R_s + R_c + j\omega(L_s + \Delta L_d). \tag{5}$$

R_g is provided from a dc end-to-end resistance measurement and R_c from the sheet resistivity of the material. We use an iterative extraction method, since π-nets are used to describe the pads. The pad inductances, L_g and L_d, are positioned inside a π-net and cannot be easily calculated as in [1] and [2]. ΔL_g and ΔL_d are correction inductances that are used to account for the error in the subtracted L_g and L_d. The

TABLE I
VALUES OF L_g, R_i, C_g, R_{dy}, R_d, L_d, R_s, AND L_s AFTER EACH ITERATION FOR A 100-μm HFET

Iteration	L_g [pH]	R_i [Ω]	C_g [fF]	R_{dy} [Ω]	R_d [Ω]	L_d [pH]	R_s [Ω]	L_s [pH]
1	34.8	5.6	93.1	249	6.55	25.3	5.58	1.76
2	25.5	5.7	94.7	251	6.83	25.0	5.59	1.79
3	25.8	5.8	95.6	250	6.83	25.1	5.58	1.78
4	25.6	5.8	95.6	250	6.83	25.1	5.58	1.78
5	25.6	5.8	95.6	250	6.83	25.1	5.58	1.78
6	25.6	5.8	95.7	250	6.83	25.1	5.58	1.78

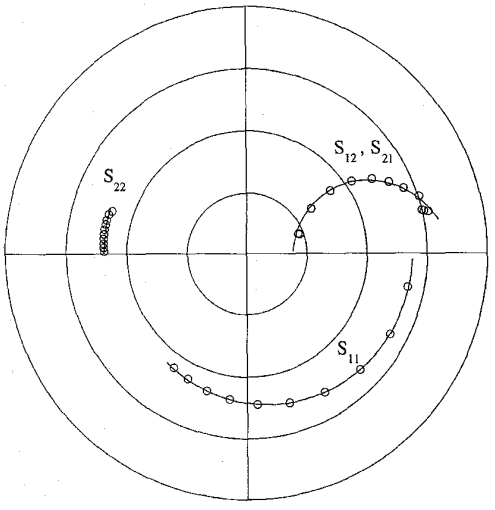


Fig. 3. Measured (o) and modeled (—) S-parameters of a cold FET (100 μm) with forward-biased gate for full channel conditions. The radius for S_{21} and S_{12} is 0.5.

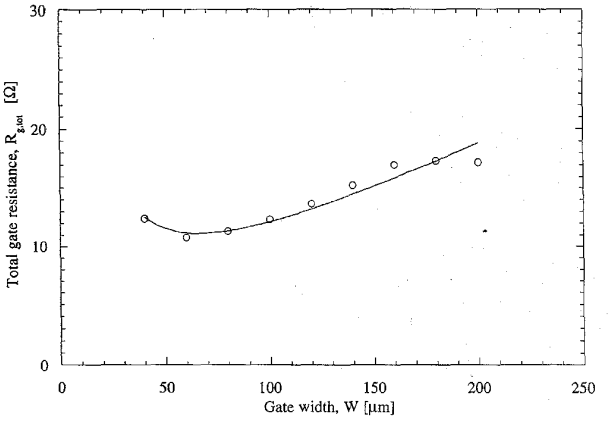


Fig. 4. Total gate resistance versus gate width.

iteration process is as follows. First, the pad capacitances and inductances are subtracted. In the first iteration the parasitic inductances, L_g and L_d, are unknown and set equal to zero. Starting values for C_g and R_{dy} are calculated at low frequencies. Equations (3)–(5) are then used to calculate the parasitics R_i, R_d, R_s, ΔL_g, ΔL_d, and L_s, where R_i is extracted from Z_{11} at high frequencies. The calculated ΔL_g and ΔL_d are added to L_g and L_d, respectively. R_{dy} and C_g are then calculated again to account for the new parasitic components. This iteration process is continued (four–six iterations) until the parasitics do not change (Table I). This extraction method does not ignore pad capacitances, since their effect cannot be neglected for a cold FET with a forward-biased gate [6].

We performed this extraction for HFET's with gate widths in the range 20–200 μm. This method of extracting the parasitic components works well for longer gate widths and excellent agreement with measured S-parameters is achieved (Fig. 3). For short gate widths, the parameter extraction is not that accurate in the determination of R_i, L_g, and R_{dy}, due to high impedance on the gate terminal.

L_d and L_g exhibit a gate width dependence, demonstrating that the inductances are composed of one part due to the pad and one part due to the extension of the gate or the drain electrode. C_g and R_{dy} scale proportional and inversely proportional, respectively, with gate width. The total gate series resistance (Fig. 4) may be expressed as

$$R_{g,\,\mathrm{tot}} = \frac{\rho_i}{W} + \rho_g \cdot W \tag{6}$$

where ρ_i and ρ_g are the Schottky and gate resistivities and W is the gate width. The extracted $R_{g,\,\mathrm{tot}}$ values were fitted to this model giving $\rho_i = 0.37$ Ω·mm and $\rho_g = 85$ Ω/mm. The ρ_g is close to the resistivity provided from the dc end-to-end measurement.

B. Gate Voltage Dependence of Intrinsic Cold FET Components

Cold FET modeling of HFET's, which operates at $V_{ds} = 0$ V as in [7] and [8], is of interest for resistive HFET mixer applications. The performance of this mixer type depends on the $C_g[V_{gs}]$, $R_c[V_{gs}]$ and $C_{ds}[V_{gs}]$ characteristics. The gate

TABLE II
INTRINSIC COMPONENT VALUES OF AN ACTIVE HFET (100 μm) NEGLECTING AND INCLUDING $\mathrm{Re}(Y_{12})$. THE PARASITIC COMPONENTS ARE: $R_g = 7.2\ \Omega$, $L_g = 25.6$ pH, $C_{\mathrm{pg}} = C_{\mathrm{pd}} = 12.8$ fF, $R_d = 6.8\ \Omega$, $L_d = 25.1$ pH, $R_s = 5.6\ \Omega$, $L_s = 1.8$ pH

	C_{gs} [fF]	C_{gd} [fF]	C_{ds} [fF]	g_m [mS]	g_d [mS]	R_i [Ω]	R_j [Ω]	τ [ps]
$\mathrm{Re}(Y_{12})$ negl.	82	2.8	19	63	2.0	9.8	-	0.49
$\mathrm{Re}(Y_{12})$ incl.	81	3.0	19	64	1.8	9.4	250	0.53

voltage dependence of these characteristics is studied using a gate symmetric equivalent circuit (Fig. 2). In the normal operation voltage range (no gate current) R_{dy} is very large and can be neglected. Furthermore, C_{ds} becomes negligible when there is a relatively small number of electrons in the channel. The Z-parameters for the intrinsic circuit are

$$Z_{11} = R_i + \frac{1}{j\omega C_g} + \frac{2R_c + j\omega C_{\mathrm{ds}} R_c^2}{4(1 + j\omega C_{\mathrm{ds}} R_c)} \tag{7}$$

$$Z_{12} = Z_{21} = \frac{R_c}{2(1 + j\omega C_{\mathrm{ds}} R_c)} \tag{8}$$

$$Z_{22} = \frac{R_c}{1 + j\omega C_{\mathrm{ds}} R_c}. \tag{9}$$

Fig. 5 shows $C_g[V_{\mathrm{gs}}]$, $R_c[V_{\mathrm{gs}}]$ and $C_{\mathrm{ds}}[V_{\mathrm{gs}}]$ for a 100-μm HFET extracted using (7)–(9). Curve fit functions describing $C_g[V_{\mathrm{gs}}]$, $R_c[V_{\mathrm{gs}}]$ and $C_{\mathrm{ds}}[V_{\mathrm{gs}}]$ can be used in harmonic balance simulations. Since C_{ds} becomes negligible and hence hard to extract at certain voltages, it may be set to a constant value in the simulations.

C. Modeling of Active FET's

The Y matrix of the intrinsic equivalent circuit of an active HFET (Fig. 6) is given by

$$Y_{\mathrm{Intrinsic}} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_{\mathrm{gs}} + Y_{\mathrm{gd}} & -Y_{\mathrm{gd}} \\ -Y_{\mathrm{gd}} - \frac{\mathrm{Im}(Y_{\mathrm{gs}})}{Y_{\mathrm{gs}}^*} \cdot g_m e^{j(\frac{\pi}{2} - \omega\tau)} & Y_{\mathrm{ds}} + Y_{\mathrm{gd}} \end{bmatrix} \tag{10}$$

where Y_{gd}, Y_{gs} and Y_{ds} represent the gate-drain, gate-source, and drain-source admittances, respectively. Usually $\mathrm{Re}(Y_{12})$ is neglected, but we have accounted for the nonzero $\mathrm{Re}(Y_{12})$ by introducing a gate-drain series resistance R_j. The exact solution of the equivalent circuit parameters from the Y-parameters is

$$R_j = -\mathrm{Re}\left(\frac{1}{Y_{12}}\right) \tag{11}$$

$$C_{\mathrm{gd}} = \frac{1}{\omega\ \mathrm{Im}\left(\frac{1}{Y_{12}}\right)} \tag{12}$$

$$R_i = \mathrm{Re}\left(\frac{1}{Y_{11} + Y_{12}}\right) \tag{13}$$

$$C_{\mathrm{gs}} = -\frac{1}{\omega \mathrm{Im}\left(\frac{1}{Y_{11} + Y_{12}}\right)} \tag{14}$$

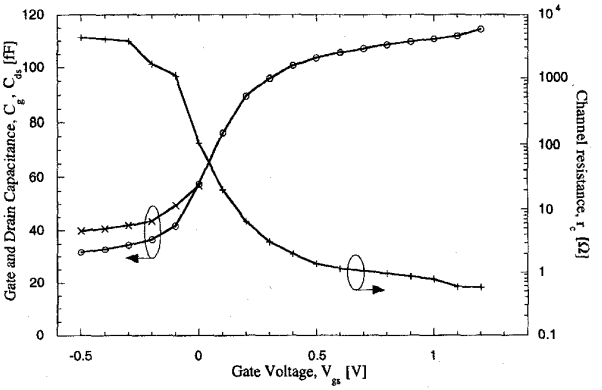


Fig. 5. Gate (o) and drain (×) capacitance and channel resistance (+) versus gate voltage at $V_{\mathrm{ds}} = 0$ V for a 100-μm HFET.

$$R_{\mathrm{ds}} = \frac{1}{\mathrm{Re}(Y_{12} + Y_{22})} \tag{15}$$

$$C_{\mathrm{ds}} = \frac{\mathrm{Im}(Y_{12} + Y_{22})}{\omega} \tag{16}$$

$$g_m = \left| \frac{(Y_{12} - Y_{21})(Y_{11} + Y_{12})}{\mathrm{Im}(Y_{11} + Y_{12})} \right| \tag{17}$$

$$\tau = \frac{\frac{\pi}{2} - \mathrm{phase}(Y_{12} - Y_{21}) + \mathrm{phase}(Y_{11} + Y_{12})}{\omega}. \tag{18}$$

Using these equations, the correspondence between measured and modeled S-parameters is improved for frequencies up to 110 GHz (Fig. 7). This is also transformed into a better estimation of maximum stable gain (MSG), maximum available gain (MAG), current gain (h_{21}), and stability factor (k) (Fig. 8). The k-factor is under-estimated if $\mathrm{Re}(Y_{12})$ is neglected, resulting in an overestimation of the gain. Table II shows the equivalent circuit parameters both when $\mathrm{Re}(Y_{12})$ is accounted for and when it is neglected. The fit of S_{12} is improved up to 50 GHz, but the improvement at higher frequencies is not that substantial. The inclusion of R_j is not sufficient to model S_{12} correctly at the W-band. R_j exhibits a frequency dependence, indicating that it is not the correct model. R_j is, however, an appropriate model in a narrow frequency range. S_{12} may be better modeled if the distributed nature of the device or a dipole capacitance [9] are included. The worse fit of S_{21} at low frequencies is a device saturation effect due to high input power.

IV. DISCUSSION AND CONCLUSION

The modeled S-parameters have good correspondence with on-wafer, W-band S-parameter measurements, showing the

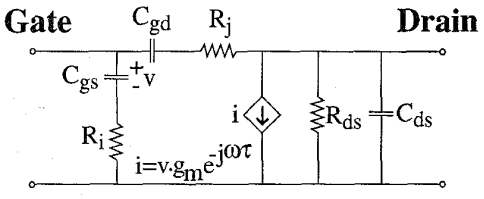
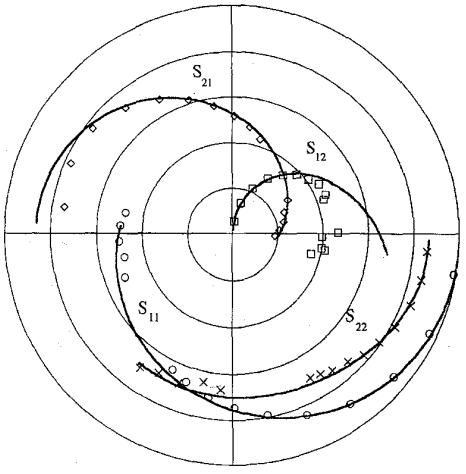
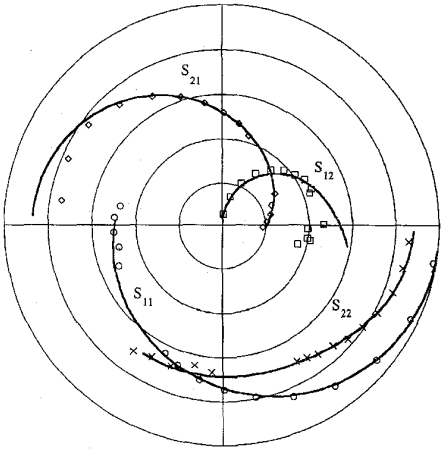


Fig. 6. The intrinsic equivalent circuit of an active HFET.



(a)



(b)

Fig. 7. Measured (dots) and modeled (—) S-parameters (0.5–50 GHz and 75–110 GHz) for an active HFET (100 μm) without $R_j(a)$ and with $R_j(b)$. The equivalent circuit parameters are taken from Table II. The radii for S_{21} and S_{12} are 5 and 0.2, respectively.

validity of the model at higher frequencies. The small-signal equivalent circuit presented in this work has been used in the design of a monolithic integrated amplifier and a resistive mixer at 119 GHz.

The distributed nature of the HFET should be considered for a more accurate high-frequency modeling. Especially for HFET's with large gate widths, this effect may be important.

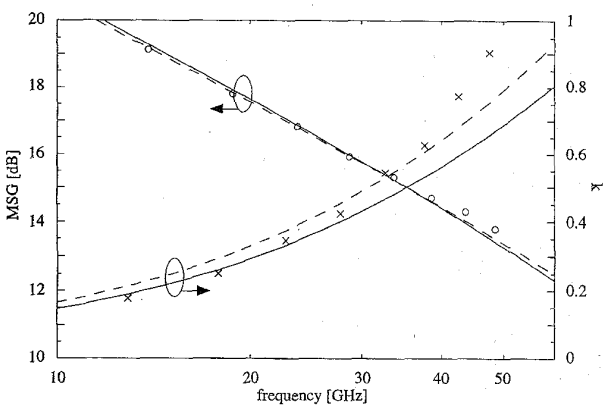


Fig. 8. Measured ($\circ$, $\times$) and modeled (—) MSG, and k-factor for a 100-μm InAlAs/InGaAs/InP HFET without R_j (—) and with R_j (– – –).

A method for modeling the distributed nature of FET's has been developed by LaRue *et al.* [10].

In conclusion, we have studied the modeling of the HFET pads, extraction of the parasitic components, and the influence of a nonzero $\mathrm{Re}(Y_{12})$ for an active HFET. The pads are modeled with a π-configured LC-network, and formulas were derived to translate this network into a transmission line. The parasitic components are extracted from a new and general cold FET equivalent circuit, which is also used to study the gate voltage dependence of the cold FET intrinsic components. A new iterative extraction method for the parasitic inductances and resistances was described. Finally, new, exact, and compact equations for the intrinsic parameters, where $\mathrm{Re}(Y_{12})$ is accounted for, were presented. These equations result in a better modeling of the S-parameters.

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Since 1980, he has been working as a Researcher at Chalmers on cooled millimeter-wave Schottky diode mixers and on the properties of millimeter-wave Schottky barrier diodes. Since 1986 he has been responsible for the development of active millimeter-wave devices and MMIC's, such as InP- and GaAs-based MESFET's and HFET's, including their modeling, and related circuits such as active and resistive mixers, low-noise amplifiers, and harmonic generators for frequencies up to 120 GHz. He became an Associate Professor at the Department of Microwave Technology at Chalmers in 1992 and, since 1995, has been employed part-time by Ericsson Microwave Systems.