SPICE Modeling of Microwave and RF Control Diodes

Robert H. Caverly, Nikolai V. Drozdovski, Lioudmila M. Drozdovskaia and Michael J. Quinn
Department of Electrical and Computer Engineering
Villanova University
800 Lancaster Avenue
Villanova, PA 19085

***Abstract* - A SPICE model for the microwave and RF PIN switching diode is presented. The model simulates the important I-region charge storage phenomenon and its effect on the PIN diode impedance-frequency characteristic. The SPICE model is described and validated by comparisons with numerical, analytical and measured results.**

I. Introduction

PIN diodes are used in a wide variety of commercial and defense applications, including antenna switching and attenuator applications. Microwave and RF design engineers frequently use time domain simulators such as SPICE for computer-aided design of microwave circuits and systems. While simple resistance-only models are currently used by design engineers [1,2], these models are not able to adequately model such important effects as I-region charge storage, which is the dominant mechanism in governing such PIN diode behavior as the impedance-frequency characteristic or the current-dependent carrier lifetime. Presented in this paper is a time domain simulation model for the PIN diode. This model includes both junction effects (making it suitable for dc bias simulation) as well as low and high frequency I-region charge storage and current-dependent lifetime effects. The model provides RF and microwave design engineers with the ability to use SPICE and other CAD tools to perform full time domain simulation of PIN diodes and ancillary circuitry in such applications as microwave and RF switches, attenuators and other control applications. Verification of the new model is made by comparing numerical, analytic and measured results.

Contact Information
Electronic Mail: r.caverly@ieee.org
Phone: (610) 519-5660
FAX: (610) 519-4436

II. Theoretical Discussion

The PIN diode is characterized by a lightly doped so-called intrinsic (or I-) region sandwiched between a heavily doped p-type and n-type region. For time domain modeling in SPICE simulators, the PI and IN junctions are characterized by the default SPICE PN junction diode circuit elements. Modeling the I-region is more problematic since this region exhibits charge storage phenomenon which is manifested in the charge-current (or Q-I) relationship. It is the I-region charge storage effect that governs such PIN diode behavior as the impedance-frequency characteristic, insertion loss and limiter action.

The charge storage phenomenon in PIN diodes is described by the ambipolar carrier transport equation:

$$\frac{\partial^2 n(x,t)}{dx^2} = \frac{n(x,t)}{D_a \tau} + \frac{1}{D_a}\frac{\partial n(x,t)}{dt} \qquad (1)$$

where the carrier lifetime τ is a function of n(x,t). The time domain model for Eqn. 1 must couple with time domain models of the junctions described earlier. From Eqn. 1, a relationship between the stored charge in the I-region and the current flowing through the diode can be written as

$$I(s) = Q(s)\frac{L_a\sqrt{1+s\tau}}{x_m \tau}\tanh\left(\frac{x_m}{L_a}\sqrt{1+s\tau}\right) \qquad (2)$$

where the minimum of the I-region stored charge density, x_m, is given by

$$x_m = \frac{W}{2}\left[1+\frac{2\lambda}{W}\tanh^{-1}\left(\frac{b-1}{b+1}\tanh(\frac{W}{2\lambda})\right)\right],$$

b is the electron to hole mobility ratio, W is the I-region thickness, $\lambda = L_a/\sqrt{1+s\tau}$, and the other symbols have their usual meanings. The term x_m reduces to W/2 for equal hole and electron

Proc. 43rd IEEE Midwest Symp. on Circuits and Systems, Lansing MI, Aug 8-11, 2000
0-7803-6475-9/00/$10.00 ©IEEE 2000

mobilities, an assumption that has been shown to have a minor effect on the results [4].

Eqn. 2 can be transformed to a form usable in SPICE by noting that if the stored charge Q(s) excites a circuit, then the response will be the current I(s). A SPICE equivalent circuit can be generated by using a Pade approximation on Eqn. 2. The excitation Q(s) is derived from the current flowing through the PN junction diodes. Fig. 1 shows the equivalent circuit for the I-region stored charge taken out to fifth order. Higher order approximations to Eqn. 2 can be used to improve simulation accuracy.

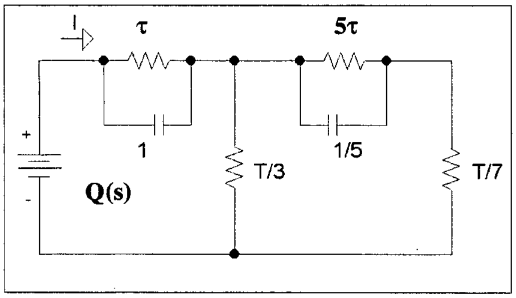

Fig. 1. SPICE equivalent circuit for I-region charge storage of the PIN diode.

In Fig. 1, the symbol τ is the ambipolar carrier lifetime and T equals x_m^2/D_a . Complete details of the model and the interaction between the I-region stored charge and the PN junctions can be found in the sample SPICE sub-circuit file shown in Appendix A. Other parameters used in the model are the parasitic bond wire inductance, limiting resistance values R_{min} (minimum resistance at high current) and R_{max} (zero bias resistance), current-dependent lifetime knee current, and intrinsic and package parasitic capacitances.

III. APPLICATION AND RESULTS

A collection of results of various device parameters that are widely observed by design engineers follows. Simulations using a commercial version of SPICE as well as a full one dimensional semiconductor device simulator [5] were used to compare the SPICE model described with analytical models [6-8]. Fig. 2 shows the resistive and reactive impedance components of a PIN diode using the proposed SPICE model (solid line) plotted with

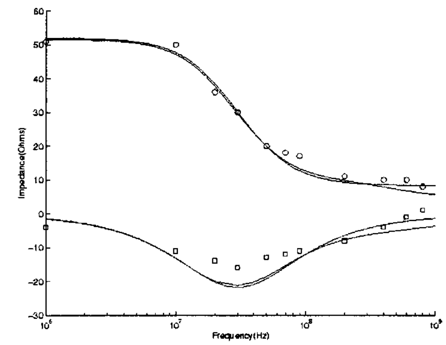

Fig. 2. Comparison of the SPICE and analytical models for a gallium arsenide PIN diode.

the analytical results (circles/crosses) for a gallium arsenide device with a 3 μm I-region width and 5.6 nanoseconds carrier lifetime at 1 mA dc bias current. The agreement between the SPICE and analytical models for both devices is very good, validating the model compared with analytical results. The gallium arsenide device was chosen for this illustration since it has a greater difference between the hole and electron mobilities. Plotted with the SPICE and analytical results are the corresponding experimental data, providing an additional level of confidence for using this proposed SPICE model for simulating the impedance-frequency response of the PIN diode.

The carrier lifetime is known to decrease with increasing DC forward bias. This decreasing lifetime makes the resistance of the device deviate from its ideal $1/I_{DC}$ behavior. Fig. 3 shows results of SPICE simulations and corresponding measured data on carrier lifetime showing the agreement between the model and experiment. In the figure, the low current carrier lifetime is 57 microseconds and the knee current I_{Knee} is 10 mA. The carrier lifetime was measured using the minimum reactance technique [9].

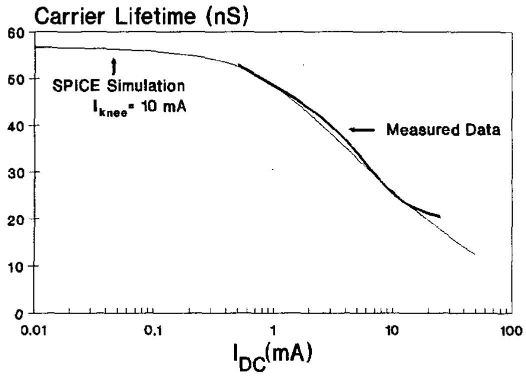

Fig. 3. Carrier lifetime measurements and SPICE simulation. The results show the current dependent lifetime. The measured data is indicated by the bold line.

Figs. 4 and 5 show comparisons of one-dimensional numerical simulations using the program ISTOK-1 [5], SPICE and measured data from several sources on the diode series resistance R_S versus DC bias current at 100 MHz. Note the excellent agreement between all the data and models over the current range, indicating that the proposed SPICE model adequately describes the PIN diode at high frequencies and at a range of bias currents.

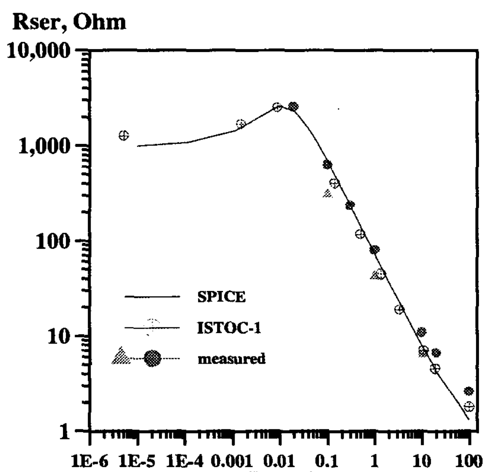

Fig. 4. Comparison of SPICE, numerical and measured PIN diode resistance data from different sources versus Dc forward current in a 175 micron I-region PIN diode.

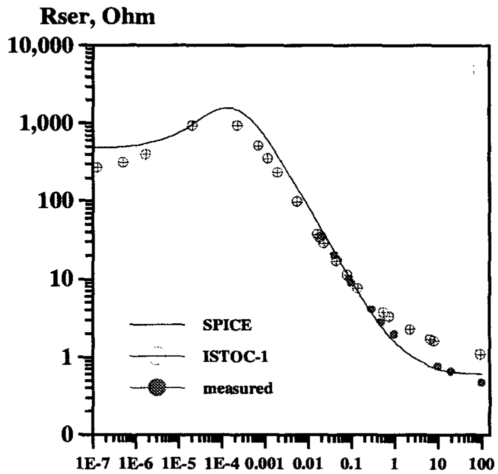

Fig. 5. Comparison of SPICE, numerical and measured PIN diode resistance data from different sources versus DC forward current. An 8 micron I-region PIN diode is used.

IV. Conclusions

A method has been presented for modeling the impedance-frequency characteristic in PIN diodes. Using this model, microwave and RF engineers designing with PIN diodes can use readily available circuit simulators such as SPICE to study the impedance-frequency effects in circuits and systems more easily. The SPICE model has been validated against both analytical models and experimental measurements.

V. Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. CCR-9805718

VI. References

1. APLAC v. 7.10e, Helsinki Univ. Tech, Oct, 1997.
2. HP-LIBRA, System IV, 1997.
3. J. Walston, "Spice Circuit yields recipe for PIN diode", *Microwaves and RF*, pp. 78-89, Nov. 1992.
4. A. Strollo, "A New SPICE Model of Power P-I-N Diode based on Asymptotic Waveform Evaluation", *IEEE Trans. Power Elec.*, vol. 12(1), pp. 12-20, Jan. 1997.
5. A. S. Shnitnikov and N.I. Filatov, "Microwave limiter diode performance analyzed by mathematical modeling", *Solid-State Electronics*, vol. 34, no. 1, pp. 91-97, 1991.

6. R. Caverly and G. Hiller, "The Small Signal ac Impedance of Gallium Arsenide and Silicon PIN Diodes," *Solid-State Electronics*, vol. 33(10), Oct., 1990.
7. R. Caverly and G. Hiller, "The Frequency Dependent Impedance of p-i-n Diodes", *IEEE Trans. Microwave Theory and Tech.,* vol. 37(4), pp. 787-790, April, 1989.
8. I.V. Lebedev, L. M. Drozdovskaya, N. V. Drozdovski, A. S. Shnitnikov, "Determination of the active component of pin-diode impedance", *Radiotekhnika i Elektronika,* vol. 41(3), pp. 370-373, Mar., 1996.
9. R. Caverly, "RF technique for determining the ambipolar carrier lifetime in PIN RF switching diodes", *Electronics Letters*, vol. 34(23), pp. 2277-2278, Dec., 1998.

VII. APPENDIX A

```
.subckt pin 9 20 params: is=1e-10,
+        n=1, ikf=3, phi=.7, ie=6, iknee=0.01
+        rlim=1.8m, repi=800k, cj=0.1pf,
+        tau=57n, w=6u, lbond=0.1nh, cpack=0.1pf
+        b=3

.param to={w*w/.001935/4}
.param vm={w*w/tau/0.1}
.param alfa={to/tau}
.param npi={2*n/(1+b)}
.param nin={2*b*n/(1+b)}

cpack 9 20 {cpack}
lbond 9 10 {lbond}
cjunc 10 20 {cj}
repi 10 12 {repi}
rlim 10 11 {rlim}
grmod 11 12 value={2*(v(11,12)*v(2,3)/vm)}
gpin 12 20 value={i(vs2)}
rpin 10 20 1e12
ej 30 0 value={v(12,20)}
vs1 30 31 0

* two different junction models
dpi 31 32 dj1
din 32 0 dj2
.model dj1 d (is={is},ikf={ikf},n={npi})
.model dj2 d (is={is},ikf={ikf},n={nin})
e1 1 0 value={i(vs1)}
vs2 1 2 0

* ge describes the current-dependent tau
ge 2 0 value={(v(2)*v(2))/iknee}

* 8th order approximation for base region
rp1 2 3 1
cp1 2 3 {tau}
rs1 3 0 {alfa/3}
rp2 3 4 5
cp2 3 4 {tau/5}
rs3 4 0 {alfa/7}
rp4 4 5 9
cp4 4 5 {tau/9}
rs5 5 0 {alfa/11}
rp6 5 6 13
cp6 5 6 {tau/13}
rs6 6 0 {alfa/15}
rp7 6 7 17
cp7 6 7 {tau/17}
rs7 7 0 {alfa/19}

.ends
```