Monolithic High Power 300 Watt, S-Band, HMIC PIN Diode Limiter

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***Abstract* — A monolithic multi-stage high power silicon/HMIC PIN diode limiter that covers the full range of UHF to S-Band frequencies has been designed that is capable of handling up to 300 watts CW of incident RF power. This monolithic MMIC limiter approach has been enabled by recent improvements to MACOM's state-of-the-art HMIC PIN diode technology. This MMIC design will be able to produce superior RF performance and power handling when compared to present hybrid assembled limiters that are based upon chip and wire integration of discrete PIN diodes but having a dramatic reduction the overall footprint and a significant reduction in device cost.**

***Index Terms* — RF/microwave/mmW limiters, high power limiters, HMIC, PIN diode limiters, PIN diodes.**

I. Introduction

Limiters are employed to protect the low power low noise amplifier that is found at the receiver input of every communication and radar transmit/receive (T/R) module. This limiter will restrict the power that reaches the LNA to safe levels to prevent the destruction of the receive chain from inadvertent RF signals.

The simplest PIN diode limiter consists of a single PIN diode in a shunt configuration from the input line to ground with a RF choke to provide a DC return, as shown in Figure 1. In this construction the low level limiting, the flat band leakage, and the power handling/limiting are determined by the thickness of the PIN diode which is employed as the active component in the limiter. [1] [2]

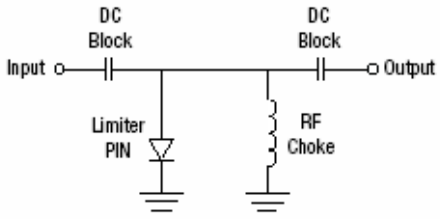

Fig. 1 Typical Single Stage Shunt PIN Diode Limiter Circuit

In this circuit design the received signal passes from input to output over the anode terminal of the single PIN diode which is in shunt to ground. As the signal transitions from input to output, a portion of the RF energy is rectified and provides a DC bias to turn on the shunt PIN diode and initiate the limiting function by shunting power to ground. In a typical single stage limiter as shown, the low level turn-on is controlled by the thickness of the "I" region of the PIN diode. For low flat leakage and rapid initiation of the limiting function, a thin "I" region is desired. However, to be able to handle high incident power levels, provide good isolation, and enable a low input capacitance to be achieved, a thick "I" region thickness is required, which always leads to a compromise solution for a single stage limiter.

For higher incident power levels, a multistage limiter, shown schematically in Figure 2 as a two stage limiter circuit, is employed. In this case, the two PIN diodes that are employed remain in shunt with the input/output transmission line and are separated by a λ/4 section, which can be either a transmission line segment or a lumped element equivalent transformation to provide the requisite RF electrical short between the two diodes.

As can be seen in Figure 2, in order to achieve low level turn-on and high power limiting, this circuit construction requires a thin "I" region PIN diode to be individually optimized for low level tum on and flat leakage and a thick "I" region PIN diode for low capacitance, good isolation, and high incident power levels.

At present, this multi-thickness "I" region requirement can only be realized as a hybrid assembly. More specifically, high power multi-stage limiters are formed by chip and wire assembly of discrete PIN diodes onto a printed circuit board, incorporated into laminate packaging, or combined utilizing multi-chip module construction. This hybrid construction approach is not limited to two stage solutions, and is able to employ as many additional limiting stages as necessary to support higher incident power handling, with the only additional constraint of the λ/2 spacing between the limiting stages.

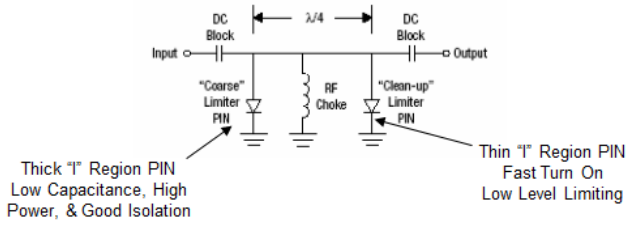

Fig. 2 Typical Multi-Stage Shunt PIN Diode Limiter Circuit

Using these hybrid assembly techniques and discrete PIN diodes, a number of high power limiters have been developed by MACOM and are offered in several surface mount package outlines. These multi-stage limiters cover the frequency spectrum from 20 MHz to 8.0 GHz in narrow and multi-octave bandwidth configurations. In terms of power handling, CW power as high as 300 watts and peak pulsed power of 1000

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watts, at an elevated case temperature of 85ºC, have been achieved, using more complicated, decoupled schottky diode current source design techniques.

While it can be observed that state-of-the-art limiter performance is able to be realized by use of discrete silicon PIN diodes and hybrid assembly techniques, this methodology has the drawback of a relatively large package footprint. In addition, the use of chip and wire/multi-module assembly techniques introduces parasitic inductances and capacitances which will limit the upper end of the frequency response.

II. Discussion

The answer to maintaining or perhaps improving the high power handling and frequency bandwidth that has been achieved by the discrete PIN diode hybrid construction is to move to an integrated MMIC approach. A fully monolithic MMIC will eliminate virtually all of the parasitic bond wires, greatly improve control of inductive interconnects between limiter stages, enable a more precise realization of the λ/4 transmission line coupling sections, and can minimize parasitic inter-stage capacitances. The only physical limitation to realizing a monolithic MMIC in a multi-stage silicon PIN diode high power limiter is the requirement for multiple "I" regions in each limiter stage. As discussed above in the hybrid discrete assembly limiter construction, this use of multiple PIN diode "I" region thicknesses obtained by individual discrete PIN diodes enabled the optimization of both the low level turn-on and flat leakage and low active capacitance, good isolation, and high incident power levels.

While several attempts at solutions to realize, both physically and electrical performance, of this multiple "I" region, hybrid constructed limiter in a monolithic format, most notably the technique described in US Patent Number 7,868,428, "PIN diode with improved power limiting", which describes the combined lateral/vertical formation of multiple thickness "I" regions on a single wafer by the use of photolithographic processes[3], have been tried, none have been able to achieve a MMIC limiter that produces acceptable RF results.

HMIC, which is an acronym for *Heterolithic Microwave Integrated Circuit*, is a unique, patented technology developed by MACOM to enable RF, microwave, and mmW monolithic circuit structures and solutions that reduce both size and cost, and is a fundamental advancement in microwave component design. This technology joins two different materials, glass and silicon, into ONE structure at a wafer level with the ability to manufacture integrated solutions at a rate of thousands at a time.

HMIC is able to construct true 3-D, RF and mechanical structures having a low loss, conductive ground plane with minimum parasitic capacitances, resulting in high Q/low loss capacitors, inductors, and transmission lines for use in high frequency integrated circuits. This technology has continually improved process and electrical component capabilities since its inception over two decades ago. HMIC has produced and continues to generate state-of-the-art silicon PIN and Schottky surface mount diodes, integrated high power PIN diode switches, single function Schottky diode mixers, PIN diode VVA s, and single stage PIN diode limiters.

Recent concepts to improve the monolithic integration capabilities of the HMIC PIN diode process, which are protected by a number of provisional patent filings [4] [5] [6], are being implemented for high power limiters and switches. Utilizing these new concepts, a monolithic three stage limiter covering S-Band operation with the ability to handle 300 watts of CW and 1.0 kilowatt peak RF incident power is being designed. A schematic of this three stage limiter is shown in Figure 3.

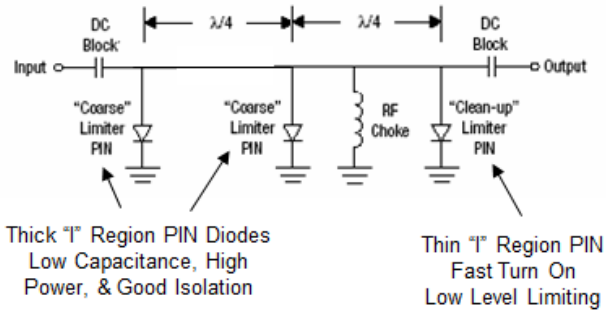

Fig. 3 Three Stage Shunt PIN Diode Limiter Circuit

These new PIN diode concepts, shown in Figure 4, will enable multiple vertical "I" regions to be employed in shunt diode configurations embedded into a single HMIC die to produce monolithic solutions that permits multistage limiters

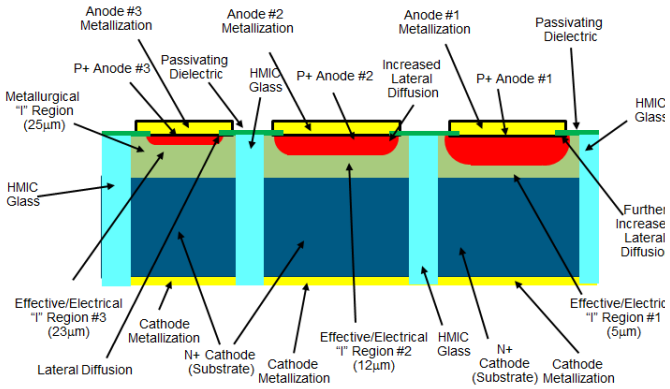

Fig. 4 Monolithic HMIC Shunt PIN Diode Construction Having Multiple "I" Regions

having the requisite "I" region thickness enabling optimization of the limiter turn-on, flat leakage, as well as the second and third limiter stages for isolation and power handling.

These multiple "I" regions are achieved by sequential anode photolithography, ion implantation, and solid state diffusion to produce different effective electrical "I" region thicknesses

from a single metallurgical "I" layer growth. The PIN diode capacitance is managed by dimensional control of the anode photolithography scaling and compensation for lateral P-type diffusion, as is shown in Figure 4.

An alternate approach to achieve multiple "I" regions in a shunt configured structure on a single HMIC die to again produce monolithic solutions is shown in Figure 5. These multiple "I" regions are again achieved by sequential anode photolithography, ion implantation, and solid state diffusion to produce different effective electrical "I" region thicknesses from a single metallurgical "I" layer growth. However, in this case, the HMIC glass not only provides diode-to-diode DC and RF isolation within the monolithic die but also is employed to control the diode capacitance independently of the lateral P-type diffusion. This unique topology provides limiter products with enhanced low and high signal parametric repeatability at a lower cost than comparable chip and wire hybrid designs.

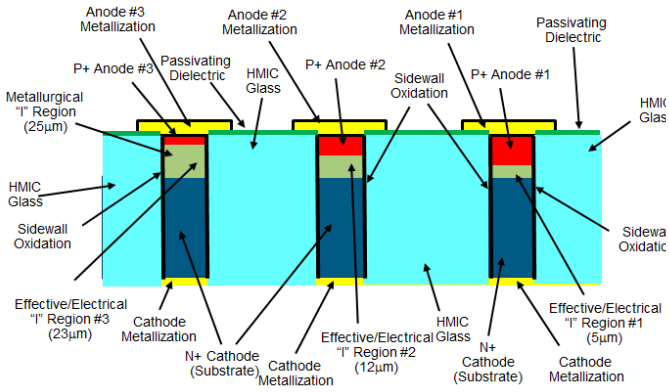

Fig. 5 Monolithic HMIC Shunt PIN Diode Construction Having Multiple "I" Regions and Using HMIC Glass to Control Diode Capacitance

III. Performance/Design

As a starting reference point in the design of a high power, S-Band, monolithic PIN diode limiter, the production performance of a commercially available, hybrid assembled S-Band, high power, multi stage PIN diode limiter is summarized in Table I below. It can be seen that over the frequency range of 2.0 GHz to 4.0 GHz, an average CW incident power of 40.0 watts could be limited to a maximum spike leakage power to the receiver of 200 millewatts and a flat leakage power of 100 millewatts by this multi-stage discrete PIN diode limiter. When operated under pulsed conditions of 50.0 µsec pulse width (PW) and a 4% duty factor (DF) into a source VSWR of 1.2:1 and a load VSWR of 1.2:1, 1.0 kilowatt of peak incident RF energy could be reduced to these same spike and flat leakage powers into the receiver. It can also be observed in Table I that this production hybrid limiter had a very good low incident power level thru insertion loss of 1.3 dB, a P_{-1dB} of +10 dBm and an input I_{IP3} of +23 dBm.

TABLE I
Performance Summary of Commercial S-Band Multi-Stage Hybrid PIN Diode Limiter

Frequency Range (GHz)	Parameter/Feature	Absolute Max
2.0 - 4.0	Insertion Loss (dB)	1.3
	VSWR	1.6:1
	Average Power (W)	40
	Peak Power (W)	1000
	Recovery Time (nS)	1000
	Spike Leakage Power (mW)	200
	Leakage Power (mW)	100
	P_{-1dB} (dBm)	+10
	I_{IP3} (dBm)	+23
	Operating Temperature	-55°C to +85°C
	Storage Temperature	-65°C to +125°C

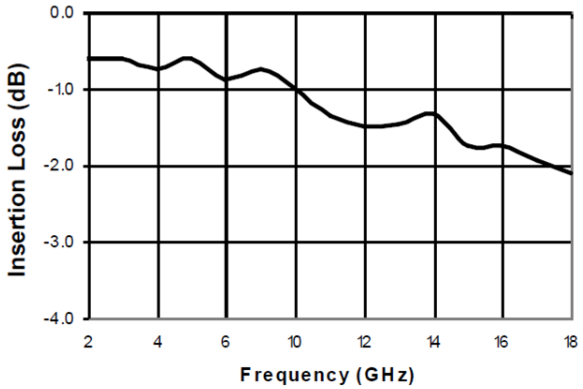

Fig.6 Insertion Loss vs Frequency for Hybrid Assembled Discrete PIN Diode Limiter

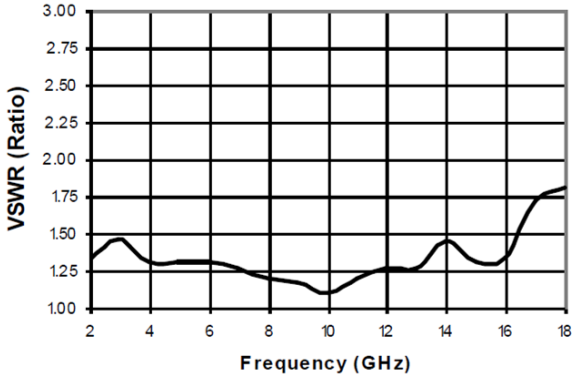

Fig.7 VSWR vs Frequency for Hybrid Assembled Discrete PIN Diode Limiter

More detailed characteristics for critical limiter parameters can be seen in Figure 6, Figure 7, and Figure 8. Figure 6 is a plot of insertion loss as a function of frequency for the multi-

stage production hybrid PIN diode limiter. It can be seen that the insertion loss is certainly less than 1.0 dB from 2.0 GHz through 10 GHz which includes all S-Band and C-Band frequencies.

Figure 7 is a graph of VSWR versus frequency for the multi-stage production hybrid PIN diode limiter that is summarized in Table I. It can be seen from this plot that the VSWR is less than 1.5:1 from 2.0 GHz through 16 GHz and more typically approximately 1.3:1 over this same range of frequencies. This not only covers all S-Band, C-Band, and X-Band frequencies but also includes the major part of Ku-Band.

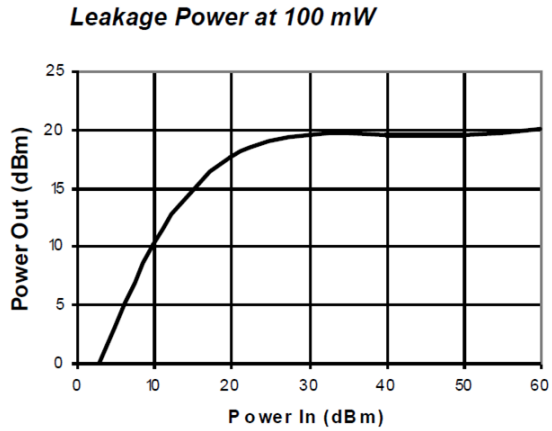

Fig.8 100mW (Output Power) Flat Leakage Power versus Pulsed Incident Power for Hybrid Assembled Discrete PIN Diode Limiters

Lastly, a plot of the output flat leakage power as a function of the incident power presented to the input of the production hybrid PIN diode limiter is shown in Figure 8. It can be observed that all incident power levels up to 60.0 dBm, (1000 watts), peak power result in a maximum flat leakage power of 20.0 dBm, (100 millewatts), at the output port of the limiter.

Using the above production, hybrid assembled S-Band, high power, multi stage PIN diode limiter as a guide, the design of a monolithic MMIC, high power 300 watt, S-Band, HMIC PIN diode limiter began with a choice of a specific limiter topology, explicit, modeled shunt configured HMIC PIN diodes, and commercially available, EM software combined with MACOM

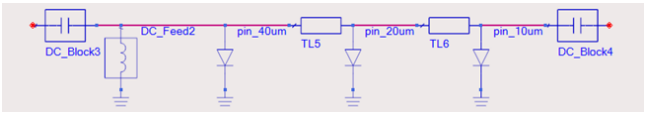

Fig.9 ADS EM Simulation Schematic of a Three Stage monolithic HMIC PIN Diode Limiter

developed custom high frequency, modeling techniques. [7] As shown in Figure 9, a three stage limiter design was chosen to be able to provide the necessary low incident power level turn-on and the requisite high level incident power handling. This three stage limiter topology was chosen in conjunction with a first stage, relatively thick 40 µm "I" region HMIC shunt PIN diode, having a to meet the high power handling requirement, and combined with 20 µm and 10 µm "I" region thickness HMIC shunt PIN diodes for the second and third limiter stages respectively. Simulations of the key limiter parameters are presented in the following figures.

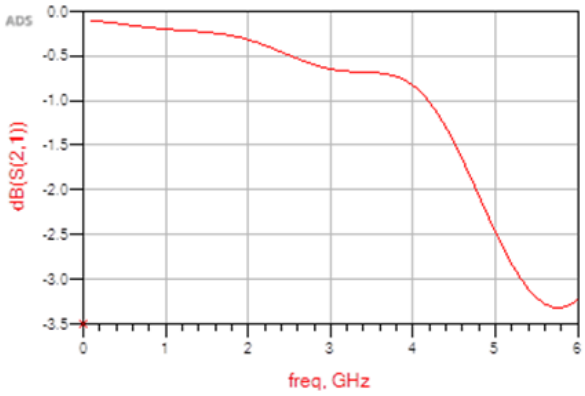

Fig.10 Simulated Insertion Loss vs Frequency for the Monolithic High Power PIN Diode Limiter MMIC

In Figure 10, a plot of the simulated insertion loss versus frequency for the monolithic S-Band high power PIN diode limiter MMIC. It can be seen that over the 2.0 GHz to 4.0 GHz frequencies of interest, the low level thru insertion loss behaves very well and is less than 0.8 dB, which simulates comparable insertion loss performance to the production discrete chip and wire limiter approaches through S band, and with the advantage of reduced circuit size and cost

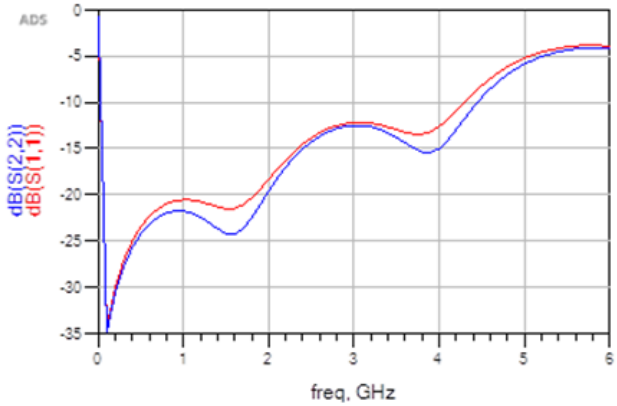

Fig.11 Simulated Return Loss vs Frequency for the Monolithic High Power PIN Diode Limiter MMIC

Figure 11 is a simulation of the return loss as a function of frequency for the monolithic S-Band high power PIN diode limiter that is under examination. Again the simulated results are very good with a return loss better than -15dB from 100 MHz to 4.0 GHz.

The key parameter of flat leakage power being passed on to the receiver port as a function of incident CW power was simulated for the monolithic MMIC high power PIN diode limiter and is presented in Figure 12. In this simulation plot,

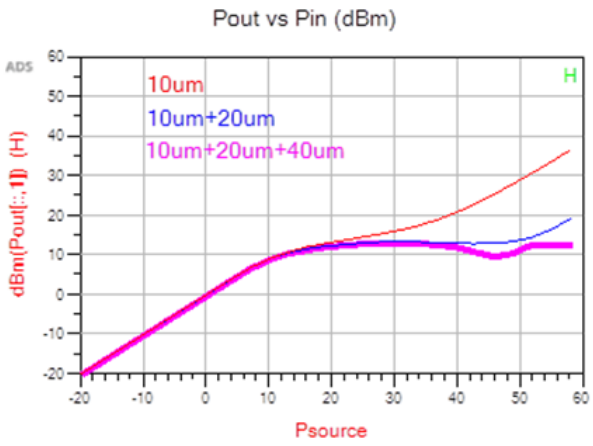

Fig.12 Simulated Flat Leakage Power vs Incident CW Power for the Monolithic High Power PIN Diode Limiter MMIC

the limiting effect of single, double and three stage limiters having HMIC PIN diodes with "I" region thicknesses respectively of 10 µm, 10 µm + 20 µm, and 10 µm + 20 µm + 40 µm is shown. It is clear from these simulated flat leakage curves that a three stage solution is required to achieve a maximum power leakage to the receiver of less than 20 dBm, 100 millewatts, up through an incident CW power to the MMIC limiter of greater than 55 dBm, 316 watts.

Lastly, in Figure 13, a similar simulation for the turn-on/spike leakage power being passed on to the receiver port as a function of incident CW power was performed for the monolithic MMIC high power PIN diode limiter. Again the same simulation methodology examining the limiting effect of single, double

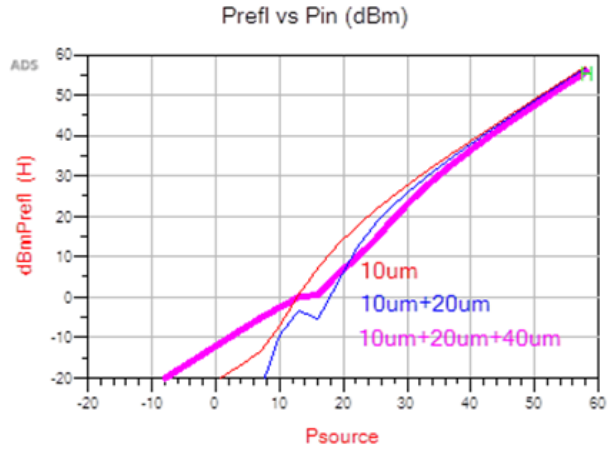

Fig.13 Simulated Turn-on/Spike Leakage vs Incident CW Power for the Monolithic High Power PIN Diode Limiter MMIC

and three stage limiters having HMIC PIN diodes with "I" region thickness respectively of 10 µm, 10 µm + 20 µm, and 10 µm + 20 µm + 40 µm on spike leakage power was followed. In Figure 13, it can be seen that the low level spike leakage overshoot can be improved by almost 20 dB by the use of three stage limiter.

IV. Conclusion

The above paper describes technology development and circuit design efforts to utilize new capabilities in the HMIC MMIC platform that enables shunt configured PIN diodes with multiple "I" region thicknesses to be employed to produce monolithic, MMIC configured high power multi-stage RF, microwave, and mmW limiters. It is expected that these new families of limiters will be able to meet expected future size, cost, reliability, and manufacturing improvements necessary for future commercial and military requirements.

Acknowledgement

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