Configuration Diagnostic Tool v1.0

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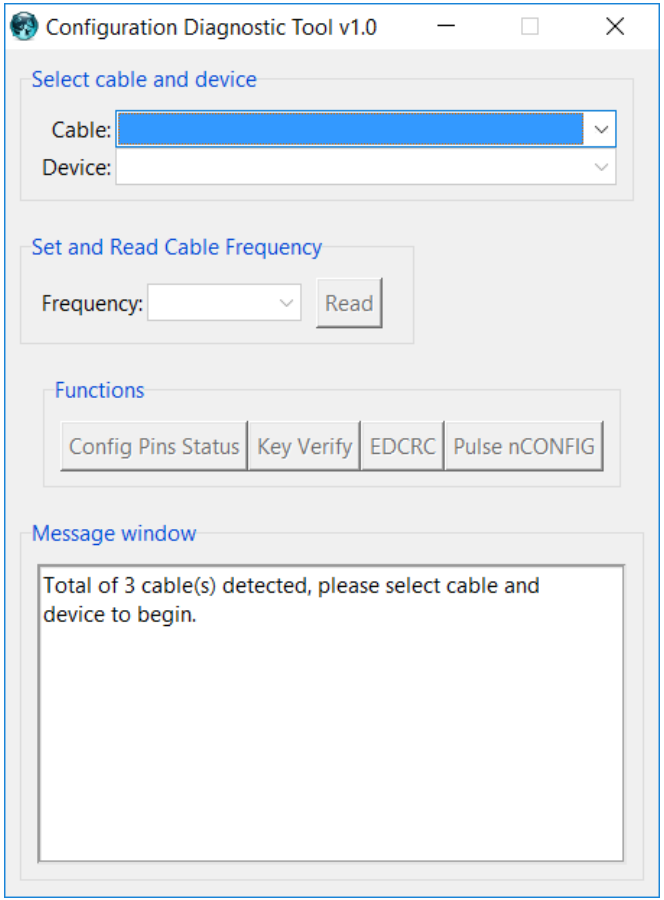
Agenda

- Overview
- Supported FPGA Families
- Features
- Known Limitation
- Where to Download

Overview (1/2)

Why we need this tool? Common questions:

- Configuration failure:
  - Have you set MSEL correctly?
  - Can you verify nCE connect to GDN?
  - What is nSTATUS and nCONFIG state?
  - Can you probe CONF_DONE?
- Design security:
  - Can you run KEY_VERIFY instruction to verify your key programming?
  - Do you program tamper protection bit?
- Error Detection CRC
  - Can you read EMR to understand the error type and location?
- How to force FPGA to reconfigure without pulse nCONFIG pin low?



Overview (2/2)

The tool consists of:

- *config_diag_tool.tcl*
- *device_data.tcl*

How to execute the tool:

- Your machine need to install Quartus Prime software in order to run this tool
  - Quartus Prime software come with Tcl interpreter
- If your Operation System has default Tcl interpreter to run .tcl file, then you may just double click *config_diag_tool.tcl*, or
- In Nios II Command Shell, execute the .tcl file with below command:

  > tclsh *config_diag_tool.tcl*

Supported FPGA Families

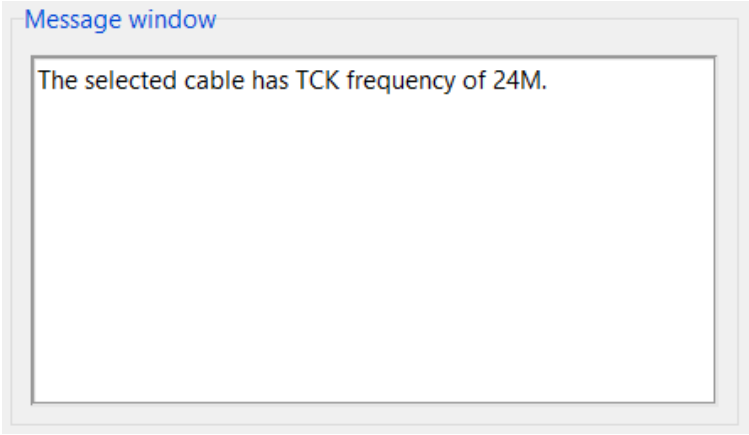
The tool can be made supportable for all Intel FPGA families, **except Stratix 10**, due to different architecture

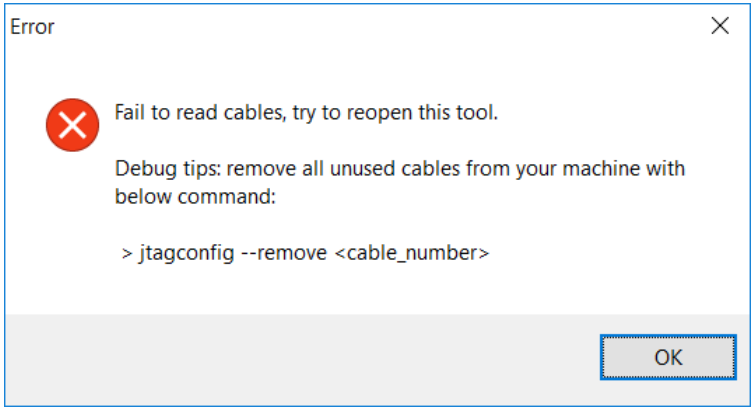
- Currently supported
  - Stratix V, Arria V, Cyclone V including SoC devices
  - Arria 10 and SoC devices
- Support can be extended
  - All FPGA families prior to 28nm and 20nm devices

Feature (1/6)

Self-explanatory

- Responses appeared in message window
- Debug tips when error occurred
  - More useful debug tips can be added from time to time

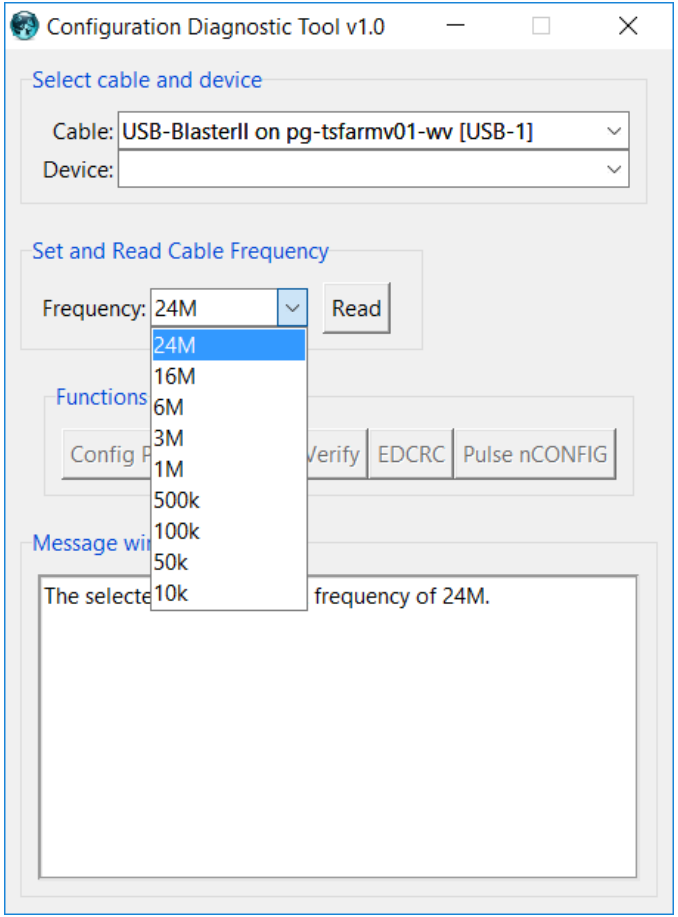




Feature (2/6)

USB Blaster II JTAG frequency configuration

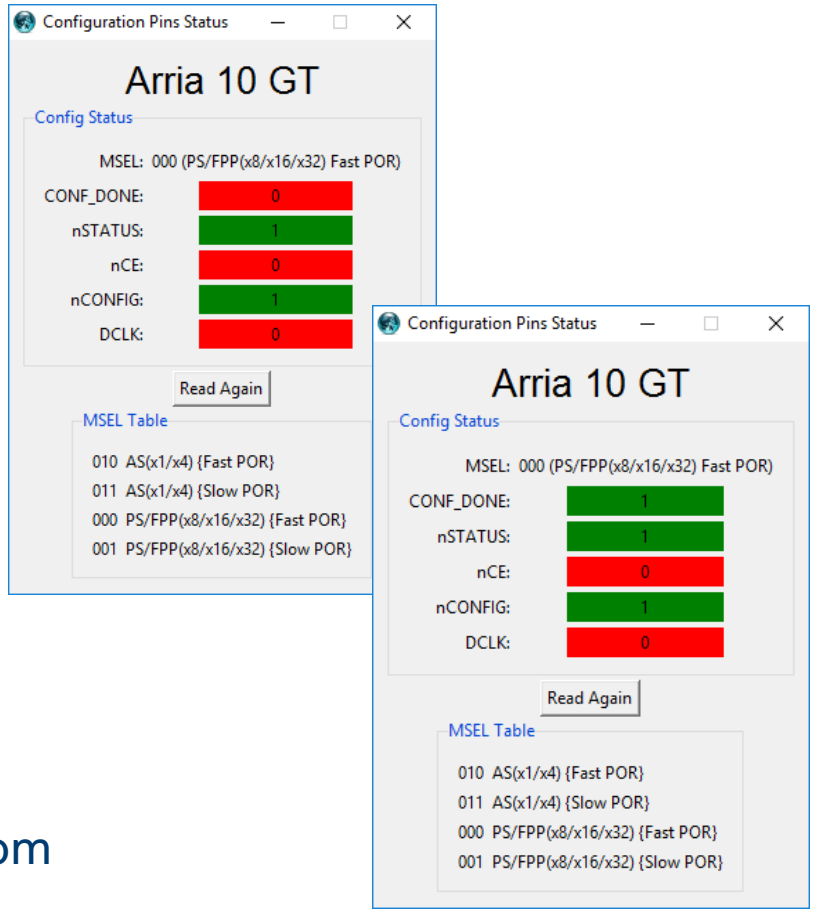
- Auto-detection upon cable selection
- Dropdown list for JTAG frequency setting



Feature (3/6)

Configuration Pins Status

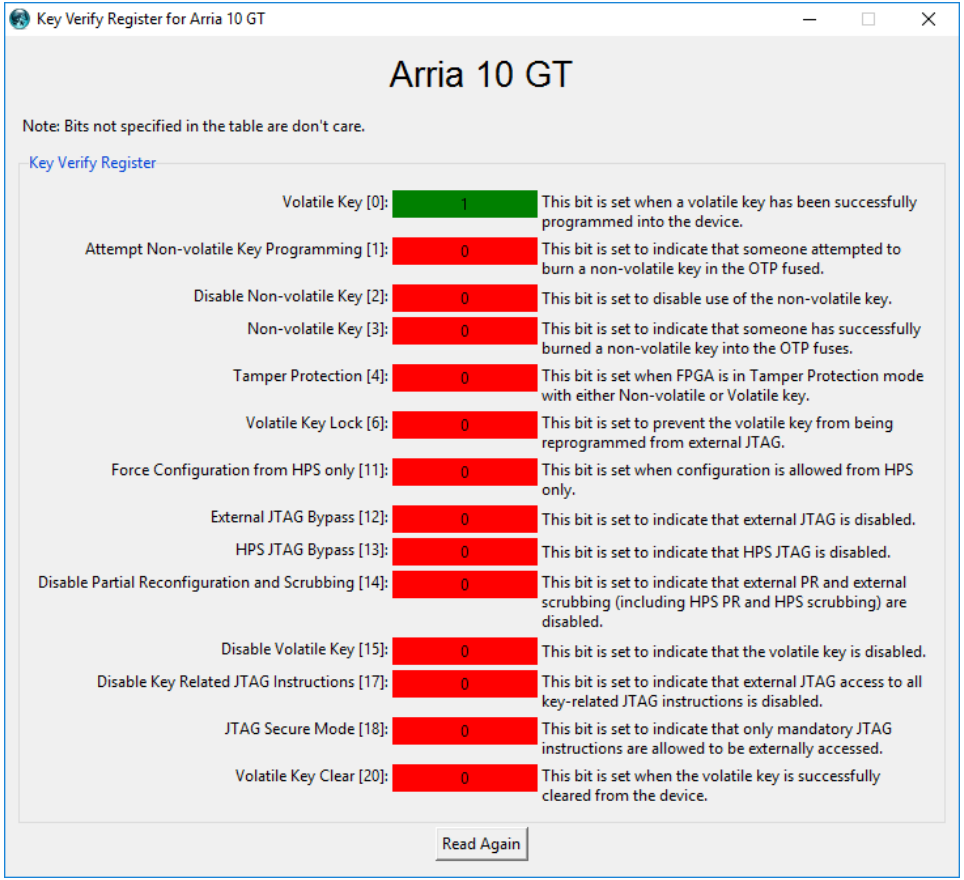
- Read the FPGA configuration pins status
  - MSEL
  - CONF_DONE
  - nSTATUS
  - nCE
  - nCONFIG
  - DCLK
- Enhancement can be made to allow custom pins to be read



Features (4/6)

Design Security

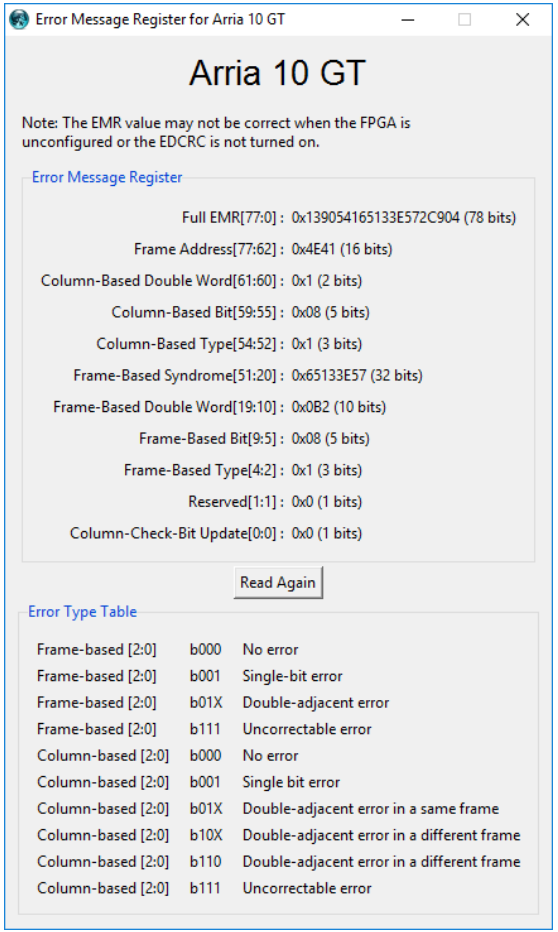
- Read the Key Verify Register and list down the bit information
  - Less dependent on User Guide



Feature (5/6)

Error Detection CRC

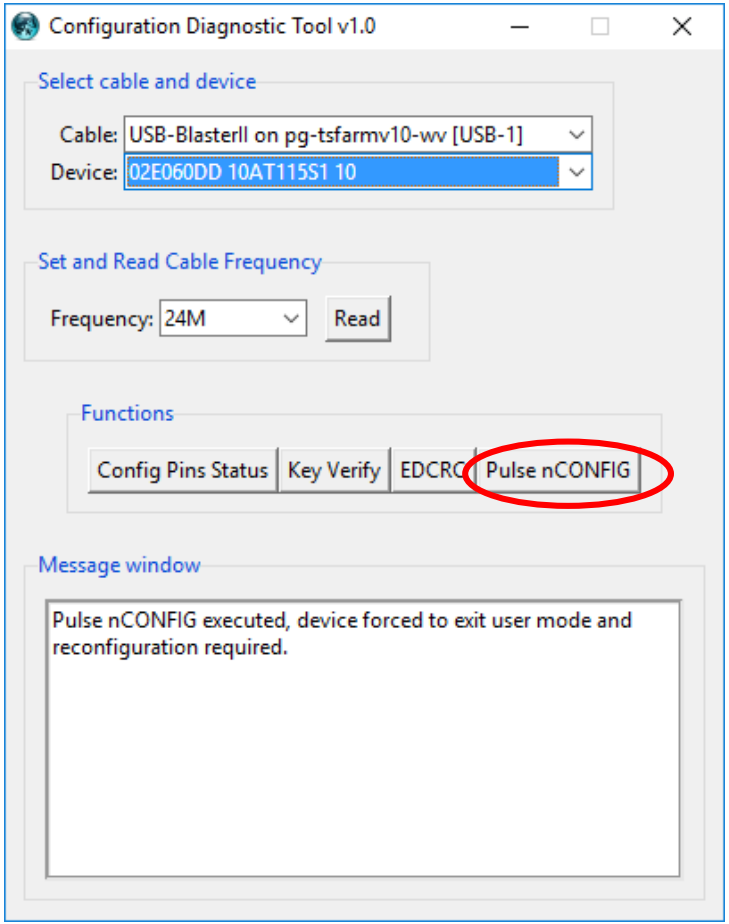
- Read Error Message Register (EMR) to understand EDCRC failure location



Features (6/6)

Pulse nCONFIG instruction

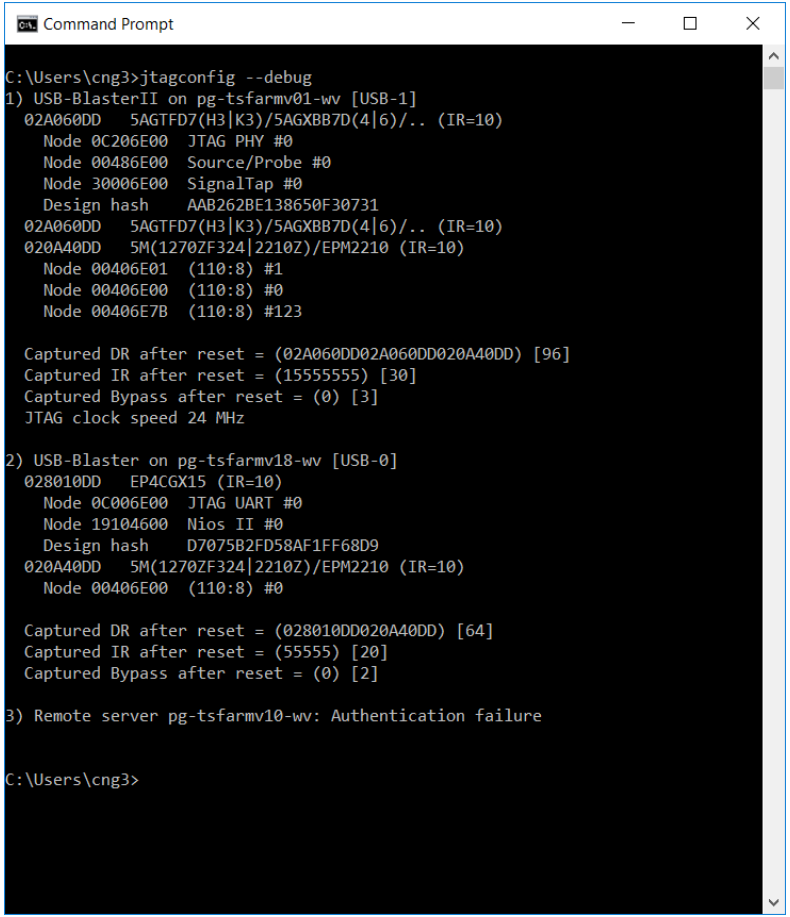
- Force FPGA exit user mode remotely
  - This is not a documented feature
  - Useful for debug purpose



Known Limitation

This tool should always work if Intel FPGA is the only device in JTAG chain. Some known limitation such as:

- If the JTAG chain consists of devices with unknown IR length (3rd party devices) to jtagconfig command
  - This tool uses “jtagconfig --debug” command to read cables and devices
- Unable to handle virtual JTAG
  - Buffer bit appeared in JTAG chain causes problem

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