WHY I WILL BE USING RISC-V IN MY NEXT CHIP

January 7, 2016 Andreas Olofsson 3 Comments Andreas' Blog

This week I attended the 3rd RISC-V Workshop and I was blown away by the momentum and energy in the room. This architecture is clearly going places! The best way to convince yourself of the quality of RISC-V ISA is to start working with the open source reference implementations on github. It took me less than 1 hour total to set up risc-v tools and generate verilog code from chisel! If you need more convincing before getting started here are the top 10 reasons why I will be using RISC-V in my next project! Those of you new to RISC-V, should read the mission statement from Krste Asanovic and David Patterson first.

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10. RISC-V is state-of-the-art

Binary compatibility is a blessing and a curse for any successful architecture. It can simultaneously be your biggest strength ("stickiness") and weakness (cost). The RISC-V team had the luxury of learning from mistakes made over the last 50 years of computer architecture development and has left all of the heavy baggage behind. Questionable features like delay slots and and bloated instruction sets have been replaced by a clean and extensible architecture. An analysis of the RISC-V instruction set architecture can be found here. Benchmarks are controversial but by most measures the RISC-V performance should be "good enough" for most use cases. In the long run, good enough and free is always going to win. For applications that need more performance there are always accelerator options. The configurability and efficiency and of the RISC-V will be big advantages in IoT applications where energy consumption is the #1 concern.

9. Rock-star team

UC Berkeley professor and RISC-V co-founder David Patterson literally "wrote the book" on computer architecture and led one of the first RISC research projects at Berkeley in the early 1980's. Many of us fell in love with computer architecture thanks to Professor Patterson's legendary books. [EDIT: corrected] The RISC-V project was started in 2010 by UC Berkeley professors Krste Asanovic, David Patterson together with graduate students Yunsup Lee and Andrew Waterman. The project has since evolved to include a large team of contributors.

The Berkeley team have been incredible productive with an impressive number of advanced node RISC-V chip tapeouts over the last few years.

8. Strong financial support

Complex open source projects live and die by the energy put into the projects by contributors and more often than not that energy is directly tied to money. In the case of RISC-V, graduate students are an essential part of the development process and they carry a cost. Significant sponsorship from DARPA and NSF is a key component in the success to date of the RISC-V project. The Berkeley group sponsors also include: Intel, Google, HP, Huawei, Nvidia, Samsung, LG, and Oracle.

7. Academic support

Academia has played (and continue to play) a big role as “king makers” for advanced technology. Computer architecture battles are fought over decades. The free and open source RISC-V has a clear mind-share advantage over proprietary architectures in academia. The RISC-V already have 40 University projects under way (Cambridge, ETH Zurich, Cornell,..). Imagine a processor landscape in the post-Moore era that includes 1,000’s of computer engineers graduating yearly completely hooked on RISC-V?

6. Grassroots support

The value of grass roots contributor support should not be underestimated in open source collaborative projects. From my Parallella experience, I can tell you that some of these contributors are the most gifted engineers on the planet. More often than not these individuals contribute out of a sense of “love and purpose”. Clearly proprietary architectures will never be able to leverage this community. So far, RISC-V has attracted an impressive number of individual contributors.

5. Industry support

At the end of the day money runs the world and no computer architecture will achieve staying power without broad industry support in one or more markets. The good news for RISC-V is that the software and industry hates hardware vendor lock-in monopolies (including IP). The recent announcement that HP, Oracle, Microsemi, and Google are all backing RISC-V is a big win for RISC-V.

4. Collaborative model

A processor core is all about the eco-system as ARM has shown convincingly over the last 20 years. But, as Linux and many other successful open source projects have demonstrated, open source collaboration wins over proprietary monopolies in the long run. The RISC-V team has shown from day one that they are very receptive to collaboration through their development practices, trade press articles, workshops, and scientific publishing. The 3rd RISC-V workshop had an impressive list of 150 attendees, with many being turned away due to lack of capacity.

3. Licensing (FREE!)

The semiconductor industry has a terrible track record in regards to open source chip design and even struggles with basic code reuse concepts. IP licensing is a well established model but one that comes at a high cost both in terms of licensing fees and time to market for new projects. UC Berkeley has very wisely chosen the no-nonsense royalty free permissive BSD license for the RISC-V code and is reportedly working on a permissive license for the instruction set itself through the RISC-V foundation. The semiconductor industry would not take kindly to a copyleft license like GPL which would force a company to open up everything inside the chip. Permissive licenses like the MIT license and BSD enable large risk averse companies (with legal departments) to participate. With permissive licenses, there is always the risk that big companies will only take (and not give back) but with GPL style licensing in they just won't get involved.

2. Price (FREE!)

The vision for IoT and other low cost applications spaces will require the semiconductor industry to stretch the dollar beyond what is possible today with traditional IP licensing and EDA tooling. As per device prices continue trending towards zero, engineering costs and royalty costs must be drastically cut. The RISC-V zero royalty model is very attractive for ultra low cost SOC products. It's hard to see how proprietary processors like ARM, ARC, MIPS, and Verisilicon will be able to compete with a free and "good enough" RISC-V eco-system. The raw silicon cost of a royalty free 64-bit RISC-V processor running Linux in an advanced process node is only a couple of cents, making it "free" for all practical purposes. The semiconductor industry has always lived by the edict of selling more chips for less: at a few cents per processor, computers will become disposable.

1. Timing

For the last 50 years, programmers, hardware engineers, product managers, and CEOs have been betting product and company futures on specific instruction set architectures. Today, there are only two winners standing (ARM and x86) and a handful of survivors (MIPS, Tensilica, Power, ARC). Over the years millions of engineering hours have been spent on software and hardware associated with losing architectures. When architectures eventually die the majority of this work has to be discarded. For the post-Moore era (from now until forever???) it is imperative that we improve both computing energy efficiency and capital efficiency. To accomplish this, we need an architecture that is bigger than any one company. Proprietary computer architectures will undoubtedly be around for a long time in legacy applications but for new and exciting markets my bet is on RISC-V!

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