OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-25664YW-4A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bazile Peter	**Anthony Perkins**	**Rekha Mani**
Date: 11/06/08	Date: 11/06/08	Date: 11/06/08

☐ **Approval for Specification only**

☐ **Approval for Specification and Sample**

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	15/05/08	--	--	Initial Release	
B	11/06/08	10		Change in pin number 29, VCC description	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	256 x 64 Dots
Colour	Yellow Monochrome
Overall Dimensions	88.00 (W) × 27.80 (H) × 2.00 (D) mm
Viewing Area	78.78 (W) x 21.18 (H) mm
Screen Size	3.12”
Mode	Passive Matrix
Duty ratio	1/64
Driver IC	SSD1322
Operating temperature	-30°C ~ +85°C
Storage temperature	-40°C ~ +90°C

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2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	256 x 64	Dots
Overall Dimensions	88.00 (W) × 27.80 (H) × 2.00 (D)	mm
Viewing Area	78.78 (W) x 21.18 (H) mm	mm
Active Area	76.78 (W) x 19.18 (H)	mm
Dot Size	0.28 (W) 0.28 (H)	mm
Dot Pitch	0.30 (W) x 0.30 (H)	mm
Weight	9.95	g
IC Controller/Driver	SSD1322	

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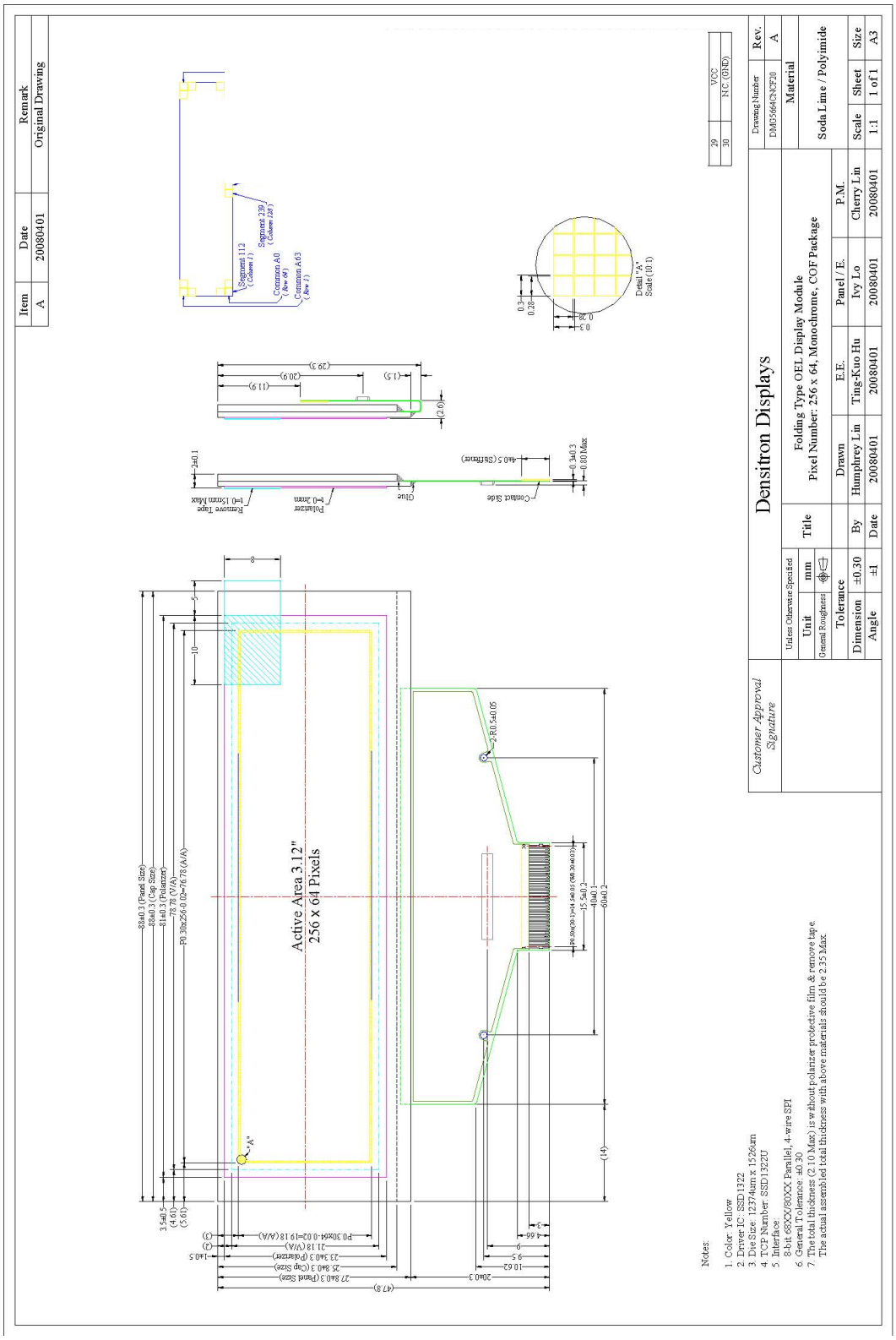
2.2 MECHANICAL DRAWING



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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	55	mA	1,2
Operating Temperature	Top	-30	+85	°C	
Storage Temperature	Tst	-40	+90	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

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3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}		11.5	12	12.5	V
High Level Input	V_{IH}		$0.8xV_{DDIO}$	--	V_{DDIO}	V
Low Level Input	V_{IL}		0	--	$0.2xV_{DDIO}$	V
High Level Output	V_{OH}	I_{OUT}=100µA, 3.3MHz	$0.9xV_{DDIO}$	--	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT}=100µA, 3.3MHz	0	--	$0.1xV_{DDIO}$	V
Operating Current for V_{CI}	I_{CI}	Note 4	-	1.8	2.25	mA
		Note 5	-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI,SLEEP}$		-	1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$		-	1	5	µA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of panel characteristics and the customers request.

Note 4: V_{CI} = 2.8V, V_{CC} = 12V, 50% Display Area Turn on.

Note 5: V_{CI} = 2.8V, V_{CC} = 12V, 100% Display Area Turn on.

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3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C. (GND)	--	*Reserved Pin (Supporting Pin).* The supporting pins can reduce the influences from stresses on the function pins. This pin must be connected to external ground.
2	VSS	P	*Ground of Logic Circuit* This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground
3	VCC	P	*Power Supply for OEL Panel* This is the most positive supply pin of the chip. They must be connected to external source.
4	VCOMH	P	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.
5	VLSS	P	*Ground of Analog Circuit* This is analog ground pin. IT should be connected to VSS externally
6~13	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessors data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.
14	E/RD#	I	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-sseries microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
15	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial mode is selected, this pin must be connected to VSS.
16 17	BS0 BS1	I	*Communicating Protocol Select* These pins are MCU interface selection input. See the following table:

	BS0	BS1
3-wire SPI	1	0
4-wire SPI	0	0
8-bit 68XX Parallel	1	1
8-bit 80XX Parallel	0	1

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18	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detailed relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams
19	CS#	I	*Chip Select* This pin is the chip select input. When the pin is enabled for MCU communication only when CS# is pulled low..
20	RES#	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
21	FR	O	*Cascade Application Connection Pin* This pin is No Connection pins. Nothing should be connected to this pin. It should be left open individually.
22	IREF	I	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10μA
23	N.C.	-	*Reserved Pin* The N.C. pin between function pins are reserved for compatible and flexible design.
24	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signals should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.
25	VDD	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances.
26	VCI	P	*Power Supply for Operation* This is a voltage supply pin. It must be connected to external source & always be equal or higher than VDD & VDDIO.
27	VSL	P	*Voltage Output Low Level for SEG Signal* This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.
28	VLSS	P	*Ground of Analog Circuit* This is the analog ground pin. It should be connected to VSS externally
29	VCC	I	*Power Supply for OEL Panel* This is the most positive supply pin of the chip. They should be connected to external source.
30	N.C. (GND)	-	*Reserved Pin (Supporting Pin).* The supporting pins can reduce the influences from stresses on the function pins. This pin must be connected to external ground.

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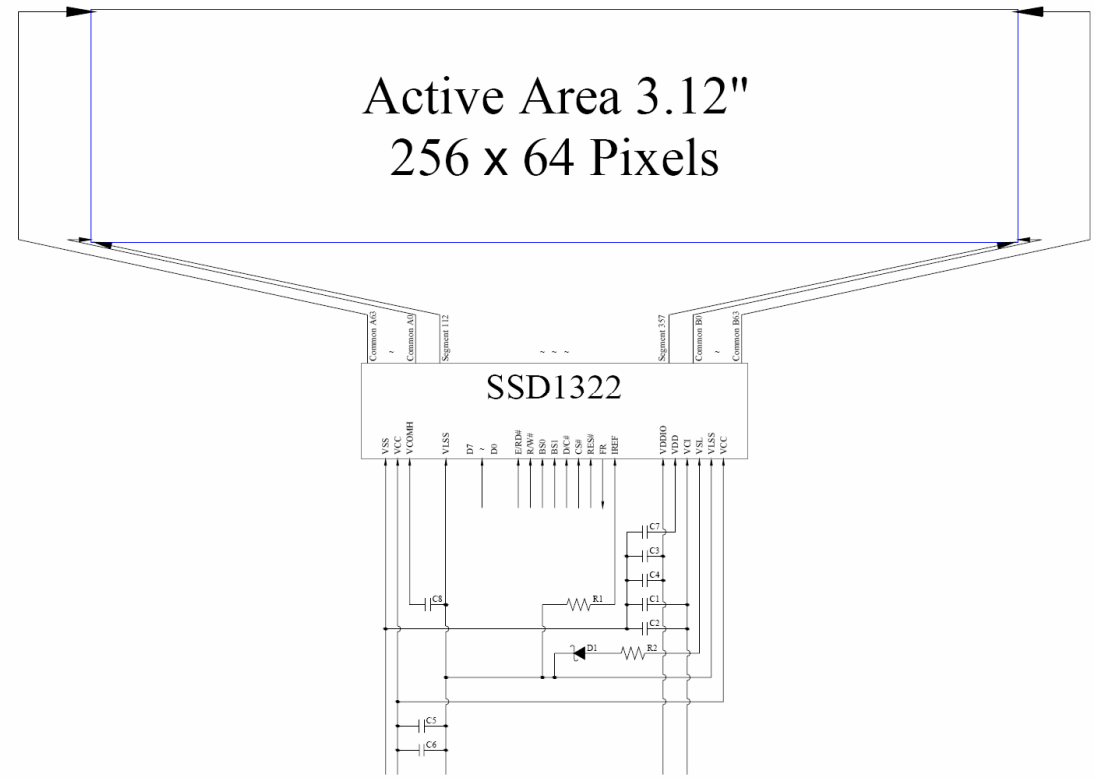
3.4 BLOCK DIAGRAM



MCU Interface Selection: BS0 and BS1
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, CS#, and RES#

C1, C3, C5: 0.1µF
C2, C4: 4.7µF
C6: 10µF
C7: 1µF
C8: 4.7uF / 25V Tantalum Capacitor R1: 680kΩ,
R1 = 680kΩ, R1=(Voltage at IREF – VSS) / IREF
R2: 50Ω, 1/4W
D1: ≤1.4V, 0.5W

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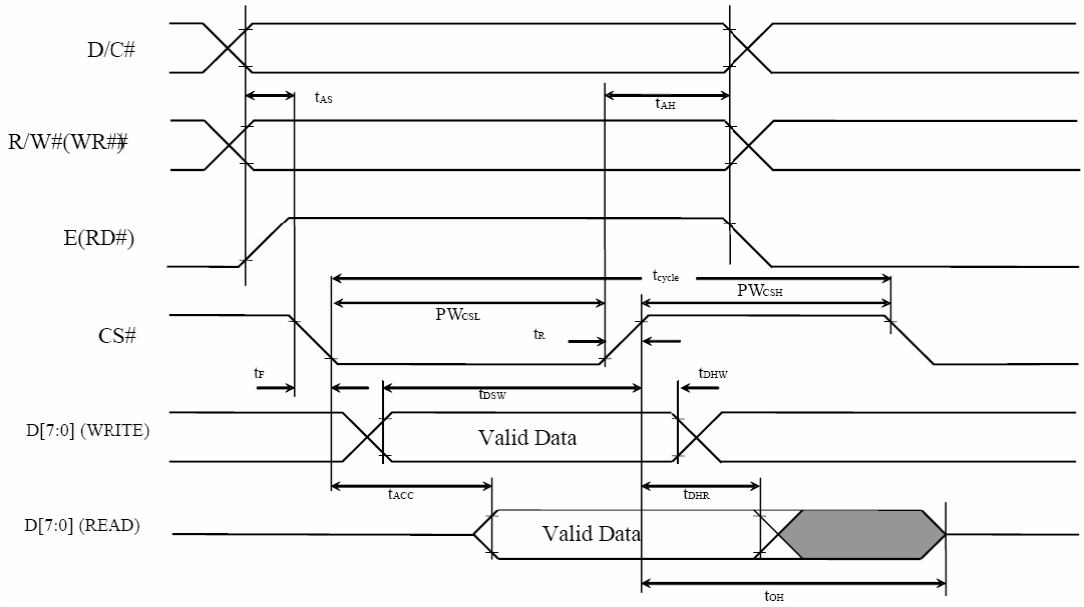
3.5 TIMING CHARACTERISTICS

3.5.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



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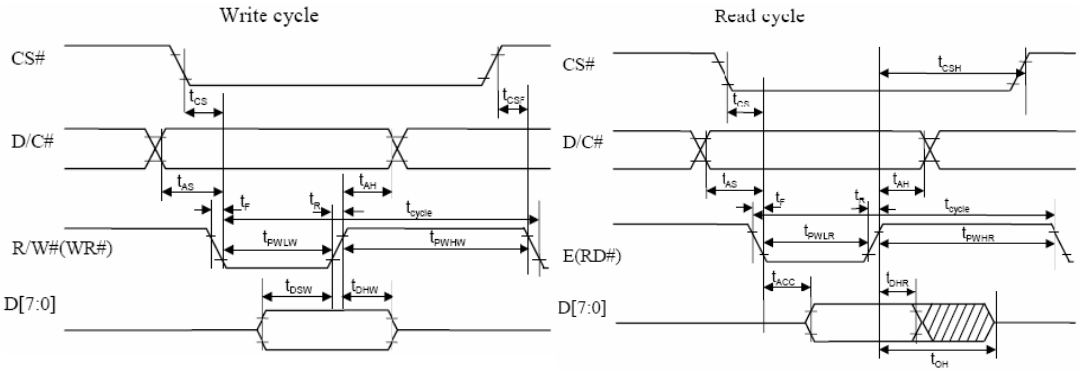
3.5.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



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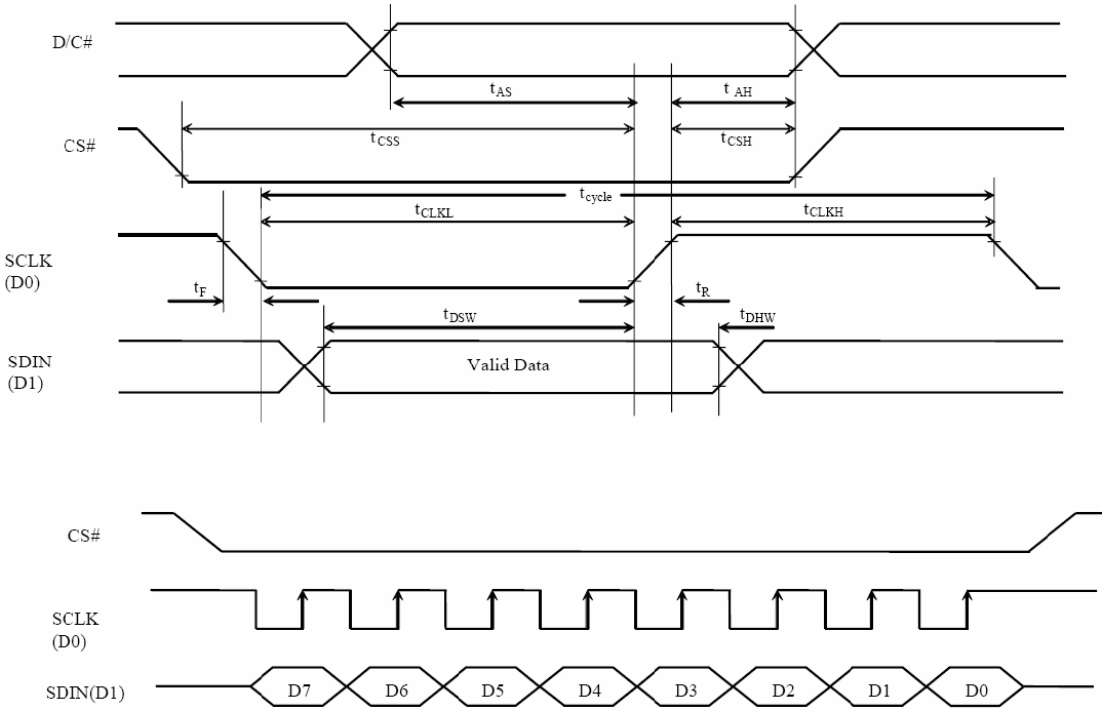
3.5.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



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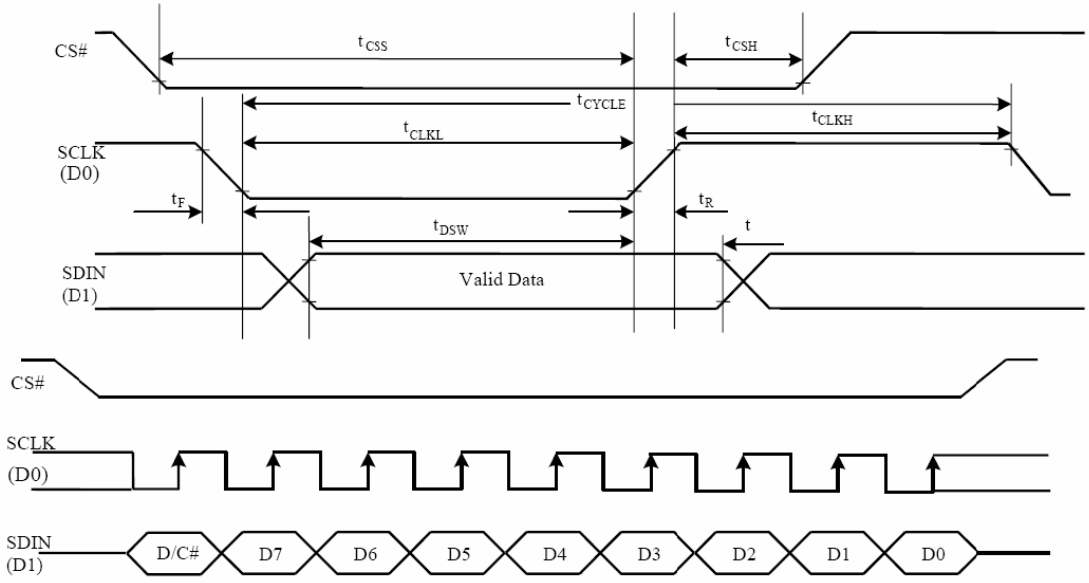
3.5.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
$t_{CLK}L$	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m^2
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.44 0.46	0.48 0.50	0.52 0.54	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at V_{CI} = 2.8V, V_{CC} = 12V

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

Refer to the Technical Manual for the SSD1322

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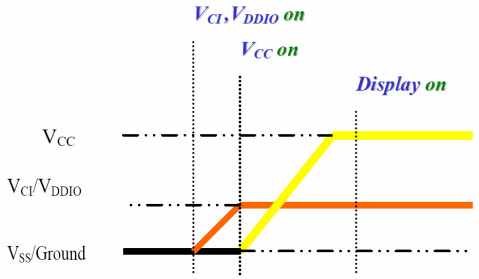
5.2 POWER DOWN AND UP SEQUENCE

To protect the panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge and discharge before/after operation.

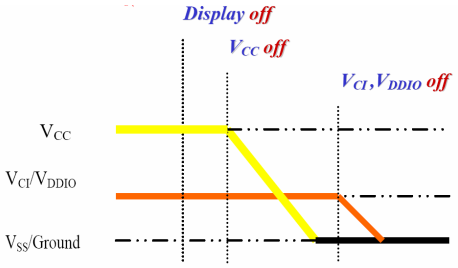
5.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms (when V_{CC} is stable)
7. Send Display on command



5.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



5.3 RESET CIRCUIT

When RES# input is low, the chip initialized with the following status:

1. Display is OFF
2. 480x128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control registers is set at 7Fh

5.4 ACTUAL APPLICATION EXAMPLE

Command usage and explanation of an actual example

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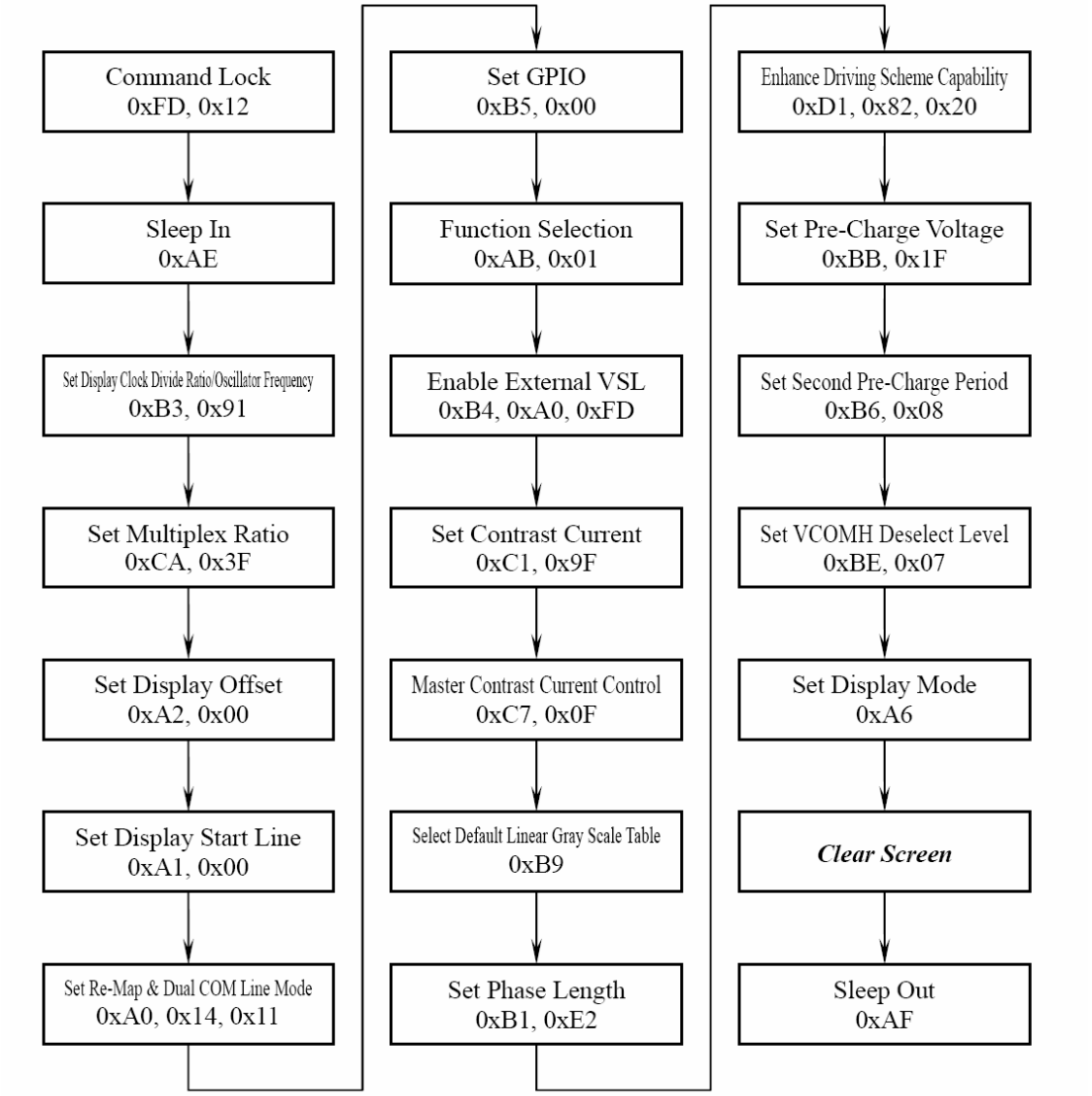
<Initialization>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

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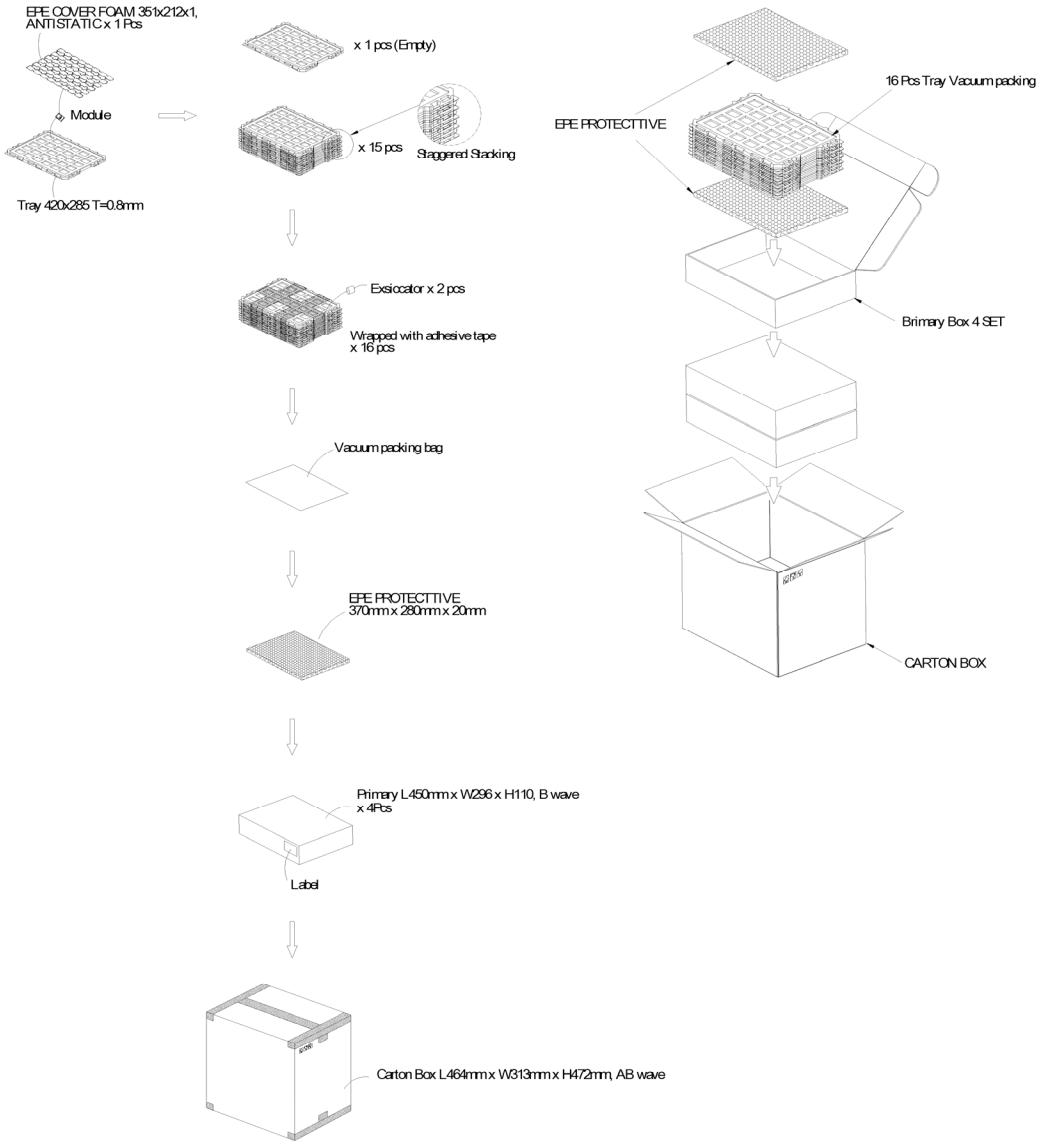
6 PACKAGING



6.1 LABELLING AND MARKING

DENSITRON DD-25664YW-4A TW YYMM

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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

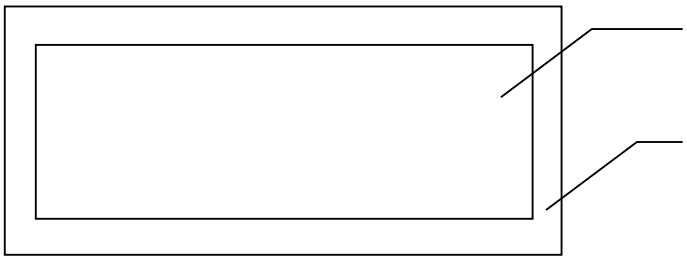
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 Delivery inspection standards

- IPC-AA610 rev. C, class 2 electronic assemblies standard

7.2.2 Zone definition



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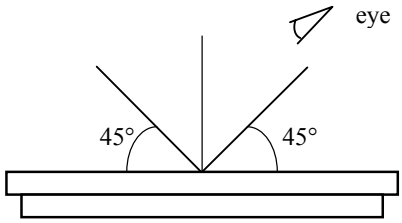
7.2.3 Visual inspection

- Inspect under 30W fluorescent lamp leaving 50 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- Inspect the module at 45° right and left, top and bottom.
- Use the optimum viewing angle during the contrast inspection.



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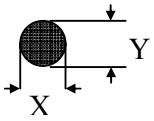
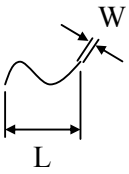
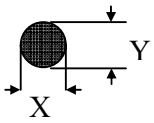
7.2.3.1 Standard of appearance inspection

Units: mm

<table>
<tr><th>Class</th><th>Item</th><th colspan="4">Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td colspan="4">Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td colspan="4">Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td colspan="4">Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td colspan="4">Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>LCD Display</td><td colspan="4">Missing lines or wrong patterns on LCD display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td colspan="4">Round type: as per following drawing
∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td colspan="4">Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td colspan="4">∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
</table>

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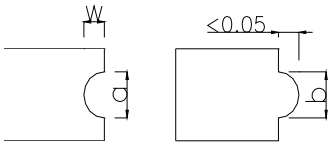
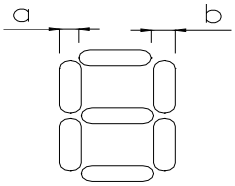
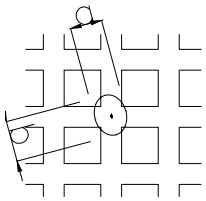
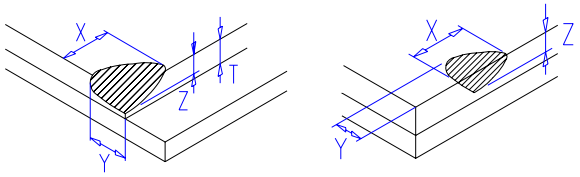
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>
1b. Pin hole on dot matrix display


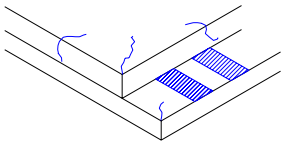
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width


<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2


<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>
X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T


</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>
Cracks not allowed

</td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affects electrical function</td></tr>
</table>

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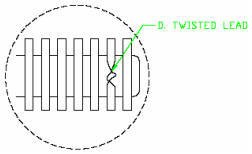
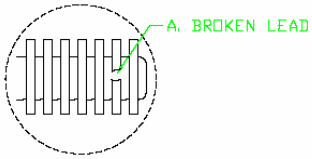
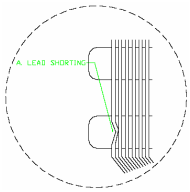
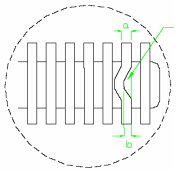
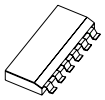
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed
  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed
  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit
  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width
  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB
  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	85°C, 500 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature & High Humidity Storage	60°C, 90% RH, 500 hrs	
Thermal Shock Storage	-40°C ↔85°C, 100 cycles 30 min. dwell	

- All operation tests are conducted in all display on pattern.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C□55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 40,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

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9 HANDLING PRECAUTIONS

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).

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