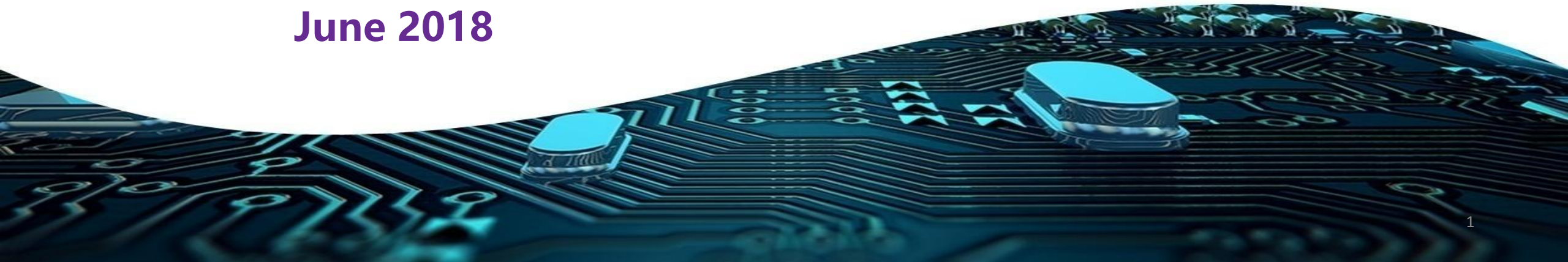
The Ultra-Low Power Open-source Core

to Accelerate the Spreading of RISC-V in China

bob_hu@nucleisys.com

June 2018



Agenda

- Personal Introduction
- The Status of RISC-V in China
- Our Passion of RISC-V in China
- Overview of Hummingbird E203 Core
- Details of Hummingbird E203 Core
- The Published 1st Chinese RISC-V Book
- The Board for Hummingbird E203
- The 2nd Coming Chinese RISC-V Book
- The Education Program for RISC-V

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Personal Introduction

Bob Hu ***bob_hu@nucleisys.com***

- **Highlights**
  - Over 10 years of ASIC design and verification experiences with 8 years of CPU industry experiences
- **Education Background**
  - Master of Microelectronics, Bachelor of EE, Shanghai Jiaotong University
- **Work Experiences**
  - 2018 ~ Now Founder, Nuclei System Technology
  - 2017 ~ 2018 Processor Architect, Wuhan Silicon Integrated
  - 2016 ~ 2017 ASIC Director, Bitmain AI processor
  - 2012 ~ 2016 R&D Manager, Synopsys ARC processor IP
  - 2010 ~ 2012 Senior CPU Designer, Marvell

“硅农亚历山大”

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The Status of RISC-V in China

Positive and Negative Status

- **Positive Status**
  - The ecosystem from industry and community growing very quickly in China Mainland
  - More and more people start to know RISC-V
- **Negative Status**
  - Very few people know RISC-V before year 2018
  - Very few people understand RISC-V
    - Many people even now treat RISC-V equal to another free and open-source Core
    - The most frequently asked question I heard is: I heard there is a RISC-V, then where can I download that "free core" ?——*Makes me dont know how to answer this question…*
    - Very few people can understand the profound effect of RISC-V to China semiconductor industry
  - Very few RISC-V cores developed by China player
  - Very few Chinese materials (include hardware and embedded software tools) for beginners
  - Very few Schools have already used RISC-V to educate in the classroom
  - Very few professional RISC-V processor IP company in China

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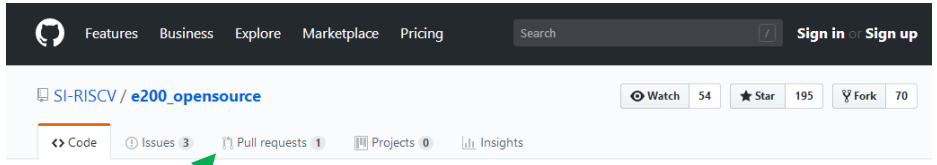
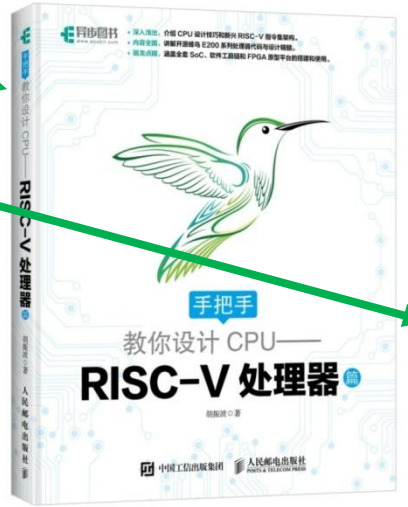
Our Passion of RISC-V in China

Our Passions and Contributions



- **Negative Situations**
  - Very few RISC-V cores developed by China player
  - Very few people know RISC-V before year 2018
  - Very few people understand RISC-V
  - Very few Chinese materials (include hardware and embedded software tools) for beginners
  - Very few Schools have already used RISC-V to educate (Starting Ongoing)
  - Very few professional RISC-V processor IP company in China
- **Our Works to Improve Them**
  - We developed and open-sourced Hummingbird E203 core
  - I Started a WeChat subscription number（微信公众号）to popularize RISC-V concepts
  - I published the 1st Chinese RISC-V book
  - I am ongoing to publish 2nd Chinese RISC-V book
  - We are promoting Hummingbird E203 into the education fields
  - We have established one start-up Company now!



2nd Book

RISC-V架构与嵌入式 开发快速入门 (RISC-V Embedded Quick Start)

Our Passion of RISC-V in China

The 1st open-source RISC-V Core from China Mainland

https://github.com/SI-RISCV/e200_opensource

Hummingbird E200 Opensource Processor Core

About

This repository hosts the project for open-source hummingbird E200 RISC processor Core.

The Hummingbird E200 core is a two-stages pipeline based ultra-low power/area implementation, which has both performance and areas benchmark better than ARM Cortex-M0+ core, makes the Hummingbird E200 as a perfect replacement for legacy 8051 core or ARM Cortex-M cores in the IoT or other ultra-low power applications.

To boost the RISC-V popularity and to speed up the IoT development in China, we are very proud to make it open-source. It is the first open-source processor core from China mainland with industry level quality and state-of-art CPU design skills to support RISC-V instruction set.

Our ambition is to make "Hummingbird E200" become next 8051 in China, please go with us to make it happen.

Usages and Applications

The open-source Hummingbird E200 core can be a perferct candidate for the following fields:

- Replace legacy 8051 core for better performance.
- Replace Cortex-M core for lower cost.
- Also, the Hummingbird E200 core as a simple ultra-low power core and SoC, which is "蜂鸟虽小、五脏俱全", with detailed Docs and Software/FPGA Demos, hence, it will be a perfect example for lab practice in university or entry-level studying.

Detailed Introduction

We have provided very detailed introduction and quick start-up documents to help you ramping it up.

The detailed introduction and the quick start documentation can be seen from `e200_opensource/doc` directory.

By following the guidences from the doc, you can very easily start to use Hummingbird E200 processor core and demo SoC.

SI-RISCV / e200_opensource

Watch 54 | Unstar 195 | Fork 71

Code | Issues 3 | Pull requests 1 | Projects 0 | Wiki | Insights

The Ultra-Low Power RISC Core

risc-v | ultra-low-power | cpu | core | china | verilog

87 commits | 1 branch | 0 releases | 2 contributors | Apache-2.0

Branch: master | New pull request | Create new file | Upload files | Find file | Clone or download

SI-RISCV Update README.md — Latest commit 92d9cf4 on 19 May

boards	add a placeholder boards directory	5 months ago
doc	Update README.md	a month ago
fpga	update the prebuilt mcs to easy user download it directly	4 months ago
prebuilt_tools	add the prebuilt tools link to easy user	5 months ago
riscv-tools	add the missing tests	5 months ago
rtl/e203	the original freedom-e310 chisel generated QSPI have a bug in Quad-mo...	a month ago
sirv-e-sdk	add the missing header file	5 months ago
tb	enlarge the interrupt generate period in tb	5 months ago
vsim	update makefile	5 months ago
.gitignore	update ignore list	5 months ago
LICENSE	upload e203 RTL codes with copyright notice and LICENSE	9 months ago
README.md	Update README.md	a month ago

Our Passion of RISC-V in China

WeChat subscription number（微信公众号）

实例讲解进驻Google两位大神主推的异构计算与RISC-V

John Hennessy和David Patterson两位计算机体系结构的泰山北斗双双进驻Google

大道至简——RISC-V架构之魂（上）

本文为《RISC-V CPU设计》专栏和《RISC-V嵌入式软件开发》专栏系列文章之一

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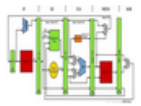

八一八处理器流水线（上）？

本文将讨论处理器的一个重要的基础知识："流水线"。本文将简要介绍处理器的一些

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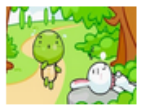


动如脱兔，静若处子——处理器低功耗设计的诀窍

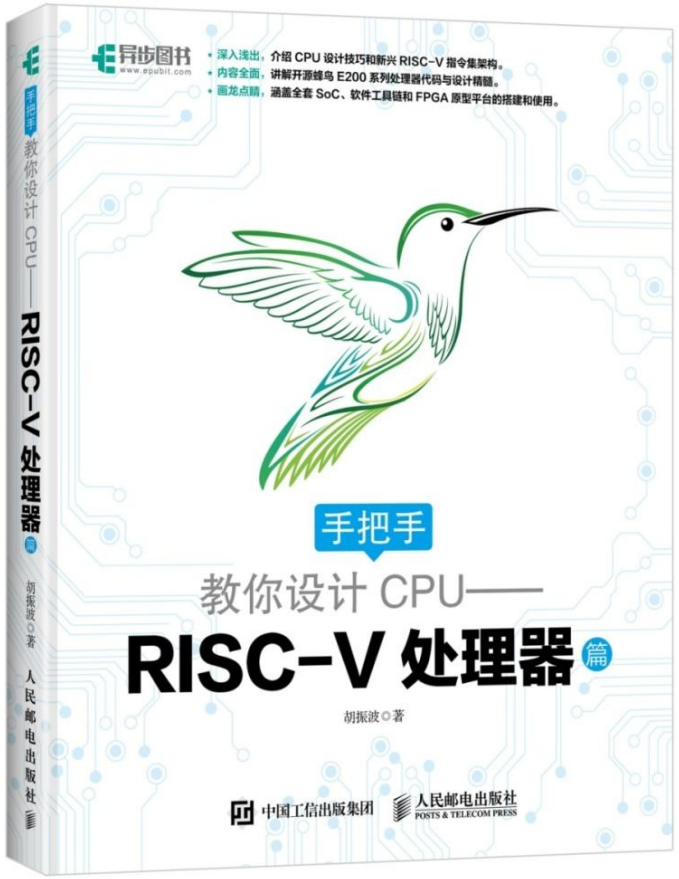
低功耗机制对于处理器而言至关重要。本章将对处理器的低功耗技术加以概述。

市，越来越多的爱好者开始使用开源的蜂鸟E203 RISC-V处理核，很多初学者留言询问有关RISC-V工具链使用的问题，因此本公众号将开始陆续发表若干篇有关RISC-V软件工具链使用的文章，包括：

- RISC-V嵌入式开发准备篇1：编译过程简介
- RISC-V嵌入式开发准备篇2：嵌入式开发的特点介绍
- RISC-V嵌入式开发入门篇1：RISC-V GCC工具链的介绍
- RISC-V嵌入式开发入门篇2：RISC-V汇编语言程序设计
- RISC-V嵌入式开发上手篇：基于HBird-E-SDK平台的软件开发与运行
- RISC-V嵌入式开发实践篇：运行开源蜂鸟E200 MCU更多示例程序
- RISC-V嵌入式开发新奇篇：基于Windows Eclipse IDE的软件开发与运行
- RISC-V嵌入式开发升华篇：基于开源蜂鸟E200 MCU移植RTOS

Our Passion of RISC-V in China

The 1st Chinese RISC-V Book in China



第一部分　CPU 与 RISC-V 综述

The book Introduced in: **https://mp.weixin.qq.com/s/eECYepzO8c_FS_I9u2zIaA**

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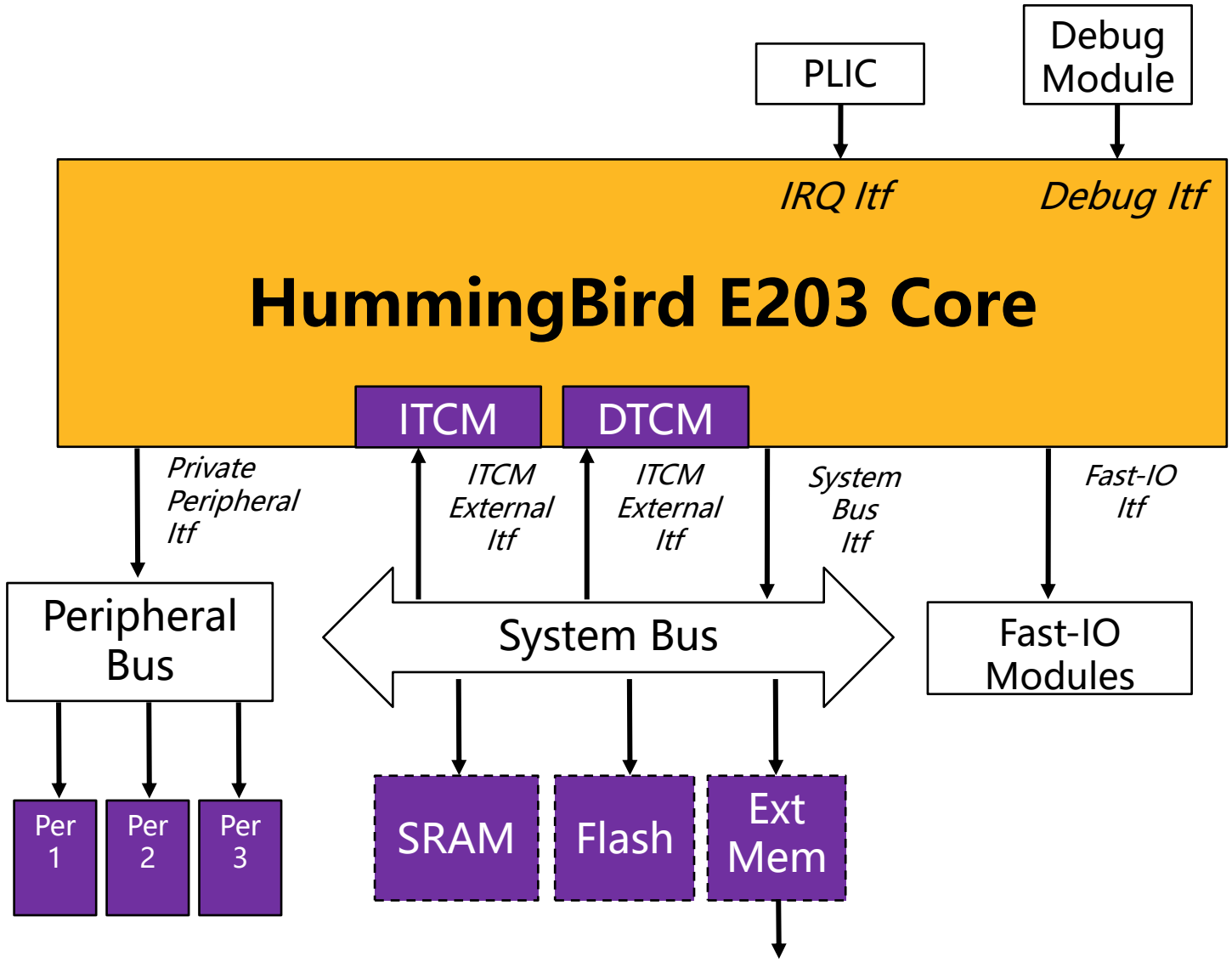
Overview of Hummingbird E203 Core

The 1st Open-Source RISC-V in China

- **Hummingbird Ultra-Low-Power Processor Core**
  - Ultra low-area 32bits RISC-V processor core
  - Two pipeline stages
  - Support RV32IMAC architecture
  - Area and Power in rival to Cortex M0/M0+/M3
  - Integrated ITCM (Instruction Tightly Coupled Memory) and DTCM (Data Tightly Coupled Memory)
  - Open-sourced in Github
    https://github.com/SI-RISCV/e200_opensource
- **Application Domains**
  - General or specified MCU core
  - Mix-signal Chip controller core
  - SoC controller core



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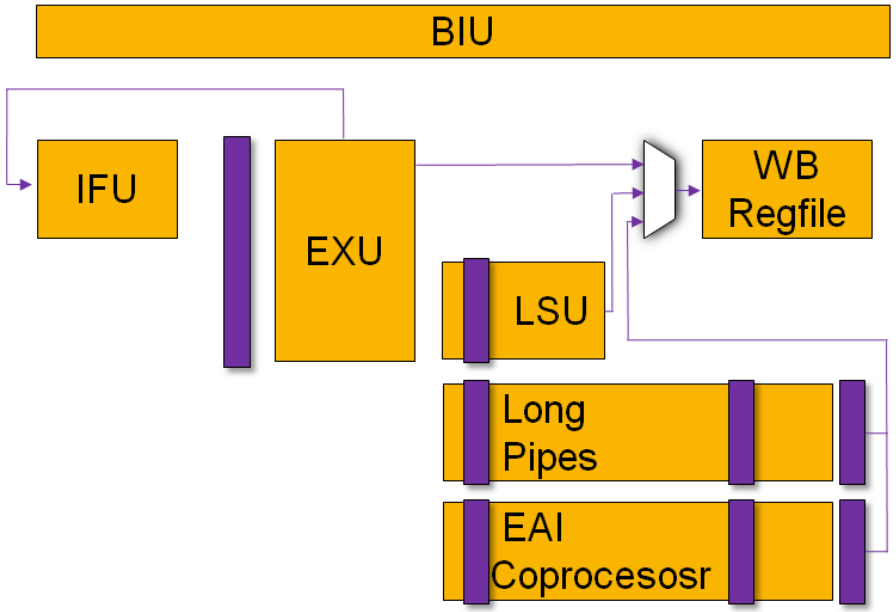
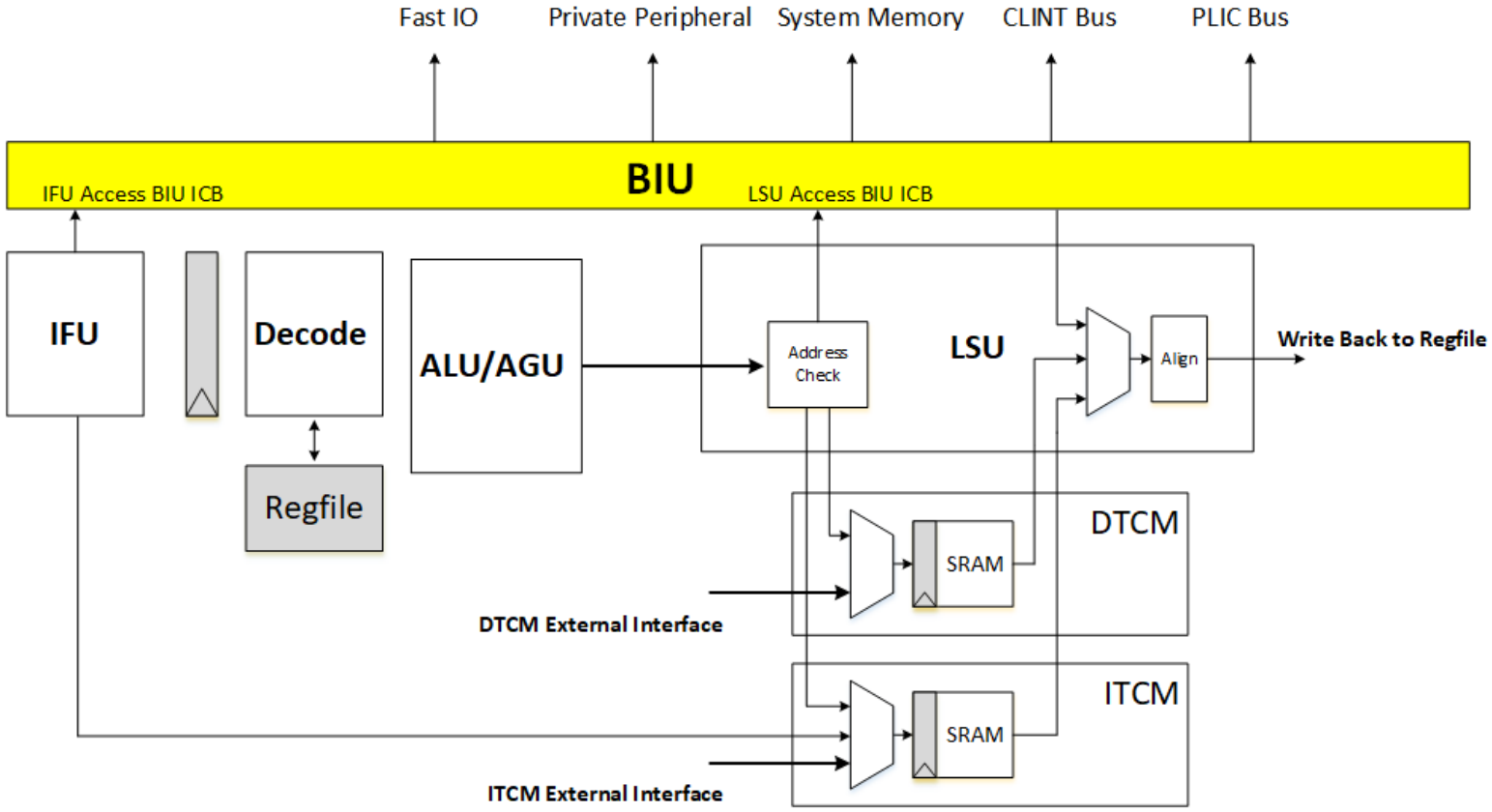
Details of Hummingbird E203 Core

Pipeline Details

- **Main Pipeline is two Stages**
  - Optimized for Area, timing and power



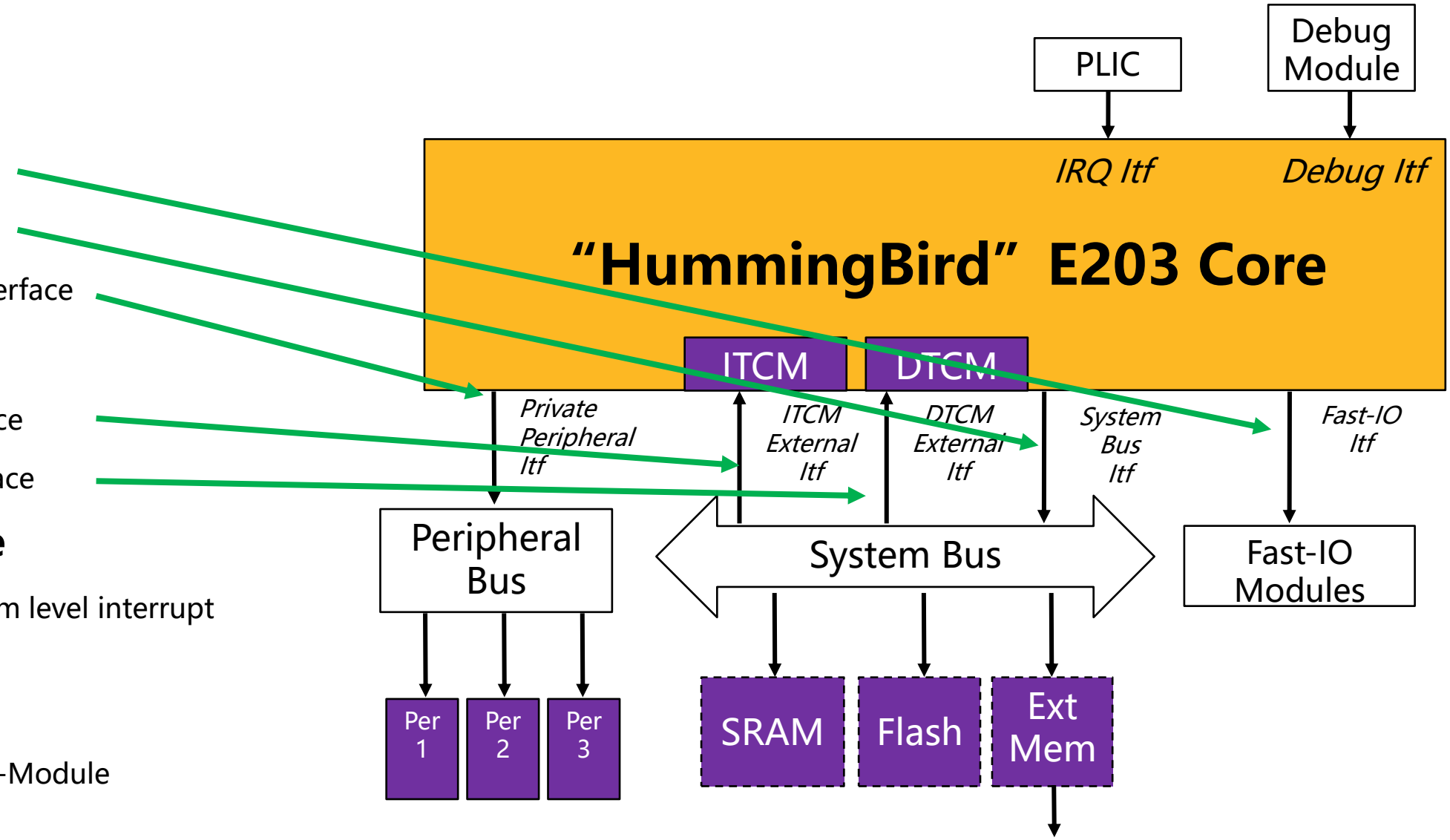


- ITCM and DTCM is integrated inside Core

Details of Hummingbird E203 Core

Interfaces

- **Master Interfaces**
  - Fast-IO Interface
  - System Bus Interface
  - Private Peripheral Interface
- **Slave Interface**
  - ITCM External Interface
  - DTCM External Interface
- **Interrupt Interface**
  - Interface with platform level interrupt controller
- **Debug Interface**
  - Interface with Debug-Module



Details of Hummingbird E203 Core

Comparison

- **Hummingbird E203 in Comparison with ARM Cortex M0/M0+**

	Cortex-M0	Cortex-M0+	Hummingbird E203
• **Dhrystone DMIPS/MHz**	• 0.84	• 0.93	• **1.23**
• **CoreMarks/MHz**	• 1.62	• 1.77	• **2.15**
• **Minimal Configuration（Gates）**	• 12K	• 12K	• **12K** (Typical Config 18K)
• **Pipeline Stages**	• 3 stages	• 2 stages	2 stages
• **Hardware Multiplier**	• Yes (Configurable for single-cycle or Multi-cycles implementations)		• Yes (Multi-Cycles Implementation)
• **Hardware Divider**	• No		• Yes (Multi-Cycles Implementation)
• **ITCM and DTCM**	• No embedded ITCM and DTCM, need customer to integrate by themselves		• **Provide embedded ITCM (64bits wide) and DTCM to easy customer**

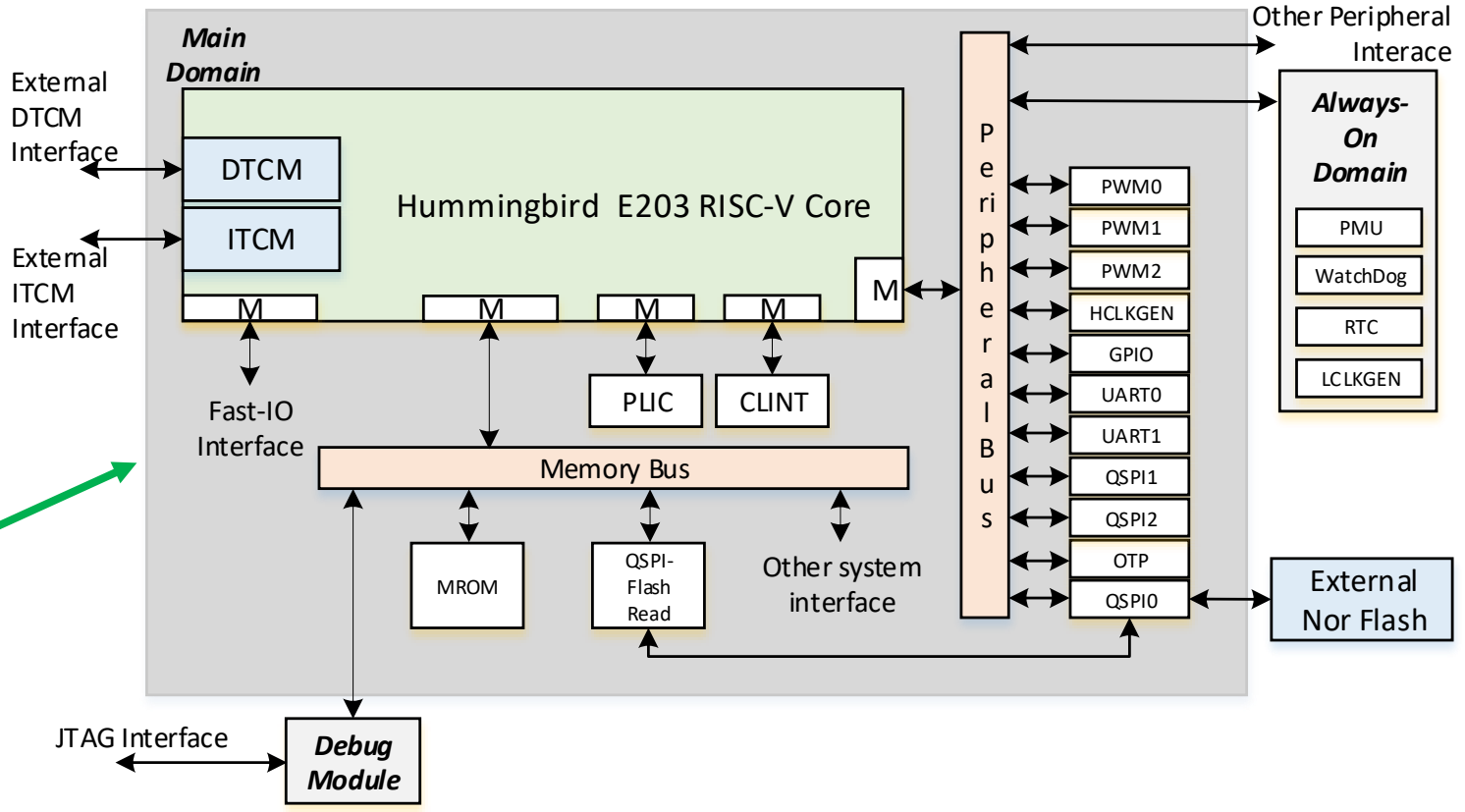
Note:

- **Besides open-sourced Hummingbird E203，there are commercial version （Nuclei N200 Series）which can contact Bob Hu by adding WeChat subscription number（微信公众号：硅农亚历山大）**

Details of Hummingbird E203 Core

Features

- **Instruction Set Architecture Features:**
  - Supporting architecture RV32IMAC
  - Supporting Machine Mode Only
  - Supporting Interrupts, PLIC, Timer
- **Highlighted Open-source Features**
  - Basic JTAG interactive debug support
  - Together with typical fully SoC open-sourced
  - FPGA demo supported with detailed doc
  - Embedded software SDK and demo provided



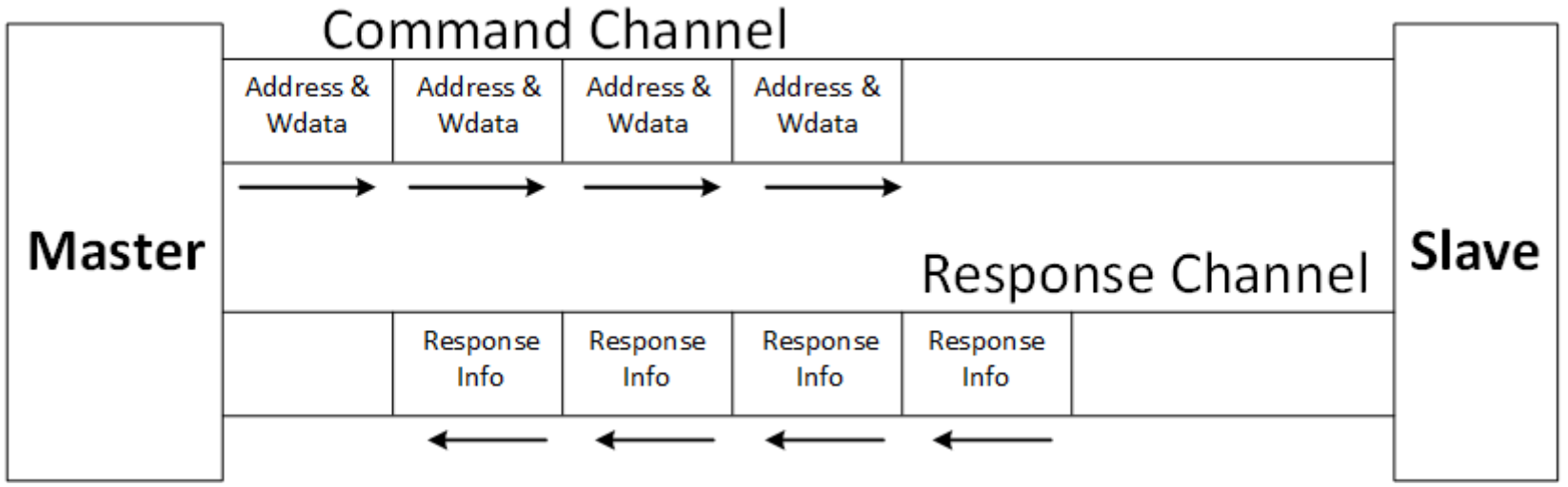
Note:

- **Will be introduced later with more details**

Details of Hummingbird E203 Core

Interfaces Protocol

- **The open-source version use Self-defined ICB interface**
  - Very simple, combined the merits of AHB and AXI, very easy to be converted to AHB/AXI/APB



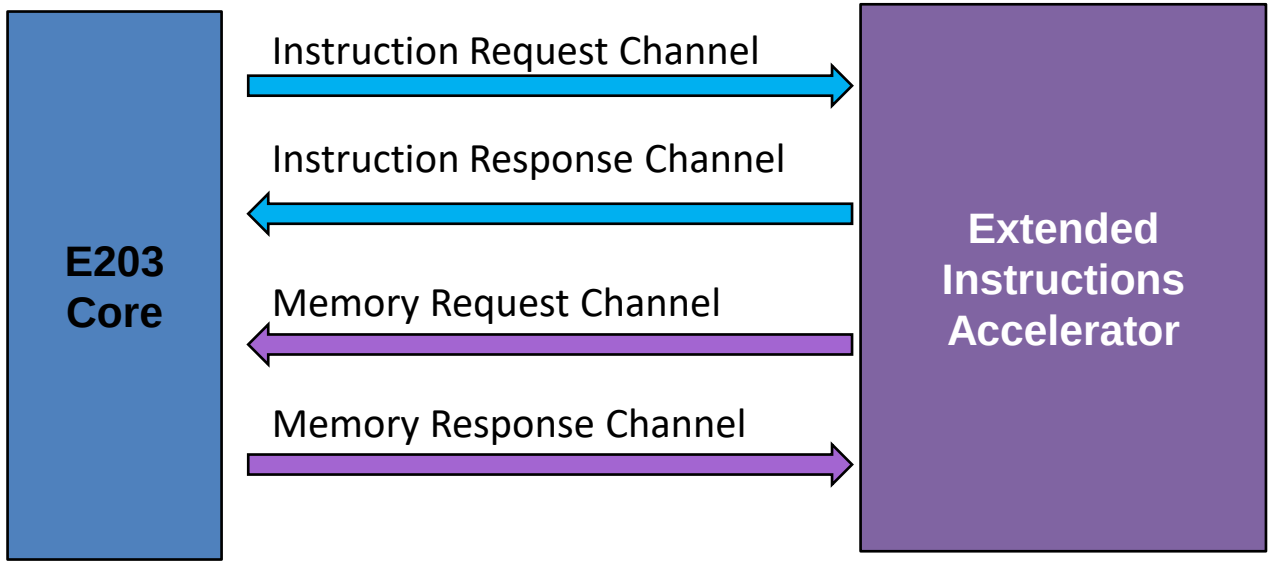
- **NOTE:**
  - The commercial version provide AHB/AXI/APB interfaces configurable

Details of Hummingbird E203 Core

Coprocessor Extension

- **The EAI (Extended Accelerator Interface)**
  - Four Channels protocol defined
  - Extended Instruction accelerator just need to follow the protocol
  - The extended Instructions can just use the reserved "custom" instructions inline into the C/C++ program, no need to change the compiler toolchain

Four-Channels Coprocessor Interface



- **NOTE:**
  - The EAI Interface is not yet open-sourced (the intern student is wanted)
  - The commercial version provide EAI

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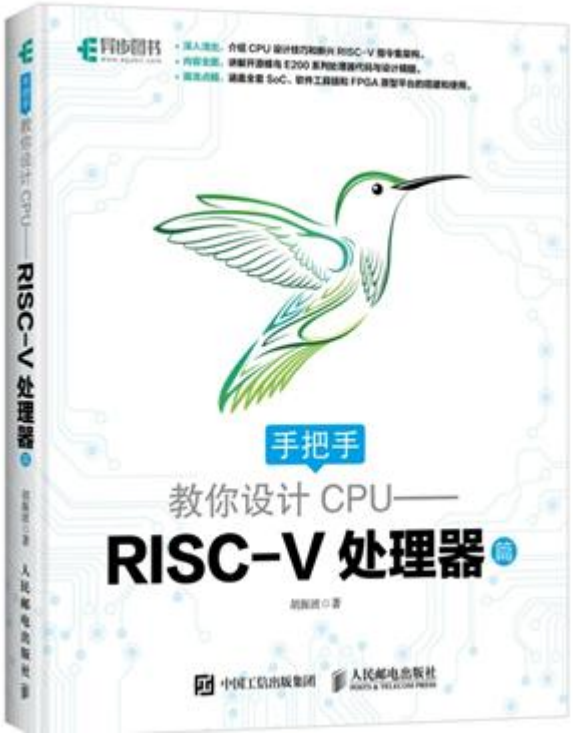
The Published 1st Chinese RISC-V Book

Contents of Book

- **All Other Detailed Information can be seen from the book**



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The Board for Hummingbird E203

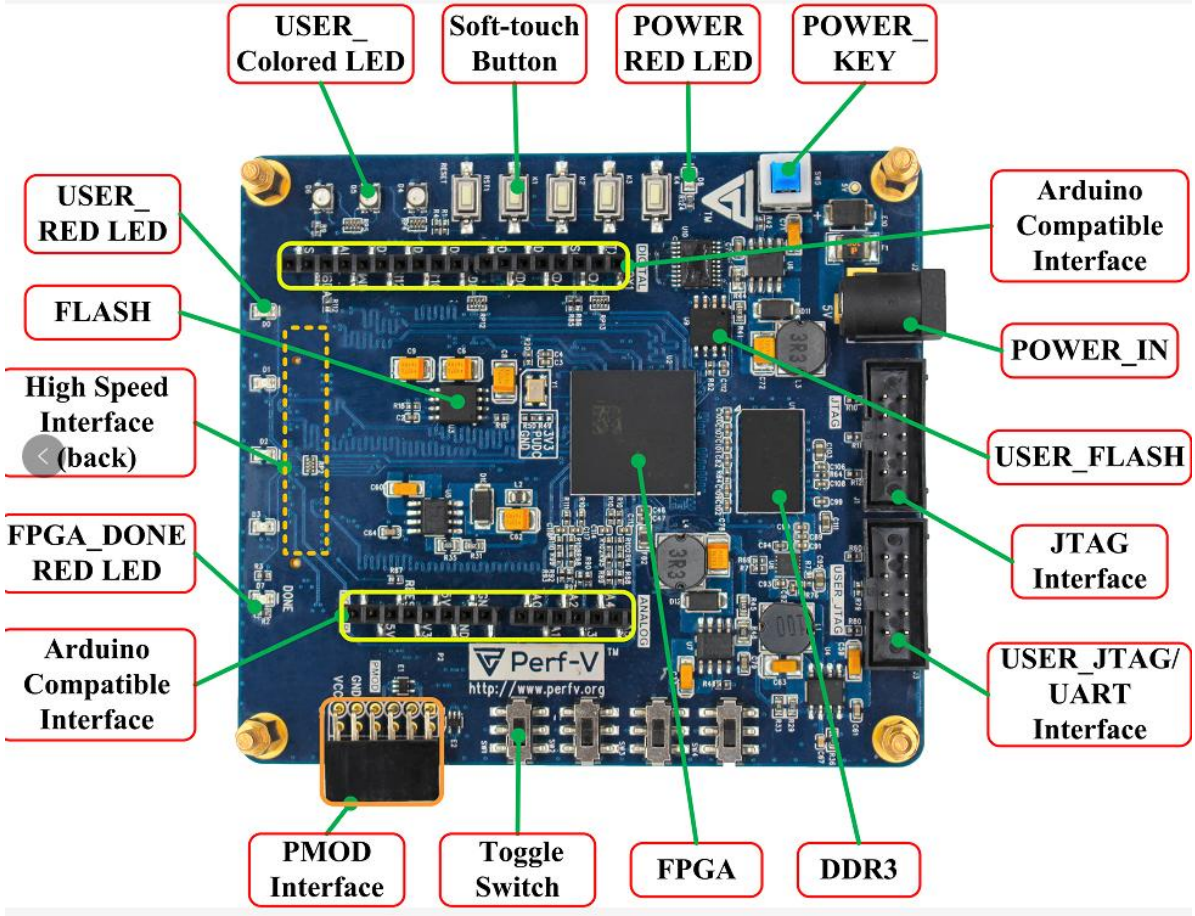
FPGA-based MCU Board

- **Xilinx FPGA based MCU Board（<399~1299RMB)**

Perf-V

PerfXLab

澎 峰 科 技



The Board for Hummingbird E203

FPGA-based MCU Board

- **Anlogic (上海安路) FPGA based MCU Board (<100RMB)**
- **PANGO (紫光同创) FPGA based MCU Board (<100RMB)**

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The next coming 2nd Chinese RISC-V Book

Contents of Book

- **The 1st book is to spread RISC-V by detailed introduction of E203 Core**
  - Targeting for hardware Chip designer
- **The 2nd book is to introduce how to use RISC-V for embedded software development**
  - Targeting the embedded software programmer
  - This is even more important because most of the people are the user, who are not interested into designing CPU but just using CPU
  - Will be firstly opened in the WeChat subscription number（微信公众号：硅农亚历山大）

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The Education Program for RISC-V

Education Program

- **Provide the trainings for beginners**
  - .....
- **Promote the open-source Hummingbird E203 into the Classroom of Chinese University**
  - With books
  - With boards
  - With the pre-designed class contents
  - Conduct the contests and club
  - ...
  - ...
  - Thinking very hard....  Need help.....
  - ....

Q & A

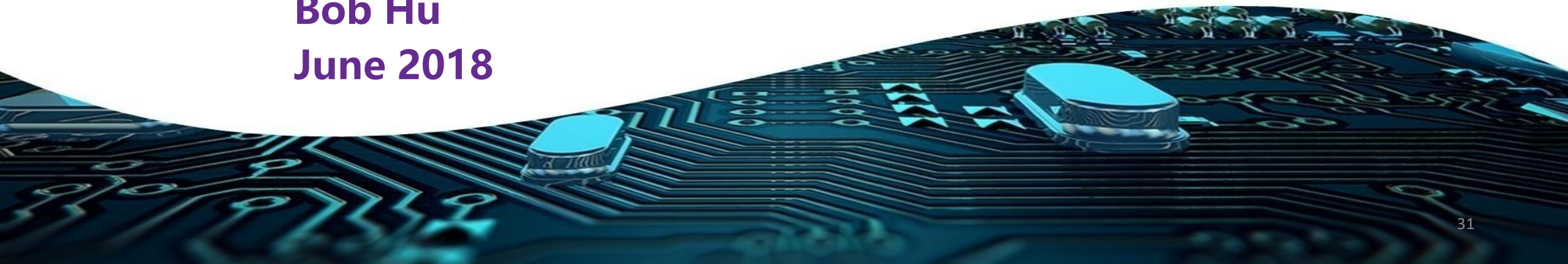
Thanks

NUCLEI
芯来科技(武汉)有限公司

Nuclei N200 Series
RISC-V Core IP Introduction

Bob Hu

June 2018



Company Introduction

- **Our Missions**
  - To be a RISC-V processor core vendor based on China Mainland
  - Enable Chinese semiconductor industry with RISC-V Core with China Mainland Domestic Autonomy（国产自主可控) and better local service

NUCLEI
芯来科技(武汉)有限公司

- **Business Scope**
  - RISC-V processor core IP licensing
  - RISC-V processor core and subsystem customization
- **Highlights**
  - Hummingbird E203 processor core with ultra low-area/power features, launched at 2017 (1st RISC-V from China Mainland) targeting to Deeply-embedded and IoT domains
  - Nuclei N200 series included the N203, N205, N207
  - The measured data from real silicon chip proved the better power consumptions over rival Cortex-M core
  - Perfect replacements to ARM Cortex-M processor cores with lower royalties

Nuclei N200 Overall Introduction

Low-power core with ICache to easy SIP with Nor Flash

N200 Processor Core Series

Replace ARM Cortex-M4F/M7 for double-precision floating-point

- **Nuclei N200 Series Features and Comparison**

	N203	N205	N205f	N205fd	N207
RISC-V Arch	RV32IMAC	RV32IMAC	RV32IMAFC	RV32IMAFDC	RV32IMAC
Hardware Multiplier/Divider	**Yes** • 17 cycle Multiplier • 33 cycles divider	**Yes** • 1 cycle Multiplier • 33 cycles divider			
Single-precision FPU	No	No	**Yes**	**Yes**	**Configurable**
Double-precision FPU	No	No	No	**Yes**	**Configurable**
ICache	No	No	No	No	**Yes**

Replace ARM Cortex M0/M0+

Replace ARM Cortex M0/M0+/M3

Replace ARM Cortex-M4F for single-precision floating-point

The Merits of Commercial Version

	E203 Open Source Version	N200 Commerical Version
• Full features of JTAG debugging	No	Yes
• Quality and Service Warrant	No	Yes
• Optimization of Area and performance	No	Yes
• Hierarchical Structure for Easier Intergration	No	Yes
• Standard AMBA Bus Interface	No	Yes
• Extending Interface for Co-Processors	No	Yes
• Dual Lines Debugging Interfaces	No	Yes
• Fast Vector Nested Intrrupt Controller	No	Yes
• Multiple-Privilege Levels and MPU	No	Yes
• Unaligned Load/Store handled by Hardware	No	Yes

Nuclei N200 Overall Introduction

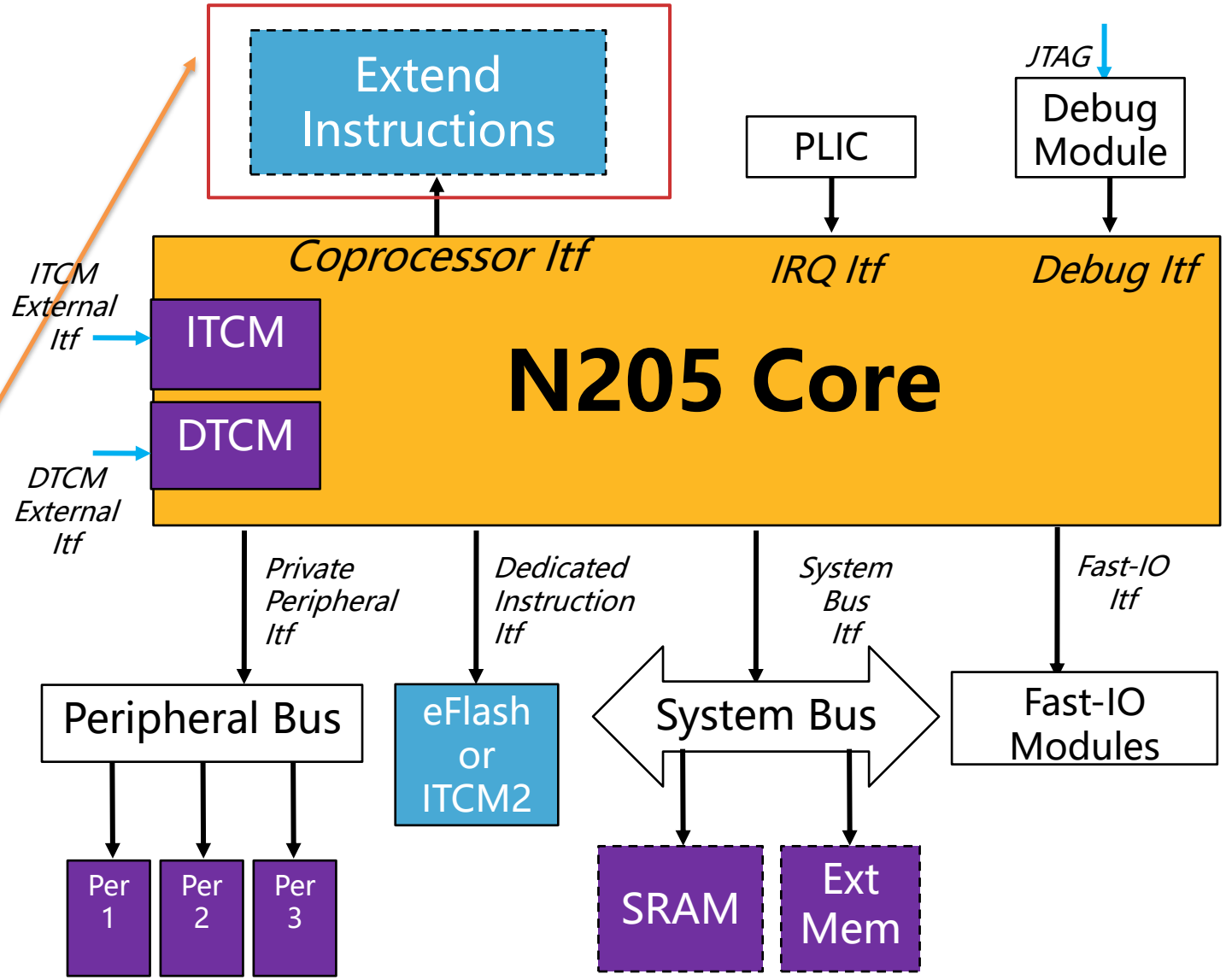
N200 Processor Core Series over ARM

- **Nuclei N200 Series in Comparison with ARM Cortex-M Series**

	Cortex-M0	Cortex-M0+	Cortex-M3	Cortex-M4F	N203	N205	N205f	N205fd	N207
Dhrystone DMIPS/MHz	0.84	0.93	1.25	1.25	**1.23**	**1.47**	**1.47**	**1.47**	**1.47**
CoreMarks/MHz	1.62	1.77	3.32	3.40	**2.15**	**3.36**	**3.40**	**3.40**	**3.36~3.40**
Minimal Config (Gates)	12K	12K	36K	90K	**12K**	**20K**	**60K**	**90K**	**Configurable**
Pipeline Stages	3 stages	2 stages	3 stages		2 stages	2 stages	2 stages	2 stages	2 stages
Hardware Multiplier	Yes (1-cycle or Multi-cycles)		Yes	Yes	Yes (Multi-cycles	Yes (1-cycle)	Yes (1-cycle)	Yes (1-cycle)	Yes (1-cycle)
Hardware Divider	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Single-precision FPU	No	No	No	Yes	No	No	Yes	Yes	**Configurable**
Double-precision FPU	No	No	No	No	No	No	No	Yes	**Configurable**
DSP Extension	No	No	No	Yes	Support user define and extendable				
Instruction Cache	No	No		No	No	No	No	No	Yes
ITCM and DTCM	No embedded ITCM and DTCM, need customer to integrate by themselves				**Provide embedded ITCM (64bits wide) and DTCM to easy customer**				
ECC protection to ITCM/DTCM	Need customer to implement by themselves				**Provide ECC protection to ITCM and DTCM**				
Extendibility	No				**Support user to extend instructions**				

Nuclei N205 Core Introduction

- **Features**
  - Based on 2 stage pipeline implementations
  - Area in rival to Cortex-M0+, performance in rival to Cortex-M3
  - Provided embedded Tightly Couple Memories ITCM and DTCM with ECC protection supported
  - Provide dedicated instruction interface to support eFlash or another ITCM2
- **Strengths**
  - **Support User-Expendability (e.g., user defined DSP operation)**
  - Perfect Replacement to ARM Cortex-M3
    - Better Performance
    - Smaller Areas
    - Lower Royalty Fees



Nuclei N207 Core Introduction

- **Features**

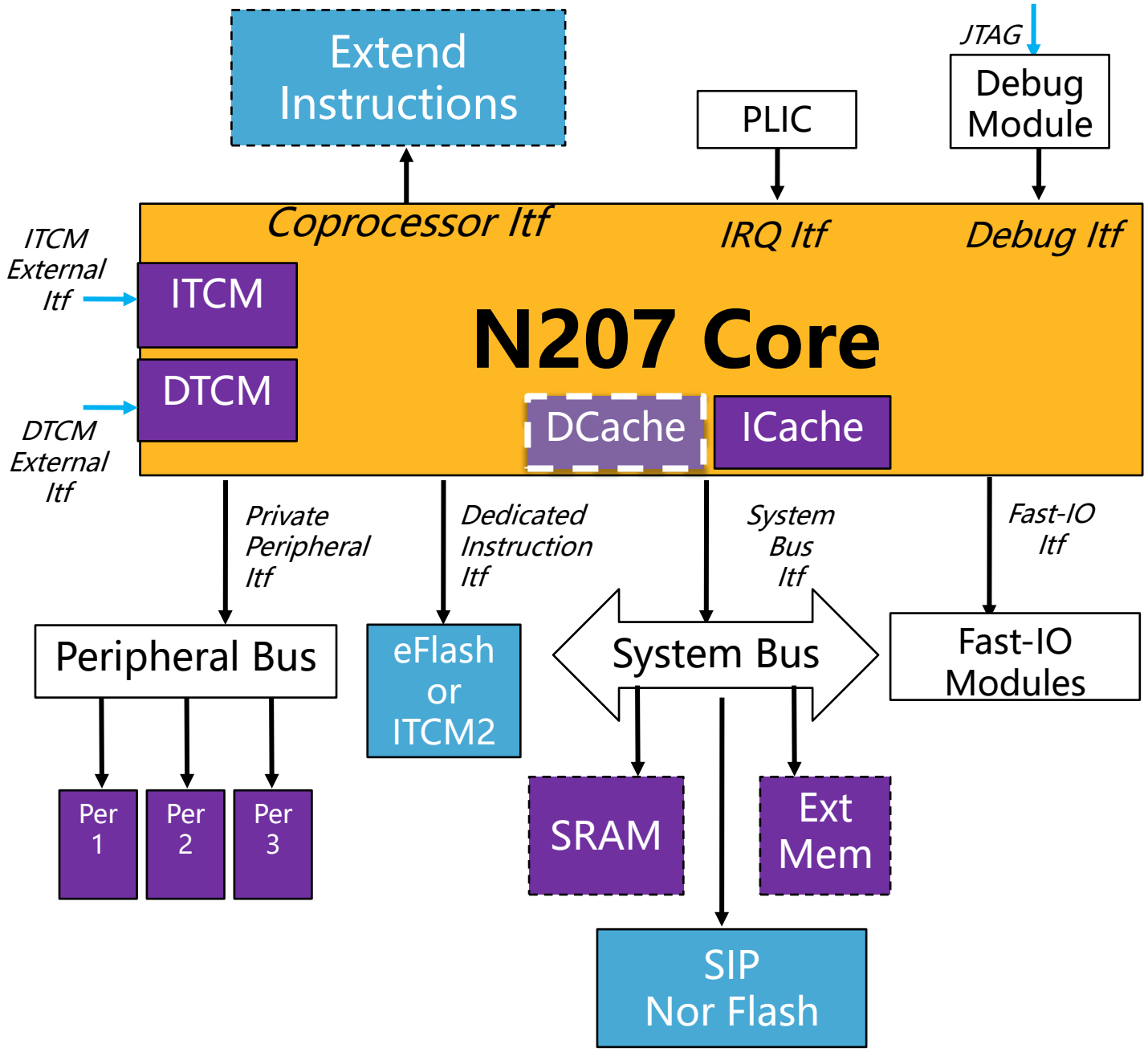
  In additional to N205 features:

  - Added ICache（2-Way，32Bytes Cache Line Size，Cache-Size configurable）
  - Added Configurable DCache（2-Way，32Bytes Cache Line Size，Cache-Size configurable）

- **Strengths**

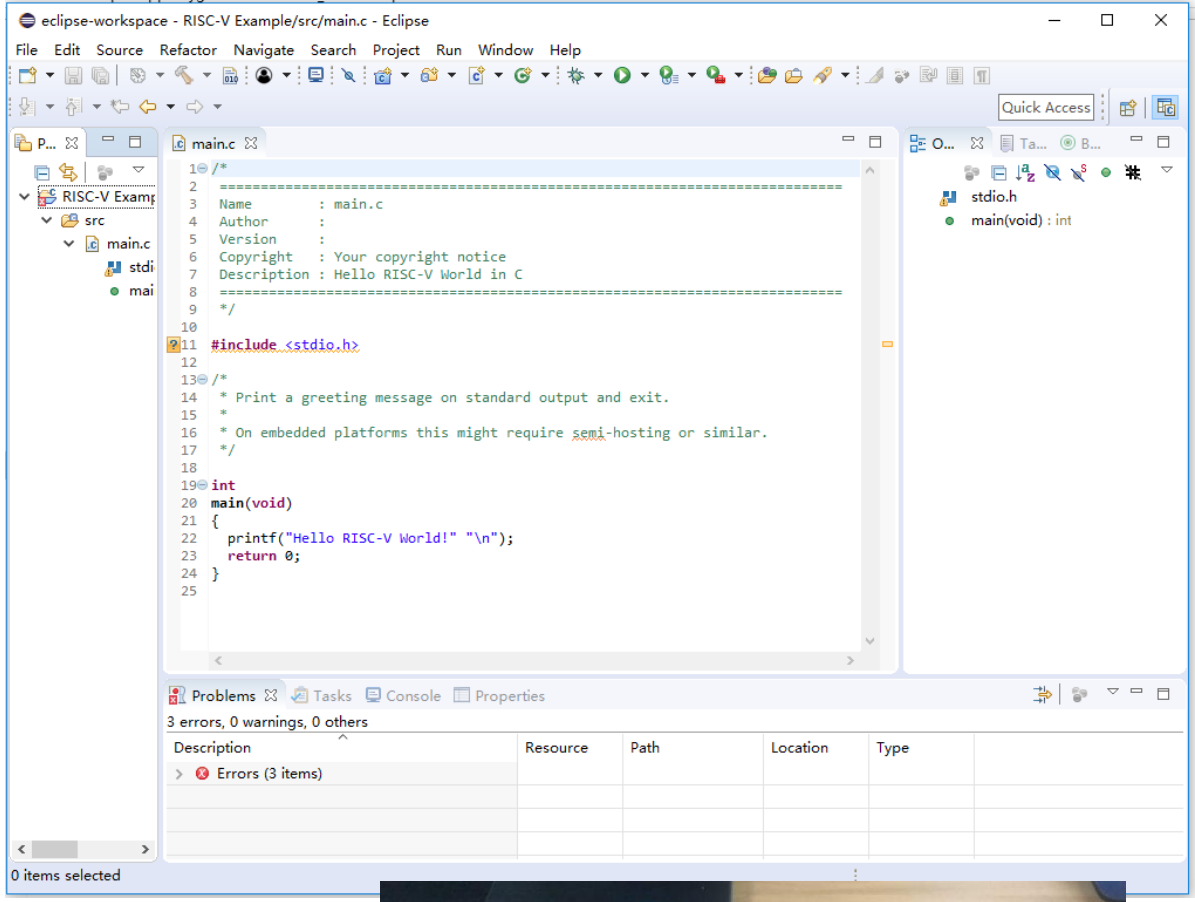
  In additional to N205 features:

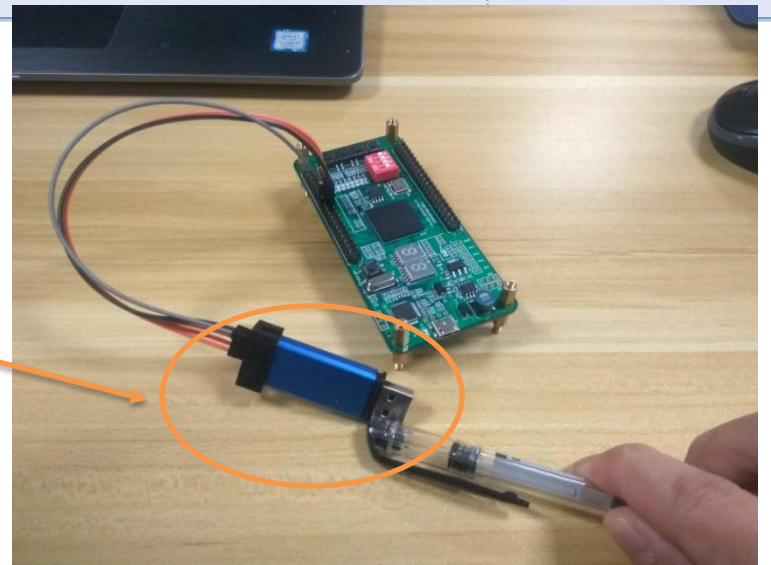
  - Utilize the ICache, use SIP package external Nor-flash, to reach better flexibility and cost
  - The ITCM size can be reduced, the eFlash can be eliminated to reduce die cost
  - Note：The critical instruction can still be put in on-chip ITCM (but with smaller size)



Tool-chain and Software Development Environment

- **C/C++ Compiler**
  - Standard GNU GCC Toolchain（with both Linux and Windows version）
- **Software Development Kit**
  - Hbird-E-SDK：based on GCC Toolchain
- **Windows and Linux IDE**
  - Eclipse C/C++ Development IDE
  - Note：utilize the whole RISC-V ecosystem，any IDE supporting RISC-V will support Hummingbird E200（because of standard ISA）
- **Software Simulation**
  - Based on QEMU
- **JTAG Debugger**
  - JTAG Debugger（USB-Disk size，Cost around 30 RMB）
- **RTOS Support**
  - FreeRTOS
  - RT-Thread
  - Note：utilize the whole RISC-V ecosystem，any RTOS supporting RISC-V will support Hummingbird E200（because of standard ISA）





Q & A

Thanks

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