FROM RESEARCH TO INDUSTRY

cea tech

PULSAR

Parallel heterogeneous and Low-power Smart ARchitecture

HETEROGENEOUS MULTICORE BASED ON RISC-V PROCESSORS AND FD-SOI SILICON PLATFORM

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Outline

Context

- THINGS2DO is a Pilot Line project funded by ENIAC
  - ENIAC is a public-private partnership in nanoelectronics strengthening European competitiveness and sustainability

- Objectives
  - Build a large ecosystem around FD-SOI in Europe
  - Develop IP and chipsets libraries for FD-SOI
  - Develop a complete high level FD-SOI design flow
  - Allow companies, including start-up to have access to FD-SOI foundries in a cost effective manner, for small or medium quantities
  - Show FD-SOI benefit on real demonstrators
  - Build design centers for FD-SOI

- More than 40 partners

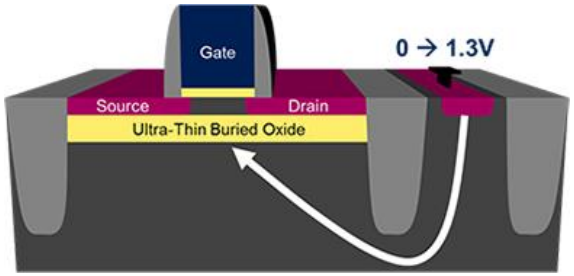
FD-SOI technology

What is FD-SOI?

©ST

FD-SOI advantages

- Reduce leakage
- Allow wide voltage range
- Is more fault tolerant
  - no possible latch-up
- Allow body-bias



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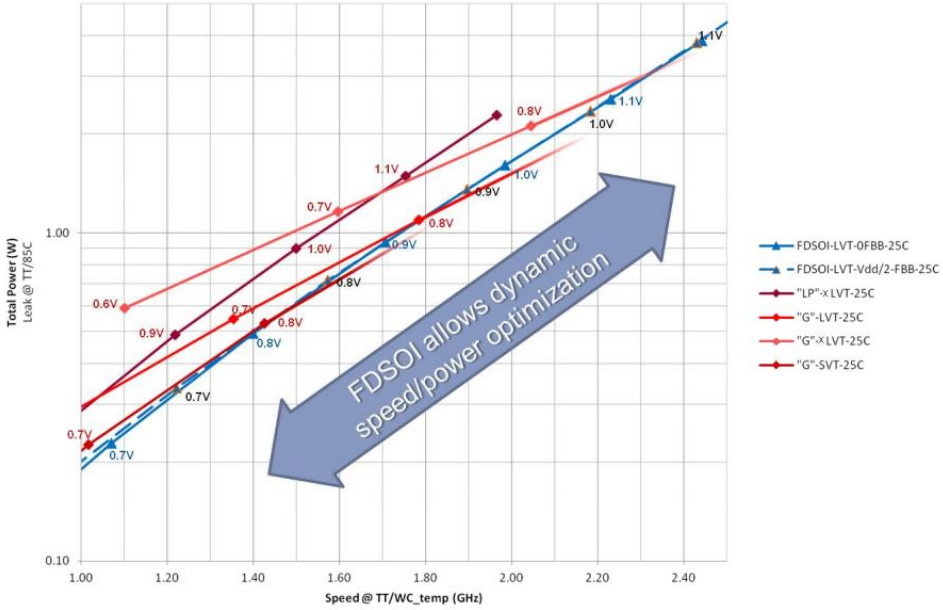


P. Flatresse, G. Cesana and X. Cauchy, "Planar fully depleted silicon technology to design competitive SOC at 28nm and beyond", ST, 2012

Outline

1 INTRODUCTION

2 PULSAR PLATFORM

3 SILICON IMPULSE

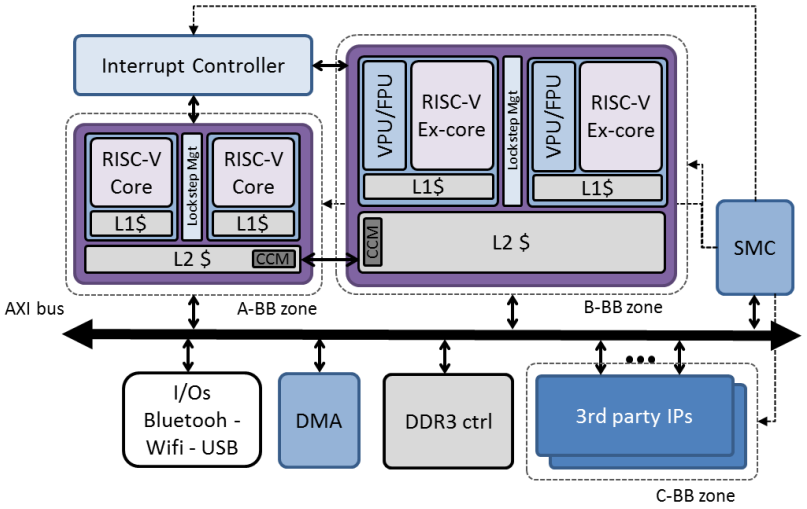
4 CONCLUSION

PuLSAR

- A RISC-V big.LITTLE heterogeneous multicore
  - Two « small » cores
    - Rocket without FPU
    - 8KB L1 caches
  - Two « big » cores
    - 3-way superscalar BOOM
    - 32KB L1 caches
  - L2 cooperative caching
  - Instructions monitor (ROCC)
- AMBA interconnection
  - Generated by Synopsys CoreAssembler
  - AXI4 + AHB + APB network
  - I2C, UART and timers peripherals
- Multiple body-bias zones
- Smart monitoring
  - AntX processor
  - Non-functional parameters management
    - Performance, ageing, power consumption, temperature

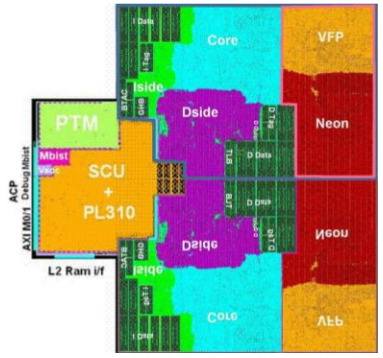
RISC-V

PuLSAR
Parallel heterogeneous and Low-power Smart ARchitecture



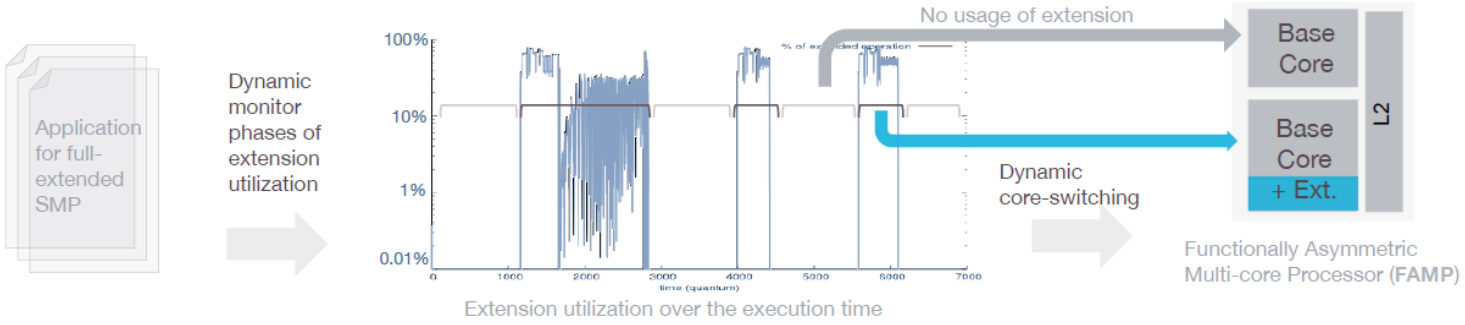
Dynamic management of FAMP

- In SMP architectures, extensions accelerate some specific tasks from 4x to 1000x
  - But are used less than 5% of time
  - May consume up to 25% of the processor area



CORTEX A9 dual core Floorplan
From Osprey – 1.9W TDP 2GHz (6.7mm2)

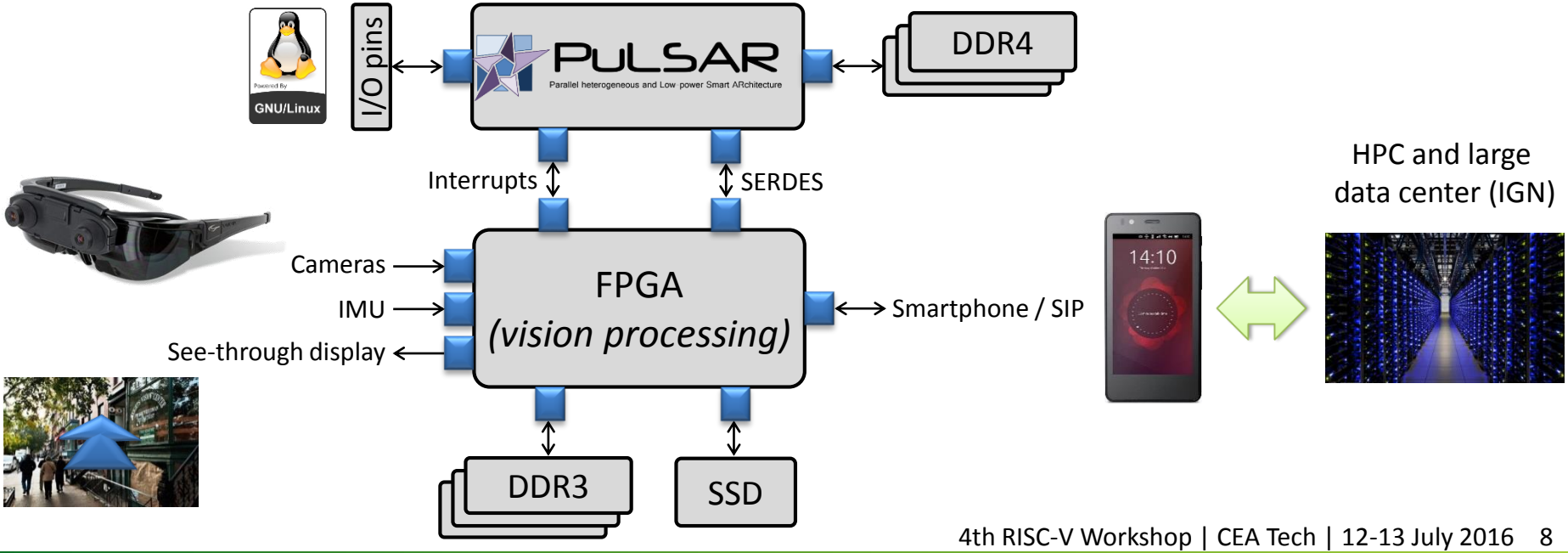
- Functionally Asymmetric Multicore Processor (FAMP)
  - Objectives
    - Maintain a reduced silicon area
    - Limit performance degradation
    - Reduce the energy consumption
  - Techniques
    - By limiting the use of costly extensions for critical sections
    - By optimizing task placement according to performance



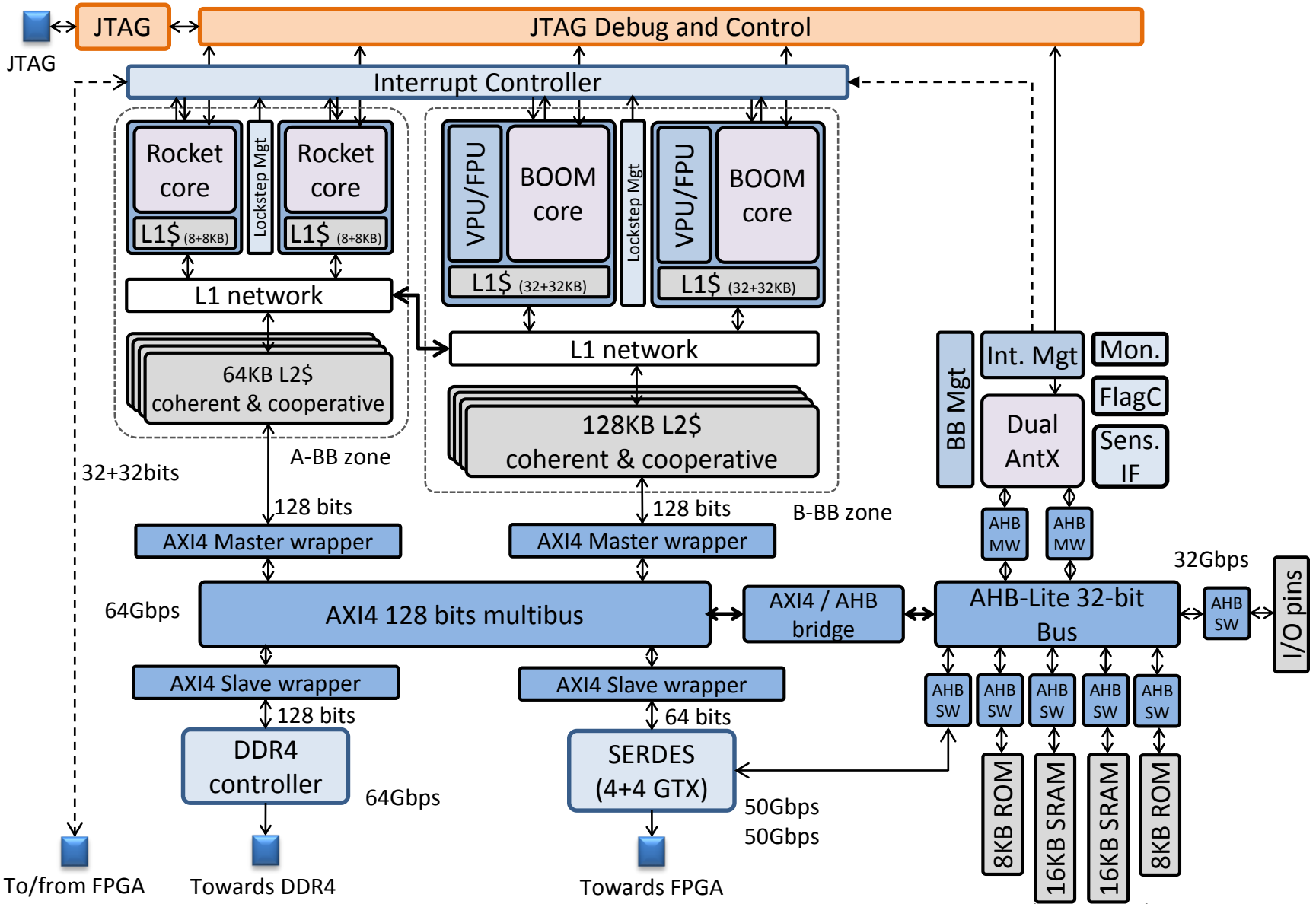
Extension utilization over the execution time

PuLSAR context

- Pedestrian navigation system
  - Composed of a System-on-Glasses (SOG) and a System-in-Pocket (SIP) (e.g. smartphone)
  - Display augmented reality by using accurate positioning data from the IGN datacenter
- SoG architecture
  - SoC: PuLSAR
  - FPGA: dedicated video processing and high-bandwidth connection to peripherals
  - Peripherals: Stereoscopic cameras, inertial measurement unit and see-through display

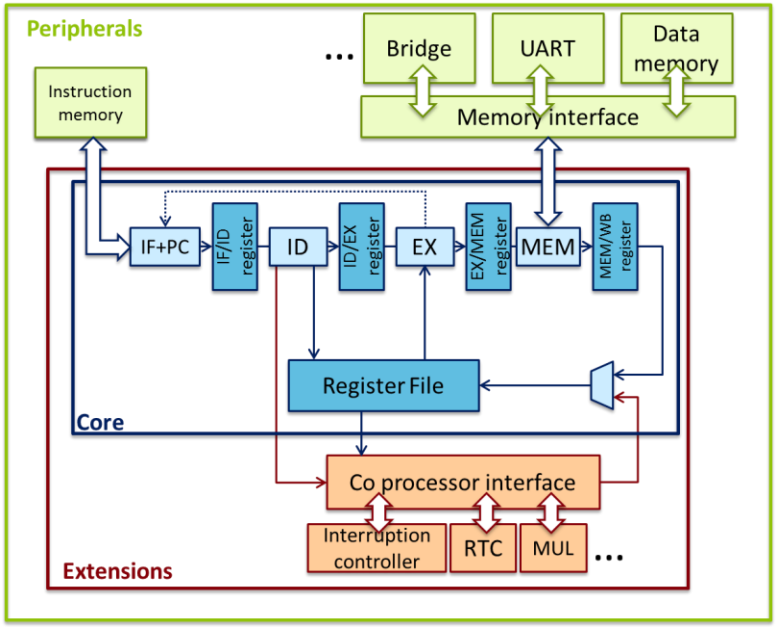


PuLSAR SOC architecture



AntX processor

- CEA Tech tiny processor
  - 32-bit RISC Harvard architecture
    - 70 instructions, 16-bit and 32-bit
    - Small memory footprint
  - Mono-thread, in-order pipeline, 16 registers (32 bits)
  - 5 stages (fetch, decode, execute, memory, write-back)
  - Cache memories (optional), AHB interface
  - Coprocessor (optional)
    - ~4096 coprocessor instructions
    - e.g.: IT controller, 2-cycle multiplier...
    - Body-bias control unit
- Full SDK
  - GCC, binutils, C standard lib, C++
  - SystemC simulator



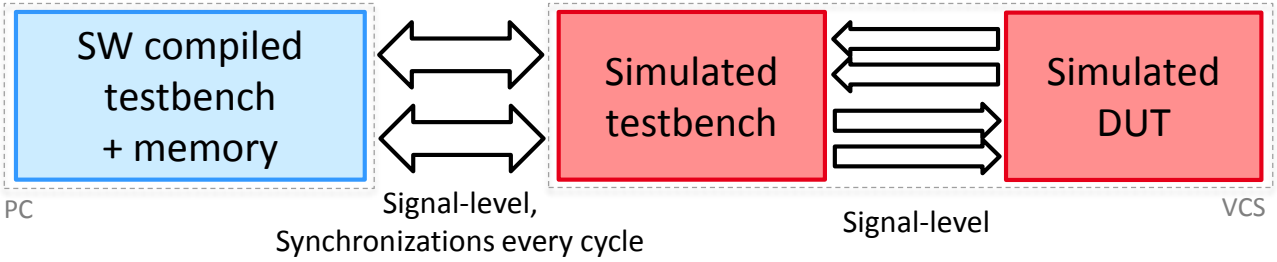
Verilog RTL simulation

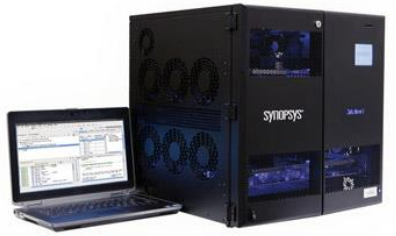
- Designed RTL
  - Pass ISA & benchmark tests
  - Boot Linux
- Quite easy design space exploration with Chisel
  - Number and type of cores, cache sizes, accelerators…
- However, RTL simulations are very long
  - VCS or ModelSim run the design at only few kHz
  - Benchmark tests need minutes to hours depending on the number of cores
    - Booting Linux requires few hours before reaching ash (for four cores)

  ⇒ Impossible to run and debug applications under Linux with through Verilog RTL simulation
- Spike?
  - Not accurate enough for benchmarking and architecture exploration
  - Not completely same as hardware (heterogeneous, custom modifications?)

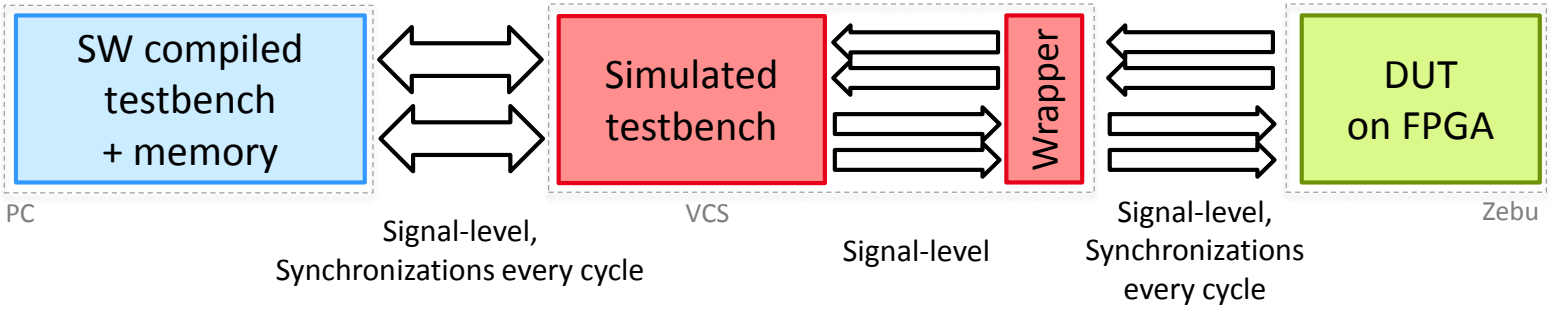
Hardware emulation with Zebu

- Rocket chip base RTL simulation flow

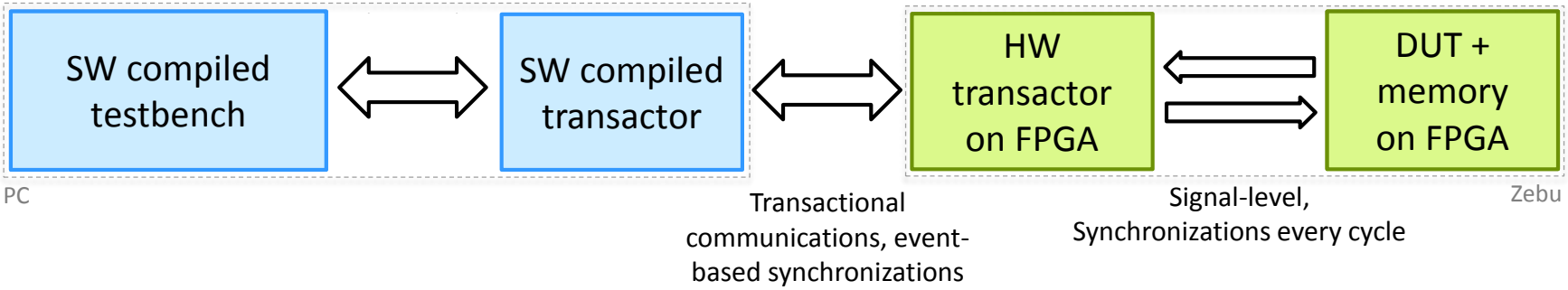




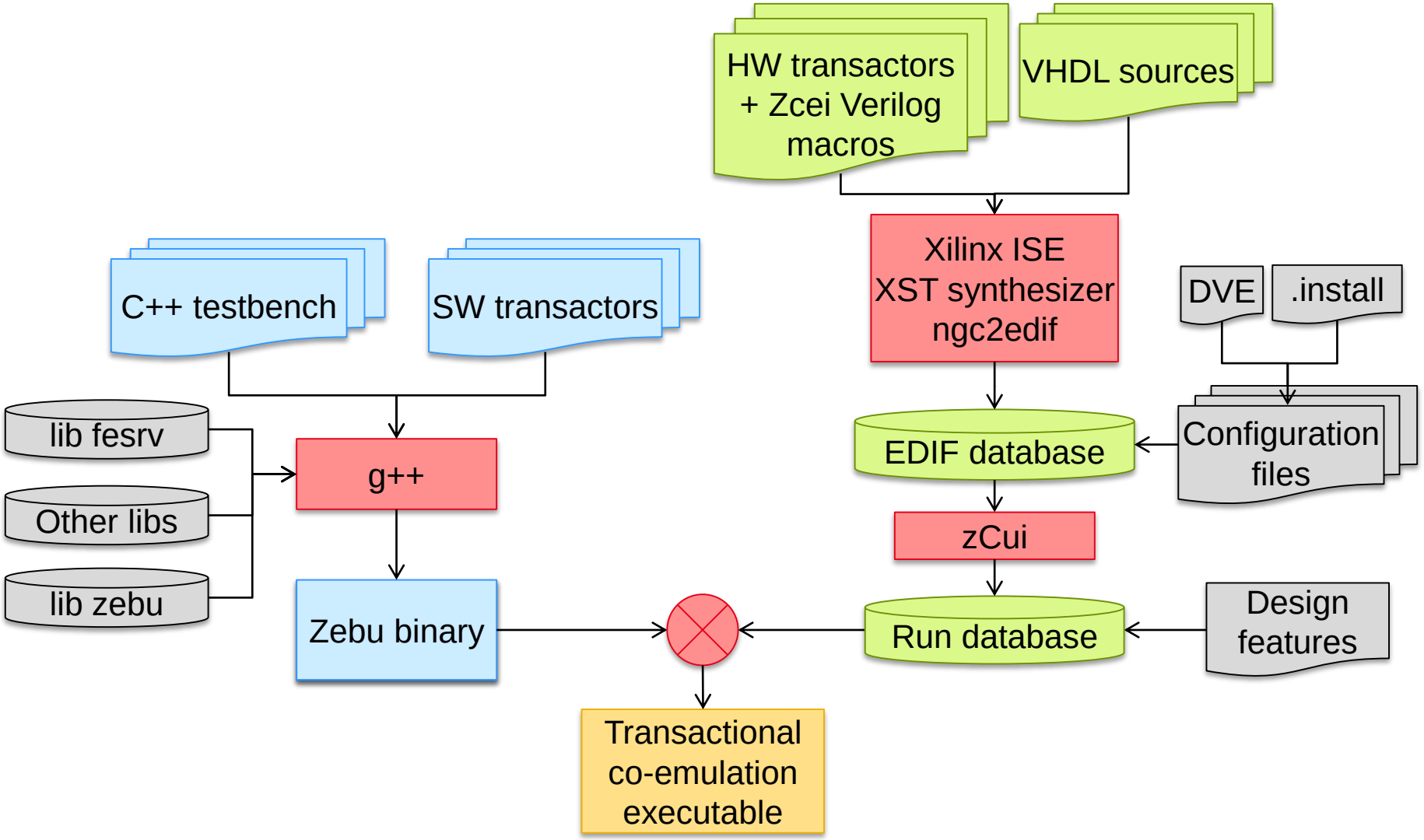
- Signal based co-emulation



- Transactional based co-emulation



Transactional co-emulation flow



Emulation performance

- Achieved performance
  - FPGA clock ~ 7MHz
  - Linux boot ~140s
- Still possible to create waveform and check register states!
- BBL changes
  - Add the number of cores in the implementation registers

  ⇒Remove spike/QEMU dependency

  - Always catch float errors

  ⇒Soft float

Emulation performance (cont'd)

- Minor change to Linux cpuinfo
  - Display real core ISA
- Run swaptions under Linux from PARSEC [1]
  - Promising results
  - Still some library problems for other benchmarks

```
# cat /proc/cpuinfo
hart    : 0
isa     : RV64IMA
        I: Base Integer Instruction Set
        M: Integer Multiplication and Division Standard Extension
        A: Atomic Instructions Standard Extension

hart    : 1
isa     : RV64IMA
        I: Base Integer Instruction Set
        M: Integer Multiplication and Division Standard Extension
        A: Atomic Instructions Standard Extension

hart    : 2
isa     : RV64IMAFD
        I: Base Integer Instruction Set
        M: Integer Multiplication and Division Standard Extension
        A: Atomic Instructions Standard Extension
        F: Single-Precision Floating-Point Standard Extension
        D: Double-Precision Floating-Point Standard Extension

hart    : 3
isa     : RV64IMAFD
        I: Base Integer Instruction Set
        M: Integer Multiplication and Division Standard Extension
        A: Atomic Instructions Standard Extension
        F: Single-Precision Floating-Point Standard Extension
        D: Double-Precision Floating-Point Standard Extension
```

[1] C. Bienia, "Benchmarking Modern Multiprocessors," Princeton University, 2011

SESAM: virtual prototyping

- A multicore VP framework based on SystemC/TLM 2.0
  - Accept third-parties ISS
    - QEMU, GenIssLib, ArchC…
- Fast and multi-host architectural exploration
  - Performance, energy consumption, temperature
  - Fault-injection , reliability/ageing
- Fast and adaptable accuracy
  - 3 to 1000 MIPS
  - Up to 90% accurate compared to RTL
- Multicore non-intrusive debugging
- Large set of HW IPs
  - NoCs, caches, DDR3 controller…
- Multi-level HW description
  - C/C++, TLM, RTL, SystemC, VHDL…
  - Support co-simulation with 3rd party-tools
  - Support co-emulation with HW emulators

Scale: parallel SystemC kernel

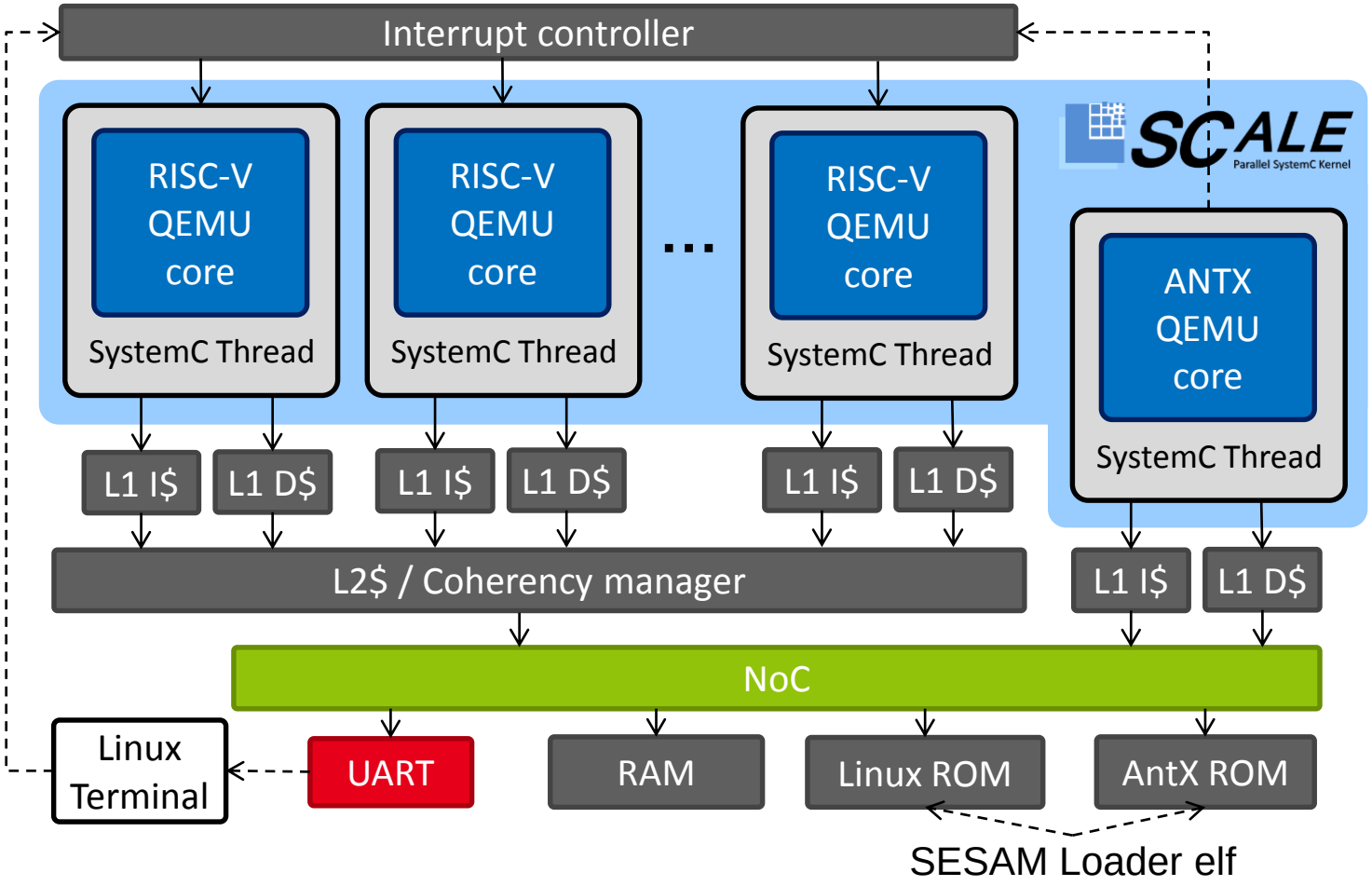
- SCale: A new parallel SystemC kernel
  - Compliant with Accellera standards
    - TLM, TLM2.0, SystemC 2.3.1
  - Supports multiple parallel architectures
    - Tilera64, AMD Bulldozer, i7…
  - Published at DATE 2016

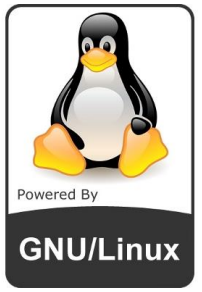
SCALE
Parallel SystemC Kernel

*Up to **x34** on 64 x86 cores*

- Main Foundations
  - Parallel and deterministic
    - Online conflict checking mechanism, repeatable simulations...
  - Can be used with any VP environment / easy to integrate
    - No structural modeling or usage limitation
      - Support RTL / TLM simulations (LT, AT)
    - SystemC models can use any communication layers
      - TLM, DMI, global variables or SystemC channels

PuLSAR virtual prototype





Synthesis results

- FD-SOI libraries
  - Core 12 LL, typical, 0.90V, 25°C for the quad core design
  - SPReg/DPReg, typical, 0.90V, 25°C for L1 & 256 KB L2 caches
- 2.64mm², 0.6W, 700MHz

Criteria	Design without caches	Caches Memories	Total
Design area (mm²)			2.64
Combinational	0.435	-	0.435
Non Combinational	0.442	1.77	2.21
Power (mW)			621
Internal	421	190	611
Leakage	9.4	< 1	10

Outline

From concept to prototype or product

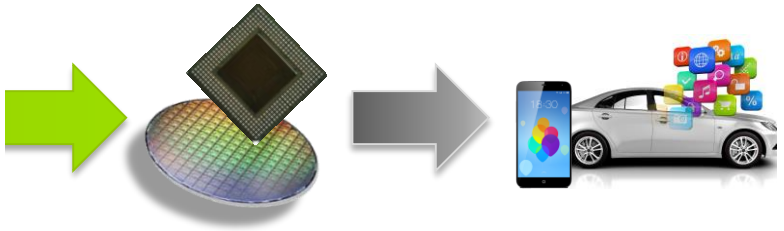
Industrials

Ideas & needs

SILICON IMPULSE

Prototype

Innovative product



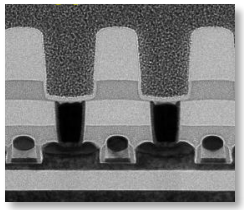
Easy access to advanced technologies and R&D skills

Inclusion into partner ecosystem

Help you to access CEA Tech advanced technologies mainly Ultra Low Power technology

Focus on FD-SOI technologies

- CEA Tech is a pioneer in FD-SOI technology development
- CEA Tech has been a key contributor to the FD-SOI process development from its onset
- Silicon Impulse helps FD-SOI adoption by developing the ecosystem
- Unique expertise in design flow and IP offering to leverage the advantages of FD-SOI guaranteeing success



FD-SOI is our DIFFERENCIATOR

Targeted applications

MICRO-SERVER

Energy efficiency

CONSUMER

Ultra-Wide Voltage range operation

IOT

Effective Analog/RF integration

Automotive, Space

Reliability & robustness

Help COMPANIES LAUNCH innovative products powered by leading edge design solutions

Business model

From concept to production ramp-up

SILICON IMPULSE

CONSULTING

- Feasibility analysis
- System architecture
- Solution evaluation
- Benchmarking
- Trainings

DESIGN

- IP Development
- Circuit Design
- System Design

PROTOTYPING

- MPW Shuttle
- Assembly
- Test

PRODUCTION RAMP-UP

- Qualification
- Transfer to foundry
- Supply Chain

PRODUCTION

- (foundry)

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Silicon Impulse can help EVERY step of the way

In-house industrial tools

Automated 12'' Wafer Sort

Mentor -Veloce 2 (240Mgate capacity) and Synopsys-EVE Emulation Platform

Verigy 93K Tester Platform (ATE) with Mixed Signal and RF extensions

Industrial equipment from emulation to test

Pick & Place Handler

Silicon Impulse partners

Foundries

GLOBAL FOUNDRIES

life.augmented

cmp

IP vendors

SYNOPSYS®

invecas

Design houses

DOLPHIN INTEGRATION

EASii IC

Supply chain

PRESTO Engineering

DOLPHIN INTEGRATION

Emulation

Mentor Graphics®

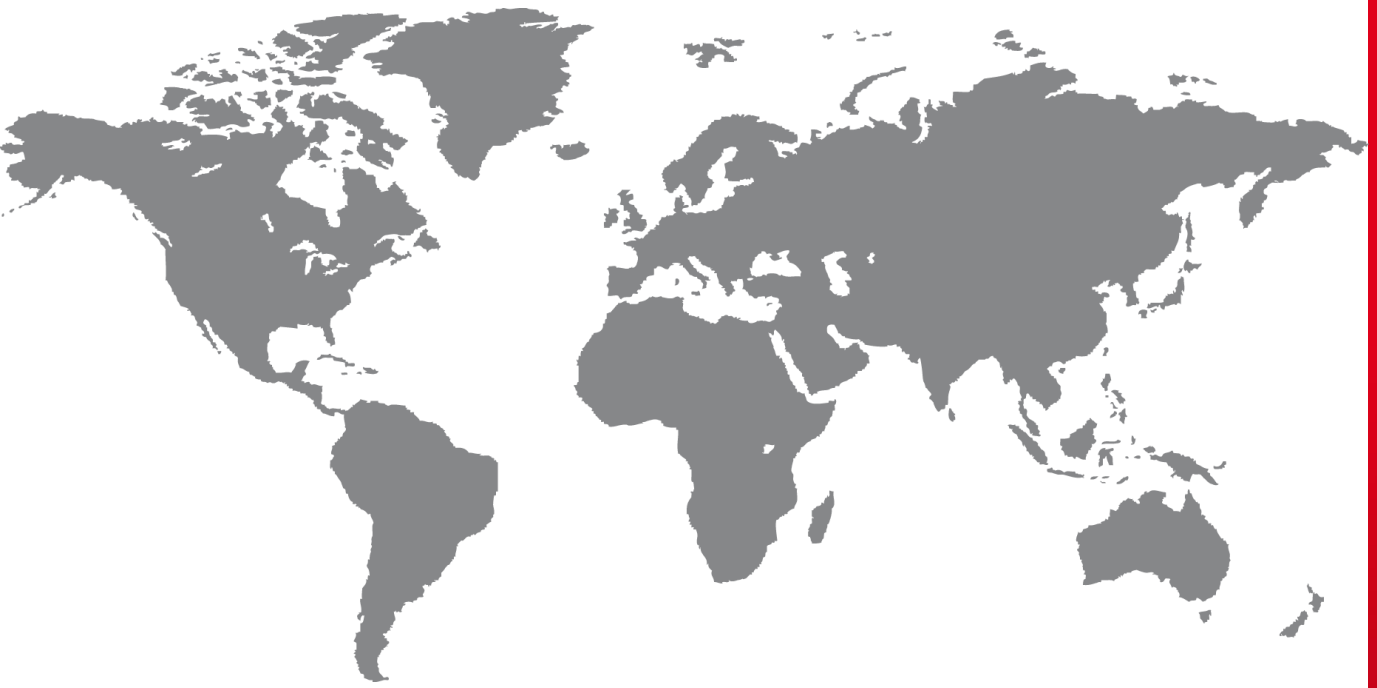
Embedded solution

list cea tech

A collaborative platform

Conclusions

- PuLSAR
  - Development of an heterogeneous platform based on RISC-V
  - Fast software and hardware development/test capabilities
  - Fast virtual prototyping platform based on QEMU
  - Encouraging FD-SOI 28 nm syntheses
- Silicon Impulse
  - An IC gateway between R&D and Industry
  - Early access to advanced technologies
    - Leverage the advantages of FD-SOI
  - A one stop-shop platform from a concept to its production ramp-up
- Next steps
  - Cooperative cache and lockstep mechanisms
  - Hardware debug capabilities (e.g. JTAG)
  - Advanced FAMP management in Linux
  - Complete PuLSAR virtual prototyping platform in SESAM



THANK YOU!

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