DESIGN DOCUMENTATION

(DOCUMENT 2)

CS/ECE 6710 DIGITAL VLSI DESIGN

GROUP 5

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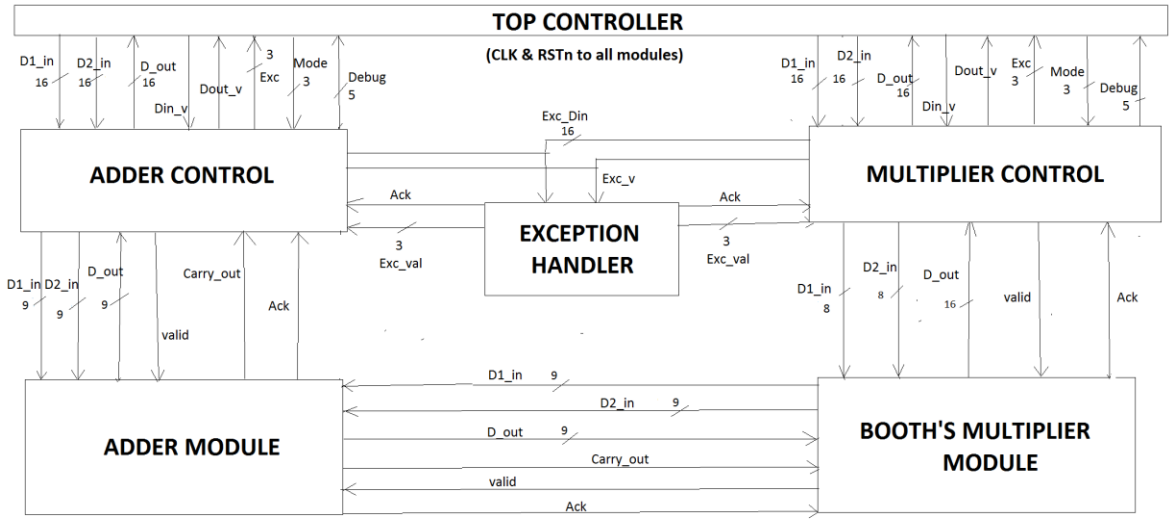
Block diagram

This section describes the block diagram of the 16 bit implementation of Floating point unit



The top controller forms the interface with the external master. Once the top controller has received instructions about operation type(addition/multiplication)and data from the master, it routes the data (D1_in,D2_in) to the respective modules for addition or subtraction. If the adder unit is busy, but the multiplier is idle, it can still accept multiplication request from the external master. The mode bits are also passed on to the individual controllers for configuring them for passing data while in debug mode. As the figure illustrates, the exception checker module and the 9bit adder unit are shared by the Booth multiplier and the Adder controller. The sharing mechanism is controlled by a 2bit priority arbiter . The booth while accessing the adder unit can use the adder unit a maximum of 8 times. If any addition request arrives from the Adder_controller, the priority arbiter helps it to capture cycle in between to complete its computation, thus disallowing the booth access to become greedy. A similar arbitration mechanism is placed for the exception checker access.

System Verilog code for individual modules

https://github.com/arnabd88/FPU/tree/master/16bitdesign
Code Directory: /home/arnabd/Semester1/DVLSI/Cadence-f15/Project/FPU/16bitdesign

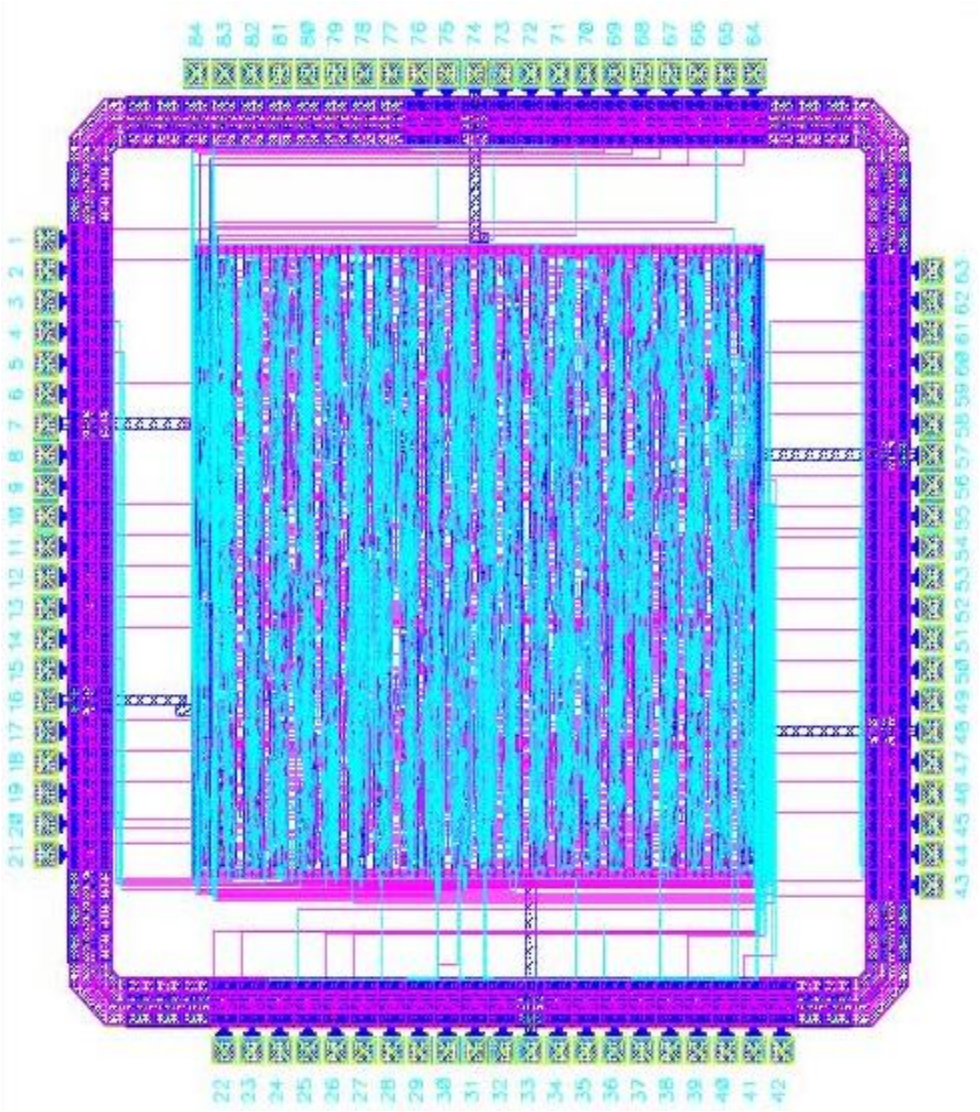
Library directory: /home/arnabd/Semester1/DVLSI/Cadence-f15/Lib6710_05
Project Directory: /home/arnabd/Semester1/DVLSI/Cadence-f15/ProjectFinal
Top level cell name: wholechip

Synthesis results details

The design was synthesized using design compiler with AMI 0.5um process standard cell library at a frequency of 50Mhz. The synthesis results are summarized below

CLK = 50Mhz	SYNTHESIS RESULTS	
	Slack	0.01 ns
	Combinational Area	629985.614105
	Total Cell Area	999021.605927
	Combinational Cells	725
	Sequential Cells	198
	Cell Internal Power	30.5925mW (97%)
	Net Switching Power	947.0820uW (3%)
	Total Dynamic Power	31.5396mW
	Cell Leakage Power	194.5735mW
	Critical Path	u_adder_cntrl/Final_Mantissa_reg_reg_1_ -> u_adder_cntrl/Final_Exponent_reg_reg_7_

Full chip routed design



The edi place and route was executed on the full design and not separately on individual modules. Hence, the floorplan of our design is just the core of the chip shown above. CCAR was only used for the pad connections.

Place and Route timing analysis

This section shows the timing analysis reports obtained from place and route using encounter.

Pre-CTS timing report

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.111  |  0.111  |  5.901  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   364   |   335   |   364   |
+--------------------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |    0.000    |      1 (1)       |
|   max_tran     |      2 (2)       |   -0.004    |      2 (2)       |
|   max_fanout   |      0 (0)       |      0      |      0 (0)       |
|   max_length   |      0 (0)       |      0      |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 59.595%
Routing Overflow: 0.00% H and 14.14% V
------------------------------------------------------------
```

Post-CTS timing report

```
------------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.088  |  0.088  |  6.901  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   364   |   335   |   364   |
+--------------------+---------+---------+---------+

+----------------+--------------------------------+------------------+
|                |              Real              |       Total      |
|    DRVs        +------------------+-------------+------------------|
|                |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+----------------+------------------+-------------+------------------+
|   max_cap      |      0 (0)       |    0.000    |      0 (0)       |
|   max_tran     |      2 (2)       |   -0.004    |      2 (2)       |
|   max_fanout   |      0 (0)       |      0      |      0 (0)       |
|   max_length   |      0 (0)       |      0      |      0 (0)       |
+----------------+------------------+-------------+------------------+

Density: 61.037%
Routing Overflow: 16.81% H and 38.26% V
------------------------------------------------------------------
```

Post-route timing report

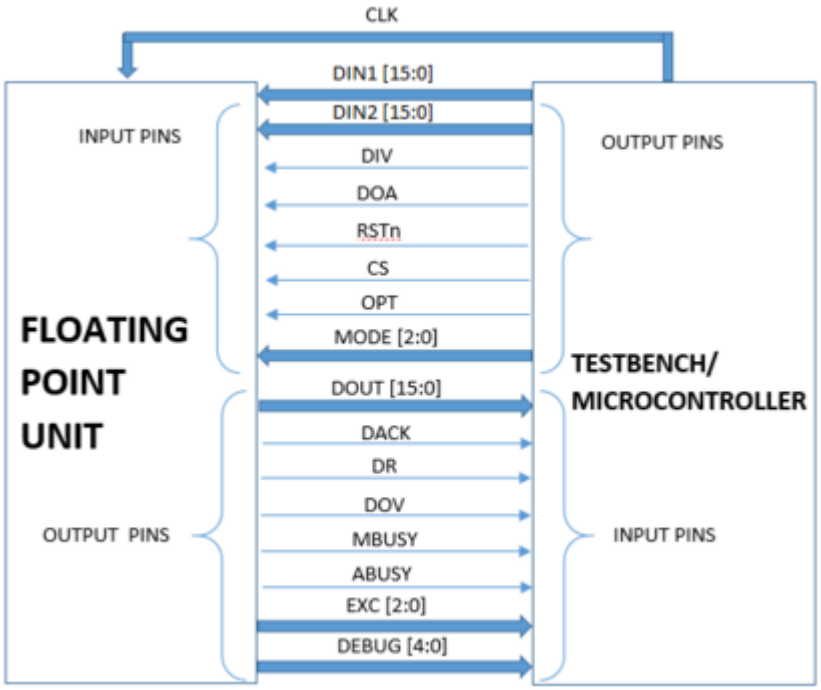
```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.001  |  0.001  |  6.659  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|   364   |   335   |   364   |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+-------------------+
|                |              Real             |       Total       |
|    DRVs        +------------------+------------+-------------------|
|                |  Nr nets(terms)  | Worst Vio  | Nr nets(terms)    |
+----------------+------------------+------------+-------------------+
|   max_cap      |       0 (0)      |   0.000    |       0 (0)       |
|   max_tran     |       0 (0)      |   0.000    |       0 (0)       |
|   max_fanout   |       0 (0)      |     0      |       0 (0)       |
|   max_length   |       0 (0)      |     0      |       0 (0)       |
+----------------+------------------+------------+-------------------+

Density: 61.050%
Total number of glitch violations: 0
------------------------------------------------------------
```

Pin level diagram

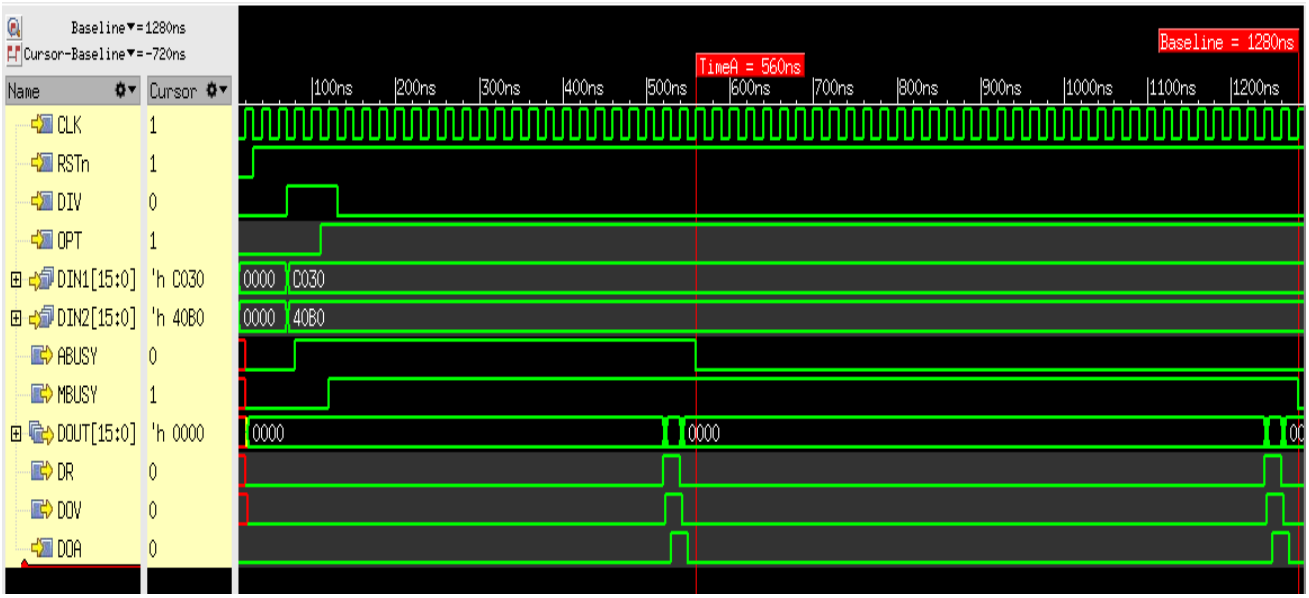


Pin Details

Pin Name in IC	Pad #	Type
CLK	1	In
RSTn	2	In
CS	3	In
DIV	4	In
DOA	5	In
OPT	6	In
MODE<2:0>	<8:10>	In
DIN2<15:0>	<11:27>	In
DIN1<15:0>	<28:44>	In
DACK	45	Out
DR	46	Out
DOV	47	Out
EXC<2:0>	<49:51>	Out
DEBUG<4:0>	<52:56>	Out
ABUSY	58	Out
MBUSY	59	Out
DOUT<15:2>	<60:73>	Out
DOUT<1:0>	<75:76>	Out
GND	7,48,74	Inout
VDD	16, 33, 57	Inout
NC	<77:84>	No Connect

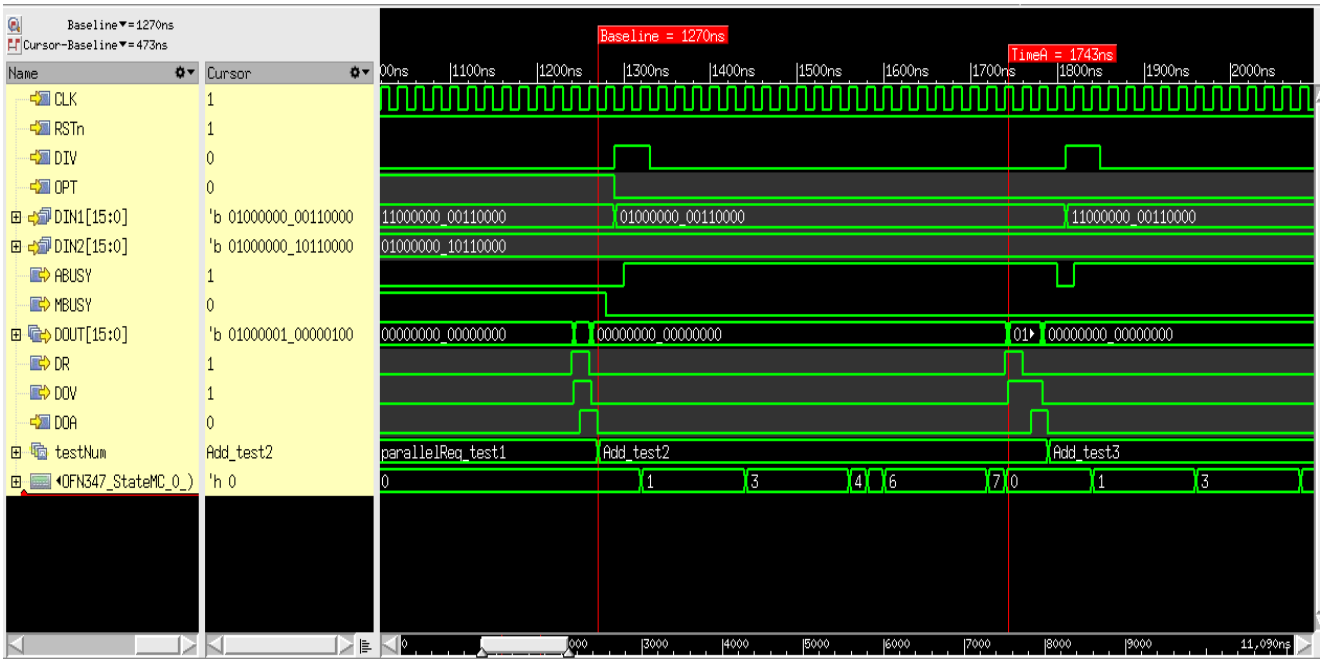
Simulation Results

1. Parallel Request Service: This snapshot shows the capability of the FPU to service an addition and multiplication request in parallel. After exiting from reset, the DIV(datain_valid) is set and valid data is provided on the two input line DIN1[15:0] and DIN2[15:0]. OPT, which indicates the operation type, is set to 0 , indicating addition request. The FPU takes in the data and asserts ABUSY to 1, indicating to the master that it has accepted the addition request and the adder unit is busy. Note that MBUSY is 0 at this point, which indicates to the master that the FPU can still accept inputs for multiplication. In the next clock, DIV remains high, with new data provided on DIN1 and DIN2, and OPT changed to 1. This indicates new computation request from the master . OPT being 1 indicates multiplication request. The FPU takes in the multiplication request(even though it is busy servicing the addition request), and asserts the MBUSY signal to indicate the master that the its multilication request has been accepted. Both ABUSY and MBUSY being 1 indicates the FPU cannot accept anymore request untill one of its servicing unit gets released.



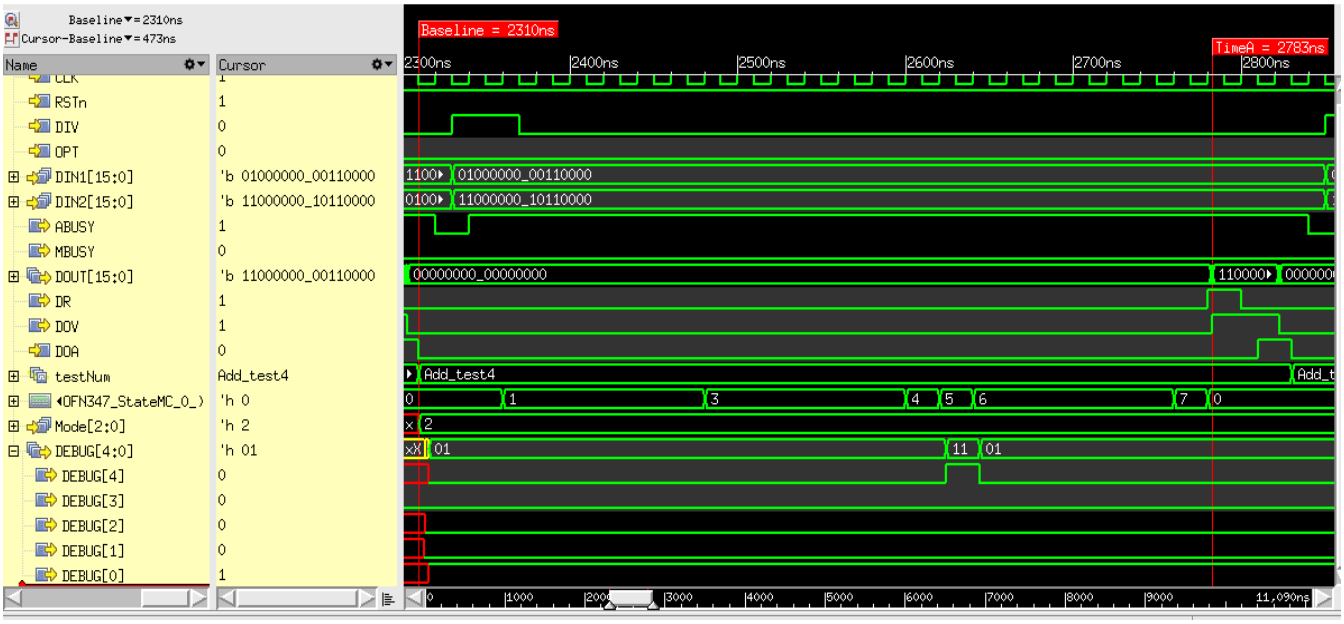
Parallel Request Service

2. Adder Flow: It shows the data flow for servicing an addition request. Once DIV is set and data provided on DIN1 and DIN2, the ABUSY goes high and computation starts in the adder module. The last signal indicates the statemachine values of the adder controller. The statemachine at 7 is the setoutput stage, where it sets the computed data on the output bus and loops back to idle state



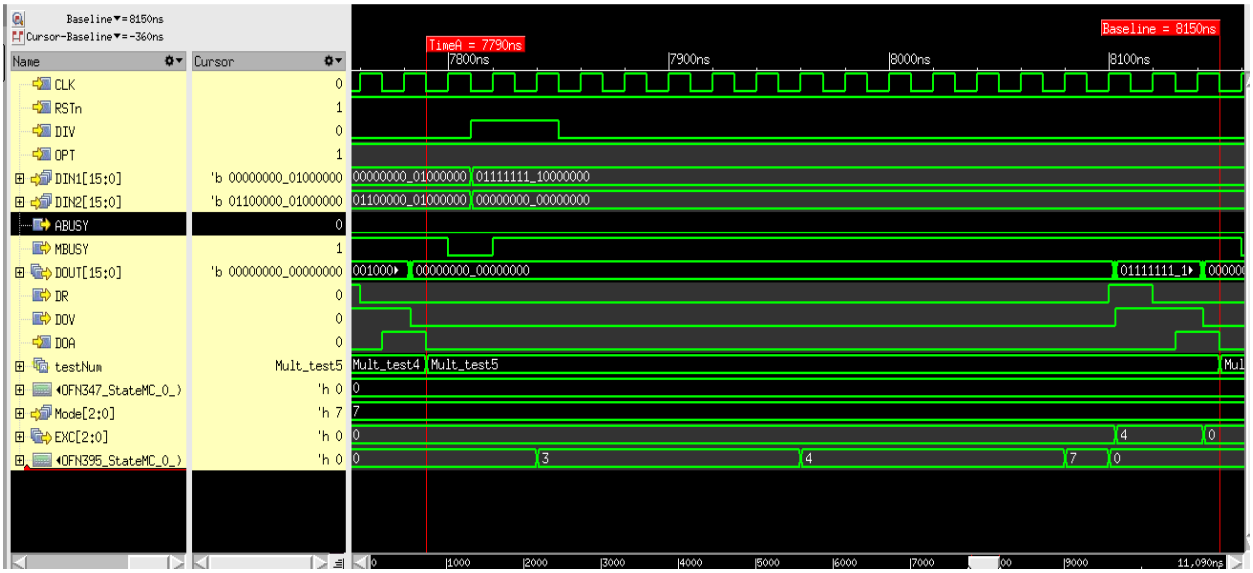
Adder Flow

3. AdderFlowSub: This snap shows addition of two inputs with different sign bits. In addition, it also shows the working of the debug mode. The MODE value is set to 010, which routes the internal status bits to the debug pins. DEBUG[4] indicates that the data on debug pin is valid data. The status bits are channeled to the debug pins in state 5.



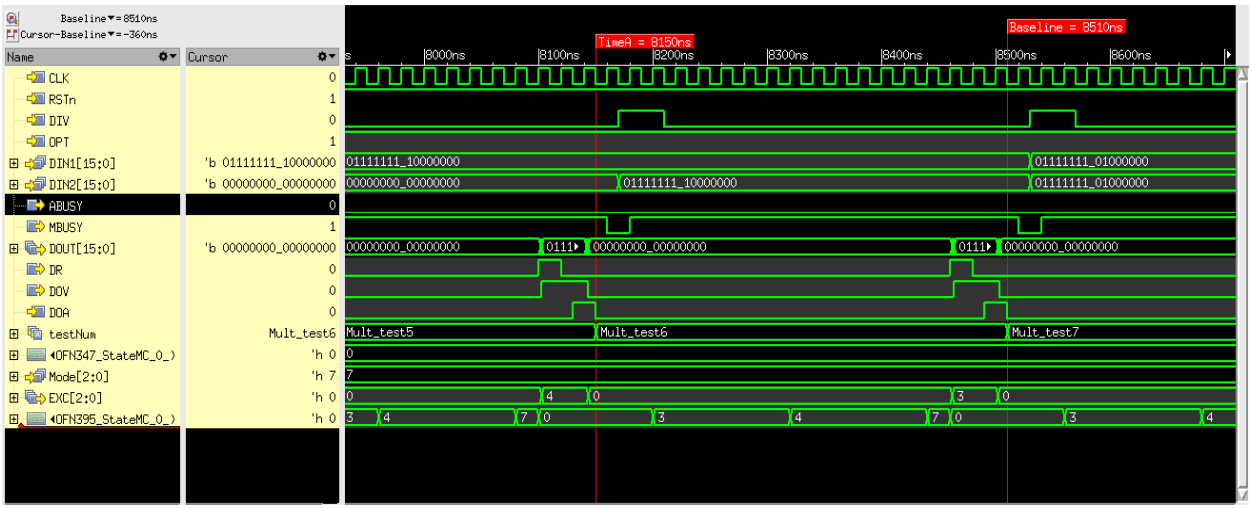
AdderFLowSub

4. MultFlowExc1: This snap explains the multiplier operation and protocol. The statemachine depicts the flow of control. The EXC indicates occurence of an exception with exception code 4



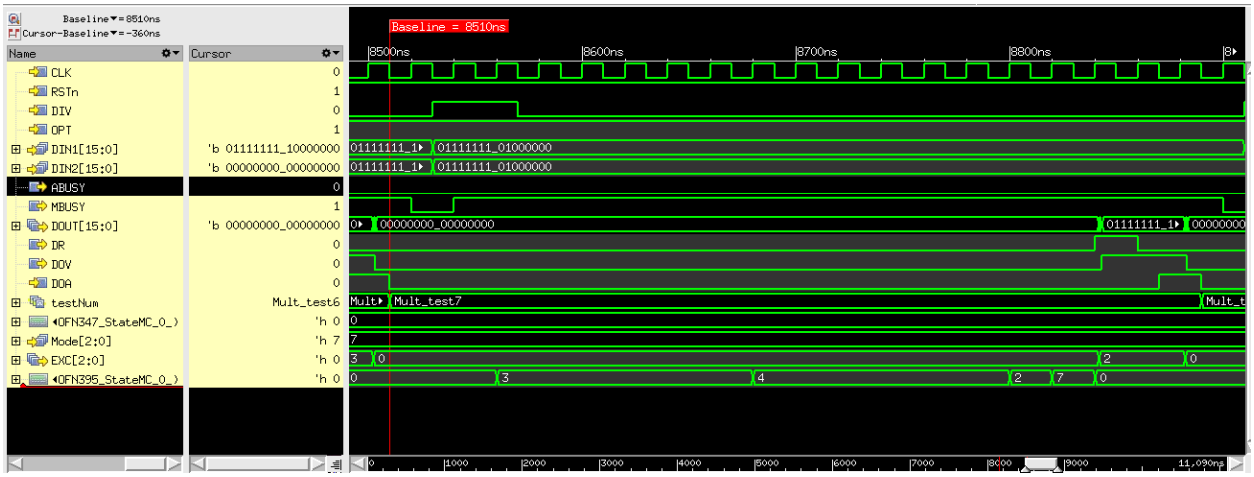
MultFlowExc1

5. MultFlowExc2: This snap explains the multiplier operation and protocol. The statemachine depicts the flow of control. The EXC indicates occurence of an exception with exception code 3.



MultFlowExc2

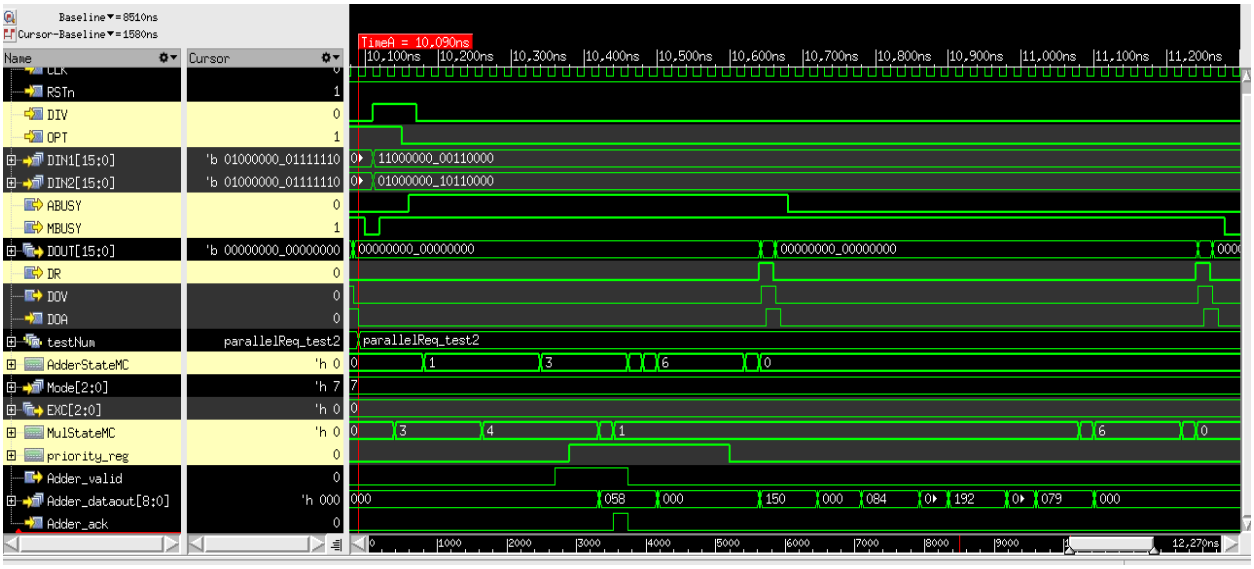
6. MultFlowExc3: This snap explains the multiplier operation and protocol. The statemachine depicts the flow of control. The EXC indicates occurence of an exception with exception code 2



MultFlowExc3

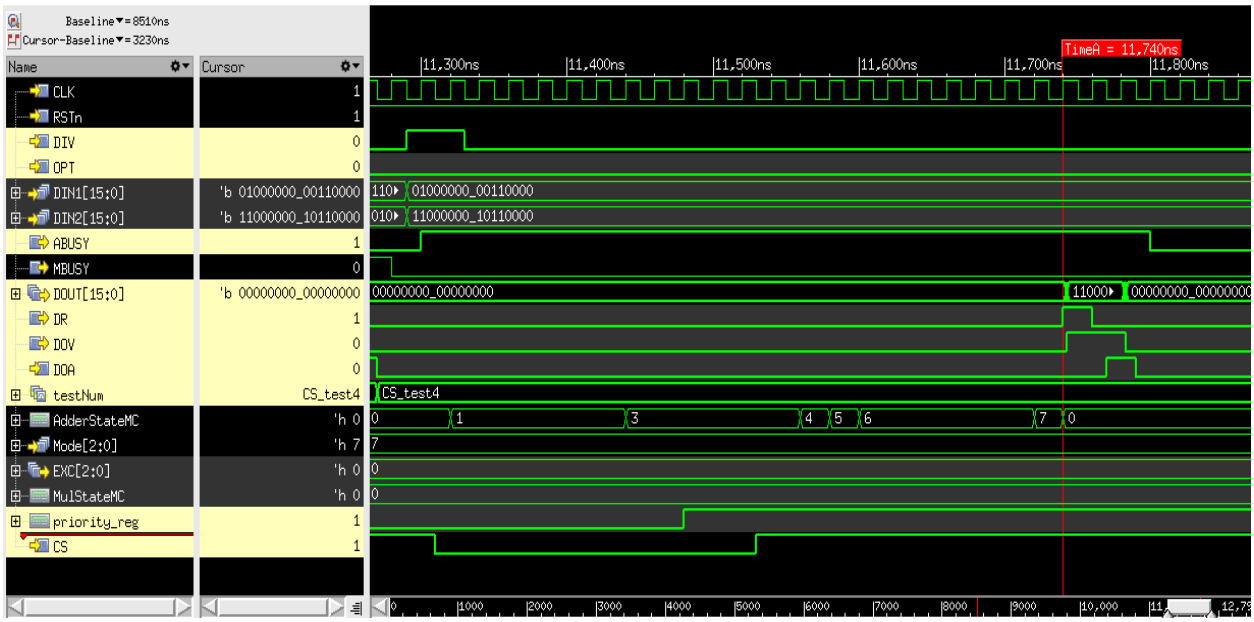
7. MultiRequestArbitration: The setup of this problem is similar to 1, that is, there is parallel processing of adder and multiplier unit, except that here the multiplier unit request is set first before the adder. Inside the FPU, there is a 9bit adder that is shared between the adder controller and the booth of the multiplier unit. The booth requires access to the adder unit for

successive addition operations. There is a priority arbitration interconnect place in between, to arbitrate on the requests received such that the adder controller requests doesn't gets stalled once the multiplier has started access. In the waveform, even though the multiplier starts first access to the adder unit, the arbitration logic allows the adder controller to capture a cycle in between thus preventing it from stalling for the entire duration of booth computation.



MultiRequestArbitration

8. Deselect_chipSelect: This shows that once the operation has been initiated, the chip select can be turned off. During this time, the master can use some other shared resources instead of investing on the FPU. The chip select is only required during receiving input operands and providing result data.



Deselect_chipSelect