STANDARD CELL LIBRARY DOCUMENTATION

(DOCUMENT 3)

Table of Contents

Introduction

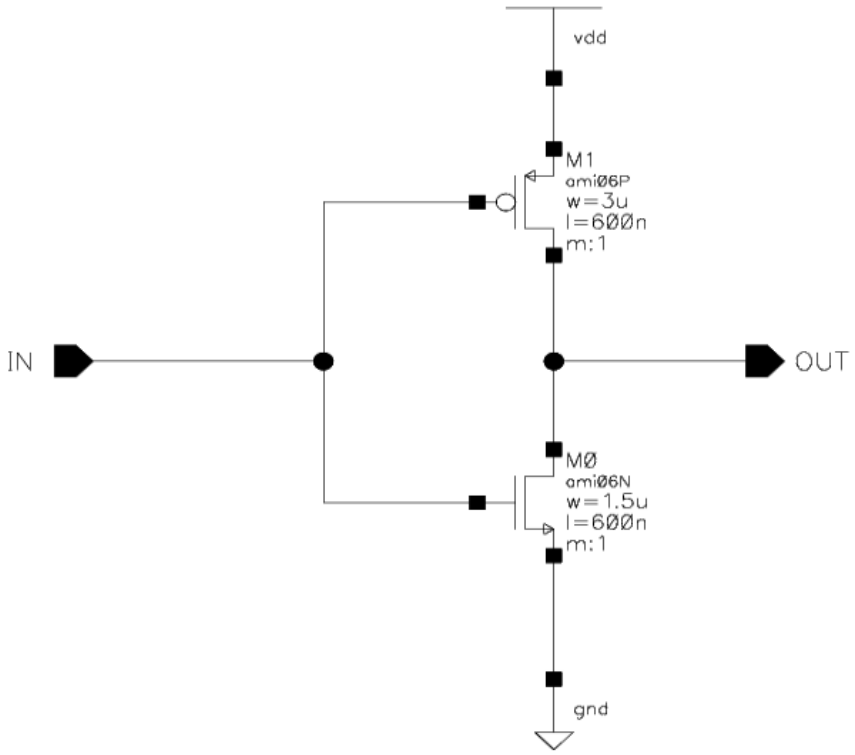
In this document, all the standard cells in our library (Lib6710_05) are described in detail. For each cell, the following information is provided: schematic, layout, behavioral model, timing data & user's guide.

Standard Cell: Inverter

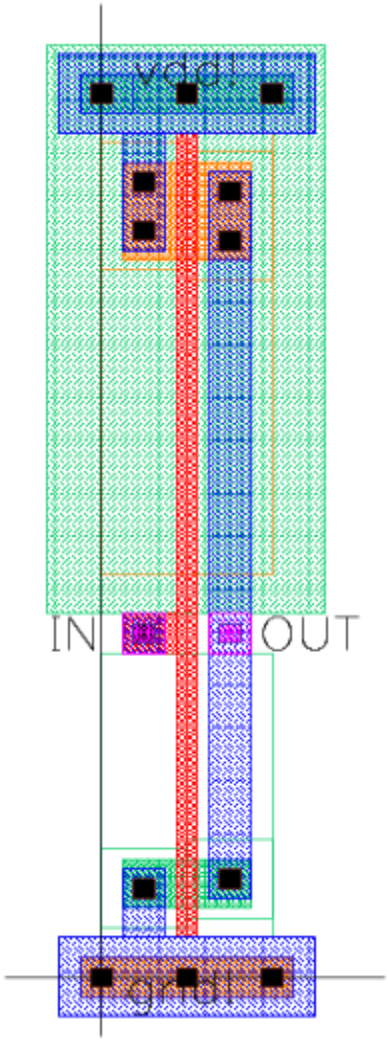
There are three types of inverters in our standard cell library: standard 1X sized inverter (INVX1), inverter with 4X drive strength (INVX4), and inverter with 8X drive strength (INVX8).

INVX1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "INVX1" "behavioral"

module INVX1 ( OUT, IN );

  input IN;
  output OUT;

  not  not1(OUT, IN);

    specify

        (IN => OUT) = (1.0, 1.0);

    endspecify

endmodule
```

Timing Data

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.93	4.44
Falling propagation delay (ns)	1.2	5.89
Rising output slope (ns)	0.66	3.63
Falling output slope (ns)	0.85	4.72

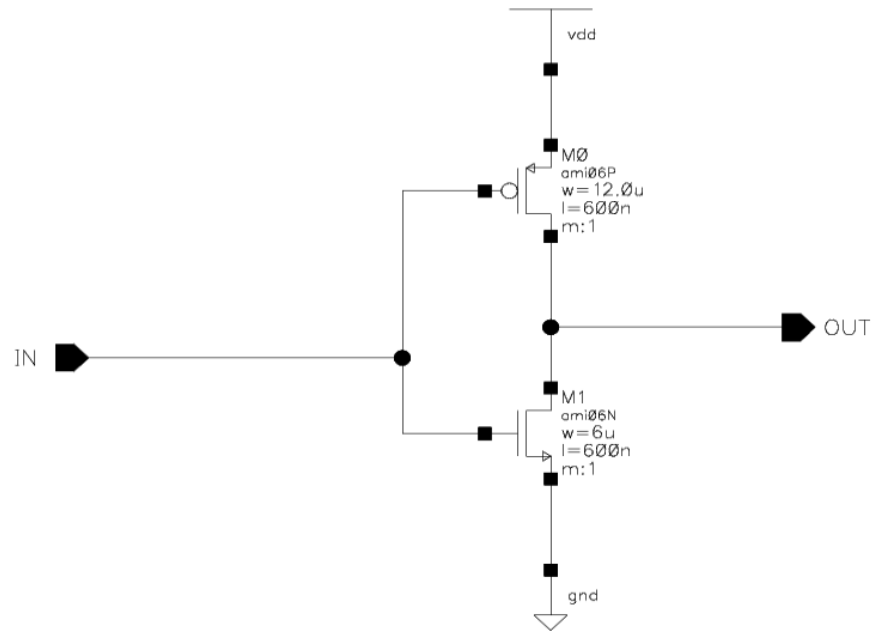
User's Guide

The Boolean expression is:

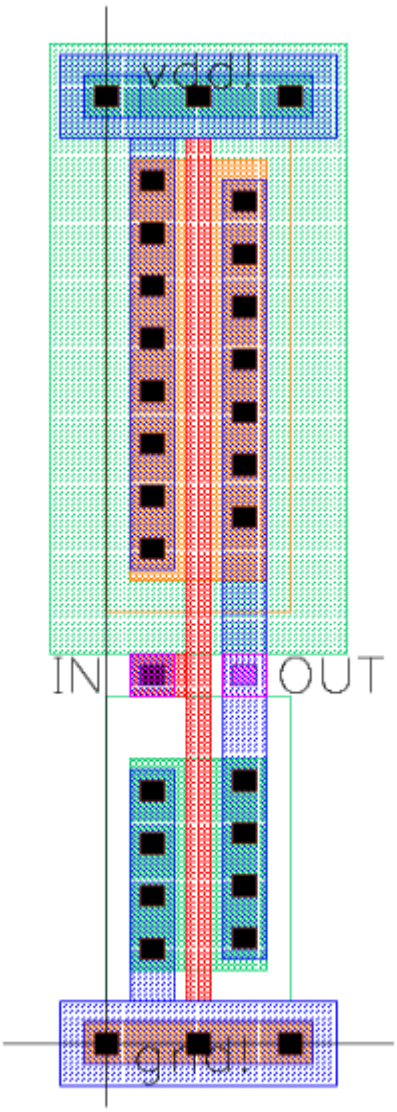
$$OUT = \sim IN$$

INVX4

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "INVX4" "behavioral"

module INVX4 ( OUT, IN );

  output OUT;
  input IN;

    not n1(OUT, IN);

    specify

        (IN => OUT) = (1.0, 1.0);

    endspecify

endmodule
```

Timing Data

Delays	Input slope = 0.42 ns Output loading = 0.4 pF	Input slope = 1.2 ns Output loading = 2.4 pF
Rising propagation delay (ns)	0.83	3.93
Falling propagation delay (ns)	0.84	4.09
Rising output slope (ns)	0.55	3.13
Falling output slope (ns)	0.55	3.15

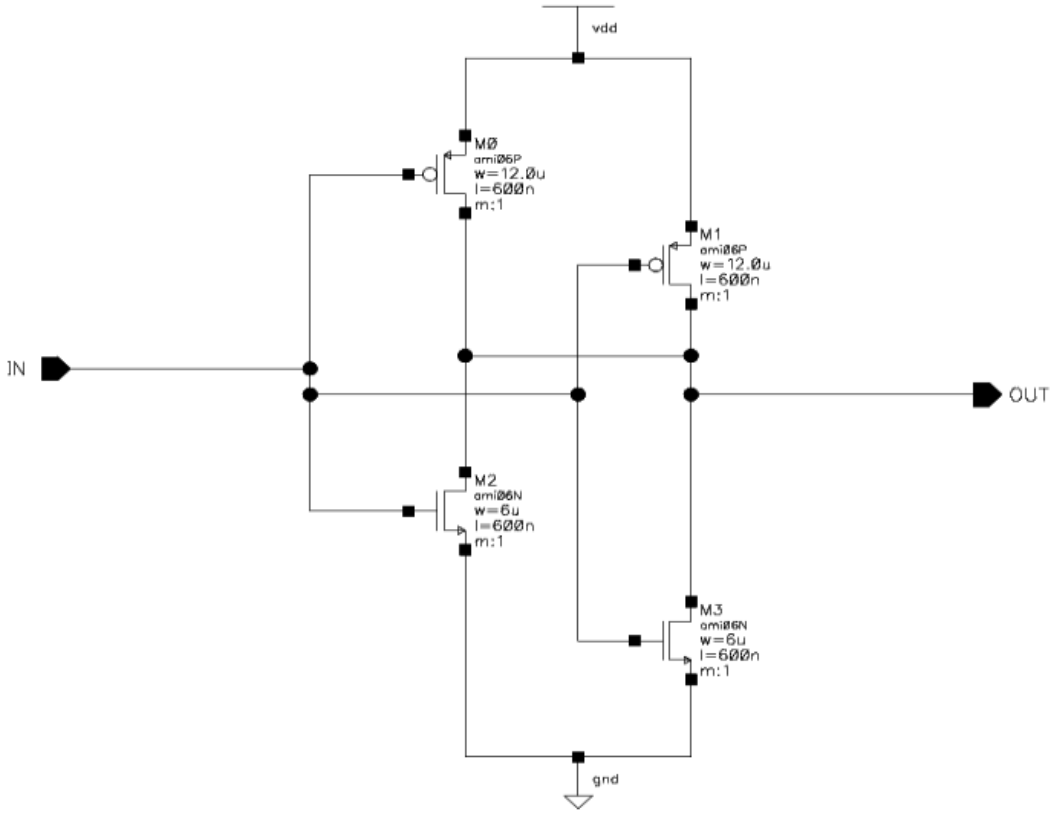
User's Guide

The Boolean expression is:

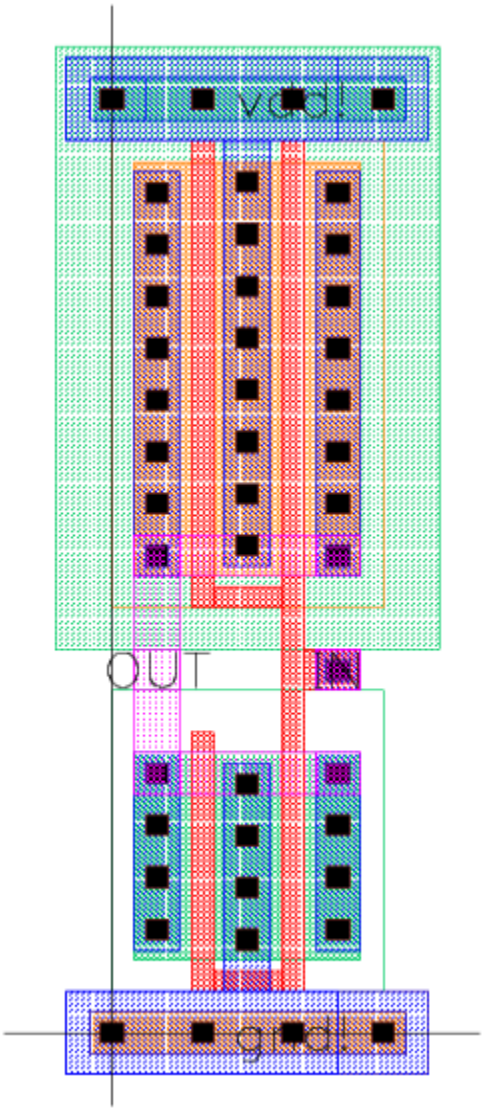
$$OUT = \sim IN$$

INVX8

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "INVX8" "behavioral"

module INVX8 ( OUT, IN );

  output OUT;
  input IN;

    not n1(OUT, IN);

    specify

        (IN => OUT) = (1.0, 1.0);

    endspecify

endmodule
```

Timing Data

Delays	Input slope = 0.42 ns Output loading = 0.8 pF	Input slope = 1.2 ns Output loading = 4.8 pF
Rising propagation delay (ns)	0.83	3.93
Falling propagation delay (ns)	0.84	4.09
Rising output slope (ns)	0.55	3.13
Falling output slope (ns)	0.55	3.15

User's Guide

The Boolean expression is:

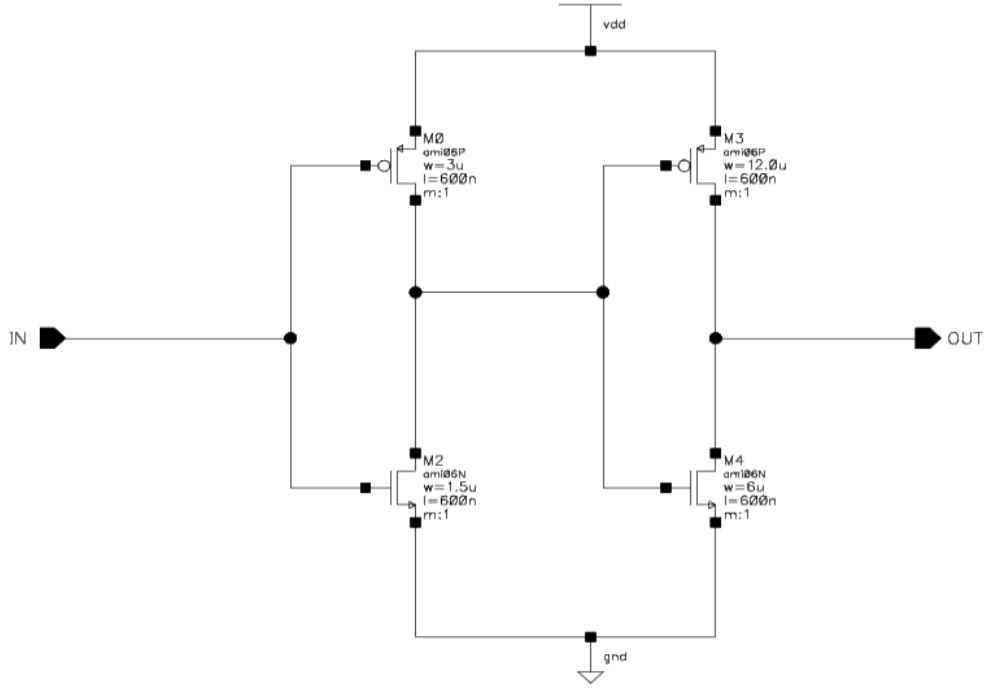
$$OUT = \sim IN$$

Standard Cell: Buffer

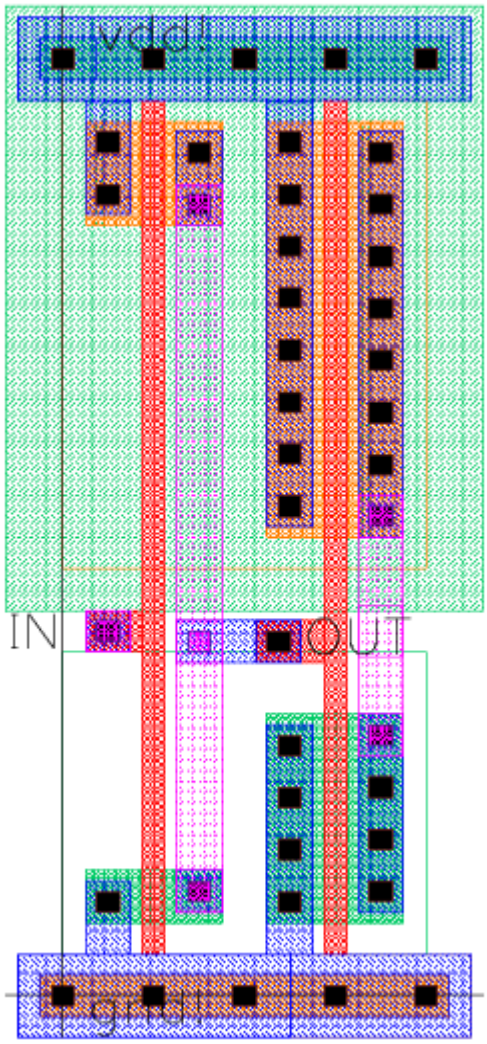
There are two types of buffers in our standard cell library: buffer with 4X drive strength (BUF4X), and buffer with 8X drive strength (BUF8X).

BUF4X

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "BUF4X" "behavioral"

module BUF4X ( OUT, IN );

  output OUT;
  input IN;

  buf u_buf(OUT, IN);

    specify

        (IN => OUT) = (1.0, 1.0);

    endspecify

endmodule
```

Timing Data

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.74	1.86
Falling propagation delay (ns)	0.67	1.77
Rising output slope (ns)	0.21	0.82
Falling output slope (ns)	0.20	0.82

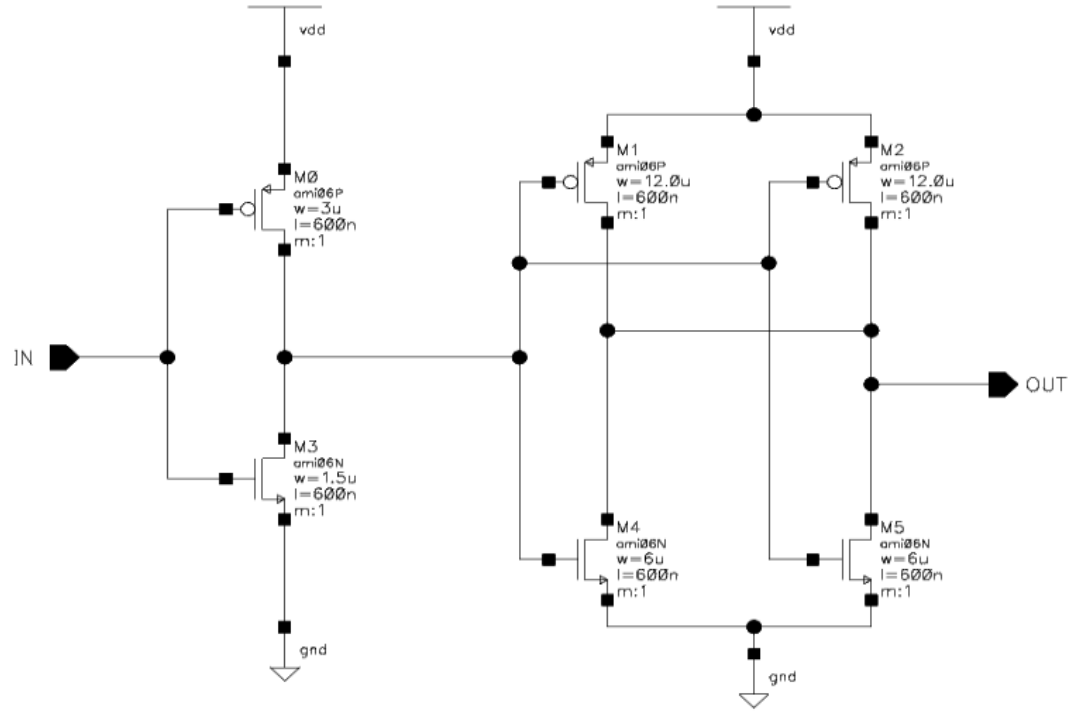
User's Guide

The Boolean expression is:

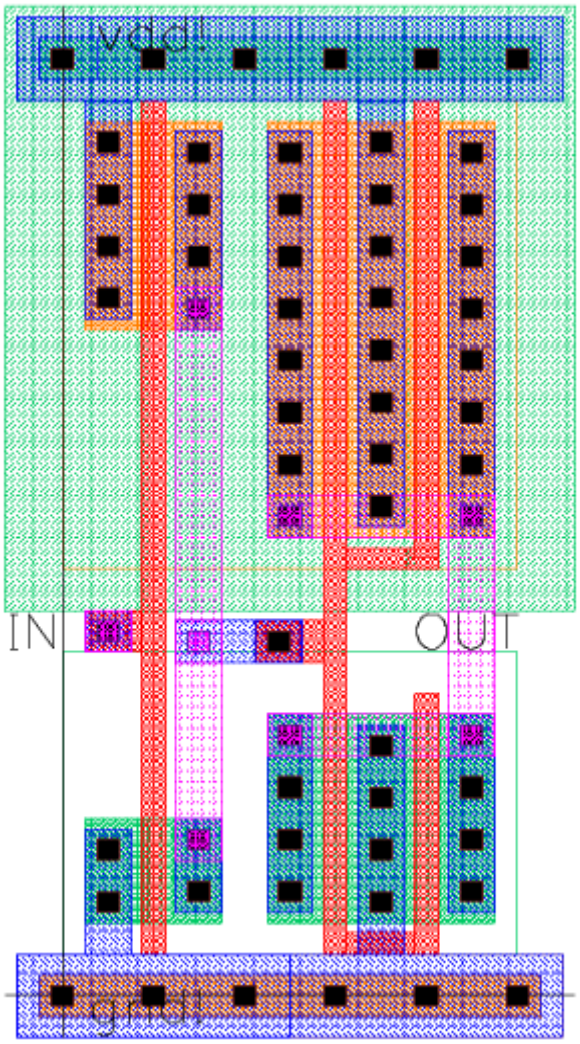
$$OUT = IN$$

BUF8X

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "BUF8X" "behavioral"

module BUF8X ( OUT, IN );

  output OUT;
  input IN;

  buf u_buf(OUT, IN);

    specify

        (IN => OUT) = (1.0, 1.0);

    endspecify

endmodule
```

Timing Data

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.58	1.31
Falling propagation delay (ns)	0.58	1.36
Rising output slope (ns)	0.14	0.45
Falling output slope (ns)	0.13	0.45

User's Guide

The Boolean expression is:

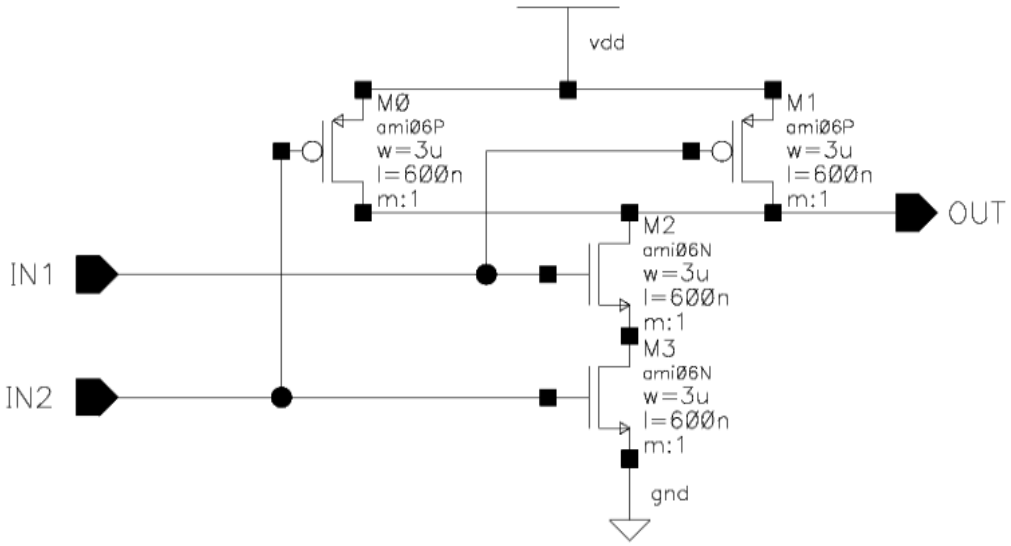
$$OUT = IN$$

Standard Cell: NAND

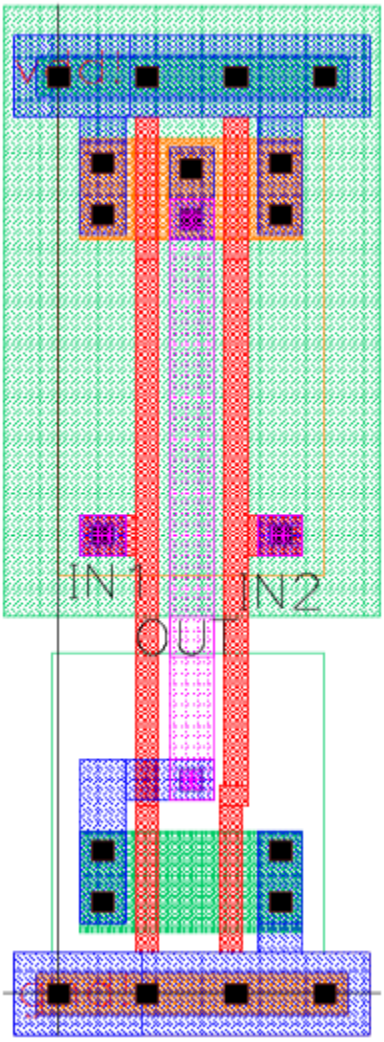
There are three types of NAND gates in our standard cell library: standard 2-input 1X sized NAND gate (NAND2X1), a 2-input NAND gate with 2X drive strength (NANDX2), and a 3-input 1X sized NAND gate (NAND3X1).

NAND2X1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "NAND2X1" "behavioral"


module NAND2X1 ( OUT, IN1, IN2 );

  input IN2;
  output OUT;
  input IN1;

nand NAND2X1 (OUT, IN1, IN2);


specify


(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.96	4.48
Falling propagation delay (ns)	0.80	3.69
Rising output slope (ns)	0.66	3.64
Falling output slope (ns)	0.55	2.93

Due to body effect, the worst case delays & slopes will occur for the path IN1 => OUT. The timing data for IN2 => OUT is similar to the above table to the first decimal point (a little lesser), for almost all cases.

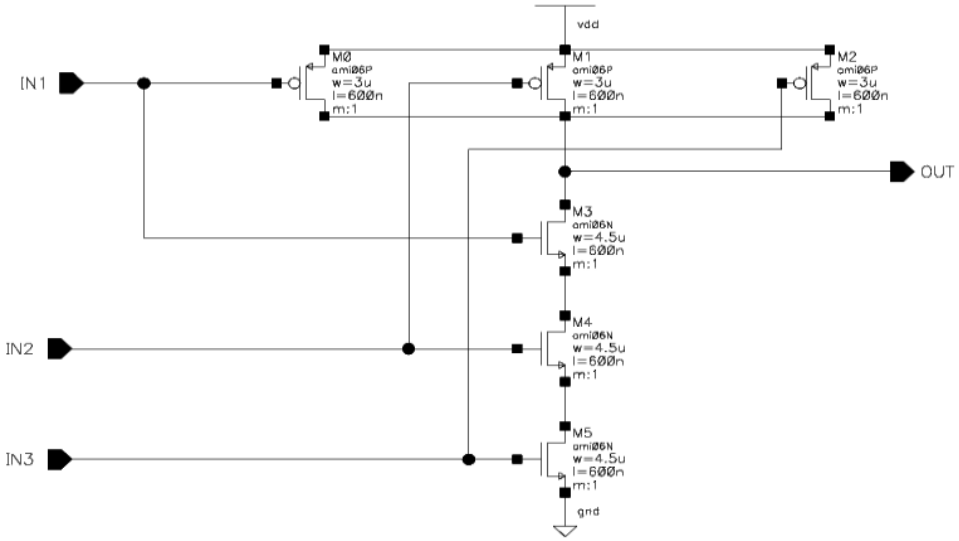
User's Guide

The Boolean expression is:

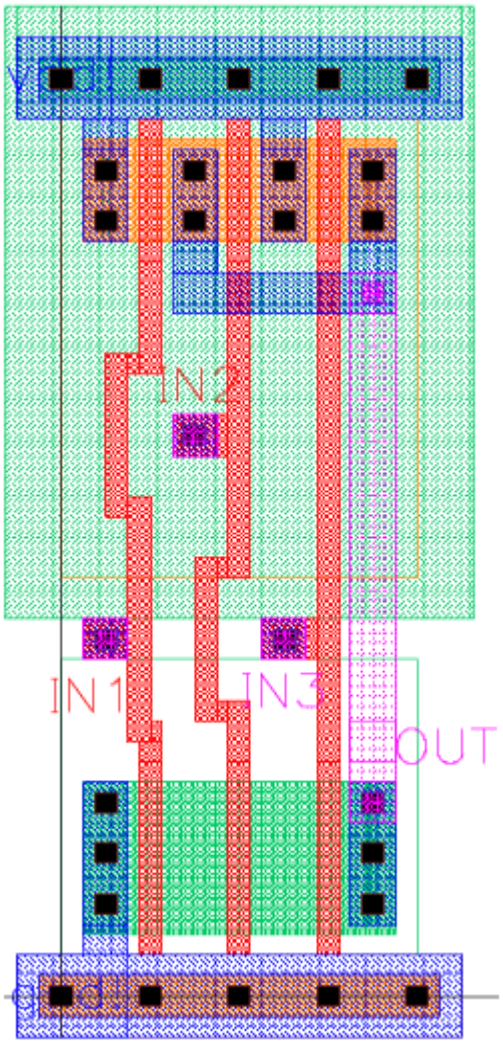
$$OUT = \sim(IN1 \,\&\, IN2)$$

NAND3X1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "NAND3X1" "behavioral"

module NAND3X1 ( OUT, IN1, IN2, IN3 );

  input IN3;
  input IN2;
  output OUT;
  input IN1;
  wire OUT;

assign OUT=~(IN1&IN2&IN3);

specify

(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);
(IN3 => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	1.12	4.64
Falling propagation delay (ns)	0.67	2.97
Rising output slope (ns)	0.80	3.78
Falling output slope (ns)	0.51	2.56

Due to body effect, the worst case delays & slopes will occur for the path IN1 => OUT.

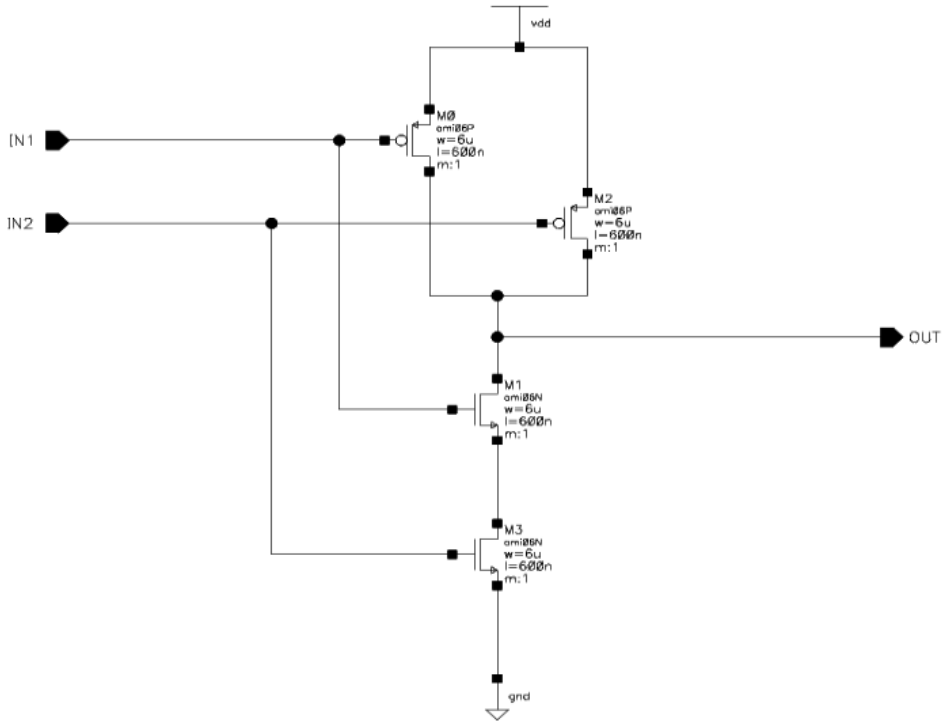
User's Guide

The Boolean expression is:

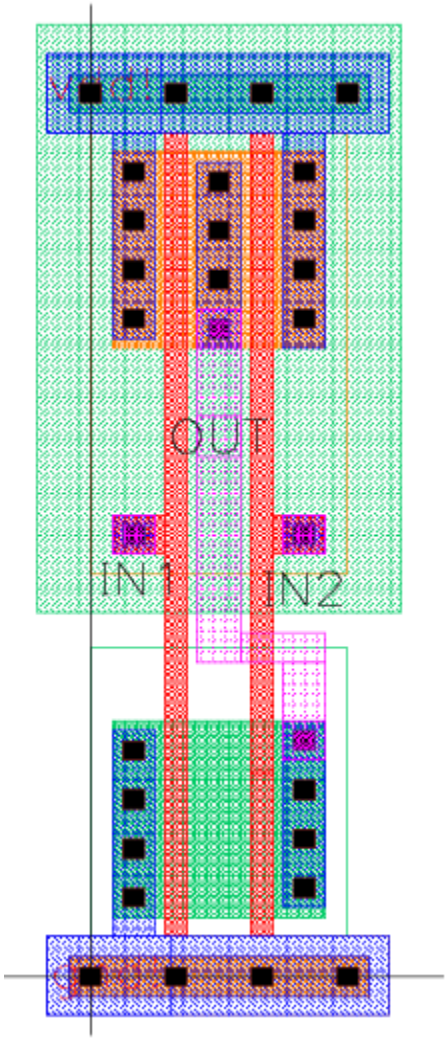
$$OUT = \sim(IN1 \,\&\, IN2 \,\&\, IN3)$$

NANDX2

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "NANDX2" "behavioral"

module NANDX2 ( OUT, IN1, IN2 );

  input IN2;
  output OUT;
  input IN1;

  nand u_n1(OUT, IN1, IN2);

  specify

    (IN1 => OUT) = (1.0, 1.0);
    (IN2 => OUT) = (1.0, 1.0);

  endspecify

endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.2 pF	Input slope = 1.2 ns Output loading = 1.2 pF
Rising propagation delay (ns)	0.92	4.15
Falling propagation delay (ns)	0.66	3.13
Rising output slope (ns)	0.62	3.33
Falling output slope (ns)	0.48	2.58

Due to body effect, the worst case delays & slopes will occur for the path IN1 => OUT.

User's Guide

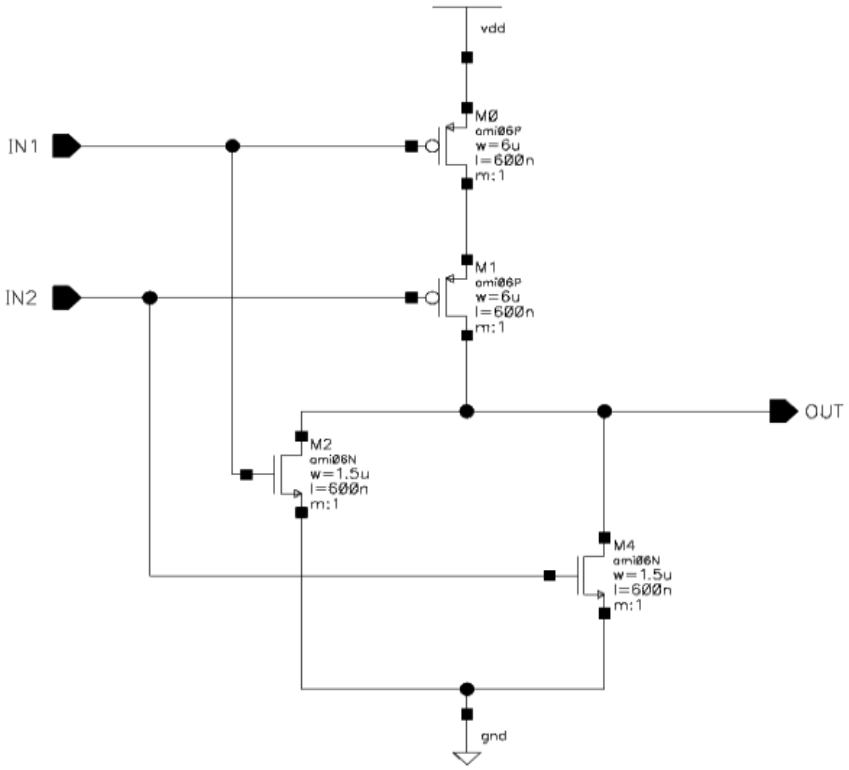
The Boolean expression is:

$$OUT = \sim(IN1 \,\&\, IN2)$$

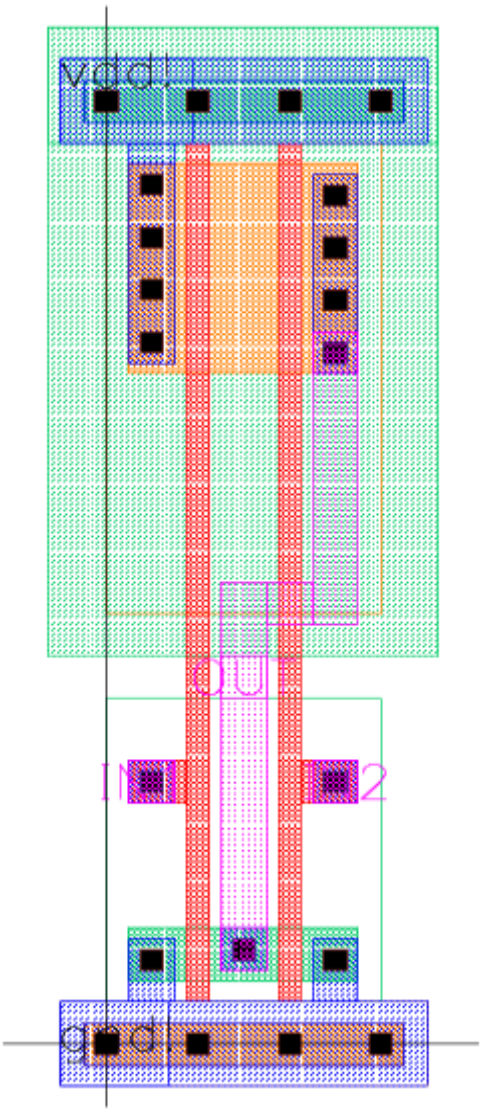
Standard Cell: NOR

NOR2X1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "NOR2X1" "behavioural"


module NOR2X1 ( OUT, IN1, IN2 );

  input IN2;
  output OUT;
  input IN1;

  nor  nor2(OUT, IN1, IN2);

  specify

    (IN1 => OUT) = (1.0, 1.0);
    (IN2 => OUT) = (1.0, 1.0);

  endspecify

endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.82	3.73
Falling propagation delay (ns)	1.36	6.05
Rising output slope (ns)	0.60	3.16
Falling output slope (ns)	0.96	4.83

The worst case delays & slopes occurs for the path IN1 => OUT.

User's Guide

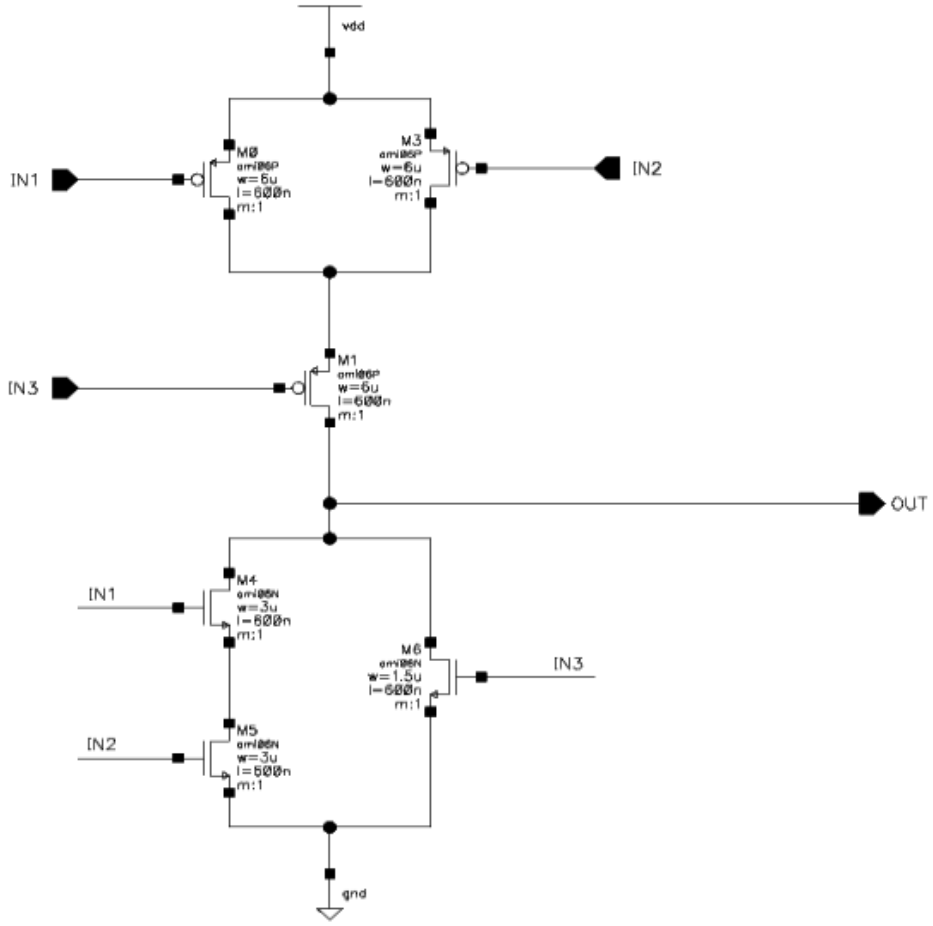
The Boolean expression is:

$$OUT = \sim(IN1 \mid IN2)$$

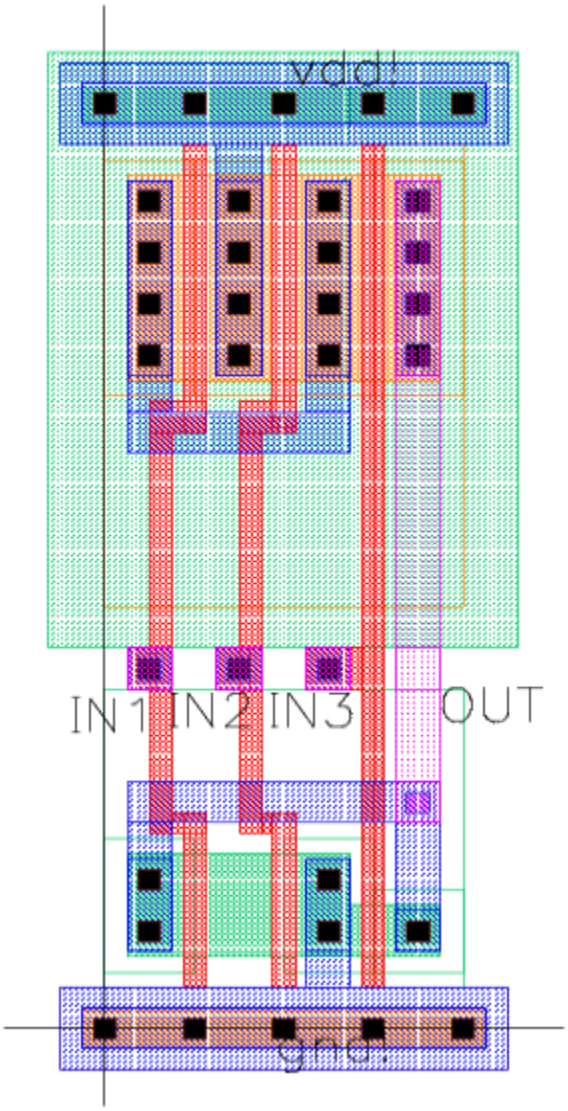
Standard Cell: And-Or-Invert

AOI21

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "AOI21" "behavioral"


module AOI21 ( OUT, IN1, IN2, IN3 );

  input IN3;
  input IN2;
  output OUT;
  input IN1;

assign OUT="((IN1&IN2)|IN3);

specify

(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);
(IN3 => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.86	3.78
Falling propagation delay (ns)	0.92	3.83
Rising output slope (ns)	0.61	3.17
Falling output slope (ns)	0.64	3.02

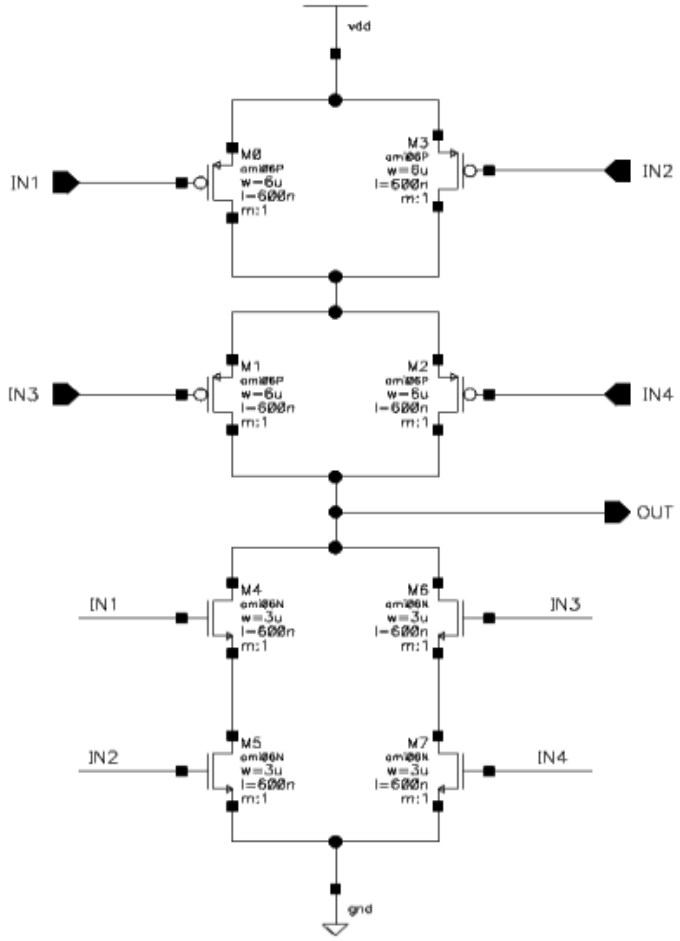
User's Guide

The Boolean expression is:

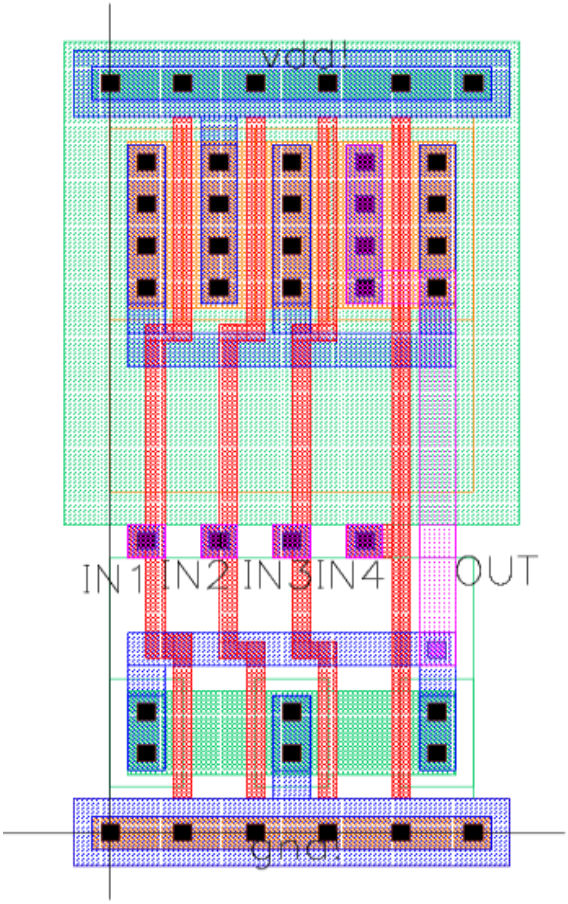
$$OUT = \sim((IN1 \,\&\, IN2) \mid IN3)$$

AOI22

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "AOI22" "behavioral"


module AOI22 ( OUT, IN1, IN2, IN3, IN4 );

  input IN4;
  input IN3;
  input IN2;
  output OUT;
  input IN1;

assign OUT="((IN1&IN2)|(IN3&IN4));

specify

(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);
(IN3 => OUT) = (1.0, 1.0);
(IN4 => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.85	3.48
Falling propagation delay (ns)	0.99	3.90
Rising output slope (ns)	0.58	2.82
Falling output slope (ns)	0.69	3.08

User's Guide

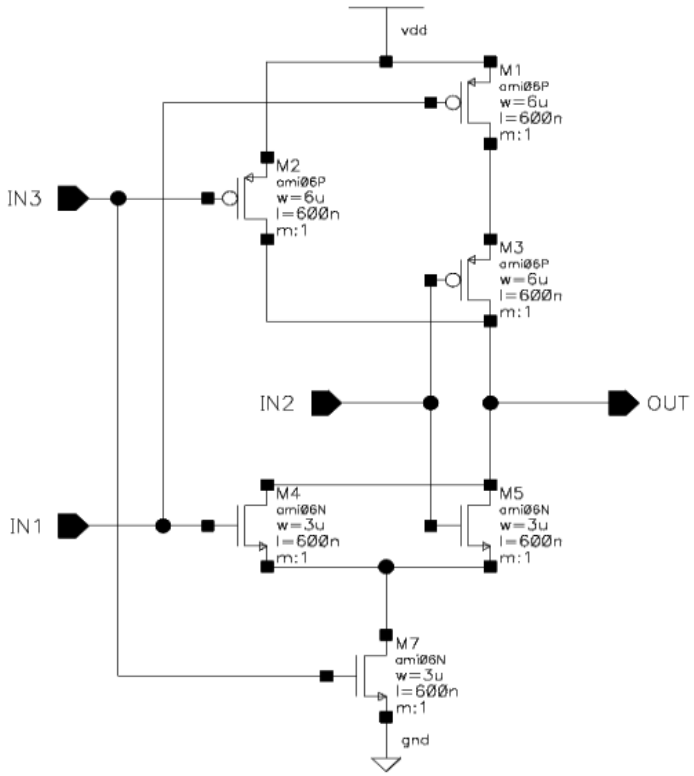
The Boolean expression is:

$$OUT = \sim((IN1 \,\&\, IN2) \mid (IN3 \,\&\, IN4))$$

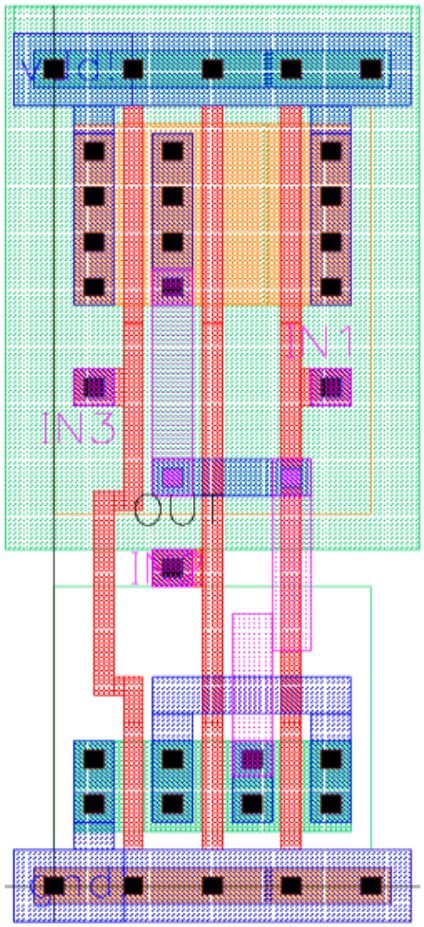
Standard Cell: Or-And-Invert

OAI21

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "OAI21" "behavioral"


module OAI21 ( OUT, IN1, IN2, IN3 );

  input IN3;
  input IN2;
  output OUT;
  input IN1;


assign OUT=~((IN1|IN2)&IN3);

specify

(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);
(IN3 => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.86	3.79
Falling propagation delay (ns)	0.91	3.82
Rising output slope (ns)	0.62	3.18
Falling output slope (ns)	0.63	3.02

User's Guide

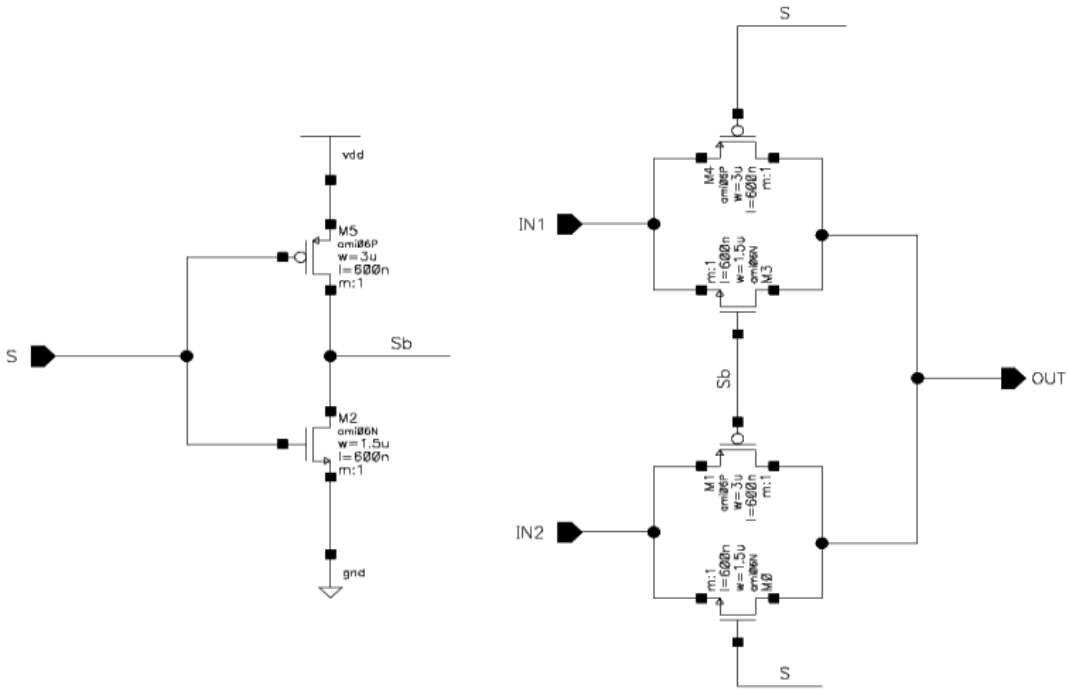
The Boolean expression is:

$$OUT = \sim((IN1 \mid IN2) \,\&\, IN3)$$

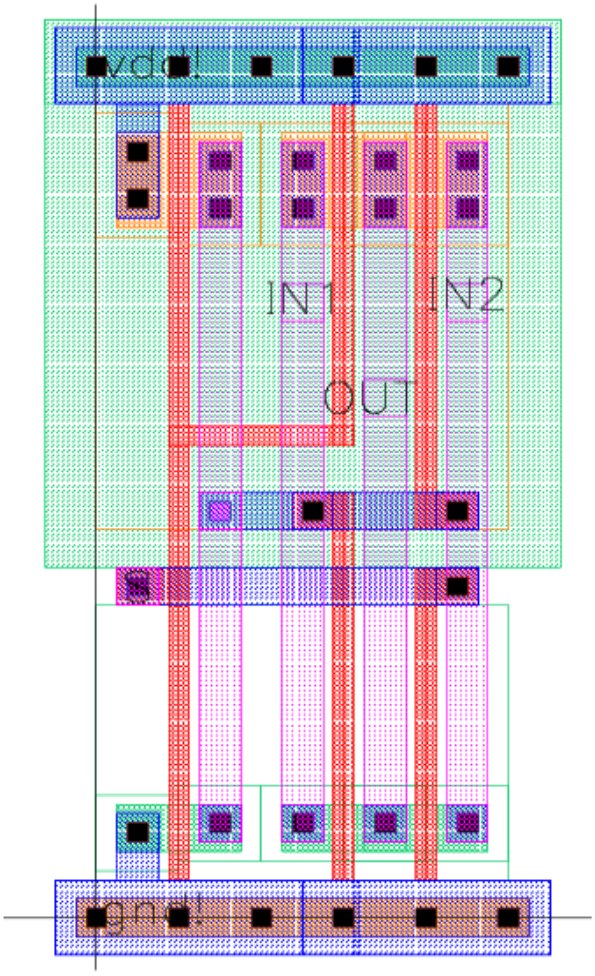
Standard Cell: Multiplexer

MUX2X1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "MUX2X1" "behavioral"


module MUX2X1 ( S, IN1, IN2, OUT );

  input IN1, IN2, S;
  output OUT;

assign OUT = S ? IN2 : IN1;


specify


(IN1 => OUT) = (1.0, 1.0);
(IN2 => OUT) = (1.0, 1.0);
(S => OUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for IN1 => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.71	3.42
Falling propagation delay (ns)	0.78	3.83
Rising output slope (ns)	0.67	3.27
Falling output slope (ns)	0.76	3.84

Timing Data (for S => OUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	0.92	3.76
Falling propagation delay (ns)	0.96	4.20
Rising output slope (ns)	0.59	3.22
Falling output slope (ns)	0.69	3.79

User's Guide

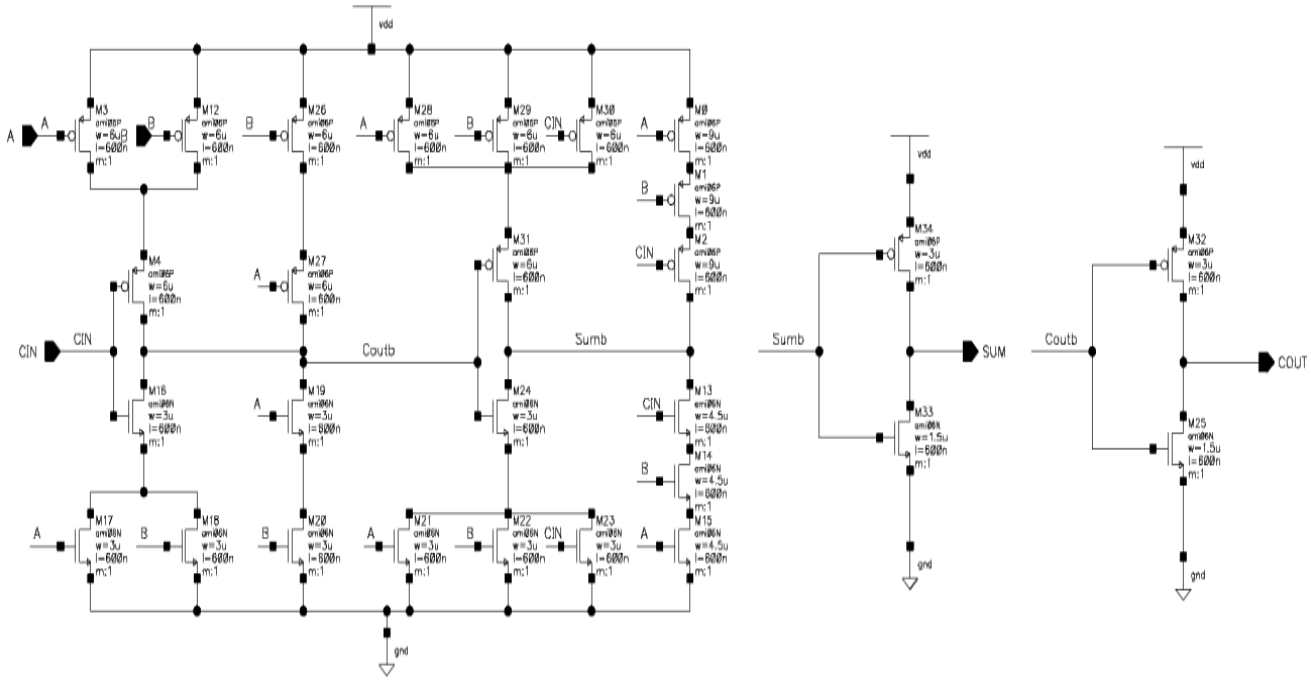
The Boolean expression is:

$$OUT = (\sim S \,\&\, IN1) | \, (S \,\&\, IN2)$$

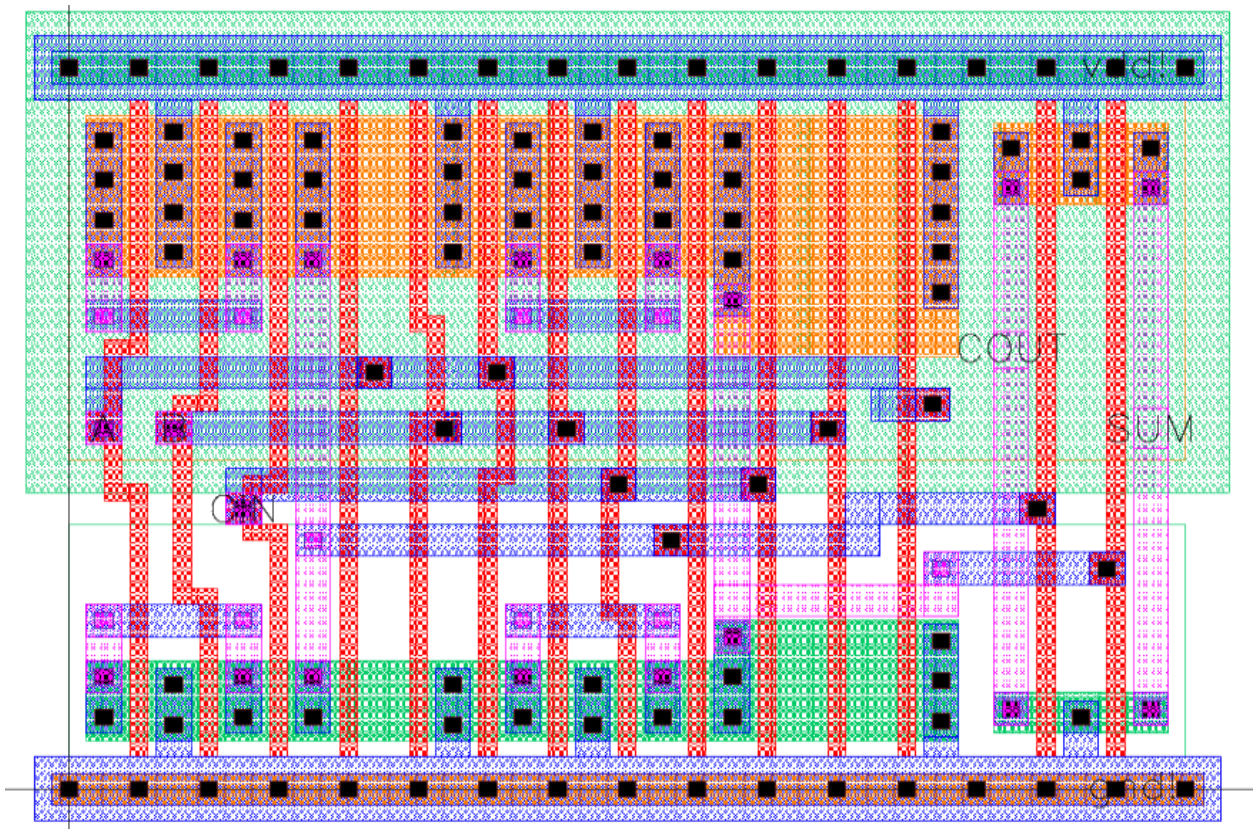
Standard Cell: 1-bit Full Adder

FULLADD

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "FULLADD" "behavioral"


module FULLADD ( COUT, SUM, A, B, CIN );

  input A;
  input B;
  input CIN;
  output COUT;
  output SUM;

assign {COUT, SUM} = A + B + CIN;

specify

(A => SUM) = (1.0, 1.0);
(B => SUM) = (1.0, 1.0);
(CIN => SUM) = (1.0, 1.0);

(A => COUT) = (1.0, 1.0);
(B => COUT) = (1.0, 1.0);
(CIN => COUT) = (1.0, 1.0);

endspecify


endmodule
```

Timing Data (for A => COUT)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	1.25	4.66
Falling propagation delay (ns)	1.55	6.19
Rising output slope (ns)	0.68	3.63
Falling output slope (ns)	0.86	4.71

Timing Data (for A => SUM)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	1.18	4.54
Falling propagation delay (ns)	1.48	6.10
Rising output slope (ns)	0.66	3.63
Falling output slope (ns)	0.85	4.71

User's Guide

The Boolean expression is:

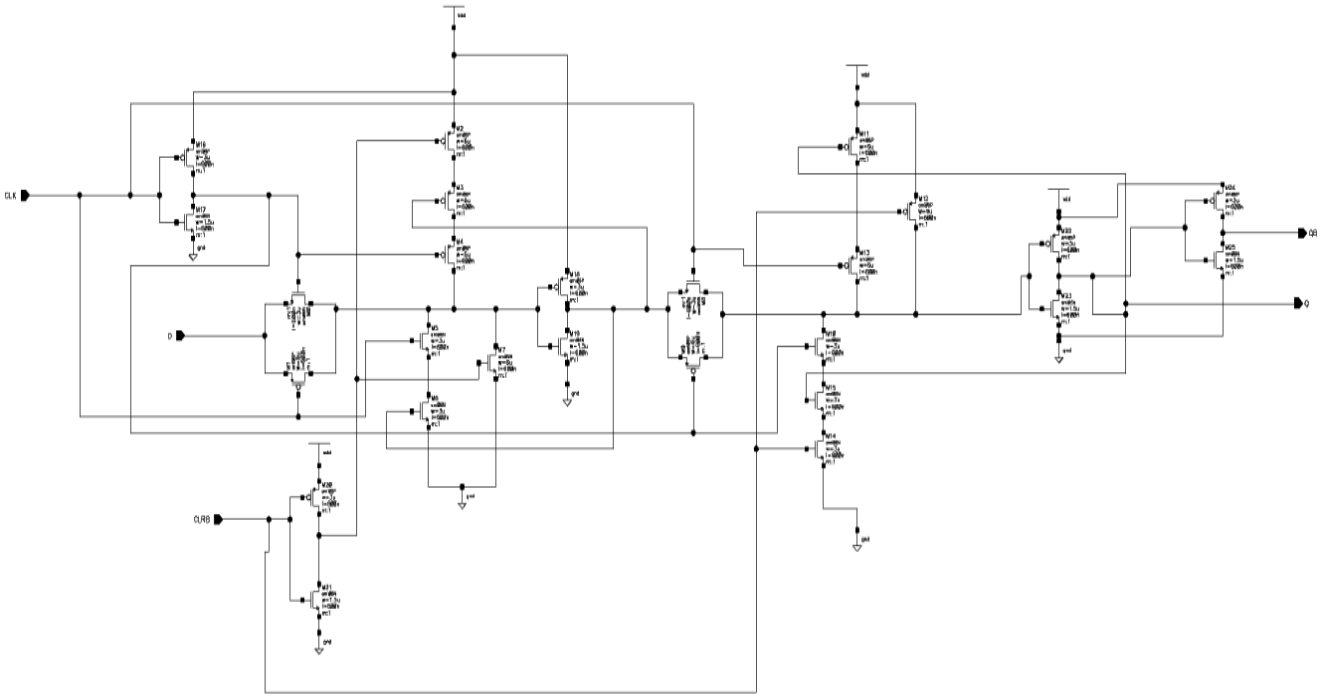
$$COUT = ((A \mid B) \,\&\, CIN) \mid (A \,\&\, B)$$

$$SUM = (A \,\&\, B \,\&\, CIN) \mid ((A \mid B \mid CIN) \,\&\, (\sim COUT))$$

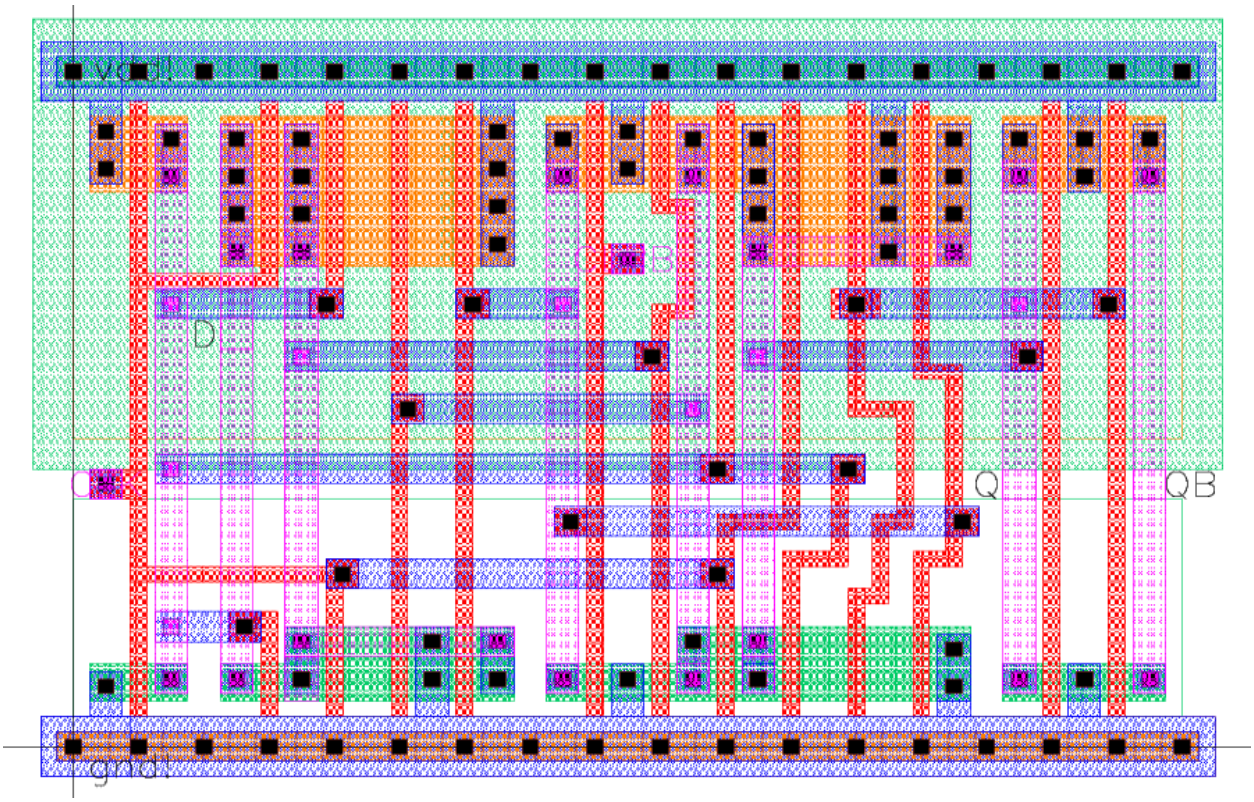
Standard Cell: D Flip-Flop

DFFRX1

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib6710_05", "DFFRX1" "behavioral"

module DFFRX1 ( Q, QB, CLK, D, CLRB );

  input CLRB;
  input CLK;
  input D;
  output Q;
  output QB;


  reg Q_buf ;

  assign Q  =  Q_buf ;
  assign QB = ~Q_buf ;

  always@(posedge CLK or negedge CLRB) begin
     if(CLRB==1'b0)  Q_buf <= 1'b0 ;
     else            Q_buf <= D    ;
  end

  specify

    (D => Q) = (1.0, 1.0);
    (CLK => Q) = (1.0, 1.0);
    (CLRB => Q) = (1.0, 1.0);

    (D => QB) = (1.0, 1.0);
    (CLK => QB) = (1.0, 1.0);
    (CLRB => QB) = (1.0, 1.0);

  endspecify

endmodule
```

Timing Data (Setup & Hold Times)

Delays	D Input slope = 1.2 ns Clock slope = 0.06 ns	D Input slope = 1.2 ns Clock slope = 0.6 ns
Hold time for rising edge of D (ns)	-0.41	-0.68
Hold time for falling edge of D (ns)	0.27	0.17
Setup time for rising edge of D (ns)	1.32	1.03
Setup time for falling edge of D (ns)	0.93	0.69

Timing Data (CLK => Q)

Delays	Input slope = 0.42 ns Output loading = 0.1 pF	Input slope = 1.2 ns Output loading = 0.6 pF
Rising propagation delay (ns)	1.44	4.89
Falling propagation delay (ns)	2.00	6.74
Rising output slope (ns)	0.87	3.80

Falling output slope (ns)	1.12	4.93

User's Guide

The Boolean expression is:

$$@(posedge\ CLK \mid negedge\ CLRB)$$

$$Q\ =\ D, \qquad If\ CLRB\sim = 0$$

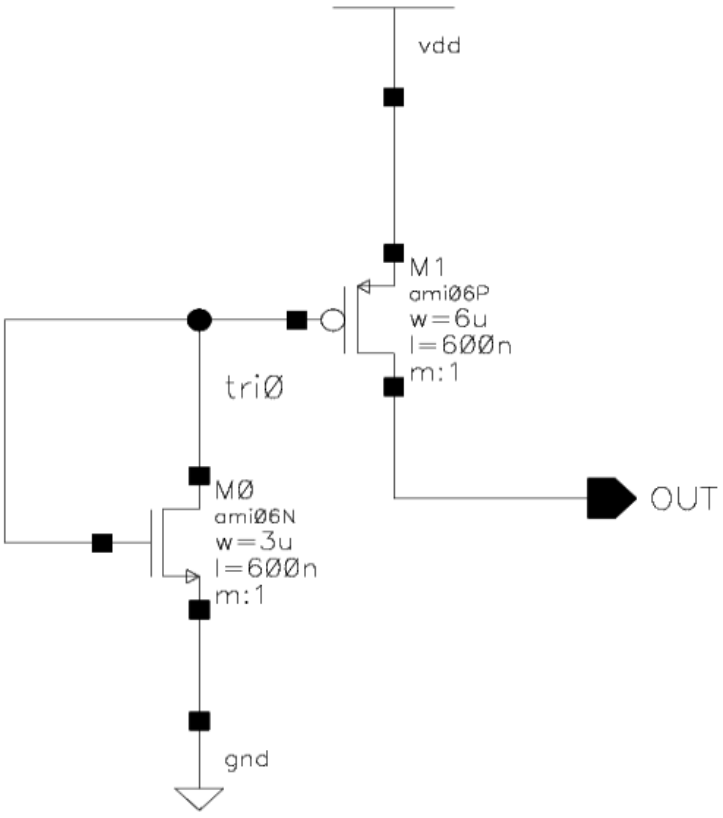
$$Q\ =\ 0, \qquad else$$

The D flip-flop is master-slave, rising-edge triggered with an asynchronous active-low clear signal. There exists no drive fight for the internal nodes.

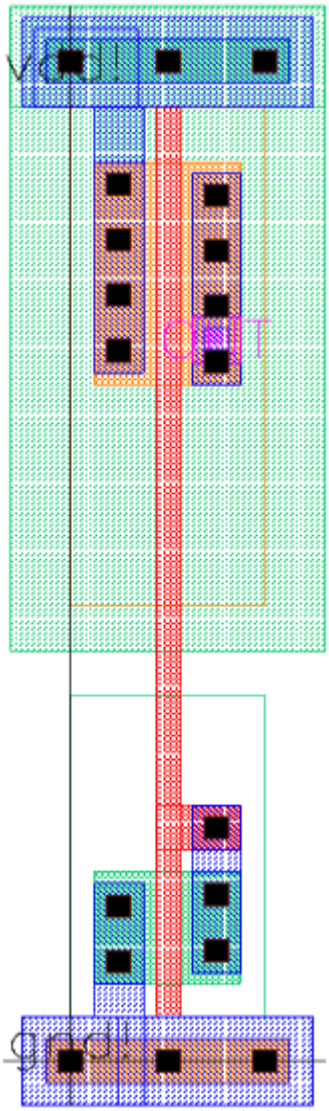
Standard Cell: TIEHI & TIELO

TIEHI

Schematic



Layout



Behavioral Model

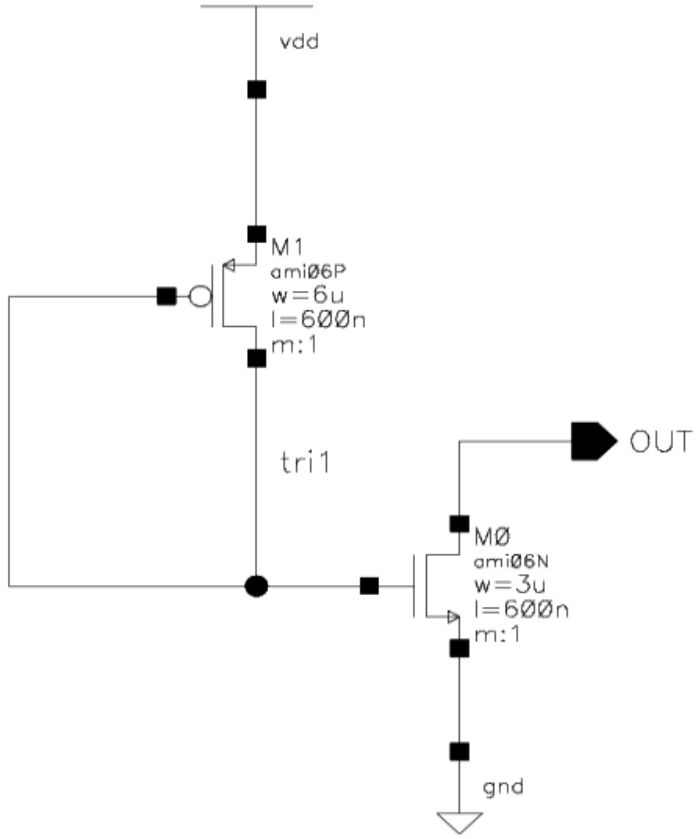
```
//Verilog HDL for "Lib_6710_05", "TIEHI" "behavioral"

module TIEHI ( OUT );
    output OUT;

supply1 OUT;

endmodule
```

User's Guide

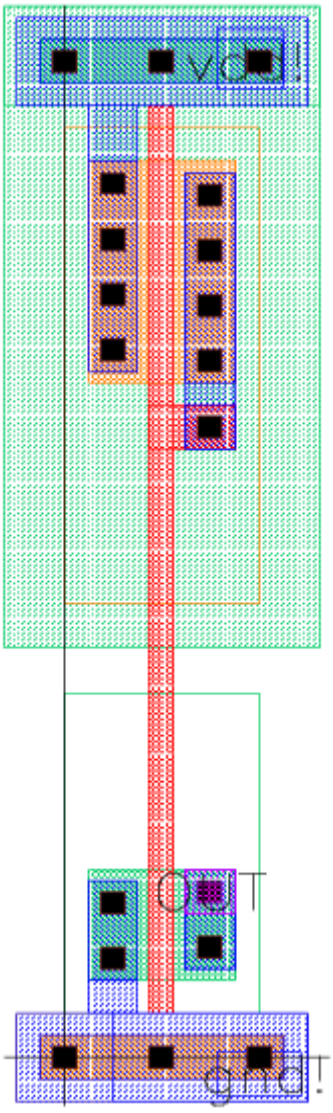
The TIEHI cell provides a connection to VDD. It has only one output, and no inputs. A diode-connected NMOS device provides a low voltage to the gate of the PMOS transistor. This PMOS device then generates a high voltage at its drain output.

TIELO

Schematic



Layout



Behavioral Model

```
//Verilog HDL for "Lib_6710_05", "TIELO" "behavioral"


module TIELO ( OUT );
    output OUT;

supply0 OUT;

endmodule
```

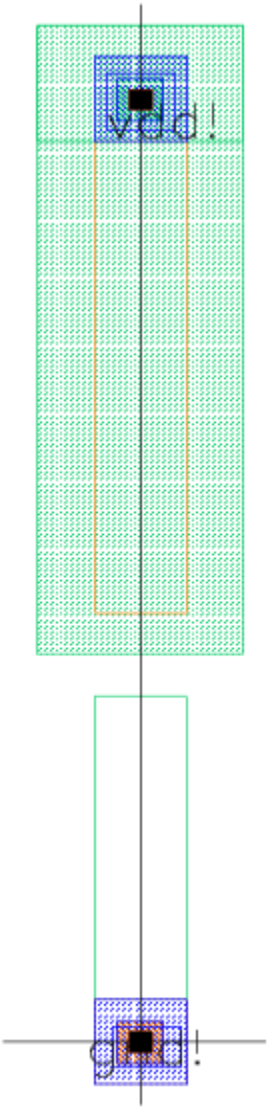
User's Guide

The TIELO cell provides a connection to ground. It has only one output, and no inputs. A diode-connected PMOS device provides a high voltage to the gate of the NMOS transistor. This NMOS device then generates a low voltage at its drain output.

Standard Cell: Filler

Filler

Layout

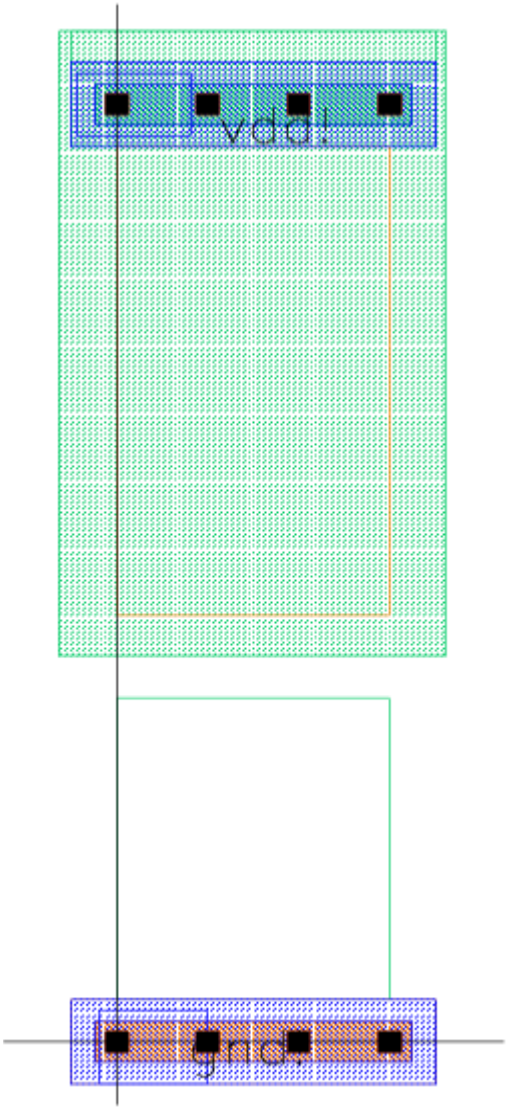


User's Guide

A filler cell is used by the place and route tool to fill-in the gaps in the standard cell rows. It has a width of 2.4 µm, and consists of VDD, GND, & NWELL layers. A single-width filler has only one contact width.

Filler4

Layout

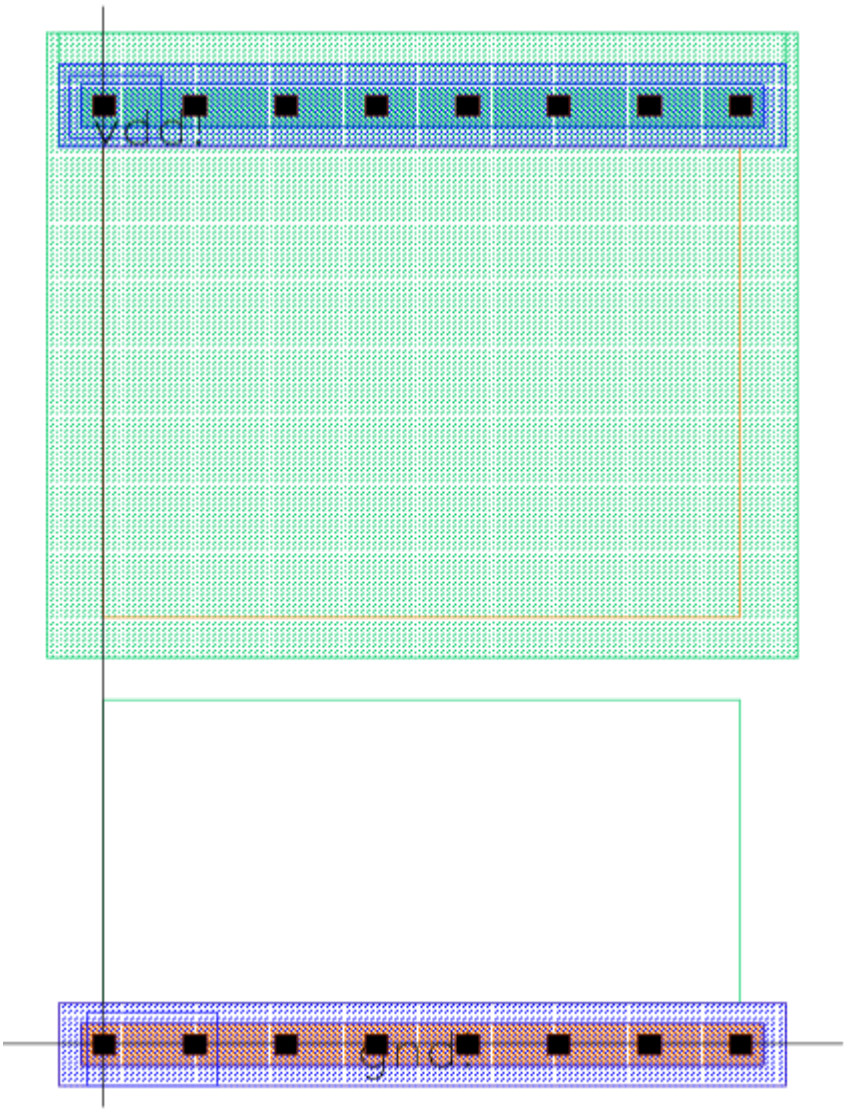


User's Guide

The Filler4 cell has a width of four contacts.

Filler8

Layout



User's Guide

The Filler8 cell has a width of eight contacts.