Arquitectura de Computadoras

HC11 SCI

Ing. Edgardo Gho

MODA/ LIR
MODB/ VSTBY
XTAL
EXTAL
E
IRQ
XIRQ/VPPE*
RESET
MODE CONTROL
OSC
CLOCK LOGIC
INTERRUPT LOGIC
ROM OR EPROM (SEE TABLE)
EEPROM (SEE TABLE)
RAM (SEE TABLE)
M68HC11 CPU
COP
TIMER SYSTEM
PERIODIC INTERRUPT
PULSE ACCUMULATOR
PAI
OC2
OC3
OC4
OC5/IC4/OC1
IC1
IC2
IC3
BUS EXPANSION ADDRESS
ADDRESS/DATA
R/W
AS
STROBE AND HANDSHAKE PARALLEL I/O
STRB
STRA
SERIAL PERIPHERAL INTERFACE SPI
SS
SCK
MOSI
MISO
SERIAL COMMUNICATION INTERFACE SCI
TxD
RxD
VDD
VSS
VRH
VRL
A/D CONVERTER
PORT A
PORT B
CONTROL
PORT C
CONTROL
PORT D
PORT E
PA7/PAI
PA6/OC2/OC1
PA5/OC3/OC1
PA4/OC4/OC1
PA3/OC5/IC4/OC1
PA2/IC1
PA1/IC2
PA0/IC3
PB7/ADDR15
PB6/ADDR14
PB5/ADDR13
PB4/ADDR12
PB3/ADDR11
PB2/ADDR10
PB1/ADDR9
PB0/ADDR8
PC7/ADDR7/DATA7
PC6/ADDR6/DATA6
PC5/ADDR5/DATA5
PC4/ADDR4/DATA4
PC3/ADDR3/DATA3
PC2/ADDR2/DATA2
PC1/ADDR1/DATA1
PC0/ADDR0/DATA0
STRB/R/W
STRA/AS
PD5/SS
PD4/SCK
PD3/MOSI
PD2/MISO
PD1/TxD
PD0/RxD
PE7/AN7
PE6/AN6
PE5/AN5
PE4/AN4
PE3/AN3
PE2/AN2
PE1/AN1
PE0/AN0

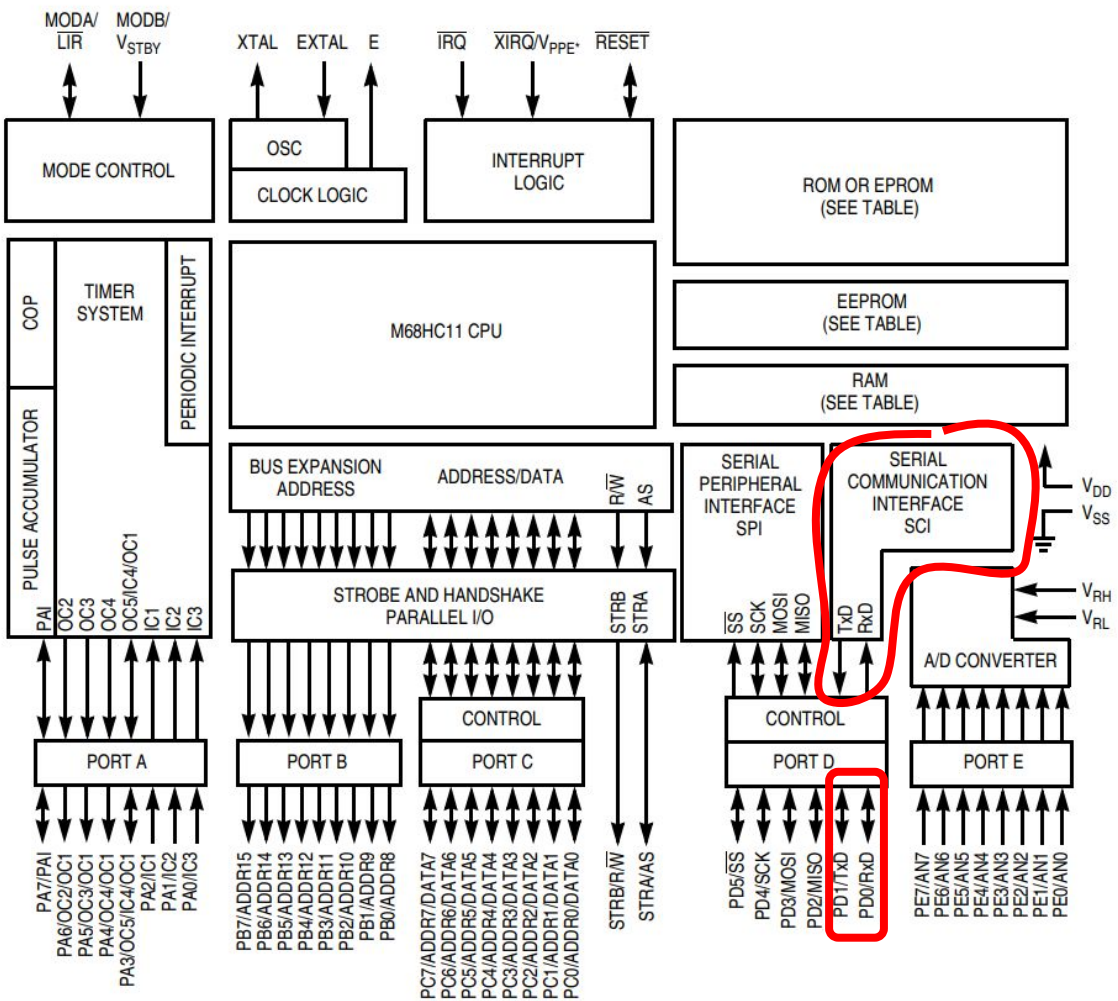
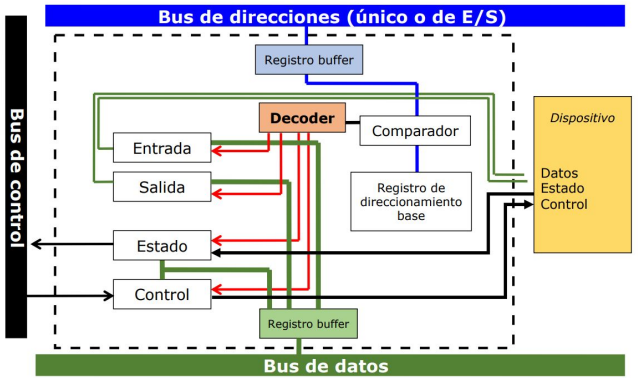
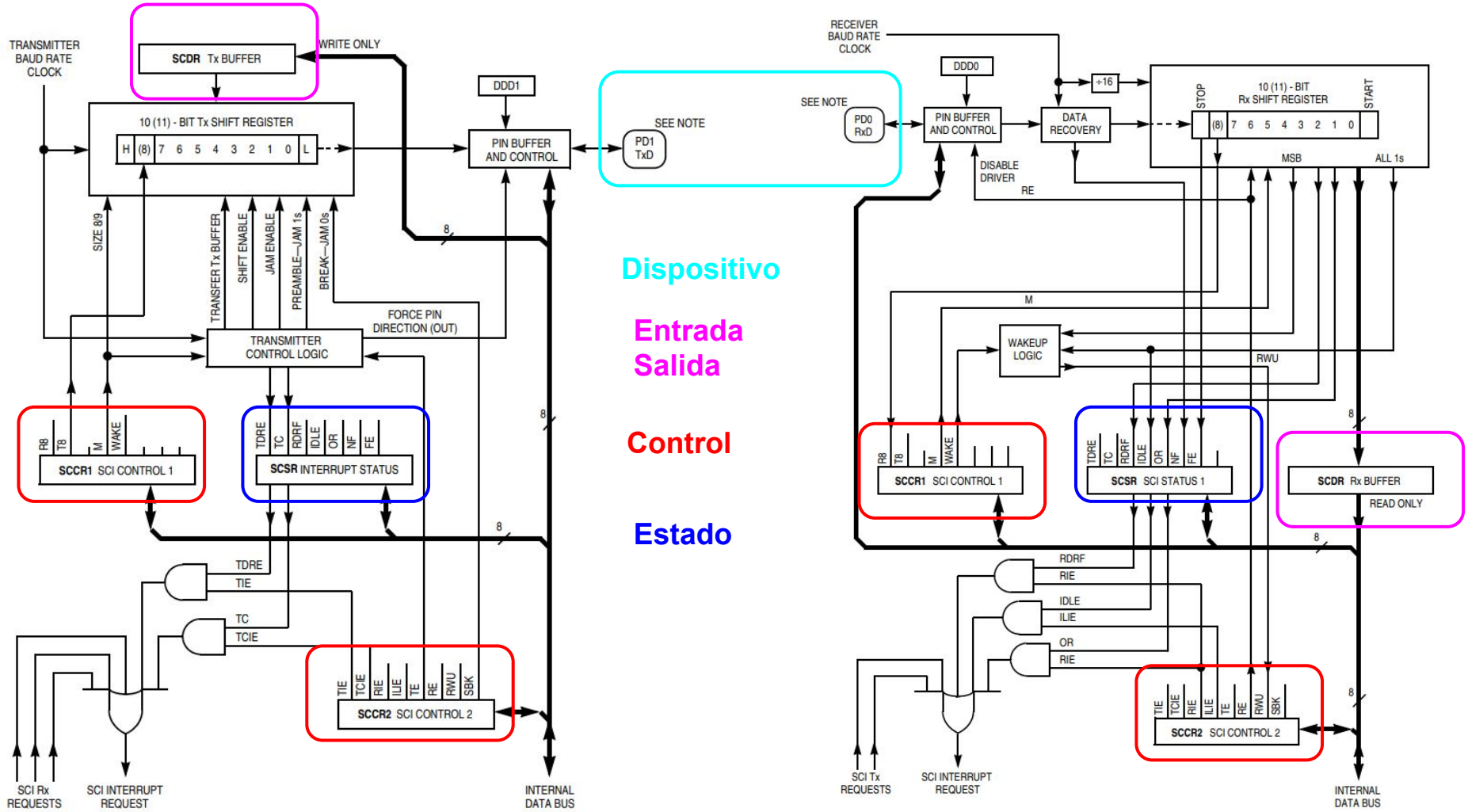


Diagrama básico de una interfaz




TRANSMITTER BAUD RATE CLOCK
SCDR Tx BUFFER
WRITE ONLY
10 (11) - BIT Tx SHIFT REGISTER
H (8) 7 6 5 4 3 2 1 0 L
DDD1
PIN BUFFER AND CONTROL
SEE NOTE
PD1 TxD
SIZE 8/9
TRANSFER Tx BUFFER
SHIFT ENABLE
JAM ENABLE
PREAMBLE—JAM 1s
BREAK—JAM 0s
FORCE PIN DIRECTION (OUT)
TRANSMITTER CONTROL LOGIC
RB T8 M WAKE
SCCR1 SCI CONTROL 1
TDRE TC RDRF IDLE OR NF FE
SCSR INTERRUPT STATUS
TDRE
TIE
TC
TCIE
TIE TCIE RIE ILIE TE RE RWU SBK
SCCR2 SCI CONTROL 2
SCI Rx REQUESTS
SCI INTERRUPT REQUEST
INTERNAL DATA BUS
RECEIVER BAUD RATE CLOCK
DDD0
÷16
SEE NOTE
PD0 RxD
PIN BUFFER AND CONTROL
DATA RECOVERY
STOP
10 (11) - BIT Rx SHIFT REGISTER
START
(8) 7 6 5 4 3 2 1 0
MSB
ALL 1s
DISABLE DRIVER
RE
M
WAKEUP LOGIC
RWU
R8 T8 M WAKE
SCCR1 SCI CONTROL 1
TDRE TC RDRF IDLE OR NF FE
SCSR SCI STATUS 1
SCDR Rx BUFFER
READ ONLY
RDRF
RIE
IDLE
ILIE
OR
RIE
TIE TCIE RIE ILIE TE RE RWU SBK
SCCR2 SCI CONTROL 2
SCI Tx REQUESTS
SCI INTERRUPT REQUEST
INTERNAL DATA BUS
Dispositivo
Entrada
Salida
Control
Estado

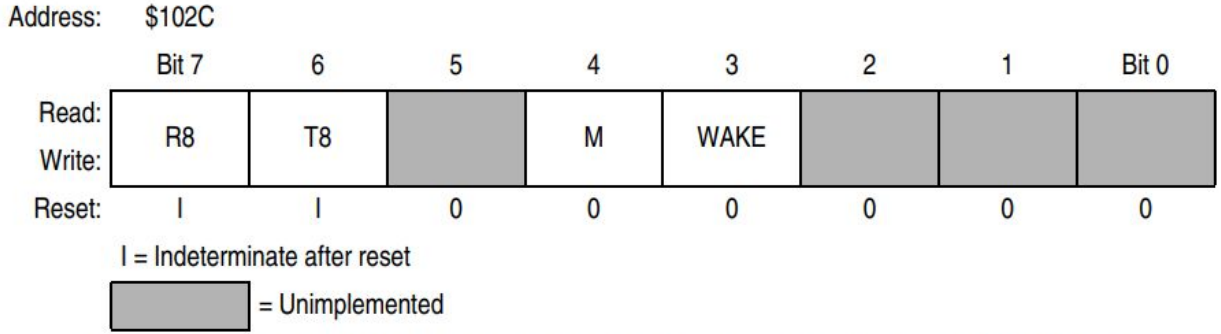


Figure 7-4. Serial Communications Control Register 1 (SCCR1)

R8 — Receive Data Bit 8

If M bit is set, R8 stores the ninth bit in the receive data character.

T8 — Transmit Data Bit 8

If M bit is set, T8 stores the ninth bit in the transmit data character.

Bit 5 — Unimplemented

Always reads 0

M — Mode Bit (select character format)

0 = Start bit, 8 data bits, 1 stop bit

1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle Bit

0 = Wakeup by IDLE line recognition

1 = Wakeup by address mark (most significant data bit set)

Table 7-1. Baud Rate Values

Prescaler Selects						Prescale Divide	Baud Set Divide	Crystal Frequency (MHz)					
								4.00	4.9152	8.00	10.00	12.00	16.00
								Bus Frequency (MHz)					
SCP2	SCP1	SCP0	SCR2	SCR1	SCR0			1.00	1.23	2.00	2.50	3.00	4.00
0	0	0	0	0	0	1	1	62500	76800	125000	156250	187500	250000
0	0	0	0	0	1	1	2	31250	38400	62500	78125	93750	125000
0	0	0	0	1	0	1	4	15625	19200	31250	39063	46875	62500
0	0	0	0	1	1	1	8	7813	9600	15625	19531	23438	31250
0	0	0	1	0	0	1	16	3906	4800	7813	9766	11719	15625
0	0	0	1	0	1	1	32	1953	2400	3906	4883	5859	7813
0	0	0	1	1	0	1	64	977	1200	1953	2441	2930	3906
0	0	0	1	1	1	1	128	488	600	977	1221	1465	1953
0	0	1	0	0	0	3	1	20833	25600	41667	52083	62500	83333
0	0	1	0	0	1	3	2	10417	12800	20833	26042	31250	41667
0	0	1	0	1	0	3	4	5208	6400	10417	13021	15625	20833
0	0	1	0	1	1	3	8	2604	3200	5208	6510	7813	10417
0	0	1	1	0	0	3	16	1302	1600	2604	3255	3906	5208
0	0	1	1	0	1	3	32	651	800	1302	1628	1953	2604
0	0	1	1	1	0	3	64	326	400	651	814	977	1302
0	0	1	1	1	1	3	128	163	200	326	407	488	651
0	1	0	0	0	0	4	1	15625	19200	31250	39063	46875	62500
0	1	0	0	0	1	4	2	7813	9600	15625	19531	23438	31250
0	1	0	0	1	0	4	4	3906	4800	7813	9766	11719	15625
0	1	0	0	1	1	4	8	1953	2400	3906	4883	5859	7813
0	1	0	1	0	0	4	16	977	1200	1953	2441	2930	3906
0	1	0	1	0	1	4	32	488	600	977	1221	1465	1953
0	1	0	1	1	0	4	64	244	300	488	610	732	977
0	1	0	1	1	1	4	128	122	150	244	305	366	488
0	1	1	0	0	0	13	1	4808	5908	9615	12019	14423	19231
0	1	1	0	0	1	13	2	2404	2954	4808	6010	7212	9615
0	1	1	0	1	0	13	4	1202	1477	2404	3005	3606	4808
0	1	1	0	1	1	13	8	601	738	1202	1502	1803	2404
0	1	1	1	0	0	13	16	300	369	601	751	901	1202
0	1	1	1	0	1	13	32	150	185	300	376	451	601
0	1	1	1	1	0	13	64	75	92	150	188	225	300
0	1	1	1	1	1	13	128	38	46	75	94	113	150
1	0	0	0	0	0	39	1	1603	1969	3205	4006	4808	6410
1	0	0	0	0	1	39	2	801	985	1603	2003	2404	3205
1	0	0	0	1	0	39	4	401	492	801	1002	1202	1603
1	0	0	0	1	1	39	8	200	246	401	501	601	801
1	0	0	1	0	0	39	16	100	123	200	250	300	401
1	0	0	1	0	1	39	32	50	62	100	125	150	200
1	0	0	1	1	0	39	64	25	31	50	63	75	100
1	0	0	1	1	1	39	128	13	15	25	31	38	50

Address: $102B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TCLR	SCP2	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
Reset:	0	0	0	0	0	U	U	U
U = Unaffected		**0**	**1**	**1**		**0**	**0**	**0**

Figure 7-7. Baud Rate Register (BAUD)

```
;Seteo el puerto serie en 9600 bauds
;Esto se define en la pagina 113 del datasheet
LDAA        #%00110000
STAA        BAUD
```

Address:	$102D							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 7-5. Serial Communications Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable Bit
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable Bit
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable Bit
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle-Line Interrupt Enable Bit
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable Bit
When TE goes from 0 to 1, one unit of idle character time (logic 1) is queued as a preamble.
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable Bit
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wakeup Control Bit
0 = Normal SCI receiver
1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break

```
;Prendo las interrupciones para recibir serie
; Ver pagina 111 del manual
LDAA        #%00101100
STAA        SCC2
```

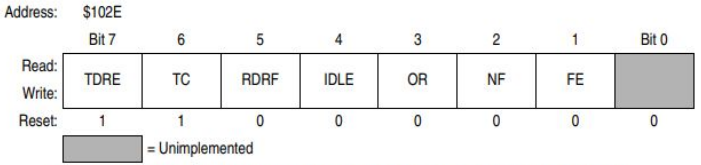


Figure 7-6. Serial Communications Status Register (SCSR)

TDRE — Transmit Data Register Empty Flag

This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR with TDRE set and then writing to SCDR.

0 = SCDR busy
0 = SCDR empty

TC — Transmit Complete Flag

This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR with TC set and then writing to SCDR.

0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag

This flag is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR with RDRF set and then reading SCDR.

0 = SCDR empty
1 = SCDR full

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR with IDLE set and then reading SCDR.

0 = RxD line active
1 = RxD line idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR with OR set and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR with NF set and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

```
;;; Posiciones de memoria
;;; donde se controla el
;;; puerto serie
BAUD        EQU     $102B
SCC2        EQU     $102D
SCDR        EQU     $102F
SCSR        EQU     $102E
SERIE       EQU     $FFD6
```

```
;Seteo el puerto serie en 9600 bauds
;Esto se define en la pagina 113 del datasheet
LDAA        #%00110000
STAA        BAUD

;Prendo las interrupciones para recibir serie
; Ver pagina 111 del manual
LDAA        #%00101100
STAA        SCC2
```

```
ORG SERIE
DW  SERIAL_ISR
ORG RESET
DW  MAIN
```

```
SERIAL_ISR:
        ;; Hay que leer SCSR y verificar cual fue la interrupcion
        ;; que disparo la rutina. Como en este caso solo esta encendida
        ;; la interrupcion de recepcion de bytes, solo leemos el valor
        ;; pero no verificamos nada. El Hardware REQUIERE leer este valor
        ;; siempre aunque no lo usemos para nada. Esto limpia internamente
        ;; los flags sino vuelve a dispararse la interrupcion luego del RTI.
        LDAA        SCSR
        LDAA        SCDR ;;Cargamos el dato que llego por serie en A
        ;; Hacemos algo con el dato...
        RTI
```

```
;;;;;;;;; Rutina SendSerie
;;;;
;;;;  Envia por puerto serie byte a byte los valores del buffer.
;;;;  NO utiliza interrupciones, por ende debe esperar a que cada
;;;;  byte sea enviado para enviar el siguiente.
SendSerie:
        ; Busco el fin del buffer
        LDAB        BUFFPOINTER
        LDX         #BUFFER
        ABX

LoopSend:
        ; Verifico si estoy al principio del buffer
        DEX
        CPX     #BUFFER-1
        BEQ     FinLoop
        LDAA        0,X
        ;En A tengo el valor a enviar
        ;Necesito verificar que el puerto serie
        ;esta libre para enviar bytes. Esto se hace
        ;leyendo el bit mas significativo de SCSR.
        ; Si el bit esta en 0, entonces se puede transmitir
WaitTX      LDAB        SCSR
        ANDB        #%10000000
        BEQ     WaitTX
        ;Para transmitir escribo el byte en SCDR
        STAA        SCDR
        BRA     LoopSend
FinLoop:
        CLR     BUFFPOINTER
        RTS
```

Address: $102E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
Reset:	1	1	0	0	0	0	0	0

= Unimplemented

Figure 7-6. Serial Communications Status Register (SCSR)

TDRE — Transmit Data Register Empty Flag

This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR with TDRE set and then writing to SCDR.

0 = SCDR busy

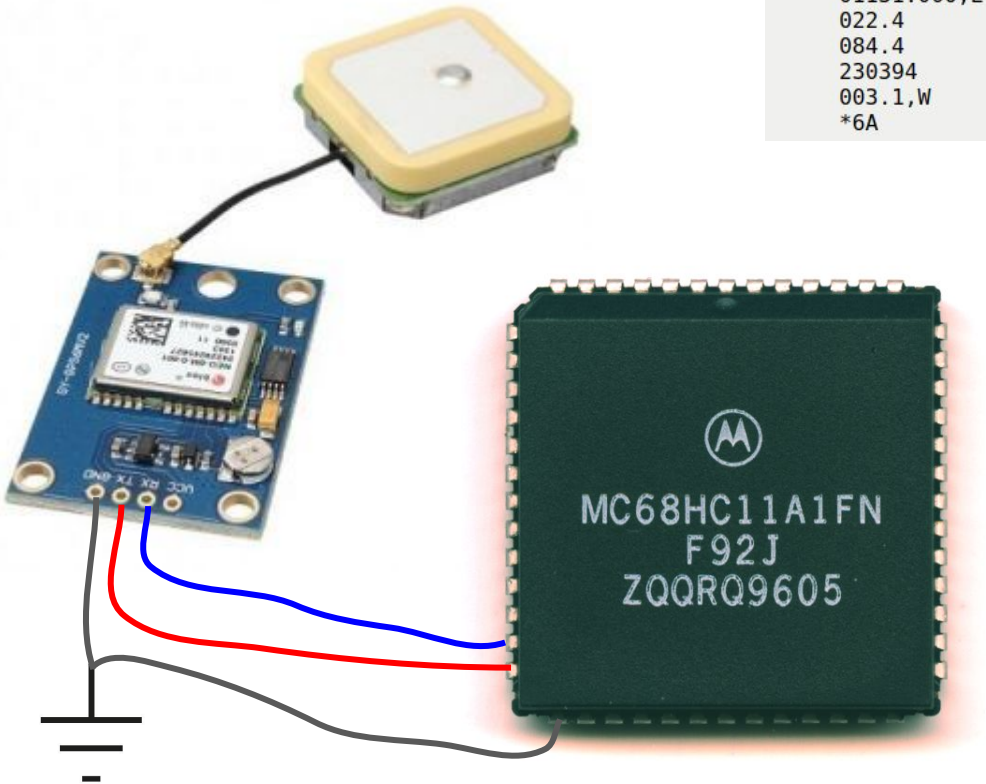
0 = SCDR empty

NMEA

RMC - NMEA has its own version of essential gps pvt (position, velocity, time) data. It is called RMC,

```
$GPRMC,123519,A,4807.038,N,01131.000,E,022.4,084.4,230394,003.1,W*6A

Where:
     RMC          Recommended Minimum sentence C
     123519       Fix taken at 12:35:19 UTC
     A            Status A=active or V=Void.
     4807.038,N   Latitude 48 deg 07.038' N
     01131.000,E  Longitude 11 deg 31.000' E
     022.4        Speed over the ground in knots
     084.4        Track angle in degrees True
     230394       Date - 23rd of March 1994
     003.1,W      Magnetic Variation
     *6A          The checksum data, always begins with *
```



NMEA Protocol Frame