Design Specification

1. Application Overview:

The design is a 3-bit parity generator circuit with the ability to count up cyclically in even, odd, pause, reset or normal counting modes.

The circuit uses a 7-segment LED display to show the current count.

2. System Setup:

The circuit operates synchronously with the clock signal (CLK).

The circuit has four control signals:

- **RESET**: resets the circuit to the initial state.
- **PAUSE**: pauses the counting operation.
- **EVEN** : selects the even counting mode.
- **ODD** : selects the odd counting mode.

The circuit has an output Q[2:0] representing the current count value.

The circuit has an output LED_7SEG[6:0] for controlling the 7-segment display.

3. Operating Modes:

The circuit operates in the following truth table:

Input				Output			
EVEN	**ODD**	**PAUSE**	**RESET**	Q_n	Q_{n+1}	LED_n	LED_{n+1}
0	0	0	0	000	001	1111110	0110000
0	0	0	0	001	010	0110000	1101101
0	0	0	0	010	011	1101101	1111001
0	0	0	0	011	100	1111001	0110011
0	0	0	0	100	101	0110011	1011011
0	0	0	0	101	110	1011011	1011111
0	0	0	0	110	111	1011111	1110000
0	0	0	0	111	000	1110000	1111110
0	0	0	1	xxx	000	xxxxxxx	1111110
0	0	1	0	000	000	1111110	1111110
0	0	1	0	001	001	0110000	0110000
0	0	1	0	010	010	1101101	1101101

0	0	1	0	011	011	1111001	1111001
0	0	1	0	100	100	0110011	0110011
0	0	1	0	101	101	1011011	1011011
0	0	1	0	110	110	1011111	1011111
0	0	1	0	111	111	1110000	1110000
0	0	1	1	xxx	000	xxxxxxx	1111110
0	1	0	0	001	011	0110000	1111001
0	1	0	0	011	101	1111001	1011011
0	1	0	0	101	111	1011011	1110000
0	1	0	0	111	001	1110000	0110000
0	1	0	1	xxx	000	xxxxxxx	1111110
0	1	1	0	001	001	0110000	0110000
0	1	1	0	011	011	1111001	1111001
0	1	1	0	101	101	1011011	1011011
0	1	1	0	111	111	1110000	1110000
0	1	1	1	xxx	000	xxxxxxx	1111110
1	0	0	0	000	010	1111110	1101101
1	0	0	0	010	100	1101101	0110011
1	0	0	0	100	110	0110011	1011111
1	0	0	0	110	000	1011111	1111110
1	0	0	1	xxx	000	xxxxxxx	1111110
1	0	1	0	000	000	1111110	1111110
1	0	1	0	010	010	1101101	1101101
1	0	1	0	100	100	0110011	0110011
1	0	1	0	110	110	1011111	1011111
1	0	1	1	xxx	000	xxxxxxx	1111110
1	1	0	0	000	001	1111110	0110000
1	1	0	0	001	010	0110000	1101101
1	1	0	0	010	011	1101101	1111001
1	1	0	0	011	100	1111001	0110011
1	1	0	0	100	101	0110011	1011011
1	1	0	0	101	110	1011011	1011111
1	1	0	0	110	111	1011111	1110000
1	1	0	0	111	000	1110000	1111110
1	1	0	1	xxx	000	xxxxxxx	1111110
1	1	1	0	000	000	1111110	1111110

1	1	1	0	001	001	0110000	0110000
1	1	1	0	010	010	1101101	1101101
1	1	1	0	011	011	1111001	1111001
1	1	1	0	100	100	0110011	0110011
1	1	1	0	101	101	1011011	1011011
1	1	1	0	110	110	1011111	1011111
1	1	1	0	111	111	1110000	1110000
1	1	1	1	xxx	000	xxxxxxx	1111110

- **RESET:** When RESET is activated, Q is set to 0.
- **PAUSE:** When PAUSE is activated, the circuit stops counting and holds the current value of Q.
- **Normal Counting:** When both EVEN and ODD are either disabled or enabled simultaneously, the circuit counts up cyclically from 0 to 7.
- **Even Counting:** When EVEN is activated, the circuit counts only even numbers (0, 2, 4, 6).
- **Odd Counting:** When ODD is activated, the circuit counts only odd numbers (1, 3, 5, 7).

4. I/O Definition and Protocol:

- **CLK:** Clock signal, triggered on the rising edge (posedge).
- **RESET:** Reset signal, active high.
- **PAUSE:** Pause signal, active high.
- **EVEN:** Even counting mode selection signal, active high.
- **ODD:** Odd counting mode selection signal, active high.
- **Q[2:0]:** 3-bit output representing the current count.
- **LED_7SEG[6:0]:** 7-bit output controlling the 7-segment LED display.