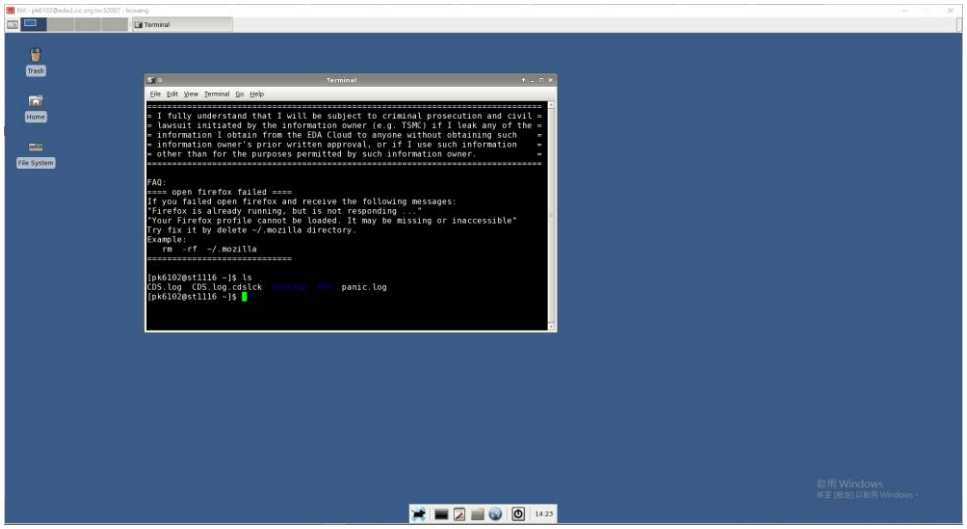
Overview of EDA Cloud

- Provide **EDA tools**
  - Design Compiler、IC Compiler、PrimeTime、Milkway、VCS-MX、Verdi…
- Provide cell based and full custom process data
  - Apply **TSMC90GUMTM**(90nm)
- Edit and manage at **frontend** and compute at **backend**

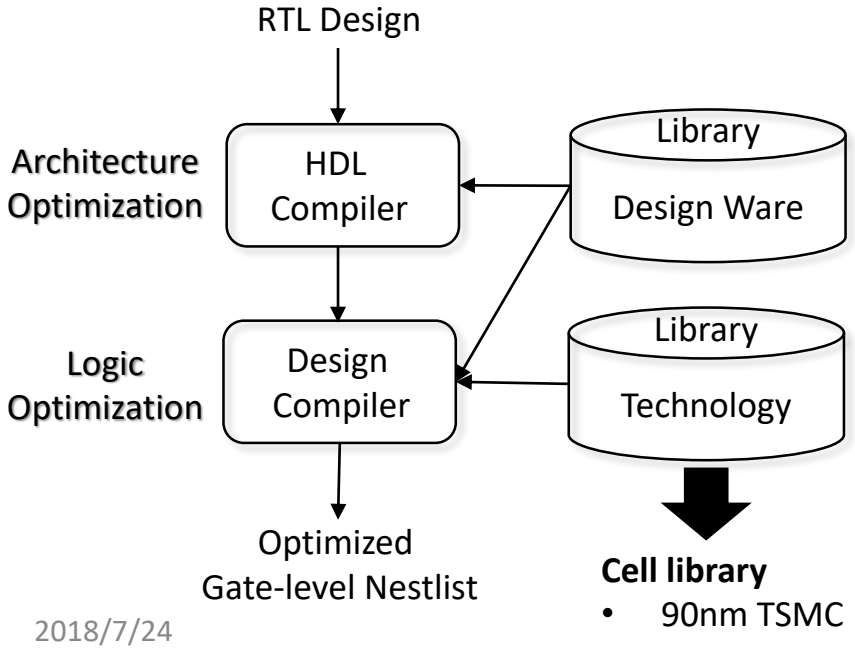
- Operation details
  - Connect w/ NX Client
  - Apply password of half hour



View of EDA cloud

Review Flow of Logic Synthesis

- HDL compiler
  - Translate RTL with GTECH library(no timing information)
- Design compiler
  - Map design blocks to gate level design with cell library(have timing information)



Flow of Design Compiler

1. Input: analyze, elaborate
2. Link: link
3. Set size&mode of wire load: set_wire_load_model
4. Synthesis: compile
5. Report: report_timing , report_power, report_constraint
6. Design saving: write(ddc, netlist), write_sdf, write_sdc

Synthesis Script of NVDLA

- NVIDIA provide a template of synthesis script(.tcl) <Git: Link>
- Design compiler run with synthesis script
- Main configures of synthesis script
  - Import Process Data to Design Compiler

```
export TARGET_LIB="/cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db"
export LINK_LIB="\
        /cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/syn/dw_foundation.sldb \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/gtech.db \
"
```

  - Use wireload Model(non-physical synthesis)

```
wire_load("tsmc090_wl20") {
  resistance  : 8.5e-8;
  capacitance : 1.5e-4;
  area        : 0.7;
  slope       : 133.334;
  fanout_length       (1,133.334);
}
```

Result of Design Compiler

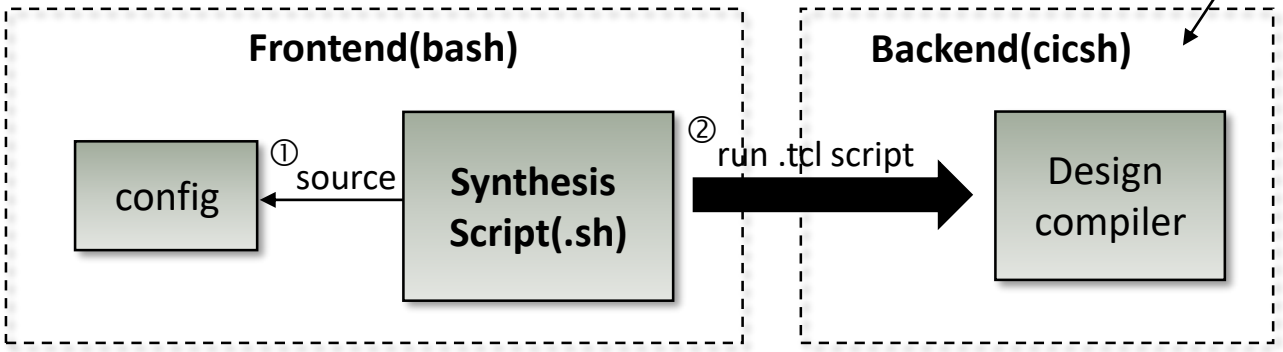
- Cost 8 days
- Synthesis of NVDLA with 8 parts
  - NVNVDLA_partition_a
    - Modules: rt_cmac_b2cacc, cacc, clk_over_on_sync, rst
  - NVNVDLA_partition_c
    - Modules: rt_cacc2glb, rt_csb2cacc, rt_csc2cmac, rt_csc2cmac_b, cbuf, cdma, csc, clk_over_on_sync, rst
  - NVNVDLA_partition_m
    - Modules: cmac, clk_over_on_sync, rst
  - NVNVDLA_partition_o
    - Modules: rt_csb2cmac, rt_csc2cmac_a, bdma, cdp, csb_master, cvif, glb, mcif, pdp, rubik, clk_over_on_sync, rst, falcon_reset
  - NVNVDLA_partition_p
    - Modules: rt_cmac_a2cacc, sdp, clk_over_on_sync, rst

```
-rw-r--r-- 1 pk6102 TN90GUTM 141207069 Jan 12 03:54 NV_NVDLA_partition_a.gv
-rw-r--r-- 1 pk6102 TN90GUTM       376 Jan 12 03:54 NV_NVDLA_partition_a.sdc
-rw-r--r-- 1 pk6102 TN90GUTM 361966420 Jan 14 07:37 NV_NVDLA_partition_c.gv
-rw-r--r-- 1 pk6102 TN90GUTM       376 Jan 14 07:36 NV_NVDLA_partition_c.sdc
-rw-r--r-- 1 pk6102 TN90GUTM 471257804 Jan 18 19:17 NV_NVDLA_partition_p.gv
-rw-r--r-- 1 pk6102 TN90GUTM       376 Jan 18 19:15 NV_NVDLA_partition_p.sdc
[pk6102@st1116 net]$
-rw-r--r-- 1 pk6102 TN90GUTM 100786044 Jan 19 14:38 NV_NVDLA_partition_o.gv
-rw-r--r-- 1 pk6102 TN90GUTM       376 Jan 19 14:37 NV_NVDLA_partition_o.sdc
```

Netlist(.gv) of each parts in NVDLA

Problem of Run .tcl Script with DC

- Problem
  - Env problem synthesis script
  - EDA cloud run Rdc_shell in backend with shell of CIC(cicsh)



- Solution
  - Set required environment parameters one by one in .tcl script
  - Revise synthesis script

Revised Place of Script(EDA cloud can't export any file)

- syn_launch.sh

```
elif [ "$mode" == "wlm" ] ; then
    echo "[INFO]: Running DC (non-physical/Wireload model)..."
        export SYN_MODE=$mode
#       for module in $modules
#       do
                export MODULE=$module
                export RTL_DEPS="$BUILD_NAME/scripts/${module}.files.vc"
                COMMAND_PREFIX_PATCHED="${COMMAND_PREFIX/\<MODULE\>/$module}"
                COMMAND_PREFIX_PATCHED="${COMMAND_PREFIX_PATCHED/\<LOG\>/$LOG_DIR}"
                if [ -z "$restore_db" ] ; then
                    echo $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f ../$BUILD_NAME/scripts/dc_run.tcl -output_log_file ../$LOG_DIR/${module}_${SYN_MODE}.log
                    echo `pwd`
                    #cd $BUILD_NAME
                    #$COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f ../$BUILD_NAME/scripts/dc_run.tcl -output_log_file ../$LOG_DIR/${module}_${SYN_MODE}.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f $BUILD_NAME/scripts/dc_run_a.tcl -output_log_file $LOG_DIR/NV_NVDLA_partition_a_${SYN_MODE}.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f $BUILD_NAME/scripts/dc_run_c.tcl -output_log_file $LOG_DIR/NV_NVDLA_partition_c_${SYN_MODE}.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f $BUILD_NAME/scripts/dc_run_o.tcl -output_log_file $LOG_DIR/NV_NVDLA_partition_o_${SYN_MODE}.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f $BUILD_NAME/scripts/dc_run_m.tcl -output_log_file $LOG_DIR/NV_NVDLA_partition_m_${SYN_MODE}.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -no_gui -f $BUILD_NAME/scripts/dc_run_p.tcl -output_log_file $LOG_DIR/NV_NVDLA_partition_p_${SYN_MODE}.log
                else
                    export RESTORE_DB=$restore_db
                    echo $COMMAND_PREFIX_PATCHED $DC_PATH  -f ../$BUILD_NAME/scripts/dc_interactive.tcl -output_log_file ../$LOG_DIR/${module}_${SYN_MODE}.interactive.log
                    echo `pwd`
                    #cd $BUILD_NAME
                    #$COMMAND_PREFIX_PATCHED $DC_PATH  -f ../$BUILD_NAME/scripts/dc_interactive.tcl -output_log_file ../$LOG_DIR/${module}_${SYN_MODE}.interactive.log
                    $COMMAND_PREFIX_PATCHED $DC_PATH  -f $BUILD_NAME/scripts/dc_interactive.tcl -output_log_file $LOG_DIR/${module}_${SYN_MODE}.interactive.log
                fi
#           done
```

- config.sh

```
export TOP_MACS="NV_NVDLA_partition_a NV_NVDLA_partition_c NV_NVDLA_partition_o NV_NVDLA_partition_m NV_NVDLA_partition_p"

export NVDLA_ROOT="/project/dr196/pk61/pk6102/nvdla/hw-nvdlav1"

# Where do I find the RTL source verilog/system verilog files?
export RTL_SEARCH_PATH=" \
        $(ls -d ${NVDLA_ROOT}/vmod/nvdla/*) \
        ${NVDLA_ROOT}/vmod/rams \
        ${NVDLA_ROOT}/vmod/vlibs \
"
export EXTRA_RTL=" \
        ${NVDLA_ROOT}/vmod/nvdla/nocif/NV_NVDLA_XXIF_libs.v \
"

# If there are verilog header files, where do I find them?
export RTL_INCLUDE_SEARCH_PATH=" \
        ${NVDLA_ROOT}/vmod/include \
"
```

```
export TARGET_LIB="/cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db"
export LINK_LIB="\
        /cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/syn/dw_foundation.sldb \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/gtech.db \
"
export MW_LIB=""
export TF_FILE=""
export TLUPLUS_FILE=""
export TLUPLUS_MAPPING_FILE=""
export MIN_ROUTING_LAYER=""
export MAX_ROUTING_LAYER=""
export HORIZONTAL_LAYERS=""
export VERTICAL_LAYERS=""
export WIRELOAD_MODEL_NAME="tsmc090_wl20"
export WIRELOAD_MODEL_FILE=""
export DONT_USE_LIST=""
```

Revised Place of Script(EDA cloud can't export any file)

- dc_run.tcl

```
# ====================
# Setup variables/procs
# ====================

set synMsgInfo "Info:"
set synMsgErr  "Error:"
set synMsgWarn "Warning:"
set MODULE "NV_NVDLA_partition_a"
```

```
# Directories
setVar CONS_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/cons
setVar DB_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/db
setVar LOG_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/log
setVar REPORT_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/report
setVar NET_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/net
setVar FV_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/fv
setVar MW_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/mw
setVar DLIB_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/design_lib
setVar DEF_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/def
setVar SCRIPTS_DIR /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/scripts
#setVar SEARCH_PATH "."
setVar SEARCH_PATH /project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn
setVar RTL_EXTENSIONS ".v .sv .gv"
setVar RTL_INCLUDE_EXTENSIONS=".vh .svh"
```

```
# From config
setVar TOP_NAMES "NV_NVDLA_partition_a NV_NVDLA_partition_c NV_NVDLA_partition_o NV_NVDLA_partition_m NV_NVDLA_partition_p"
setVar NVDLA_ROOT "/project/dr196/pk61/pk6102/nvdla/hw-nvdlav1"
setVar RTL_SEARCH_PATH " \
        $(ls -d ${NVDLA_ROOT}/vmod/nvdla/*) \
        ${NVDLA_ROOT}/vmod/rams \
        ${NVDLA_ROOT}/vmod/vlibs \
"
setVar EXTRA_RTL " \
        ${NVDLA_ROOT}/vmod/nvdla/nocif/NV_NVDLA_XXIF_libs.v \
"
setVar RTL_INCLUDE_SEARCH_PATH " \
        ${NVDLA_ROOT}/vmod/include \
"
setVar DEF "def"
setVar CONS "config"
setVar TARGET_LIB "/cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db"
setVar LINK_LIB "\
        /cad/CBDK/CBDK_TSMC90GUTM_Arm_v1.2/CIC/SynopsysDC/db/slow_hvt.db \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/syn/dw_foundation.sldb \
        /cad/synopsys/synthesis/2015.06-sp1/libraries/syn/gtech.db \
"
setVar WIRELOAD_MODEL_NAME "tsmc090_wl20"
setVar AREA_RECOVERY 1
setVar INCREMENTAL_RECOMPILE_COUNT 2
setVar RTL_DEPS "/project/dr196/pk61/pk6102/nvdla/hw-nvdlav1/nvdla_syn/scripts/NV_NVDLA_partition_a.files.vc"
```