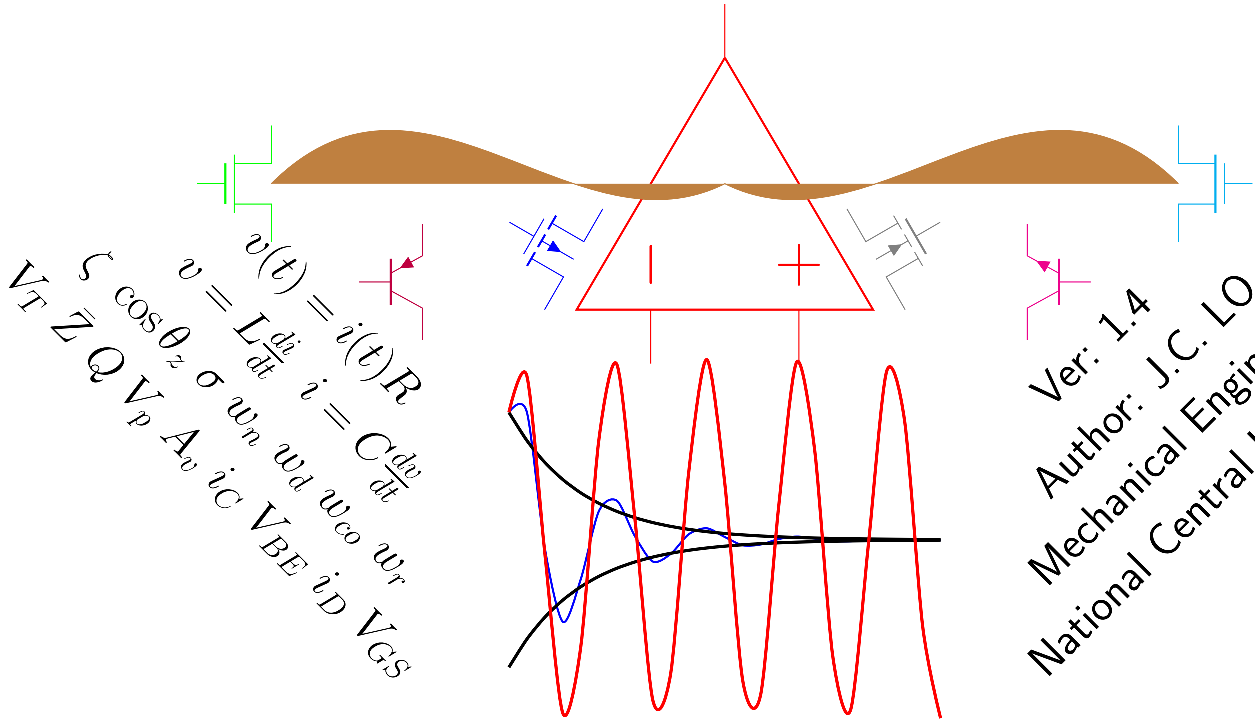

Ver: 1.4
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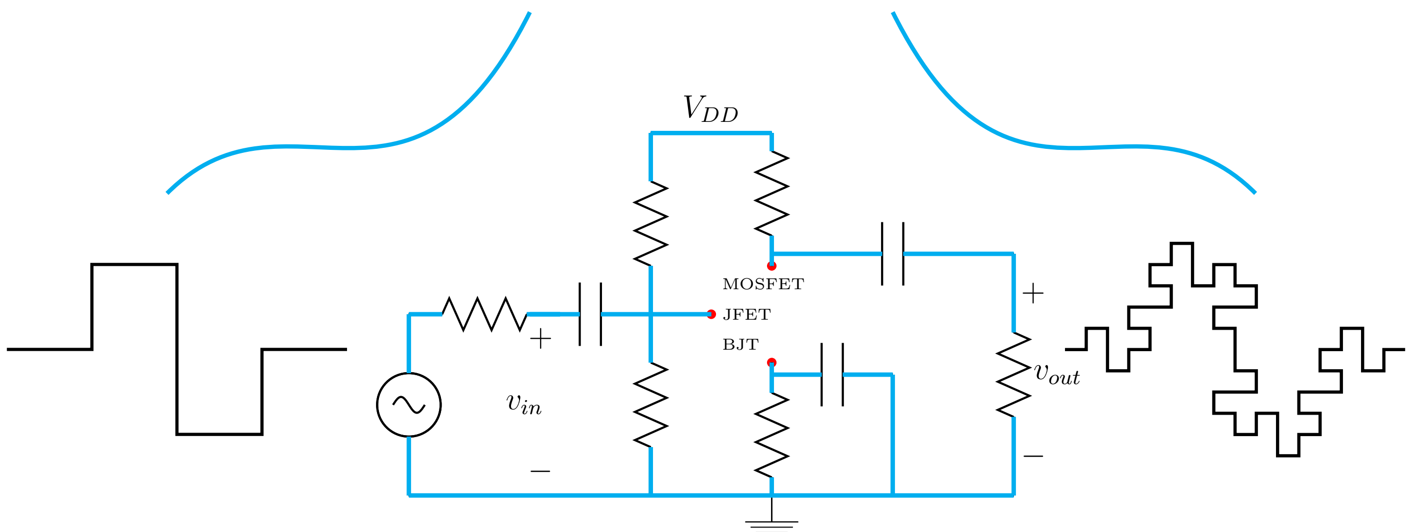
eThinking in Circuits

with PSpice©

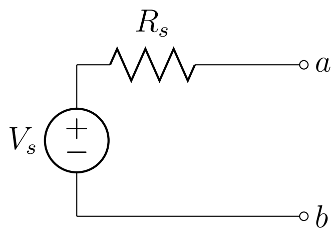
Date released August 23, 2011

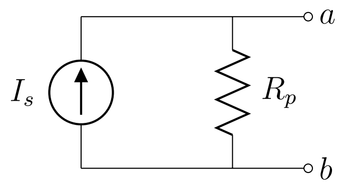


Key Equations and Formulae

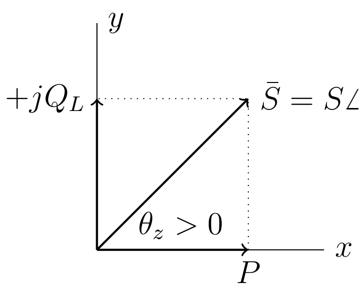
G(iga)=10^9, M(ega)=10^6, K(ilo)=10^3, m(illi)=10^{-3}, μ(micro)=10^{-6}, n(ano)=10^{-9}, p(ico)=10^{-12}.

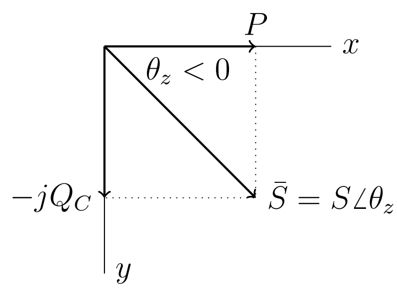
$$v = iR, \quad v = L\frac{di}{dt}, \quad i = C\frac{dv}{dt}$$





$$\bar{Z}_R = R, \quad \bar{Z}_C = \frac{1}{jwC}, \quad \bar{Z}_L = jwL, \quad V_{\max} = \sqrt{2}V_{rms}, \quad \theta_z = \theta - \phi = cos^{-1}pf$$





$$P = V_{rms}I_{rms}\cos(\theta - \phi) = I_{rms}^2 R = \frac{V_{rms}^2 R}{Z^2}, \quad Q = V_{rms}I_{rms}\sin(\theta - \phi) = I_{rms}^2 X = \frac{V_{rms}^2 X}{Z^2},$$

Cutoff Region: For $v_{GS} < V_{to}$, $i_D = 0$.
Triode Region (linear region): $v_{DS} \leq v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$, $i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$
Saturation Region: $v_{DS} > v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$, $i_D = K(v_{GS} - V_{to})^2$
Boundary region: $v_{DS} = v_{GS} - V_{to}$, $i_D = Kv_{DS}^2$

To my wife, Lisa; son, Albert; and daughter, Jannie.

Preface

After years of teaching, spark the thought providing students with a quick and basic understanding of the fundamentals of Electrical Engineering. Endless effort results in this lecture note.

The lecture note is divided into 7 chapters:

Chapter 1 introduces basic electrical quantities and fundamental law of circuit elements, showing definitions and $v - i$ relationship of each elements – Ohm's law, Faraday's law and Henry's law.

Equipped with the basis, Chapter 2 addresses notions of circuits composed of electrical sources and circuit elements and introduces circuit laws that govern the currents flowing in branches and voltages across each elements. With the fundamentals established, we are ready to study solving DC circuits.

Chapter 3 studies circuit theorems that can be utilized to find equivalent circuits that generate identical $v - i$ characteristics at the terminals of interests. Following the network reduction, loop-current and node-voltage techniques are introduced to analyze various circuits containing dependent and/or independent sources.

Chapter 4 begins to present material for analysis of AC circuits. Exponential signal is first introduced to convert cosine functions into an exponential signals that preserve their exponential forms when a differentiating or integrating operator is executed. Following that, the concept of impedance is addressed and the phasor concept is debuted, removing the element of time characteristics and allowing AC circuits be analyzed by the Ohm's law techniques – those techniques found in DC analysis. Lastly in Chapter 4, AC power is taught and phasor diagram is addresses to introduce the notions of lead and lag.

Having studied the steady-state analysis of AC circuits, Chapter 5 investigates transient response of AC circuits when switches are involved. Since AC circuits are linear systems in nature. The circuit elements – capacitors and inductors – are characterized by a first-order or second-order ordinary differential equation, unable to change instantaneously. As such, AC circuits inherits transient features that are interesting to analyze.

So much so for fixed frequency analysis in AC circuits, Chapter 6 investigates electrical network with varying frequency, introducing sinusoidal signals. In fact, all the electrical currents and voltages in a linear circuit are function of angular frequency, meaning the input signals are allowed to vary. In addition, the impedance of inductors and capacitors is also function of frequency, allowing special network such as filter to be analyzed and designed for special applications.

Chapter 7 addresses basic electronic devices. All problems, either end-of-chapter or at the bottom of each page, are designed to help students gain more insights and therefore, to consolidate the principles developed in this lecture. Moreover, brief answers are provided for reference.

The main goal of this note is to help students overcome the anxiety toward the study of Electrical Engineering that they sometimes bring with them. I have been rewarded to see the fact that students move from anxiety to curiosity does happen.

Happy Studying!
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What's new in Version 1.4:

- All graphs are re-drawn and, mostly, colored using Matlab or pgfplots
- Typeset by LaTeX2e(MiKTex 2.9.3972.0), pgfCVS2010-9-28_TDS, circuitikz 0.2.3.
- Problem sets at the end of chapters and answers are provided.
- Four new chapters on electronics are attached.
- Summary sections for every chapter are added.
- Index and thumb index are formally added.
- Book front and back covers make their first debut.
- Preface rewritten and polished.
- Key equations and formulae added.
- Numerous typo errors corrected. (I take credits for all typos and mistakes in this Reader.)
- PSpice experiments are added and steps to run the program are included.
- Also written by the author **iThiking in Control with Matlab**.

Version 1.0

- Texts started typeset in Latex2e.
- MATLAB and PSpice were not emphasized but used.
- Graphs were plotted using Visio, some hand-drawn.

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Chapter 1

Introduction

In this lecture, only fundamental electrical circuits are taught and analyzed because they constitute the basis of all branches of Electrical Engineering. Mastery of electrical circuit analysis skills is essential for later courses in Electrical Engineering and other disciplines in engineering.

1.1 Electrical Components

Circuits components can be divided into two categories: passive elements that consume energy and active elements that generate energy.

Passive elements: resistor, capacitor, inductor, transformer

Eventually, we will discuss the characteristics of each passive elements, except transformer.

Active elements: transistor, motor, generator.

1.2 Electrical Quantities

1. Charge: The smallest unit of charge that exits in nature are

$$\begin{aligned} Electron(-q) &= -1.602 \times 10^{-19} coulomb \\ Proton(+q) &= +1.602 \times 10^{-19} coulomb \end{aligned}$$

   Charge flows through conductors (i.e. wires in physical circuits), resulting in current flowing through a conductor or circuit element

2. Current: moving charges (positive charge & negative charge). It has magnitude and direction. To find the current flowing through a conductor, we select a reference direction. Then consider positive charges moving along the reference direction as a positive contribution to the net charge and negative charges moving in the reference direction is counted as a negative

contribution to the net charge.[1][2]

$$\begin{aligned} i &= \frac{dq}{dt} = \frac{dg^{+}}{dt} + \frac{dg^{-}}{dt} \quad (A = \frac{C}{s})^{3} \\ &= the\ rate\ of\ flow\ of\ (positive)\ charges \end{aligned}$$

Current Convention:

$$\left.\begin{array}{r} \oplus \rightarrow \\ \leftarrow \ominus \end{array}\right\} positive\ current\ (reference\ direction) \rightarrow i$$

When a current is constant with time, we always refer it as **direct currents**, abbreviated as DC. A current varies with time, alternating direction periodically, is called **alternating currents**, abbreviated AC. To find charge given current, integrating this equation yields

$$q(t) = \int_0^t i(\tau)d\tau + q(0)$$

where $q(0)$ is the initial charge at time $t = 0$.

Example 1.1 (Determine current given charge) *[1, Page 10] Suppose* $q(t) = 2 - 2e^{-100t}, t \geq 0$. *Find the current*[4]

$$i(t) = \frac{dq}{dt} = 200e^{-100t}, t \geq 0$$

□

Remark 1: There are many examples, given $i(t)$ to find $q(t)$ or vice versa, such as the one given in the example 1. The skills remain the same as what was shown in the example 1, thus, we will not elaborate on those again to make this class note concise. You may want to see another example in the problem set.

It is well known that charges of same sign repel each other, while charges of opposite sign attract. Since charges exert forces on other charges, energy must be consumed in moving a charge in the vicinity of other charges. Therefore, when charge flows through conductors, energy between circuit elements is transferred. A good example is illustrated by a flashlight where chemical energy stored in the battery is delivered to and absorbed by the bulb where it appears as heat and light.

[1] What is the contribution to net charges for positive charges moving opposite to the reference direction?

[2] What is the contribution to net charges for negative charges moving against the reference direction?

[3] Based on the definition, what does one ampere of current mean?

[4] Plot the $q(t)$ and $i(t)$ to scale versus time. Noting that both $q(t)$ and $i(t)$ are exponentially decay functions, you can check $t = 0$ and $t = infty$ to find the functional values at these time instants.

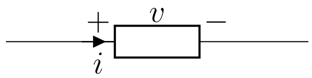


Figure 1.1: An Element: R, L, C

3. Voltage: Potential difference which is converted into kinetic energy ($\frac{1}{2}mv^2$), thus pushing charges forward. The notion is similar to gravitational potential difference when lifting a mass M to a height h requires work (energy) of $MghN-m$ on our part.

$$\begin{aligned} v &= \frac{d\omega}{dq} \quad (V = \frac{J}{C})^5 \\ &= \textit{energy released per unit charge} \end{aligned}$$

Voltage Convention: Voltage has polarity indicating the direction of energy flow. + polarity has higher potential than - polarity.

If positive charge moves from + toward - (i.e. current entering an element from + polarity), the element absorbs energy and does work that appears as heat, mechanical energy, stored chemical energy or as some other form of energy. Such elements have a general name known as **load**. In particular, they are known as **resistors, capacitors, inductors**.

On the other hand, if positive charge moves from - toward + (i.e. current entering an element from - polarity), the element provides energy. Such elements have a general name known as **source**. In particular, they are known as **battery, DC, AC**.

The reference convention we have mentioned for load and source, respectively, is known as **passive reference configuration**. Having learned this notion, the elements in Figure 1.1 can be divided into two categories as shown in Figure 1.2.

A DC voltage means its value is constant with time in both magnitude and polarity, while an AC voltage means its value is changing in magnitude and alternating in polarity with time. Keep the following remarks in mind.

Remarks:

(a) Current is a measure of charge flow through an element, whereas voltage is a measure of energy transferred when charge moves from one end to the other.

(b) Current has direction and voltage has polarity.

(c) In analyzing electrical circuits, we may not know the **actual** direction of current flowing though a conductor, the **actual** polarity of voltage across an element. Therefore, we start the analysis by assigning a current direction and voltage polarity arbitrarily. If we find at the end of calculation that the value of an electrical variable is negative then we know that the true direction/polarity is opposite of the direction/polarity selected

[5] Based on the definition, what does a 12V battery mean?

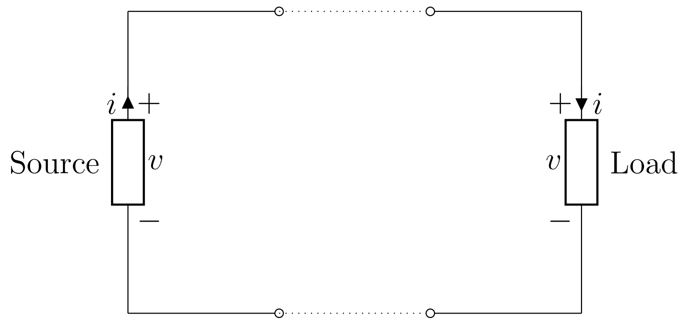


Figure 1.2: Source/Load diagram

initially. For example, referring to Figure 1.1, if the current i found after calculation is -5, then we know there is a 5 amperes current flowing from right to left, opposite to the reference direction initially assigned.

4. Energy & Power: Having understood the definitions of current and voltage, we investigate further the notions of energy and power.

$$
\begin{aligned}
dw &= v \cdot dq = v\frac{dq}{dt} \cdot dt = vidt \\
w &= \int_{t_1}^{t_2} vidt = \int_{t_1}^{t_2} pdt \\
p &= \frac{dw}{dt} = \frac{vdq}{dt} = vi \quad (volts \times amperes = \frac{J}{C} \times \frac{C}{s} = \frac{J}{s} = Watts) \\
&= the\ rate\ of\ energy\ transferred\ /\ transformed \\
P_{av} &= \frac{1}{t_2 - t_1}\int_{t_1}^{t_2} vi\ dt \\
&= The\ average\ power\ over\ a\ period\ of\ time, t_2 - t_1.
\end{aligned}
$$

Similarly, we have energy/power convention described in the passive reference configuration 1.2. We use verbs like **provide, deliver, send, generate** to describe electrical quantities being generated by sources while using verbs like **absorb, consume, receive, draw** for loads. The focal point is to hand draw a diagram 1.2 on a sheet of paper when one reads the verbal phrases.

How to determine whether the energy/power calculated represents energy supplied or absorbed by the element. Based on the diagram 1.2, a positive value of p indicates that energy is absorbed by the element and a negative value shows that energy is supplied by the element. The notion is best illuminated by the following example.

Example 1.2 (Power and energy calculations) *[1, Page 10] Assume that the current direction and voltage polarity are initially assigned in Figure 1.2. If the values of current and voltage after calculation are*

- *For the load on the right:*

1. *If* $i = 2A$, $v = 12$, *then* $p = 12V \times 2A = 24W$, *the load absorbing power.*
2. *If* $i = -2A$, $v = 12$, *then* $p = 12V \times -2A = -24W$, *the load absorbing negative power or equivalently, the load generating power.*

- *For the source on the left:*

1. *If* $i = 2A$, $v = 12$, *then* $p = 12V \times 2A = 24W$, *the source supplying power.*
2. *If* $i = 2e^{-t}A$, $v = -12$, *then* $p = -12V \times 2e^{-t}A = -24e^{-t}W$, *the source supplying negative power or equivalently the source absorbing power. The energy transferred for the interval* $[0\ \infty]$ *is given by*
$$w = \int_0^{\infty} p(t)dt = \int_0^{\infty} -24e^{-t}dt = 24e^{-t}|_0^{\infty} = -24J.$$
The source generates $-24J$ *joules of energy, absorbing* $24J$. *That is, the energy is absorbed by the source.*

□

Remark 2: Like remark 1, the focal point here is to let one be familiar with formulas, learning the trick between integrations and derivatives. Also be aware of the proper interpretation of signs.

Example 1.3 [6] *Given figure 1.2, Let* $i(t) = 2t$ *and* $v(t) = 10t$ *for the source and* $i(t) = 10$ *and* $v(t) = 20 - 2t$ *for the load, respectively, find the power as a function of time and energy transferred between* $t_1 = 0$ *and* $t_2 = 10s$ *for each case.*

□

1.3 Electrical Laws

These laws establish mathematic model among electrical quantities and various circuit elements, expressing voltage across and current flowing in an element.

1.3.1 Ohm's law

The law, in honor of George Ohm, is used to describe relationship of resistor voltage, resistor current and resistance.
$$v = iR$$
where
$$R = \rho\frac{l}{A}, l = length, R = resistance(\Omega), \rho = resistivity$$

[6] This is an exercise.

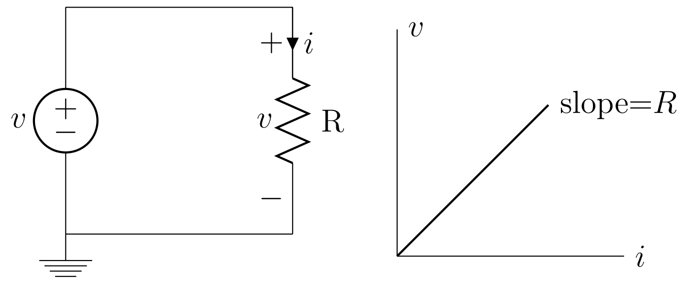


Figure 1.3: Ohm's Law

Note that the resistor above is labeled according to the passive convention. Consequently, a plus sign in the ohm's law is assumed. In situation for which the reference current **enters the negative polarity of the voltage**, Ohm's law becomes

$$v = -iR$$

An example to illustrate the techniques is given in Example 2.1, Chapter 2, to be taught later.

The Ohm's law enables us to find current (knowing v and R), power and energy consumption of a resistor, which is displayed below:

$$i = \frac{v}{R} = Gv$$

where $G = \frac{1}{R}$ is called conductance. Moreover,

$$\begin{aligned} p &= vi = (iR)i = i^2R = \frac{v^2}{R} \\ \omega &= \int_{t_1}^{t_2} pdt = R\int_{t_1}^{t_2} i^2 dt = \frac{1}{R}\int_{t_1}^{t_2} v^2 dt \end{aligned}$$

PSpiceLab 1.1 (Ohm's Law) *Use PSpice to verify Ohm's law using DC sweep analysis.*
Solution:
Objectives: (1) Understand the linear relationship between DC voltage and current. (2) Learn DC sweep technique.
PreLab: DC sweep will activate a solver in PSpice that generates a sequence of v and i electric quantities corresponding to a user-defined range of DC inputs. The generated datum can be plotted on a two dimensional graph. This is a useful analysis for DC circuits.
Lab: Follow the steps to find the answer as expected.
PostLab: Exchange x and y axes will not change the linear relationship, but the meaning of slop is different.

□

1.3.2 Faraday's law

The law, in honor of Michael Faraday, is used to describe the voltage and current relationship of a capacitor

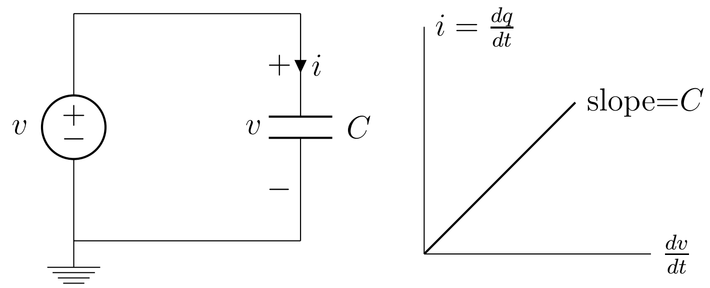


Figure 1.4: Faraday's Law

$$i = \frac{dq}{dt} = C\frac{dv}{dt}$$

where

$$C = \epsilon\frac{A}{d}, C = capacitance(F), \epsilon = permittivity(F/m)$$

The typical values of C range from $pF(10^{-12}F)$ to $0.01F$. Note that the capacitor above is labeled according to the passive convention. Consequently, a plus sign in the Faraday's law is assumed. If the references **were opposite to** the passive configuration, Faraday's law takes the following form

$$i = -C\frac{dv}{dt}$$

Faraday's law enables us to derive the following quantities

$$\begin{aligned} q &= Cv \\ v(t) &= \frac{1}{C}\int_{-\infty}^{t} i(\tau)d\tau = \frac{1}{C}\int_{-\infty}^{t_0} i(\tau)d\tau + \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau = v(t_0) + \frac{1}{C}\int_{t_0}^{t} id\tau \\ p &= vi = v(C\frac{dv}{dt}) \\ \omega &= \int_{-\infty}^{t} p(\tau)d\tau = C\int_{-\infty}^{t} v(\tau)\frac{dv(\tau)}{d\tau}d\tau = \frac{1}{2}Cv^2(t) = \frac{q^2(t)}{2C} \end{aligned}$$

PSpiceLab 1.2 (Faraday's Law) *Use PSpice to verify Faraday's law using time domain transient analysis.*

Solution:

Objectives: (1) Understand rate of change. (2) Represent a PWL time function. (3) Learn time domain transient analysis.

PreLab: (1) Consider the following PieceWise Linear (PWL) time function where each point requires a coordinate.

(2) Time domain transient analysis performs a real-time simulation that generates a time behavior of $v(t)$ and $i(t)$ over a user-defined time frame with an appropriate time step. The generated datum can be plotted with a default time variable on the x-axis. This is a useful analysis for AC circuits.

Lab: Follow the steps to see the results which are consistent with analysis.

PostLab: How to represent a pulse function using PWL? (Hint: two points yields a line.)

□

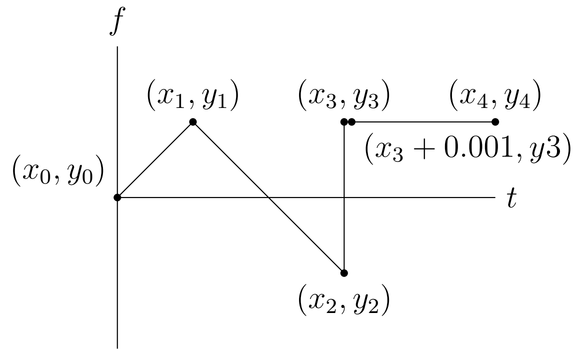


Figure 1.5: Piecewise Linear Function Representation

1.3.3 Henry's law

The law, in honor of Joseph Henry, is used to describe voltage and current quantities of an inductor.

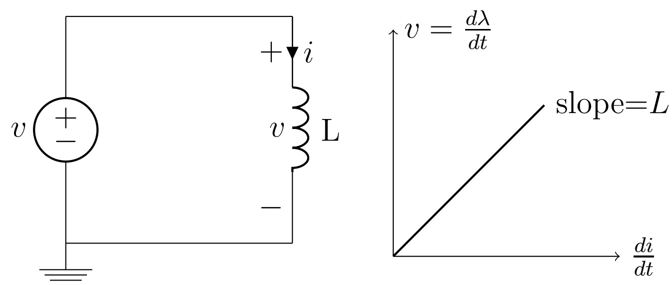


Figure 1.6: Henry's Law

$$v = \frac{d\lambda}{dt} = L\frac{di}{dt}$$

where

$$L = \frac{\mu n^2 A}{l + \frac{9}{10}r}, L = inductance(H), \mu = permeability(H/m)$$

The typical values of L range from μH to $0.1H$. Note that the inductor above is labeled according to the passive convention. Consequently, a plus sign in the Henry's law is assumed. If the references **were opposite to** the passive configuration, Henry's law takes the following form

$$v = -L\frac{di}{dt}$$

Again, Henry's law makes the following derivations possible

$$\begin{aligned} \lambda &= Li \\ i(t) &= \frac{1}{L}\int_{-\infty}^{t} v(\tau)d\tau = \frac{1}{L}\int_{-\infty}^{t_0} v(\tau)d\tau = i(t_0) + \frac{1}{L}\int_{t_0}^{t} v(\tau)d\tau \end{aligned}$$

$$
\begin{aligned}
p(t) &= vi = (L\frac{di}{dt})i \\
\omega(t) &= \int_{-\infty}^{t} p(\tau) f\tau = L\int_{-\infty}^{t} \frac{di}{d\tau} i \, d\tau = \frac{1}{2}Li^2(t) = \frac{\lambda^2(t)}{2L}
\end{aligned}
$$

1.4 Continuity of Stored Energy

An instantaneous change in energy requires an infinite power since $p = dW/dt \to \infty$ when $dt \to 0$. Thus, the stored energy must be a continuous function of time — energy could not change instantaneously. This property indicates that **inductor currents** ($\frac{1}{2}Li^2$) and **capacitor voltages** ($\frac{1}{2}Cv^2$) can not change instantaneously, a powerful technique when one studies transient response of AC circuits.

1.5 Electrical Sources

1.5.1 Ideal independent sources

Independent sources have such property that their output voltage(current) measured at output terminals are independent of loads. That is, whatever the loads are, the voltage or current remain constant at the output terminals. They are customary represented by a circle in circuit diagrams.

1. Ideal voltage source: The characteristic of an independent voltage source is that its voltage

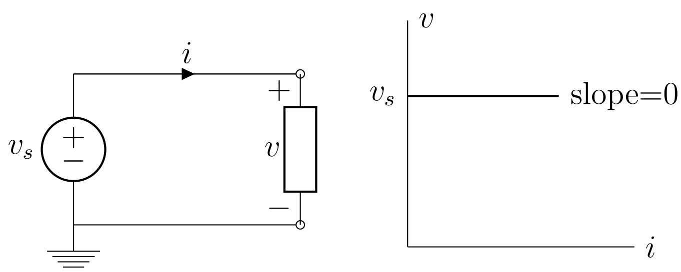


Figure 1.7: Ideal Voltage Source

v is independent of current i, meaning the voltage v is kept constant regardless of the value of the current. Thus $R = \frac{v}{i} = 0$.

However, in real world, when the current is drawn from the terminals, this terminal voltage drops and therefore is not kept constant. This is known as the loading effect. To model such phenomena, we have the following circuit model (known as Thevenin equivalent.) It is readily seen that the $v - i$ property characterizing the input and output relation is

$$v = v_s - iR_s \tag{1.1}$$

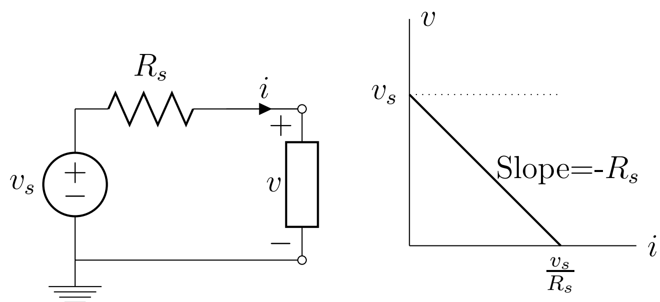


Figure 1.8: Non-Ideal Voltage Source

2. Ideal current source: The characteristic of an independent current source is that its current i

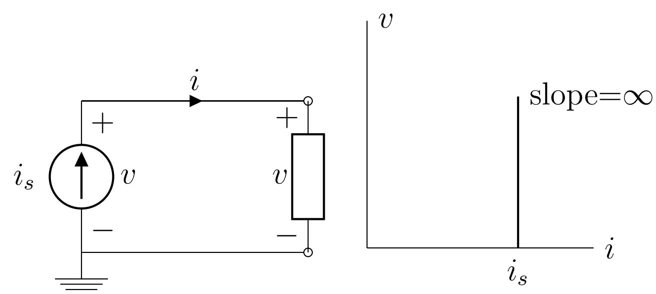


Figure 1.9: Ideal Current Source

is independent of voltage across the source v, meaning the current i is kept constant regardless of the value of the voltage. Thus $R = \frac{v}{i} = \infty$.

Again, in real world, the current is not kept constant and we have the following model (known as Norton equivalent.) It is readily known that the $v - i$ property characterizing the input and output relation is

$$i = i_s - \frac{v}{R_p} \tag{1.2}$$

1.5.2 Ideal dependent sources

These sources are also known as ideal controlled sources because it is controlled by other voltage or current in a circuit. In stead of a circle representing an independent source, the symbol for dependent source is customary a diamond to controlled sources in circuit diagrams. Four examples of dependent sources are shown below:

1. Voltage-Controlled Voltage Source (VCVS): A voltage source that is controlled by voltage v_1 elsewhere in a circuit. Usually, the v_1 is an unknown variable to be determined. In PSpice, VCVS is symbolized by E.

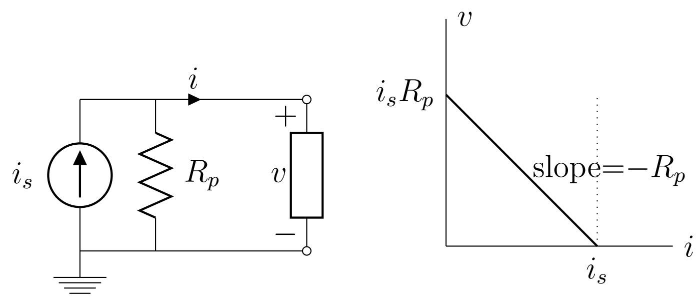


Figure 1.10: Non-Ideal Current Source

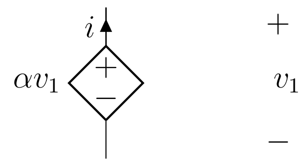


Figure 1.11: Voltage-Controlled Voltage Source/VCVS

2. Voltage-Controlled Current Source (VCCS): A current source that is controlled by voltage v_1 elsewhere in a circuit. Again, the v_1 is an unknown variable to be determined. In PSpice, VCCS is symbolized by G. When wiring, the controlling variable should be wired to the terminals on the left-hand side whilst the energy source terminals are on the right-hand side. An example is drawn to illustrate the idea. A diamond shape with an arrow says that it is

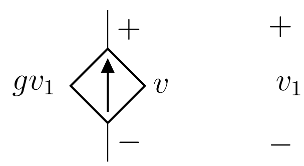


Figure 1.12: Voltage-Controlled Current Source/VCCS

a dependent current source. What does it depend on? the information on the right says $2v_1$, so it depends on a voltage somewhere in the circuit. After searching, v_1 is labeled below the element at upper right corner.

3. Current-Controlled Voltage Source (CCVS): A voltage source that is controlled by current i_1 elsewhere in a circuit. Usually, the i_1 is an unknown variable to be determined. In PSpice, CCVS is symbolized by H. An example to show the dependency is displayed below. Again, the diamond shape with polarity and the information above it means this is a current dependent voltage source. Further investigation shows it depends on current flowing through 5Ω resistor. Notice that an independent source remains a known constant value, say 5 volts, all the time, while an ideal dependent source does remain constant but unknown. You will know the value only after solving the circuit problem.

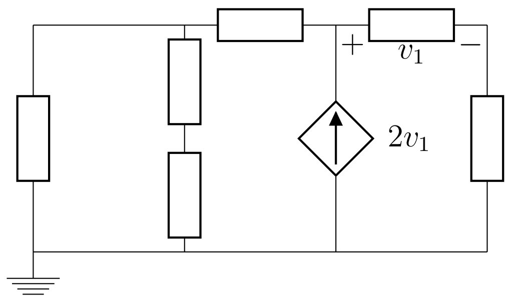


Figure 1.13: Voltage-controlled Current Source/VCCS

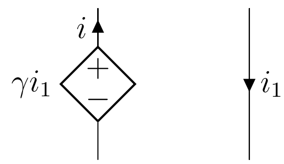


Figure 1.14: Current-Controlled Voltage Sources/CCVS

4. Current-Controlled Current Source (CCCS): A current source that is controlled by current i_1 elsewhere in a circuit. Likewise, the i_1 is an unknown variable to be determined. In PSpice, CCCS is symbolized by F.

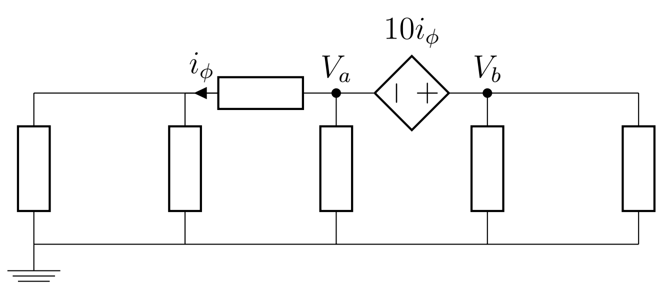


Figure 1.15: Current-Controlled Voltage Source/CCVS

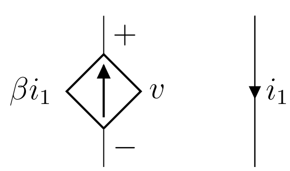


Figure 1.16: Current-Controlled Current Sources/CCCS

1.6 Problems

Problem 1.1 *A heater is rated for 1200W when operated at 110V, find the resistance of the heater and the operating current. (Hint: $p = \frac{v^2}{R}$)*
Answer: $R = 10.08\Omega$, *I=10.9A.*

Problem 1.2 *In the Figure 1.17, find the current i_R and the power of each element in the circuit and state whether each is absorbing or delivering energy.*

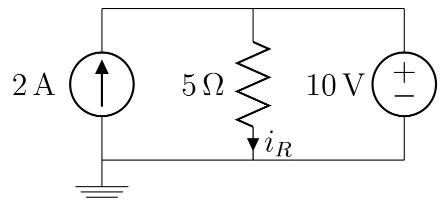


Figure 1.17: Circuit Diagram for Problem 1.2

Answer: *(a) $i_R = 2A$ (b) $P_{2A} = 10 \times 2 = 20W$, delivering; $P_{5\Omega} = 20W$, absorbing; $P_{10V} = 10 \times 0 = 0W$.*

Problem 1.3 *Given the Figure 1.18, solve for i_x.*

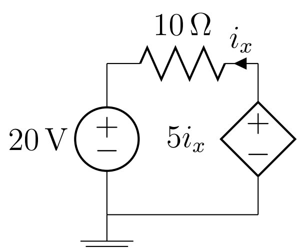


Figure 1.18: Circuit Diagram for Problem 1.3

Answer: $i_x = -4A$.

Problem 1.4 *The current flowing to the right is depicted in the Figure 1.19, find the movement of net charge past a point to the right.*

Remark: [Expand your thinking to draw inferences] Note that the problem could have given you a charge $(q - t)$ plot and ask you to find current $(i - t)$ plot. Likewise, the problem may, say, give you a $v - t$ plot for an inductor whose $v - i$ is governed by $v = L\frac{di}{dt}$ and ask you to find its $i - t$ plot. The same applies to capacitors.

Problem 1.5 *Determine the power delivered to (absorbed by) the elements shown in Figure 1.20*
Answer: *(a) -6 W (b) 50 W (c) 40 W (d) -16 W (e) -42 W (f) 90 W*

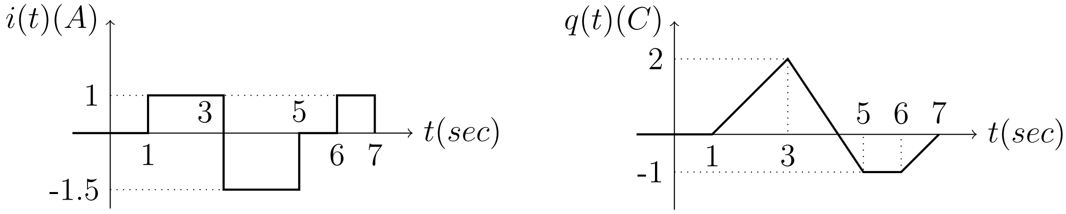


Figure 1.19: Answer to Problem 1.4

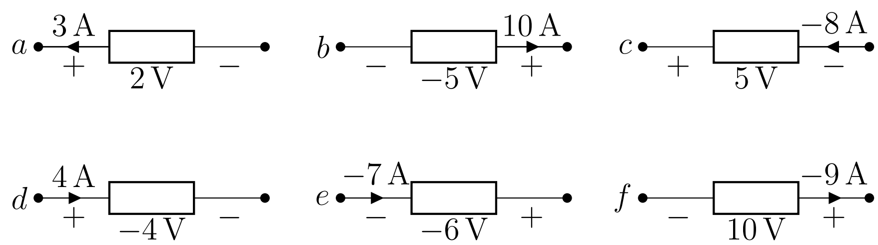


Figure 1.20: Circuit Diagram for Problem 1.5

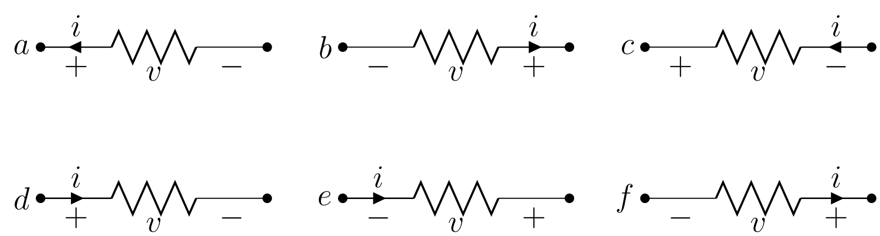


Figure 1.21: Circuit Diagram for Problem 1.6

Problem 1.6 (Draw inference from the example above) *Write the correct Ohms' law for the elements shown in Figure 1.21*
Answer: *(a)* $v = -iR$ *(b)* $v = -iR$ *(c)* $v = -iR$ *(d)* $v = iR$ *(e)* $v = -iR$ *(f)* $v = -iR$

Problem 1.7 *If the two equations(1.1) and (1.2) are identical (ie., v and i are identical), find the relationship between Thevenin and Norton equivalents.(Hint: read the $v - i$ plots and compare)*
Answer: $v_s = i_s R_p$ *and* $R_s = R_p$.

Chapter 2

Circuit Laws

2.1 Circuit Laws (In honor of Gustav Kirchhoff)

Given Figure 2.1, we define the following terms.

1. An electrical circuit is a group of circuit elements connected in a closed path by conductors.

2. A node in an electrical circuit is a point at which two or more circuit elements are jointed together, as shown by the black dots.

3. A loop in an electrical circuit is a closed path that starts from a node, going clockwise/counterclockwise through circuit elements, and back to the starting node.

4. A branch is a conductor that has an element attached to it, as shown by lines $1-2$, $2-3$, and $3-0$, etc.

5. A branch without any element attached is considered as a node because there is no voltage drop.

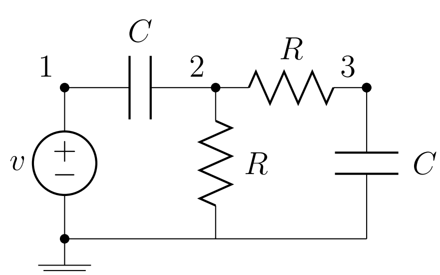


Figure 2.1: Definitions for Nodes and Loops

2.1.1 Kirchhoff's Voltage Law (KVL)

KVL provides relationships among the element voltages in a loop of a circuit. It has two translations.

- The algebraic sum of the voltages around a loop is zero.
  A convenient convention is to use the first polarity mark encountered for each voltage to decide if it should be added or subtracted in the algebraic sum. That is, if polarity marks + are encountered, the voltage carries a plus sign. If polarity marks - are encountered, the voltage carries a minus sign.

- In a specified direction (not necessarily a current direction), the algebraic sum of the voltage rises is equal to the algebraic sum of the voltage drops. Here a voltage rise means in the specified direction the voltage rises from negative polarity to positive polarity. A voltage drop would mean the voltage drops from positive to negative polarity.
  In shorts, $\sum$ voltage rises $= \sum$ voltage drops

Remarks:

1. KVL must be satisfied for all loops of a circuit.

2. KVL also applies to larger, closed loop of a circuit called supermesh where a large closed path is selected and viewed as a super mesh/loop.

3. KVL is essentially a statement of conservation of energy since traveling around a loop the total energy is zero due to $i(v_1 - v_2 + v_3 = 0)$.

2.1.2 Kirchhoff's Current Law (KCL)

KCL provides relationships among the element currents at a node of a circuit. It again has two interpretations.

- The algebraic sum of all currents entering (leaving) a node is zero.
  To compute the net current entering a node, we add the currents entering and subtract the currents leaving. Or equivalently, we add the currents leaving and subtract the current leaving. The focal point is to pick one particular direction (entering or leaving) as positive and the other as negative.

- At a node, the algebraic sum of all currents entering the node is equal to the algebraic sum of all currents leaving the node.
  In shorts, $\sum$ current leaving $= \sum$ currents entering.

Remarks:

1. KCL must be satisfied for all nodes of a circuit.

2. KCL also applies to larger, closed regions of a circuit called supernodes where a group of elements is clustered together and viewed as a super node.

3. KCL is a statement of conservation of charge. That is, nodes can not accumulate or store charge. Charge entering a node must leave that node immediately and go. ($i_1 - i_2 + i_3 = \frac{dq_1}{dt} - \frac{dq_2}{dt} + \frac{dq_3}{dt} = 0$)

Example 2.1 (Circuit analysis using arbitrary references) *[1, Page 35] Referring to Figure 1.2 where $v_s = 10\,V$ and $R = 5\Omega$, now assign any reference except the passive convention.*

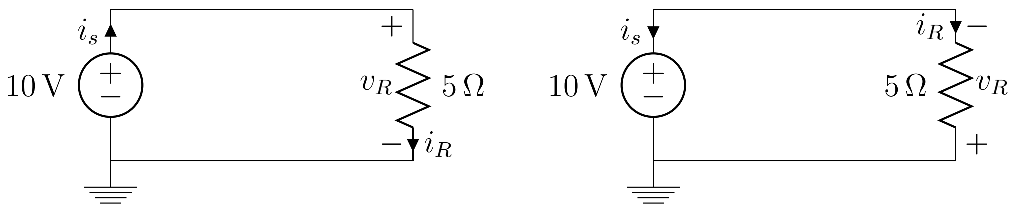


Figure 2.2: Example 2.1

Solution: *Traveling clockwise via KVL, we have*

$$-v_s - v_R = 0$$

yielding $v_R = -v_s = -10$. By Ohm's law, we have $i_R = -v_R/R = 2A$. Also, by KCL at the top node, we have $i_s + i_R = 0$, yielding $i_s = -i_R = -2A$. The power for the voltage source is $p_s = v_s i_s = 10(-2) = -20\,W$, absorbing. And the power for the resistor is $p_R = v_R i_R = (-10)(2) = -20\,W$, delivering.

Alternatively, you may think the source and the resistor labeling does not follow the passive convention. Thus for the source $p_s = -v_s i_s = -10(-2) = 20\,W$, delivering and for the resistor $p_R = -v_R i_R = -(-10)(2) = 20\,W$, absorbing.

This example shows that application of circuit laws will tell us not only the magnitudes of the currents and voltages but the true voltage polarities and current directions as well.

Example 2.2 (One variable, one equation) *: Solve for the $i_3(t)$.*

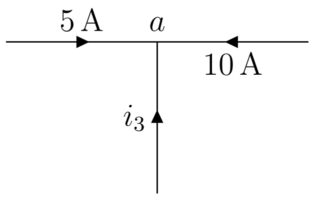


Figure 2.3: Example 2.2

Solution: *Applying KCL at the node, we have $\sum i_a = 0 = 5 + 10 + i_3 = 0$. Thus, $i_3 = -15A$, leaving the node.*

□

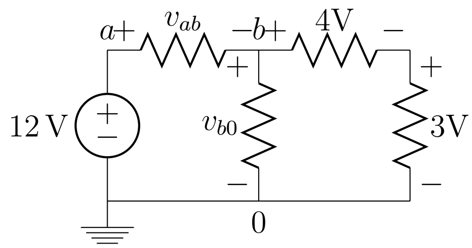


Figure 2.4: Example 2.3

Example 2.3 (Two variables, two equations) *: Solve the following circuit.*
Solution: *Applying KVL around the outer loop yields*

$$-12 + v_{ab} + 4 + 3 = 0 \quad \textit{equivalently, } 12 = v_{ab} + 4 + 3$$

giving $v_{ab} = 5V$. Note that choosing outer loop provides one equation with one variable.

Applying KVL around the loop 0ab0 gives

$$-12 + 5 + v_{b0} = 0, \quad \textit{equivalently, } 12 = 5 + v_{b0}$$

from which we obtain $v_{bo} = 7V$.

The trick here is to find a loop that has only one unknown variable attached to it[1]*. These examples demonstrate that one algebraic equation can only be used to solve for one unknown variable. Two(three, $\cdots$) unknown variables need two(three, $\cdots$) algebraic equations to obtain a solution. The same is true for KCL.*

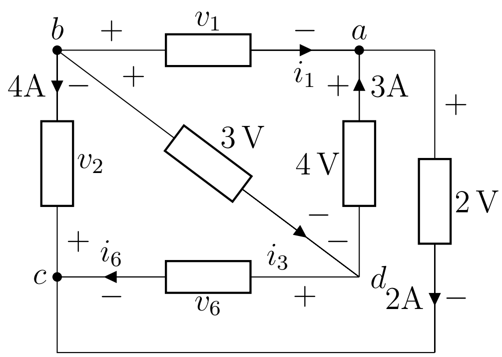
□

Example 2.4 (Another trick problem) *[2, Page 14] Find the unknown currents and voltages and check the conservation of energy.*
Solution: *The key to such problem is to find one variable for one node so that KCL can be applied. To this end, writing KCL at node a yields $i_1 + 3 = 2$, resulting $i_1 = -1A$. Node b generates $i_1 + i_3 + 4 = 0$, resulting $i_3 = -3A$. Lastly, node d provides $i_3 = 3 + i_6$, yielding $i_6 = -6A$. Moreover, we could also use supernode technique to find i_3. Assuming a supernode is located at the top, we have $3 = 2 + 4 + i_3$, yielding $i_3 = -3A$.*

To continue, we find one variable for one loop so that KVL can be used to determine $v_1 = v_2 = -1V$, and $v_6 = -2V$. Actually, you still can use supermesh technique to verify the voltages you just obtained.

Lastly, lets check whether the conservation of energy holds. The result is shown in Table 2.5, where row 3 and 4 are actually generating powers since they consume negative power and that means they generate positive powers.

□



Elements	Power consumed
1	1W
2	4W
3	-9W
4	-12W
5	4W
6	12W
Total	0W

Figure 2.5: Conservation of Energy for Example 2.4

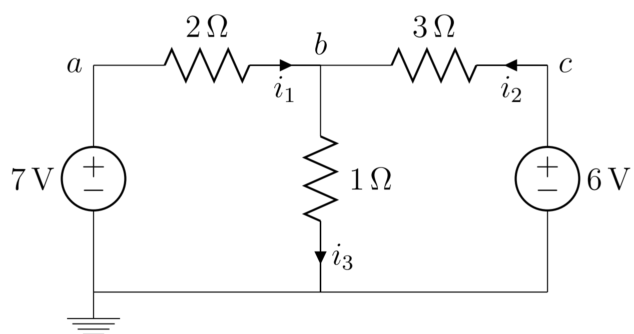


Figure 2.6: Example 2.5-2.8

Example 2.5 *Given the circuit shown in figure 2.6, solve the following circuit for currents i_1, i_2 and i_3.*
Solution: *KCL at node b is*

$$i_1 + i_2 - i_3 = 0^2.(clockwise\ direction)$$

Since there are 3 unknown currents to determine, we need 3 equations to obtain a feasible solution. Two more equations are needed and can be found via KVL:
KVL for loop oabo is

$$-7 + 2i_1 + i_3 = 0$$

and for loop obco:

$$-i_3 - 3i_2 + 6 = 0^3$$

[1]Try the loop 0ab0, what do you get? Can you solve the single equation for two unknowns?
[2]How about nodes a, c, and 0?

Solving these equations simultaneously, we obtain $i_1 = 2A$, $i_2 = 1A$, and $i_3 = 3A$.
A MATLAB script written to solve the above problem ($Ai = V$) is displayed below.

```
A=[1 1 -1; 2 0 1; 0 -3 -1];
V=[0; 7; -6];
i=inv(A)*v
```

□

Example 2.6 (Node voltage method) *Same circuit shown in Figure 2.6, solve the following circuit.*
Solution: *Take node 0 as the reference ground, thus $v_{ao} = 7$, $v_{co} = 6$ and v_{bo} is to be determined. KCL at node b leads to*

$$i_1 + i_2 - i_3 = \frac{7 - v_b}{2} + \frac{6 - v_b}{3} - \frac{v_b}{1} = 0.$$

Solving, we have $v_b = 3V$, $i_1 = 2A$, $i_2 = 1A$, $i_3 = 3A$.

□

Example 2.7 (Loop current method) *Same circuit shown in Figure 2.6, solve the following circuit.*
Solution: *Arbitrarily assuming a clockwise direction for both loops and assigning polarity as shown in the circuit, we write KVL for loop oabo*

$$-7 + 2i_a + 1(i_a - i_b) = 0$$

and KVL for loop obco

$$\begin{aligned} 0 &= -[-(i_b - i_a)] - [-3i_b] + 6 \\ &= (i_b - i_a) + 3i_b + 6. \end{aligned}$$

Solving these equations simultaneously, we have $i_a = 2A$ and $i_b = -1A$.
A MATLAB script, displayed below, is written for this problem.

```
A=[3 -1;-1 4];
v=[7; -6];
i=inv(A)*V
```

However, in determining the voltages, we observe that the voltages of $R = 1$ and $R = 2$ ohms are NOT labeled with the passive sign convention with respect to i_b, so that a minus sign must be inserted into the Ohm's law

$$v_{3\Omega} = -i_b R = -(-1)3 = 3V, \quad v_{1\Omega} = -(i_b - i_a)R = -(-1-2)1 = 3V.$$

What do we learn from this example? The focal point is **if the element voltage and current are not labeled with the passive sign convention, a minus sign must be inserted into the Ohm's law**. *Thus, the safest way is, when given the choice, to label the resistor voltage and current according to the passive sign convention.*

□

[3] How about loop *oabco*?

2.1.3 Voltage divider/division, EE lab verification

When a voltage is applied to a series combination of resistances, a fraction of the voltage appears across each of the resistance. To see this, consider the following series circuit of two resistances with a voltage source applied across the series connection.

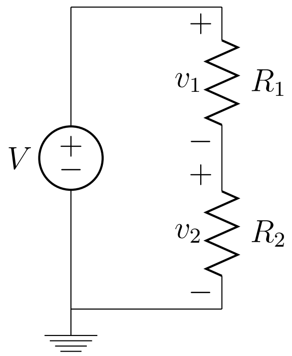


Figure 2.7: Voltage Divider

Applying KVL to the single loop yields current

$$i = \frac{v}{R_1 + R_2}.$$

Ohm's law finds the voltage distribution across each resistance

$$v_2 = v(\frac{R_2}{R_1 + R_2}), \quad v_1 = v(\frac{R_1}{R_1 + R_2}).$$

We therefore conclude that the fraction of the total voltage that appears to $R_2(R_1)$ in a series circuit is the ratio of $R_2(R_1)$ to the total resistance. Notice that the largest voltage appears across the largest resistance in series.

Example 2.8 (Voltage divider) *: Solve the following circuit*

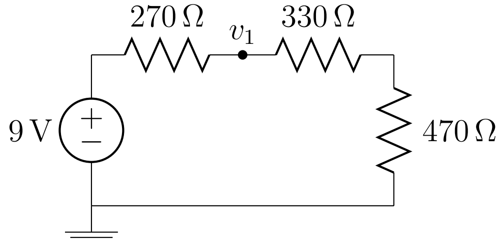


Figure 2.8: Example 2.8

Solution: *Voltage divider formula yields*

$$v_1 = 9 \cdot \frac{330 + 470}{270 + 330 + 470} = 9 \cdot \frac{800}{1070} = 6.729V.$$

Thus,

$$v_{270\Omega} = 9 - 6.729 = 2.271V.$$

□

Example 2.9 (Voltage divider) *Solve the following circuit.*

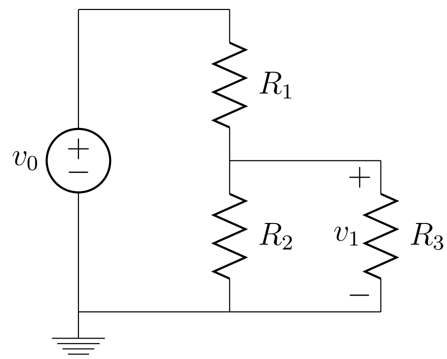


Figure 2.9: Example 2.9

Solution: *Find the equivalent resistance for the parallel resistance and apply voltage divider formula to find v_1 displayed below*

$$v_1 = v_0 \cdot \frac{(\frac{R_2R_3}{R_2+R_3})}{R_1 + (\frac{R_2R_3}{R_2+R_3})} = \frac{v_0 \cdot R_2R_3}{R_1R_2 + R_1R_3 + R_2R_3}.$$

□

Although we have derived the voltage division for two resistances in series, it applies for any number of resistances as long as they are connected in series. Therefore, a general form for a total of r resistances in series is

$$v_{R_i} = v\left(\frac{R_i}{\sum_{i=1}^{r} R_i}\right).$$

Example 2.10 (Voltage division) *[2, Page 59] Determine the voltage v_1 and v_2.*
Solution: *Arbitrarily assigning a loop current in the clockwise direction and forming KVL yield*

$$-(-6i) + 10 + i - 4 + 2i + 3 + 4i - 5 = 0, \quad equiv. \;\; i = \frac{-4}{13} = -0.308A$$

Thus, $v_1 = 2i = -0.615A$ and $v_2 = -6i = 1.846V$ due to passive sign convention.

Another approach(voltage division):

$$v_1 = -4\left(\frac{2}{6+1+2+4}\right) = -0.615, \quad v_2 = 4\left(\frac{6}{6+1+2+4}\right) = 1.846.$$

□

Example 2.11 (Pspice Program for EE lab – voltage divider) *Re-do your lab examples for voltage divider by checking the theoretical/true values using Pspice program.*

□

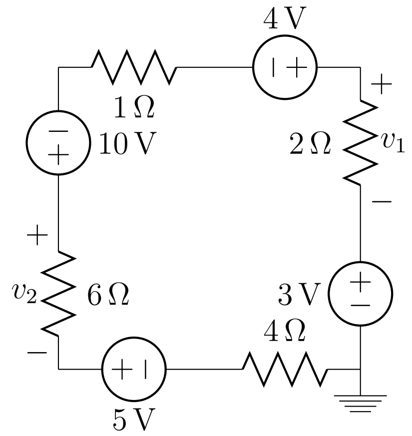


Figure 2.10: Example 2.10

2.1.4 Current divider/division, EE lab verification

When a current is flowing to a parallel combination of resistances, it divides and a fraction of the total current flows through each resistance. The next rule, current division, is similar to the voltage division rule. To see this, consider the parallel combination of two resistances across which a current is applied as shown below.

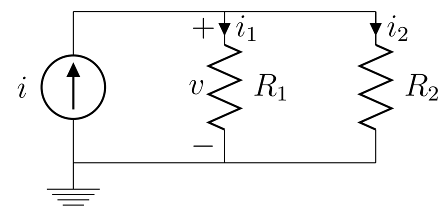


Figure 2.11: Current Divider

First label the voltage v at the top node. Then the corresponding KCL translates to

$$i = i_1 + i_2 = \frac{v}{R_1} + \frac{v}{R_2} = v\left(\frac{R_2 + R_1}{R_1 R_2}\right) = v\left(G_1 + G_2\right).$$

Rearranging, we have the voltage across the resistances, which are of the same magnitude and polarity

$$v = \frac{R_1 R_2}{R_1 + R_2} i = \frac{i}{G_1 + G_2}.$$

Ohm's law finds the current distribution in each resistance

$$i_1 = i\left(\frac{R_2}{R_1 + R_2}\right) = i\left(\frac{1/G_2}{1/G_1 + 1/G_2}\right) = i\left(\frac{G_1}{G_1 + G_2}\right)$$

and

$$i_2 = i\left(\frac{R_1}{R_1 + R_2}\right) = i\left(\frac{1/G_1}{1/G_1 + 1/G_2}\right) = i\left(\frac{G_2}{G_1 + G_2}\right).$$

For two resistances in parallel, the fraction of the total current flowing through one resistance is the ratio of the *opposite* resistance to the sum of two resistances. Notice that this formula only applies to two resistances in parallel structure. If there are more than two resistances connected in parallel, we should combine them into two equivalent resistances in parallel so that we have only two resistances before applying the formula.

However, if conductance expression is used, rather than resistance expression, to derive the rule, for a total of r conductances in parallel we have the following general form

$$i_{R_i} = i\left(\frac{G_i}{\sum_{i=1}^{r} G_i}\right)$$

Notice that the formula is expressed in conductance, not resistance.

Example 2.12 (Current division) *[2, Page 82] Determine the voltage v_x in the circuit.*

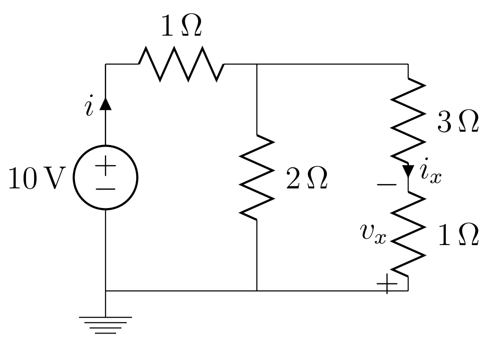


Figure 2.12: Example 2.12

Solution: *First label the currents i and i_x for the purpose of using current division. The current i may be determined by*

$$i = \frac{10}{1 + (2//4)} = \frac{30}{7}A$$

Next moving back to the original circuit, we apply current division formula and obtain

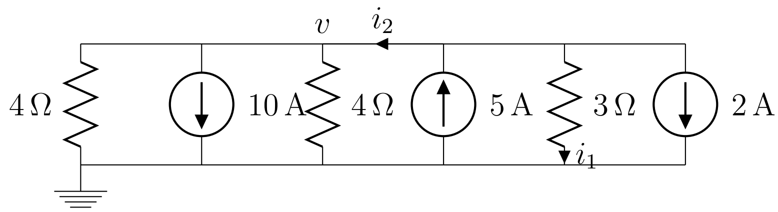
$$i_x = \frac{30}{7}\left(\frac{2}{2+4}\right) = \frac{10}{7}A$$

From this we obtain

$$v_x = -i_x 1 = -\frac{10}{7}V$$

Again observe the minus sign in this last result, required by the passive sign convention.

□



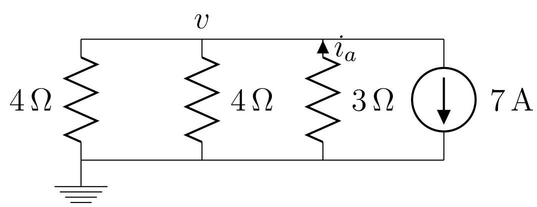


Figure 2.13: Example 2.13

Example 2.13 (Current division) *[2, Page 65] Determine the currents i_1, i_2 in the circuit.*
Solution: *First label voltage at the top with positive polarity assigned, write KCL for this node (assuming entering currents are positive)*

$$5-(\frac{v}{3})-2-10-\frac{v}{4}-\frac{v}{4}=0, \quad or \quad -7=\frac{v}{3}+\frac{v}{4}+\frac{v}{4}$$

From which we obtain $v=-8.4V$, and

$$i_2=\frac{v}{4}+\frac{v}{4}+10=5.8A, \quad i_1=(-8.4/3)=-2.8.A$$

Observe the minus sign in the last result, required by the passive sign convention.

Another approach:

$$i_a=7\left(\frac{\frac{1}{3}}{\frac{1}{4}+\frac{1}{4}+\frac{1}{3}}\right)=2.8A$$

Notice that i_a is the current direction flowing out of $7A$ current source and entering the negative polarity of 3Ω resistor while the i_1 is opposite to it. Therefore, $i_1=-i_a=-2.8A$ and $v=3i_1=-3i_a=-8.4V$.

□

Example 2.14 (Pspice Program for EE Lab – current divider) *Re-do your lab examples by checking the theoretical/true values using Pspice program.*

□

The methods we have studied are useful, but they alone can not solve all circuit problems. We need more tools and that is discussed in the next chapter.

2.2 Problems

Problem 2.1 *In the figure for problem 2.14, (a) find the value i_3, (b) the value of i_6, (c) the value of v_s. and (d) the power dissipated in each resistor, (e) the power delivered by 12A source.*

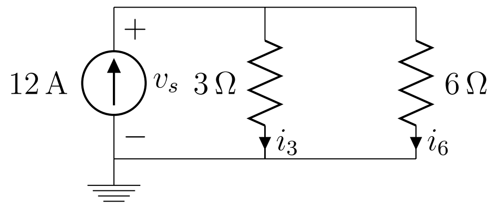


Figure 2.14: Circuit Diagram for Problem 2.1

Answer: *(a)* $i_3 = 8A$ *(b)* $i_6 = 4A$ *(c)* $v_s = 24V$ *(d)* $192W$ *and* $96W$*, (e)* $288W$

Problem 2.2 *Given the figure for problem 2.15, solve for i_s. (Hint: i_x enters 15Ω resistor from negative polarity.)*

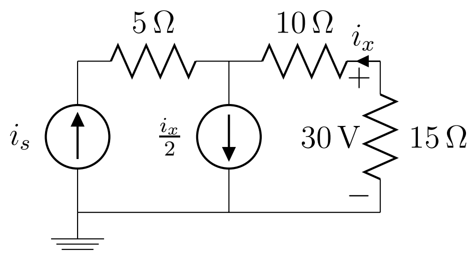


Figure 2.15: Circuit Diagram for Problem 2.2

Answer: $i_s = 1A$.

Problem 2.3 *Device X requires 4V at 1.5mA and device Y operates at 2V at 1mA. The two devices are to be operated from a 9V as shown in Figure for problem 2.16. Specify the values of R_1 and R_2.*

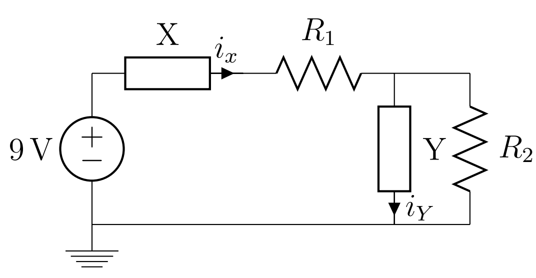


Figure 2.16: Circuit Diagram for Problem 2.3

Answer: $R_1 = 2K\Omega$, $R_2 = 4K\Omega$.

Problem 2.4 *In the circuit for problem 2.17, determine the unknown voltages and currents and verify conservation of power. After computation, check the bigger closed loop (supermesh) to verify the KVL.*

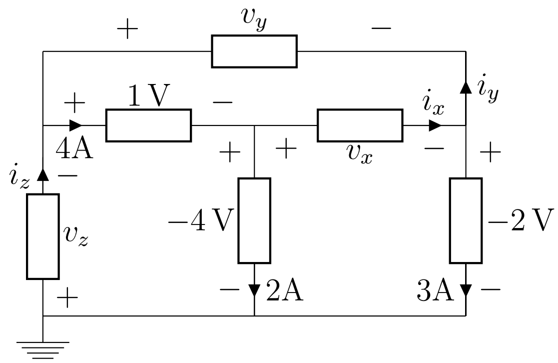


Figure 2.17: Circuit Diagram for Problem 2.4

Answer: *$i_x = 2A, i_y = -1A$, and $i_z = 5A$. $v_x = -2V, v_y = -1V$, and $v_z = 3V$. For elements located from top to down and left to right, we have -1W, 4W, -4W, 15W, -8W, -6W and the total is zero.*

Problem 2.5 *Find v and the power of each element in the circuit of Figure 2.18 and state whether each is absorbing or delivering energy.*

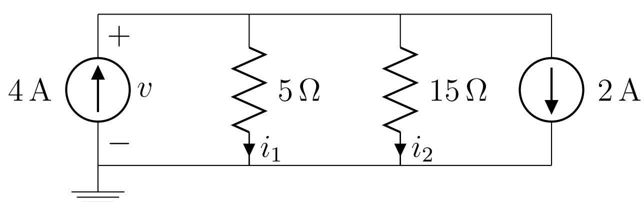


Figure 2.18: Circuit Diagram for Problem 2.5

Answer: *$v = 7.5V$, $p_{4A} = 30W$ delivering, $p_{5\Omega} = 11.25W$ absorbing, $p_{15\Omega} = 3.75W$ absorbing, $p_{2A} = 15W$ absorbing.*

Problem 2.6 *Find the values of v, v_1, v_2 and i in Figure 2.19.*

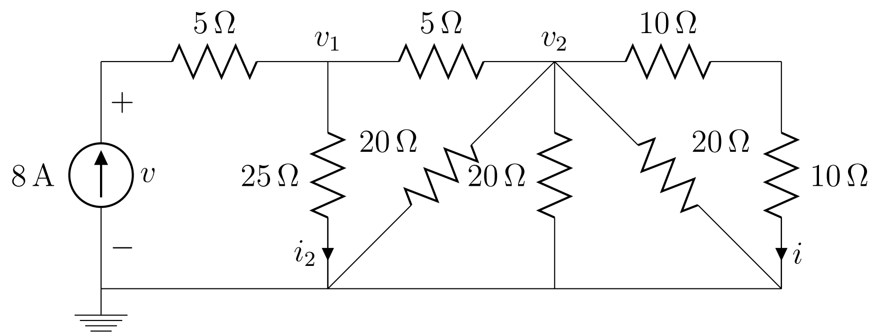


Figure 2.19: Circuit Diagram for Problem 2.6

Answer: $i = 1A$, $v_2 = 20V$, $v_1 = 100V$, $v = 140V$.

Problem 2.7 *Assume i_{ab}=0 and v_{ab}=0, find R_x given R_1, R_2 and R_3 in Figure 2.20*

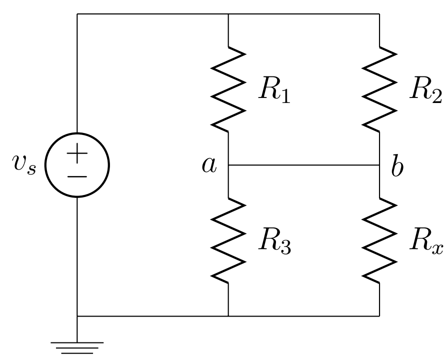


Figure 2.20: Circuit Diagram for Problem 2.7

Answer: $R_x = \frac{R_2}{R_1} \times R_3$.

Problem 2.8 *Find the current, voltage and power for each element in the circuit shown in Figure 2.21 and state whether each is absorbing or delivering energy.*

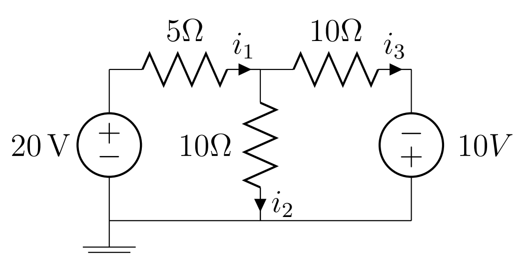


Figure 2.21: Circuit Diagram for Problem 2.8

Answer: $v = 7.5V$, $i_1 = 2.5A$, $i_2 = 7.5A$, $i_3 = 1.75A$, *Resistors: absorbing* $30.25W$, $6.625W$, $30.625W$ *and sources: delivering* $50W$, $17.5W$.

Chapter 3

DC Circuits

After learning the two fundamental laws – KVL and KCL – governing the electrical quantities, v and i, in a circuit, we now focus ourselves on the circuit theorems that can speed up calculations, allowing us to replace an original circuit with an equivalent circuit.

3.1 Network Theorems / Circuit Theorems

The concept of network theorems are a very important and powerful circuit analysis tool that we will frequently employ on many occasions, thereby, speeding up determination of voltages and currents when analyzing a circuit.

3.1.1 Equivalence

Two electrical circuits are equivalent if they have the same $v-i$ characteristics at the external terminals, $\forall R$. So equivalence simply says that load attached to external terminals (or terminals of interest) can not tell differences which circuit the load is attached to.

It should be clear to the readers that **equivalence does not mean the internal structure of the underlying two circuits must look the same**. Generally, they will not.

Example 3.1 (Equivalence) *[2, Page 33] Find the current i so that circuit A and B are equivalent.*
Solution: *For circuit A, we obtain KVL*

$$v_A = 3i_A + 5$$

From circuit B, we have

$$i_B = \frac{v_B}{3} + i, \quad (or \quad v_B = 3i_B - 3i).$$

To have equivalence, we must require $i_A = i_B$ and $v_A = v_B$, yielding $i = -\frac{5}{3}A$.

□

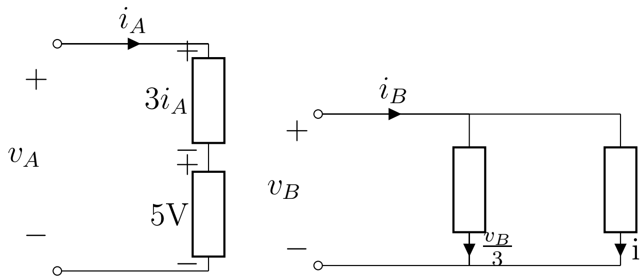


Figure 3.1: Example 3.1. Notion of Equivalence

3.1.2 Source transformations

Independent voltage source and independent current source can be converted into each other mutually. That is, one can always convert a voltage source in series with a resistor into the corresponding current source in parallel with the same resistor. To illustrate, consider the following circuit diagram and if the two circuits are identical in terms of their external behaviors, having the same current and voltage measured at the terminals a and b, the load can not tell what type of sources is attached. The notion is demonstrated below.

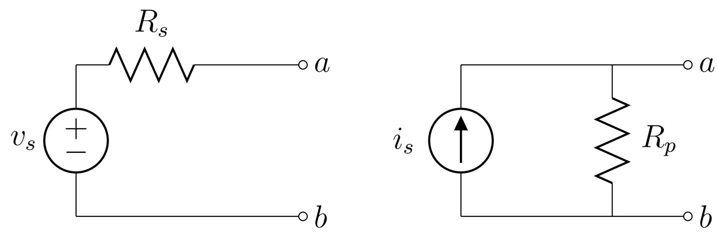


Figure 3.2: Source Transformation

Notice that the voltage polarity + is labeled at the top where the arrow of current direction is. By definition of equivalence, the two circuits have the same $v - i$ characteristics for **all** resistances. Although we can try two resistors of any values, these two resistors – $R = \infty$ and $R = 0$ – are used since they have physical meanings. To start, we use open circuit technique to the circuits shown above and find

$$\text{Open circuit } (R = \infty) : v_{ab} = v_s \text{ and } v_{ab} = i_s R_p, \text{ respectively}$$

Similarly, short circuit analysis yields

$$\text{Short circuit } (R = 0) : i_{ab} = v_s / R_s \text{ and } i_{ab} = i_s, \text{ respectively}$$

By definition of equivalence, we have

$$i_s = \frac{v_s}{R_s}, \quad R_p = R_s. \tag{3.1}$$

The identity (3.1) says that given v_s and R_s (a voltage source in series with a resistor) can be converted into current source i_s in parallel with a resistor R_p and vice versa.

3.1.3 Network reduction

Network reduction can enable us to simplify a complex circuit into a simple circuit by converting resistors into one equivalent resistor, depending on their series or parallel structures. We start our analysis for resistor networks displayed in Figure 3.3 showing a series network and Figure 3.4 for a parallel network.

Resistors in series

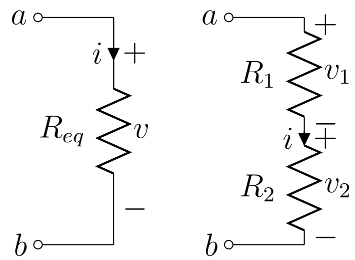


Figure 3.3: Series Equivalent

Since resistors in series have the same current flowing in the resistors, we have, applying KVL,

$$v = iR_{eq}$$

for the circuit on the left and

$$v = v_1 + v_2 = iR_1 + iR_2 = i(R_1 + R_2)$$

for the circuit on the right in Figure 3.3. By equivalence, we must have

$$R_{eq} = R_1 + R_2.$$

In general, we have

$$R_{eq} = R_1 + R_2 + \cdots + R_n = \sum_i^n R_i.$$

Resistors in parallel

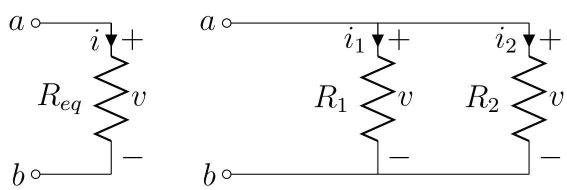


Figure 3.4: Parallel Equivalent

Parallel circuits have same voltage across the parallel combinations. The circuit on the right yields

$$i = i_1 + i_2 = \frac{v}{R_1} + \frac{v}{R_2} = v(\frac{1}{R_1} + \frac{1}{R_2})$$

and the circuit on the left gives

$$i = v\frac{1}{R_{eq}}.$$

Therefore, by equivalence, we have

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} \; or \; G_{eq} = G_1 + G_2.$$

In general, we have

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \cdots + \frac{1}{R_n} = \sum_i^n \frac{1}{R_i} = \sum_i^n G_i$$

Inductors in series

Now replacing the resistors R_1, R_2, and R_{eq} in Figure 3.3 with L_1, L_2, and L_{eq} and using the same derivation techniques shown for resistors, we immediately have

$$v = v_1 + v_2 = L_1\frac{di}{dt} + L_2\frac{di}{dt} = (L_1 + L_2)\frac{di}{dt}$$

and

$$v = L_{eq}\frac{di}{dt}$$

Therefore, the equivalence condition yields

$$L_{eq} = L_1 + L_2.$$

In general, we have

$$L_{eq} = L_1 + L_2 + \cdots + L_n = \sum_i^n L_i.$$

Inductors in parallel

Now replacing the resistors R_1, R_2 and R_{eq} in Figure 3.4 with L_1, L_2, and L_{eq}, we have

$$i = i_1 + i_2 = \frac{1}{L_1}\int_0^t v d\tau + \frac{1}{L_2}\int_0^t v \; d\tau = (\frac{1}{L_1} + \frac{1}{L_2})\int_o^t v \; d\tau$$

and

$$v = \frac{1}{L_{eq}}\int_o^t v \; d\tau$$

Therefore, we have

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2}.$$

In general, we have

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \cdots + \frac{1}{L_n} = \sum_i^n \frac{1}{L_i}.$$

Capacitors in series

Now replacing the resistors R_1, R_2, and R_{eq} in Figure 3.3 with C_1, C_2, and C_{eq}, we have

$$v = v_1 + v_2 = \frac{1}{C_1}\int_0^t i\ d\tau + \frac{1}{C_2}\int_0^t i\ d\tau = (\frac{1}{C_1} + \frac{1}{C_2})\int_0^t i\ d\tau.$$

and

$$v = \frac{1}{C_{eq}}\int_o^t i\ d\tau$$

Therefore the following holds

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}.$$

In general, we have

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \cdots + \frac{1}{C_n} = \sum_{i=1}^{n}\frac{1}{C_i}.$$

Capacitors in parallel

Now replacing the resistors R_1, R_2, and R_2 in Figure 3.4 with C_1, C_2, and C_{eq}, we have

$$i = i_1 + i_2 = C_1\frac{dv}{dt} + C_2\frac{dv}{dt} = (C_1 + C_2)\frac{dv}{dt}$$

and

$$i = C_{eq}\frac{dv}{dt}$$

Therefore

$$C_{eq} = C_1 + C_2.$$

In general, we have

$$C_{eq} = C_1 + C_2 + \cdots + C_n = \sum_{i=1}^{n} C_i.$$

Example 3.2 (Network reduction) *Use circuit reduction technique and solve the following circuit to find the power delivered by the* $6V$ *voltage source.*

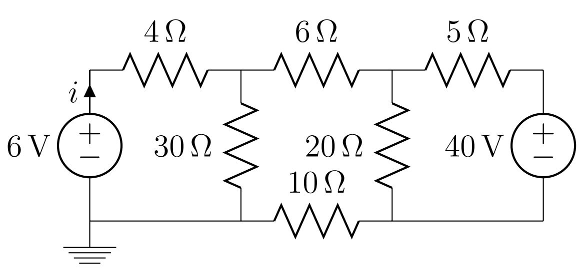
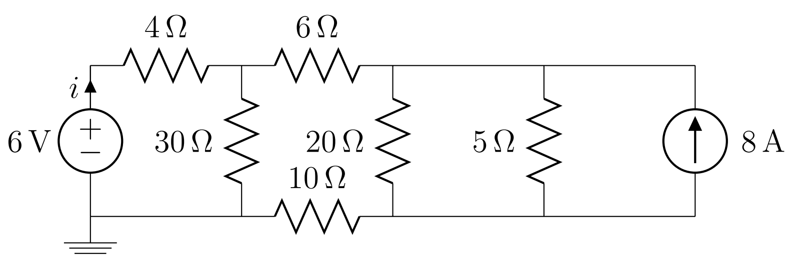


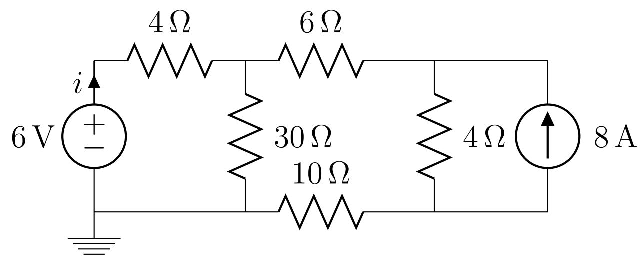
Figure 3.5: Example 3.2

Solution:

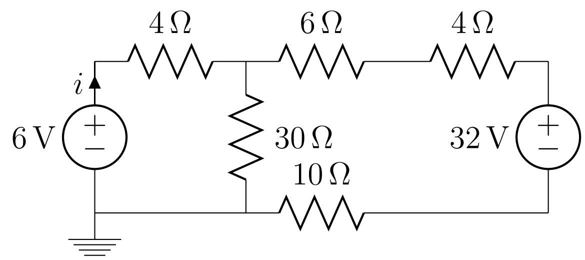
Step 1: Convert $40V$ *voltage source in series with a resistor into* $8A$ *current source in parallel with the same resistor.*


4 Ω
6 Ω
i
6 V
30 Ω
20 Ω
10 Ω
5 Ω
8 A

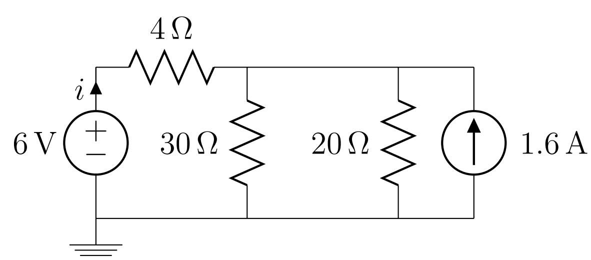
Step 2: Parallel reduction $20//5 = 4\Omega$



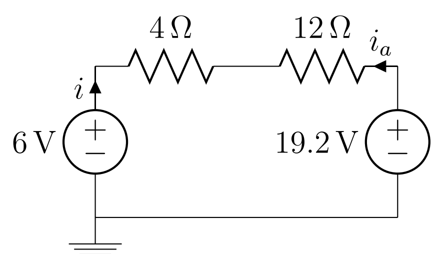
Step 3: Convert $8A$ *current source in parallel with* 4Ω *into* $8V$ *voltage source in series with the same resistor.*



Step 4: Apply source conversion on the $32V$ *voltage in series with* 4Ω *resistor.*



Step 5: repeat the process mentioned above again to generate a single loop circuit. For the single



loop circuit, simple calculation obtains $i_a = \frac{19.2-6}{16} = 0.825A$. $P_{6V} = vi = 6(-0.825) = -4.95W$, *generating. This is equivalent to say* $4.95W$, *consuming.*

□

3.1.4 Thevenin equivalent circuit. EE lab verification

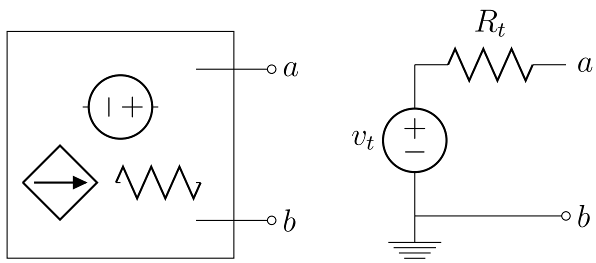


Figure 3.6: Thevenin equivalent

Thevenin theorem, in honor of M.L. Thevenin, is given below as the circuits shown in Figure 3.6. We inspect the open circuit first, realizing that no current can flow through an open circuit. Thus the Thevenin source voltage v_t is equal to the open circuit voltage of the original network, an equivalent constraint

$$v_{ab} = v_t = v_{oc}.$$

Secondly, we analyze the short circuit, realizing that the current of the Thevenin equivalent can be obtained by Ohms's law v_t/R_t. Thus the Thevenin short circuit current v_t/R_t is equal to the short circuit current of the original network, an equivalent constraint.

$$i_{ab} = \frac{v_t}{R_t} = i_{sc}.$$

In addition, observing the Thevenin circuit in Figure 3.6, we find that zeroing/deactivating the Thevenin voltage source, replacing it by a short circuit, the resistance seen at the terminals is the Thevenin resistance. This also implies that if deactivating all independent voltage sources, we can find the equivalent resistance immediately.

PSpiceLab 3.1 *Use PSpice to find Thevenin equivalent circuit using (1) open and short circuit techniques and (2) a switching element.*
Solution: *To find v_{oc} simply attach a resistance, say 5 Mega, to the terminals of concern. To find I_{sc}, just close the terminal with a line representing short-circuit. Once these voltage and current are found, resistor is determined by $R = \frac{v_{oc}}{I_{sc}}$. A fairly quick method is to attach a switch that will open at some time, say $t_0 > 0$, after simulation taken place. Then plot the v vs. i of the same terminals.*

3.1.5 Norton equivalent circuit, EE Lab verification

Norton theorem, in honor of Edward Norton, is given below as the Norton equivalent shown in Figure 3.7. We follow the derivation shown for Thevenin equivalent, yielding

$$\begin{aligned} \text{Short circuit } (R=0) &\ : \ i_{ab} = i_n = i_{sc} \\ \text{Open circuit } (R=\infty) &\ : \ v_{ab} = i_n R_n = i_s R_n = v_{oc}. \end{aligned}$$

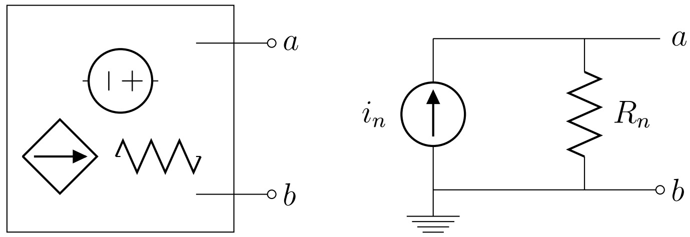


Figure 3.7: Norton equivalent

If we zero/deactivate the Norton current source in Figure 3.7, replacing it by an open circuit, the Norton equivalent becomes a resistance of R_p. Just as deactivation of voltage sources holds for finding equivalent resistance, we can find the equivalent resistance immediately by deactivating current sources. In sum, we conclude that

- If a network has NO dependent sources, we can find the Thevenin/Norton resistance by zeroing the independent sources, a zero voltage being shorted and a zero current source being opened.
- It should be noted that the network must be resistive.
- What shall we do if the network contains dependent sources? We will answer this concern after some examples.

Example 3.3 (Thevenin Theorem) *Find the Thevenin equivalent circuit seen by terminal ab.*

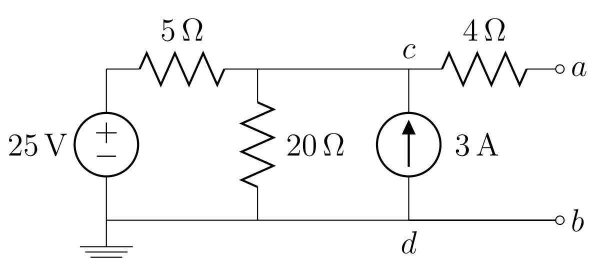


Figure 3.8: Example 3.3

Solution: *We will demonstrate this example by analyzing open circuit ($R = \infty$) and short circuit ($R = 0$) analysis.*
v_{ab}=*open circuit voltage*

$$\frac{v_{ab} - 25}{5} + \frac{v_{ab}}{20} - 3 = 0 \rightarrow v_{ab} = 32V$$

i_{ab}=*short circuit current*

$$\frac{v_{cd} - 25}{5} + \frac{v_{cd}}{20} - 3 + \frac{v_{cd}}{4} = 0 \rightarrow v_{cd} = 16V$$

From which, we obtain

$$i_{ab} = \frac{v_{cd}}{4} = \frac{16}{4} = 4A \quad R_t = \frac{v_{ab}}{i_{ab}} = \frac{32}{4} = 8\Omega.$$

There is another way of determining the Thevenin resistance by zeroing the voltage sources and current sources respectively. Then find the equivalent resistance from the terminals of concern. For this example, we see the equivalent resistance seen from terminal ab is $4+5//20 = 8\Omega$. *An equivalent Thevenin circuit is given below.*

Method 2: *Another approach is to use different resistances, for example,* $R = 6\Omega$ *and* $R = 16\Omega$. *Actually, we can select any two resistances when analyzing the problem*[1].

Assume that $R = 6\Omega$ *is connected to the ab terminals. To find* i_{ab}*, we need to find* v_{cd} *first. Thus we label the node-voltage* v_{cd} *at the top, picking the ground node at the bottom. KCL yields*

$$\frac{v_{cd} - 25}{5} + \frac{v_{cd}}{20} - 3 + \frac{v_{cd}}{10} = 0 \rightarrow v_{cd} = \frac{160}{7}V$$

from which we find

$$i_{ab} = \frac{16}{7}A.$$

Repeat step one just shown one more time for the case where $R = 16\Omega$ *is attached at terminals ab*

$$\frac{v_{cd} - 25}{5} + \frac{v_{cd}}{20} - 3 + \frac{v_{cd}}{20} = 0 \rightarrow v_{cd} = \frac{80}{3}V$$

from which we find

$$i_{ab} = \frac{4}{3}A.$$

To find the equivalent circuit, we need to find the corresponding i_{ab} *for the Thevenin circuit which satisfies the following constraint when* $R = 6\Omega$ *and* $R = 16\Omega$ *are attached, respectively.*

$$\begin{aligned} i_{ab} &= \frac{v_t}{R_t + 6} = \frac{16}{7} \quad or \quad 7v_t - 16R_t = 96 \\ i_{ab} &= \frac{v_t}{R_t + 16} = \frac{4}{3} \quad or \quad 4v_t - 8R_t = 64 \end{aligned}$$

Solving, we obtain the same Thevenin circuit as method 1 did.
This example shows that to find Thevenin/Norton equivalents, we need two different resistors to form two simultaneous equations to solve for $v_s(i_n)$ *and* R_s. *Yet,* $R = 0$ *and* $R = \infty$ *are recommended for their simplicity.*

□

Example 3.4 (Thevenin Theorem) *Given the same circuit in the last example 3.9, find the Thevenin equivalent circuit seen by the* 20Ω *resistance, (assuming that a* 6Ω *is attached at terminal*

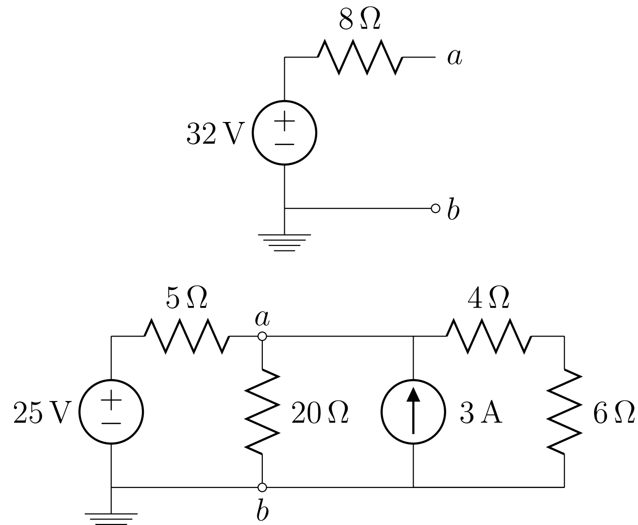


Figure 3.9: Example 3.4

ab.)

Solution: *We will demonstrate this example by analyzing open circuit ($R = \infty$) and short circuit ($R = 0$) analysis.*

v_{ab}=*open circuit voltage*

$$\frac{v_{ab} - 25}{5} + \frac{v_{ab}}{10} - 3 = 0 \to v_{ab} = \frac{80}{3}$$

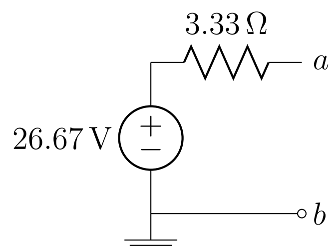
i_{ab}=*short circuit current*

$$i_{ab} = \frac{25}{5} + 3 = 8A.$$

From which, we obtain[2]

$$R_t = \frac{v_{ab}}{i_{ab}} = \frac{10}{3}\Omega.$$

To find the equivalent resistance via zeroing independent sources, we find $5//10 = \frac{10}{3}\Omega$.



Another approach is to use different resistances, for example, $R = 6\Omega$ *and* $R = 16\Omega$[3]

[1]Why is that two resistances are sufficient to solve the problem?
[2]Draw the corresponding Thevenin circuit and verify it via PSpice.
[3]This is a homework problem.

□

Example 3.5 (Thevenin Equivalent with Dependent Source) *Solve the following circuit.*

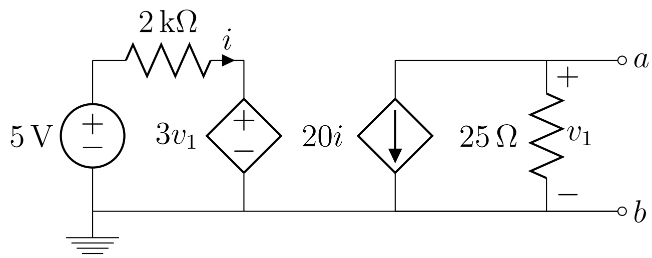


Figure 3.10: Example 3.5

Solution: *Open circuit analysis yields*

$$v_{ab} = v_1 = -20i \times 25 = -500i$$

where

$$i = \frac{5 - 3v_1}{2K}.$$

Thus, we have

$$v_1 = -5V.$$

Short circuit analysis finds

$$i_{sc} = -20i = -20\frac{5}{2K}$$

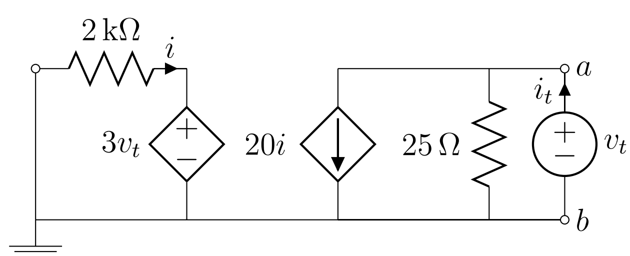
This is because ab is shorted, and thus $v_1 = 0$. This means that the dependent source $3v_1 = 0$. Thus,

$$i_{sc} = -50mA$$

Ohm's law gives

$$R_{TH} = \frac{-5}{-50} \times 10^3 = 100\Omega.$$

Another method to find equivalent resistance: Zeroing the independent voltage source is equivalent



to replace independent voltage source by a short circuit. Thus we have

$$i_T = \frac{v_T}{25} + 20i$$

Furthermore,

$$i = \frac{0 - 3v_T}{2K} = -\frac{3v_T}{2K}.$$

Thus

$$G_{TH} = \frac{i_T}{v_T} = \frac{1}{25} - \frac{6}{200} = \frac{1}{100}\Omega, \ \textit{meaning } R_{TH} = 100\Omega.$$

Noting that the numerical values of v_T and i_T are NOT important, only their ratio matters. Therefore, one may assume $v_T = 1$ and solve for the corresponding numerical values of i_T so that $R_{TH} = \frac{1}{i_T}$.

□

Although there exists a way zeroing independent sources to determine equivalent resistance when only independent sources are involved, we will frequently be asked to determine equivalent resistance when dependent sources are involved. How to solve such problems? The following diagram illustrate the idea.

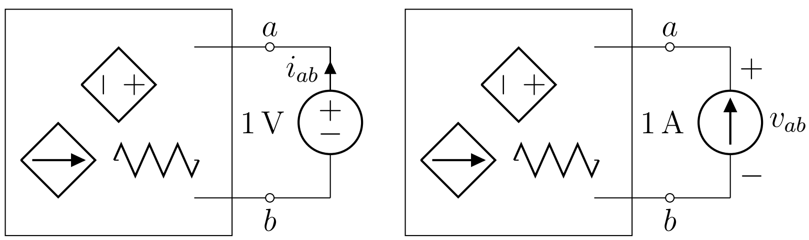


Figure 3.11: Determination of Equivalent Resistance

It is readily clear from the diagram that the equivalent resistance is obtained as

$$R_{eq} = \frac{1}{i_{ab}} \quad \text{or} \quad R_{eq} = \frac{v_{ab}}{1}$$

Also be aware that only dependent sources are allowed. If there are independent sources, deactivate the independent source first.

Example 3.6 *[2, Page 103] Determine the equivalent resistance at terminals ab for the circuit below.*
Solution: *Applying a 1-V voltage source across terminals ab and using KCL at node c, we have*

$$\begin{aligned} i_y &= i_z + 4i_y \\ i_y &= \frac{1 - 3i_z - v_c}{2} \\ v_c &= 3i_z \end{aligned}$$

Substituting, we have

$$\frac{v_c}{3} + 3\frac{1 - 2v_c}{2} = 0.$$

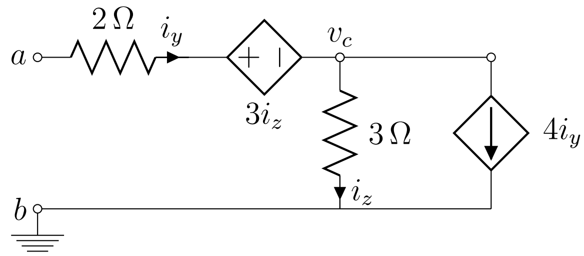


Figure 3.12: Example 3.6

Solving for v_c, *we have* $v_c = \frac{9}{16}$, $i_z = \frac{3}{16}$ *and* $i_y = -\frac{1}{16}$. *This means*

$$R_{eq} = \frac{v_{ab}}{i_{ab}} = \frac{1V}{i_y = -1/16} = -16\Omega.$$

A second method, which is the best compared with the first method, is to apply a 1-A current source to terminals ab. Accordingly, we constrain the controlling variable i_y, *which becomes*

$$i_y = 1A.$$

The current i_z *then becomes, with KCL applied at node c*

$$i_z = -4i_y + i_y = -3A$$

Applying KCL around the left loop gives

$$v_{ab} = 2i_y + 3i_z + 3i_z = -16V.$$

This means

$$R_{eq} = \frac{v_{ab}}{i_{ab}} = \frac{-16}{i_y = 1} = -16\Omega.$$

Obviously, the choice of test sources (whether a voltage source or current source) is somewhat arbitrary since either will lead to the same result. However, if a choice will pin down a controlling variable of a controlled source, that will be the best choice[4].

□

Example 3.7 *Given the circuit in Figure 3.13, (10 pts each)*
(a) attach a test source at terminal ab to determine the equivalent resistance seen by terminal ab.
(b) Find the Thevenin and Norton equivalent circuit seen by terminal ab and draw the circuit diagram.
Firstly, disable the independent source.
Answer: *(a) Use a unity voltage source to find* $i_{sc} = 0.2A$ *and thus* $R_t = \frac{1}{0.2} = 5\Omega$. *(b)* $V_{oc} = 10V$, $I_{sc} = 2A$, $R_t = 5\Omega$.

[4] Solve Example 3.5 with current source attached to terminals *ab*. Hint: Assume a current flowing into 25 Ω.

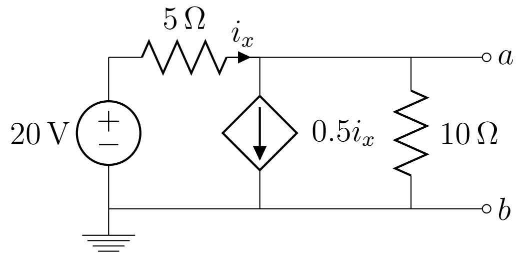


Figure 3.13: Example 3.7

□

Example 3.8 (Pspice Program for EE Lab) *Re-do your lab examples by checking the theoretical/true values using Pspice program.*

□

3.2 Circuits Analysis

3.2.1 Loop-Current Approach (Mesh Method)

This section explains how to solve a circuit problem based on solving a set of simultaneous KVL equations. In loop-current analysis, we write voltage equations and solve for the loop-current eventually. Once the loop-currents are found, it is relatively easy to find the currents, voltages, and powers for each element in the circuit.

Circuits with no current sources (i.e. only voltage sources)

Example 3.9 *Solving the following circuit*

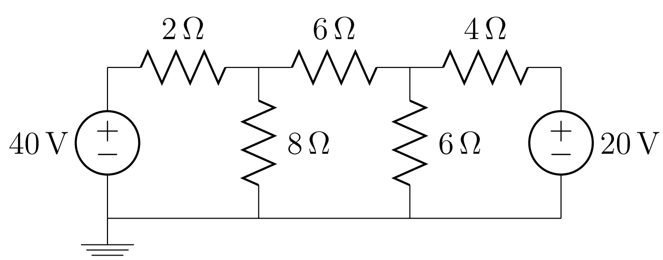


Figure 3.14: Example 3.9

Solution: *After labeling the loop currents for each mesh in a clockwise direction and assigning the voltage polarity arbitrarily, we have, traveling around the loop clockwise and summing voltages,*

$$-40 + 2i_1 + 8(i_1 - i_2) = 0$$

$$-[-8(i_2 - i_1)] + 6i_2 + 6(i_2 - i_3) = 0$$
$$-[-6(i_3 - i_2)] + 4i_3 + 20 = 0$$

Solving these simultaneous equations, we have $i_1 = 5.6A$, $i_2 = 2A$, $i_3 = -0.8A$. *To solve these equations, a MATLAB script* **inv** *can be used. Put the equations into a compact matrix form displayed below:*

$$\begin{bmatrix} 10 & -8 & 0 \\ -8 & 20 & -6 \\ 0 & -6 & 10 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 40 \\ 0 \\ -20 \end{bmatrix}$$

which has the standard form $Ax = b$, *yielding* $x = A^{-1}b$ *for a solution. For MATLAB, key in the following statements under MATLAB environment.*

```
A=[ 10 -8 0; -8 20 -6; 0 -6 10]
b=[40; 0; -20]
x=inv(A)*b
```

□

Example 3.10 *Solving the following circuit*

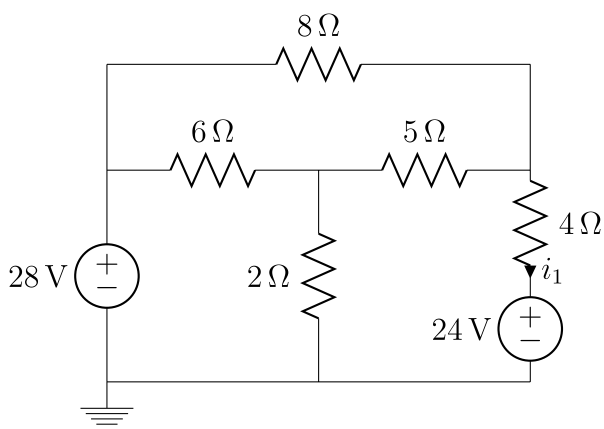


Figure 3.15: Example 3.10

Solution: *Defining loop currents clockwise for 3 meshes and labeling the voltage polarities, we find*

$$-28 + 6(i_1 - i_2) + 2(i_1 - i_3) = 0$$
$$8i_2 + 5(i_2 - i_3) + 6(i_2 - i_1) = 0$$
$$2(i_3 - i_1) + 5(i_3 - i_2) + 4i_3 + 24 = 0.$$

Solving these simultaneous equations, we have $i_1 = 4A, i_2 = 1A, i_3 = -1A$ [5].

□

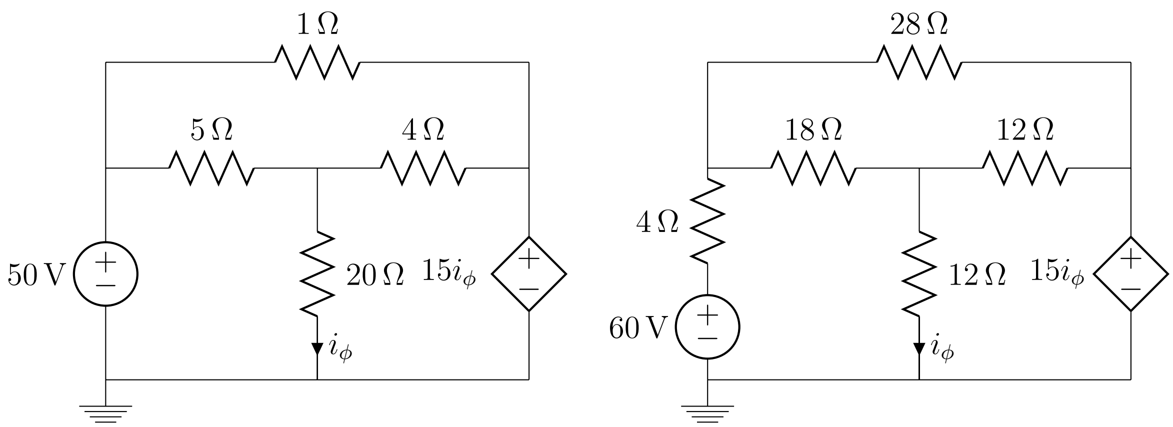


Figure 3.16: Example 3.11-3.12

Example 3.11 *Solve the following circuit.*
Solution: *Defining a clockwise loop current direction to all meshes, after the standard procedure stated above is applied, we have*

$$-50 + 5(i_1 - i_2) + 20(i_1 - i_3) = 0$$
$$i_2 + 4(i_2 - i_3) + 5(i_2 - i_1) = 0$$
$$20(i_3 - i_1) + 4(i_3 - i_2) + 15i_\phi = 0$$
$$i_\phi = i_1 - i_3. - \textit{Imposed by the presence of dependent source}$$

Solving these simultaneous equations, we have $i_1 = 29.6A$*,* $i_2 = 26A$*,* $i_3 = 28A$ [6].

□

Example 3.12 *Solve the following circuit.*
Solution: *Defining a clockwise loop current direction to all meshes, we have*

$$-60 + 4i_1 + 18(i_1 - i_2) + 12(i_1 - i_3) = 0$$
$$18(i_2 - i_1) + 28i_2 + 12(i_2 - i_3) = 0$$
$$12(i_3 - i_1) + 12(i_3 - i_2) + 15i_\phi = 0$$
$$i_1 - i_3 = i_\phi.$$

Solving these simultaneous equations, we have $i_1 = 2.25A$*,* $i_2 = 0.75A$*,* $i_3 = 0.25A$ [7].

□

[5] Verify the result by using PSpice/MATLAB.
[6] Verify the result by using PSpice/MATLAB.
[7] Verify the result by using PSpice/MATLAB.

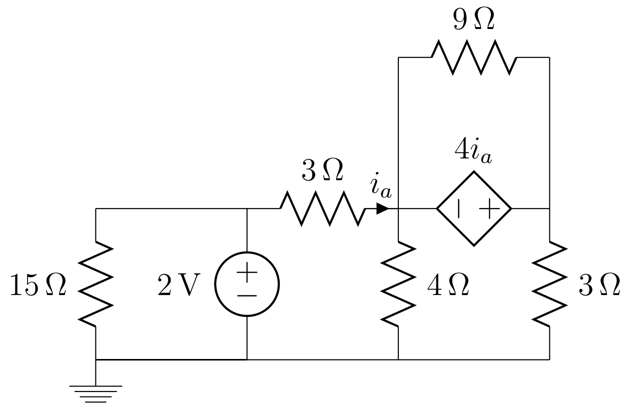


Figure 3.17: Example 3.13

Example 3.13 *Solve the following circuit.*
Solution: *Defining a clockwise loop current direction to all meshes, we have*

$$
\begin{aligned}
&15i_1 + 2 = 0\\
&-2 + 3i_2 + 4(i_2 - i_4) = 0\\
&9i_3 + 4i_a = 0\\
&4(i_4 - i_2) - 4i_a + 3i_4 = 0\\
&i_a = i_2.
\end{aligned}
$$

Solving these simultaneous equations, we have $i_1 = -0.1333A$, $i_2 = 0.8235A$, $i_3 = -0.366A$, $i_4 = 0.9412A$ [8].

□

Circuits with current sources

Sometimes it is impossible to write voltage equations when current sources are encountered. To solve the problem a variable for the unknown voltage at the current sources is required, an extra algebraic equation needed for the additional variable. However, if we do not want to increase the system equations, supermesh method can be used.

Example 3.14 *Solve the following circuit.*
Solution: *Defining a clockwise loop current direction to all meshes, we have*

$$
\begin{aligned}
&-30 + 3i_1 + 2(i_1 - i_2) + 6i_1 = 0\\
&2(i_2 - i_1) + 8i_2 + 5(i_2 - i_3) + 4i_2 = 0\\
&i_3 = -16\\
&5(i_3 - i_2) = -v_o.
\end{aligned}
$$

[8]Verify the result by using PSpice/MATLAB.

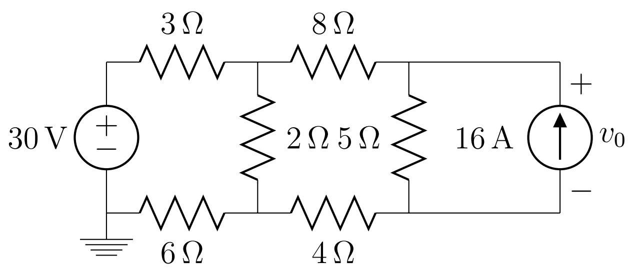


Figure 3.18: Example 3.14

Solving these simultaneous equations, we have $i_1 = 2A$, $i_2 = -4A$ [9].

□

Example 3.15 *Solve the following circuit.*

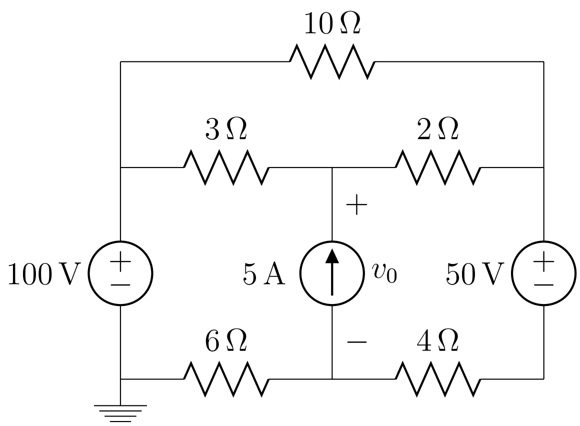


Figure 3.19: Example 3.15

Solution: *Assuming clockwise directions in every mesh, we have*

$$
\begin{aligned}
&-100 + 3(i_1 - i_2) + v_o + 6i_1 = 0 \\
&10i_2 + 2(i_2 - i_3) + 3(i_2 - i_1) = 0 \\
&-v_o + 2(i_3 - i_2) + 50 + 4i_3 = 0 \\
&i_3 - i_1 = 5.
\end{aligned}
$$

Solving these simultaneous equations, we have $i_1 = 1.75A$, $i_2 = 1.25A$, $i_3 = 6.75A$, $v_0 = 88V$. *As seen in this example,an extra equation results due to the unknown* v_0. *To reduce the system number, we apply super-mesh method, traveling the outer loop, and obtain*

$$-100 + 3(i_1 - i_2) + 2(i_3 - i_2) + 50 + 4i_3 + 6i_1 = 0$$

[9]Verify the result by using PSpice/MATLAB.

$$
\begin{aligned}
&10i_2 + 2(i_2 - i_3) + 3(i_2 - i_1) = 0\\
&i_3 - i_1 = 5.
\end{aligned}
$$

Solving, we have the same solutions. Or better yet, try a bigger current mesh (i.e., supermesh)

$$
\begin{aligned}
&i_1 = -5\\
&10i_2 + 2(i_2 - i_3) + 3(i_2 - i_1 - i_3) = 0\\
&-100 + 3(i_3 + i_1 - i_2) + 2(i_3 - i_2) + 50 + 4i_3 + 6(i_3 + i_1) = 0.
\end{aligned}
$$

□

Example 3.16 *Solve the following circuit.*

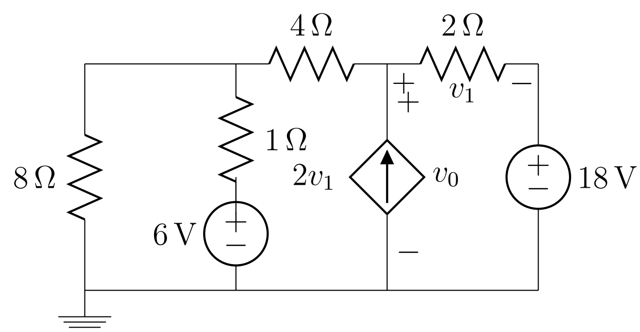


Figure 3.20: Example 3.16

Solution: *Assuming clockwise directions in every mesh, we have*

$$
\begin{aligned}
&8i_1 + (i_1 - i_2) + 6 = 0\\
&-6 + (i_2 - i_1) + 4i_2 + v_o = 0\\
&-v_0 + 2i_3 + 18 = 0\\
&i_3 - i_2 = 2v_1 = 2 \times 2i_3 \qquad \textit{thus}, i_2 + 3i_3 = 0 \ \textit{or} \ v_1 = 2i_3.
\end{aligned}
$$

Solving these simultaneous equations, we have $i_1 = -1A$, $i_2 = -3A$, $i_3 = 1A$ [10].

□

To summarize, we have the following procedure for loop-current method to solve a circuit problem.

1. Assign variables for each unknown loop-currents.

2. Write network simultaneous equations using KVL (summing of voltage).

[10] Solve this problem via PSpice/MATLAB.

3. If current sources are involved, either assign a voltage variable and add an extra equation or use the supermesh method.

4. If dependent sources are involved, extra equations are needed, depending on the number of dependent sources.

5. Use the values solved for the loop-currents to determine other currents, voltages and powers in the circuit.

3.2.2 Node-voltage Approach (Nodal Method)

This section explains how to solve a circuit problem based on solving a set of simultaneous KCL equations. In node-voltage analysis, we write current equations and solve for the node-voltage eventually. Once the node-voltages have been found, it is relatively easy to find the currents, voltages, and powers for each element in the circuit.

Circuits with no voltage sources (i.e. only current sources)

Example 3.17 *Solve the following circuit.*

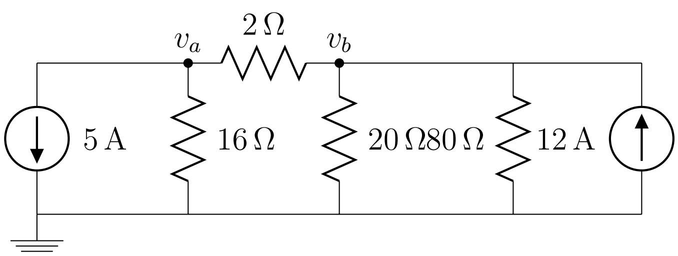


Figure 3.21: Example 3.17(a)

Solution: *There are two nodes in the circuit. At node a, we apply KCL, adding all of the currents leaving node a and setting the sum to zero,*

$$5 + \frac{v_a}{16} + \frac{v_a - v_b}{2} = 0.$$

At node b, KCL yields

$$\frac{v_b}{20} + \frac{v_b}{80} - \frac{v_a - v_b}{2} - 12 = 0.$$

Solving these simultaneous equations, we have $v_a = 48V$, $v_b = 64V$[11]. Or using of network theorem on source transformation, we have the following circuit diagram after reduction. whose single loop

[11]Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.

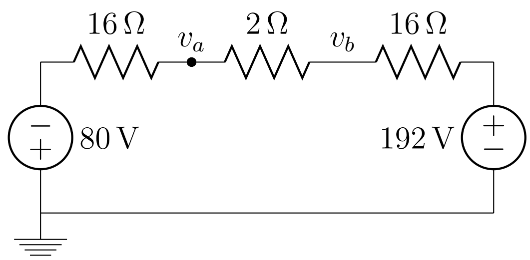


Figure 3.22: Example 3.17(b)

equation is easily obtained

$$I = \frac{192 - (-80)}{34} = 8$$
$$v_a - 16 \times 8 = -80.$$

Therefore $v_a = 48\,V$.

□

Example 3.18 *Solve the following circuit.*

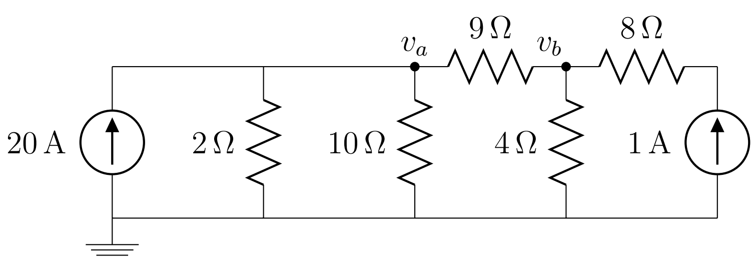


Figure 3.23: Example 3.18

Solution: *Assume entering current is positive and we have*

$$20 - \frac{v_a}{2} - \frac{v_a}{10} + \frac{v_b - v_a}{9} = 0$$

Similarly, at node b, we have

$$-\frac{v_b - v_a}{9} - \frac{v_b}{4} + 1 = 0.$$

Solving these simultaneous equation, we have $v_a = 30V$, $v_b = 12V$[12].

□

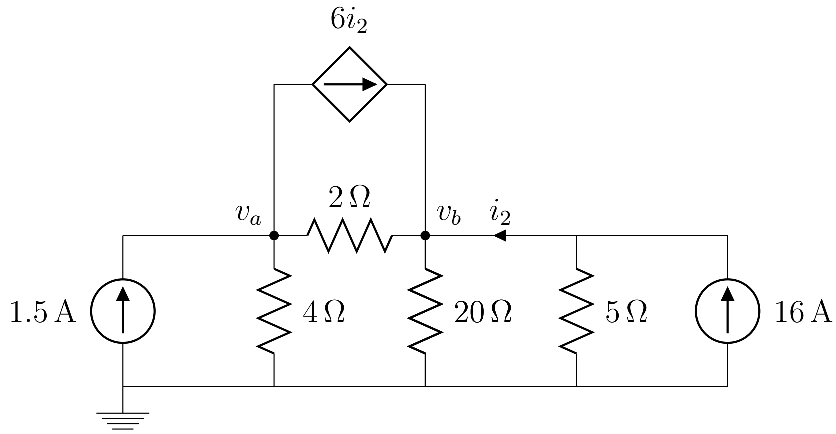


Figure 3.24: Example 3.19

Example 3.19 (Dependent Current Sources) *Solve the following circuit.*
Solution: *Assume entering current is positive and we have*

$$1.5 - \frac{v_a}{4} - \frac{v_a - v_b}{2} - 6i_2 = 0$$
$$6i_2 + \frac{v_a - v_b}{2} - \frac{v_b}{20} + i_2 = 0$$
$$i_2 = -\frac{v_b}{5} + 16.$$

Solving the simultaneous equations, we have $v_a = 10\,V$, $v_b = 60\,V$, $i_2 = 4A$[13].

□

Example 3.20 (Dependent Current Sources) *Solve the following circuit.*
Solution: *Assume entering current is positive and we have*

$$-\frac{v_a}{15} + 2 - i_a = 0$$
$$i_a - \frac{v_b}{4} - \frac{v_b - v_c}{9} + 4i_a = 0$$
$$\frac{v_b - v_c}{9} - 4i_a - \frac{v_c}{3} = 0$$
$$i_a = \frac{v_a - v_b}{3}.$$

Solving the simultaneous equations, we have $v_a = 15\,V$, $v_b = 12\,V$, $v_c = -6\,V$[14].

□

[12]Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[13]Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[14]Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.

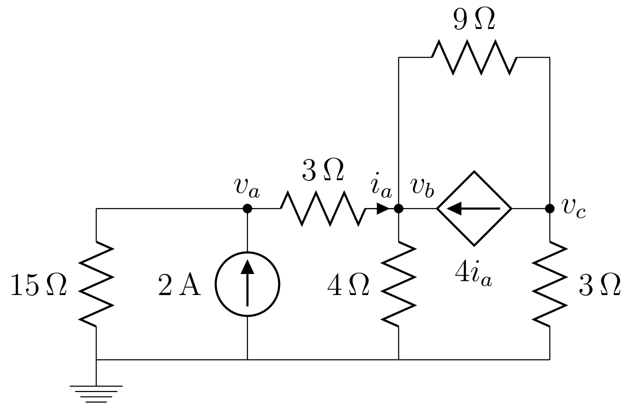


Figure 3.25: Example 3.20

Circuits with voltage sources

When voltage sources are involved, it is, in some cases, hard to write KCL at each node. Again to solve the problem a variable is needed for the unknown current flowing through the voltage source. Thus an extra algebraic equation results. However, such case can be avoided, if super node notion is applied.

Example 3.21 *Solve the following circuit.*

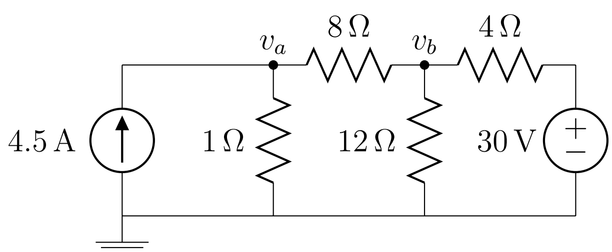


Figure 3.26: Example 3.21

Solution: *Summing the current entering node a, we have*

$$4.5 - \frac{v_a}{1} - \frac{v_a - v_b}{8} = 0$$

Similarly, at node b, KCL yields

$$\frac{v_a - v_b}{8} - \frac{v_b}{12} + \frac{30 - v_b}{4} = 0.$$

Solving simultaneous equations, we have $v_a = 6V$, $v_b = 18V$[15].

□

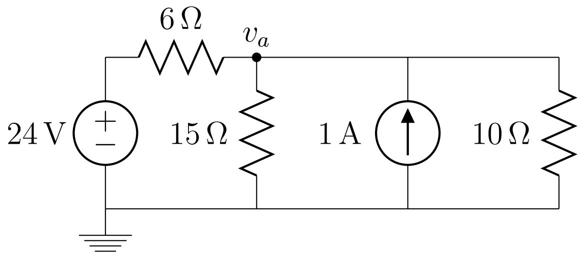


Figure 3.27: Example 3.22

Example 3.22 *Solve the following circuit.*
Solution: *Summing the currents leaving node a, we have*

$$\frac{v_a - 24}{6} + \frac{v_a}{15} - 1 + \frac{v_a}{10} = 0.$$

Therefore $v_a = 15V$[16].

□

Example 3.23 *Solve the following circuit.*

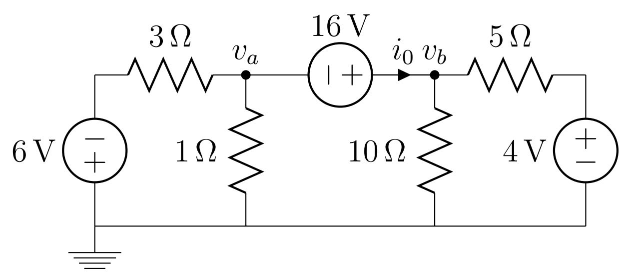


Figure 3.28: Example 3.23

Solution: *Summing the currents leaving node a, we have*

$$\frac{v_a + 6}{3} + \frac{v_a}{1} + i_0 = 0.$$

Similarly, at node b, we have

$$-i_0 + \frac{v_b}{10} - \frac{4 - v_b}{5} = 0.$$

Since a voltage source appears between node a and node b, it is impossible to write current equations for both nodes without assigning an unknown i_0 *for the current flowing through the* $-16V$ *voltage source, requiring an extra equation.*

$$v_b = v_a + 16.$$

[15] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[16] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.

Solving simultaneous equations, we have $v_a = -3.6735V$, $v_b = 12.3265V$[17]. *Another way to obtain a current equation is to form a supernode and the apply* KCL

$$\frac{v_a+6}{3} + \frac{v_a}{1} + \frac{v_b}{10} - \frac{4-v_b}{5} = 0$$
$$v_b = v_a + 16$$

from which we obtain the same solution $v_a = -3.673V$, $v_b = 12.327V$[18].

□

Example 3.24 *Solve the following circuit.*

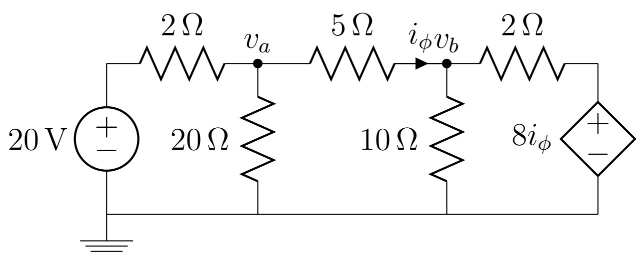


Figure 3.29: Example 3.24

Solution: *Summing the currents entering node a and node b, we have*

$$\frac{20-v_a}{2} - \frac{v_a}{20} - \frac{v_a-v_b}{5} = 0$$
$$\frac{v_a-v_b}{5} - \frac{v_b}{10} + \frac{8i_\phi - v_b}{2} = 0.$$

Next, find an expression for the controlling variable in terms of node-voltages. This is because the diamond shape indicates it is a dependent source, an extra equation required.

$$i_\phi = \frac{v_a - v_b}{5}.$$

Solving simultaneous equations, we have $v_a = 16V$, $v_b = 10V$, $i_\phi = 1.2A$[19].

□

Example 3.25 (Dependent Voltage Sources) *Solve the following circuit.*
Solution: *Summing the currents entering node a and assigning an unknown current* i_0 *through the dependent source, we have*

$$-i_\phi - \frac{v_a}{50} - i_0 = 0.$$

[17] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[18] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[19] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.

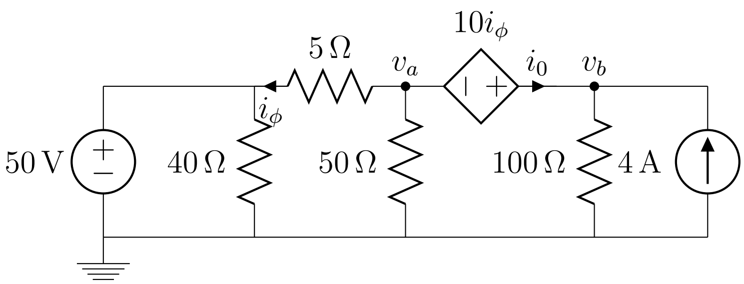


Figure 3.30: Example 3.25

Similarly, at node b, we have

$$i_0 - \frac{v_b}{100} + 4 = 0.$$

Next, find an expression for the controlling variable in terms of node-voltages

$$\begin{aligned} v_b &= v_a + 10 i_\phi \\ i_\phi &= \frac{v_a - 50}{5} \end{aligned}$$

Solving simultaneous equations, we have $v_a = 60V$, $v_b = 80V$, $i_0 = -3.2A$[20]. *Or use supernode method*

$$\begin{aligned} &-i_\phi - \frac{v_a}{50} - \frac{v_b}{100} + 4 = 0 \\ &v_b = v_a + 10 i_\phi \\ &i_\phi = \frac{v_a - 50}{5}. \end{aligned}$$

□

Example 3.26 (Wheatstone Bridge) *[1, Page 97] Given the following circuit where* R_1, R_2 *and* R_3 *are known. Find the resistance* R_x *when balanced condition* $i_{ab} = 0$ *and* $v_{ab} = 0$ *is reached*[21].
Solution: *Writing* KCL *at note a and b, respectively, leads to*

$$i_1 = i_{ab} + i_3 \text{ and } i_2 + i_{ab} = i_4$$

since $i_{ab} = 0$, *we have*

$$i_1 = i_3 \text{ and } i_2 = i_4$$

Traveling clockwise around upper triangle and lower triangle, KVL *yields*

$$R_1 i_1 + v_{ab} = R_2 i_2 \text{ and } v_{ab} + i_4 R_x = R_3 i_3$$

[20] Use the mesh method to solve the problem and verify the result by using PSpice/MATLAB.
[21] Given the wheatstone bridge above where $R_1 = 1\Omega, R_2 = 2\Omega, R_3 = 3\Omega, R_x = 4\Omega$, terminal ab is open and $v_s = 0$, find the equivalent resistance seen from terminal ab.

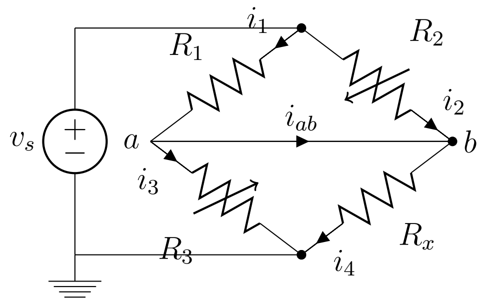


Figure 3.31: Example 3.26

since $v_{ab} = 0$, we have

$$R_1 i_1 = R_2 i_2 \text{ and } R_3 i_3 = i_4 R_x.$$

Dividing each side of the first equation by the respective side of the second equation, we have

$$\frac{R_1 i_1}{R_3 i_3} = \frac{R_2 i_2}{R_x i_4}$$

since $i_1 = i_3$ and $i_2 = i_4$, we have

$$\frac{R_1}{R_3} = \frac{R_2}{R_x}$$

This example tells that by adjusting R_2 and R_3, we are able to measure R_x when balance condition is reached.

Having gone through the examples in details, we summarize in below the solving procedure for node-voltage method:

1. Assign variables for each unknown node-voltages.
2. Write network equation using KCL.
3. If voltage sources are involved, either assign a current variable, adding an extra equation or use the supernode method.
4. If dependent sources are involved, extra equations are needed, depending on the number of dependent sources.
5. Use the valued solved for the node-voltages to determine other currents, voltages and powers in the circuit.

3.3 The Principle of Superposition

A function $f(x)$ is linear[22] if $f(ax_1 + bx_2) = af(x_1) + bf(x_2)$. In other words, the total response is the sum of individual responses. In circuit terms, for circuits containing N independent sources, any element voltage (or current) in that circuit is composed of the sum of N contributions, each of which is due to one of the independent sources acting individually when all others are set equal to zero (being deactivated). **A deactivated independent source is replaced by a short circuit while a deactivated independent current source is replaced by an open circuit**.

Circuits with independent sources

The concept of superposition is better explained by given out an example.

Example 3.27 (Circuits with Independent Sources) *Find currents due to voltage sources and current sources, respectively.*

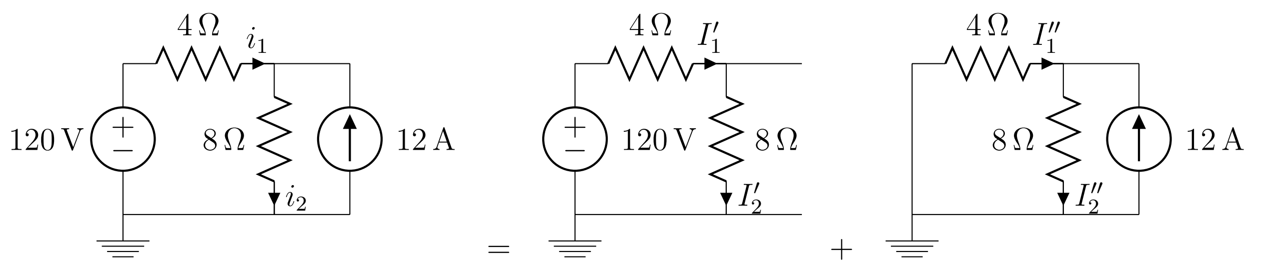


Figure 3.32: Example 3.27

Solution: *For circuit T, writing KCL at node a yields*

$$\frac{120 - v_a}{4} + 12 = \frac{v_a}{8}$$

Solving, we have $v_a = 112V$, $i_1 = (120 - 112)/4 = 2A$ and $i_2 = 112/8 = 14A$.

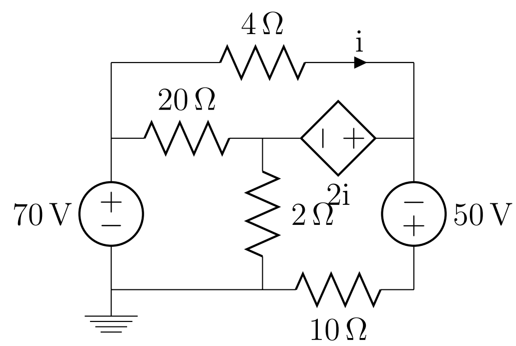
For T', a simple Ohm's law yields

$$i_1' = i_2' = \frac{120}{12} = 10A.$$

For T'', a simple current divider yields

$$i_1'' = -12(\frac{8}{12}) = -8A, i_2'' = 4A.$$

Notice that $i_1 = i_1' + i_1''$ and $i_2 = i_2' + i_2''$.



Circuits with dependent sources

Example 3.28 (Circuits with Dependent Sources) *Find currents due to different sources respectively.*
Solution: *Firstly, we decompose the overall circuit into two different circuits with single source only.*

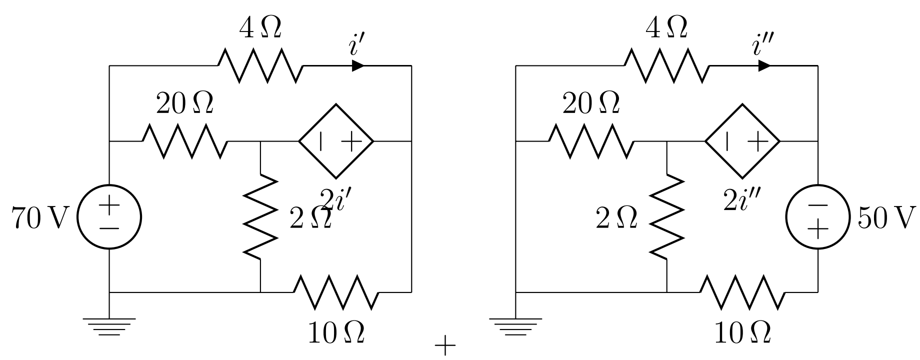


Figure 3.33: Example 3.28

For circuit T, writing KVL for 3 individual loop yields (assuming clockwise direction)

$$\begin{aligned}70 &= 20(i_a - i_b) + 2(i_a - i_c)\\ 0 &= 4i_b + 2i_b + 20(i_b - i_a)\\ 50 &= -2i_b + 2(i_c - i_a) + 10i_c\end{aligned}$$

Solving, we have $i_a = 13A$, $i_b = 10A$, and $i_c = 8A$.
For T', we have

$$\begin{aligned}70 &= 20(i'_a - i'_b) + 2(i'_a - i'_c)\\ 0 &= 4i'_b + 2i'_b + 20(i'_b - i'_a)\\ 0 &= -2i'_b + 2(i'_c - i'_a) + 10i'_c\end{aligned}$$

[22] How to interpret the linear function if only x_1 exists? i.e., $b = 0$.

Solving, we have $i'_a = 11.6170A$*,* $i'_b = 8.9362A$*, and* $i'_c = 3.4255A$*.*

For T''*, we have*

$$\begin{aligned} 0 &= 20(i''_a - i''_b) + 2(i''_a - i''_c) \\ 0 &= 4i''_b + 2i''_b + 20(i''_b - i''_a) \\ 50 &= -2i''_b + 2(i''_c - i''_a) + 10i''_c \end{aligned}$$

Solving, we have $i''_a = 1.3830A$*,* $i''_b = 1.0638A$*, and* $i''_c = 4.5745A$*, confirming that* $i_a = i'_a + i''_a$*,* $i_b = i'_b + i''_b$*, and* $i_c = i'_c + i''_c$*.*

We conclude that **dependent sources do not contribute to a separate term to the total response***. This is because if we zero both of the independent sources, the total response becomes zero.*

3.4 Problems

Equivalence

Problem 3.1 *Determine the current* $v(t)$ *and* $i(t)$ *in Figure 3.34 such that the two circuits are equivalent at terminal ab.*

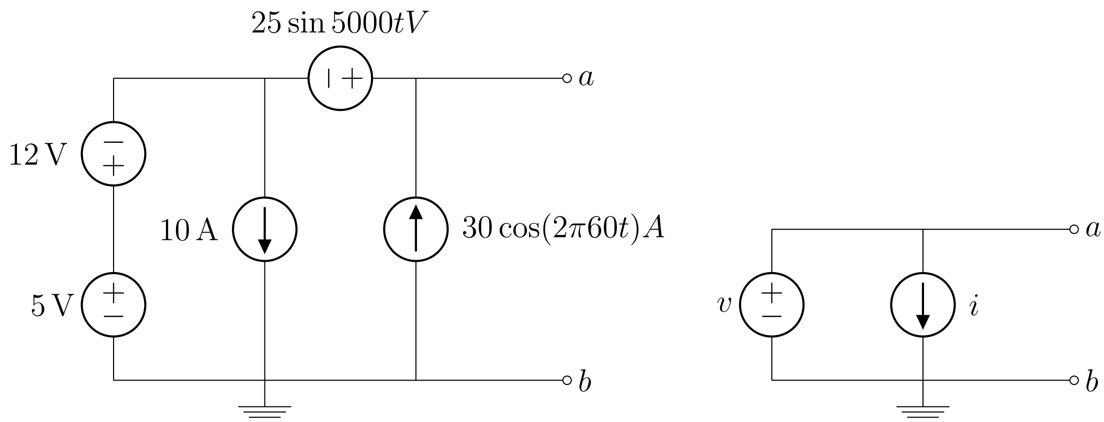


Figure 3.34: Circuit Diagram for Problem 3.1

Answer: $i = 10 - 30\cos(2\pi 60t)A$, $v = 5 - 12 + 25\sin 5000tV$.

Problem 3.2 *In the Figure 3.35, find the equivalent resistance looking in at terminals cd (a) if terminals a and b are open. (b) If terminals a and b are shorted. (c) If terminals a and b are connected with a voltage source* v_s*, find the value of the voltage* $v_{cd} = v_c - v_d$.

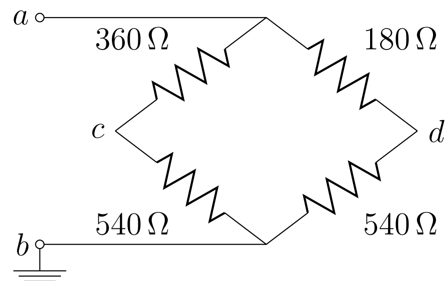


Figure 3.35: Circuit Diagram for Problem 3.2

Answer: *(a)* 360Ω *(b)* 351Ω *(c)* $v_{cd} = \frac{3}{20}v_s$.

Problem 3.3 *Given the Figure 3.36, (a) find Thevenin equivalent resistance seen from terminal ab. (Hint: connect a 1-A current source across terminals ab, then solve the network by node-voltage method.) (b) If the line segment $\bar{12}$ is moved to the dotted line position, what is the equivalent resistance seen from terminal ab (no need to attach any external source.)*

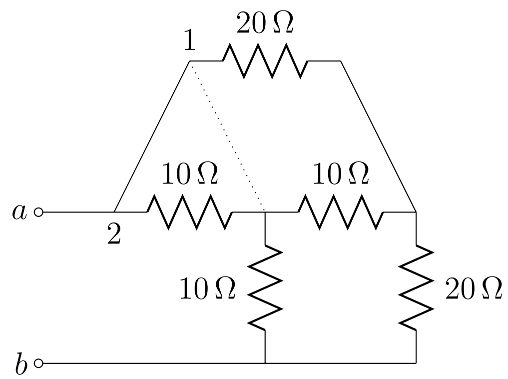


Figure 3.36: Circuit Diagram for Problem 3.3

Answer: *(a)* $190/11 = 13.333\Omega$. *(b)* $\frac{190}{11}\Omega$

Problem 3.4 *Determine the equivalent resistance at terminal ab shown in Figure 3.37.*

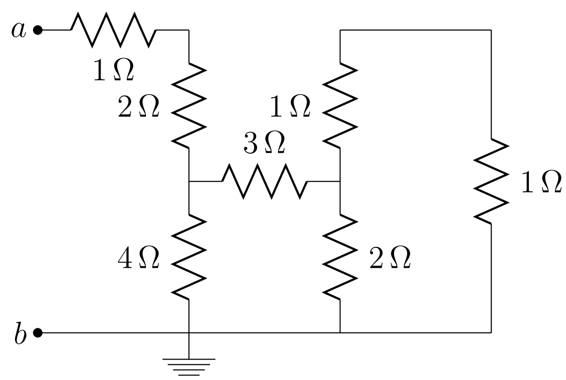


Figure 3.37: Circuit Diagram for Problem 3.4

Answer: 5Ω.

Problem 3.5 *Given the Figure 3.38, find the Thevenin equivalent seen by R_L and the Norton equivalent seen by R_L.*
Answer: *(a)* $v_{oc} = 10V$, $R_{th} = 0\Omega$. *(b)* $i_{sx} = 1A$, $R_{th} = \infty\Omega$. *(This example justifies the notion that voltage sources are always in series with a resistor and current sources are always in parallel with a resistor.)*

Problem 3.6 *Given the Figure 3.39, use source transformation to solve for the values of i_1, i_2.*
Answer: *(a)* $i_1 = 1A$, $i_2 = 2A$.

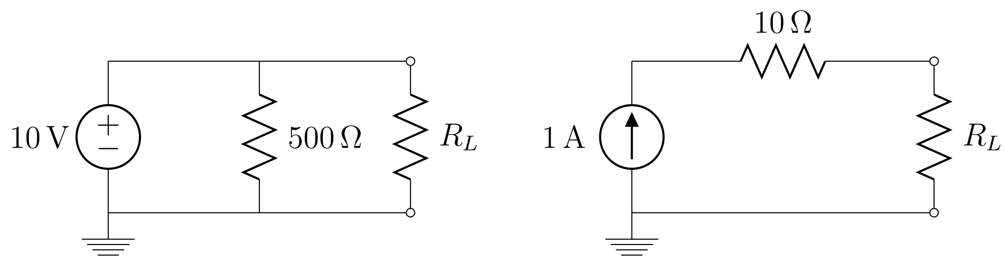


Figure 3.38: Circuit Diagram for Problem 3.5

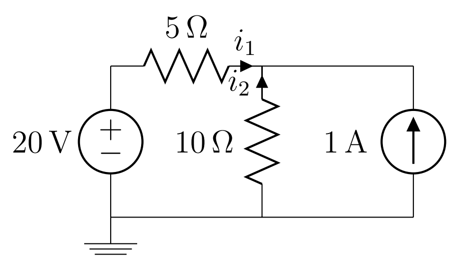


Figure 3.39: Circuit Diagram for Problem 3.6

Problem 3.7 *Given the Figure 3.40, find the Thevenin equivalent circuit.*

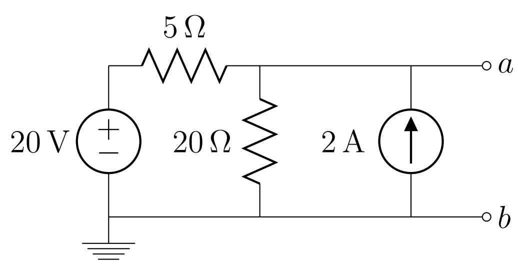


Figure 3.40: Circuit Diagram for Problem 3.7

Answer:*(a)* $v_{oc} = 4V$ *(b)* $R_{th} = 4\Omega$.

Problem 3.8 *Find the Thevenin equivalent for the circuit shown in Figure 3.41 by finding (a) open-circuit voltage and (b) short-circuit current.*

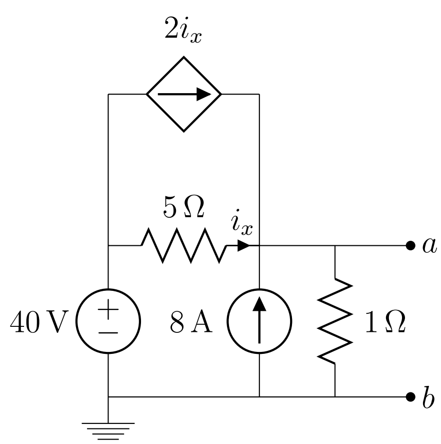


Figure 3.41: Circuit Diagram for Problem 3.8

Problem 3.9 *In the Figure 3.42, (a) find the short-circuit current. (b) Find the open-circuit voltage. (c) Find the Norton equivalent resistance by inspection. (d) Draw the Norton equivalent circuit seen from terminal ab. (e) the current flowing in* 2Ω *resistor. (f) The power consumed by the* 2Ω *resistor.*
Answer: *(a)* $i_{ab} = \frac{28}{3}$ *(b)* $v_{ab} = \frac{56}{3}$ *(c)* $R_{th} = 2$ *(d)* $i_{12\Omega} = \frac{4}{3}$ *(d)* $P_{12\Omega} = \frac{64}{3}$

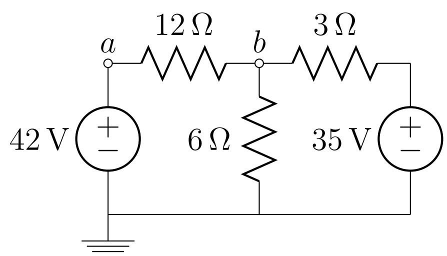


Figure 3.42: Circuit Diagram for Problem 3.9

Problem 3.10 *Given the Figure 3.43, find the Thevenin and Norton equivalent respectively.*

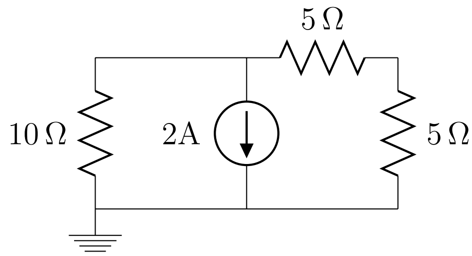


Figure 3.43: Circuit Diagram for Problem 3.10

Answer: *(a)* $v_{oc} = -5V$, $R_{th} = 3.75$ *(b)* $i_{sc} = -1.33A$, $R_n = 3.75$.

Problem 3.11 *Given the circuit in Figure 3.44, (a) solve for the node voltage* v_1 *and* v_2 *shown in the figure. (b) Find the current* i_x*. (c) Find the Thevenin* v_{oc} *seem from* 10Ω *resistor. (d) Find the Thevenin* i_{sc} *seem from* 10Ω *resistor.*

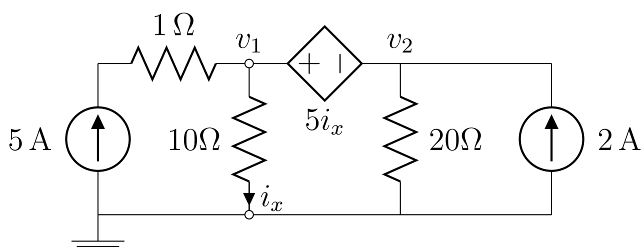


Figure 3.44: Circuit Diagram for Problem 3.11

Answer: *(a)* $v_1 = 56V$, $v_2 = 28V$. *(b)* $i_x = 5.6A$. *(c)* $v_{oc} = 140V$ *(d)* $i_{sc} = \frac{28}{3}A$, $R_t = 15\Omega$.

Problem 3.12 *Given the circuit in Figure 3.45, (a) attach a test source at terminal ab to determine the equivalent resistance seen by terminal ab. (b) Find the Thevenin and Norton equivalent circuit seen by terminal ab and draw the circuit diagram.*

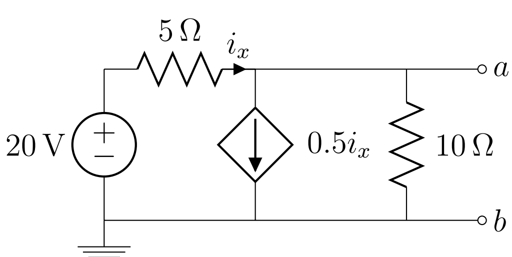


Figure 3.45: Circuit Diagram for Problem 3.12

Answer: *(a) Use a unity test voltage source to find* $i_{test} = 0.2A$ *and thus* $R_t = \frac{1}{0.2} = 5\Omega$. *(b)* $v_{oc} = 10V$, $i_{sc} = 2A$, $R_t = 5\Omega$.

Problem 3.13 *Given Figure 3.46, when a* 100Ω *load is attached to a circuit, the load voltage is* $10V$*. When the load is increased to* 200Ω*, the load voltage becomes* $12V$*. Find and draw the Thevenin and Norton equivalents for the circuit.*

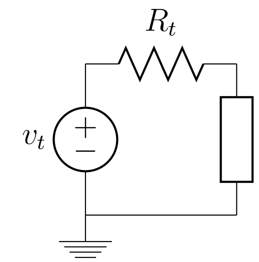


Figure 3.46: Circuit Diagram for Problem 3.13

Answer: $R_t = 50\Omega$, $v_t = 15V$.

Problem 3.14 *Find the Thevenin equivalent seen from terminal ab to the left for the circuit in Figure 3.47 and calculate (a)* v_{oc} *(b)* i_{sc} *(c)* R_{th} *and (d) draw the Thevenin equivalent circuit.*

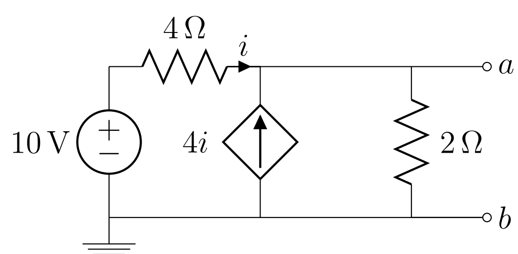


Figure 3.47: Circuit Diagram for Problem 3.14

Answer: *(a)* $v_{oc} = 7.14V$*. (b)* $i_{sc} = 12.5A$*. (c)* $R_{th} = 0.57\Omega$.

Problem 3.15 *Find the Thevenin circuits for the circuit shown in Figure 3.48.*

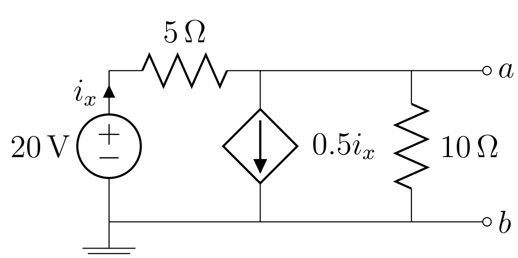


Figure 3.48: Circuit Diagram for Problem 3.15

Answer: $v_{ab} = 10V$, $i_{ab} = 2A$, $R_t = 5\Omega$.

Circuit analysis

Problem 3.16 *Find the i_1 in Figure 3.49 where the ground node is not labeled. (a) Which method would you use? and why? (b) Indicate your ground node in your diagram and solve for i_1.*

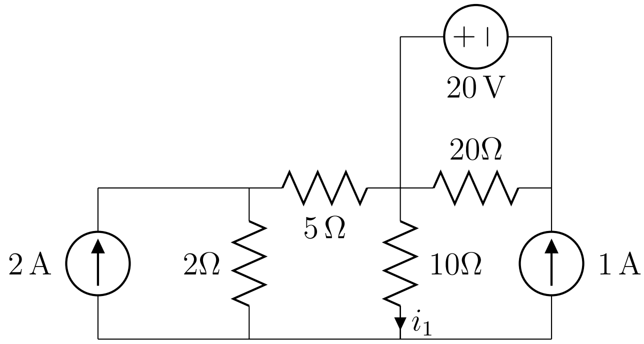


Figure 3.49: Circuit Diagram for Problem 3.16

Answer: *(a) Label the top node of 1A current source as the ground node so that only two nodes are needed to solve the circuit problem. (b) $i_1 = 0.647A$.*

Problem 3.17 *In the Figure 3.50, determine the current in the 3Ω resister using (a) node-voltage method (b) loop-current method (c) Thevenin equivalent seen from terminal ab.*
Answer: *(a) $3A$ (b) $i_1 = 1.33A$, $i_2 = 3A$ (c) $v_{oc} = 14V$, $R_{th} = 4\Omega$, $i = 3A$.*

Problem 3.18 *Assuming clockwise current direction for the figure of problem 3.51, (a) write the simultaneous equation. (b) Solve for the loop current as indicated*
Answer: *(a) $-12 = 3i_1 + 4(i_1 - i_2) - 4$, $4(i_1 - i_2) = 5i_2 + 8(i_2 - i_3)$, $-4 = 8(i_3 - i_2) + 6i_3$ (b) $i_1 = -1.529A, i_2 = -0.676A, i_3 = -0.672A$.*

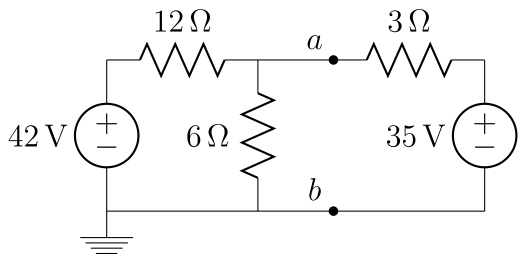


Figure 3.50: Circuit Diagram for Problem 3.17

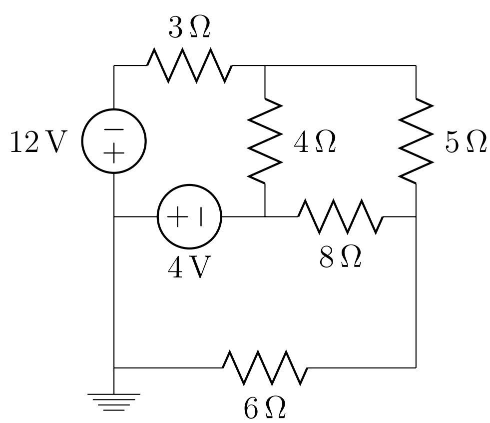


Figure 3.51: Circuit Diagram for Problem 3.18

Problem 3.19 *Given the figure for problem 3.52, (a) find the Thevenin and Norton equivalents. (b) Use superposition method to find the voltage across* 2Ω*.*

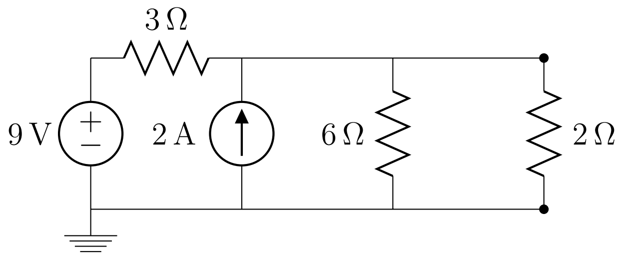


Figure 3.52: Circuit Diagram for Problem 3.19

Answer: *(a)* $v_{oc} = 10V$, $R_{th} = 2\Omega$; $i_{sc} = 5A$, $R_{th} = 2\Omega$ *(b) 3+2=5V.*

Problem 3.20 *Given the Figure 3.53, (a) use the node-voltage method to solve for the values of* v *and* i_x*. (b) Let the voltage be replaced by 20V voltage source, find the values of* v *and* i_x *again.*

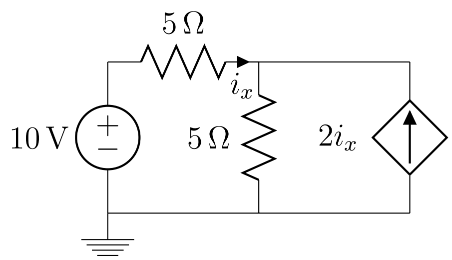


Figure 3.53: Circuit Diagram for Problem 3.20

Answer: *(a)* $v = 7.5$, $i_x = 0.5A$. *(b)* $v = 15$, $i_x = 1A$ *by linearity property.*

Problem 3.21 *Given the Figure 3.54, solve for the currents.*

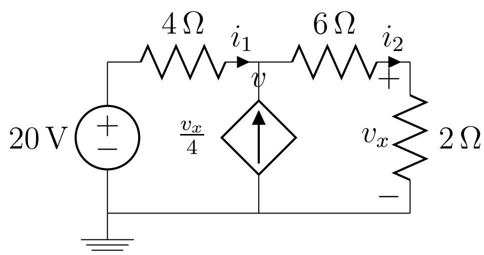


Figure 3.54: Circuit Diagram for Problem 3.21

Answer: $i_1 = 1A, i_2 = 2A$.

Problem 3.22 *Given the Figure 3.55, find the current i_1, i_2 and i_3.*

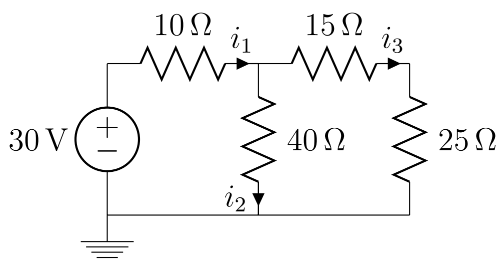


Figure 3.55: Circuit Diagram for Problem 3.22

Answer: $i_1 = 1A$, $i_2 = i_3 = 0.5A$.

Problem 3.23 *Given the Figure 3.56, solve for i_s.*

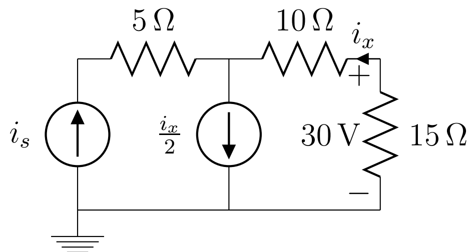


Figure 3.56: Circuit Diagram for Problem 3.23

Answer: $i_s = 1A$.

Problem 3.24 *Given the Figure 3.57, use node-voltage method to find the value of i_1.*

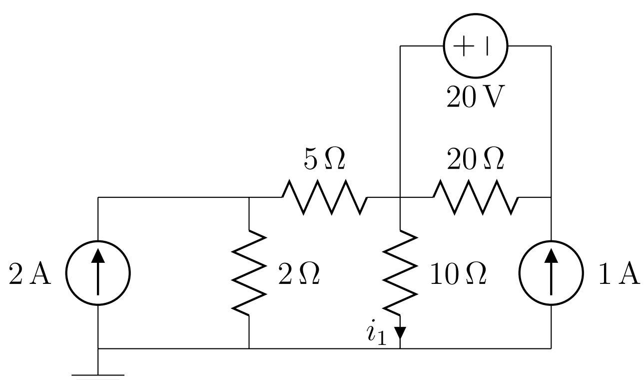


Figure 3.57: Circuit Diagram for Problem 3.24

Answer: $i_1 = 0.6470A$.

Problem 3.25 *Given the Figure 3.58, determine i by using (a) loop-current method (b) node-voltage method (c) superposition method.*

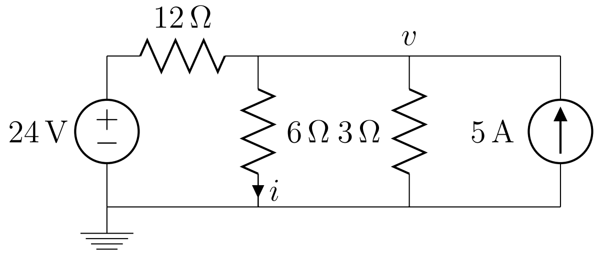


Figure 3.58: Circuit Diagram for Problem 3.25

Answer: *(a) $i = i_1 + i_2 = 2A$ (b) $v = 12V, i = 2A$ (c) $i = i_1 + i_2 = 0.5714 + 1.4826 = 2A$.*

Problem 3.26 *Given the Figure 3.59, find (a) the current i_1 (b), the voltage v_0 and (c) the value of dependent current source.*

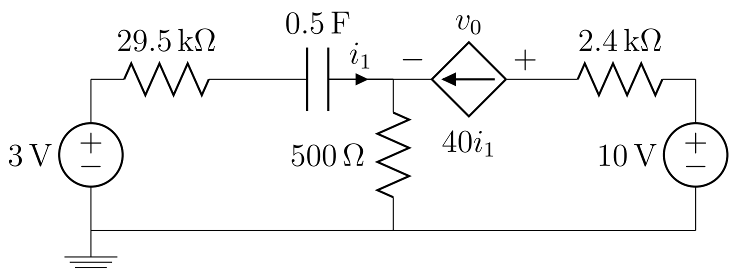


Figure 3.59: Circuit Diagram for Problem 3.26

Answer: *(a) (b) (c) (d) (e)*

Problem 3.27 *Find the voltage v and the current i_1 and i_2 for the circuit in Figure 3.60.*

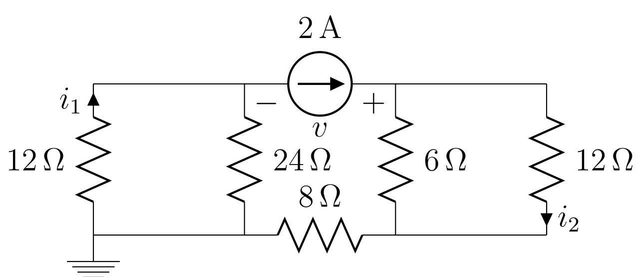


Figure 3.60: Circuit Diagram for Problem 3.27

Answer: $i_1 = \frac{4}{3}A$, $i_2 = \frac{2}{3}A$, $v = 40V$.

Problem 3.28 *Solve Figure 3.61 for v_1 and v_2.*

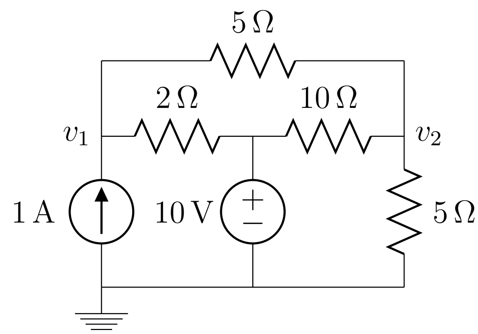


Figure 3.61: Circuit Diagram for Problem 3.28

Answer: $v_1 = 10.32V$, $v_2 = 6.129V$.

Problem 3.29 *Write a set of KCL for Figure 3.62 below*

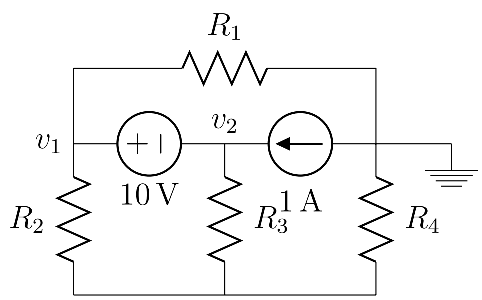


Figure 3.62: Circuit Diagram for Problem 3.29

Answer: $\frac{v_1}{R_1} + \frac{v_1 - v_3}{R_2} + \frac{v_2 - v_3}{R_3} = 1$, $\frac{v_1 - v_3}{R_2} + \frac{v_2 - v_3}{R_3} = \frac{v_3}{R_4}$, $v_1 - 10 = v_2$.

Problem 3.30 *In the Figure 3.63, determine the current in the 3Ω resister using (a) node-voltage method (b) loop-current method (c) Thevenin equivalent seen from terminal ab.*

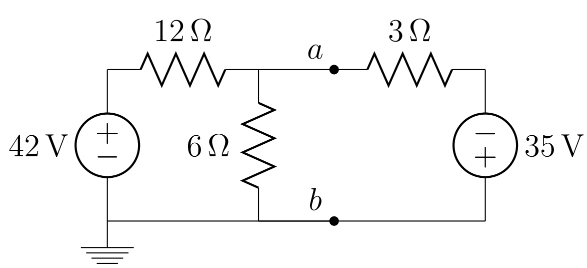


Figure 3.63: Circuit Diagram for Problem 3.30

Answer: *(a) $i_{3\Omega} = 2.5714A$ (b) same as (a) (c) $v_{oc} = 16V, R_{th} = 3.22$.*

Problem 3.31 *Find the unknown current i_x and the unknown voltage v_x using mesh current analysis for the circuit in Figure 3.64 where the dependent source is related to the currents i_x and i_2 by $v_x = 5(i_2 - i_x)$*

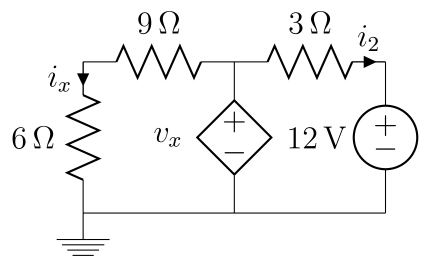


Figure 3.64: Circuit Diagram for Problem 3.31

Answer: $i_x = 4A, v_x = 60V$.

Problem 3.32 *The current source i_x is related to the voltage v_x in Figure 3.65 by the relation $i_x = v_x/3$, find the voltage across the 8Ω resistor by nodal analysis.*

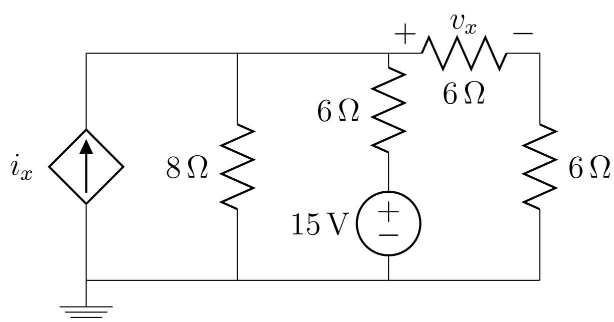


Figure 3.65: Circuit Diagram for Problem 3.32

Answer: $v_a = 12V$, $v_x = 16V$.

Problem 3.33 *Use mesh-current and node-voltage method to find i_a and i_b in Figure 3.66.*

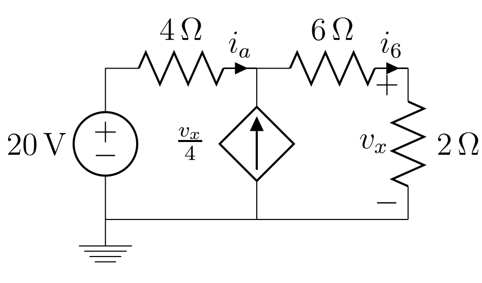


Figure 3.66: Circuit Diagram for Problem 3.33

Answer: $i_a = 1A$, $i_b = 2A$.

Problem 3.34 *Find the Thevenin circuit seen from terminal a and b of Figure 3.67. Find the current flowing through a and b due to the 20V voltage source.*

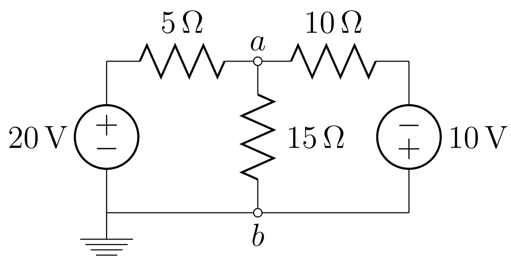


Figure 3.67: Circuit Diagram for Problem 3.34

Answer: $R_{th} = \frac{10}{3}\Omega$, $i = 1.82A$, $i_1 = 0.73A$.

Superposition

Problem 3.35 *Find the responses $v_{1,15V}$ of 10Ω due to 15V, $v_{2,2A}$ of 5Ω due to 2A for the circuit in Figure 3.68. Furthermore, find $v_{1,2A}$ of 10Ω due to 2A, $v_{2,15V}$ of 5Ω due to 15V.*

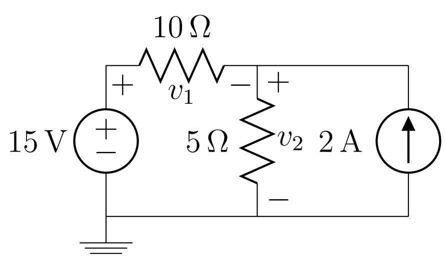


Figure 3.68: Circuit Diagram for Problem 3.35

Answer: $v_{1,15} = 10V$, $v_{2,15} = 5V$, $v_{1,2A} = -6.667V$, $v_{2,2A} = 6.667V$.

Problem 3.36 *(a) Find the individual current i in Figure 3.69 due to 3A current source and 30V voltage source, respectively, using superposition. (b) If the value of $3A$ current source is increased to $6A$, what is the i*
Answer: *Since $i_{30V} = 2A$ and $i_{3A} = 2A$, we have $i = 4A$. (b) $i_{6A} = 4A$, so $i = 6A$.*

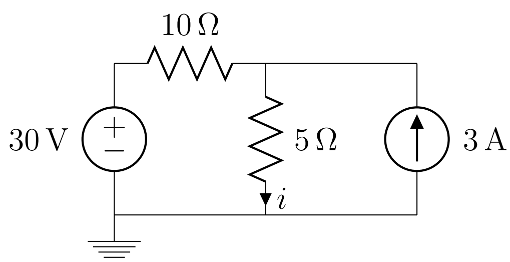


Figure 3.69: Circuit Diagram for Problem 3.36

Problem 3.37 *(a) Find the voltage v_a and v_b for the circuits of Figure 3.70 by superposition. (b) Find v_a and v_b again when the current source is replaced by 2mA.*

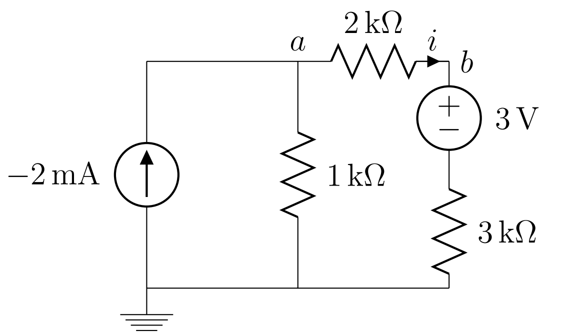


Figure 3.70: Circuit Diagram for Problem 3.37

Answer: *(a) $v_a = -1.167V$, $v_b = 0.5V$. (b)*

Problem 3.38 *Given the Figure 3.71, use principle of superposition to find the current i_o. (a) Draw individual circuits for each energy source. (b) Find i_o due to 90V voltage-source. (c) Find i_0 due to 30 A current source. (d) Find i_o due to 45 V voltage source. (e) Find total current i_o due to all energy sources.*

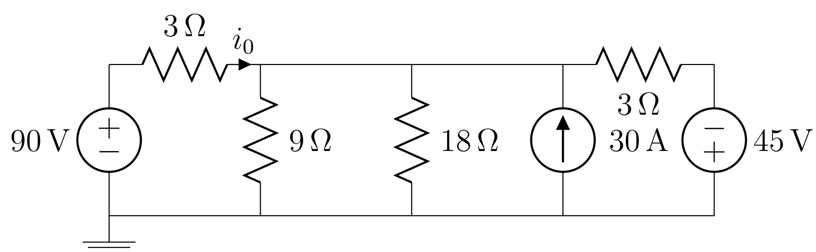


Figure 3.71: Circuit Diagram for Problem 3.38

Answer: *(a) (b) (c) (d) (e)*

Problem 3.39 *Given the circuit in Figure 3.72, (a) how many nodes are there, including ground node? (b) Find the the voltage v at the source. Now let the source be $v = 12V$, find the voltage across 5Ω resistor. (c) by using equivalent resistance technique and (d) using superposition technique.*
Answer: *(a) 5 nodes (b) $v = 24V$ (c) $v_{5\Omega} = 0.1 \times 5 = 0.5V$. (d) Knowing $y = f(x)$ for linear systems, we have $\bar{y} = f(\alpha x) = \alpha f(x) = \alpha y$. Since $1 = f(24)$, we have $y = f(12) = f(\frac{1}{2}24) = \frac{1}{2}f(24) = 0.5V$.*

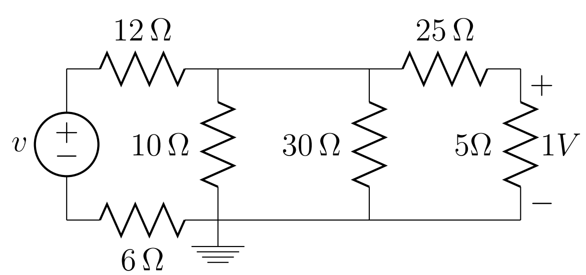


Figure 3.72: Circuit Diagram for Problem 3.39

Problem 3.40 *Determine the $\Delta - Y$ equivalent 3.73. That is, given Delta find Y and vice versa.*

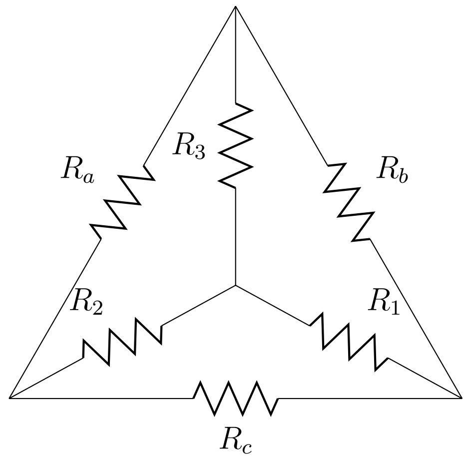


Figure 3.73: Circuit Diagram for Problem 3.40

Answer: *(a)* $R_1 = \frac{R_b R_c}{R_a+R_b+R_c}$, $R_2 = \frac{R_a R_c}{R_a+R_b+R_c}$, $R_3 = \frac{R_a R_b}{R_a+R_b+R_c}$. *(b)* $R_a = \frac{R_1R_2+R_2R_3+R_3R_1}{R_1}$, $R_b = \frac{R_1R_2+R_2R_3+R_3R_1}{R_2}$, $R_c = \frac{R_1R_2+R_2R_3+R_3R_1}{R_3}$.

Problem 3.41 *Find the i_1 in Figure 3.74 where the ground node is not labeled.*
(a) Which method would you use? and why?
(b) Indicate your ground node in your diagram and solve for i_1.

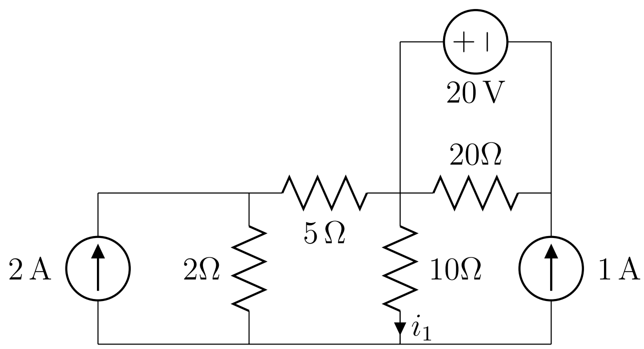


Figure 3.74: Circuit Diagram for Problem 3.41

Answer: $i_1 = 0.647A$.

Problem 3.42 *Find the current, voltage and power for each element in the circuit shown in Figure 3.75 and state whether each is absorbing or delivering energy.*
Answer: $v = 7.5V$, $i_1 = 2.5A$, $i_2 = 7.5A$, $i_3 = 1.75A$, *Resistors: absorbing* $30.25W$, $6.625W$, $30.625W$ *and sources: delivering* $50W$, $17.5W$.

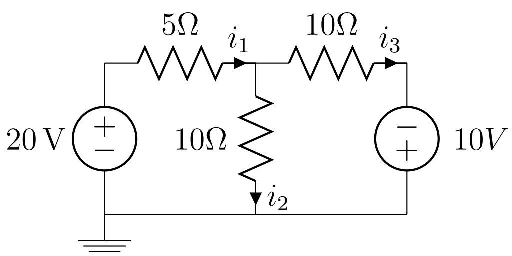


Figure 3.75: Circuit Diagram for Problem 3.42

Problem 3.43 *Given the circuit in Figure 3.76,*
(a) solve for the node voltage v_1 and v_2 shown in the figure.
(b) Find the current i_x.
(c) Find the Thevenin v_{oc} seem from 10Ω resistor.
(d) Find the Thevenin i_{sc} seem from 10Ω resistor.

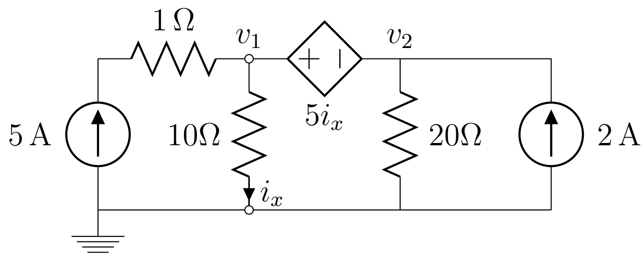


Figure 3.76: Circuit Diagram for Problem 3.43

Answer: *(a) $v_1 = 56V$, $v_2 = 28V$. (b) $i_x = 5.6A$. (c) $v_{oc} = 140V$ (d) $i_{sc} = \frac{28}{3}A$, $R_t = 15\Omega$.*

Problem 3.44 *Given the circuit in Figure 3.77,*
(a) attach a test source at terminal ab to determine the equivalent resistance seen by terminal ab.
(b) Find the Thevenin and Norton equivalent circuit seen by terminal ab and draw the circuit diagram.

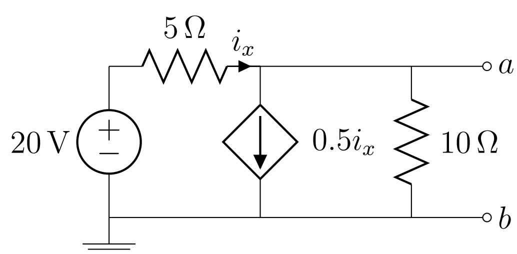


Figure 3.77: Circuit Diagram for Problem 3.44

Answer: *(a) Use a unity voltage source to find $i_{sc} = 0.2A$ and thus $R_t = \frac{1}{0.2} = 5\Omega$. (b) $V_{oc} = 10V$, $I_{sc} = 2A$, $R_t = 5\Omega$.*

Problem 3.45 *Given the circuit in Figure 3.78,*
(a) how many nodes are there, including ground node?
(b) Find the the voltage v at the source.
Now let the source be $v = 12V$, find the voltage across 5Ω resistor.
(c) by using equivalent resistance technique and
(d) using superposition technique.
Answer: *(a) 5 nodes (b) $v = 24V$ (c) $v_{5\Omega} = 0.15 = 0.5V$. (d) Knowing $y = f(x)$ for linear systems, we have $\bar{y} = f(\alpha x) = \alpha f(x) = \alpha y$. Since $1 = f(24)$, we have $y = f(12) = f(\frac{1}{2}24) = \frac{1}{2}f(24) = 0.5V$*

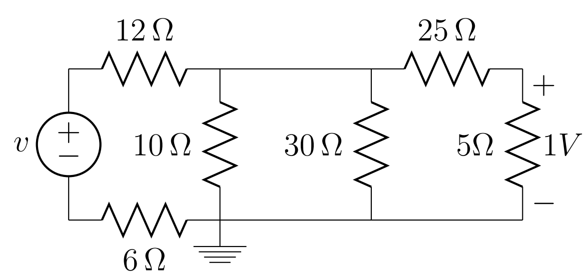


Figure 3.78: Circuit Diagram for Problem 3.45

Chapter 4

AC Circuits

Circuits with sinusoidal sources are a central theme in Electrical Engineering because many important applications are found in real life. For example, the power distributed in a power grid is sent via sinusoidal voltage and current. The cell phones use sinusoidal signals in communications, so are radio stations and TV stations. Thus, understanding how to analyze circuits with sinusoidal sources enables us to know how AC power is distributed to residential areas and to know the time responses of switched systems, frequency responses of circuits subjected to sinusoidal inputs.

4.1 Complex Signals/Exponential Signals

In an AC circuit, all the voltage and current sources are sinusoidal. Thus without loss of generality, it is fair to assume

$$v(t) = V_{\max}\cos(\omega t+\theta) = \sqrt{2}V_{rms}\cos(\omega t+\theta) \tag{4.1}$$

$$i(t) = I_{\max}\cos(\omega t+\phi) = \sqrt{2}I_{rms}\cos(\omega t+\phi) \tag{4.2}$$

where $V_{\max}, I_{\max}$ are the peak value of voltage and current respectively, w is the angular frequency with units of radians per second and θ, ϕ are the phase angles. V_{rms}, I_{rms} are the root-mean-square value of the voltage and current. Here we define the root-mean-square (effective) value of a periodic sinusoidal signal as

$$Y_{rms} = \sqrt{\frac{1}{T}\int_0^T y^2(t)dt} = \frac{Y_{\max}}{\sqrt{2}}, \quad Y = V \text{ or } I.$$

Example 4.1 *Let $v(t) = V_{\max}\sin wt$. Find v_{ave} and v_{rms}.*

$$v_{ave} = \frac{1}{2\pi}\int_0^{2\pi} V_{\max}\sin wt\ dwt = 0$$

$$v_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} V_{\max}^2\sin^2 wt\ dwt = \frac{V_{\max}^2}{2\pi}\int_0^{2\pi}(\frac{1}{2}+\frac{1}{2}\cos 2wt)\ dwt = \frac{V_{\max}^2}{2}$$

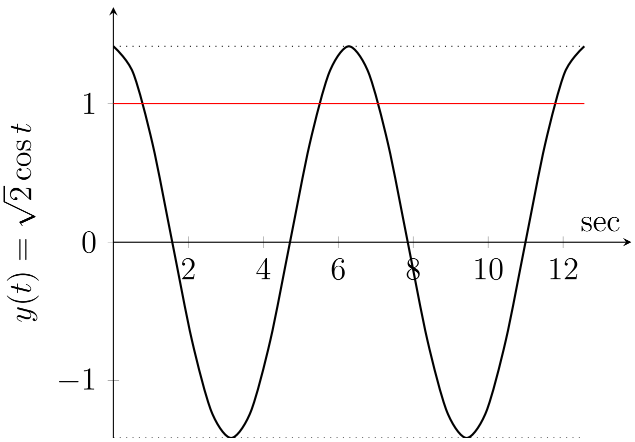


Figure 4.1: Time Trajectory of $\sqrt{2}\cos t, t = [0\ 4\pi]$

Thus for a periodically sinusoidal function the average value is zero, yet its RMS value is $0.707V_{\max}$. There is another example in the problem set for periodic triangular function.

1. Sinusoidal signals are periodic, repeating the same value in each period T. Because the cosine (or sine) function completes one cycle when the angle increases by 2π, we get $wT = 2\pi$, obtaining $w = 2\pi f$ where $f = \frac{1}{T}$ is the frequency in Hertz.

2. Given a sinusoidal voltage waveform (4.1), to find the time where the sinusoidal signal functions reach its peak value, we have

$$\begin{aligned} wt_{max} + \theta(assuming\ in\ degree) &= 0^\circ\ or\ 360^\circ \\ t_{\max} &= \frac{360^\circ - \theta}{2\pi f} = \frac{360^\circ - \theta}{360^\circ} \times T. \end{aligned}$$

3. For uniformity, we express sinusoidal functions by using the cosine function rather than the sine function. The $\sin z$ functions are related by the identity $\sin(z) = \cos(z - 90^\circ)$.

By using Euler's(/oiler/) formula $e^{jx} = \cos x + j\sin x$, we have

$$\begin{aligned} v(t) &= Re[v_e(t)] = Re[V_{\max}\cos(\omega t + \theta) + jV_{\max}\sin(\omega t + \theta)] \\ &= Re[V_{\max}e^{j(\omega t + \theta)}] = Re[\sqrt{2}V_{rms}e^{j(\omega t + \theta)}] \\ i(t) &= Re[i_e(t)] = Re[I_{\max}\cos(\omega t + \phi) + jI_{\max}\sin(\omega t + \phi)] \\ &= Re[I_{\max}e^{j(\omega t + \phi)}] = Re[\sqrt{2}I_{rms}e^{j(\omega t + \phi)}]. \end{aligned}$$

We have the following observations:

1 The real/actual signal can be obtained by taking the Real part of the complex signal/exponential signal. i.e., $v(t) = Re[V_e(t)]$

2 The most important properties of a complex signal is that it reproduces itself when integrates or differentiates.

To see that properties, we investigate each circuit element laws subject to exponential voltage and current.

- Resistors (Ohm's law)

$$v_e(t) = i_e(t)R.$$

- Inductors (Faraday's law)

$$v_e(t) = L\frac{di_e(t)}{dt} = L\frac{d}{dt}(I_{max}e^{j(\omega t+\phi)}) = (j\omega L)I_{max}e^{j(\omega t+\phi)} = j\omega L I_e.$$

The identity shows that an exponential function remains exponential after the derivative operation.

- Capacitors (Henry's law)

$$v_e(t) = \frac{1}{C}\int_{-\infty}^{t} i_e(\tau)d\tau = \frac{1}{C}\int_{-\infty}^{t} I_{max}e^{j(\omega\tau+\phi)}d\tau = (\frac{1}{j\omega C})I_{max}e^{j(\omega t+\phi)} = \frac{1}{j\omega C}i_e.$$

The identity shows that an exponential function remains exponential after the integral operation. Note that the integral of $I_e(t)$ at $-\infty$ is assumed to be zero.

4.2 Impedance Concepts

From previous section, a form of ohm's low was found when complex voltage and current signals are applied to the circuit elements — R, L, and C. However, it is noted that the concept is limited to complex exponential signals only.

$$\begin{aligned} Z_R &= \frac{v_e}{i_e} = \frac{i_e R}{i_e} = R\ \Omega \\ Z_L &= \frac{v_e}{i_e} = \frac{j\omega L i_e}{i_e} = j\omega L\ \Omega \\ Z_C &= \frac{v_e}{i_e} = \frac{\frac{1}{j\omega C}i_e}{i_e} = \frac{1}{j\omega C}\ \Omega. \end{aligned}$$

Note that Z_R, Z_L and Z_C are all in ohm's form, also the general relation between complex voltage and current is $V_e = I_e Z_e$ (ohm's low) for $R, L,$ and C elements. We come to think whether those technique introduced in DC circuits can be used in AC circuits too. To see this, consider a series RLC circuit with AC voltage source given below.

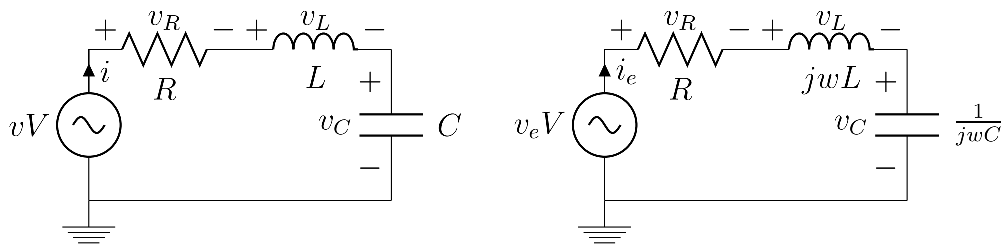


Figure 4.2: Series Circuits (a) Nominal Signal (b) Complex Signal

Applying KVL clockwise yields

$$\begin{aligned} v_e &= v_R + v_L + v_C = i_e R + L\frac{di_e}{dt} + \frac{1}{C}\int_{-\infty}^{t} i_e(\tau)d\tau \\ &= (R + j\omega L + \frac{1}{j\omega C})i_e, \quad \text{for complex/exponential signals.} \end{aligned}$$

The identity shows that when complex signal is used the differential-integral form is reduced to an algebraic form if L is replaced with jwL and C is replaced with $\frac{1}{jwC}$ while R is intact. To see more, consider a parallel RLC circuit with AC current source:

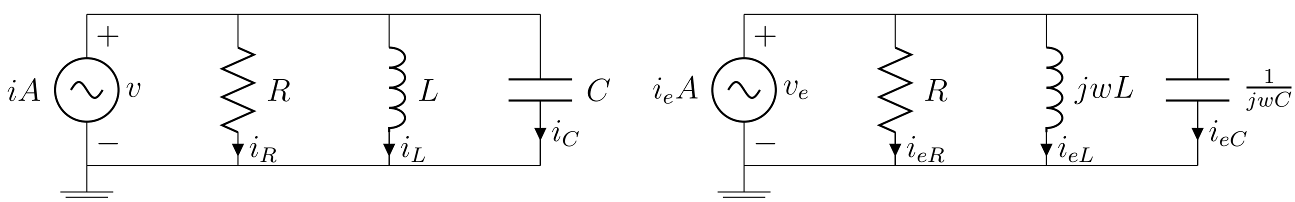


Figure 4.3: Parallel circuits (a) Nominal Signal (b) Complex Signal

Applying KCL at the node on top yields

$$\begin{aligned} i_e &= i_R + i_L + i_C = \frac{v_e}{R} + \frac{1}{L}\int_{-\infty}^{t} v_e(\tau)d\tau + C\frac{dv_e}{dt} \\ &= (\frac{1}{R} + \frac{1}{j\omega L} + j\omega C)v_e, \quad \text{for complex/exponential signals.} \end{aligned}$$

The identity, again, shows that when complex signal is used the differential-integral form is reduced to an algebraic form if L is replaced with jwL and C is replaced with $\frac{1}{jwC}$ while R is intact. The preceding introduction is known as the impedance concept, we define impedance as the ratio of the complex voltage to the complex current, denoted by $\bar{Z}$.

$$\bar{Z} = \frac{V_e(t)}{I_e(t)} = R + jX = Ze^{j\theta_z} = Z\angle\theta_z = Z\cos\theta_z + jZ\sin\theta_z.$$

The reciprocal of impedance is called admittance, denoted by $\bar{Y}$.

$$\bar{Y} = \frac{1}{\bar{Z}} = \frac{1}{R + jX} = \frac{R - jX}{R^2 + X^2} = G + jB.$$

4.3 Phasor Concept

Phasors are complex numbers representing sinusoidal voltages or currents. The magnitude of a phasor equals the peak value and the angle equals the phase angle of the sinusoidal signals written in a cosine form.

$$v(t) = V_{max}\cos(\omega t+\theta) = Re\{V_e(t)\} = Re\{V_{max}e^{j(\omega t+\theta)}\} = Re\{\sqrt{2}V_{rms}e^{j\theta}e^{j\omega t}\}$$
$$i(t) = I_{max}\cos(\omega t+\phi) = Re\{I_e(t)\} = Re\{I_{max}e^{j(\omega t+\phi)}\} = Re\{\sqrt{2}I_{rms}e^{j\phi}e^{j\omega t}\}.$$

where $v(t)$ and $i(t)$ mean time function in cosine form while V_e and I_e stand for time function in exponential/complex form. Note that the $e^{j\omega t}$ term in the braces is the same for all voltage and currents associated with a given source, therefore we define the phasor.

$$\begin{aligned}
\bar{V} &= V_{max}e^{j\theta} = \sqrt{2}V_{rms}e^{j\theta} \quad or \quad V_{rms}\angle\theta \\
\bar{I} &= I_{max}e^{j\phi} = \sqrt{2}I_{max}e^{j\phi} \quad or \quad I_{rms}\angle\phi \\
\bar{Z} &= \frac{v_e(t)}{i_e(t)} = \frac{V_{max}e^{j\theta}e^{j\omega t}}{I_{max}e^{j\phi}e^{j\omega t}} = \frac{\sqrt{2}V_{rms}e^{j\theta}e^{j\omega t}}{\sqrt{2}I_{rms}e^{j\phi}e^{j\omega t}} = \frac{V_{rms}}{I_{rms}}e^{j(\theta-\phi)} = Ze^{j\theta_z} \\
&= \frac{V_{rms}e^{j\theta}}{I_{rms}e^{j\phi}} = \frac{\bar{V}}{\bar{I}} = \frac{V_{rms}\angle\theta}{I_{rms}\angle\phi} = \frac{V_{rms}}{I_{rms}}\angle\theta-\phi = Z\angle\theta_z.
\end{aligned}$$

The definitions can be visualized as a vector of length $V_{\max}$ (or V_{rms}) that rotates counterclockwise in the complex plane with an angular velocity w rad/s. As the vector rotates, its projection on the real axis traces out the voltage as a function of time $v(t)$. This is due to the fact that $v(t) = Re[V_{\max}e^{jwt}]$. Note that utilizing the phasor concept makes $\bar{V}$, $\bar{I}$, and $\bar{Z}$ simply complex constants, not a function of time.

Except for the fact that we use complex computation, the steady-state analysis for AC circuits is virtually the same as that of DC circuits. We, therefore, provide only a few examples to illustrate the technique.

Example 4.2 (Time Expression vs. Phasor Expression)

$$\begin{aligned}
v(t) &= 170\cos(377t-40^\circ)V \longleftrightarrow \bar{V} = 170\angle-40^\circ \\
i(t) &= 10\sin(1000t+20^\circ)A \longleftrightarrow \bar{V} = 10\angle-70^\circ \\
\bar{V} &= 86.3\angle 26^\circ V \longleftrightarrow v(t) = 86.3\cos(\omega t+26^\circ)V.
\end{aligned}$$

It is clear from the example that, in phasor representation, we only keep magnitude and angle infomation and leave $\cos wt$ *in heart.*

□

Example 4.3 (Benefits using Phasor Technique) *Given* $y_1 = 20\cos(\omega t-30^\circ)$ *and* $y_2 = 40\cos(\omega t+60^\circ)$*, find* $y = y_1 + y_2$ *by using (1) trigonometry and (2) phasor concept.*

Solution:

$$
\begin{aligned}
y_1 &= 20\ cos\omega t \cos 30^\circ + 20 \sin \omega t \sin 30^\circ \\
+)y_2 &= 40\ cos\omega t \cos 60^\circ - 40 \sin \omega t \sin 60^\circ \\
--- & \quad ------------------ \\
y &= 37.32 \cos \omega t - 24.64 \sin \omega t \\
&= 44.72(\cos \omega t + 33.43^\circ).
\end{aligned}
$$

$$
\begin{aligned}
\bar{Y} &= \bar{Y}_1 + \bar{Y}_2 = 20\angle -30^\circ + 40\angle 60^\circ \\
&= (17.32 - j10) + (20 + j34.64) \\
&= 37.32 + j24.64 = 44.72\angle 33.43^\circ.
\end{aligned}
$$

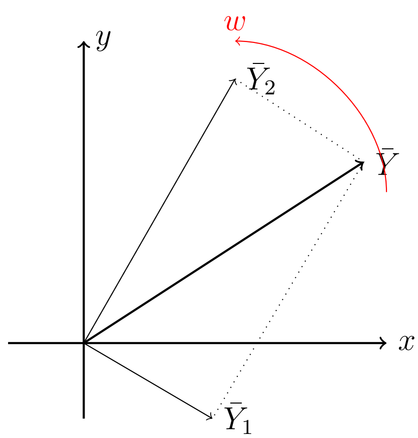


Figure 4.4: Example 4.3, Phasor Diagram

□

Example 4.4 (Differential Approach) *Solve the following circuit problem*
Solution: *Loop current method yields*

$$
V_s = 750 \cdot \sqrt{2} \cos 5000t = iR + \frac{1}{C}\int_0^t i(\tau)d\tau + L\frac{di}{dt}
$$

$$
-750 \cdot 5 \cdot 10^3 \cdot \sqrt{2} \sin 5000t = \frac{32 \cdot 10^{-3}}{1}\frac{d^2 i}{dt} + 90\frac{di}{dt} + \frac{10^6}{5} i. \tag{4.3}
$$

Assume the solution $i(t)$ has the following form

$$
i(t) = A_1 \sin 5000t + A_2 \cos 5000t
$$

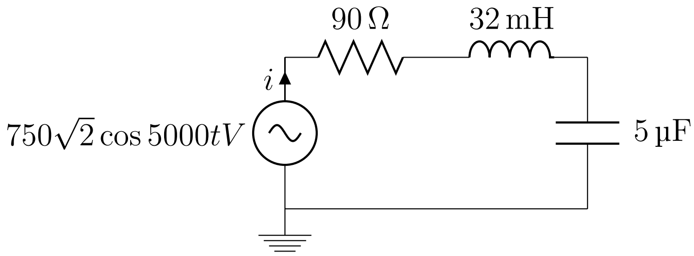


Figure 4.5: Example 4.4(a), Time domain

then we have

$$\begin{aligned}
\frac{di(t)}{dt} &= 5\cdot 10^3 A_1\cos 5000t - 5\cdot 10^3 A_2 \sin 5000t \quad (4.4)\\
\frac{d^2i(t)}{dt^2} &= -25\cdot 10^6 A_1 \sin 5000t - 25\cdot 10^6 A_2\cos 5000t. \quad (4.5)
\end{aligned}$$

Substituting (4.4) and (4.5) into (4.3) and equating the coefficients of same order generates

$$\begin{aligned}
-120A_1 - 90A_2 &= -750\sqrt{2}\\
90A_1 - 120A_2 &= 0
\end{aligned}$$

which leads to $A_1 = 4\sqrt{2}$, $A_2 = 3\sqrt{2}$. *Thus, the solution current is*

$$i(t) = 4\sqrt{2}\sin 5000t + 3\sqrt{2}\cos 5000t = 5\sqrt{2}\cos(5000t - 53.13^\circ)A. \quad (4.6)$$

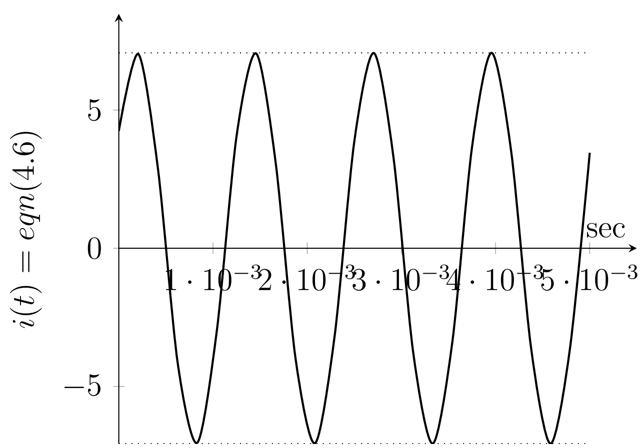


Figure 4.6: Time Response $i(t)$ for Example 4.4

Lets try phasor domain approach

$$\begin{aligned}
\bar{Z}(j\omega) &= R + j\omega L - j\frac{1}{\omega C} = 90 + j(160 - 40) = 90 + j120 = 150\angle 53.13^\circ\\
\bar{I} &= \frac{\bar{V}}{\bar{Z}} = \frac{750\angle 0^\circ}{150\angle 53.13^\circ} = 5\angle -53.13^\circ A.
\end{aligned}$$

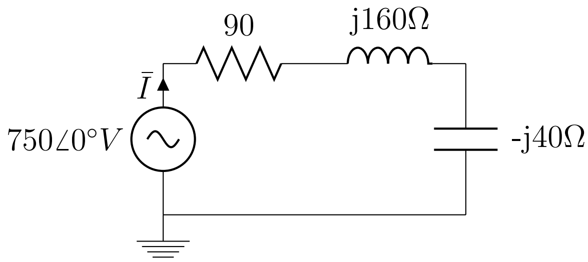


Figure 4.7: Example 4.4(b), Phasor Domain

Thus, $i(t) = 5 \cdot \sqrt{2}\cos(5000t - 53.13°)A$.

□

Example 4.5 *Solve the following circuit using impedance concept.*[1]

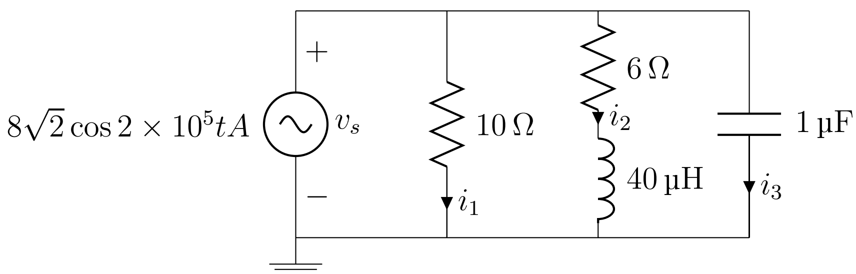


Figure 4.8: Example 4.5(a), Time Domain

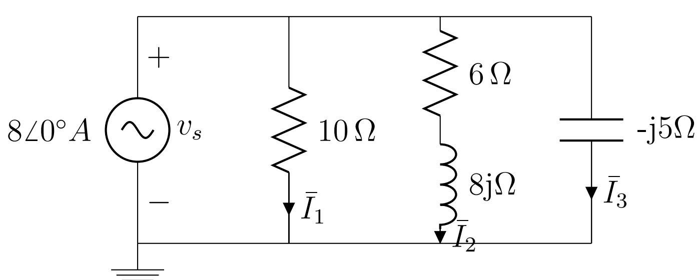


Figure 4.9: Example 4.5(b), Phasor Domain

Solution: *Applying KCL at the top node yields*

$$8\angle 0° = \frac{\bar{V}}{10} + \frac{\bar{V}}{6+j8} + \frac{\bar{V}}{-j5}$$

[1]Follow the notions in the previous example, find the ODE and solve the problem using PSpice.

giving

$$\bar{V} = (8\angle 0°)/(\frac{1}{10} + \frac{1}{6+j8} + \frac{1}{-j5}) = 40\angle -36.87°V, \quad 40\sqrt{2}\cos(2\times 10^5 t - 36.87°)V.$$

Therefore, we have

$$\begin{aligned}
\bar{I}_1 &= \frac{\bar{V}}{10} = 4\angle -36.87°A, \quad i_1 = 4\sqrt{2}\cos(2\times 10^5 t - 36.87°)A \\
\bar{I}_2 &= \frac{\bar{V}}{6+j8} = 4\angle -90°A^2, \quad i_2 = 4\sqrt{2}\cos(2\times 10^5 t - 90°)A \\
\bar{I}_3 &= \frac{\bar{V}}{-j5} = 8\angle 53.13°A^3, \quad i_3 = 8\sqrt{2}\cos(2\times 10^5 t - 53.13°)A.
\end{aligned}$$

□

Example 4.6 *[1, Steady-State Analysis, Page 202] Solve $\bar{V}_1$ and $\bar{V}_2$ for the following circuits*[4].

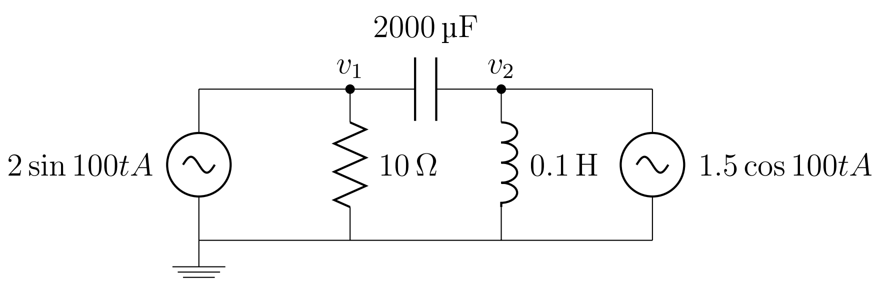


Figure 4.10: Example 4.6(a)

Solutions: *Applying KCL at node 1 and 2, we have*

$$\begin{aligned}
2\angle -90° &= \frac{\bar{V}_1}{10} + \frac{\bar{V}_1 - \bar{V}_2}{-j5} \\
1.5\angle 0° &= \frac{\bar{V}_2}{j10} + \frac{\bar{V}_2 - \bar{V}_1}{-j5}
\end{aligned}$$

Solving, we have $\bar{V}_1 = 16.12\angle 29.74°$ *and* $\bar{V}_2 = 28.01\angle 2.04°$.

To briefly recap the concept learned up to now, we have Table 4.1 listed below. Bear in mind the the notations we used so far are $\bar{V}, \bar{I}, \bar{Z}$, representing a complex constant.

[3] Try verifying $\bar{I}_2$ via Pspice.
[3] Try verifying $\bar{I}_3$ via Pspice.
[4] Verifying the results using loop-current method and find $\bar{V}_1$ and $\bar{V}_2$ via PSpice.

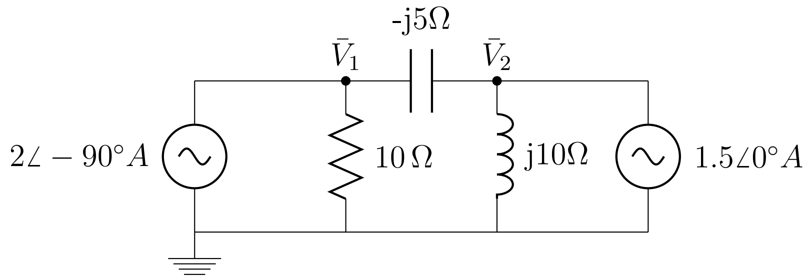


Figure 4.11: Example 4.6(b)

	$R, jwL, \frac{1}{jwC}$		
Complex input	$\rightarrow$ Impedance, Algebraic eqn	$\rightarrow$	Complex output
$\Uparrow$ Phasor $M\angle\theta$	$R, jwL, \frac{1}{jwC}$		$\Downarrow e^{j(wt+\theta)}$
Exponential Input	$\rightarrow$ Impedance, Algebraic eqn	$\rightarrow$	Exponential Output
$\Uparrow$ Euler $e^{j(wt+\theta)}$			$\Downarrow Re(e^{j(wt+\theta)})$
Sinusoidal Input	$\rightarrow$ Mathematic Differential eqn.	$\rightarrow$	Sinusoidal Output

Table 4.1: Sinusoidal Signals to Complex Signals

4.4 Power in AC

Consider a circuit where a voltage source is applied to a series of RLC network. Let the voltage be $v(t) = V_{max}\cos(wt)$ whose phasor representation is $\bar{V} = V_{max}\angle 0°$ and the equivalent impendence is $\bar{Z} = R + jX = Z\angle\phi$. By ohm's law, we have

$$\bar{I} = \frac{\bar{V}}{\bar{Z}} = \frac{V_{max}\angle 0°}{Z\angle\phi} = I_{max}\angle-\phi$$

where $I_{max} = \frac{V_{max}}{Z}$. The equation above involves $\bar{Z}$ which is a combination of three different circuit elements. Before proceeding to a general load, it is instructive to consider the following three scenarios:

- A purely resistive load: For this load, $\bar{Z} = R\angle 0°$ means $\phi = 0°$ and we have

$$\begin{aligned} v(t) &= V_{max}\cos(wt) \\ i(t) &= I_{max}\cos(wt) \\ p(t) &= v(t)i(t) = V_{max}I_{max}\cos^2(wt) \end{aligned}$$

  Notice that the current is in phase with the voltage[5]. The analysis shows that the power is positive at all times. We therefore conclude that the energy flows in the direction from source to load. The resistance is always consuming power.

[5]Please explain why.

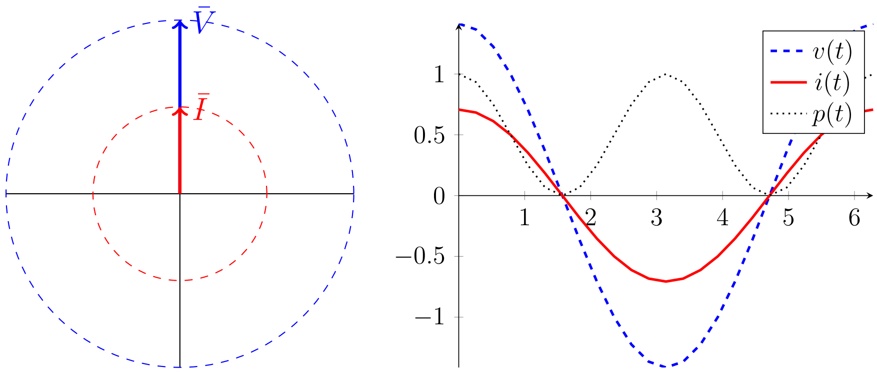


Figure 4.12: Power for Purely Resistive Network

- A purely inductive load: For this load, $\bar{Z} = wL\angle 90°$ means $\phi = 90°$ and we have

$$
\begin{aligned}
v(t) &= V_{max}\cos(wt)\text{[6]} \\
i(t) &= \frac{V_{max}}{wL}\cos(wt - 90°) = I_{max}\sin(wt) \\
p(t) &= v(t)i(t) = V_{max}I_{max}\cos(wt)\sin(wt) = \frac{V_{max}I_{max}}{2}\sin(2wt) \\
&= V_{rms}I_{rms}\sin(2wt)
\end{aligned}
$$

Notice that the current lags the voltage by 90°[7]. The analysis shows that the power is changing in sign for every half cycle. Half of the time the power is positive, showing that the source is delivering the power to the inductance, while the other half of the time the power is negative, showing that the inductance is returning the power to the source. We therefore conclude that the average energy power is zero, a protruding feature for reactive power.

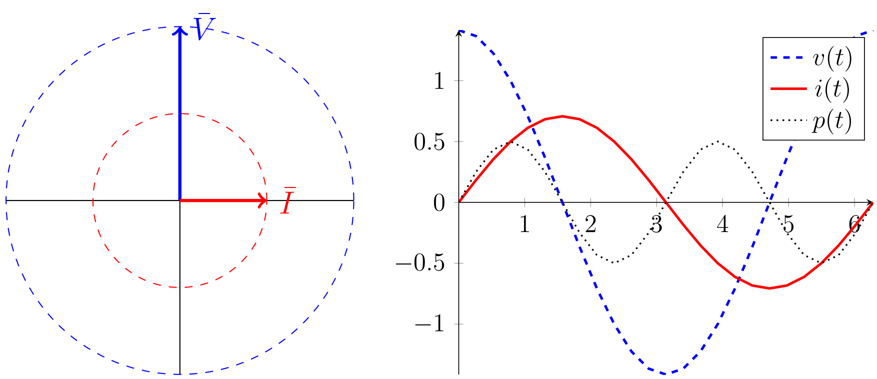


Figure 4.13: Power for Purely Inductive Network

[6]Find the voltage, current and power versus time for a purely inductive load via PSpice.
[7]Please explain why.

- A purely capacitive load: For this load, $\bar{Z} = \frac{1}{wC}\angle -90°$means $\phi = -90°$, and we have

$$\begin{aligned} v(t) &= V_{max}\cos(wt) \\ i(t) &= V_{max}wC\cos(wt+90°) = -I_{max}\sin(wt) \\ p(t) &= v(t)i(t) = -V_{max}I_{max}\cos(wt)\sin(wt) = -\frac{V_{max}I_{max}}{2}\sin(2wt) \\ &= -V_{rms}I_{rms}\sin(2wt) \end{aligned}$$

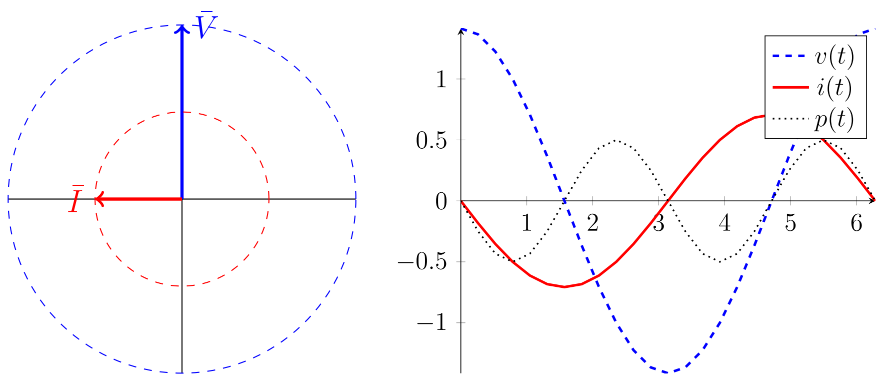


Figure 4.14: Power for Purely Capacitive Network

Notice that the current leads the voltage by 90°[8]. The analysis shows that the power is changing in sign for every half cycle. Half of the time the power is negative, showing that the source is receiving the power from the capacitance, while the other half of the time the power is positive, showing that the capacitance is receiving the power from the source. We therefore conclude that the average energy power is zero, a protruding feature for reactive power. However, notice that reactive power is negative for a capacitance $(\frac{1}{jwC})$and positive for an inductance(jwL). If a load has both inductance and capacitance with equal magnitude of reactive power, the reactive power cancels.

- A general load with all three components: Now consider a general load where the ϕ can be any value from $-90°$ to $+90°$. It is worth noting that

1. for resistive load, $\bar{I}_R = I_{max}\angle 0°$ lags and $\phi = 0$, thus

2. for inductive load, $\bar{I}_L = I_{max}\angle -90°$ lags and $\phi > 0$, thus

3. for capacitive load, $\bar{I}_C = I_{max}\angle 90°$ lags and $\phi < 0$, thus

[7]Find the voltage, current and power versus time for a purely capacitive load via PSpice.
[8]Please explain why.

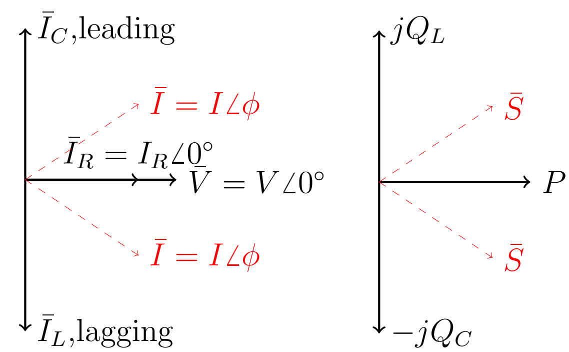


Figure 4.15: $\bar{V}$-$\bar{I}$ and Q_L-Q_C Phasor Diagram, Assuming $\theta = 0°$

We should be aware that $\bar{V} - \bar{I}$ and $Q_L - Q_C$ are all phasor representations, but with slightly different notions. don't be confused.

In this general case, we simply let the phase angle of current ϕ and the phase of the voltage θ has a nonzero value for generosity. The general case is displayed in the next subsection.

4.4.1 Instantaneous power

Assume the alternating voltage and current have the form stated in (4.1)-(4.2). The instantaneous power could be obtained by $p(t) = v(t)i(t)$. Thus

$$\begin{aligned}
p(t) &= V_{\max}\cos(wt+\theta)I_{\max}\cos(wt+\phi) \\
&= \frac{V_{\max}I_{\max}}{2}\cos(\theta-\phi) + \frac{V_{\max}I_{\max}}{2}\cos(2wt+\theta+\phi) \\
&= V_{rms}I_{rms}\cos(\theta-\phi) + V_{rms}I_{rms}\cos(2wt+\theta+\phi) \\
&= V_{rms}I_{rms}\cos(\theta-\phi)\{1+\cos(2wt+2\phi)\} + V_{rms}I_{rms}\sin(\theta-\phi)\sin(2wt+2\phi)
\end{aligned}$$

Notice that the terms involving sinusoidal functions $\cos(2wt)$ and $\sin(2wt)$ have average values of zero. Thus instantaneous power is seldom used for copulations but average power is.

4.4.2 Average real power

$$P_{ave} = \frac{1}{2\pi}\int_0^{2\pi} p(\tau)\tau = V_{rms}I_{rms}\cos(\theta-\phi)\ W$$

Its units are watts (W).

4.4.3 Average reactive power

$$Q_{ave} = \frac{1}{2\pi}\int_0^{2\pi} p(\tau)\tau = 0\ VAR.$$

Its physical units are watts. However, to emphasize the fact that Q does not represent real power, its units are usually given as Volt-Amperes Reactive (VAR).

4.4.4 Complex power

A convenient way to compute the real average power and reactive power is through the complex power computation and it is illustrated below.

$$\begin{aligned} \bar{S} &= P + jQ = \bar{V}\bar{I}^* = (V_{rms}\angle\theta)(I_{rms}\angle\phi)^* = V_{rms}I_{rms}\angle(\theta-\phi) \\ &= V_{rms}I_{rms}\cos(\theta-\phi) + jV_{rms}I_{rms}\sin(\theta-\phi). \end{aligned}$$

Since $\bar{V} = \bar{I}\bar{Z}$ (Ohm's law in AC), we have

$$\begin{aligned} \bar{S} &= P + jQ = \bar{V}\bar{I}^* = (\bar{I}\bar{Z})\bar{I}^* = I_{rms}^2(R+jX) = I_{rms}^2R + jI_{rms}^2X \\ &= \bar{V}(\frac{\bar{V}}{\bar{Z}})^\star = \frac{V_{rms}^2}{R-jX} = \frac{V_{rms}^2R}{Z^2} + j\frac{V_{rms}^2X}{Z^2}. \end{aligned}$$

Notice that the formula is based on RMS value. It is fine to use maximum value instead[9].

4.4.5 Apparent power

Apparent power is defined as the product of the effective voltage and effective current, Therefore

$$Apparent\ power = V_{rms}I_{rms} = \frac{1}{2}V_{max}I_{max}$$

its units are volt-amperes (VA).

4.4.6 Power triangle

The relationships between real power P, reactive power Q, apparent power $V_{rms}I_{rms}$ and the power angle $\theta_z = \theta - \phi$ can be represented by power triangle shown in Figure 4.16.
where

$$\begin{aligned} P &= V_{rms}I_{rms}\cos(\theta-\phi) = I_{rms}^2R = \frac{V_{rms}^2R}{Z^2} \\ Q &= V_{rms}I_{rms}\sin(\theta-\phi) = I_{rms}^2X = \frac{V_{rms}^2X}{Z^2} \\ \theta_z &= \theta - \phi = cos^{-1}pf \end{aligned}$$

and the angle $\theta_z = \theta - \phi$ is called the power angle (a.k.a. the phase of impedance) and is taken as the phase of the voltage θ minus the phase of the current ϕ due to the Ohm's law. It is common to take the voltage as reference and state whether the current leads (capacitive load $-j(1/wC)$) or lags (inductive load jwL). More on leading and lagging current will be discussed in what follows.

[9] How do you find the formula?

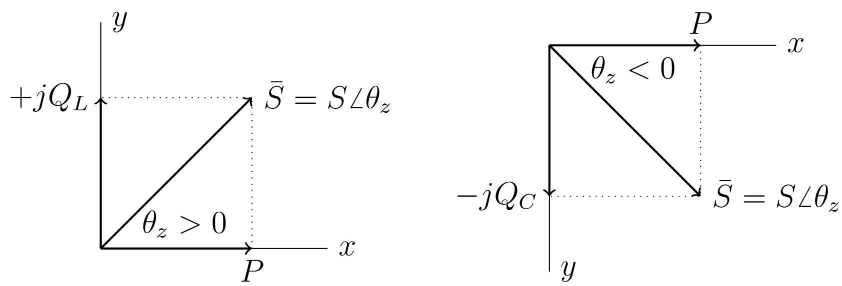


Figure 4.16: Power Triangle

4.4.7 Leading/Lagging power factor

We know the following facts for steady-state analysis: Ohm's law is applicable $\bar{V} = \bar{I}\bar{Z}$, and the impedance is a complex number $\bar{Z} = R + jX$, where $jX = j\omega L$, $\frac{1}{j\omega C}$ or combinations of both. To ease the presentation, we consider the following two cases:
(A) A purely capacitive network whose impedance law $\bar{V} = \bar{I}\bar{Z}$ relationship is described by

$$\bar{V} = \bar{I} \cdot \frac{1}{j\omega C} \Leftrightarrow \bar{I} = \bar{V}(j\omega C) = (V_{rms}\angle\theta)(\omega C\angle 90^\circ) = V_{rms}\omega C\angle\theta + 90^\circ,$$

The computation shows that current leads voltage by 90°, meaning leading current.
(B) A purely inductive network, which means

$$\bar{V} = \bar{I} \cdot j\omega L \Leftrightarrow \bar{I} = \bar{V}(\frac{1}{j\omega L}) = (V_{rms}\angle\theta)(\frac{1}{\omega L}\angle - 90^\circ) = \frac{V_{rms}}{\omega L}\angle - 90^\circ + \theta$$

The computation shows that current lags behind voltage by 90°, meaning lagging current. A $\bar{V} - \bar{I}$ phasor diagram is shown in Figure 4.17.

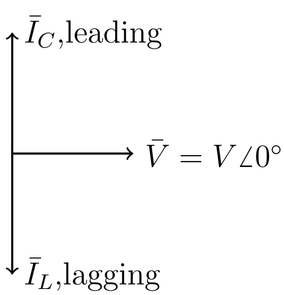


Figure 4.17: $\bar{V}$-$\bar{I}$ Phasor Diagram, Assuming $\theta = 0^\circ$

What happens when $\bar{Z}$ is not purely capacitive or inductive? Well the angle between $\bar{V}$ and $\bar{I}$ will not be exactly $\pm 90^\circ$ but less than 90° for leading current and larger than -90° for lagging current.

However, to draw the power triangle, due to complex conjugate operation is applied, the angle reversed. To see this, we have

For a purely capacitive network

Applying apparent power formula, we have the following derivations

$$\begin{aligned}\bar{S} &= \bar{V}\bar{I}^* = (V\angle\theta)(I\angle\phi)^* = (V_{rms}\angle\theta)(V_{rms}\omega C\angle-\theta-90°) = V_{rms}^2\omega C\angle-90° \\ &= -jV_{rms}^2 wC.\end{aligned}$$

and the power diagram is shown in Figure 4.18.

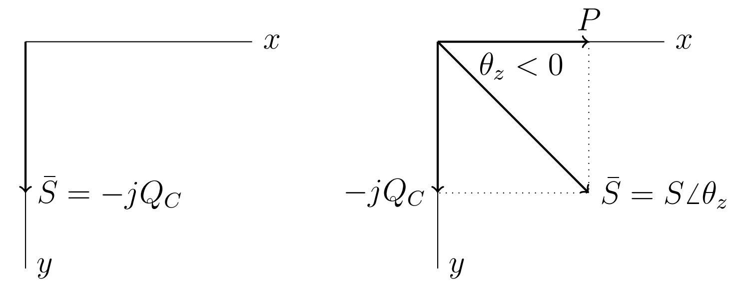


Figure 4.18: Power Phasor Diagram, $\bar{S}$=$P - jQ_C$, Capacitive Load, Leading

For a purely inductive network

Applying apparent power formula, we have the following derivations

$$\begin{aligned}\bar{S} &= \bar{V}\bar{I}^* = (V\angle\theta)(I\angle\phi)^* = (V_{rms}\angle\theta)(\frac{V_{rms}}{\omega L}\angle 90° - \theta) = \frac{V_{rms}^2}{\omega L}\angle 90° \\ &= j\frac{V_{rms}^2}{wL}.\end{aligned}$$

and the power diagram is shown in Figure 4.19.

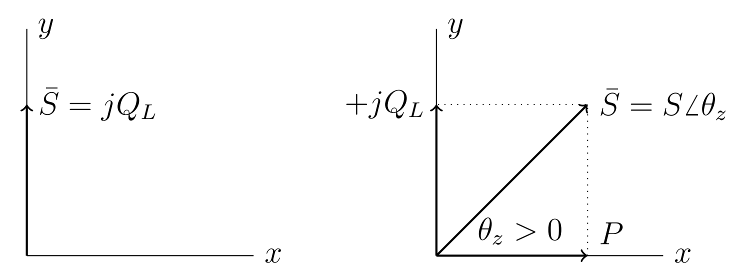


Figure 4.19: Power Phasor Diagram, $\bar{S}$=$P + jQ_L$, Inductive Load, Lagging

Last but not the least, another quick trick is to apply the formula $\theta_z = \theta - \phi$. For a leading current ($\phi > \theta$) we have $\theta_z < 0$ and $\theta_z > 0$ for a lagging current ($\phi < \theta$). There you have it: an upper power triangle at the first quadrant for lagging power factor and a lower triangle at the forth quadrant for leading power factor (Please refer to Figure 4.16).

Example 4.7 *Consider the following circuit where power information to load A:10KVA, pf=0.5, leading and load B: 5kW, pf=0.7, lagging information are given. Find the current* $\bar{I}$.

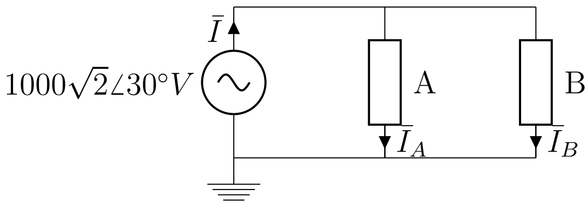


Figure 4.20: Example 4.7

Solution: *Summarize the information in the form of power triangle.*
Load A: the power triangle is drawn for 10KVA, pf=0.5 leading. Noting that the angle θ_A *represents*

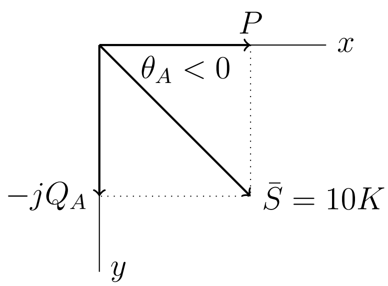


Figure 4.21: Power Triangle for Load A

difference between the voltage angle and the current angle $(\theta - \phi)$. *With that, we have the following calculations.*

$$\begin{aligned}
0.5 &= \cos\theta_A \Longrightarrow \theta_A = -60° = \theta - \phi \\
P_A &= 10 \cdot \cos\theta_A = 5KW \\
Q_A &= (10^2 - 5^2)^{\frac{1}{2}} = -8.66KVAR \\
\theta - \phi &= -60° \rightarrow \ 30 - \phi = -60° \rightarrow \phi = 90° \\
5KV &= VI_A \cos 60° = 1000 I_A \cdot 0.5 \rightarrow I_A = 10000/1000, \ \textit{thus} \ \bar{I}_A = 10\angle 90°.
\end{aligned}$$

Similarly, for load B, we have the power triangle drawn for 5KW, pf=0.7 lagging. and the related information is deciphered as displayed below.

$$\begin{aligned}
0.7 &= \cos\theta_B \\
\theta_B &= \theta - \phi = 45.57° \\
Q_B &= 5\tan\theta_B = 5.101KVAR \\
\theta - \phi &= +45.57° \rightarrow 30° - \phi = 45.57° \rightarrow \phi = -15.57° \\
5KW &= VI_B \cos 45.57° = VI_B \cdot 0.7 \rightarrow I_B = 7143/1000, \ \textit{thus} \ \bar{I}_B = 7.143\angle - 15.57°
\end{aligned}$$

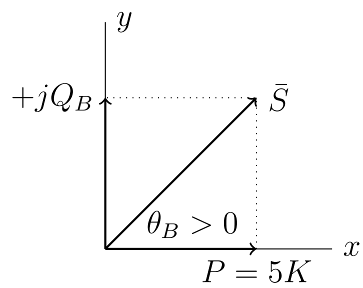


Figure 4.22: Power Triangle for Load B

To find the total energy distributions, we have for sources

$$
\begin{aligned}
Q_{total} &= -8.66K + 5.101K = -3.559KVAR \\
P_{total} &= 5K + 5K = 10KW \\
\theta_z &= \tan^{-1}(Q/P) = -19.59^\circ = \theta - \phi \\
S_{total} &= (P^2 + Q^2)^{\frac{1}{2}} = 10.61KVA \rightarrow I = 10610/1000, \ \textit{thus}\ \bar{I}_{total} = 10.61\angle 49.59^\circ. \\
&= \bar{I}_A + \bar{I}_B = j10 + 6.881 - j1.917 = 6.881 + j8.0883
\end{aligned}
$$

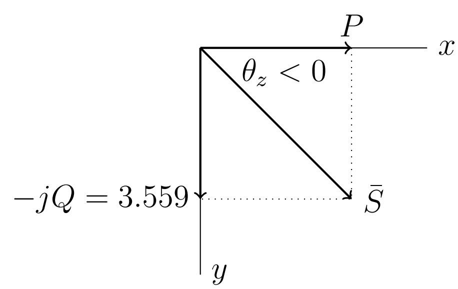


Figure 4.23: Power Triangle for the Overall Circuit

4.4.8 Maximum power transfer

Facing the problem of finding maximum power transferred from source to a load, we need to adjust the load impedance Z_l so that the power is absorbed by Z_l and is not wasted into heat in the transmission line. To this end, we use techniques learned from Calculus to find the maximum power transfer. Consider the following Thevenin equivalent circuit.

$$\bar{I} = \frac{\bar{V}_s}{\bar{Z}_s + \bar{Z}_l} = \frac{V_s \angle \theta_s}{(R_s + R_l) + j(X_s + X_l)}$$

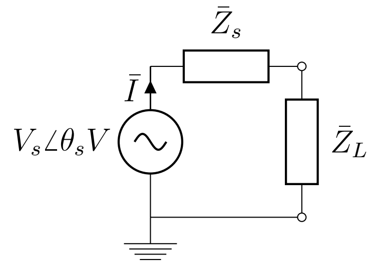


Figure 4.24: Maximum Power Transfer

Obviously, the magnitude of $\bar{I}$ is

$$I = \frac{V_s}{\sqrt{(R_s + R_l)^2 + (X_s + X_l)^2}}.$$

Here the angle information is insignificant due to the fact that $P = I^2R$, thus

$$P_l = I^2 R_l = \frac{V_s^2 R_l}{(R_s + R_l)^2 + (X_s + X_l)^2}.$$

To maximize P_l, we differentiate P_l with respect to R_l and X_l, which leads to

$$\frac{\partial P_l}{\partial X_L} = 0 \Rightarrow X_l = -X_s$$
$$\frac{\partial P_l}{\partial R_L} = 0 \Rightarrow R_l = R_s.$$

which implies that

$$\bar{Z}_l = R_l + jX_l = R_s - jX_s = \bar{Z}_s^*.$$

This is known as the load is matched to the source. Knowing that, we have maximum power transfer as below.

$$\begin{aligned} P_l = I^2 R_l &= \frac{V_s^2 R_l}{(2R_s)^2} \\ &= \frac{V_{s,rms}^2}{4R_s} \\ &= \frac{V_{s,max}^2}{8R_s} \end{aligned}$$

□

The derivations are based on Thevenin model, implying that whenever maximum power is sought, we convert the underlying circuit into Thevenin equivalent first.

For resistive network, the maximum power transfer occurs at the Load resistance equals to Thevenin resistance. This is shown by the following example.

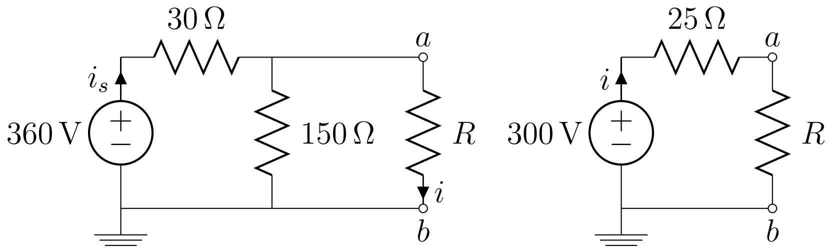


Figure 4.25: Example 4.8

Example 4.8 (Maximum power for DC network) *Given the circuit diagram below, find maximum power transferred.*
Solution: *Find its equivalent Thevenin circuit. To find the Thevenin resistance is to zero the voltage source and compute the equivalent resistance seen from the load side (i.e., terminal ab) which is a parallel structure.*

$$R_T = 30//150 = \frac{30 \cdot 150}{180} = 25\Omega \Rightarrow R_l = 25\Omega$$

To find the Thevenin open voltage, we remove the R and compute the voltage at 150Ω which is readily seen by a voltage divider.

$$V_T = \frac{360}{30+150} \cdot 150 = 300V$$

Lastly, we find

$$P = I^2 R = (\frac{300}{50})^2 \cdot 25 = 900W$$

□

PSpiceLab 4.1 (Maximum Power Transfer) *With the example above, use PSpice DC Sweep and part PARAMETER to verify the maximum power transfer function.*
Objectives: Lean how a circuit parameter can be changed over a certain range.
PreLab: $P = VI = I^2R = \frac{v^2}{R}$ *is a quadratic form and its maximum occurs at extremes.*
Lab: Follow the steps to see the result as expected.
PostLab: How to find the maximum power transfer for the AC case?

□

Example 4.9 (Maximum power transfer for AC circuit) *Given the following AC circuit in impedance, find its maximum power transferred.*
Solution: *Again, based on the derivations, we need to find Thevenin circuit, then find the conjugate of* Z_{line}*. To this end, we have*

$$\bar{V}_T \quad = \quad \frac{16\angle 0^\circ}{4-j3}(-j6) = 19.2\angle -53.13^\circ$$

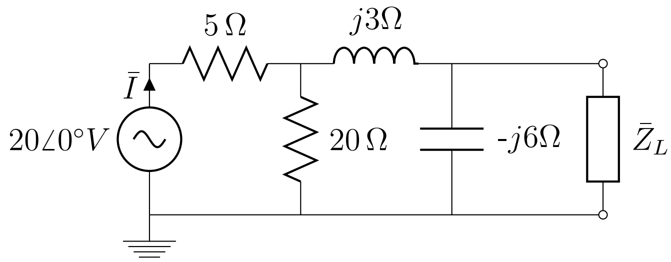


Figure 4.26: Example 4.9(a)

$$
\begin{aligned}
\bar{Z}_T &= (4+j3)//(-j6) = \frac{(4+j3)(-j6)}{4-j3} = 5.76 - j1.68\Omega \\
P_L &= I^2 R_L = (\frac{19.2}{2\times 5.76})^2 \times 5.76 = 16W - \textit{average power}
\end{aligned}
$$

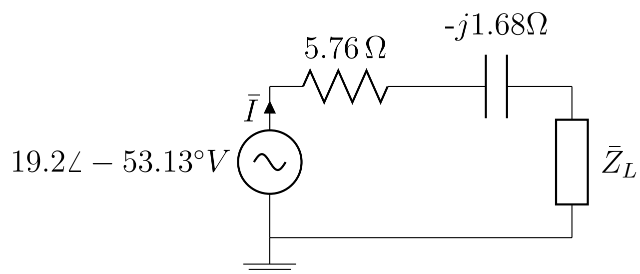


Figure 4.27: Example 4.9(b)

□

Example 4.10 *[1, Page 228, AC Power Calculation] Find the power and reactive power delivered from the source (*$10\sin 1000t$*). Furthermore, find the complex power of all elements.*

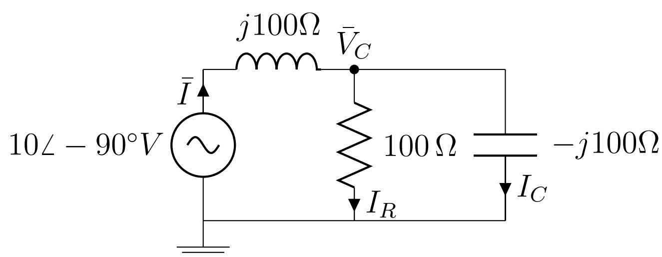


Figure 4.28: Example 4.10

Solutions: *Labeling the node-voltage $\bar{V}_C$ at the top of capacitor and writing KCL give*

$$\begin{aligned} \bar{I} &= \bar{I}_R + \bar{I}_C \\ \frac{10\angle-90^\circ - \bar{V}_C}{j100} &= \frac{\bar{V}_C}{-j100} + \frac{\bar{V}_C}{100} \end{aligned}$$

which gives $\bar{V}_C = -10\angle 0^\circ$; ie, $v_C(t) = -10\cos(1000t)$. To find $\bar{I}$, $\bar{I}_R$, and $\bar{I}_C$, we have

$$\begin{aligned} \bar{I} &= \frac{10\angle-90^\circ + 10\angle 0^\circ}{j100} = 0.1414\angle-135^\circ \\ \bar{I}_R &= \frac{-10\angle 0^\circ}{100} = -0.1\angle 0^\circ = 0.1\angle 180^\circ \\ \bar{I}_C &= \frac{10\angle 0^\circ}{j100} = 0.1\angle-90^\circ \end{aligned}$$

To find the complex power, we have

$$\begin{aligned} \bar{S}_s &= \frac{1}{2}\bar{V}_s\bar{I}^* = \frac{1}{2}(10\angle-90^\circ)(0.1414\angle 135^\circ) = 0.7071\angle 45^\circ = 0.5 + j0.5 = P_s + jQ_s \\ \bar{S}_R &= \frac{1}{2}\bar{V}_R\bar{I}_R^* = \frac{1}{2}(10\angle 180^\circ)(0.1\angle-180^\circ) = 0.5\angle 0^\circ = 0.5 + j0 = P_R \\ \bar{S}_C &= \frac{1}{2}\bar{V}_C\bar{I}_C^* = \frac{1}{2}(10\angle 180^\circ)(0.1\angle 90^\circ) = 0.5\angle 270^\circ = 0 - j0.5 = jQ_C \\ \bar{S}_L &= \frac{1}{2} = I^2(j100) = \frac{1}{2}(0.1414)^2(j100) = j1.0 = jQ_L. \end{aligned}$$

It is easy to verify that $Q_s = Q_L + Q_C$ and $P_s = P_R$.

□

Example 4.11 *[1, Page 225, AC Power Calculation] A voltage source $\bar{V} = 500\sqrt{2}\ \angle 40^\circ$ delivers 5KW to a load with a power factor of 100% (unity power factor). (a) Find the reactive power and the phasor current. (b) Repeat the problem if the power factor is 20% lagging. (c) In which case the wiring be a lower cost? (d) Compute the capacitance that must be placed in parallel with the load to achieve a 90% lagging power factor.*

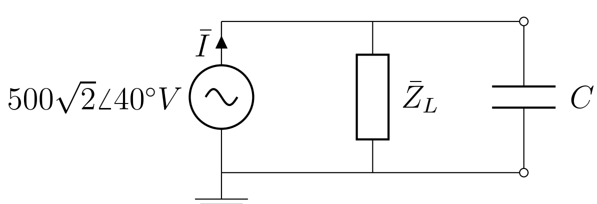


Figure 4.29: Example 4.11

Solutions: *(a) From the power triangle, we know that* $P = VI\cos(\theta - \phi)$*. Thus,*

$$I_{rms} = \frac{P}{V_{rms}\cos(\theta - \phi)} = \frac{5000}{500} = 10A.$$

yielding $\bar{I} = 10\sqrt{2}\angle 40°$ *and* $Q = 0$.

(b) For 20% power factor lagging, we need to find the angle $\theta - \phi = \cos^{-1} 0.2 = 78.46°$*. To find the inductive power* Q_L *which is positive for lagging currents, we have*

$$Q_L = 5000\tan 78.46° = 24.49KVAR.$$

Finally, to find the lagging current, we apply the formula $P = V_{rms}I_{rms}\cos(\theta - \phi)$ *or* $Q = V_{rms}I_{rms}\sin(\theta - \phi)$.

$$I_{rms} = \frac{Q_L}{V_{rms}\sin(\theta - \phi)} = \frac{24490}{500 \times 0.9798} = 50A$$

yielding $\bar{I} = 50\sqrt{2}\angle -38.46°$ *and* $Q = 24.49KVAR$.

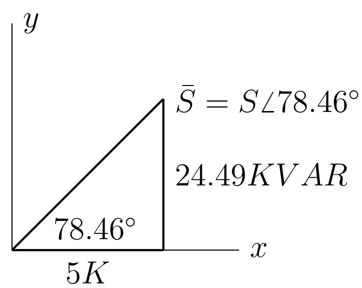


Figure 4.30: 20% Power Factor Lagging

(c) Comparing the results of (a) and (b), it is readily seen that case (b), which has reactive power, causes higher currents in the power distribution system, resulting in more I^2R *losses and therefore, more expensive.*

(d) After adding the capacitor, the real power will still be 5KW and the power angle will becomes

$$\theta_{new} = \cos^{-1} 0.9 = 25.84°$$

which means the new value of the reactive power will be

$$Q_{new} = 5000\tan 25.84° = 2.421KVAR. \quad I_{rms} = \frac{Q_L}{V_{rms}\sin(\theta - \phi)} = \frac{2421}{500 \times 0.4359} = 11.1A.$$

Thus the reactive power of the capacitance must be

$$Q_C = Q_{new} - Q_L = 2421 - 24490 = -22.069KVAR.$$

Since we know that $-jQ_C = \bar{V}_{rms}(\frac{\bar{V}_{rms}}{\frac{1}{jwC}})^{\star} = -jV_{rms}^2 wC$ *for a pure capacitor, we have*

$$C = \frac{Q_C}{V_{rms}^2 2\pi 60} = \frac{22069}{500^2 2 \times 377} = 234\mu F.$$

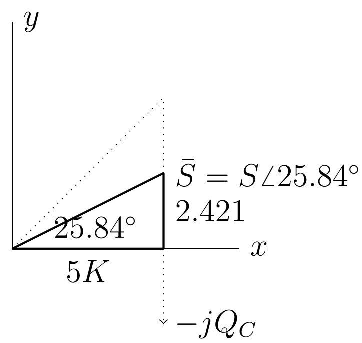


Figure 4.31: Power Factor Correction

DC, Scalar Arithmetic	AC	$\overline{AC}$, Complex Arithmetic
R	R, L, C	R, $j\omega L$, $\frac{1}{j\omega C}$
V	$v(t) = \sqrt{2}V_{rms}\cos(\omega t + \theta)$	$\bar{V} = V_{rms}\angle\theta$
I	$i(t) = \sqrt{2}I_{rms}\cos(\omega t + \phi)$	$\bar{I} = I_{rms}\angle\phi$
	$v_R(t) = i(t)R$	
$V = IR$	$v_L(t) = L\frac{di_L(t)}{dt}$	$\bar{V} = \bar{I}\bar{Z}$
	$i_C(t) = C\frac{dv_C(t)}{dt}$	
KCL, KVL	KCL, KVL	KCL, KVL
Algebraic eqn.	Differential eqn.	Algebraic eqn.
Parallel, series	Yes, but complicated	Parallel, series
Thevenin's	No	Thevenin's
Superposition	Yes, but complicated	Superposition
$P = VI$	$p(t) = v(t)i(t)$	$\bar{S} = \bar{V}\bar{I}^* = P + jQ$

Table 4.2: Comparison between DC and AC

□

Although the steady-state solution of an AC circuit is solved using phasor and impedance notions. This technique can be viewed as a generalized DC scheme. The following table demonstrates this fact. Notice the similarity between the first and the third column. The first column involves only real number, algebraic computation in R, whilst the third column requires complex number, algebraic computation in C.

4.5 Recap

In this chapter, we have gained knowledge of
• The difference between DC and AC circuits.
• To take care of the differentiation and integration, complex signals, impedance and phasor are introduced which make computation a lot easier.
• Conversion from time domain expressions to phasor domain expressions and vice versa. It is a computation involving complex numbers, not a scalar computation anymore.
• The notion of lagging current and leading current.
• Power concept is more involved than the DC power, yet there are related. Power triangle is an important tool to connect all power terminologies.

4.6 Problems

Phasor

Problem 4.1 *Consider the circuit shown in Figure 4.32. Find the phasor for i_s, v, i_R, i_L and i_C. Compare the peak value of $i_L(t)$ with the peak value of $i_s(t)$. Do you find the answer surprising? Explain please.*

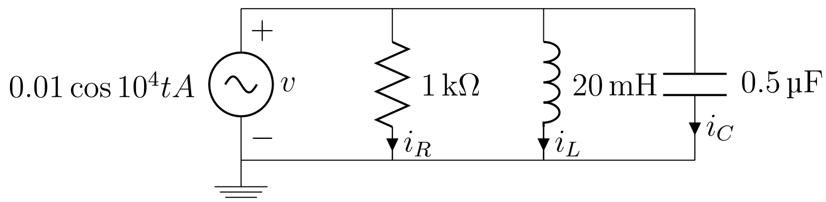


Figure 4.32: Circuit Diagram for Problem 4.1

Answer: $\bar{I}_s = 10\angle 0° mA$, $\bar{V} = 10\angle 0° V$, $\bar{I}_R = 10\angle 0° mA$, $\bar{I}_L = 50\angle -90° mA$, $\bar{I}_C = 50\angle +90° mA$. *The peak of $i_L(t)$ is five times larger than $i_s(t)$. This is reasonable because $\bar{I}_L + \bar{I}_C = 0$.*

Problem 4.2 *Find the phasor for the voltage and the currents for the circuit shown in Figure 4.33. Construct a phasor diagram showing i_s, v, i_R, i_L and i_C. What is the phase relationship between i_s and v?*

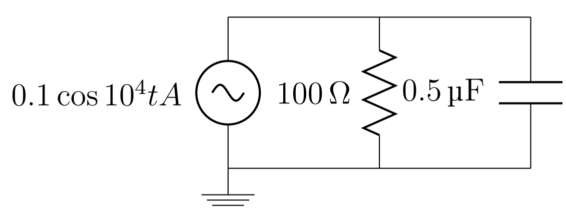


Figure 4.33: Circuit Diagram for Problem 4.2

Answer: $\bar{I}_s = 100\angle 0°$ *mA*, $\bar{V} = 8.944\angle -26.56°$ *V*, $\bar{I}_R = 89.44\angle -26.56°$ *mA*, $\bar{I}_C = 44.72\angle 63.44°$ *mA*, $\bar{V}$ *lags* $\bar{I}_s$ *by* $26.56°$.

Problem 4.3 *Find the voltage $v_1(t)$ and $v_2(t)$ in steady state for the circuit Figure 4.34. (you need to solve the simultaneous equation)*
Answer: $v_1 = 16.1\angle 29.7° V$, $v_2 = 28\angle 1° V$.

Problem 4.4 *Consider the circuit of Figure 4.35 (a) Find $i(t)$. (b) Construct a phasor diagram showing all three voltages and current. (c) What is the phase relationship between $v_s(t)$ and $i(t)$?*
Answer: *(a)* $i(t) = 0.0283\cos(500t - 135°)$ *(b)* $\bar{V}_R = 7.07\angle -135°$, $\bar{V}_L = 7.07\angle -45°$. *(c)* $i(t)$ *lags* $v_s(t)$ *by* $45°$.

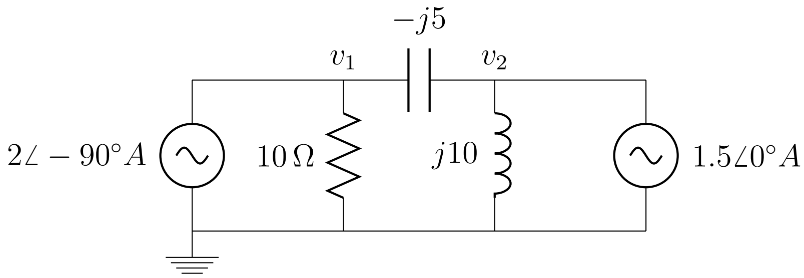


Figure 4.34: Circuit Diagram for Problem 4.3

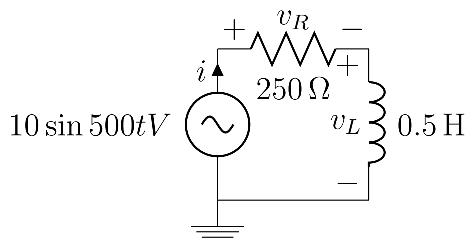


Figure 4.35: Circuit Diagram for Problem 4.4

Thevenin/Norton equivalents

Problem 4.5 *Find the Thevenin impedance, Thevenin voltage, Norton current and draw the Thevenin equivalent circuit for the circuit shown in Figure 4.36*

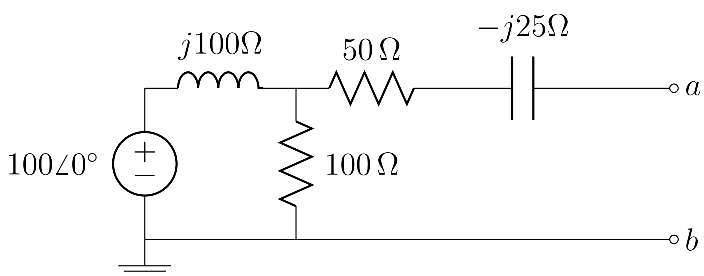


Figure 4.36: Circuit Diagram for Problem 4.5

Answer: $\bar{Z}_t = 100 + j25\Omega,\ V_{oc} = 70.71\angle -45°, \bar{I}_n = 0.686\angle -59°.$

Problem 4.6 *Given the following time domain circuit Figure 4.37 with max voltage value, (a) find the equivalent phasor domain circuit. (b) Find the Thevenin equivalent v_t and R_t seen form terminal ab. (c) Draw the Thevenin circuit. (d) Use the Thevenin circuit found in (c) to determine the current $i(t)$ through terminal ab.*
Answer: *(a)* $\frac{1}{j\omega C} = -j5\Omega$. *(b)* $v_t = 8\angle 0°,\ R_t = 6\Omega$. *(c) Trival (d)* $i(t) = 0.8\sqrt{2}\cos(2\times 10^5 t - 53.13°)A$.

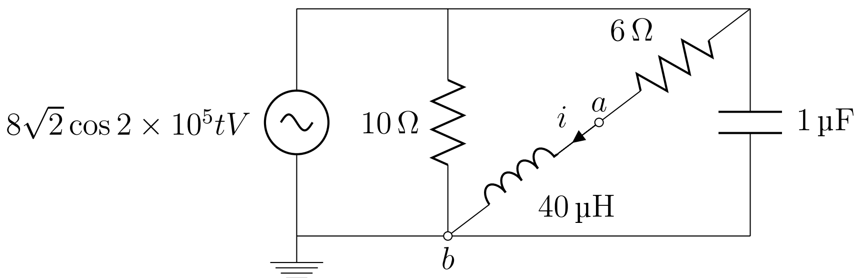


Figure 4.37: Circuit Diagram for Problem 4.6

Power related

Problem 4.7 *Consider the circuit shown in Figure 4.38. (a) Find the voltage $v_C(t)$ in steady state. (b) Find the phasor current through each element. (c) Compute the power and reactive power taken from the source. (d) Compute the power and reactive power delivered to each element.*

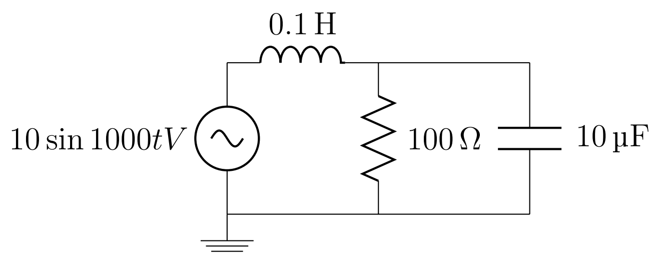


Figure 4.38: Circuit Diagram for Problem 4.7

Answer: *(a)* $\bar{V}_C(t) = 0.1\angle - 90°$, *(b)* $\bar{I} = \frac{\bar{V}_s}{j100} + 50 - j50$, $\bar{I}_R = \frac{\bar{V}_C}{100}$, $\bar{I}_C = \frac{\bar{V}_C}{-j100}$, *(c)* $P + jQ = 0.5 + j0.5$, *(d)* $P_R = 0.5W, Q_L = 1VAR, Q_C = -0.5VAR$.

Problem 4.8 *Given the phasor domain circuit, Figure 4.39, with max voltage value, (a) Find equivalent impedance seen by the source. (b)Find the source current and determine whether the source current leads or lags? (c) Draw the power triangle for the voltage source and determine the P and Q, and pf.*

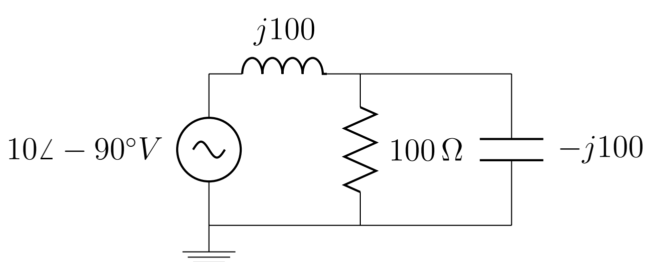


Figure 4.39: Circuit Diagram for Problem 4.8

Answer: *(a)* $R_{eq} = 50 + j50\Omega$. *(b)* $\bar{I} = 0.1414\angle - 135°A$.

Problem 4.9 *Two loads, A and B, are connected in parallel as shown in Figure 4.40. Load A consumes 10kW with a 0.9 lagging power factor. Load B has an apparent power of 15kVA with a 0.8 lagging power factor. Find the power, reactive power and apparent power delivered by the source. What is the power factor seen by the source?*

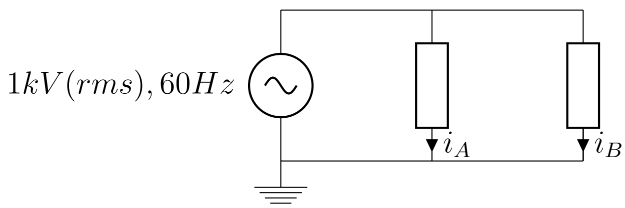


Figure 4.40: Circuit Diagram for Problem 4.9

Answer: $P = 22KW$, $Q = 13.84KVAR$, $S = 26.11KVA$, $\bar{I} = 25.98\angle -32.18$, $\bar{S} = 21.99 + j13.84$, $pf = 0.85$.

Problem 4.10 *Consider a RLC circuit, Figure 4.41, excited by* $v(t) = 100\sqrt{2}\cos 10tV$ *with* $R = 20\Omega$, $L = 1H$ *and* $C = 0.1F$. *(a) Use the phasor method to find the steady-state response current in the circuit. (b) Draw the power triangle of the load (i.e., R, L, C).*

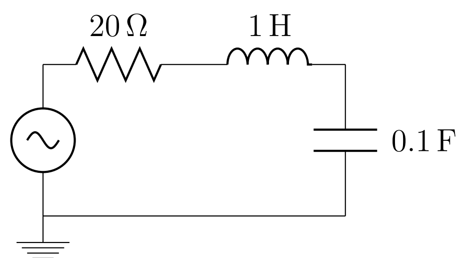


Figure 4.41: Circuit Diagram for Problem 4.10

Answer:

Problem 4.11 *Find the Thevenin equivalent circuit for the circuit shown in Figure 4.42. Find the maximum power that this circuit can deliver to a load (a) if the load can have any complex impedance; (b) if the load is purely resistive. (Hint:* $R_{load} = |Z_t|$ *and* $P = 1/2\bar{V}_{max}\bar{I}^*_{max} = \bar{V}_{rms}\bar{I}^*_{rms}$.*)*
Answer: *(a)* $\bar{I}_{load} = 1\angle 0°$, $P_{load} = 50W$. *(b)* $\bar{I}_{load} = 0.919\angle -13.28°$, $P_{load} = 42.23W$.

Problem 4.12 *For the Figure 4.43, (a) find the Thevenin equivalent (b) Determine the maximum power that can be delivered to a load when the load can have any complex value. (c) Determine the maximum power that can be delivered to a load when the load is pure resistance. (Hint:the maximum power transfer is equal to the magnitude of the Thevenin impedance.*
Answer: *(a)* $\bar{Z}_t = 70.71\angle -45°$, *(b)* $P_{max} = 25W$, *(c)* $P_{max} = 20.71W$.

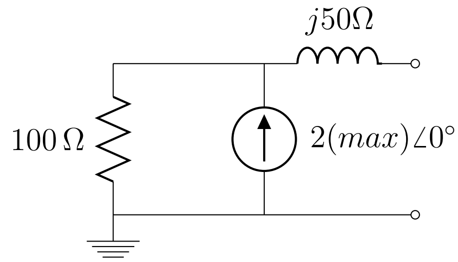


Figure 4.42: Circuit Diagram for Problem 4.11

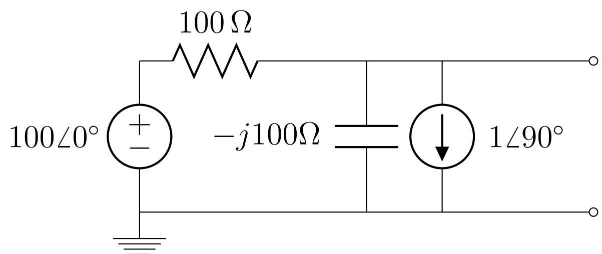


Figure 4.43: Circuit Diagram for Problem 4.12

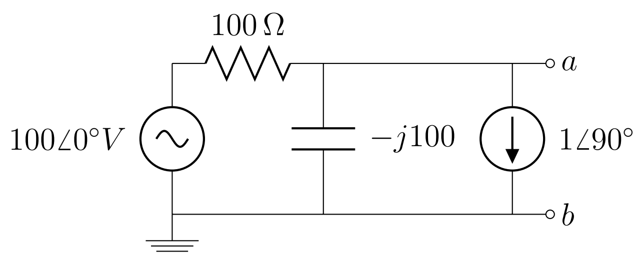


Figure 4.44: Circuit Diagram for Problem 4.13

Problem 4.13 *Given Figure 4.44, (a) find the Thevenin equivalent circuits. (b) Determine the maximum power that can be delivered to a load by the equivalent circuit if the load must be a pure resistance and connected to terminal a and b.*
Answer: *(a)* $V_T = 100\angle -90°V$. *(b) For those who solve the the problem without correction. It is unreasonable because the* $Z_T = 0$ *and* $V_T = 1\angle 90°V$, $P = 0.007071W$.

Problem 4.14 *In the Figure 4.45 (a) Find the phasor current* $\bar{I}$. *(b) the power(P), the reactive power(Q) and apparent power(S) delivered by the source (c) the power factor and state whether it is lagging or leading.*
Answer: $\bar{S} = 10kW + 5.305kVAR$, $pf = 88.347$ *lagging.*

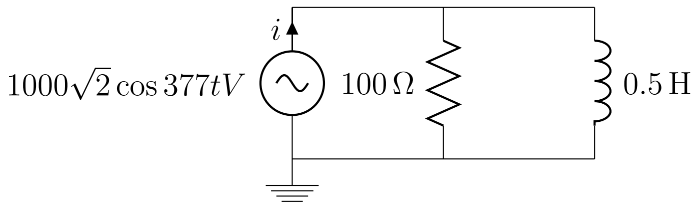


Figure 4.45: Circuit Diagram for Problem 4.14

Steady-State response

Problem 4.15 *For the circuit Figure 4.46, use the node voltage techniques to (a) find the simultaneous KCL equations. (b) Solve for $\bar{V}_1(t)$ and $v_1(t)$.*

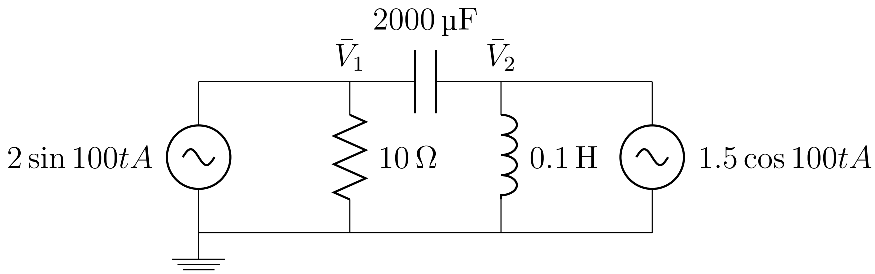


Figure 4.46: Circuit Diagram for Problem 4.15

Answer: *(a)* $\bar{V}_1 = 16.1\angle 29.7°$. *(b)* $v_1(t) = 16.1\cos(100t + 29.7°)$.

Problem 4.16 *(a) Redraw the circuit in Figure 4.47 into impedance domain. Note that the given circuit is in time domain. (b) Find the equivalent impedance for the parallel structure C and R. (c) Find the current i. (d) Find voltage v_C.*

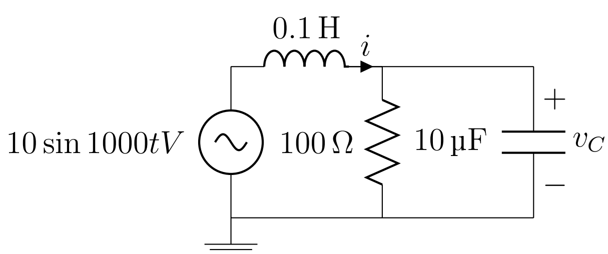


Figure 4.47: Circuit Diagram for Problem 4.16

Answer: *(a) Use of Ls and $1/Cs$ to draw (b)* $\bar{Z}_{RC} = 50 - j50$ *(c)* $\bar{I} = 0.1414\angle -135°$ *(d)* $\bar{V}_C = 10\angle -180°$

Problem 4.17 *Given a circuit diagram shown in Figure 4.48*
(a) Draw the phasor circuit. (5 pts)

(b) Solve for $i(t)$. (10 pts)
(c) Find the complex power delivered by the source. (5 pts)

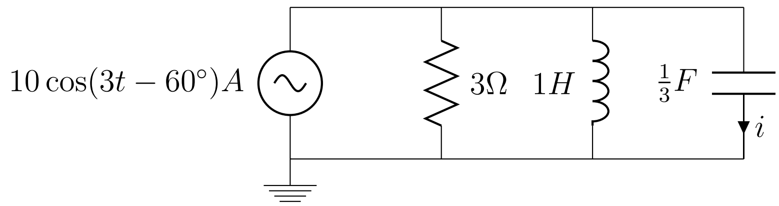


Figure 4.48: Circuit Diagram for Problem 4.17

Answer: *(a) (b)* $i(t) = 13.42\cos(3t - 33.43°)A$ *(c).*

Problem 4.18 *Given a circuit diagram shown in Figure 4.49*
(1) Find the phasor current $\bar{I}_x$.
(2) Find the voltage $v(t)$.
(3) Find the complex power delivered by the dependent source.

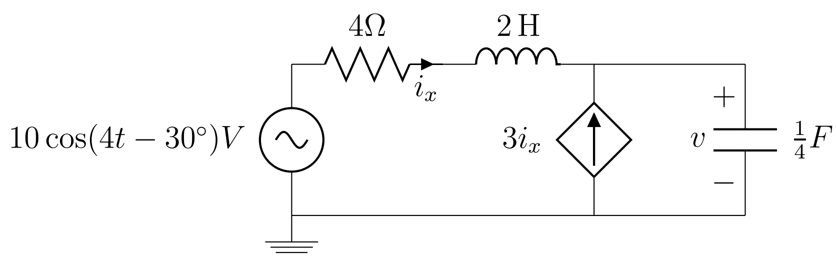


Figure 4.49: Circuit Diagram for Problem 4.18

Answer: *Labeling v on the top of dependent current source and KCL yields*

$$10\angle -30° = (4 + j8)\bar{I}_x + (-j4)\bar{I}_x$$

Solving, we have $\bar{I}_x = 1.77\angle -75°$. $\bar{V} = 7.07\angle -165°$. $v(t) = 7.07\cos(4t - 165°)$.

Problem 4.19 *Given the circuit in Figure 4.50, applying superposition to answer the questions below*
(a) What is the current $i(t)$ flowing through the inductor due to voltage source? (10 pts)
(b) What is the current $i(t)$ flowing through the inductor due to current source? (10 pts)

Answer: *(a)* $1.77\cos(2t - 75°)$*. (b)* $1.11\cos(2t - 16.31°)$.

Problem 4.20 *Given the circuit in Figure 4.51, the voltage across the load is* $170(\max)\angle 0° V$*, with 5KW and 0.8 leading pf.*
(a) Find the current flowing through the load $\bar{I}$.

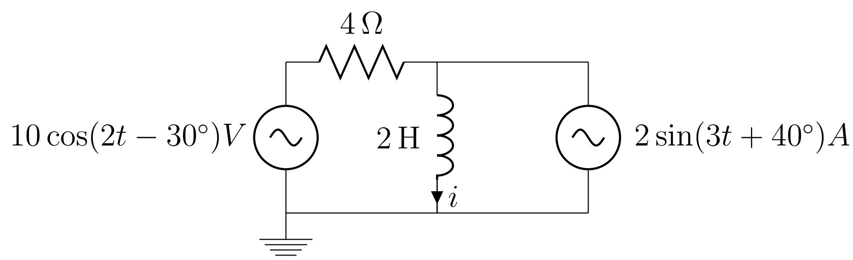


Figure 4.50: Circuit Diagram for Problem 4.19

(b) Draw the $\bar{V}$-$\bar{I}$ diagram and power triangle, respectively.
(c) Place an inductor across the load, determine the value of inductor to correct the power factor to unity if the frequency is 60Hz.

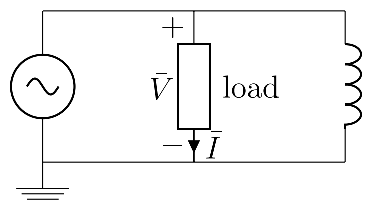


Figure 4.51: Circuit Diagram for Problem 4.20

Answer: *(a)* $\bar{I} = 73.53\angle 36.86°V$, $Q = 3.75KVar$. *(b) skip. (c)* $Q_L = \bar{V}_L \bar{I}_L^* = \frac{V_L^2}{2\pi 60L}$ *yields* $L = 10mH$

Problem 4.21 *Given the following periodic triangular function of Figure 4.52, find* v_{ave} *and* v_{rms}.

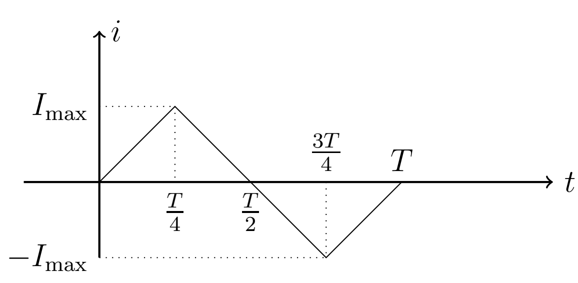


Figure 4.52: Triangular Function for Problem 4.21

Answer: (a) $i_{ave} = 0$. *(b)* $i_{rms} = \frac{I_{\max}}{\sqrt{3}}$. *Hint: find the function first.* $i(t) = \frac{4I_{\max}}{T}$, $0 > t > \frac{T}{4}$.

Problem 4.22 *In Figure 4.53(a), use phasor techniques to (a) determine the Thevenin equivalent voltage as seen by terminal ab, (b) to find Thevenin equivalent impedance as seen by terminal ab,*

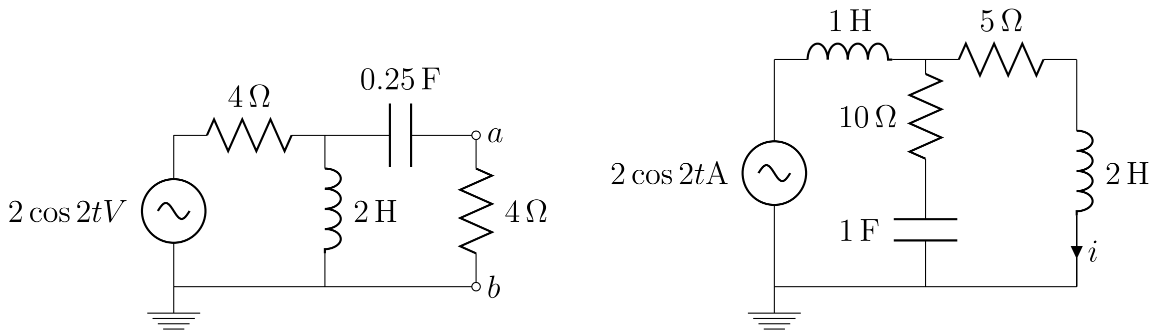


Figure 4.53: Figure (a) and (b) for Problem 4.22

(c) solve for $i(t)$ in time domain,
Answer: *(a)* $V_{oc} = \sqrt{2}\angle 45°$ *(b)* $\bar{Z}_{eq} = 2\angle 0°$ *(c)* $i(t) = 0.2357\cos(2t + 45°)$

Problem 4.23 *In Figure 4.53(b), use phasor techniques to solve for $i(t)$ in time domain.*
Answer:

Problem 4.24 *In the circuit of figure 4.54, find the power, reactive power and apparent power deliver by the source.*
Answer: *(a)* $P = 5000W$ *(b)* $Q = 383.9Var$ *(c)* $S = 5015VA$.

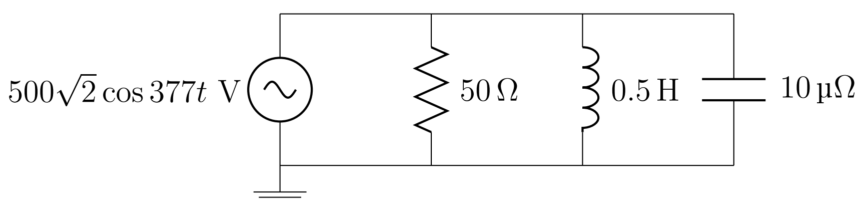


Figure 4.54: Power Calculation for Problem 4.24

Problem 4.25 *In the circuit of Figure 4.55, the voltage across the capacitive reactance is* $20\angle -56.75°V$ *(a) Find the voltage across $j60\Omega$. (b) Determine the source voltage $\bar{V}_s$.*

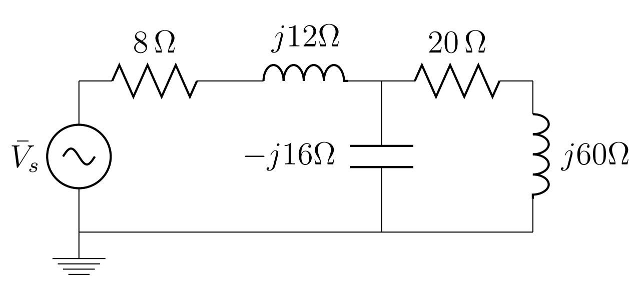


Figure 4.55: Circuit Diagram for Problem 4.25

Answer: *(a)* $19\angle -38.31°$ *(b)* $\bar{V}_s = 12.84\angle -13.56° V$ *(c) (d) (e)*

Problem 4.26 *Consider the circuit in Figure 4.56, find the Thevenin equivalent seen from terminal $j3\Omega$. (b) Draw equivalent Thevenin circuit with inductance included. (c) Solve for current I flowing in the inductance. (d) Use loop-current method, express two simultaneous equations in terms of $\bar{I}_1$ and $\bar{I}_2$. (You are not required to solve it)*

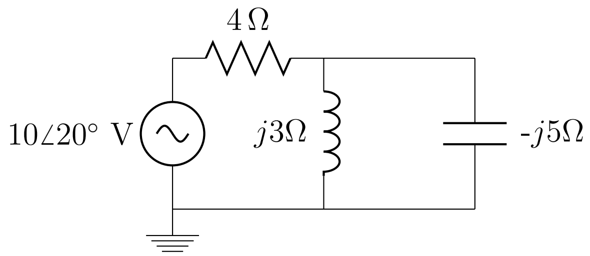


Figure 4.56: Circuit Diagram for Problem 4.26

Answer: *(a)* $\bar{Z} = 2.44 - j1.95 = 3.123\angle - 38.66°$, $\bar{V}_{oc} = 7.81\angle - 18.66°$. *(b) trivial (c)* $\bar{I} = 2.94\angle - 41.94°$ *A. (d)* $10\angle 20° = (4 + j3)I_1 - j3\bar{I}_2$. $0 = -j3\bar{I}_1 - j2\bar{I}_2$.

Problem 4.27 *Given the circuit in Figure 4.57, (a)find the individual impedance of the circuit elements. (b) What is the equivalent impedance seen by the sources (c) find the current $i(t)$. (d) The power generated by the source*

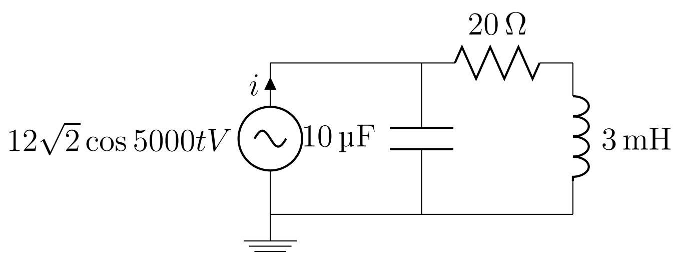


Figure 4.57: Circuit Diagram for Problem 4.27

Answer: *(a)* $R = 20\Omega$, $\bar{Z}_L = j15\Omega$, $\bar{Z}_c = -j20\Omega$ *(b)* $18.9 - j15.3\Omega$ *(c)* $i(t) = 0.494\sqrt{2}\cos(5000t + 39.09°)$ *(d)* $P + jQ = 4.61 - j3.74$.

Chapter 5

Transient Responses

Up to now, we have learned how to find the voltage across a circuit element or current flowing in an electrical circuit. For DC circuits these quantities are simply scalars of real numbers. For AC circuits these quantity are complex numbers involving magnitude and angle. However, they are all treated as either a real constant or a complex constant. In this Chapter, we are going to see the time trajectories of these electrical quantities on a scope. Since circuits are linear systems, there exit analytic techniques to analyze its time behaviors systematically and this is the focus of this Chapter. Linear system (such as circuits) time responses of an input can be divided into two responses:

• A forced response — due to external DC/AC energy source. A forced response can be maintained indefinitely as long as the external sources exist. The forced response is also known as steady-state responses.

• A natural response — due to internal energy storage (capacitors and inductors). A natural response tends to die out because of dissipation. When the natural responses die out, the steady-state condition due to forced response is reached.

The following diagram shows the difference.

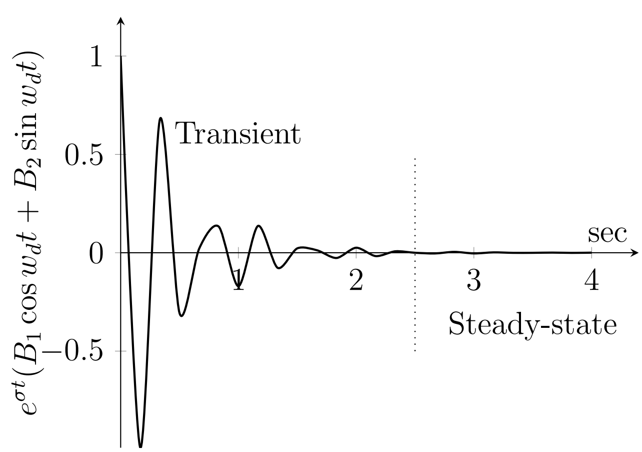


Figure 5.1: Transient and Steady-State Responses

5.1 Steady-State Response

Since steady-state response will last forever as long as the external force (either AC or DC) exists and it was discussed in previous chapter, we will summarize the procedure in what follows:

5.1.1 *RLC* circuits with AC sources

The kernel idea for such circuits is to convert the AC circuit elements into equivalent impedances, and all the electrical quantities into phasors representations. Once these notions are adopted, the techniques learned from DC circuits can be applied equally well.

Solving procedures for the forced response using phasors and impedances

Except the fact that the voltages, currents, and impedances can be complex, the equations are exactly like those of DC circuits because only resistors are active.

1. Convert the time expression of voltages and currents into the corresponding phasors. (All of the sources must have the same frequency)
2. Convert the capacitances (C) into $\frac{1}{jwC} = \frac{1}{wC}\angle -90°$, the inductances ($L$) into $jwL = wL\angle 90°$ and the resistances remains R.
3. Analyze the circuit using the techniques learned from DC circuit and solve for relevant variables with complex arithmetic.

5.1.2 *RLC* circuits with DC sources

At DC steady-state, capacitors behave as an open circuit because the voltage across the capacitor is fixed and $i_c(\infty) = C\frac{dv_C}{dt} = 0$. Likewise, at DC steady state, inductors behave as a short circuit because the current flowing through an inductor is a constant current and thus $v_L(\infty) = L\frac{di_L}{dt}$. With that in mind, we can find the steady-state values easily. Here are examples to demonstrate the concepts.

Example 5.1 (Steady-State values for DC circuits) *Find the steady-state values of the following circuit:*
Solution: *When $t \to \infty$, the capacitor is open and the inductor is shorted. $i(\infty) = 2A, \quad v(\infty)) = 50V$.*

□

Example 5.2 (Steady-State values for DC circuits) *Find the steady-state values of the following circuit:*
Solution: *When $t \to \infty$, the capacitor is open and the inductor is shorted. $i_1(\infty) = \frac{20}{10} = 2A, \quad i_2(\infty) = i_3(\infty) = 1A$.*

□

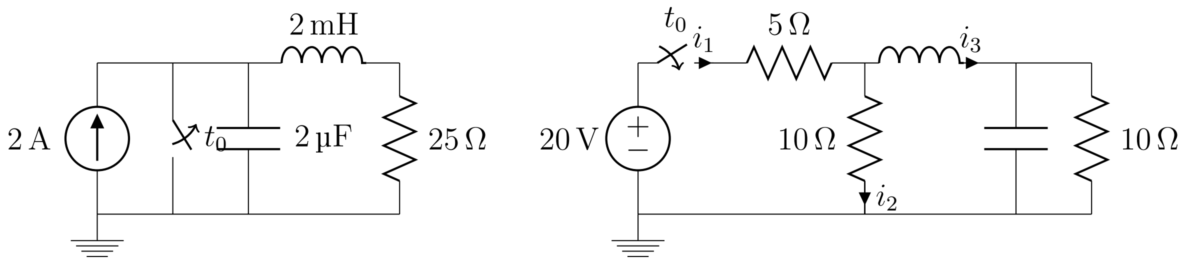


Figure 5.2: Example 5.1-5.2

Solving procedures for the forced response for *RLC* circuits with DC sources

1. Replace the capacitors with open circuits.
2. Replace the inductors with short circuits.
3. Solve the remaining circuits.

Before we embark on a study to learn the dynamic behavior of an electrical circuit, a clear understanding of a switching operation in the context of circuit analysis is important. To this end, we need to introduce the notion of time-line which is illustrated below. Here, 0 is the time of

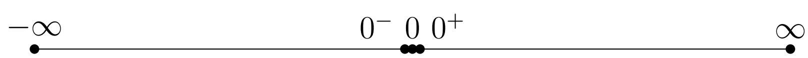


Figure 5.3: A Time-Line

switching, usually we assume it is zero (i.e., $t = 0$) for convenience. The instant before and after the switch operation is labeled as 0^- and 0^+ respectively. Furthermore, ∞ stands for a long time after switches taken place. Likewise, if a switch operation takes place at $-\infty$, then 0^- would means a long time after the switch operation taken place at $-\infty$.

5.2 First-Order Systems

We will study the 1^{st} order system first and then the 2^{nd} order systems second. In either case, we will investigate systems with and without external energy sources. Although only simple circuits are illustrated, a computer simulation program can tackle complex circuits.

5.2.1 Unforced systems

Firstly, we consider a simple case where no external sources are considered. That is, only internal energy stored in capacitors and/or inductors. Given the following circuit, find the current flowing into the resistor when the switch is open.(Assume the capacitor has $v_C(0) = v_0$ initially.)

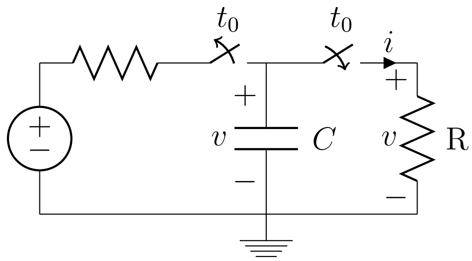


Figure 5.4: A First-Order RC System, Initially Charged

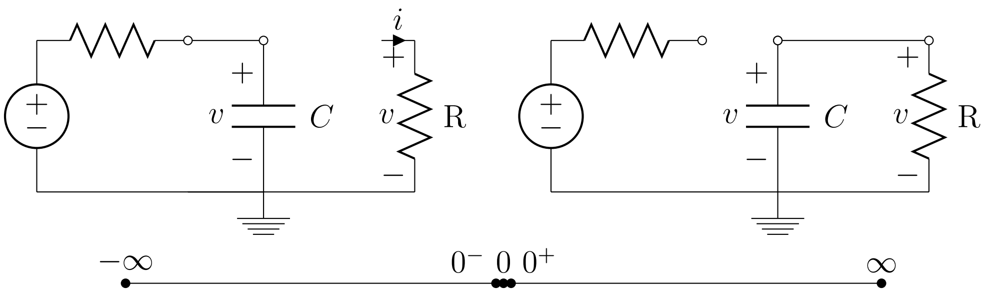


Figure 5.5: Before and After Switching Actions

The switching system has the following interpretation with a time line
Method 1: Traveling around and summing voltage, KVL equation is

$$-v_C + v_R = 0 \leftrightarrow -(-\frac{1}{C}\int i\ dt) + Ri = 0$$

Differentiating and substituting $i = Ae^{st}$ leads to

$$\frac{1}{C}i + R\frac{di}{dt} = (Rs + \frac{1}{C})Ae^{st} = 0$$

Therefore the characteristic equation yields

$$s = -\frac{1}{RC}$$

and thus the transient solution is

$$i(t) = Ae^{-\frac{t}{RC}}.$$

To find the coefficient A, we use the initial condition. Prior to the switch is open, the capacitor voltage is charged to V_0. Since v_C can not change instantaneously $(\frac{1}{2}Cv^2)$, we have $v_C(0^+) = v_C(0^-) = V_0 = i(0^+)R$ due to a parallel circuit configuration. Thus $i(0^+) = V_0/R$ and the transient solution is

$$i_R(t) = \frac{V_0}{R}e^{-\frac{t}{RC}}, \quad t \geq 0, \quad \tau = time\ constant = RC.$$

Method 2: Another way to find the dynamic equation is the use of KCL. Writing a KCL equation at the node on the top, we have

$$-C\frac{dv}{dt} = \frac{v}{R}, \quad i.e.\ C\frac{dv}{dt} + \frac{v}{R} = 0$$

from which we substitute $v = Ae^{st}$ into the equation above and find the characteristic equation

$$RCs + 1 = 0, \quad s = \frac{-1}{RC}$$

yielding

$$v(t) = Ae^{\frac{-t}{RC}} \quad t \geq 0. \tag{5.1}$$

To find the coefficient A, the initial condition yields $v(0^-) = V_0 = v(0^+) = A$[1]. A typical first-order transient time solution for equation (5.1) is displayed below

The idea of time constant is to characterize the decay rate of an exponential function. Time constant is defined as in one time constant the voltage drops by the factor $e^{-1} \approx 0.368$. Geometrically, it is the time span from the origin to a point where a tangent line at the starting point ($y_{\max}$) intersects the x-axis. Or equivalently, the point where the function reaches $0.368 \times y_{\max}$ value. It is readily seen from 5.6 that the time constant is 5 sec and this confirms with the function $y(t) = e^{0.2t}$.

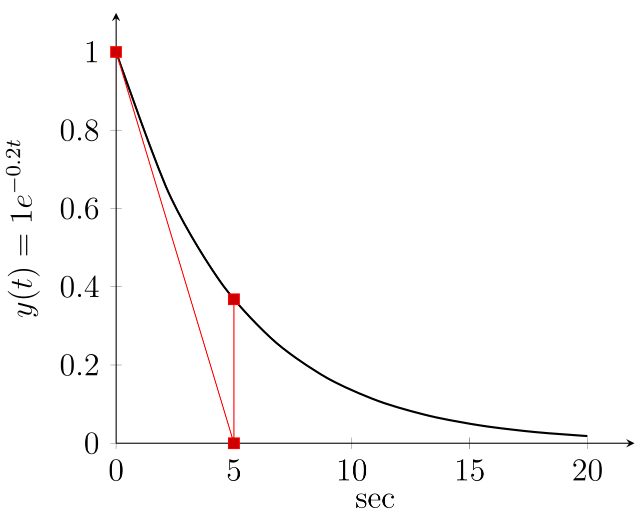


Figure 5.6: Time Constant Illustration

Let's look at another example given below:(Assume the inductor has $i_L(0) = i_0$ initially.)

which has the following interpretation with a time line: Method 1: Traveling around the loop clockwise and summing voltages, KVL equation yields

$$v_L + v_R = L\frac{di}{dt} + iR = 0.$$

[1]Find the resistor current.

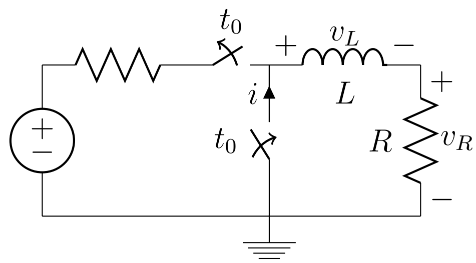


Figure 5.7: Another First-Order RL System, Initially Charged

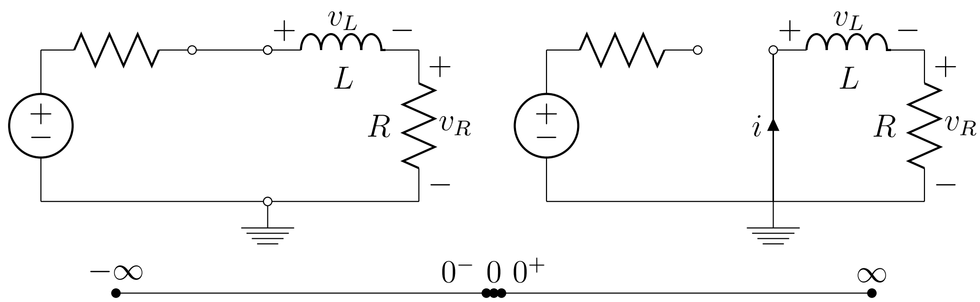


Figure 5.8: Before and After Switching Actions

Assuming $i(t) = Ae^{st}$ and substituting the assumed form into the equation gives

$$(Ls + R)Ae^{st} = 0$$

which arrives at $s = -R/L$ and $i_L(t) = Ae^{-\frac{R}{L}t}$.

To find the coefficient A, we resort to initial condition. Before the switch closes, the inductor current reaches a steady-state value of I_0 and it can not change instantaneously since energy can not change instantaneous ($W = \frac{1}{2}Li^2$), we have $i_L(0^+) = i_L(0^-) = I_0 = Ae^0 = A$. Therefore the transient solution is

$$i_L(t) = I_0 e^{-\frac{R}{L}t}, t \geq 0 \text{ and } \tau = L/R^2$$

Another example is illustrated below. The circuit has been laid there for a long time and reaches the steady state, which says $v(0^-) = 0$ and that means $i(0^-) = \frac{V_s}{R_1}$. Furthermore, when the switch is open, the source is disconnected from the system whose current dynamics is described by the following first order system

$$v_L - v_R = 0 \leftrightarrow L\frac{di}{dt} - (-iR_2) = 0$$

whose characteristic equation is $Ls + R_2 = 0$ and we have

$$i(t) = Ae^{-\frac{R_2}{L}t}$$

[2]How about a second method using KCL techniques?

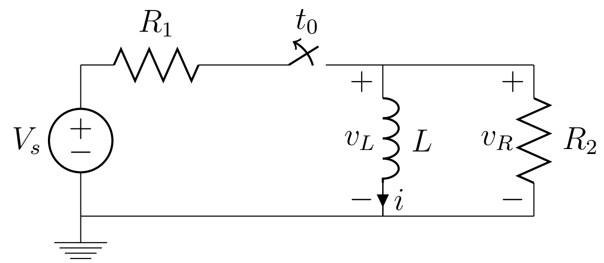


Figure 5.9: A First-Order RL System with External Force Initially

since $i_L(0) = A = \frac{V_s}{R_1}$ due to an inductor circuit, the transient solution is

$$i(t) = \frac{V_s}{R_1} e^{-\frac{R_2}{L}t}, \quad t \geq 0$$

with time constant $\tau = \frac{L}{R_2}$[3].

5.2.2 Forced systems

We have gone through the cases where external sources are neglected. But this is not the whole picture of transient response analysis. How to solve transient problems if the circuits have external sources involved?

Consider the following circuit with external forces. As always, we can tackle the problem in two ways. Method 1: Applying KCL to the node on the top yields

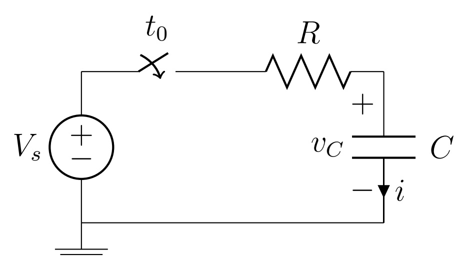


Figure 5.10: A First-Order RC System with an External Force

$$\frac{V_s - v_C}{R} = C\frac{dv_C}{dt}.$$

Rearranging, we have

$$RC\frac{dv_C}{dt} + v_C = V_s, \quad RCs + 1 = 0$$

[3]How about a second method using KCL techniques?

Following the steps shown for unforced systems, we have the unforced response

$$v_C(t) = Ae^{\frac{-t}{RC}}.$$

To find the forced response (the steady-state response for RLC circuit with DC input), we find $v_C(\infty) = V_s$ since the capacitor is open. Therefore we have a complete response

$$v_C(t) = v_C(\infty) + Ae^{-t/RC} = V_s + Ae^{-t/RC} \tag{5.2}$$

To find the coefficient A, we observe that an initially rest system (capacitor voltage can not change instantaneously) yields $0 = V_s + A$, giving $A = -V_s$. Hence,

$$v_C(t) = V_s - V_s e^{-t/RC}, \quad t \geq 0$$

To find the capacitor current, differentiating the capacitor voltage gives

$$i = C\frac{dv_C}{dt} = -\frac{V_s}{R}e^{-\frac{t}{RC}}, \quad t \geq 0$$

A typical first-order transient time solution involving forced input for equation (5.2) is displayed below

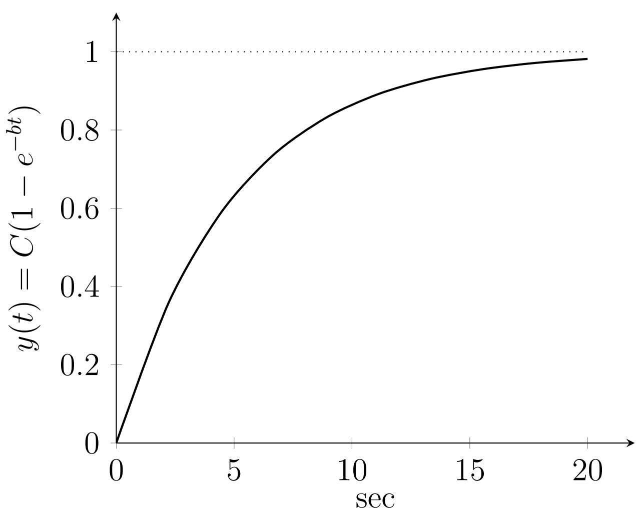


Figure 5.11: A Typical First-Order Time Response with a Forced Input

Method 2: Equivalently, another approach using KVL yields

$$V_s = iR + \frac{1}{C}\int i(\tau)d\tau$$

Differentiating, we have

$$0 = RC\frac{di}{dt} + i \quad (RCs + 1 = 0)$$

Hence, $i(t) = Ae^{-\frac{t}{RC}}$. To find the coefficient A, we know that

$$i(0^+) = \frac{V_s}{R} = A$$

due to an initially rest system whose capacitor voltage can not change instantaneously. Hence

$$i(t) = \frac{V_s}{R}e^{-\frac{t}{RC}}\text{[4]}, \quad t \geq 0.$$

Consider a second example below where a step by step systematic procedure is summarized for readers to follow.
Method 1:

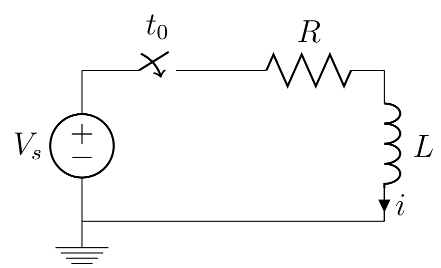


Figure 5.12: A First-Order RL System with an External Force

1. Find the initial condition. Since the inductor current can not change instantaneously before and after the switch closes. The initially rest condition means that the inductor current is zero, $i_L(0) = 0$.

2. Find the ODE. Writing a KVL equation around the loop yields

$$V_s = iR + L\frac{di}{dt}, \quad Ls + R = 0 \quad i.e.\ 0.1s + 50 = 0$$

3. Find the steady-state response. The forced response is easy to find and it is $i_L(\infty) = \frac{V_s}{R}$ after the switch closes for a long time.

4. Find the transient response. $i(t) = Ae^{-\frac{R}{L}t}, t \geq 0.$ and thus the complete solution is

$$i_L(t) = i_L(\infty) + Ae^{-\frac{R}{L}t} = \frac{V_s}{R} + Ae^{-\frac{R}{L}t}$$

[4] Given $i(t)$, find $v_c(t)$.

5. Find the coefficient A. Initial condition indicates that $i_L(0^+) = 0 = V_s/R + A$, giving $A = -\frac{V_s}{R}$. This is because the switch is open prior to $t = 0$ and the inductor current is zero. Hence

$$i_L(t) = \frac{V_s}{R}(1 - e^{-\frac{R}{L}t}), \quad t \geq 0.$$

Method 2: Equivalently, another approach using KCL yields

1′ Find the initial condition: Since the inductor current can not change instantaneously before and after switch is closed. No voltage drops over the resistor and therefore, the inductor voltage jumps to V_s when the switch closes. This means that the inductor voltage can change instantaneously.

2′ Find the ODE. Labeling v_L at the corner of R and L, KCL yields

$$\frac{V_s - v_L}{R} = \frac{1}{L}\int v_L(\tau)d\tau.$$

Arranging, we have

$$\frac{1}{R}\frac{dv_L}{dt} + \frac{1}{L}v_L = 0 \quad (\frac{1}{R}s + \frac{1}{L} = 0)$$

3′ Find the steady-state response. Since no forced input, we have $V_L(\infty) = 0$.

4′ Find the transient response.

$$v_L(t) = Ae^{-\frac{R}{L}t}, \quad t \geq 0.$$

and thus the complete solution is the transient response.

5′ Find the coefficient A. Initial condition assures $v_L(0^+) = V_s = Ae^0$. Therefore, the complete solution is

$$v_L(t) = V_s e^{-\frac{R}{L}t}, \quad t \geq 0.$$

To find the inductor current, integrating the inductor voltage yields

$$i_L(t) = \frac{1}{L}\int_0^t v(\tau)d\tau = \frac{1}{L}\int_0^t V_s e^{-\frac{R}{L}\tau}d\tau = \frac{V_s}{R}e^{-\frac{R}{L}\tau}|_t^0 = \frac{V_s}{R}(1 - e^{-\frac{R}{L}t}).$$

Let's see more examples in which we solve the problems step by step.

Example 5.3 (Transient Behavior with External Forces) *Given the following first-order RC circuit, find voltage across the capacitor.*
Solution: *Method 1:*

1. *Find the initial condition. Since the circuit is initially at rest,* $v_C(0^-) = 0$.

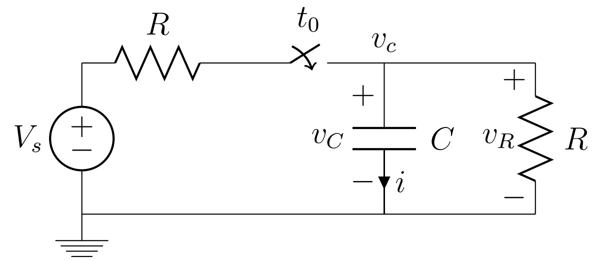


Figure 5.13: Example 5.3

2. *Find the ODE. Labeling the voltage variable v_C at the top node, current flowing in equals current flowing out and KCL gives*

$$\frac{V_s - v_C}{R} = C\frac{dv_C}{dt} + \frac{v_C}{R}$$

Arranging yields

$$C\frac{dv_C}{dt} + \frac{2v_C}{R} = \frac{V_s}{R}$$

3. *Find the steady-state response.* $v_C(\infty) = v_s/2$

4. *Find the transient response. The characteristic equation is*

$$RCs + 2 = 0, \quad s = -2/RC$$

Thus, the complete solution is

$$v_C(t) = \frac{V_s}{2} + Ae^{-\frac{2}{RC}t}$$

5. *Find coefficient A. Using initial condition* $v_C(0^+) = 0 = \frac{V}{2} + A$ *gives* $A = -\frac{V}{2}$. *The complete solution is*

$$v_C(t) = \frac{V_s}{2}(1 - e^{-\frac{2}{RC}t})^5$$

Since $\tau = RC/2 = 0.005$, the simulation time should be at least set to 5τ, for the final value will be within 1% steady-state error.

How about method 2?

□

Example 5.4 *Two switches functioning at different time periods are involved in the following circuit. Find the time response for current.*
Solution: *For $0 \le t \le 3ms$, S_1 is closed and S_2 is open.*

[5] Find the total current $i(t)$, Answer: $i(t) = \frac{V}{2R}(1 + e^{-\frac{2t}{RC}})$

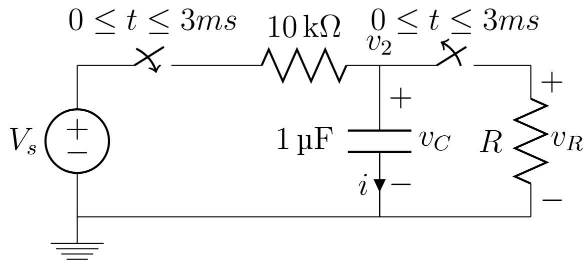
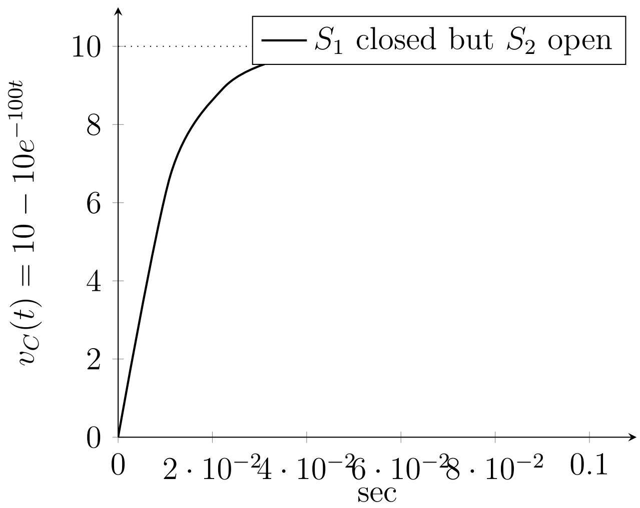


Figure 5.14: Example 5.4

1. *Find the initial condition.* $v_C(0^-) = 0$ *because the system is initially at rest.*
2. *Find ODE. Labeling* v_C *voltage variable for the capacitor and writing a KCL equation at the node*
$$\frac{V_s - v_C}{10K} = 1\mu \frac{dv_C}{dt}$$
Arranging yields
$$0.01\frac{dv_C}{dt} + v_C = V_s$$
3. *Find the steady-state solution.* $v_2(\infty) = V_s$ *due to capacitor is open.*
4. *Find the natural response from the characteristic equation* $0.01s + 1 = 0$. *We have*
$$v_{C,n}(t) = Ae^{-100t}$$
and the complete solution is
$$v_C(t) = V_s + Ae^{-100t}.$$
5. *Find the coefficient A. The initial condition* $v_C(0^+) = 0 = V_s + A$ *gives* $A = -V_s$. *The complete solution is, therefore,*
$$v_C(t) = V_s(1 - e^{-100t})V.$$
Since $\tau = RC = 0.01$, *the simulation time should be at least set to* 5τ, *for the final value will be within 1% steady-state error.*

Another approach is shown below:

1. $Z(s) = 10^4 + \frac{1}{10^{-6}s} = \frac{10^{-2}s+1}{10^{-6}s}$
2. $i_f = V/Z(0) = V/\infty = 0$
3. $i_n(t) = Ae^{-100t}A, t \ge 0$ $i_n(0^+) = V/10^4$. *Therefore* $i(t) = \frac{V}{10^4}e^{-100t}$
4. $v_2(t) = V - i(t) \times 10^4 = V(1 - e^{-100t})V$



For $3ms < t$, S_1 is closed and S_2 closed too.
Note that $v_2(3ms) = 13 = V(1 - e^{-100\times 3\times 10^{-3}})$ gives $V = 50.16V$ KCL gives

$$\frac{V - v_2}{10K} = 1\mu\frac{dv_2}{dt} + \frac{v_2}{3.5K}$$

Arranging yields

$$C\frac{dv_c}{dt} + \frac{2v_C}{R} = \frac{V}{R}$$

Thus, $v_c(t) = \frac{V}{2} + Ae^{-\frac{2}{RC}t}$. To find coefficient A, initial condition $v_C(0^+) = 0 = \frac{V}{2} + A$ gives $A = -\frac{V}{2}$. Another approach is shown below:

1. $Z(s) = 10^4 + (\frac{1}{10^{-6}}//R_2) = 10^4 + \frac{R_2}{1+10^{-6}s}$.
2. $i_f = V/Z(0) = 50.16/(10^4 + R_2)$
3. $v_2(3ms) = (50.16R_2)/(10^4 + R_2)$ *yields* $R_2 = 3498.4 \approx 3.5K\Omega$
   (a)because $\frac{di}{dt} = 0$ *therefore* V_L*=0* v *short-circuit*
   (b)$i_L(0^+) = IA, i_R(0^+) = -IA$. *because* $i_L + i_R = 0$
   $V_R = iR = -I \cdot R$, *because* $V_L = V_R = -IR = L\frac{di_L}{dt}$ *therefore* $\frac{di_L}{dt} = \frac{-2R}{L}$
   (c)$i_L + i_R = 0 \Longrightarrow \frac{1}{L}\int_0^t v(\tau)d\tau + v_0 + \frac{V}{R} = 0 \Longrightarrow \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v = 0, t \geq 0$
   therefore $v(t) = Ae^{-\frac{R}{L}t}V = -IRe^{-\frac{R}{L}t}V$ *because* $v(0) = -IR$
   (e)$i_L = -i_R = -\frac{v(t)}{R} = +Ie\frac{-\frac{R}{L}t}{A}t \geq 0$

□

Example 5.5 (First-order with external force) *Consider the RC circuit with DC current source, find the capacitor voltage.*
Solution:

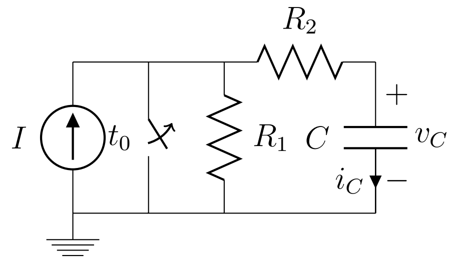


Figure 5.15: Example 5.5

1. *Find the initial conditions. Prior to the switch opens, the capacitor voltage is zero and it can not change instantaneously after the switch closes. Therefore, the initial condition is* $v_C(0^-) = 0 = v_C(0^+)$.

2. *Find the ODE. Labeling* v *at the connection between* R_1 *and* R_2 *and writing a* KCL *equation yields*

$$\begin{aligned} I &= \frac{v}{R_1} + C\frac{dv_C}{dt} \\ v &= i_C R_2 + v_C = R_2(C\frac{v_C}{dt}) + v_C \end{aligned}$$

Substituting the second equation into the first equation gives

$$I = (\frac{R_1 + R_2}{R_1})C\frac{dv_C}{dt} + \frac{v_C}{R_1}, \quad ((R_1 + R_2)Cs + 1 = 0)$$

which is a first order differential equation with force.

3. *Find the steady-state solution (particular solution, forced solution) and it is found to be (capacitor is open as* $t \to \infty$*)*

$$v_C(\infty) = IR_1$$

4. *Find the natural response (complementary solution, transient response) by considering the homogeneous equation (setting the external force to zero and use the techniques for unforced response.)*

$$v_C(t) = Ae^{\frac{-t}{(R_1+R_2)C}}.$$

5. *Find the coefficients which is* A *for this example. The initial condition* $v_C(0^-) = 0 = v_C(0^+) = IR_1 + A$ *yields* $A = -IR_1$. *The complete solution is*

$$v_C(t) = IR_1(1 - e^{\frac{-t}{(R_1+R_2)C}}), \quad t \geq 0.$$

Since $\tau = (R_1 + R_2)C = 0.005$, *the simulation time (TSTOP) should be at least set to* 5τ, *for the final value will be within 1% steady-state error.*

How about method 2?

□

Example 5.6 (First-order ODE, switching back and forth) *The following circuit is very important and serves to illustrate the general principles and concepts that are common to all circuit problems.*

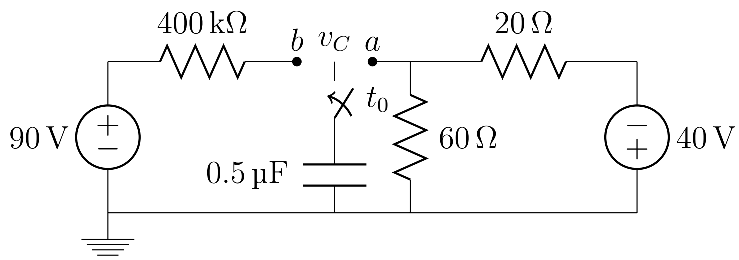


Figure 5.16: Example 5.6

Solution: *(a) Assume the switch is at position a for a long time, then flip to position b.*

1. *Find the initial conditions. Switch is at position a for a long time, thus* $v_C(0^-) = -40 \times \frac{6}{8} = -30V$.

2. *Find the 1st order ODE. Using KCL, we get*

$$\frac{90 - v_C}{4K} = 0.5 \times 10^{-6} \frac{dv_C}{dt}.$$

Substituting circuit parameters and rearranging yield

$$0.002 \frac{dv_C}{dt} + v_C = 90.$$

3. *Find the transient response. The characteristic equation is* $0.002s + 1 = 0$, *yielding* $s = -500$ *and the natural response readily obtained as*

$$v_{C,n}(t) = Ae^{-500t}, \quad t \geq 0.$$

4. *Find the forced response. It is readily seen that* $v_C(\infty) = 90$, *leading to the complete solution being*

$$v_C(t) = 90 + Ae^{-500t}, \quad t \geq 0.$$

5. *Find the coefficient A.* $v_C(0^+) = v_C(0^-) = -30 = 90 + A$, *we have* $A = -120$. *Thus*

$$v_C(t) = 90 - 120e^{-500t} V, \quad t \geq 0.$$

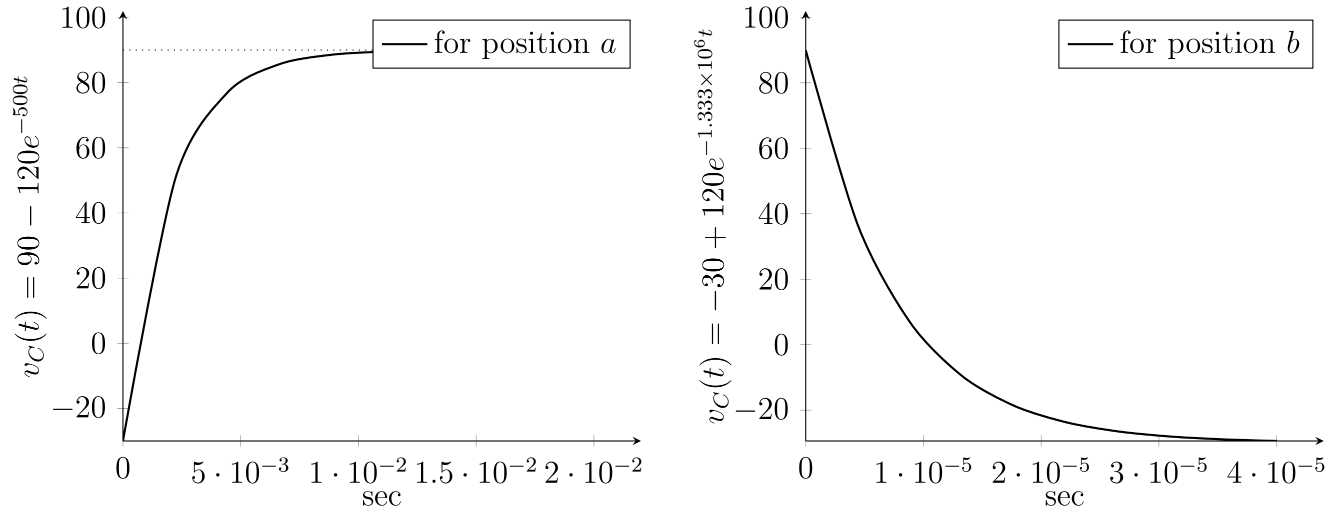


Figure 5.17: Time Response $v_C(t)$ for Example 5.6

2′) *What happens if you use the KVL in step 2.*

$$90 = 4Ki + \frac{1}{C}\int i\ dt$$

Substituting circuit parameters and differentiating yield

$$4K\frac{di}{dt} + 2 \times 10^6 i = 0.$$

3′) *Find the transient response. The characteristic equation is* $4Ks + 2 \times 10^6 = 0$, *yielding* $s = -500$ *and*

$$i_n(t) = Ae^{-500t}, \quad t \geq 0.$$

4′) *Find the forced response.* $i(\infty) = 0$ *and the complete solution is* $i(t) = Ae^{-500t}, \quad t \geq 0.$

5′) *Find the coefficient A which needs the initial condition for* $i(0^+)$. *Since* $v_C(0^+) = -30$, *the KVL still holds for*

$$90 = v_R(0^+) + v_C(0^+) = i(0^+)4K - 30.$$

Therefore, $i(0^+) = \frac{90+30}{4K} = 3 \times 10^{-2} = A$. *Thus*

$$i(t) = 3 \times 10^{-2} e^{-500t} A^6, \quad t \geq 0.$$

But to find $v_C(t)$, *an integration technique leads to*

$$v_C(t) = \frac{1}{C}\int_0^t i(\tau)\ d\tau + v_C(0) = -120e^{-500\tau}|_0^t + (-30) = 90 - 120e^{-500t}V, \quad t \geq 0.$$

(b) Now, continue to find the scenario when the switch is switched from position b back to position a.

1. *Find the initial conditions. Switch is at position b for a long time, thus* $v_C(0^-) = 90V$.
2. *Find the 1st order ODE. Using KCL, we get*

$$\frac{-40 - v_C}{20} = \frac{v_C}{60} + 0.5 \times 10^{-6}\frac{dv_C}{dt}$$

which yields

$$0.5 \times 10^{-6}\frac{dv_C}{dt} + \frac{80}{120}v_C = -2.$$

3. *Find the transient response. The characteristic equation is* $0.5 \times 10^{-6}s + \frac{8}{12} = 0$, *yielding* $s = -1.333 \times 10^6$ *and*

$$v_{C,n}(t) = Ae^{-1.333\times10^6 t}, \quad t \geq 0.$$

4. *Find the forced response.* $v_C(\infty) = -30$. *Thus, the complete solution is*

$$v_C(t) = -30 + Ae^{-1.333\times10^6 t}, \quad t \geq 0.$$

5. *Find the coefficient A. Since* $v_C(0^+) = v_C(0^-) = 90 = -30 + A$, *we have* $A = 120$. *Thus*

$$v_C(t) = -30 + 120e^{-1.333\times10^6 t}V, \quad t \geq 0.$$

Since $\tau = RC = 7.5\mu$, *the simulation time should be at least set to* 5τ, *for the final value will be within 1% steady-state error.*

□

Example 5.7 (First-Order ODE) *This example is similar to the previous example.*[7]

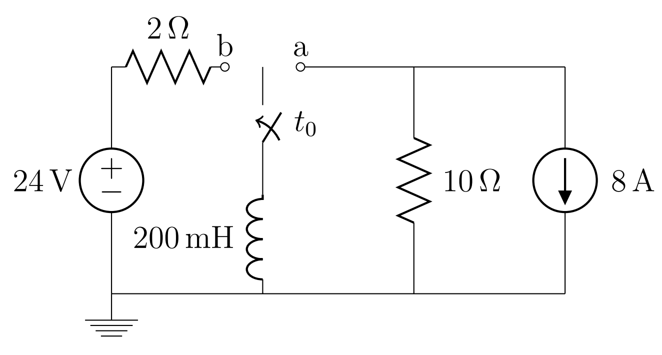


Figure 5.18: Example 5.7

Solution:
(a) Assume the switch is at position a for a long time, then flip to position b

[7] In a similar fashion as those taught in the previous example, plot the time functions.

1. *Find the initial conditions. Switch is at position a for a long time, thus* $i_L(0^-) = 8A$ *entering from the negative polarity.*

2. *Find the 1st order ODE for* $i_L(t)$*. Using KVL, we get*

$$24 = Ri + L\frac{di_L}{dt}$$

Substituting circuit parameters yields

$$0.2\frac{di_L}{dt} + 2i = 24.$$

3. *Find the transient response. The characteristic equation is* $0.2s + 2 = 0$*, yielding* $s = -10$ *and*

$$i_L(t) = Ae^{-10t}, \quad t \geq 0.$$

4. *Find the forced response.* $i_L(\infty) = 12$ *and the complete solution is*

$$i_{L,n}(t) = 12 + Ae^{-10t}, \quad t \geq 0.$$

5. *Find the coefficient A.* $i_L(0^-) = -8 = i_L(0^+) = 12 + A$*, we have* $A = -20$*, yielding*

$$i_L(t) = 12 - 20e^{-10t}A, \quad t \geq 0.$$

$2'$) *What happens if you use the KCL in step 2.*

$$\frac{24 - v_L}{2} = \frac{1}{L}\int v_L \; dt$$

which yields

$$\frac{dv_L}{dt} + 10v_L = 0.(s + 10 = 0)$$

$3'$) *Find the transient response. The characteristic equation is* $s + 10 = 0$*, yielding* $s = -10$ *and*

$$v_L(t) = Ae^{-10t}, \quad t \geq 0.$$

$4'$) *Find the forced response by setting the derivative term to zero. Thus,* $v_L(\infty) = 0$*.*

$5'$) *Find the coefficient A which needs the initial condition for* $v_L(0^+)$*. Since the KVL still holds when the switch is flip to position b, we have*

$$V_s = 24 = v_R(0^+) + v_L(0^+) = 2i(0^+) + v_L(0^+) = 2(-8) + v_L(0^+)$$

which, in turn, yields $v_L(0^+) = 40$*. Therefore,* $v_L(0^+) = 40 = A$ *and*

$$v_L(t) = 40e^{-10t}V, \quad t \geq 0.$$

But to find $i_L(t)$*, we need to use integration which is displayed below*

$$i_L(t) = \frac{1}{L}\int_0^t v_L(\tau) \; d\tau + i_L(0) = -20e^{-10\tau}|_0^t + (-8) = 12 - 20e^{-10t}V, \quad t \geq 0.$$

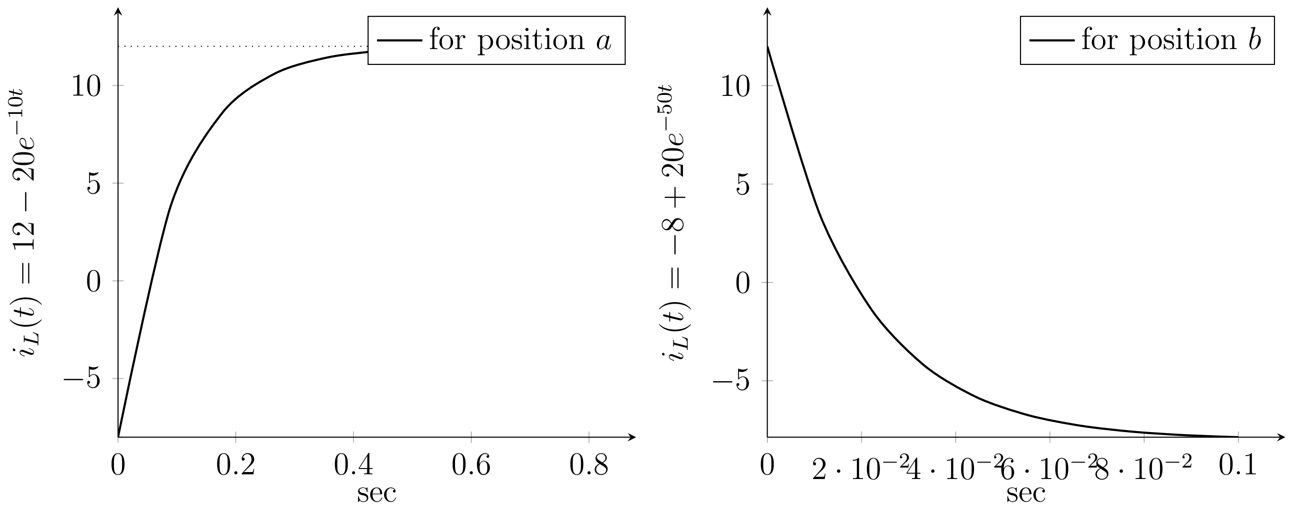


Figure 5.19: Time Response $i_L(t)$ for Example 5.7

(b) Now, continue to find the scenario when the switch is switched from position b back to position a.

1. *Find the initial conditions. Switch is at position b for a long time, thus* $i_L(0^-) = 12A$ *entering from the positive polarity.*
2. *Find the 1st order ODE for* $v_L(t)$. *Using* KCL, *we get*
$$0 = 8 + \frac{v_L}{10} + \frac{1}{0.2}\int v_L(\tau)d\tau$$
which yields (by differentiation)
$$0.1\frac{dv_L}{dt} + 5v_L = 0.(0.1s + 5 = 0)$$
3. *Find the transient response. The characteristic equation is* $0.1s+5 = 0$, *yielding* $s = -50$ *and*
$$v_{L,n}(t) = Ae^{-50t}, \quad t \geq 0.$$
4. *Find the forced response.* $v_L(\infty) = 0$. *and the complete solution is*
$$v_L(t) = Ae^{-50t}, \quad t \geq 0.$$
5. *Find the coefficient A. This is trick for this example. Since the* $i_L(0^+) = i_L(0^-) = 12$ *when the switch is flip back to position a, the initial inductor current (12A) and the current source (8A) is injecting into the 10* Ω *resistor, we have* $v_R = -20 \times 10 = -200V$ *initially. Thus* $v_L(0^+) = -200 = Ae^0$, *from which the complete solution is*
$$v_L(t) = -200e^{-50t}, \quad t \geq 0.$$

It is interesting to know that the inductor current can be obtained by integrating the inductor voltage and that is

$$i_L(t) = -8 + 20e^{-50t}A, \quad t \geq 0^8.$$

□

Example 5.8 (First-Order ODE, with AC source) *Given the following RC circuit with AC voltage source whose angular frequency is $w = 60$ ($f = w/2\pi = 9.549Hz$.)*

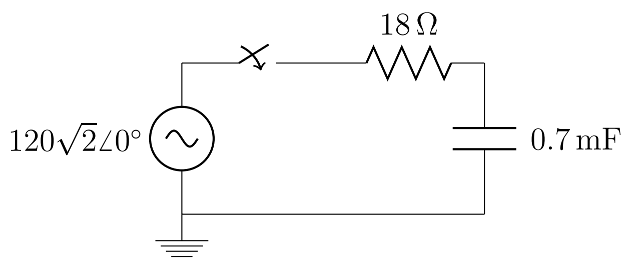


Figure 5.20: Example 5.8

Solution:

1. *Find the initial condition. Immediately after the switch is closed, the capacitor voltage remains zero and the current suddenly jumps to $120/18 = 6.667A$.*

2. *Find the ODE. Traveling around the loop and summing voltages, we have*

$$120\sqrt{2}\cos 60t = 18i + \frac{1}{C}\int i(\tau)d\tau.$$

Differentiating, we have

$$18\frac{di}{dt} + \frac{1}{0.7m}i = -120\sqrt{2} \times 60 \sin 60t$$

3. *Find the forced response, we use phasor concept and it is readily found*

$$i(\infty) = 120\angle 0^\circ/(18 - j24) = 4\angle 53.13^\circ$$

whose time expression is

$$i(\infty) = 4\sqrt{2}\cos(60t + 53.13^\circ).$$

[8] Plot the inductor current.

4. *Find the transient response. Use homogeneous equation and the characteristic equation is found to be* $18s + 1428 = 0, \quad s = -79.4$, *which yields*

$$i_n(t) = Ae^{-79.4t}.$$

Thus the complete response is

$$i(t) = 4\sqrt{2}\cos(60t + 53.13°) + Ae^{-79.4t}.$$

5. *Find the undetermined coefficient A. The initial condition yields*

$$i(0^+) = A + 4\sqrt{2}\cos 53.13° = 6.667, \quad A = 3.273.$$

Finally the complete response is

$$i(t) = 4\sqrt{2}\cos(60t + 53.13°) + 3.273e^{-79.4t}, \quad t \geq 0. \tag{5.3}$$

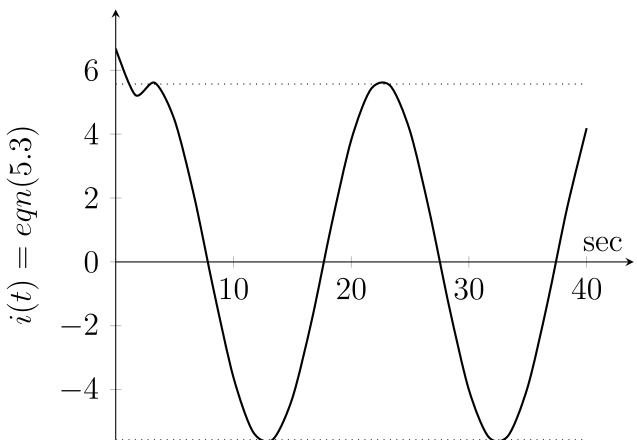


Figure 5.21: Time Response $i(t)$ for Example 5.8

□

Example 5.9 (First-order ODE) *Given the following RC circuit with AC voltage source, find the current after the switch is closed*[9]*.*
Solution:

1. *Find the initial condition. Immediately after the switch is closed, the capacitor voltage remains zero and the current becomes* $6000/5 = 1200A$.

[9] Equipped with the previous example, verify the following problem via PSpice/MATLAB.

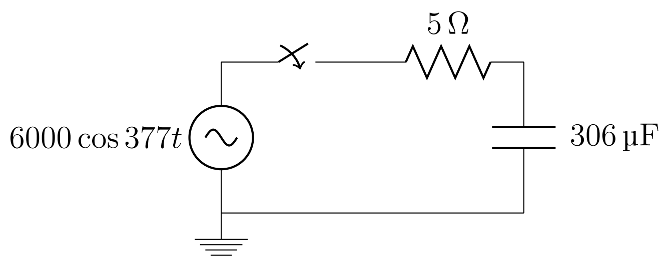


Figure 5.22: Example 4.5(b)

2. *Find the ODE for $i(t)$. Traveling around the loop and summing voltage leads to*

$$6000\cos 377t = 5i + \frac{1}{C}\int i(\tau)\tau$$

Differentiating, we have

$$\frac{10^6}{306}i + 5\frac{di}{dt} = -6000 \times 377\sin 377t, \quad (5s + \frac{10^6}{306} = 0).$$

3. *Find the forced response using phasor concept*

$$\bar{I} = 6000\angle 0^\circ/(5 - j8.668) = \frac{6000\angle 0^\circ}{10\angle -60^\circ}, \quad i.e.\ i(\infty) = 600\cos(377t + 60^\circ).$$

4. *Find the transient response. The characteristic equation for the homogeneous equation without input force is $5s + 3268 = 0$, leading to $s = -654$. Thus*

$$i_n(t) = Ae^{-654t}, \quad t \geq 0.$$

5. *Find the coefficient A. At the instant the switch closes, we have*

$$1200 = 600\cos 60^\circ + A$$

which yields $A = 600$ and the complete solution is

$$i(t) = 600\cos(377t + 60^\circ) + 600e^{-654t}. \tag{5.4}$$

□

5.2.3 Solving procedures for the first-order systems

Summary for solving the first-order circuits (RC or RL circuits) is itemized as what follows.

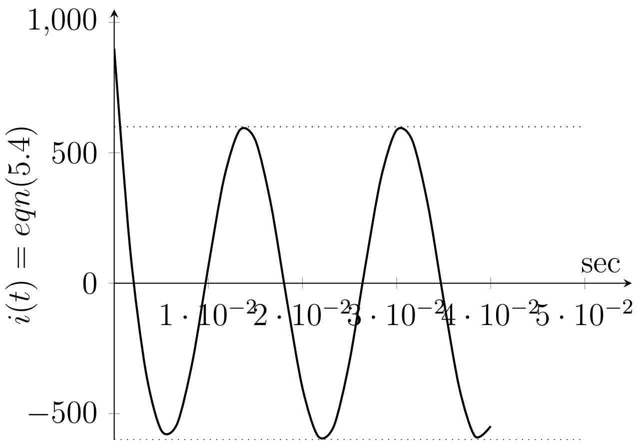


Figure 5.23: Time Response $i(t)$ for Example 5.9

Without external energy

1. Determine initial conditions using $W_C = \frac{1}{2}Cv^2, W_L = \frac{1}{2}Li^2$. That is, capacitor voltage and inductor current can not, respectively, change its value instantaneously. (If no hints, then assume initially at rest).

2. Form 1^{st}-order ODE using KCL or KVL.

3. Identify natural response / transient response $x_n(t, A) = Ae^{st}$ where x_n could be v or i.

4. Evaluate the undetermined coefficient A by using IC: $v_C(0^-) = v_C(0^+) = A$ or $i_L(0^-) = i_L(0^+) = A$.

With external energy

1. Determine initial conditions using $W_C = \frac{1}{2}Cv^2, W_L = \frac{1}{2}Li^2$. That is, capacitor voltage and inductor current can not, respectively, change its value instantaneously. (If no hints, then assume initially at rest).

2. Form 1^{st}-order ODE by using KCL or KVL

3. Identify natural/transient response $x_n(t, A) = Ae^{st}, t \geq 0$

4. Determine forced response, $x_f(t)$
(a) For DC source, use $Z(0)$ and $V = IR$
(b) For AC source, use $Z(j\omega)$ and $\bar{V} = \bar{I}\bar{Z}$ (Phasor)

5. Evaluate the undetermined coefficient A by using IC. Thus the identity,

$$x(0) = x_f + x_n(0, A) = x_f + Ae^0$$

yields $A = x(0) - x_f$.

Elements	R	L	C
$\bar{Z}(s)$	R	Ls	$\frac{1}{Cs}$
$\bar{Z}(0)$	R	0	∞
$\bar{Z}(j\omega)$	R	$j\omega L$	$\frac{1}{j\omega C}$

Table 5.1: Table of Impedance

5.3 Second-Order Systems

In what follows, we will investigate deriving transient solutions for circuits that contain two energy storage elements (one L and one C). These are said to be second-order circuits. If we combine the two L's or two C's into one single element by a series or parallel combination, then the system is of first-order.

5.3.1 Facts

Recalling the following identities that we have accumulated over the learning process.

$$\begin{aligned}
v &= L\frac{di}{dt} & i &= \frac{1}{L}\int v(\tau)d\tau \quad \text{Henry's law for inductors, t-domain} \\
V &= LsI^{10} & I &= \frac{1}{L}\frac{V}{s} \quad \text{impedance concept for inductors, s-domain} \\
i &= C\frac{dv}{dt} & v &= \frac{1}{C}\int i(\tau)d\tau \quad \text{Faraday's law for capacitors, t-domain} \\
I &= CsV & V &= \frac{1}{C}\frac{I}{s}^{11} \quad \text{impedance concept for capacitors, s-domain.}
\end{aligned}$$

5.3.2 Unforced systems

We will study unforced systems first and then forced systems. The general principles and concepts are similar to the circuits of first-order degree that we have learned in the previous sections. The solution to these second-order differential equations depends, as in the case of first-order systems, on initial conditions and on forcing function. Since all the desired circuit variables may be obtained either as a function of i_L or as a function of v_C, the choice of the preferred differential equations depends on specific circuit applications.

Parallel RLC circuits

Given the following second-order parallel RLC circuit, find its current in terms of voltage.

Picking a ground node at the bottom, assigning a current direction, and writing a KCL equation

[11] This can be proved by applying the exponential signal $i_e = e^{st} \rightarrow \frac{di_e}{dt} = se^{st} = si_e$.

[11] Prove this form.

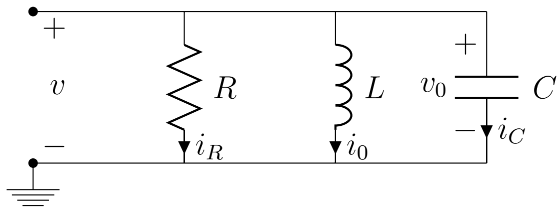


Figure 5.24: Parallel Structure

at the top node yield

$$\begin{aligned}
0 &= i_C + i_L + i_R \\
&= C\frac{dv}{dt} + i_L + \frac{v}{R} && (5.5)\\
&= C\frac{dv}{dt} + \underbrace{\frac{1}{L}\int v(\tau)d\tau}_{i_L} + \frac{v}{R}, \quad 0 = (Cs + \frac{1}{Ls} + \frac{1}{R})V && (5.6)\\
&= C\frac{d}{dt}(L\frac{di_L}{dt}) + i_L + \frac{1}{R}(L\frac{di_L}{dt}), \quad 0 = (LCs^2 + 1 + \frac{L}{R}s)I. && (5.7)
\end{aligned}$$

The s-domain expression (5.6) can be converted to (5.7) or vice versa by letting $V = LsI$ and $I = V/Ls$. The beauty of such s-domain operation is its simplicity – algebraic operation.

Method 1: Differentiating the t-domain equation (5.6) yields

$$C\frac{d^2v}{dt^2} + \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v = 0. \quad (Cs^2 + \frac{1}{R}s + \frac{1}{L} = 0) \tag{5.8}$$

The derived differential equation is expressed in v, which is v_C in this example. Can we drive an ODE in i_L?

Method 2: Start with the following identities (5.7), to obtain an ODE in i_L

$$LC\frac{d^2i_L}{dt^2} + \frac{L}{R}\frac{di_L}{dt} + i_L = 0. \quad (LCs^2 + \frac{L}{R}s + 1 = 0) \tag{5.9}$$

It should be noted that both (5.8) and (5.9) have the same characteristic equations even though the differential equations are expressed in terms of different variables, v_C and i_L respectively. The point here is that a circuit will have one unique characteristic equation. Focusing on (5.8), substituting $v(t) = Ae^{st}$ into the equation above and factoring out Ae^{st}, it is readily seen that the corresponding characteristic equation associated with ODE (5.8) is

$$Cs^2 + \frac{s}{R} + \frac{1}{L} = 0$$

which is quadratic in s. Solving, we have

$$s_1, s_2 = -\frac{1}{2RC} \pm \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}} = -\alpha \pm \sqrt{\alpha^2 - \omega_n^2} = -\alpha \pm j\omega_d.$$

where w_n is known as natural frequency/resonant frequency and w_d is called damped frequency. Notice that the third equal sign holds true only if $\alpha^2 - w_n^2 < 0$.

The general solution has the form

$$v(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}, \quad t \geq 0.$$

where the exponents s_1 and s_2 are determined by parameters R, L, C.

Learning from course of Mathematic Engineering, we know that there are 3 possible outcomes for the roots of s_1 and s_2:

1. $\alpha^2 > \omega_n^2$; Overdamped response (Distinct real roots); $\Delta > 0$.

$$v(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}$$

To find the undetermined coefficients A_1 and A_2, we find

$$\begin{aligned} v_C(0^+) &= v_0 = A_1 + A_2 \\ \frac{dv_C(0^+)}{dt} &= \frac{i_C(0^+)}{C} = s_1 A_1 + s_2 A_2 \end{aligned}$$

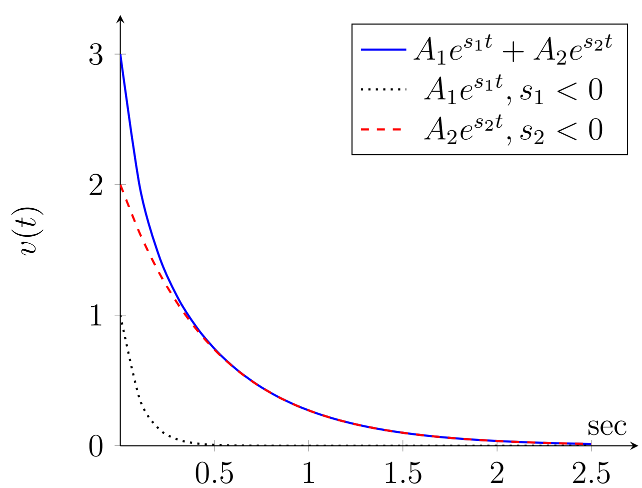


Figure 5.25: Time Response $y(t)$ for Distinct Roots (Overdamped Responses)

Can you figure out the time constant for the individual exponential functions in Figure 5.25? The meaning of time constant is worth noting from this example.

2. $\alpha^2 < \omega_n^2$; Underdamped response (Complex roots); $\Delta < 0$.

$$\begin{aligned} v(t) &= A_1 e^{-(\alpha + jw_d)t} + A_2 e^{-(\alpha - jw_d)t} \\ &= e^{-\alpha t}(A_1 e^{-jw_d t} + A_2 e^{jw_d t}) \\ &= e^{-\alpha t}[(A_1 + A_2)\cos w_d t + j(A_2 - A_1)\sin w_d t] \\ &= e^{-\alpha t}(B_1 \cos \omega_d t + B_2 \sin \omega_d t) \end{aligned}$$

To find the undetermined coefficients A_1 and A_2, we find

$$\begin{aligned} v_C(0^+) &= v_0 = B_1 \\ \frac{dv_C(0^+)}{dt} &= \frac{i_C(0^+)}{C} = -\alpha B_1 + w_d B_2 \end{aligned}$$

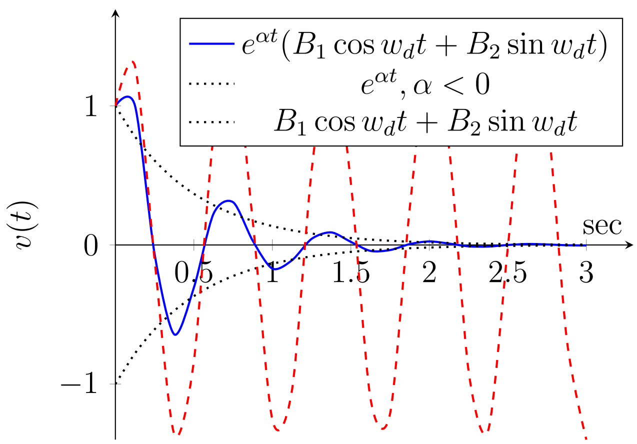


Figure 5.26: Time Response $y(t)$ for Complex Roots (Underdamped Responses)

3. $\alpha^2 = \omega_n^2$; Critically damped response (Equal real roots); $\Delta = 0$.

$$v(t) = (A_1 + A_2)e^{-\alpha t} = Ae^{-\alpha t}$$

which reduces to one undetermined constant and this is erroneous. The way to overcome this is to insert a t

$$v(t) = (A_1 + A_2 t)e^{-\alpha t}$$

This will have two undetermined constants and that is plausible for a second-order solution.

The undetermined coefficients A_1 and A_2 are determined by initial conditions

$$\begin{aligned} v_C(0^+) &= V_0, \quad \frac{dv_C(0^+)}{dt} = \frac{i_C(0^+)}{C}, \quad \text{if the ODE is expressed in } v_C \\ i_L(0^+) &= I_0, \quad \frac{di_L(0^+)}{dt} = \frac{v_L(0^+)}{L}, \quad \text{if the ODE is expressed in } i_L. \end{aligned}$$

Example 5.10 (Overdamped Response) *Given the parallel RLC circuit Figure 5.24 above with* $v_0 = 50V, i_0 = 2A, C = 0.25\mu F, L = 40mH, R = 100\Omega$, *find (a)* $i_c(0), i_L(0)$, *and* $i_R(0)$ *(b)* $\frac{dv(0^+)}{dt}$ *(c)* $v(t)$.[12]

Solution: *This is relatively ease once you learn the concepts.*

[12] Verify the result via PSpice.

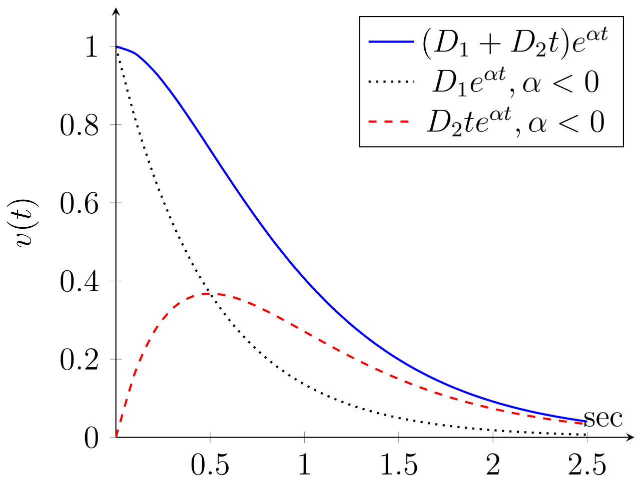


Figure 5.27: Time Response $y(t)$ for Equal Roots (Critically Damped Responses)

(a) $i_L(0) = 2A, i_R(0) = \frac{v(0)}{R} = \frac{50}{100} = 0.5A, i_C(0) = -i_L(0) - i_R(0) = -2.5A.$

(b) Since $i_C(0) = C\frac{dv(0)}{dt}$, *we have* $\frac{dv(0)}{dt} = \frac{i_C(0)}{C} = \frac{-2.5}{0.25\mu} = -10^7 V/s$

(c) $s_1, s_2 = -\frac{1}{RC} \pm \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}}, s_1 = -2679.5, s_2 = -37320.5.$ *Thus*

$$v(t) = A_1 e^{-2679.5t} + A_2 e^{-37320.5t}.$$

To find A_1 *and* A_2*, we solve the following simultaneous equations*

$$\begin{aligned} v(0) &= A_1 + A_2 = 50V \\ \frac{dv(0)}{dt} &= (-2679.5)A_1 + (-37320.5)A_2 = -10^7 V/s \end{aligned}$$

which yields $A_1 = -234.81, A_2 = 284.81$. *Therefore an overdamped solution is*

$$v(t) = -234.81e^{-2679.5t} + 284.81e^{-37320.5t} V, t \geq 0.$$

Example 5.11 (Underdamped Response) *Referring to Figure 5.24 with the following parameters:* $v_0 = 0$, $i_0 = -12.25mA$, $R = 20K\Omega$, $L = 8H$, *and* $C = 0.125\mu F$. *(a) Find* s_1 *and* s_2 *(b)* $v(t)$.
Solution: *Following the previous example, we obtain* $s_1, s_2 = -\frac{1}{2RC} \pm \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}} = -200 \pm j979.8$. *Thus*

$$\begin{aligned} v(t) &= A_1 e^{(-200+j979.8)t} + A_2 e^{(-200-j979.8)t} \\ &= e^{-200t}[(A_1 + A_2)\cos 979.8t + j(A_2 - A_1)\sin 979.8t] \\ &= e^{-200t}(B_1 \cos 979.8t + B_2 \sin 979.8t) \end{aligned}$$

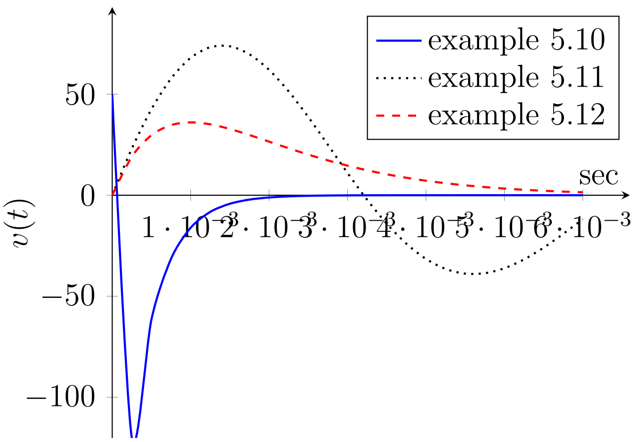


Figure 5.28: Time Response $v(t)$ for Examples 5.10-5.12

Now evaluate B_1 and B_2 by using the initial condition

$$\begin{aligned}
v_C(0^+) &= v_C(0^-) = 0 = B_1 \\
\frac{dv_C(0^+)}{dt} &= \frac{i_C(0^+)}{C} = \frac{1}{C}(-i_R(0^+) - i_L(0^+)) = \frac{1}{C}(-\frac{0}{20K} - (-12.25m)) = 98 \times 10^3 \\
&= -200B_1 + 979.8B_2.
\end{aligned}$$

Solving these simultaneous equations, we have $B_1 = 0, B_2 = 100$ and an underdamped solution is

$$v(t) = 100e^{-200t} \sin 979.8tV, \quad t \geq 0$$

□

Example 5.12 (Critically Damped Response) *Find R such that the circuit Figure 5.24 has critically damped response $v(t)$.*
[13] [14]

Solution: *We learn that for critically damped response $\alpha^2 = \omega_n^2$ must be satisfied. Thus the constraint $\frac{1}{2RC} = \sqrt{\frac{1}{LC}} = 10^3$ yields $R = 4K\Omega$. Moreover, for such response the solution form is*

$$v(t) = D_1te^{-1000t} + D_2e^{-1000t}V, \quad t \geq 0$$

To find D_1 and D_2, we, from initial condition, have

$$\begin{aligned}
v(0^+) &= D_2 = 0 \\
\frac{v(0^+)}{dt} &= D_1 + (-1000)D_2 = \frac{1}{C}(-i_R(0^+) - i_L(0^+)) = 98000V/s.
\end{aligned}$$

[13] Given the previous two examples, verify this exercise and plot the voltage solution via PSpice.
[14] Same exercise, let $R = 3K$, find the time response $v_C(t)$. What type of response is it?

Solving these simultaneous equations yields $D_1 = 98000, D_2 = 0$, *giving a critically damped solution*

$$v(t) = 98000te^{-1000t}V, \quad t \geq 0$$

□

Example 5.13 (Transient Behavior without External Force) *Using the following parameters:* $L = 0.5H, R = 400\Omega, C = 0.5\mu F, v_0 = 30V$, *find the initial conditions and expression of* $v(t)$[15].

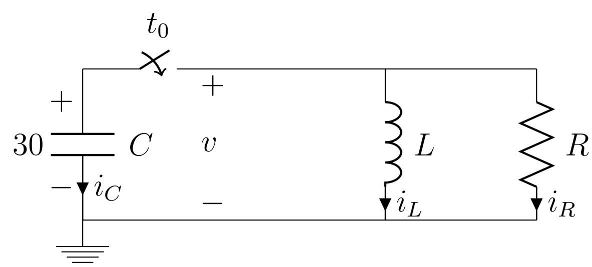


Figure 5.29: Example 5.13

Solution:

(a) Since v_C *could not change instantaneously so* $v(0^+) = v_C(0^-) = 30$, $i_R = v/R = 30/400 = 0.075A$. *Since* i_L *could not change instantaneously, thus* $i_L(0^+) = 0 = i_L(0^-)$. *Furthermore, KCL applied to the top node yields*

$$i_C + i_L + i_R = 0$$

giving

$$i_C(0^+) = -i_L(0^+) - i_R(0^+) = -0.075A$$

(b) $\frac{dv(0^+)}{dt} = \frac{i_C(0^+)}{C} = \frac{-0.075}{0.5\mu} = -150KV/s$

(c) KCL applied to the top node yields differential-integral form

$$0 = i_C + i_L + i_R = C\frac{dv}{dt} + \frac{1}{L}\int v(t)d\tau + \frac{v}{R}$$

Differentiating, we have

$$C\frac{d^2v}{dt^2} + \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v = 0, \quad (Cs^2 + \frac{1}{R}s + \frac{1}{L} = 0) \tag{5.10}$$

[15]Solve this exercise and plot time response via PSpice.

(d) $\Delta = (\frac{1}{2RC})^2 - \frac{1}{LC} = (\frac{1}{2 \cdot 400 \cdot 0.5\mu})^2 - (\frac{1}{0.5 \cdot 0.5 \times 10^{-6}}) = 2.25 \times 10^6 > 0$ *indicates an overdamped system.*

(e) *From (d), one solves for* $s_1 = -1000, s_2 = -4000$. *Thus the voltage expression is*

$$v(t) = A_1 e^{-1000t} + A_2 e^{-4000t} = -10e^{-1000t} + 40e^{-4000t} V, \quad t \geq 0$$

where A_1 *and* A_2 *are found by applying the initial condition obtained from (a)*

$$\begin{aligned} 30 &= A_1 + A_2 \\ -150,000 &= -1000A_1 - 4000A_2. \end{aligned}$$

To find an ODE in $i_L(t)$, *substitute* $v = L\frac{di_L}{di}$ *into (5.10) and follow the similar step you just learned.*

□

Series RLC circuit

Following the same notions for parallel circuit, we consider the following second-order series RLC circuit and derive the expression for current flowing in the circuit. KVL around the single loop

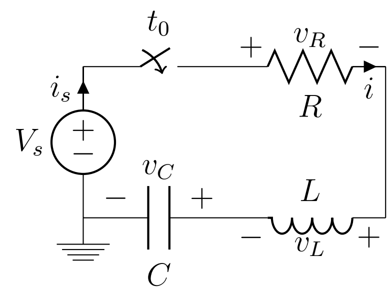


Figure 5.30: Series RLC Structure

clockwise yields

$$\begin{aligned} v &= v_R + v_C + v_L \\ &= iR + v_C + L\frac{di}{dt} && (5.11) \\ &= iR + \frac{1}{C}\int i(\tau)d\tau + L\frac{di}{dt}, \quad V = I(R + \frac{1}{Cs} + Ls) && (5.12) \\ &= (C\frac{dv_C}{dt})R + v_C + L\frac{d}{dt}(C\frac{dv_C}{dt}) && (5.13) \end{aligned}$$

Differentiating the ODE (5.12) yields

$$L\frac{d^2 i}{dt} + R\frac{di}{dt} + \frac{1}{C}i = 0$$

where the differential equation is expressed in terms of i which is i_L too. Can you find the time expression in v_C[16]? It is noted that the order of the highest derivative depends on the number of the energy-storage elements. Given (5.12), the characteristic equation is

$$Ls^2 + Rs + \frac{1}{C} = 0.$$

which has two roots

$$s_1, s_2 = -\frac{R}{2L} \pm \sqrt{(\frac{R}{2L})^2 - \frac{1}{LC}} = -\alpha \pm \sqrt{\alpha^2 - \omega_n^2} = -\alpha \pm j\omega_d$$

where w_n and w_d are defined as before. Thus, the general solution is

$$i(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}$$

where A_1 and A_2 are determined by initial conditions.

$$\begin{aligned} v_C(0^+) &= V_0, \quad \frac{dv_C(0^+)}{dt} = \frac{i_C(0^+)}{C}, \quad \text{if the ODE is expressed in } v_C \\ i_L(0^+) &= I_0, \quad \frac{di_L(0^+)}{dt} = \frac{v_L(0^+)}{L}, \quad \text{if the ODE is expressed in } i_L \end{aligned}$$

and the exponents s_1 and s_2 are determined by parameters R, L, C.

Interestingly enough, the Laplace transform (5.12) is the generalized Ohm's law ($V = IZ(s)$) we introduced when the impedance concepts was taught. The impedance concepts can be used to find the characteristic equation of the circuit.

Since having established the details in the parallel cases, we briefly summarize the results. For the second-order series RLC circuits, there are 3 possible root structures:

1. $\alpha^2 > \omega_n^2$. Overdamped response(Distinct real roots) $\Delta > 0$.

$$i(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}$$

2. $\alpha^2 < \omega_n^2$. Underdamped response (Complex roots) $\Delta < 0$.

$$i(t) = B_1 e^{-\alpha t} \cos \omega_d t + B_2 e^{-\alpha t} \sin \omega_d t$$

3. $\alpha^2 = \omega_n^2$. Critically damped response (Equal real roots) $\Delta = 0$

$$i(t) = D_1 t e^{-\alpha t} + D_2 e^{-\alpha t}.$$

Equipped with the analytical techniques, let's look into some examples to learn more about these.

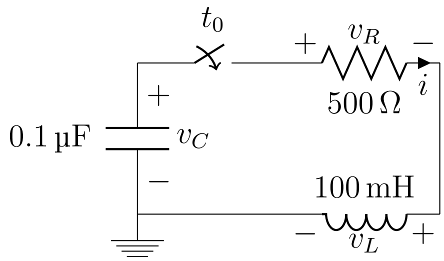


Figure 5.31: Example 5.14

Example 5.14 *Given the following circuit with $v_C(0) = 100V$, find (a) $i(t)$,(b) $v_C(t)$*[17]
Solution: *KVL applied to the single loop yields*

$$0 = v_R + v_C + v_L = iR + \frac{1}{C}\int i(\tau)d\tau + L\frac{di}{dt}$$

Differentiating, we have

$$L\frac{d^2i}{dt^2} + R\frac{di}{dt} + \frac{1}{C}i = 0, \quad (Ls^2 + Rs + \frac{1}{C} = 0) \tag{5.14}$$

whose characteristic values can be readily obtained

$$s_1, s_2 = -\frac{R}{2L} \pm \sqrt{(\frac{R}{2L})^2 - \frac{1}{LC}} = -2800 \pm j9600$$

resulting in

$$i(t) = e^{-2800t}(B_1 \cos 9600t + B_2 \sin 9600t)A.$$

Now to find B_1 and B_2, we utilize the initial condition found.

$$\begin{aligned} i(0^+) &= B_1 = 0 \\ \frac{di(0^+)}{dt} &= \frac{v_C(0^+)}{L} = \frac{100}{100} \times 10^3 = 10^3 = 9600B_2. \end{aligned}$$

Solving these simultaneous equations leads to

$$B_2 = 0.1042$$

giving

$$i(t) = 0.1042e^{-2800t} \sin 9600tA, \quad t \geq 0$$

and

$$\begin{aligned} v_C(t) &= \frac{1}{C}\int i(\tau)d\tau + V_0 = -iR - L\frac{di}{dt} \\ &= e^{-2800t}(100 \cos 9600t + 29.17 \sin 9600t)V, \quad t \geq 0. \end{aligned} \tag{5.15}$$

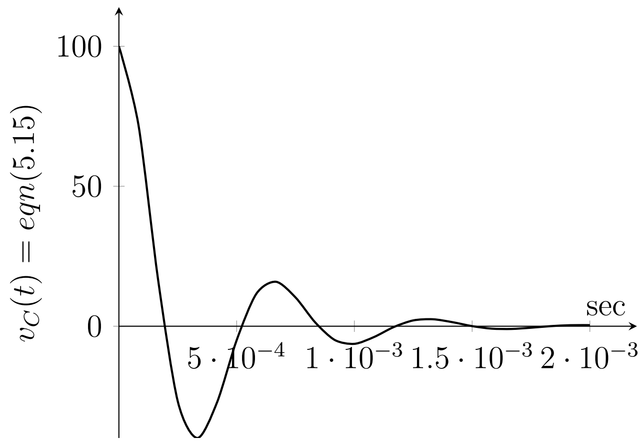


Figure 5.32: Time Response $v_C(t)$ for Example 5.14

To find an ODE in $v_C(t)$, substitute $i = C\frac{dv_C}{di}$ into (5.14) and follow the similar step you just learned.

□

Example 5.15 *Given the following circuit, find the initial condition and the current $i(t)$ after the switch is flipped to position 2.*[18].

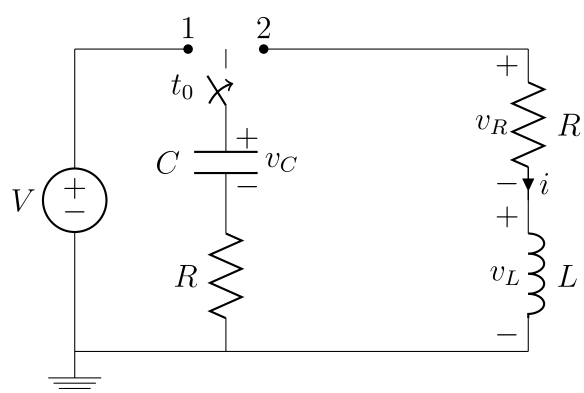


Figure 5.33: Example 5.15

Solution:

[16]Following the notions depicted in parallel RLC circuit, derive the second-order differential equation expressed in v_C.

[17]Solve this exercise and plot time response via PSpice/MATLAB.

[18]Find the time expression i_C when switch is at position 1 (Assume v_C initially rest)and plot time response via PSpice/MATLAB.

(a) $v_C(0^+) = v_C(0^-) = V$ *because* C *is open.*
$i(0^+) = i(0^-) = 0$ *because* $i_L(0) = 0$
$v_L(0^+) = v_C(0^+) = V$ *because* $i(0^+) = 0$ *implies* $v_R(0^+) = 0$.

(b) KVL *around the right-hand loop yields*

$$v_R + v_C = v_R + v_L, \quad \textit{voltage rises =voltage drops}$$

leading to

$$-iR + \underbrace{-(\frac{1}{C}\int i(\tau)d\tau)}_{v_C} = Ri + L\frac{di}{dt}, \quad 0 = (\frac{1}{Cs} + 2R + Ls)i \tag{5.16}$$

$$-(C\frac{dv_C}{dt})R - v_C = R(C\frac{dv_C}{dt}) + L\frac{d}{dt}(C\frac{dv_C}{dt}), \quad 0 = (2RCs + 1 + LCs^2)v_c. \tag{5.17}$$

Differentiating equation (5.16)[19], *we obtain*

$$L\frac{d^2i}{dt^2} + 2R\frac{di}{dt} + \frac{1}{C}i = 0, \quad (Ls^2 + 2Rs + \frac{1}{C} = 0).$$

Thus the general form is

$$i(t) = A_1e^{s_1t} + A_2e^{s_2t}A, \quad t \geq 0.$$

To find A_1 *and* A_2, *start with initial condition*

$$\begin{aligned} i(0^+) &= 0 = A_1 + A_2 \\ \frac{di(0^+)}{dt} &= \frac{v_L(0^+)}{L} = \frac{V}{L} = A_1s_1 + A_2s_2 \end{aligned}$$

□

5.3.3 Forced systems

To understand forced response, the key notions is better served by examples. To ease the presentation, the examples are categorized into to categories.

Parallel RLC **circuits**

Example 5.16 *Given the following parallel* RLC *circuit with an external current source, find* $i_L(t)$.

Solution: KCL *applied to the top node yields*

$$24 \times 10^{-3} = C\frac{dv}{dt} + \frac{v}{R} + i_L. \tag{5.18}$$

[19] An ODE in v_C is readily obtained

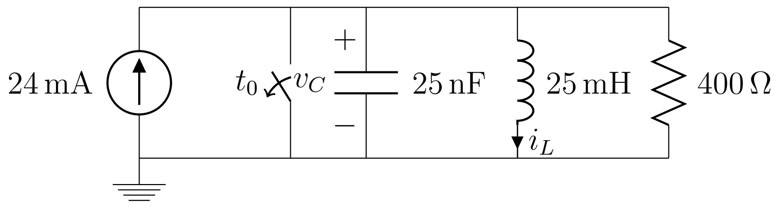


Figure 5.34: Example 5.16

Substituting $v = L\frac{di_L}{dt}$ *into the equation (5.18) gives*

$$24 \times 10^{-3} = LC\frac{d^2 i_L}{dt^2} + \frac{L}{R}\frac{di_L}{dt} + i_L, \quad (LCs^2 + \frac{L}{R}s + 1 = 0)$$

which is an ODE expressed in terms of inductor current $i_L(t)$. *Alternatively, one can substitute* $i_L = \frac{1}{L}\int v(\tau)\ d\tau$ *into the equation (5.18) and yields*

$$24 \times 10^{-3} = C\frac{dv}{dt} + \frac{v}{R} + \frac{1}{L}\int_0^t v(\tau)\ d\tau + i_L(0).$$

Differentiating, we have

$$0 = C\frac{d^2 v}{dt^2} + \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v, \quad (Cs^2 + \frac{1}{R}s + \frac{1}{L} = 0)$$

whose characteristic values are $s_1 = -20000$ *and* $s_2 = -80000$, *giving*

$$v(t) = A_1 e^{-20000t} + A_2 e^{-80000t} V, \quad t \geq 0.$$

To find the coefficients, initial condition leads to

$$\begin{aligned} v(0^+) &= v_C(0) = 0 = A_1 + A_2 \\ \frac{dv(0^+)}{dt} &= \frac{i_C(0^+)}{C} = \frac{1}{C}(24 \times 10^{-3} - i_R(0^+) - i_L(0^+)) = 24 \times 10^{-3}/25 \times 10^{-9} \\ &= 960000 = -20000A_1 - 80000A_2. \end{aligned}$$

Solving these simultaneous equation, we have $A_1 = 16$ *and* $A_2 = -16$, *resulting in*

$$v(t) = 16e^{-20000t} - 16e^{-80000t} V, \quad t \geq 0.$$

To find i_L *(5.18) implies* $i_L = 24 \times 10^{-3} - C\frac{dv}{dt} + \frac{v}{R}$ *or by formula*

$$i_L = \frac{1}{L}\int_0^t v(\tau)\ d\tau + i_L(0) = -32e^{-20000t} + 8e^{-80000t} + 24 \quad mA, \quad t \geq 0. \tag{5.19}$$

□

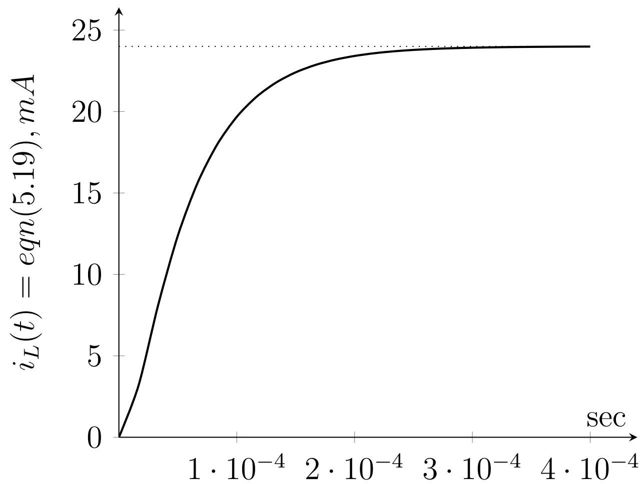


Figure 5.35: Time Response $i_L(t)$ for Example 5.16

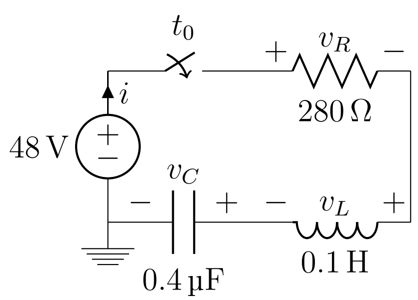


Figure 5.36: Example 5.17

Series RLC circuits

Example 5.17 *Given the following series RLC circuit with an external voltage, find its current.*
Solution: *KVL around the single loop yields*[20]

$$48 = 280i + 0.1\frac{di}{dt} + \underbrace{\frac{1}{0.4\mu}\int i(\tau)d\tau}_{v_C}\,. \tag{5.20}$$

Differentiating yields

$$0 = 0.1\frac{d^2i}{dt^2} + 280\frac{di}{dt} + \frac{1}{0.4\mu}i, \quad (0.1s^2 + 280s + \frac{10^7}{4})$$

whose characteristic values are $-1400 \pm j4800$ *and the natural response is*

$$i(t) = e^{-1400t}(B_1 \cos 4800t + B_2 \sin 4800t), \quad t \geq 0.$$

[20]Substituting i with $C\frac{v_C}{dt}$ leads to an ODE in terms of v_C. Then verify and plot $v_C(t)$ via PSpice/MATLAB in a similar fashion as the previous exercise.

As before, to find coefficients via initial condition leads to

$$\begin{aligned} i(0^+) &= 0 = B_1 \\ \frac{i(0^+)}{dt} &= \frac{v_L(0^+)}{L} = \frac{1}{0.1}(48 - v_R(0^+) - v_C(0^+)) = 480 = -1400B_1 + 4800B_2V. \end{aligned}$$

Solving these simultaneous equations, we have $B_1 = 0, B_2 = 0.1$, *yielding*

$$i(t) = 0.1e^{-1400t}\sin 4800tA, \quad t \geq 0.$$

To find v_C

$$\begin{aligned} v_C &= \frac{1}{C}\int_0^t i(\tau)\ d\tau + v_C(0) \\ &= 48 - 48e^{-1400t}\cos 4800t - 14e^{-1400t}\sin 4800tV, \quad t \geq 0. \end{aligned} \tag{5.21}$$

Notice that you could also obtain v_C *from (5.20) which says that* $v_C = 48 - 280i - 0.1\frac{di}{dt}$.

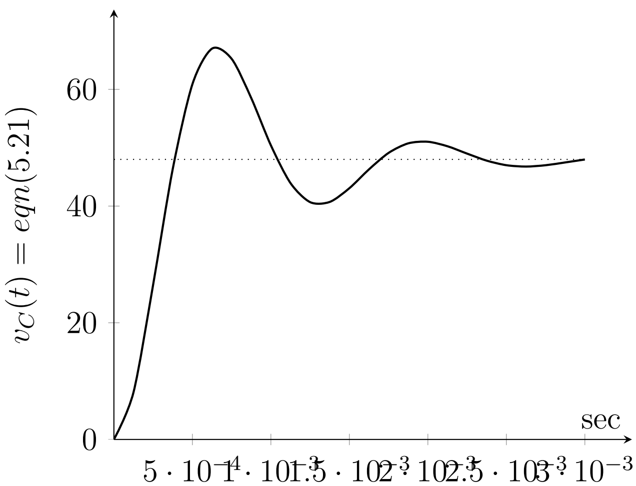


Figure 5.37: Time Response $v_C(t)$ for Example 5.17

□

Example 5.18 *Given the following series RLC circuit with an external voltage source, find the voltage across the capacitor*[21]. *Assume* $R = 300$ *and an initially rest system.*
Solution: *KVL leads to*

$$10 = 10 \times 10^{-3}\frac{di}{dt} + Ri + v_C.$$

Substituting $i = C\frac{dv_C}{dt} = 10^{-6}\frac{dv_C}{dt}$ *into the equation above, we have*

$$10 = 10^{-8}\frac{d^2v_C}{dt} + R \cdot 10^{-6}\frac{dv_C}{dt} + v_C$$

[21]Verify and plot the voltage via PSpice/MATLAB.

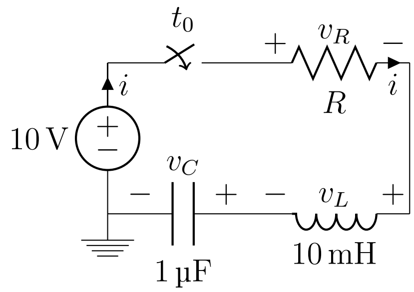


Figure 5.38: Example 5.18

whose characteristic equation yields $s_1 = -2.618 \times 10^4, s_2 = -0.3820 \times 10^4$. *Therefore,*

$$v_C(t) = 10 + A_1 e^{-2.618\times 10^4 t} + A_2 e^{-0.3820\times 10^4 t}.$$

Applying initial condition to find the coefficient results in

$$\begin{aligned} v_C(0^+) &= 0 = 10 + A_1 + A_2 \\ \frac{dv_C(0^+)}{dt} &= \frac{i(0^+)}{C} = 0 = -2.618 \times 10^4 A_1 - 0.3820 \times 10^4 A_2. \end{aligned}$$

Solving these simultaneous equations, we have $A_1 = 1.708$ *and* $A_2 = -11.708$. *Thus,*

$$v_C(t) = 10 + 1.708 e^{-2.618\times 10^4 t} - 11.708 e^{-0.3820\times 10^4 t}, t \geq 0. \tag{5.22}$$

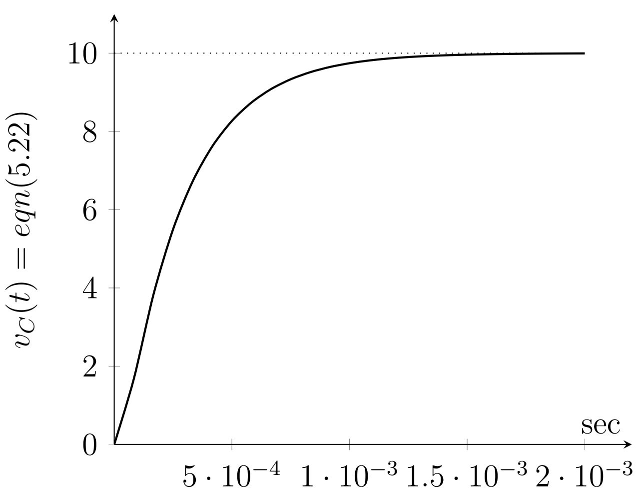


Figure 5.39: Time Response $v_C(t)$ for Example 5.18

□

Example 5.19 *Given the following series RLC circuit with an AC voltage source, find the current* $i(t)$[22].

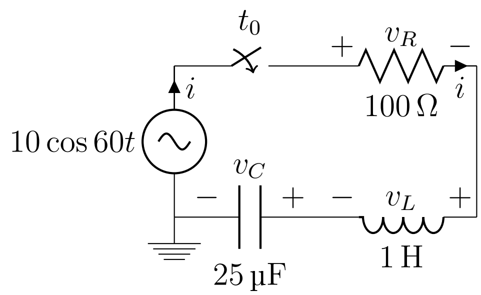


Figure 5.40: Example 5.19

Solution: *KVL yields*

$$10\cos 60t = 100i + \frac{di}{dt} + \frac{10^6}{25}\int_0^t i(\tau)d\tau.$$

Differentiating gives

$$-10\times 60\sin 60t = \frac{d^2i}{dt} + 100\frac{di}{dt} + \frac{10^6}{25}i, \quad (s^2+100s+40000=0)$$

whose characteristic values are $-50 \pm j193.6$ *and the corresponding natural response is*

$$i(t) = e^{-50t}(B_1\cos 193.6t + B_2\sin 193.6t)mA, \quad t \ge 0.$$

Now find the steady-state response via phase concept

$$\bar{I} = \frac{10\angle 0^\circ}{614.85\angle -80.64^\circ} = 0.0163\angle 80.64^\circ, \quad i_f(\infty) = 16.3\cos(60t+80.64^\circ)mA.$$

Thus the total response is

$$i(t) = 16.3\cos(60t+80.64^\circ) + e^{-50t}(B_1\cos 193.6t + B_2\sin 193.6t), \quad t\ge 0.$$

Given the initial condition, the undetermined coefficients are determined from

$$\begin{aligned} i(0^+) &= 0 = 0.0026 + B_1 \\ \frac{di(0^+)}{dt} &= \frac{v_L(0^+)}{L} = \frac{1}{L}(v_s(0^+) - v_R(0^+) - v_C(0^+)) = 10 = -0.9650 - 50B_1 + 193.6B_2 \end{aligned}$$

yielding $B_1 = -0.00265$ *and* $B_2 = 0.0043$. *Therefore*

$$i(t) = 16.3\cos(60t+80.64^\circ) + e^{-50t}(-2.65\cos 193.6t + 4.3\sin 193.6t)mA, t\ge 0. \tag{5.23}$$

[22] Verify and plot the current via PSpice/MATLAB.

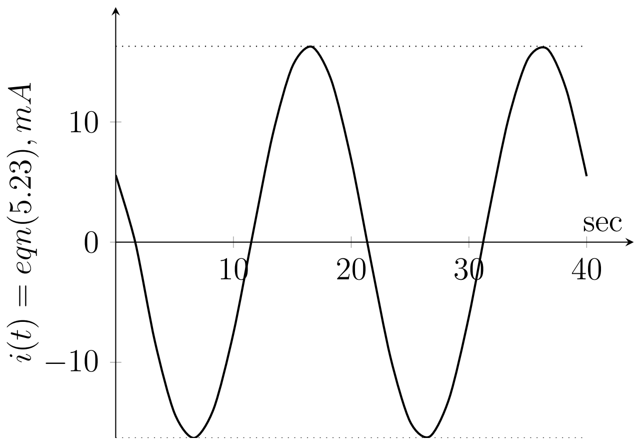


Figure 5.41: Time Response $i(t)$ for Example 5.19

□

Example 5.20 *Given the following series RLC circuit with an AC voltage source, find the current response when the switch is closed*[23].

Solution

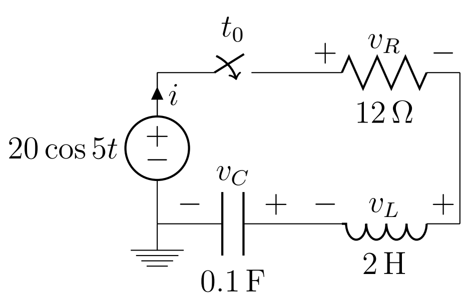


Figure 5.42: Example 5.20

KVL yields

$$20\cos 5t = 12i + 2\frac{di}{dt} + 10\int_0^t i(\tau)d\tau$$

Differentiating gives

$$-100\sin 5t = 2\frac{d^2i}{dt} + 12\frac{di}{dt} + 10i, \quad (s^2 + 6s + 5 = 0).$$

whose characteristic equations gives $s_1 = -1$ *and* $s_2 = -5$*, leading to the natural response*

$$i_n(t) = A_1e^{-t} + A_2e^{-5t}A, \quad t \geq 0.$$

[23]Verify and plot the current via PSpice/MATLAB.

Use phasor concept to find steady-state solution

$$i_f(\infty) = R_e(\frac{20\angle 0°}{12 + j8}) = 1.39\cos(5t - 33.69)A.$$

Thus the total response becomes

$$i(t) = 1.39\cos(5t - 33.69°) + A_1 e^{-t} + A_2 e^{-5t} A, \quad t \geq 0.$$

Use initial conation to find coefficients A_1 *and* A_2

$$\begin{aligned} i(0^+) &= 0 = 1.16 + A_1 + A_2 \\ \frac{di(0^+)}{dt} &= \frac{v_L(0^+)}{L} = \frac{1}{L}(20 - 0 - 0) = 10 = 3.86 - A_1 - 5A_2. \end{aligned}$$

Solving these simultaneous equations, we have $A_1 = 0.086$ *and* $A_2 = -1.25$, *yielding*

$$i(t) = 1.39\cos(5t - 33.69°) + 0.086e^{-t} - 1.25e^{-5t} A, \quad t \geq 0. \tag{5.24}$$

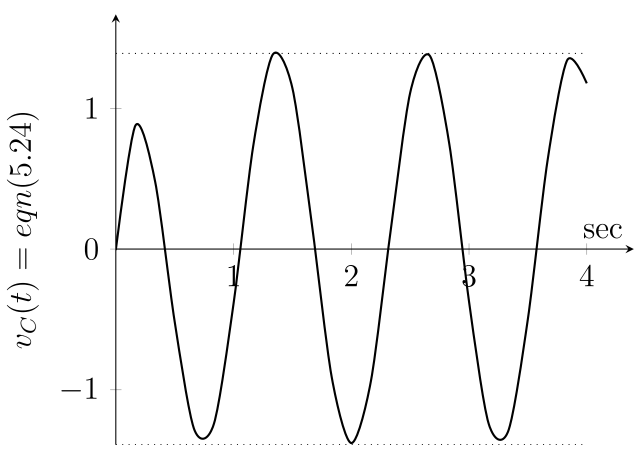


Figure 5.43: Time Response $i(t)$ for Example 5.20

□

5.3.4 Solving procedures for the second-order systems

The following is a general procedure for solving a RLC circuit whose electrical signal is expressed in the form of

$$a\ddot{x} + b\dot{x} + cx = f, \quad \frac{dx(0)}{dt} \text{ and } x(0).$$

Elements	R	L	C	Type of Impedances
$\bar{Z}(s)$	R	Ls	$1/Cs$	Exponential impedance
$\bar{Z}(0)$	R	0	∞	DC impedance
$\bar{Z}(j\omega)$	R	$j\omega L$	$1/j\omega C$	AC impedance

Table 5.2: Table of Resistance

where x can be either $i(t)$ or $v(t)$. The solution has two components: natural response and particular response.

$$\begin{aligned} x(t) &= x_n(t, A_1, A_2) + x_p(t) \\ &= x_{transient} + x_{steady-state} \\ &= x_{natural} + x_{forced} \end{aligned}$$

1. Fine the appropriate ordinary differential equation by applying KCL or KVL.

2. Determine the forced response, $x_f(t)$

   a) For DC case, use $Z(0)$ and $V = IR$ (Ohm's low)

   b) For AC case, use $\bar{Z}(j\omega)$ and $\bar{V} = \bar{I}\bar{Z}$ (Phasor technique)

3. Identify the natural response, $x_n(t, A_1, A_2)$

$$x_n(t, A_1, A_2) = A_1 e^{s_1 t} + A_2 e^{s_2 t}, \quad t \geq 0$$

4. $x(t) = x_n(t, A_1, A_2) + x_f(t)$ and evaluate the undetermined coefficients from initial conditions

$$\begin{aligned} \frac{dv_C(0^+)}{dt} &= \frac{i_C(0^+)}{C} = \frac{1}{C}(i_s(0^+) - i_R(0^+) - i_L(0^+)), \quad v_C(0^+) = v_0 \\ \frac{di_L(0)^+}{dt} &= \frac{v_L(0^+)}{L} = \frac{1}{L}(v_s(0^+) - v_R(0^+) - v_C(0^+)), \quad i_L(0^+) = i_0 \end{aligned}$$

5. What if a complicated circuit was given? Use Thevenin or Norton equivalent notions.
   So this is it. You have gone through the first-order and second-order differential equations that characterize the dynamic behaviors of electrical circuits.

5.4 Problems

Problem 5.1 *In the figure for problem 5.44, the switch has been closed for a long time and is opened at $t = 0$. (a) Calculate the initial value of current i. (b) Calculate the initial energy stored in the inductor. (c) What is the time constant of the circuit for $t > 0$? (d) What is the numerical expression for $i(t)$ for $t \geq 0$? (e) what percentage of the initial energy stored has been dissipated in the 4Ω resistor 5 ms after the switch has been open?*

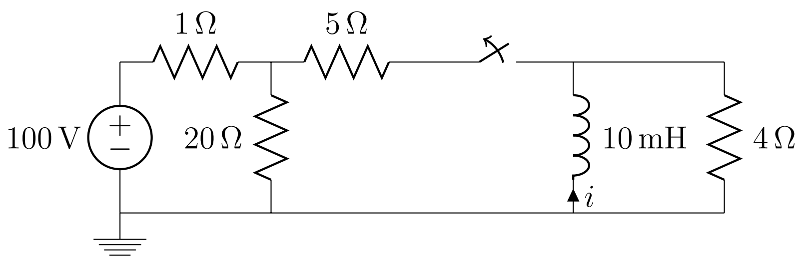


Figure 5.44: Circuit Diagram for Problem 5.1

Answer: *(a) -16A. (b) 1.28J. (c)* 2.5×10^{-3}. *(d)* $i(t) = -16e^{-400t}A, t \geq 0$. *(e)* 98.17%.

Problem 5.2 *Consider a series RL circuit with $R = 4\Omega$ and $L = 2H$, excited by a voltage source $v(t) = 10e^{-2t}\cos 5tV$. (a) Draw the circuit. (b) Find the impedance seen by the source. (c) Determine a time-domain expression for the series current.*
Answer: *(a) Trivial. A R in series with an L (b) $\bar{Z} = 10\angle - 90°\Omega$. (c) $i(t) = e^{-2t}\cos(5t - 90°A$*

Problem 5.3 *The circuit shown in problem 5.45 is operating in steady-state with the switch open prior to $t = 0$. Find the time expression for $i(t) < 0$ and for $t \geq 0$. Sketch $i(t)$ to scale versus time.*

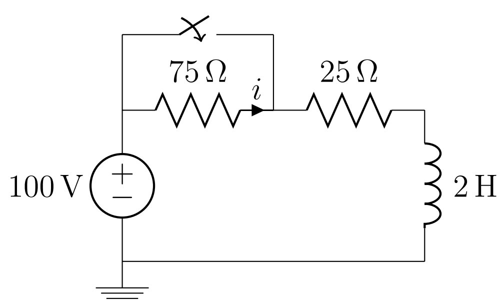


Figure 5.45: Circuit Diagram for Problem 5.3

Answer: *(a) $i(t) = 1A$, $\forall t < 0$. (b) $i(t) = 4 - 3e^{-12.5t}A, \forall t \geq 0$. (c) Curve exponentially grows from -1 to 4A.*

Problem 5.4 *Find the steady-state values of i_1, i_2 and i_3 for the circuit of Figure 5.46.*
Answer: $i_1 = 0A, i_2 = i_3 = 2A$.

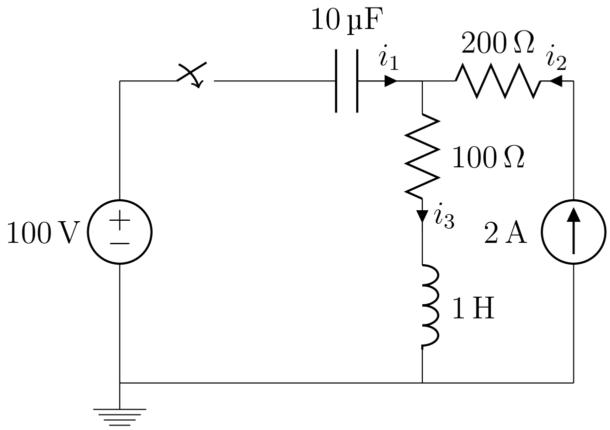


Figure 5.46: Circuit Diagram for Problem 5.4

Problem 5.5 *Consider the circuit of Figure 5.47, in which the switch opens at $t = 0$. Find the time expression for $v(t)$, $i_R(t)$ and $i_L(t)$ for $t > 0$. Assume that $i_L(0) = 0$ before the switch opens.*

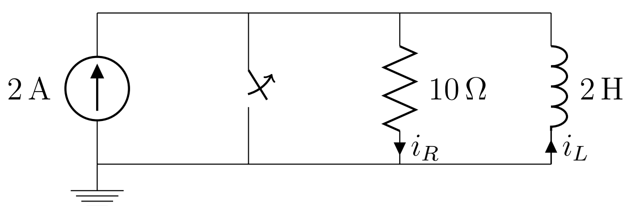


Figure 5.47: Circuit Diagram for Problem 5.5

Answer: $v(t) = 20e^{-5t}V, t \geq 0$, $i_R(t) = 2e^{-5t}A, t \geq 0$ *and* $i_L(t) = 2 - 2e^{-5t}A, t \geq 0$.

Problem 5.6 *Given the circuit of Figure 5.48, find (a) the natural response and the forced response. (b) Evaluate the initial conditions, $i(0), \frac{di(0)}{dt}$. (c) Solve for the complete current response $i(t)$. (d) At what frequency, does the response oscillate? (e) To what value should R be changed to so that the response becomes critically damped.*

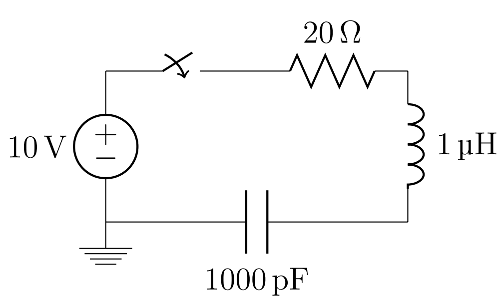


Figure 5.48: Circuit Diagram for Problem 5.6

Answer: *(a)* $i_n(t) = e^{-10^7 t}(B_1 \cos 3\times 10^7 t + B_2 \sin 3 \times 10^7 t)$, $i_f(t) = 0$ *(b)* $i(0) = 0$, $\frac{di(0)}{dt} = -10^7$. *(c)* $i(t) = \frac{1}{3}e^{-10^7 t}\sin(3\times 10^7 t)A, t \geq 0$ *(d)* 3×10^7 *rad/s (e)* $R = 63.25\Omega$.

Problem 5.7 *The resistor in the circuit shown in 5.49 is adjusted for critical damping and the initial energy stored in the circuit is* $25mJ$*, distributed equally in the inductor and capacitor. Find (a)* I_0 *(b)*V_0 *(c)*R *(d)* $v(t), t \geq 0$.

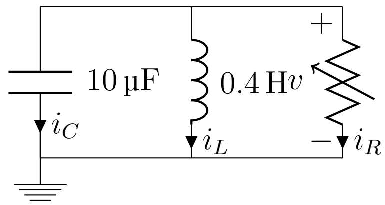


Figure 5.49: Circuit Diagram for Problem 5.7

Answer: *(a)* $i_0 = 0.25mA$. *(b)* $v_0 = 50V$. *(c)* $R = 100\Omega$. *(d)* $v(t) = 50e^{-500t} - 50000te^{-500t}V, t \geq 0$

Problem 5.8 *Given the circuit of Figure 5.50, find (a) the voltage across the capacitor when* $t = \infty$. *(b)Find the characteristic equation in s. (c) Solve for the complete current response* $v_C(t)$.

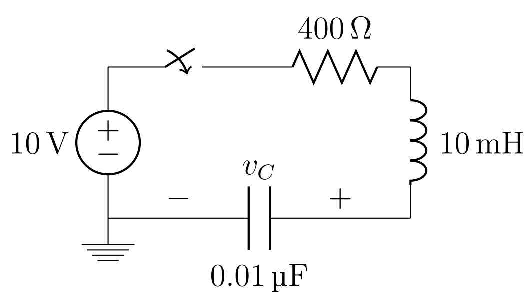


Figure 5.50: Circuit Diagram for Problem 5.8

Answer: *(a)* $v_C(\infty) = 10V$, $i_f(t) = 0$. *(b)* $10^{-2}s^2 + 400s + 10^8$. *(c)* $v_C(t) = 10 + e^{-2\times 10^4 t}[-10\cos 97900t - 2.04 \sin 97900tV, t \geq 0$.

Problem 5.9 *Given the circuit of Figure 5.51, find (a) the initial current flowing into inductor* $t = 0^+$. *(b) find the final current flowing in inductor* $i_L(\infty)$. *(c) Solve for the complete current response* $i_L(t)$. *(c)* $i_L(t) = 5.71 + 5.64e^{-\frac{t}{17.1\times 10^{-3}}}, t \geq 0$.
Answer: *(a)* $i_L(0^-) = i_L(0^+) = 66.5mA$. *(b)* $i_L(\infty) = 5.71A$.

Problem 5.10 *In the circuit of Figure 5.52, switch* S_1 *has been in position a and switch* S_2 *has been closed for a long time before* $t = 0$. *The* $2\mu F$ *capacitor is initially uncharged. (a) For* $t = 0^-$, *find* i_L, v_L, i_{C2} *and* v_{C1}. *(b) At* $t = 0$, *switch* S_1 *is flip to position 2 and switch* S_2 *is opened. For* $t = 0^+$, *find* i_R, v_R, v_{C2} *and* v_L. *(c) For* $t = 0^+$, *find* $\frac{di_R}{dt}$, $\frac{dv_{C1}}{dt}$.
Answer: *(a)* $i_L = 0.1A$, $v_L = 0V$, $i_{C2} = 0A$, $v_{C1} = 60V$. *(b)* $i_R = 0.1A$, $v_R = -30V$, $v_{C2} = 0V$, $v_L = 30V$. *(c)* $\frac{di_R}{dt} = -600A/s$, $\frac{dv_{C1}}{dt} = -10^5V/s$.

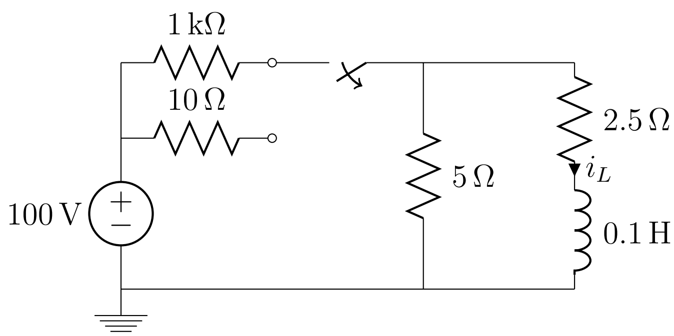


Figure 5.51: Circuit Diagram for Problem 5.9

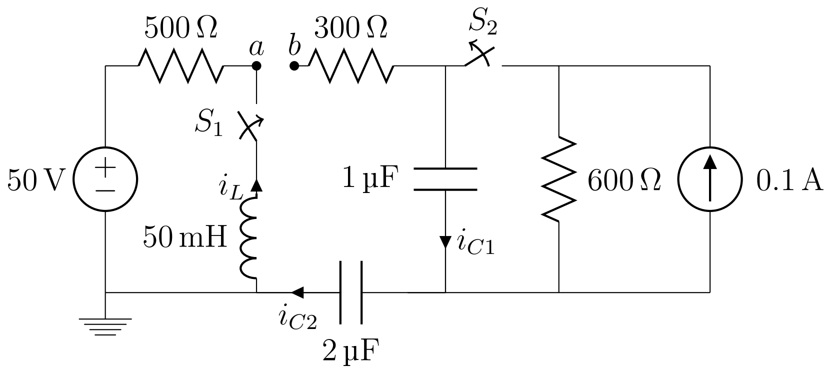


Figure 5.52: Circuit Diagram for Problem 5.10

Problem 5.11 *In the circuit of Figure 5.53, the switch is closed for a long time and opened at* $t = 0$. *(a) Determine* v_C *and* $\frac{dv_C}{dt}$ *at* $t = 0^+$. *(b) Find the impedance* $\bar{Z}_{ab}$. *(c) Determine* i_C.

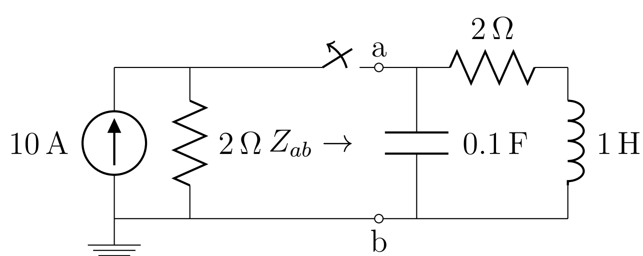


Figure 5.53: Circuit Diagram for Problem 5.11

Answer: *(a)* $v_C(0^+) = 10V$, $\frac{dv_C(0^+)}{dt} = -50V/s$ *(b)* $\bar{Z}_{ab}(s) = \frac{20+10s}{s^2+2s+10}$ *(c)* $i(t) = e^{-t}(B_1 \cos 3t + B_2 \sin 3t), t \geq 0A$.

Problem 5.12 *Given the circuit of Figure 5.54, (a) find the initial condition* $i(0)$ *and* $v(0)$ *before and after the switch open, (b) find the ODE of* $v(t)$, *(c) find the complete solution of* $v(t)$, *(d) find the complete solution of* $i_L(t)$. *(3) Draw* $i(t)$ *and* $v(t)$ *respectively.*

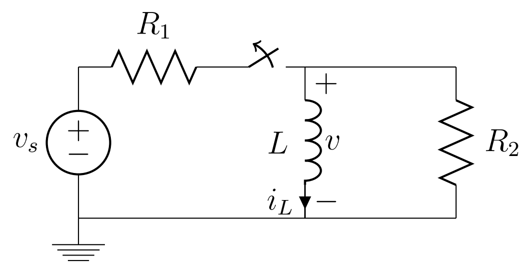


Figure 5.54: Circuit Diagram for Problem 5.12

Answer: *(a)* $v(0^-) = 0$, $v(0^+) = -\frac{V_s R_2}{R_1}$. *(b)* $\frac{dv}{dt} + \frac{R_2}{L}v = 0$, $v(t) = -\frac{V_s R_2}{R_1}e^{\frac{-R_2}{L}t, t\geq 0}$. *(c) (d)* $i_L(t) = \frac{V_s}{R_1}e^{\frac{-R_2}{L}t, t\geq 0}$. *(e) exponentially increases and decreases, respectively (setting t=0 and t=∞, respectively to see the trend.)*

Problem 5.13 *Given the circuit of Figure 5.55, (a) when the switch is closed, find the ODE of the inductor current using equivalent technique. (b) Determine the inductor current* i_L *and resistor current* i_R *for* $t > 0$*. (b) Plot the time response.*

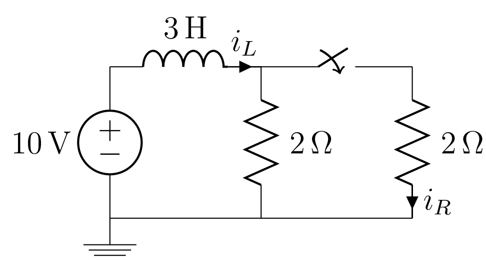


Figure 5.55: Circuit Diagram for Problem 5.13

Answer: *(a)* $3\frac{di}{dt} + i = 10$. *(b)* $i_L(t) = 10 - 5e^{-0.333t}A$, $i_R(t) = 5 - 2.5e^{-t/3}A$.

Transient response–the first-order systems

Problem 5.14 *Given the circuit shown in Figure 5.56, (a) Find initial* $i_L(0)$ *before the switch*

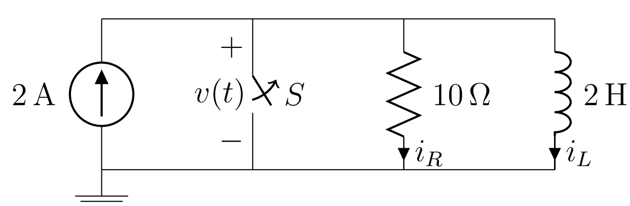


Figure 5.56: Circuit Diagram for Problem 5.14

opens. (b) Find expressions for $v(t)$, $i_R(t)$ *and* $i_L(t), \forall t > 0$.
Answer: *(a)* $i_L(0) = 2A$, *(b)* $i_L(t) = 2$, $i_R(t) = 0$, $v_L(t) = 0$.

Problem 5.15 *Solve for the current in the circuit shown in Figure 5.57 after the switch closes. Assuming $v_C(0) = 5V$, (a) find the natural response. (b) Find the forced response. (Hint: try a particular solution of the form Ae^{-t})*

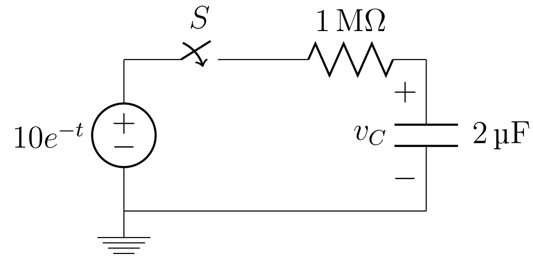


Figure 5.57: Circuit Diagram for Problem 5.15

Answer: $i_n(t) = -15e^{-\frac{t}{2}}$, $i_p(t) = 20e^{-t}$.

Problem 5.16 *At $t = 0$, a charged $10\mu F$ capacitance is connected to a resistor as shown in Figure 5.58. At $t = 0$, the resistor voltage is 50V. At $t = 30sec$, the resistor voltage is 25V. (a) Find the transient response in terms of R and C for $t > 0$. (b) Find the resistance R.*

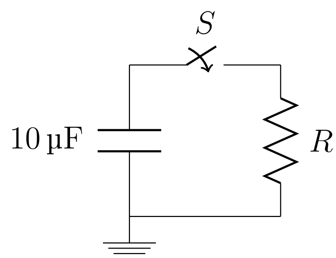


Figure 5.58: Circuit Diagram for Problem 5.16

Answer: *(a)* $v_C = v_i e^{-\frac{t}{RC}}$, *(b)* $R = 4.328M\Omega$.

Problem 5.17 *Given Figure 5.59, with $R = 2ohm$, $C = 5F$ and $I = 10A$. (1) Find the expression for the capacitor voltage $v_C(t)$ and $i_C(t)$. (2) Plot both functions.*

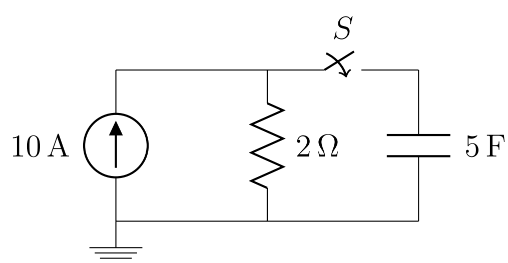


Figure 5.59: Circuit Diagram for Problem 5.17

Answer:

Problem 5.18 *For the circuit of Figure 5.60, answer the following questions. (a) What is the time constant (after the switch opens)? (b) What is the maximum magnitude of $v(t)$? (c) How does the maximum magnitude of $v(t)$ compare to the source voltage? (d) Find the time t at which $v(t)$ is one-half of its value immediately after the switch opens.*

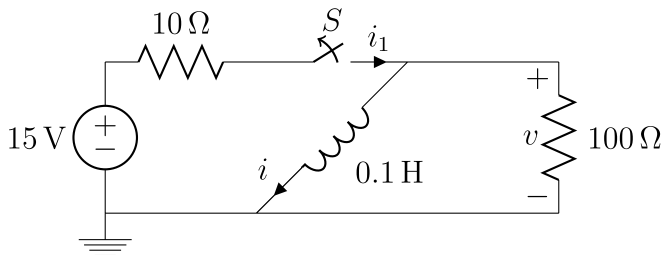


Figure 5.60: Circuit Diagram for Problem 5.18

Answer: *(a) $\tau = 1ms$ (b) $v_{max} = 150V$ (c) 10 times the value of v_s. (d) 0.6931 ms.*

Problem 5.19 *Given Figure 5.61, (1) find the complete solution for the inductor $i_L(t)$. (2) Find voltage across 6Ω resistor.*

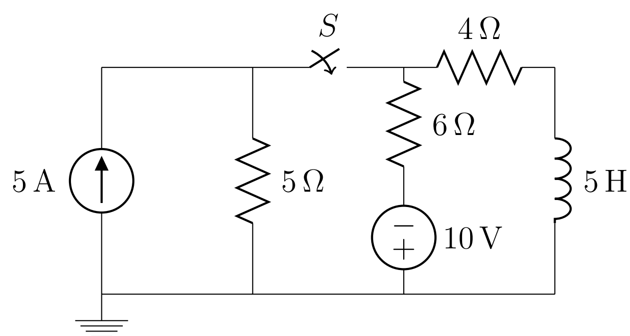


Figure 5.61: Circuit Diagram for Problem 5.19

Answer:

Problem 5.20 *Given the circuit of Figure 5.62. Switch S is closed for a long time and then open at $t = 0$. (a) Determine the initial values of i_1 and i_2 at $t = 0^+$. (b) Find the current expression for $i_2(t)$.*
Answer: $i_2(0^+) = i_2(0^-) = 2A$, $i_1(0^+) = -i_1(0^+) = -2A$, $i_2(t) = 2e^{-3t}A$.

Problem 5.21 *The circuit shown in Figure 5.63 is operating in steady state with the switch open prior to $t = 0$. Find expressions for $i(t)$ for $t < 0$ and for $t \geq 0$.*
Answer: *The steady state value is $1A$, $t < 0$, $i(t) = 4 - 3e^{-12.5t}A, t \geq 0$.*

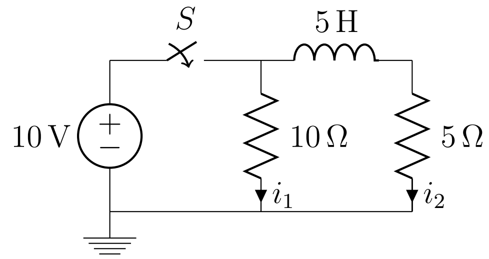


Figure 5.62: Circuit Diagram for Problem 5.20

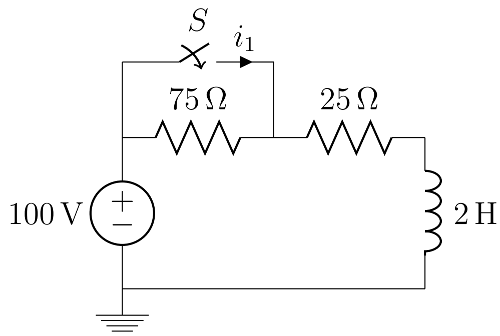


Figure 5.63: Circuit Diagram for Problem 5.21

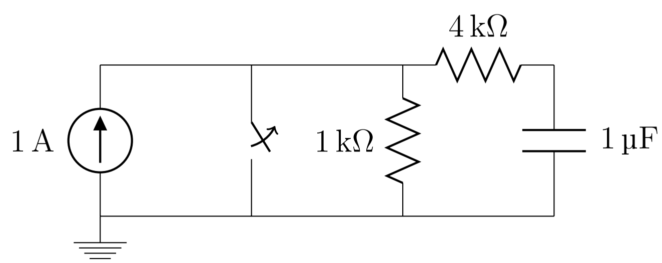


Figure 5.64: Circuit Diagram for Problem 5.22

Problem 5.22 *Given the circuit 5.64, (a) use source transformation converting current source into voltage source. (b) Use KVL to find the ODE for $v_C(t)$. (c) Find the steady-state response. (d) Find the natural response and (e) the complete solution.*
Answer: *(a) skip. (b) $s = -200$. (c) $i_C(\infty) = 0$. (d) $i_H(t) = Ae^{-200t}$. (e) $i_C(t) = 0.2e^{-200t}A$.*

Problem 5.23 *Give the circuit 5.65, (a) What is the steady-state inductor current due to 24V and 8A, respectively, right before the switch is open. (b) Use KVL to find the ODE for $i_L(t)$ after the switch is open. (c) Find the natural response . (d) Find the complete response. (e)Draw the complete response $i_L(t)$ where t is the x axis.*
Answer: *(a) $i_L(0) = 4A$. (b) (c) $i_n(t) = Ae^{-10t}$. (d) $i(t) = 12 - 8e^{-10t}A$.*

Problem 5.24 *Given Figure 5.66 and assume that the switch has been closed for a very long time prior to $t = 0$. (a) Derive the ODE for $i(t)$ and $v(t)$.(b)Find expressions for $i(t)$ and $v(t)$.*

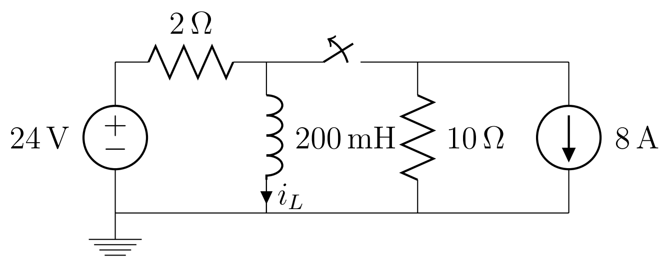


Figure 5.65: Circuit Diagram for Problem 5.23

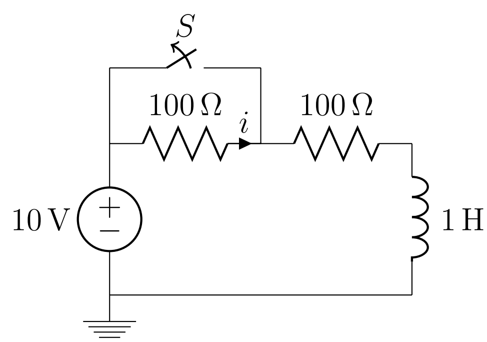


Figure 5.66: Circuit Diagram for Problem 5.24

Answer: *(a)* $v(t) = -10e^{-200t}V, t \geq 0$. *(b)* $i(t) = 0.05(1 + e^{-200t})A, t > 0$.

Problem 5.25 *Find the expression for* $i(t)$ *for* $t < 0$ *and for* $t \geq 0$. *Sketch* $i(t)$ *to scale versus time for Figure 5.67.*

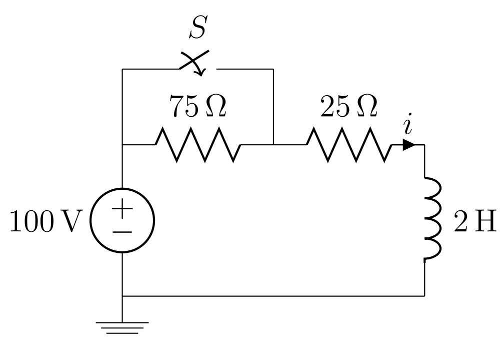


Figure 5.67: Circuit Diagram for Problem 5.25

Answer: $i(t) = 4 - 3e^{-12.5t}A, t \geq 0,\ i(t) = 1A, t < 0$.

Problem 5.26 *Find the expression for* $i(t)$ *and find the complete solution for the circuit of Figure 5.68.(assume* $i_p = Ae^{-t}$*.)*
Answer: $i(t) = -e^{-t} + e^{-0.5t}A, t \geq 0$.

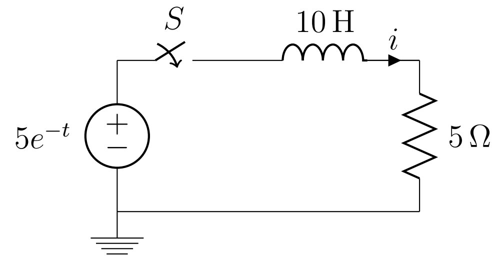


Figure 5.68: Circuit Diagram for Problem 5.26

Problem 5.27 *Given Figure 5.69. (a) Determine the initial state of $v_C(0)$. (b) Find the time constant of the system. (c) Find the steady-state value v_C(infinity). (d) Find complete solution of $v_C(t)$ by Node voltage method.*

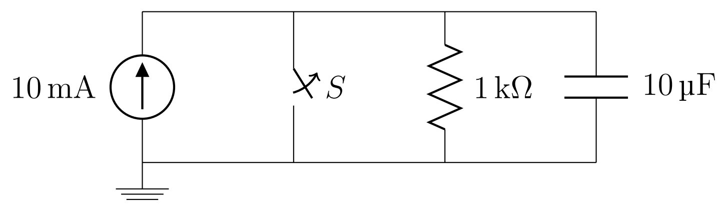


Figure 5.69: Circuit Diagram for Problem 5.27

Answer: *(a) $v_C(0^-) = 0 = v_C(0^+)$. (b) $s = -100$, $\tau = 0.01 sec$. (c) $v_C = 10V$. (d) $v_C(t) = 10(1 - e^{-100t})V$.*

Transient response–the second-order systems

Problem 5.28 *In Figure 5.70, initial conditions being zero is assumed. (a) Write the differential*

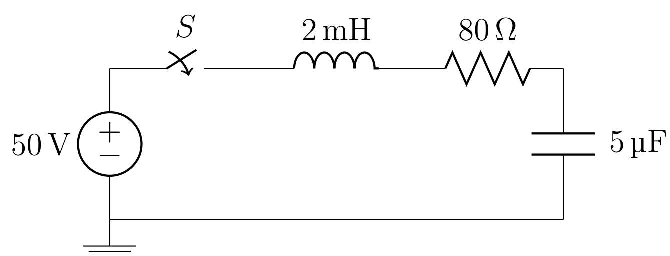


Figure 5.70: Circuit Diagram for Problem 5.28

equation for $v_C(t)$. (b) Solve for $v_C(t)$ if $R = 80\Omega$.
Answer: *(a) $\frac{d^2 v_C(t)}{dt^2} + 4 \times 10^4 \frac{dv_C(t)}{dt} + 10^8 v_C(t) = 50 \times 10^8$, $s_1 = -0.2679 \times 10^4$, $s_2 = -3.732 \times 10^4$. (b) $v_C(t) = 50 - 53.87e^{s_1 t} + 3.867e^{s_2 t}$.*

Problem 5.29 *Determine $i_L(t)$ and $v_C(t)$ for $t > 0$ in the circuit given in Figure 5.58*

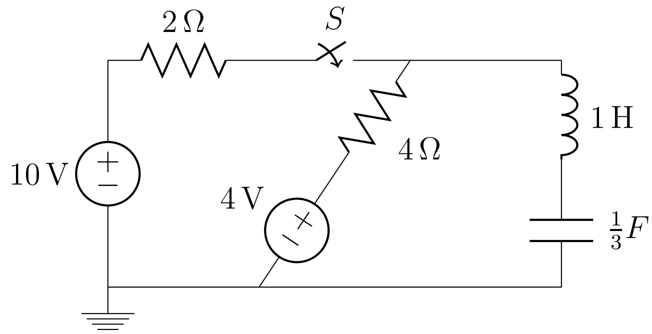


Figure 5.71: Circuit Diagram for Problem 5.29

Problem 5.30 *A dc source is connected to a series RLC circuit by a switch that closes at t=0 as shown in Figure 5.72. The initial conditions are $i(0) = 0$ and $v_C(0) = 0$. Write the differential equation for $v_C(t)$. Solve for $v_C(t)$ if $R = 20\Omega$.*

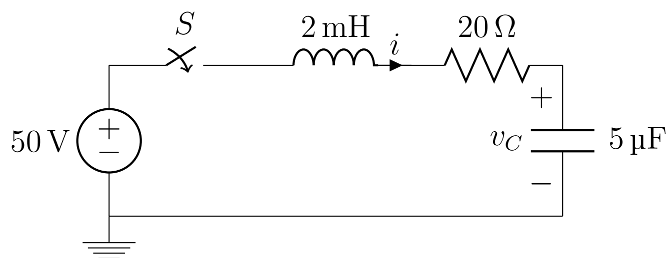


Figure 5.72: Circuit Diagram for Problem 5.30

Answer: $v_C(t) = 50 - 50e^{-\alpha t}\cos\omega_n t - 28.86e^{-\alpha t}\sin\omega_n t.$

Problem 5.31 *Consider the circuit shown in Figure 5.73. Initially, both the current in the inductor and the voltage across the capacitor are zero. Find the steady-state values of i_1, i_2, i_3, i_4 and v_C after the switch has been closed for a long time.*

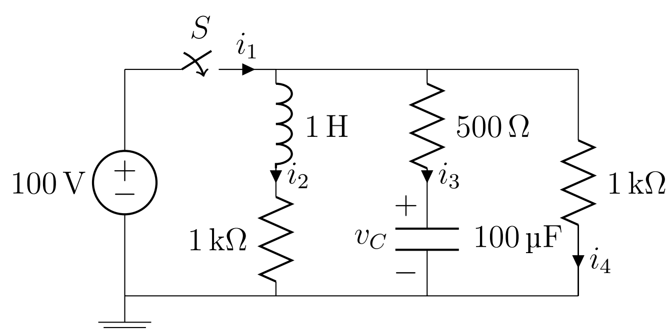


Figure 5.73: Circuit Diagram for Problem 5.31

Answer: $i_1 = 200mA$, $i_2 = i_4 = 100mA$, $i_3 = 0A, v_C = 100V.$

Problem 5.32 (Take-Home Exam) *(a) When S_1 and S_2 in Figure 5.74 are closed, derive the ODE for input current $i(t)$ and solve for $i(t)$. (Simulation should be included). (b) Find the impedance in terms of s, seen from the terminal a and b of S_1. Explain how this impedance is related to the ODE you found in (a). (c) When S_1 is closed and S_2 is open, derive the ODE for the capacitor voltage $v(t)$ and solve for $v(t)$. (Simulation should be included). (d) Find the impedance for $\bar{Z}(s)$ seen form the terminal c and d of S_2. Explain any connection with $\bar{Z}(s)$ of (c).*

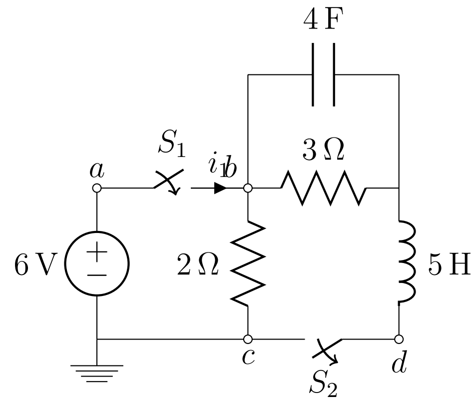


Figure 5.74: Circuit Diagram for Problem 5.32

Answer: *(a)* $60\frac{d^2i_1}{dt^2}+5\frac{di_1}{dt}+3i_1 = 15$, $i(t) = 5+e^{-0.042t}(-2\cos 0.22t+5.073\sin 0.22t)$ *(b)* $\frac{120s^2+10s+6}{60s^2+29s+5}$. *(c)* $\frac{60s^2+5s+3}{12s+1}$.

Problem 5.33 *Given Figure 5.75, assume the energy storage elements are initially at rest. (a) Find the steady state solution for $v(t)$. (b) Derive the ODE for $v(t)$.(c) Find the general solution $v(t)$.*

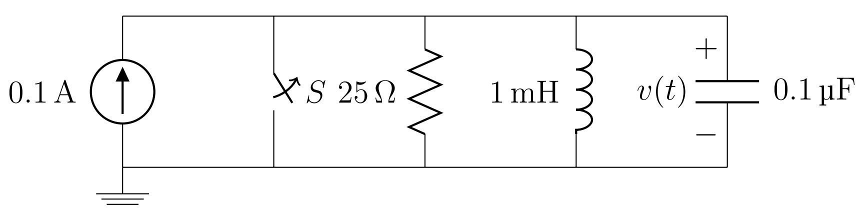


Figure 5.75: Circuit Diagram for Problem 5.33

Answer: *(a)* $v(\infty) = 0V$ *(b)* $v(t) = A_1e^{-0.268*10^5t} + A_2e^{-3.73*10^5t}V$ *(c)* $v(t) = 2.89(e^{-0.268*10^5t} - e^{-3.73*10^5t})V, t \geq 0$.

Problem 5.34 *Given a more involved Figure 5.76.(a) Find the equivalent Thevenin circuit seen by the capacitor. What are v_t and R_t respectively? (b) Determine i_C for $v(0)$.(c) Solve for $v(t), t > 0$ in terms of V_t, R_t, V_2. (This is a symbolic calculation, not numerical)*

Answer: *(a)* $v_T = R_3(\frac{v_1}{R_1} + \frac{v_2}{R_2})$. *(b)* $v(t) = v_T + (v_2 - v_T)e^{-\frac{t}{R_TC}}$. *(c)* $v(t) = v_T + Ae^{-\frac{t}{R_TC}}$.

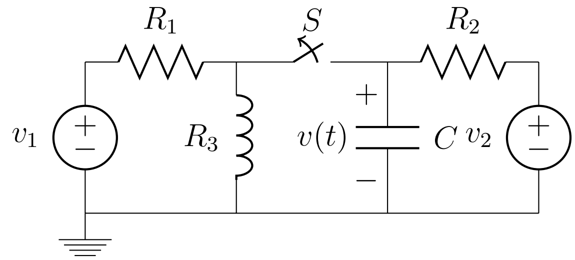


Figure 5.76: Circuit Diagram for Problem 5.34

Problem 5.35 *Solve for the steady-state values of the labeled currents and voltages for Figure 5.77.*

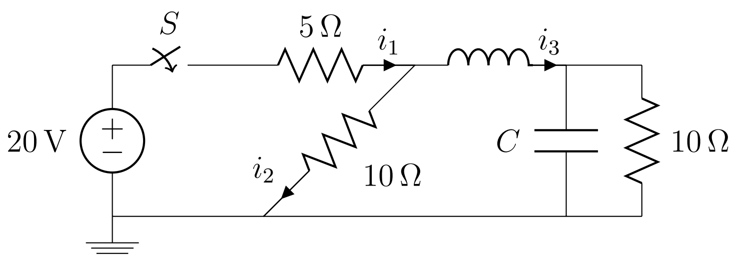


Figure 5.77: Circuit Diagram for Problem 5.35

Answer: $i_1 = 2A$, $i_2 = 1A$, $i_3 = 1A$.

Problem 5.36 *Find the steady-state values of i_1, i_2 and i_3 for the circuit shown in Figure 5.78.*

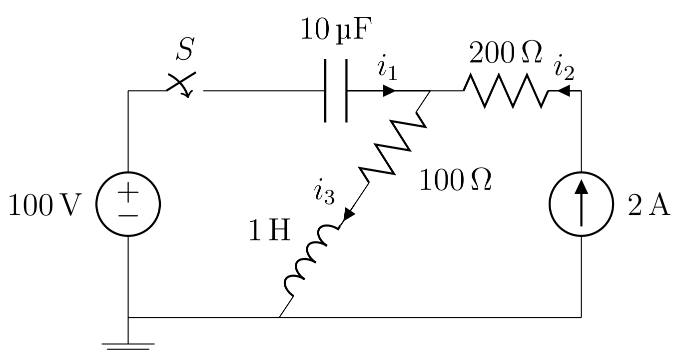


Figure 5.78: Circuit Diagram for Problem 5.36

Answer: $LC\frac{d^2i_3}{dt} + CR\frac{di_3}{dt} + i_3 = 2$. $i_1(\infty) = 0$, $i_1(\infty) = 2A$, $i_1(\infty) = 2A$.

Problem 5.37 *Assume the circuit Figure 5.79 is initially at rest, closed at $t = 0$ second and then open at $t = 1$ second. (a) Find the initial value for $V_C(0)$, $\frac{dV_C(0)}{dt}$ and $i_L(0)$ at the moment when the* *switch is open. (b) Find the ODE in terms of v_C (voltage of capacitor) when the switch is open. (c) Find the characteristic equation for ODE found in (b). (d) Write the complete solution for v_C without solving for coefficients A_1 and A_2.*

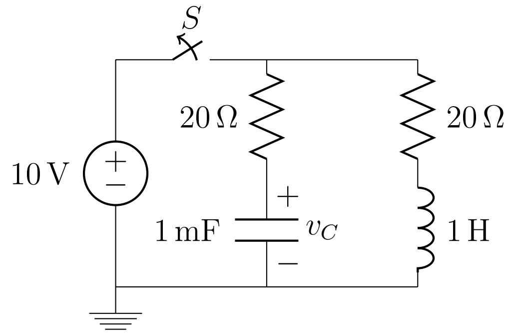


Figure 5.79: Circuit Diagram for Problem 5.37

Answer: *(a)* $v_C(0^+) = 10V, i_L(0^+) = 0.5A$ *(b)* $10^{-3}\frac{d^2v_C}{dt^2} + 40 \times 10^{-3}\frac{dv_C}{dt} + v_C = 0$. *(c)* $s_1 = -20 + j24.5$, $s_2 = -20 - j24.5$. *(d)* $v_C(t) = e^{-20t}(B_1 \cos 24.5t + B_2 \sin 24.5t)$.

Problem 5.38 *Given the circuit in Figure 5.80*
(a) Find the inductor current before the switch is closed.
(b) After the switch is closed, find the Thevenin seen by terminal ab and draw the equivalent circuit diagram with the inductor attached.
(c) Find the inductor current $i_L(t)$ after the switch is closed.

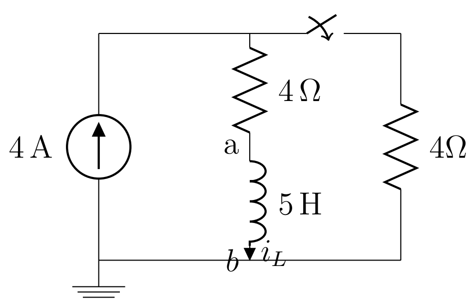


Figure 5.80: Circuit Diagram for Problem 5.38

Answer: *(a)* $i_L(0^-) = 4A$ *(b)* $V_{oc} = 16V$, $I_{sc} = 2A$, $R_t = 8\Omega$. *(c)*

$$16 = 8i + 5\frac{di}{dt} \quad 5s + 8 = 0, \quad s = -\frac{-8}{5}$$

$i_L(t) = Ae^{\frac{-8t}{5}} + 2, \quad A = 2.$

Chapter 6

Frequency Responses

All the input signals we have learned so far in an AC circuit have a fixed frequency that can not be changed during analysis. In fact, all the currents and voltages in a linear circuit are function of angular frequency. It is precisely this dependency (on frequencies) that allows special networks such as filters to be designed for particular applications. In this chapter, the frequency of an input signal is allowed to vary. The different frequency response of L and C to a sinusoidal signal is the key to frequency selective networks, which can block a certain range of frequency and allow some frequencies to pass. Depending on the parameters of L and C, the selective circuits are devised into 3 major categories in our text (but more can be found in many text books).

6.1 Low-Pass Filters

Given the following circuit diagram, the underlying problem is to investigate the magnitude of the output signal $\bar{V}_{out}$ when the frequency of the input signal is varying. In this subsection, we will investigate a circuit that allows low frequencies to pass while block high frequencies as much as possible. In other words, only low frequencies get passed to the output. To this end, start with KVL around the single and find the phasor current displayed below.

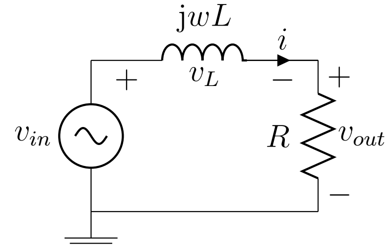


Figure 6.1: First-Order Low-Pass RL Filter

$$\bar{I} = \frac{\bar{V}_{in}}{R + j\omega L} = \frac{V_{in}\angle 0^\circ}{R + j\omega L} = \frac{V_{in}}{R\sqrt{1 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{-\omega L}{R})$$

Method 1: from circuit law

Then apply ohm's law to the resistor, to obtain the output voltage

$$\bar{V}_{out} = \bar{I} \cdot R = \frac{V_{in}}{\sqrt{1 + (\omega L/R)^2}} \angle - \tan^{-1}(\frac{\omega L}{R}) \tag{6.1}$$

whose $|output/input|$ ratio (known as the transfer function) can be readily found as

$$|H(\omega)| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + (\omega L/R)^2}} = \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_{co}})^2}} \tag{6.2}$$

where $\omega_{co} = \frac{R}{L}(or, f_{co} = \frac{R}{2\pi L})$ corner frequency, cut-off frequency, or half power frequency. This is because at the corner frequency, the power transferred to the output is half of its input power. To see this, setting $w = w_{co} = \frac{R}{L}$ in equation (6.1) leads to

$$\bar{V}_{out} = \frac{\bar{V}_{in}}{\sqrt{2}}$$

yielding

$$P_{out} = \frac{V_{out}^2}{R} = \frac{V_{in}^2}{2R} = \frac{P_{in}}{2}.$$

Method 2: Use impedance notion

The transfer function (6.2) can be obtained easily using impedance concept. To this end, recalling voltage divider yields

$$\bar{V}_{out} = \frac{R\bar{V}_{in}}{R + Ls}$$

and the transfer function evaluated at a particular frequency is

$$H(s)|_{s=jw} = \frac{\bar{V}_{out}}{\bar{V}_{in}} = \frac{R}{R + jwL} = \frac{1}{1 + \frac{jwL}{R}}$$

whose magnitude is that of (6.2)[1]. This demonstrates that to find the transfer function of a circuit network you can use either circuit laws or impedance concept.

It is also interesting, from equation (6.1), to understand how the output voltage changes with input frequency. Recalling (6.1) and varying the frequency w from 0 to ∞, we see that

$$\begin{aligned} V_{out} &= V_{in}, \quad \angle V_{out} = 0^\circ \quad \text{when } w \to 0 \\ V_{out} &= \frac{V_{in}}{\sqrt{2}}, \quad \angle V_{out} = -45^\circ \quad \text{when } w \to w_{co} \\ V_{out} &= 0, \quad \angle V_{out} = -90^\circ \quad \text{when } w \to \infty \end{aligned}$$

meaning, this is a low frequency passed circuit. A quick way to find whether a circuit is a low-pass or high-pass filter can be inferred from the impedance property of an inductors which behaves like

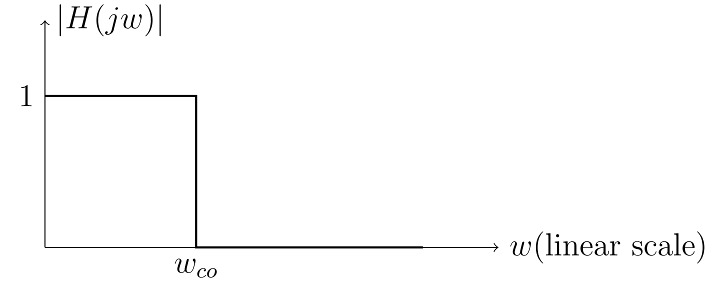


Figure 6.2: Ideal Low-Pass Magnitude vs linear w Plot

a short circuit when $w \to 0$, resulting in $V_{out} = V_{in}$ and behaves like an open circuit when $w \to \infty$, resulting in $V_{out} = 0$.

Another low-pass filter circuit is a little bit complex than the first circuit, leading to a second order low-pass filer.

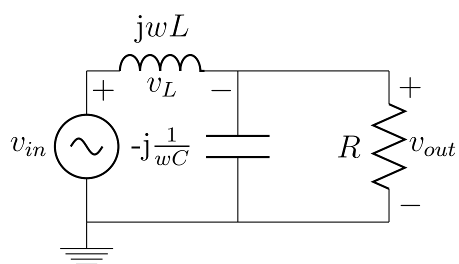


Figure 6.3: Second-Order Low-Pass RLC Filter

Method 1: from circuit law

Again start with KVL around the left-hand loop and the right-hand loop respectively.

$$\begin{aligned} \bar{V}_{in} &= \bar{I}_1(j\omega L) + (\bar{I}_1 - \bar{I}_2)\frac{1}{j\omega C} = \bar{I}_1(j\omega L + \frac{1}{j\omega C}) = \bar{I}_2(\frac{1}{j\omega C}) \\ 0 &= (\bar{I}_2 - \bar{I}_1)\frac{1}{j\omega C} + \bar{I}_2 \cdot R = -\bar{I}_1(\frac{1}{j\omega C}) + \bar{I}_2(R + \frac{1}{j\omega C}). \end{aligned}$$

Solving, we have

$$\bar{I}_2 = \frac{\bar{V}_{in}}{R(1-\omega^2 LC) + j\omega L} = \frac{V_{in}}{R\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{-\omega L}{R(1-\omega^2 LC)}).$$

Then, apply the Ohm's law to the output resistor, to obtain output voltage

$$\bar{V}_{out} = \bar{I}_2 R = \frac{V_{in}}{\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{-\omega L}{R(1-\omega^2 LC)}).$$

[1]Verify this result.

From which, the output-input ratio is obtained as[2]

$$|H(\omega)| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \tag{6.3}$$

Method 2: Use impedance concept

Despite the complexity in obtaining the transfer function for the second order low-pass filter, there is another way to find the transfer function via impedance concept and is given below.

$$\begin{aligned} H(s) &= \frac{V_{out}}{V_{in}} = \frac{(1/jwC)//R}{jwL + (1/jwC)//R} \\ &= \frac{\frac{R}{RCs+1}}{Ls + \frac{R}{RCs+1}} = \frac{R}{RLCs^2 + Ls + R} = \frac{1}{LCs^2 + Ls/R + 1} \end{aligned}$$

Evaluating $H(s)$ at $s = jw$ leads to

$$H(jw) = \frac{1}{1 - w^2 LC + j\frac{wL}{R}}.$$

whose magnitude is exactly that of (6.3).

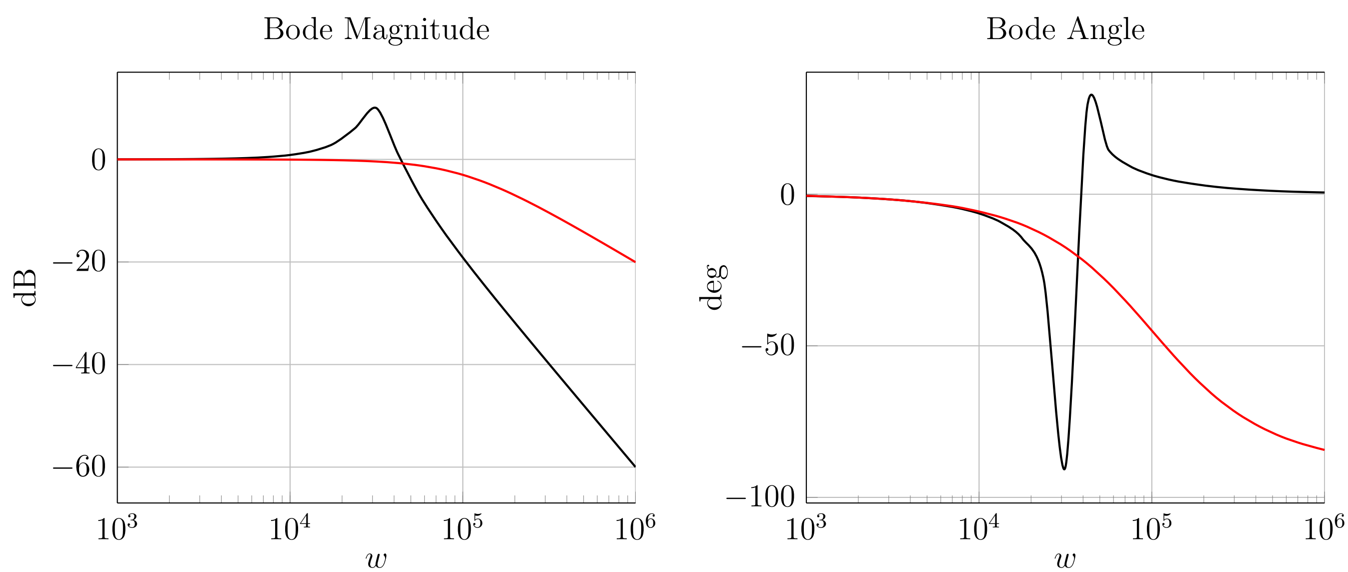


Figure 6.4: Bode Plots for 1^{st}- and 2^{nd}-order Low-Pass Filters

[2]Find the transfer function in s. $H(s) = \frac{1}{LCs^2 + \frac{L}{R}s + 1}$.

6.2 High-Pass Filters

Understanding the notion of low-pass filter, we will investigate circuits that allow high frequencies to pass but block low frequencies as much as possible. First-older high-pass filter is introduced first and then the second-order filter second. Following the analysis for low-pass filters, we find the phasor current displayed below

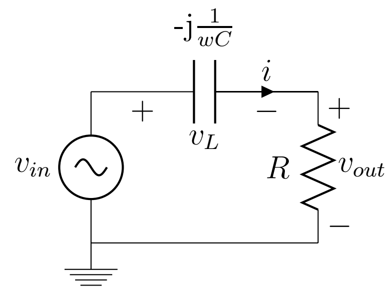


Figure 6.5: First-Order High-Pass RC Filter

$$\bar{I} = \frac{\bar{V}_{in}}{R - j\frac{1}{\omega C}} = \frac{V_{in}\angle 0^\circ}{R(1 - j\frac{1}{\omega RC})} = \frac{V_{in}}{R\sqrt{1 + (\frac{1}{\omega RC})^2}} \angle \tan^{-1}(\frac{1}{\omega RC})$$

Applying Ohm's law to the output resistor, to find the output voltage

$$\bar{V}_{out} = \bar{I} \cdot R = \frac{V_{in}}{\sqrt{1 + (1/\omega RC)^2}} \angle \tan^{-1}(\frac{1}{\omega RC}) \tag{6.4}$$

Then, the transfer function describing the output-input relationship is

$$|H(\omega)| = \frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{1 + (1/\omega RC)^2}} = \frac{1}{\sqrt{1 + (\omega_{co}/\omega)^2}} \tag{6.5}$$

where the frequency $\omega_{co} = \frac{1}{RC}$ is known as corner frequency, break frequency, cutoff frequency, or half power frequency. Recalling (6.4) and varying the frequency w from 0 to ∞, we see that

$$\begin{aligned} V_{out} &= 0, \quad \angle V_{out} = 90^\circ \quad \text{when } w \to 0 \\ V_{out} &= \frac{V_{in}}{\sqrt{2}}, \quad \angle V_{out} = 45^\circ \quad \text{when } w \to w_{co} \\ V_{out} &= V_{in}, \quad \angle V_{out} = 0^\circ \quad \text{when } w \to \infty \end{aligned}$$

meaning, it is a high frequency passed circuit[3]. For a second-order high-pass filter, we start writing KVL for the two loops respectively

[3]Analyzing the impedance property of a capacitor when frequency varies and make you conclusion.

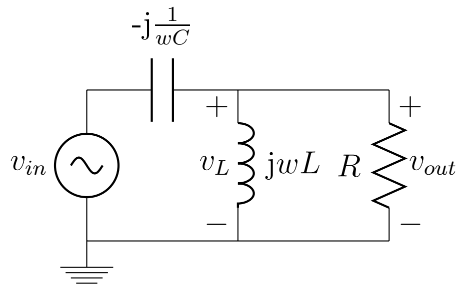


Figure 6.6: Second-Order High-Pass RLC Filter

$$
\begin{aligned}
\bar{V}_{in} &= \bar{I}_1(\frac{1}{j\omega C}) + (\bar{I}_1 - \bar{I}_2)j\omega L = \bar{I}_1(\frac{1}{j\omega C + j\omega L}) - \bar{I}_2(j\omega L) \\
0 &= (\bar{I}_2 - \bar{I}_1)j\omega L + \bar{I}_2 R = -\bar{I}_1(j\omega L) + \bar{I}_2(R + j\omega L)
\end{aligned}
$$

Solving, we have the current for the right-hand loop

$$
\bar{I}_2 = \frac{(-\omega^2 LC\bar{V}_{in})}{R(1-\omega^2 LC) + j\omega L} = \frac{(-\omega^2 LC)V_{in}}{R\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{-\omega L}{R(1-\omega^2 LC)})
$$

and the output voltage becomes

$$
\bar{V}_{out} = \bar{I}_2 R = \frac{(-\omega^2 LC)V_{in}}{\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{-\omega L}{R(1-\omega^2 LC)})
$$

Lastly, the transfer function[4] is

$$
|H(\omega)| = \frac{V_{out}}{V_{in}} = \frac{\omega^2 LC}{\sqrt{(1-\omega^2 LC)^2 + (\omega L/R)^2}} \angle \tan^{-1}(\frac{(\omega/\omega_n)^2}{\sqrt{(1-\omega^2/\omega_n^2)^2 + \xi^2(\omega/\omega_n)^2}}).
$$

Although, we did not use impedance notion in this section, the second method remains valid in deriving the results. You are encouraged to use any method when it is convenient to use.

After establishing the notions of frequency selection circuits, we are ready to move forward to understand how to plot frequency response. To this end, Bode plot is useful. Two plots are needed to completely describe the concept of Bode plots. One is a plot of magnitude and the other is a plot of angle/phase.

6.3 Bode Plots

A plot shows magnitude in decibels vs frequency in a log scale. It is useful when dealing with transfer functions.

[4]Find the $H(s)$ via impedance concept and plot the frequency response.

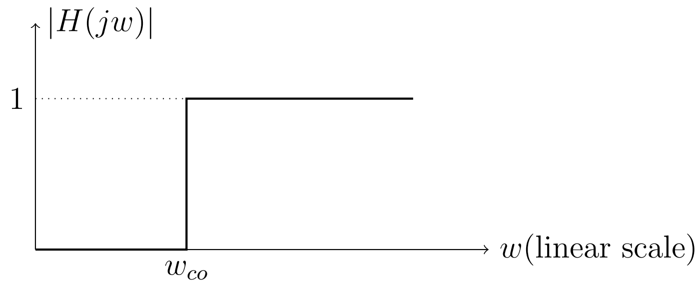


Figure 6.7: Ideal High-Pass Magnitude vs linear w Plot

To begin with, we need to convert a transfer function magnitude into decibels. To this end, we define

$$|H(jw)|_{dB} \triangleq 20 \log |H(jw)|.$$

Some numerical examples are listed below.

$$\begin{array}{ll} 100 \longleftrightarrow 40\text{dB} & 1/100 \longleftrightarrow -40\text{dB} \\ 2 \longleftrightarrow 6\text{dB} & 1/2 \longleftrightarrow -6\text{dB} \\ 1 \longleftrightarrow 0\text{dB} & \sqrt{2} \longleftrightarrow -3\text{dB} \end{array}$$

The advantages of such definition are

1. Extreme magnitudes can be displayed clearly on a single plot.

2. Decibels plots can be approximated by straight lines provided that a logarithmic scale is used for frequency.

3. Multiplication of magnitudes can be converted into addition. For example,

$$20 \log(10w) = 20 \log w + 20 \log 10 = 20 \log w + 20 \ dB$$

which illustrates that an increase of a factor of 10 contributes 20 dB.

$$20 \log(10^n w) = 20 \log w + 20 \log 10^n = 20 \log w + 20n \ dB. \tag{6.6}$$

The geometrical explanation of (6.6) is depicted below

Or another example,

$$20 \log(2w) = 20 \log w + 20 \log 2 = 20 \log w + 6.06 \ dB$$

which illustrates that an increase of a factor of 2 contributes 6 dB.

$$20 \log(2^n w) = 20 \log w + 20 \log 2^n = 20 \log w + 6.06n \ dB. \tag{6.7}$$

w	$10w$	10^2w	10^3w	10^4w	Decade scale

Figure 6.8: Log Scale

w	$w+1$	$w+2$	$w+3$	$w+4$	Linear scale
w	$10w$	10^2w	10^3w	10^4w	Decade scale
w	$2w$	2^2w	2^3w	2^4w	Octave scale

Figure 6.9: Illustration of 3 Different Scales

A linear scale means the variable is *added* by a factor for equal length while a logarithmic scale means the variable is *multiplied* by a factor for equal length. The concept is illustrated in the following. Before proceeding, we define

A decade is a 10-to-1 change in frequency measured in a logarithmic scale. Since on a log scale, we have

$$\log\frac{10}{1} = \log\frac{100}{10} = \log\frac{10^3}{10^2} = \log 10 = 1.$$

That is to say one log unit increment is equivalent to a factor of 10 times increment in linear scale. So a decade is a range of frequency for which the ratio of the highest frequency to the lowest frequency is 10. With this in mind, you will see a multiplication of 10^x for an equal increment of length on the x-axis while on a linear scale, an equal length represents addition of a given amount, say 1 or 5. In sum, the number of decade is calculated according to what follows.

$$\text{number of decade } \sharp \triangleq \log_{10}(\frac{w_2}{w_1}) \Leftrightarrow \frac{w_2}{w_1} = 10^{\sharp}.(or\ equivalently, w_2 = w_1 \times 10^{\sharp})$$

Furthermore, it is convenient to use line approximations for the first-order terms. Consider the first-order term that will become clear shortly.

$$dB_i = 20\log\sqrt{[1+(\frac{w}{w_i})^2]} \approx 20\log(\frac{w}{w_i}) = 20\log w - 20\log w_i, \quad w >> w_i \tag{6.8}$$

The equation (6.8) bears the form $y = ax + b$ (ie., a linear function), where $y = dB_i$, $x = \log w$, $a = 20$, and $b = -20\log w_i$. To plot, we evaluate the following particular points to sketch.

When plotting via PSpice, users are asked to provide information on START frequency (w_{start}), END frequency (w_{end}), and Number of points per Decade (nd). The formula above can be applied to

Frequencies (x)	dB_i (y)
$\frac{w_i}{100}$	$0dB$
$\frac{w_i}{10}$	$0dB$
w_i corner freq.	$3.010\ dB$
$10w_i$	$20dB$
$100w_i$	$40dB$
$10^n w_i$	$20ndB$

Table 6.1: Evaluation of Points

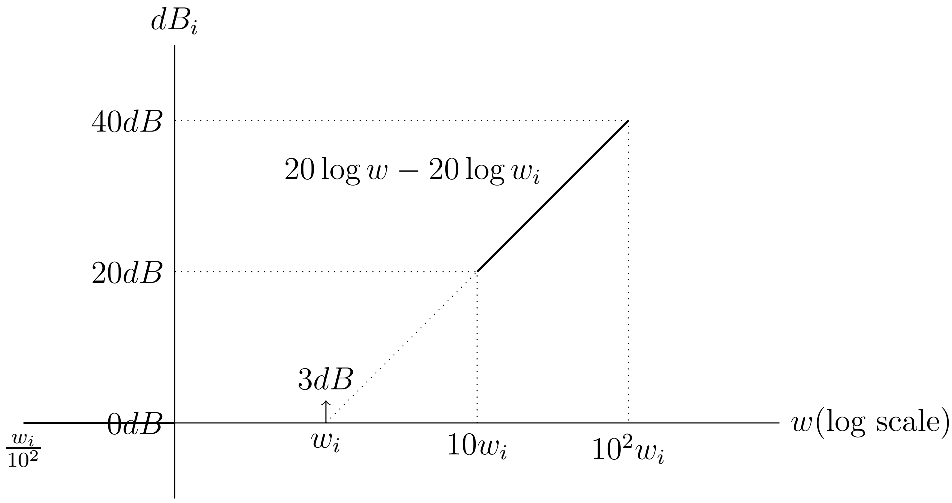


Figure 6.10: Line Approximation of Magnitude Bode Plot for the 1^{st}-order Term

determine the frequencies **in a given decade** between w_{start} and w_{end}. For example, if $w_{start} = 50$ and $w_{end} = 5000$ and the number of points per decade is nd=20, the frequencies **in one decade** between 50 and 500 would be

$$w_k = w_{start} \times 10^{k/nd}, \quad k = 0, 1, 2, \cdots, nd \tag{6.9}$$

yielding

$$w_0 = 50, w_1 = 56.10, w_2 = 62.95, \cdots, w_{20} = 500. \quad (unit : Hz\ or\ rad/sec.)$$

An octave is a 2-to-1 change in frequency measured in a logarithmic scale.

$$\text{number of octave } \sharp \triangleq \log_2(\frac{w_2}{w_1}) = \log(\frac{w_2}{w_1})/\log 2 \Leftrightarrow \frac{w_2}{w_1} = 2^{\sharp}.$$

It is noted that the formula (6.9) to find frequencies in a decade is readily applicable to find frequencies in an octave by replacing the number 10 with 2. Therefore, **an advantage of logarithm over linear scale is that a wide range of frequency can be covered in one plot**. Before continuing our analysis, recall the following property of logarithms given by

$$\log(\frac{ab}{cd}) = \log ab - \log cd = \log a + \log b - \log c - \log d.$$

To illustrate, consider the first-order low-pass transfer functions (see (6.2) for reference)

$$H(f) = \frac{1}{1 + j(\frac{f}{f_c})} = \frac{1}{1 + j(\frac{w}{w_c})}, \quad w = 2\pi f$$

whose magnitude is

$$H(f) = \frac{1}{\sqrt{1 + (\frac{f}{f_c})^2}} \angle - \tan^{-1}(\frac{f}{f_c}).$$

The decibel is defined as

$$|H(f)|_{dB} = 20 \log \frac{1}{\sqrt{1 + (\frac{f}{f_c})^2}} = 20 \log(1) - 20 \log[1 + (\frac{f}{f_c})^2]^{\frac{1}{2}} = -10 \log[1 + (\frac{f}{f_c})^2].$$

Low freq. asymptote

For $f << f_c$ $\quad |H(f)|_{dB} = -10 \log(1) = 0dB$

$\angle H(f) = -\tan^{-1} 0 = 0°.$

For $f = 10^{-2} f_c$ $\quad |H(f)|_{dB} = -10 \log(1 + (\frac{0.01 f_c}{f_c})^2) \approx 0dB$

$\angle H(f) = -\tan^{-1} 0.01 = -0.58°.$

For $f = 10^{-1} f_c$ $\quad |H(f)|_{dB} = -10 \log(1 + (\frac{0.1 f_c}{f_c})^2) \approx 0dB$

$\angle H(f) = -\tan^{-1} 0.1 = -5.72°.$

For $f = f_c$ $\quad |H(f)|_{dB} = -10 \log 2 = -3dB$

$\angle H(f) = -\tan^{-1} 1 = -45°.$

High freq. asymptote

For $f = 10 f_c$ $\quad |H(f)|_{dB} = -10 \log(1 + (\frac{10 f_c}{f_c})^2) \approx -20dB$

$\angle H(f) = -\tan^{-1} 10 = -84.28°.$

For $f = 10^2 f_c$ $\quad |H(f)|_{dB} = -10 \log(1 + (\frac{10^2 f_c}{f_c})^2) \approx -40dB$

$\angle H(f) = -\tan^{-1} 100 = -89.42°.$

For $f >> f_c$ $\quad |H(f)|_{dB} = -10 \log(\frac{f}{f_c})^2 dB$

$\angle H(f) = -\tan^{-1} \infty = -90°.$

Obviously, we have $\angle H(f) = -\tan^{-1}(\frac{f}{f_c})$.

Notice that the point in the magnitude plot where low frequency asymptote and high frequency asymptote meets is known as corner, cutoff, break, or half power frequency. Yet, where is the corner frequency in the angle plot? You will find it occurs at $\angle H(jf_c) = \pm 45°$ in the angle plot.

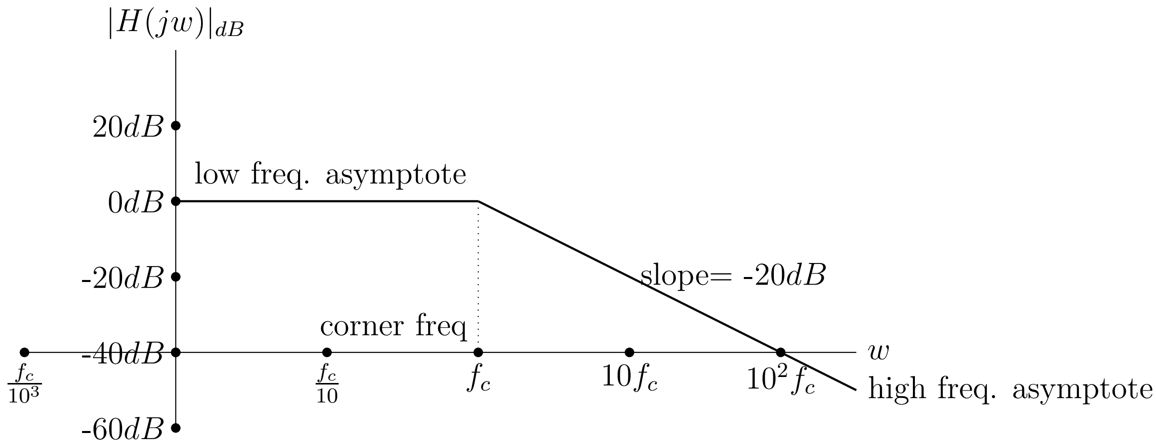


Figure 6.11: Line Approximation of Magnitude Bode Plot for the 1st-order Low-Pass Filter

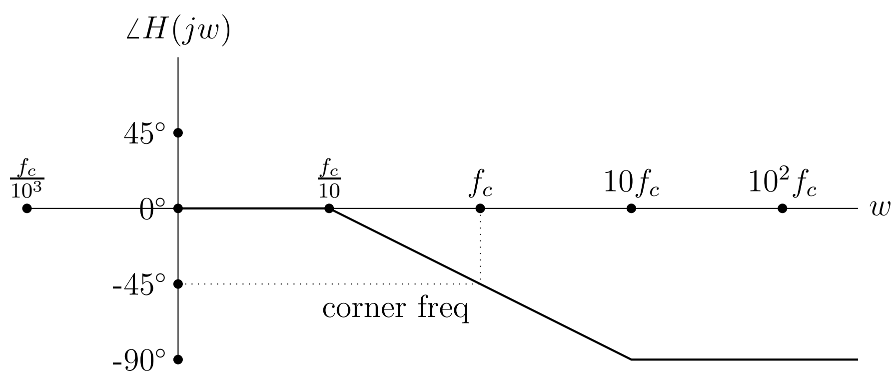


Figure 6.12: Line Approximation of Angle Bode Plot for the 1st-order Low-Pass Filter

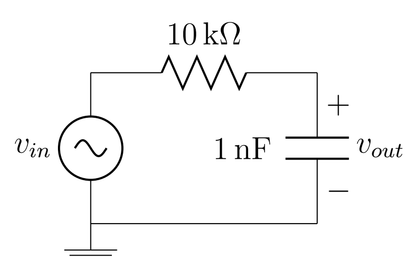


Figure 6.13: Example 6.1

Example 6.1 (Frequency Response of Low-Pass Filters) *Given the following circuit, find the frequency response.*
Solution: *Apply voltage divider to obtain the following input-output ratio (transfer function) in*

terms of w.

$$\bar{Z} = 10^4 - j\frac{10^9}{\omega}, \quad \bar{V}_{out} = \frac{\bar{V}_{in}(-j10^9/\omega)}{10^4 - j(10^9/\omega)} = \frac{\bar{V}_{in}}{1 + j(\omega/10^5)}$$

thus $\omega_{co} = 10^5 = 1/RC, f_{co} = 15.9KHz$. *Furthermore*[5]

$$20\log|\frac{\bar{V}_{out}}{\bar{V}_{in}}| = -20\log\sqrt{1 + (\frac{\omega}{10^5})^2}$$

$$\begin{array}{ll} For\ \omega >> 10^5 & 20\log|\frac{V_{out}}{V_{in}}| \approx -20\log(\omega/10^5) \\ For\ \omega << 10^5 & 20\log|\frac{V_{out}}{V_{in}}| \approx -20\log 1 = 0. \end{array}$$

It is noted that over high frequency range ($10^n w$)*, the asymptote is a straight line with slope of 20dB per decade. To see this, it is easy to verify the following identity*

$$-20\log\frac{10^n w}{10^5} = -20\log\frac{w}{10^5} - 20\log 10^n = -20\log\frac{w}{10^5} - 20n \quad dB$$

meaning for an increase of one decade the magnitude drops -20dB. Please refer to Figure 6.10 for detail, noting that it is negative slope for this case ($w_i = 10^5$)*.*

□

Now consider the transfer function of a high-pass filter (see (6.5) for reference)

$$\begin{aligned} H(f) &= \frac{j(\frac{f}{f_c})}{1 + j(\frac{f}{f_c})} = \frac{\frac{f}{f_c}}{\sqrt{1 + (\frac{f}{f_c})^2}} \angle \frac{\pi}{2} - \tan^{-1}(\frac{f}{f_c}) \\ &= \frac{1}{1 - j(\frac{f_c}{f})} = \frac{1}{\sqrt{1 + (\frac{f_c}{f})^2}} \angle \tan^{-1}(\frac{f_c}{f}). \end{aligned}$$

Therefore

$$|H(f)|_{dB} = -10\log[1 + (\frac{f_c}{f})^2]$$

and arguing in the same fashion as the low-pass filter, we have

Low freq. asymptote

$$\begin{array}{ll} \text{For } f << f_c & |H(f)|_{dB} = -10\log(\frac{f_c}{f})^2 dB \\ & \angle H(f) = -\tan^{-1} 0 = 90^\circ. \\ \text{For } f = 10^{-2} f_c & |H(f)|_{dB} = -10\log(1 + (\frac{f_c}{0.01 f_c})^2) \approx -40dB \end{array}$$

[5] Plot the frequency response of this 1st-order and 2nd-order low-pass filter via PSpice.

$$\angle H(f) = -\tan^{-1} 100 = 89.42°.$$

For $f = 10^{-1} f_c$ $\quad |H(f)|_{dB} = -10\log(1 + (\frac{f_c}{0.1 f_c})^2) \approx -20dB$

$$\angle H(f) = -\tan^{-1} 10 = 84.28°.$$

For $f = f_c$ $\quad |H(f)|_{dB} = -3dB$

$$\angle H(f) = -\tan^{-1} 1 = 45°.$$

High freq. asymptote.

For $f = 10^2 f_c$ $\quad |H(f)|_{dB} = -20\log(1 + (\frac{f_c}{100 f_c})^2) \approx 0dB$

$$\angle H(f) = -\tan^{-1} 0.01 = 0.58°.$$

For $f = 10^1 f_c$ $\quad |H(f)|_{dB} = -20\log(1 + (\frac{f_c}{10 f_c})^2) \approx 0dB$

$$\angle H(f) = -\tan^{-1} 0.1 = 5.72°.$$

For $f >> f_c$ $\quad |H(f)|_{dB} = -20\log(1) = 0dB$

$$\angle H(f) = -\tan^{-1} 0 = 0°.$$

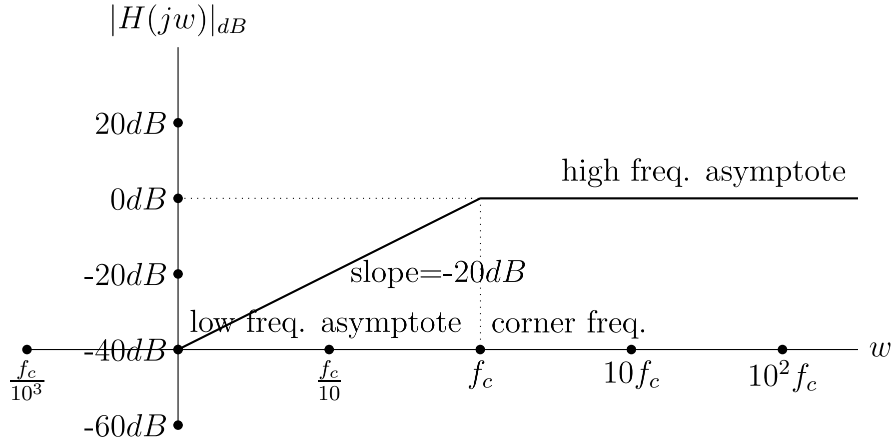


Figure 6.14: Line Approximation of Magnitude Bode Plot for the 1^{st}-order High-Pass Filter

Example 6.2 (Frequency Response of High-Pass Filters) *Given the following circuit, find the frequency response.*
Solution: *Apply voltage divider to obtain the following input-output ratio (transfer function) in terms of w.*

$$Since \bar{Z} = 10,000 - j10^9/\omega, \quad \bar{V}_{out} = \frac{\bar{V}_{in} \cdot 10,000}{10,000 - j10^9/\omega} = \frac{\bar{V}_{in}}{1 - j10^5/\omega}.$$

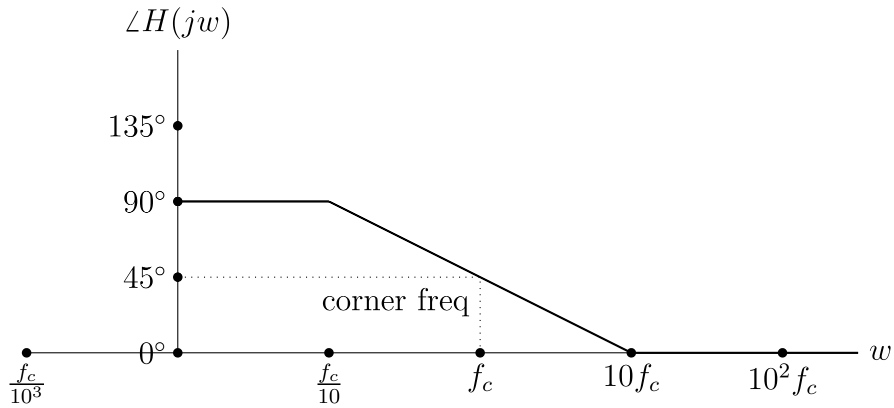


Figure 6.15: Line Approximation of Angle Bode Plot for the 1^{st}-order High-Pass Filter

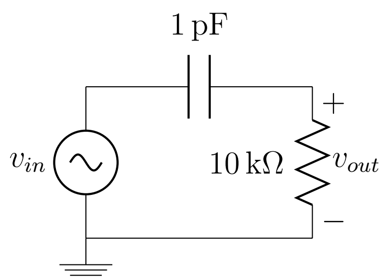


Figure 6.16: Example 6.2

Thus $\omega_{co} = 10^5 rad/s, f_{co} = 15.9KHz$. *Furthermore,*

$$20\log|\frac{\bar{V}_{out}}{\bar{V}in}| = 20\log\frac{1}{\sqrt{1+(10^5/\omega)^2}} = -20\log\sqrt{1+(\frac{10^5}{\omega})^2}$$

$$For\ \omega << 10^5, \qquad 20\log|\frac{V_{out}}{V_{in}}| = -20\log 10^5/\omega = 20\log\frac{\omega}{10^5}$$

$$For\ \omega >> 10^5, \qquad 20\log|\frac{V_{out}}{V_{in}}| \approx -20\log 1 = 20\log 1.$$

□

Example 6.3 (Effect of Low-Pass Filters) *Suppose that an input signal given by*

$$v_{in}(t) = 5\cos(20\pi t) + 5\cos(200\pi t) + 5\cos(2000\pi t)$$

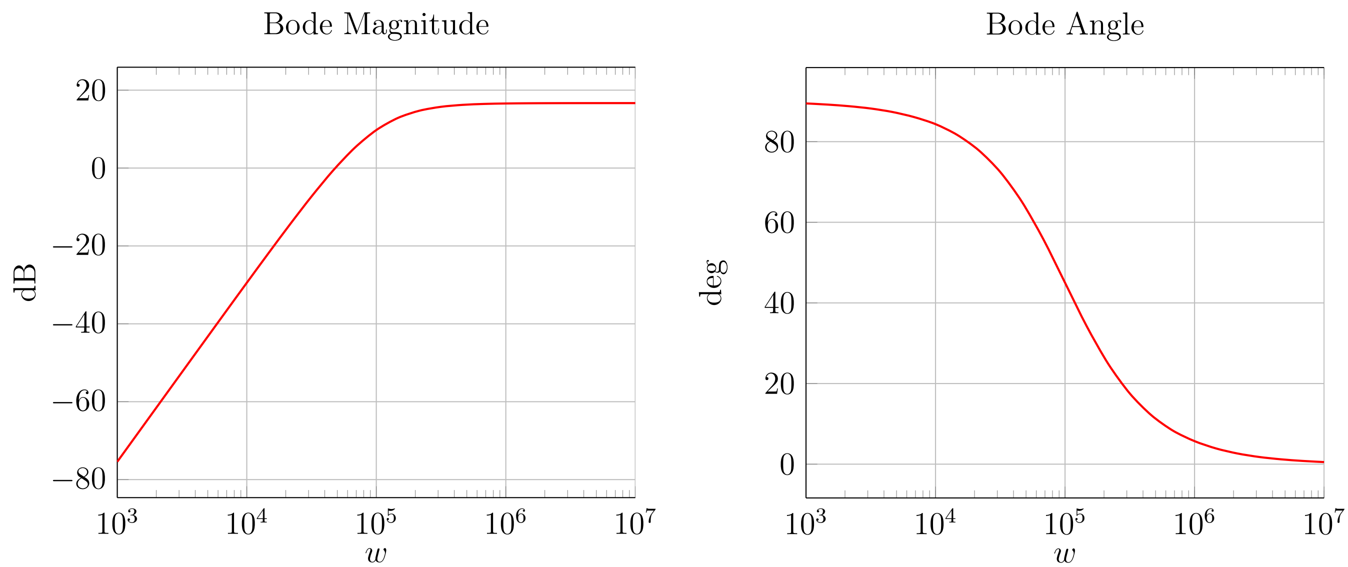


Figure 6.17: Bode Plots for 1^{st} High-Pass Filters

is applied to the low-pass RC filter shown below $R = 1000/2\pi$ *and* $C = 10\mu F$*. Find an expression for the output signal.*
Solution: *Applying voltage divider, we have*

$$\bar{V}_{out} = \left(\frac{\frac{1}{jwC}}{R + \frac{1}{jwC}}\right)\bar{V}_{in} = \frac{1}{1 + jwRC}\bar{V}_{in}$$

yielding

$$|H(jw)| = \frac{1}{1 + \sqrt{(\frac{w}{w_{co}})^2}}, \text{ where } w_{co} = \frac{1}{RC} = 2\pi f_{co} \tag{6.10}$$

whose cut-off frequency is $f_{co} = \frac{1}{2\pi RC} = 100$ *Hz. It should be easy to see that* f_{co} *is inversely proportional to* R[6]*.The Bode plot can be readily obtained.*

Since the input signal contains 3 different frequencies, we analyze the output componentwise. Evaluating the transfer function for the frequency $f = 10 = 10^{-1} f_{co}$*, we have*

$$H(10) = \frac{1}{1 + j\frac{f}{f_{co}}} = \frac{1}{1 + j\frac{10}{100}} = 0.9950\angle - 5.71^\circ$$

Noting that the magnitude 0.9950 is equivalent to 0.04321 in dB (since $10 \log 0.9950 = 0.04321$ *dB).*

$$\bar{V}_{out} = H(10)\bar{V}_{in} = (0.9950\angle - 5.71^\circ)(5\angle 0^\circ) = 4.975\angle - 5.71^\circ$$

[6] Try $R = 10^4/2\pi$ and plot the Bode diagram, what do you find?

Evaluating the transfer function for the frequency $f = 100 = f_{co}$*, we have*

$$H(100) = \frac{1}{1 + j\frac{f}{f_{co}}} = \frac{1}{1 + j\frac{100}{100}} = 0.7071\angle - 45^{\circ}$$

Noting that the magnitude 0.7071 is equivalent to -0.301 in dB (since $10 \log 0.7071 = -0.301$ *dB).*

$$\bar{V}_{out} = H(100)\bar{V}_{in} = (0.7071\angle - 45^{\circ})(5\angle 0^{\circ}) = 3.535\angle - 45^{\circ}$$

Evaluating the transfer function for the frequency $f = 1000 = 10f_{co}$*, we have*

$$H(1000) = \frac{1}{1 + j\frac{f}{f_{co}}} = \frac{1}{1 + j\frac{1000}{100}} = 0.09950\angle - 84.29^{\circ}$$

Noting that the magnitude 0.09950 is equivalent to -20 in dB (since $10 \log 0.0995 = -20$ *dB).*

$$\bar{V}_{out} = H(1000)\bar{V}_{in} = (0.09950\angle - 84.29^{\circ})(5\angle 0^{\circ}) = 0.4975\angle - 84.29^{\circ}.$$

Now, we can write an expression for the output signal by adding the output components together.

$$v_{out}(t) = 4.975\cos(20\pi t - 5.71^{\circ}) + 3.535\cos(200\pi t - 45^{\circ}) + 0.4975\cos(2000\pi t - 84.29^{\circ})$$

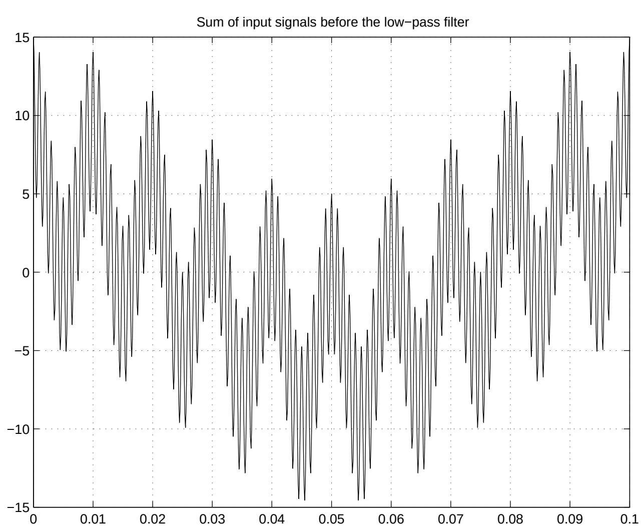


Figure 6.18: Plot of Time Domain Input Signals

□

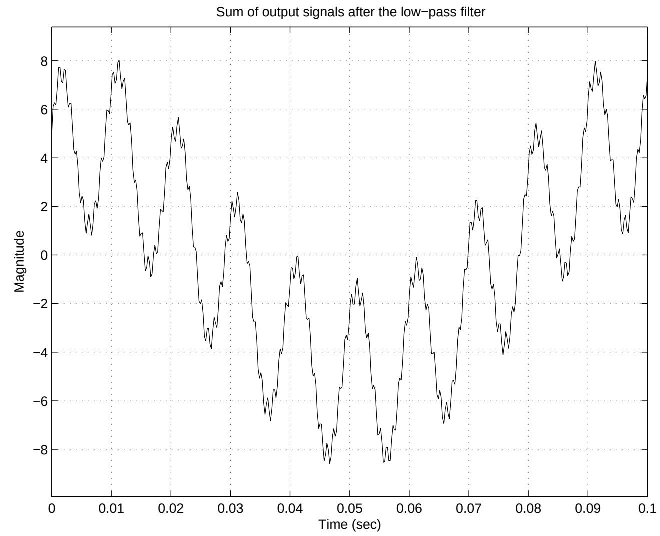


Figure 6.19: Plot of Time Domain Output Signals

6.4 Band-Pass Filters

Filters may also be band-pass where only a band of frequencies is passed while all others are attenuated (rejected). To analyze a band-pass filer, we need to define a terminology first: 3-dB Bandwidth. That is, The range of frequency in which the amplitude of the signal is equal to or greater than $1/\sqrt{2}$ times the maximum amplitude of the signal.

In what follows, we will study the combination of an inductor and a capacitor in series or in parallel where a phenomenon known as resonance can occur.

6.4.1 Series resonance

A characteristic of low-loss (R≈0), second-order system, at a particular resonant frequency, the system could have a forced response with significant amplitude for a moderate forced input. Given the series RLC circuit below, with varying input frequency from 0 to ∞, it is readily seen that the phasor current is

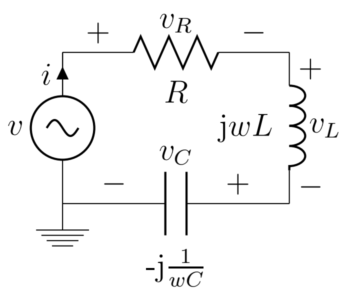


Figure 6.20: Series RLC Structure

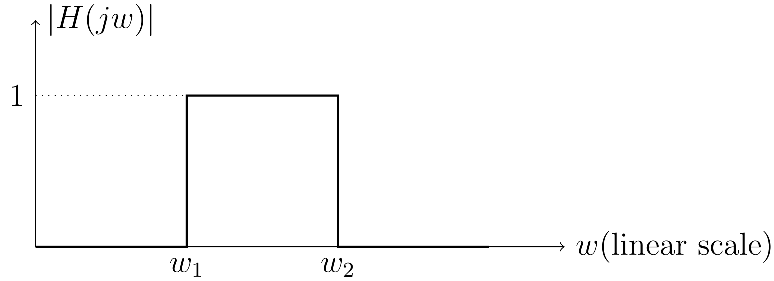


Figure 6.21: Ideal Band-Pass Magnitude vs linear w Plot

$$\bar{I} = \frac{\bar{V}}{R + j(\omega L - \frac{1}{\omega C})} = \frac{V}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} \angle \tan^{-1} -(\frac{\omega L - \frac{1}{\omega C}}{R}) \tag{6.11}$$

Note that I will be maximized when $\omega L = \frac{1}{\omega C}$, therefore the resonant frequency is defined as the ω such that $\bar{Z}(\omega_r) = R \approx 0$. Thus, $\omega_r L = \frac{1}{\omega_r C}$ or equivalently, $\omega_r = \frac{1}{\sqrt{LC}} = \omega_n$.

It is noted that if the series connection is excited at the resonant frequency w_r the series combination is equivalent to a pure resistive network (acting like a short circuit if $R \approx 0$.) Furthermore, recalling the series circuit, we observe that at $w = 0$ the capacitor is an open circuit and at $w = \infty$ the inductor is an open circuit, so that at these extremes in frequency, the resulting current is zero, meaning no output. Thus this is a selective network; but this time, it blocks high and low frequencies and let a certain band frequency passes. This is why it is called a band-pass filter.

To find the band (range of frequency), let's try to find its 3-dB bandwidth. Since

$$\frac{V}{\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}} = \frac{V}{\sqrt{2}R}$$

we have, after removing the numerator,

$$\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2} = \sqrt{2}R$$

squaring, we have

$$R^2 + (\omega L - \frac{1}{\omega C})^2 = 2R^2$$

which, after taking the square root, yields

$$\omega^2 LC + \omega RC - 1 = 0 \quad \text{and} \quad \omega^2 LC - \omega RC - 1 = 0.$$

Applying formula for quadratic equation to the equations above, to find solution for w.

$$-\tfrac{R}{2L} \pm \sqrt{(\tfrac{R}{2L})^2 + \tfrac{1}{LC}} \qquad \tfrac{R}{2L} \pm \sqrt{(\tfrac{R}{2L})^2 + \tfrac{1}{LC}}$$

$$\omega_1 = -\tfrac{R}{2L} + \sqrt{(\tfrac{R}{2L})^2 + \tfrac{1}{LC}} \qquad \omega_2 = \tfrac{R}{2L} + \sqrt{(\tfrac{R}{2L})^2 + \tfrac{1}{LC}}$$

thus the bandwidth $(w_2 - w_1)$ of the series circuit is

$$\beta = \omega_2 - \omega_1 = \frac{R}{L}$$

An important measure of the ability of the filter to pass a band of frequencies is its quality factor which is to determine the sharpness near resonance.

$$Q_s = \frac{\omega_r}{\beta} = \frac{\omega_r L}{R} = \frac{1}{\omega_r RC}$$

Hence, increasing R lowers the Q_s, degrading the filter.

To find the frequency response, we determine the transfer function from V to I in terms of s. To this end, impedance Ohm's law gives

$$V = IZ(s) = I(R + Ls + \frac{1}{Cs})$$

leading to

$$H(s) = \frac{I}{V} = \frac{1}{R + Ls + \frac{1}{Cs}}.$$

Letting $s = jw$, we have[7]

$$H(jw) = \frac{I}{V} = \frac{1}{R + j(wL - \frac{1}{wC})} \tag{6.12}$$

whose magnitude in dB is readily obtained as

$$|H(jw)|_{dB} = 20\log|H(jw)| = -10\log[R^2 + (wL - \frac{1}{wC})^2].$$

Following the similar procedure introduced before, we have

$$w \to 0 \qquad |H(jw)|_{dB} = -20\log\frac{1}{wC} = 20\log\frac{w}{C}, \quad \text{capacitive} \tag{6.13}$$

$$w \to w_r \qquad |H(jw)|_{dB} = -20\log R, \quad \text{pure resistive} \tag{6.14}$$

$$w \to \infty \qquad |H(jw)|_{dB} = -20\log wL, \quad \text{inductive} \tag{6.15}$$

It is known from (6.13) and (6.15) that the magnitude plot will decrease $-20dB$ per decade. Most importantly, equation (6.14) does not yield $0dB$ and do you know why?

Note that the transfer function is from V to I. If the transfer function from V to V_R is desired, we have

$$H(jw) = \frac{V_R}{V} = \frac{R}{R + j(wL - \frac{1}{wC})} = \frac{R}{R[1 + j(\frac{wL}{R} - \frac{1}{wRC})]} = \frac{1}{1 + j(\frac{wL}{R} - \frac{1}{wRC})} \tag{6.16}$$

The plot should give you $0dB$ at resonance.

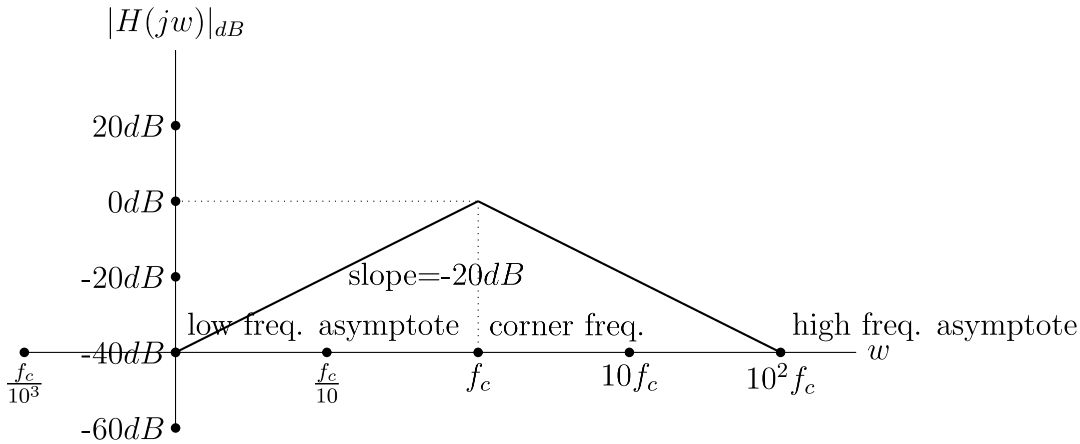


Figure 6.22: Line Approximation of Magnitude Bode Plot for a Band-Pass Filter

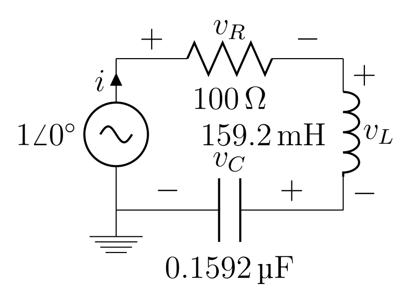


Figure 6.23: Example 6.4

Example 6.4 (Series Resonance) *[1] Given the following circuit and suppose it is working at the resonant frequency, find the phasor voltages across the elements and draw a phasor diagram.*
Solution: *First, find the resonant frequency*

$$f_r = \frac{1}{2\pi\sqrt{LC}} = 1000Hz, \quad Q_= \frac{2\pi f_r L}{R} = 10$$

At the resonant frequency, we find

$$\bar{Z}_C = j2\pi f_r L = j1000\Omega, \quad \bar{Z}_L = -j\frac{1}{2\pi f_r C} = -j1000\Omega.$$

As expected, the reactance $wL = \frac{1}{wC}$ are equal in magnitude at resonance, leading to pure resistive network $\bar{Z} = R + \bar{Z}_L + \bar{Z}_C = 100\Omega$. To continue, we find the loop current and element voltages below

$$\bar{I} = \frac{1\angle 0^\circ}{100} = 0.01\angle 0^\circ$$

and

$$\bar{V}_R = \bar{I}R = 1\angle 0^\circ, \quad \bar{V}_C = \bar{I}\bar{Z}_C = 10\angle -90^\circ, \quad \bar{V}_L = \bar{I}\bar{Z}_L = 10\angle 90^\circ$$

[7] compared with (6.11), what is your observation from (6.12)?

and the phasor diagram 6.24 showing the voltage relationship is displayed below. It is noted that

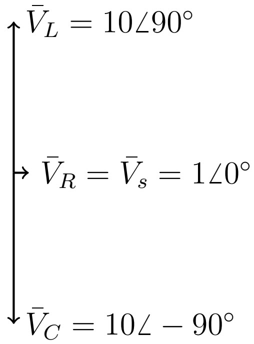


Figure 6.24: Phasor Diagram

the voltage magnitudes across the inductance and capacitance are magnified by the quality factor Q_s *when compared with the source voltage* $\bar{V}_s$.

□

Example 6.5 (Series Resonance) *Given* $\omega_r = 5Mrad/s$, $\omega_1 = 4.5Mrad/s$, $C = 0.01\mu F$, *find* Q_s, β, L *and* R.

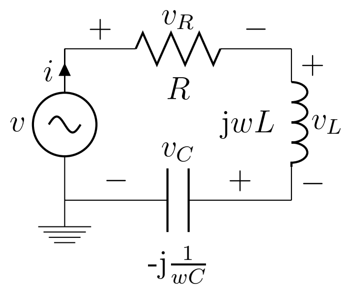


Figure 6.25: Example 6.5

Solution: *Since* $\omega_r = 1/\sqrt{LC}$, *we have* $L = 1/C\omega_r^2 = 4\mu F$. *Applying formula leads to*

$$4.5 \times 10^6 = \omega_1 = -\frac{R}{2 \cdot 4.5 \times 10^6} + \sqrt{(\frac{R}{9 \times 10^6})^2 + (5 \times 10^6)^2}$$

yielding $R = 4.22\Omega$. *Moreover,*

$$\omega_2 = \frac{R}{2L} + \sqrt{(\frac{R}{2L})^2 + \frac{1}{LC}} = 5.555 \times 10^6 rad/s = 5.555Mrad/s$$

Thus

$$\beta = \omega_2 - \omega_1 = 1.055 \times 10^6 = 1.055Mrad/s$$
$$Q_s = 5 \times 10^6/1.055 \times 10^6 = 4.74.$$

□

6.4.2 Parallel resonance

Given the following circuit diagram, we, by Ohm's law, have

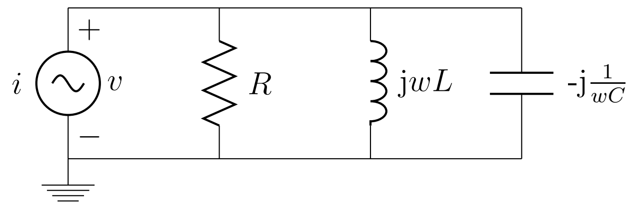


Figure 6.26: Parallel Structure

$$\bar{V} = \frac{\bar{I}}{\bar{Y}} = \frac{I}{(\frac{1}{R} + \frac{1}{j\omega L}) + j\omega C} = \frac{I}{\sqrt{(\frac{1}{R})^2 + (\omega C - \frac{1}{\omega L})^2}} \angle tan^{-1} - (\omega C - \frac{1}{\omega L})R$$

V will be maximized when $\omega C = \frac{1}{\omega L}$, therefore, the resonant frequency is the ω_r such that $\bar{Z}(\omega_r) = R$, in other words

$$\omega_r C = \frac{1}{\omega_r L} \text{ or } \omega_r = \frac{1}{\sqrt{LC}} = \omega_n. \tag{6.17}$$

It is noted that if the parallel connection is excited at the resonant frequency w_r the parallel combination is equivalent to a pure resistive network (an open circuit if $R = 0$.) Furthermore, recalling the parallel circuit, we observe that at $w = \infty$ the capacitor is a short circuit and at $w = 0$ the inductor is a short circuit, so that at these extremes in frequency, the resulting current is $\bar{I}_s$ flowing through either capacitor or inductor (In either cases, the resistor current is 0.)

Again, let's find its $3dB$-bandwidth. Since

$$\frac{I}{\sqrt{(\frac{1}{R})^2 + (\omega C - \frac{1}{\omega L})^2}} = \frac{IR}{\sqrt{2}}$$

we have

$$\frac{1}{R^2} + (\omega C - \frac{1}{\omega L})^2 = \frac{2}{R^2}$$

yielding

$$\omega^2 LC + \frac{L}{R}\omega - 1 = 0 \qquad \omega^2 LC - \frac{L}{R}\omega - 1 = 0$$

$$-\frac{1}{2RC} \pm \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} \qquad \frac{1}{2RC} \pm \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}}$$

$$\omega_1 = -\frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} \qquad \omega_2 = \frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}}$$

Thus the bandwidth of the parallel circuit is

$$\beta = \omega_2 - \omega_1 = \frac{1}{RC}$$

and the quality factor is

$$Q_p = \frac{\omega_r}{\beta} = \omega_r RC = \frac{R}{\omega_r L}.$$

Hence, increasing R raises the Q_s, upgrading the filter.

To find the frequency response, we determine the transfer function from I to V in terms of s. To this end, the impedance Ohm's law gives

$$I = VY(s) = V(\frac{1}{R} + \frac{1}{Ls} + Cs)$$

leading to

$$H(s) = \frac{V}{I} = \frac{1}{\frac{1}{R} + \frac{1}{Ls} + Cs}.$$

Letting $s = jw$, we have

$$H(jw) = \frac{V}{I} = \frac{1}{\frac{1}{R} + j(wC - \frac{1}{wL})}$$

whose magnitude in dB is readily obtained as

$$|H(jw)|_{dB} = 20\log|H(jw)| = -10\log[\frac{1}{R^2} + (wC - \frac{1}{wL})^2].$$

Following the similar procedure introduced before, we have

$$w \to 0 \qquad |H(jw)|_{dB} = -20\log\frac{1}{wL} = 20\log\frac{w}{L}, \quad \text{inductive} \tag{6.18}$$

$$w \to w_r \qquad |H(jw)|_{dB} = -20\log\frac{1}{R}, \quad \text{pure resistor} \tag{6.19}$$

$$w \to \infty \qquad |H(jw)|_{dB} = -20\log wC, \quad \text{capacitive} \tag{6.20}$$

It is known from (6.18) and (6.20) that the magnitude plot will decrease $-20dB$ per decade. Most importantly, equation (6.19) does not yield $0dB$ and do you know why? Note also that the transfer function is from I to V. Readers are encouraged to find the transfer function from I to I_R?

Example 6.6 (Parallel Resonance) *Given $R = 2K\Omega$, $L = 40mH$, $C = 0.25\mu F$, find the following quantities:*

a) ω_r, ω_1, ω_2, Q_p, $V_m(\omega_r)$, $V_m(\omega_1)$, $V_m(\omega_2)$

b) The R such that $\beta = 500rad/s$

Solution: *Applying the formulas, we have the following results.*

$$\omega_r = 1/\sqrt{LC} = 1/\sqrt{40\times 10^{-3}\cdot 0.25^{-6}} = 10^4 rad/s(1590Hz)$$

$$\omega_1 = -\frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} = 9049.88rad/s$$

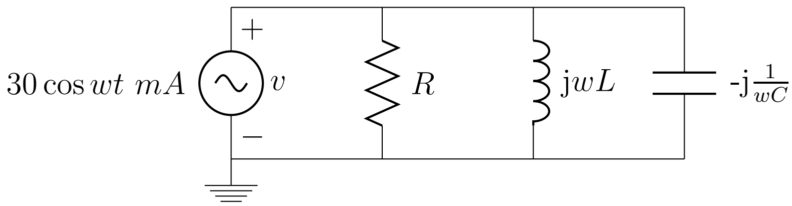


Figure 6.27: Example 6.6

$$
\begin{aligned}
&\omega_2 = \frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 + \frac{1}{LC}} = 11,049.88 rad/s \\
&V_m(\omega_r) = I_m \cdot R = 50 \times 10^{-3} \cdot 2 \times 10^3 = 100V \\
&V_m(\omega_1) = V_m(\omega_2) = V_m/\sqrt{2} = 70.7V \\
&R = 1/\beta \cdot C = 1/500 \cdot 0.25 \times 10^{-6} = 8K\Omega.
\end{aligned}
$$

The magnitude plot indicates that the peak frequency is $f = w_0/2\pi = 1590KHz$.

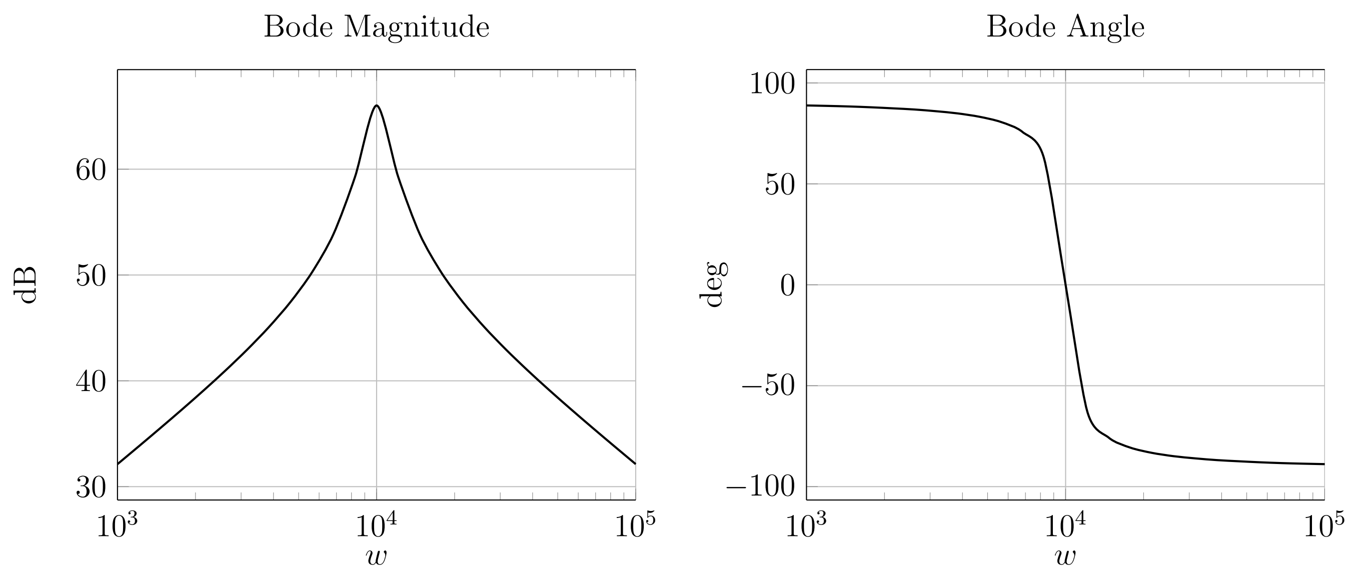


Figure 6.28: Bode Plot of a Parallel Resonance Circuit

□

An application of narrow band filters is seen in rejecting interference due to AC line power. Any undesired 60-Hz signal originating in the AC line power can cause serious interference in sensitive instruments. Given the following circuit, find its transfer function and plot the Bode plot.

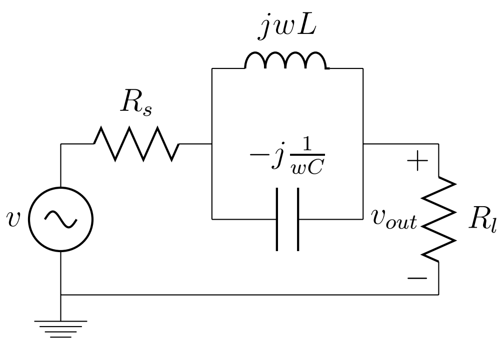


Figure 6.29: A Notch Filter

Applying voltage divider, we have

$$\bar{V}_{out} = \left(\frac{R_l}{R_s + R_l + jwL//jwC}\right)\bar{V}_{in} = \left(\frac{R_l}{R_s + R_l + j\frac{wL}{1-w^2LC}}\right)\bar{V}_{in}$$

yielding zero output (i.e. signal is blocked) when $w^2LC = 1$. To filter out the undesired 60-Hz noise, we have the following formula

$$(2\pi 60)^2 LC = 1$$

Let $L = 100mH$ then $C = 70.36\mu F$. To find its transfer function, we have

$$H(w) = \frac{R_l}{R_s + R_l + j\frac{wL}{1-w^2LC}} = \frac{R_l}{\sqrt{(R_s + R_l)^2 + (\frac{wL}{1-w^2LC})^2}}\angle - \tan^{-1}\frac{wL(R_s + R_L)}{1 - w^2LC}.$$

Thus

$$\begin{aligned}
\text{For } w << w_{co}, \quad |H(w)|_{dB} &= 20\log R_l - 10\log[(R_s + R_l)^2 + (\frac{wL}{1 - w^2LC})^2] \\
&= 20\log\frac{R_l}{R_s + R_l} \\
\text{Hint: } w &\to 0, \quad jwL = 0 \text{ and } 1/jwC = \infty \\
\text{For } w = w_{co}, \quad |H(w)|_{dB} &= 20\log R_l - 10\log[(R_s + R_l)^2 + (\frac{wL}{1 - w^2LC})^2] \\
&= 20\log\frac{R_l}{\infty} \\
\text{For } w >> w_{co}, \quad |H(w)|_{dB} &= 20\log R_l - 10\log[(R_s + R_l)^2 + (\frac{wL}{1 - w^2LC})^2] \\
&= 20\log\frac{R_l}{R_s + R_l} \\
\text{Hint: } w &\to \infty, \quad jwL = \infty \text{ and } 1/jwC = 0
\end{aligned}$$

This is known as a band-reject filter. However, in this example $w_1 = w_2$ and a special name notch filter is given.

The following numerical example is based on the analysis displayed above.

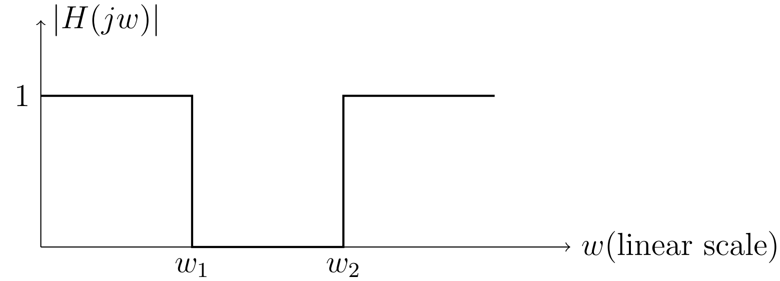


Figure 6.30: Ideal Band-Reject Magnitude vs linear w Plot

Example 6.7 (60-Hz Notch Filter) *[1] The frequency responses (magnitude and angle) in two scales (log and linear) are generated by the following MATLAB coding.*

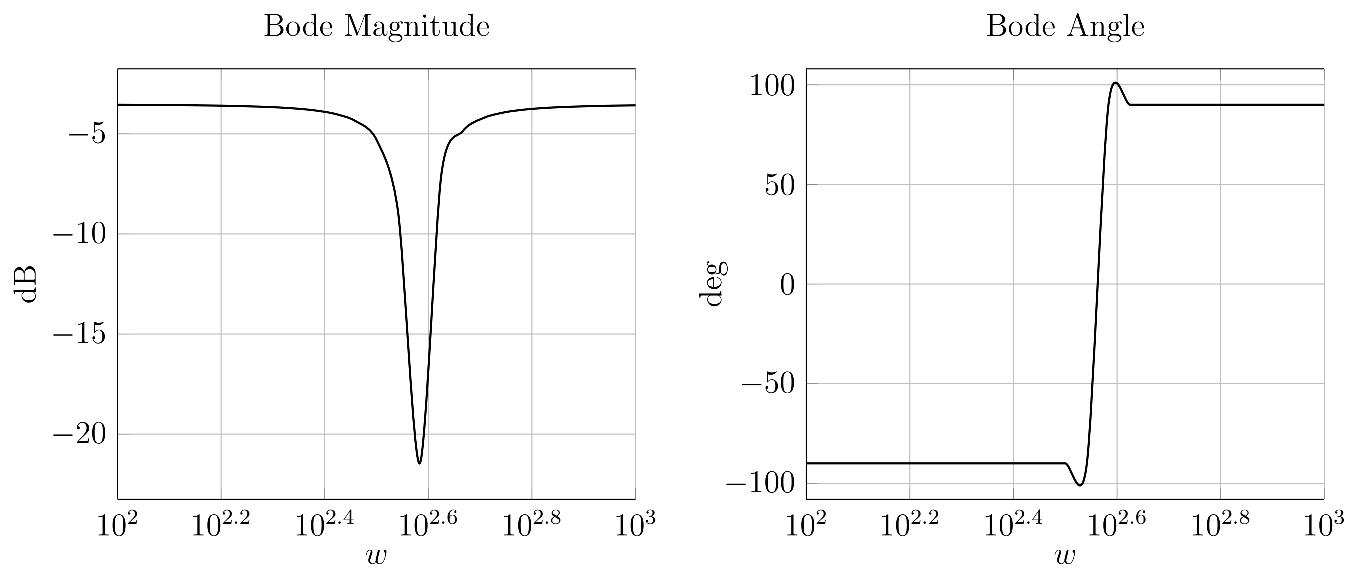


Figure 6.31: Bode Plot of a Notch Circuit

□

Example 6.8 (Time response vs. frequency response) *The natural response of Example 6.25 is $V = 100e^{-100t} sin 100\sqrt{99}t$ V with $C = 1\mu F$. Find w_r, β, Q_p, R and L.*
Solution: *Referring to example 6.29, we can derive a differential-integral form as follows*

$$I = I_R + I_C + I_L = \frac{v}{R} + C\frac{dv}{dt} + \frac{1}{L}\int v d\tau.$$

Differentiating, we obtain

$$C\frac{d^2v}{dt^2} + \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v = 0, \quad (Cs^2 + \frac{1}{R}s + \frac{1}{L} = 0)$$

whose characteristic values are

$$\begin{aligned} s_1, s_2 &= -\frac{1}{2RC} \pm \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}} \\ &= -\alpha \pm \sqrt{\alpha^2 - w_r^2} \\ &= -\alpha \pm j w_d \end{aligned}$$

Same derivation is found in Section 5.3. With this knowledge and knowing that $V = 100e^{-100t} sin 100\sqrt{99}t$, *we have*

$$100 = \alpha = \frac{1}{2 \cdot R \cdot 10^{-6}}$$

Solving, $R = 5K\Omega$ *and* $\beta = \frac{1}{RC} = 2\alpha = 200 rad/s$. *This demonstrates that the time domain parameter* 2α *contains bandwidth information. Furthermore, the damped frequency*[8]

$$\omega_d = \sqrt{w_r^2 - \alpha^2}$$

we have

$$\omega_r = \sqrt{\omega_d^2 + \alpha^2} = 1000 rad/s.$$

This shows that resonant frequency is contained in $\alpha^2 + w_d^2$. *In sum, the relationship between time response and frequency response is displayed below.*

$$\beta = 2\alpha \quad and \quad w_r^2 = \alpha^2 + w_d^2$$

The remaining characteristic parameters are easily obtained [9]

$$\begin{aligned} &L = 1/C\omega_r^2 = 1/(10^{-6} \cdot (10^3)^2) = 1H \\ &Q_p = \omega_r / 2\alpha = 1000/2 \cdot 100 = 5. \end{aligned}$$

This example shows that one can obtain frequency information by analyzing the time domain information. Of course, to do that you need to learn the analysis that we have gone through. Notice that increasing R *raises* Q_p *but lowers* Q_s. *After learning this example, do this exercise*[10]

□

Example 6.9 *Given the following radio circuit where the variable capacitor represents the tuner that can select certain radio stations. Find the frequency when* $C = 200pF$.
Solution: *Apply voltage divider to obtain the following input-output ratio (transfer function* $\frac{RLCs^2+Ls+R}{LCs^2+1}$*) in terms of* w.

$$\frac{\bar{V_0}}{\bar{V}} = \frac{(200\mu//C)}{10K + (200\mu//C)} = \frac{10^6}{10^6 + j(2\omega - \frac{5\times 10^{13}}{\omega})}$$

The peak value occurs at

$$2\omega_r = \frac{5 \times 10^{13}}{\omega_r}$$

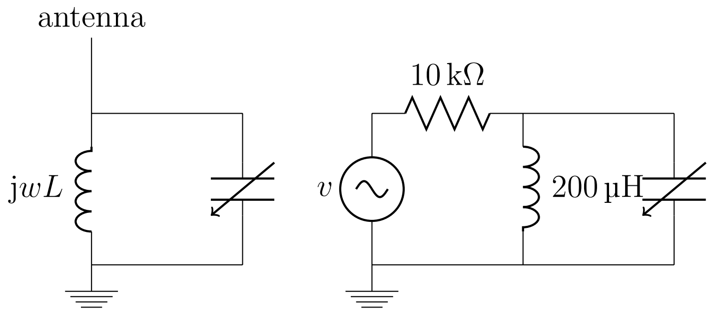


Figure 6.32: Example 6.9

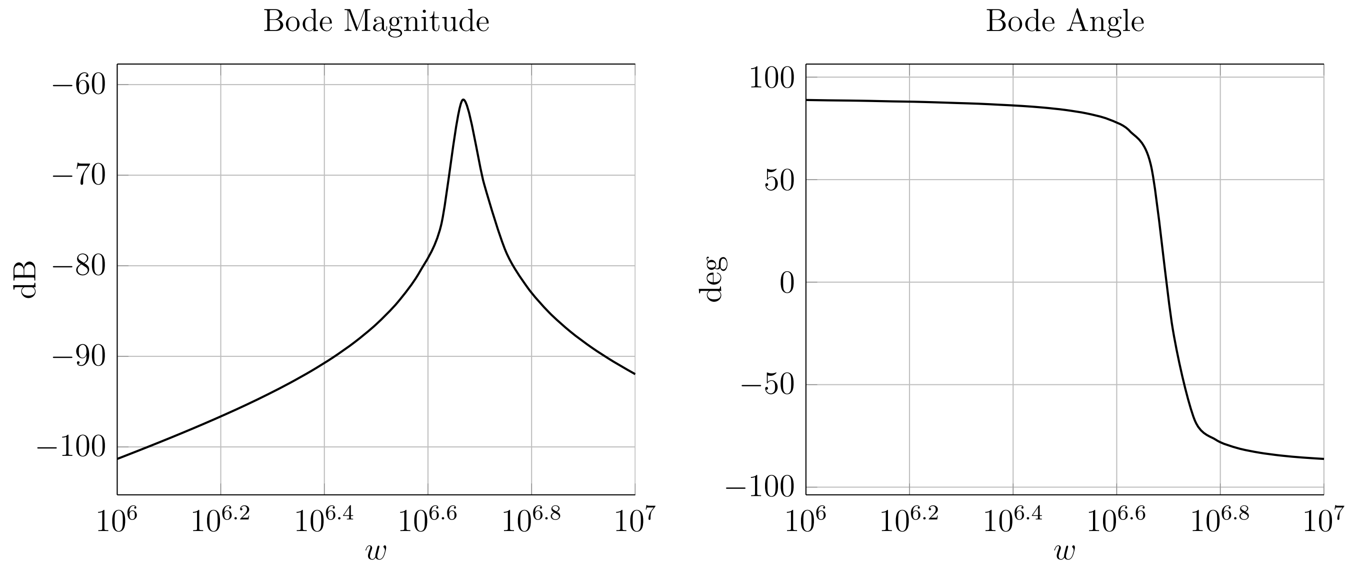


Figure 6.33: Bode Plot of a Radio Circuit

which yields $\omega_r = 5 \times 10^6 rad/s$, *that is,* $f_r = 796KHz \approx 800KHz$.

The magnitude plot shows that the peak occurs at $800KHz$ *approximately.*

□

[8]Explain why? Hint: The characteristic equation is $LCs^2 + \frac{L}{R}s + 1 = 0$

[9]Find w_1 and w_2 of this example respectively and verify it with Bode plot.

[10]Use the same R, L, C parameters given in Example 6.25, find its natural response and re-calculate its β and w_r.

6.5 Problems

Problem 6.1 *(a) What frequency is half way between 100 and 1000KHz on a* log *frequency scale? (b) On a linear frequency scale?*
Answer: *(a)* $\log \frac{x}{100} = \frac{1}{2}$*, thus x=316.2Hz. (b)550 Hz.*

Problem 6.2 *How may decades are between* $f_1 = 20Hz$ *and* $f_2 = 15KHz$ *(i.e., audio frequency)? (b) How many octaves*
Answer: *(a)* $\log \frac{15K}{20} = 2.87$ *(b) 9.55.*

Problem 6.3 *In the Figure 6.34, determine the cutoff frequency for the high-pass filter.*

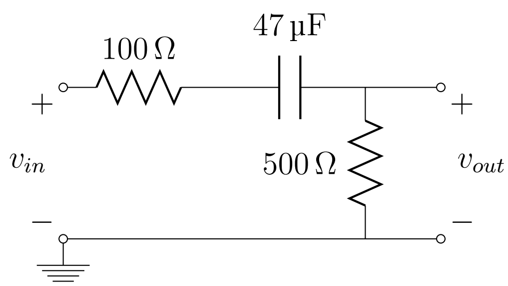


Figure 6.34: Circuit Diagram for Problem 6.3

Answer: *56.86 rad/s.*

Problem 6.4 *Suppose that an input signal given by*

$$v_{in} = 5\cos(500\pi t) + 5\cos(1000\pi t) + 5\cos(2000\pi t)$$

is applied to the low pass RC filter shown in figure for problem 6.35. (a) Find an expression for the output signal. (b) What is your observations when compared with the input signal.

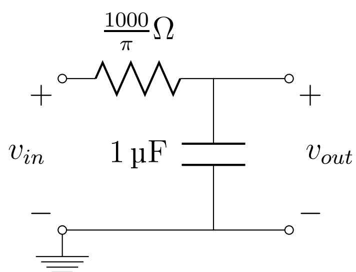


Figure 6.35: Circuit Diagram for Problem 6.4

Answer: *(a)* $v_{in} = 4.472\cos(500\pi t - 25.57°) + 3.535\cos(1000\pi t - 45°) + 2.236\cos(2000\pi t - 63.43°)$ *(b) The input frequency is unchanged, but the input magnitude is attenuated and its angle is shifted.*

Problem 6.5 *The following components are available to construct a parallel resonant circuit:* $L_1 = 7.5mH$, $L_2 = 15mH$, $C_1 = 6\mu F$, $C_2 = 3\mu F$ *and* $R = 2k\omega$. *Design a circuit that will have the highest possible resonant frequency. Specify (a)* w_r *(b)* w_1 *(c)* w_2 *(d)* β *(e)* Q. *(Hint: There are two ways to combine two similar elements – series and parallel.*
Answer: *(a)* L_{eq}*=7.5m//15m=5mH,* $C_{eq} = 6\mu + 3\mu = 2\mu F$, $w_r = 10^4$ *(b)* $w_1 = 9875.78$ *rad/s (c)* w_2*=10125.78 rad/s (d)* $\beta =$ *250 rad/s (e)* $Q = 40$.

Problem 6.6 *Up to present, you have learned 4 different filters LOW-PASS, HIGH-PASS, BAND-PASS, and BAND-REJECT. Given the circuits in Figure 6.36 (a) what kind of selective circuits they are and state the reason why. (b) find their transfer function respectively. (c) Draw the remaining filters and find their transfer function.*

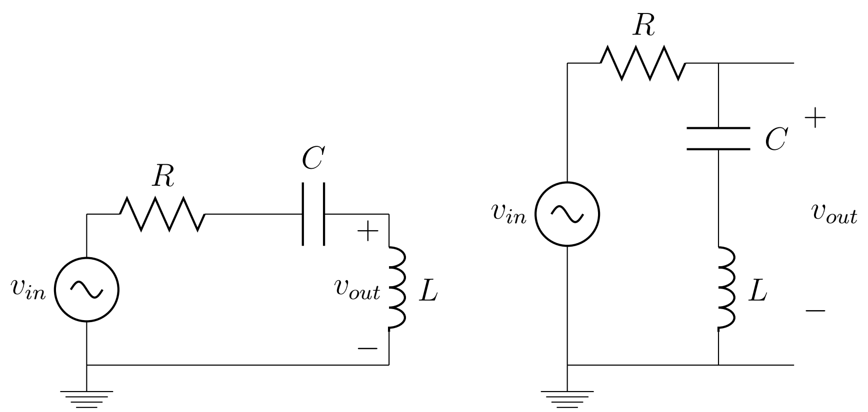


Figure 6.36: Circuit Diagram for Problem 6.6

Answer: *(a) High-pass,* $H(jw) = \frac{jwL}{r+jwl-j\frac{1}{wC}}$ *(b) Band-reject,* $H(jw) = \frac{jwL-\frac{1}{wC}}{R+jwl-j\frac{1}{wC}}$ *(c) when* V_R *is output, we have a band-pass filter (d) when* V_C *is output, we have a low-pass filter*

Problem 6.7 *Suppose that we want a series band-pass filter that passes components between 45-55KHz. Design a circuit using 1mH inductor (a) what is the* f_r *(2) Find* Q_s *(c) Find R using formula* Q_s. *(d) Find* C *using formula* f_r.
Answer: *(a)* $f_r = 50kHz$ *or* $100\pi k$ *Rad/s (b)* $Q_s = 5$ *(c)* $R = 20\pi\Omega$*(d)* $C = 0.101 \times 10^{-7}F$.

Problem 6.8 *Given a series RLC circuit, find its impedance in terms of R,* Q_s*, and* f_r.
Answer: $\bar{Z} = R[1 + Q_s(\frac{f}{f_r} - \frac{f_r}{f})]\Omega$.

Problem 6.9 *Given the circuit for problem 6.37, (a) find the type of filter when output is at the inductor terminal (b) when output is measured at LC terminal. Use Pspice to check the result.*
Answer: *(a) A high-pass filter (b) A band-reject filter.*

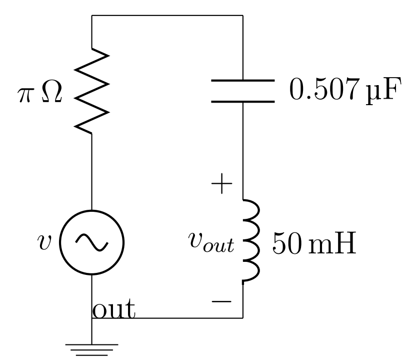


Figure 6.37: Circuit Diagram for Problem 6.9

Chapter 7

Diodes

Diodes are the simplest nonlinear element in electronics. They are constructed by p-type (holes) and n-type (free electrons) material, causing an electric field barrier near junction area. Their pn junction properties appear in almost all electronic elements to be taught in this book. Being familiar with diodes can be a crucial step in learning more complicated electronic devices. It is understandable, to keep this book brief, that we will skip the diode internal physics, but focus our discussion on the external behaviors of diodes and some of their circuit applications. To know more about diode physics please check the references for details.

7.1 Fundamentals

Diodes can only have two states for operations – ON or OFF; at any instant only one state (either ON or OFF) is valid. As shown in Figure 7.1, if a positive voltage $v_D > 0.6$ ($0.6V$ is known as a knee/threshold voltage) is applied to the diode, a large current can flow in the diode. This condition is termed forward bias. If a negative voltage v_D is applied to the diode, only a small current can flow until its breakdown voltage is reached in the diode and this is called reverse bias. It is noticed that when diode conducts, the resistance is very small, as can be seen by the vertical line in the $i - v$ curve whose slope is almost infinity. Theoretically, the current and voltage relationship of a pn junction diode is governed by Shockley equation

$$i_D = I_s(exp(\frac{v_D}{nV_T}) - 1) \approx I_s exp(\frac{v_D}{nV_T}) \tag{7.1}$$

where n parameter is related to type of material used in a diode. V_T is thermal voltage and I_s is saturation current on the order of 10^{-14}A. Diodes that are operated in the reverse bias region is called Zener diodes where breakdown voltage v_{break} at the reverse-bias region is reached.

PSpiceLab 7.1 ($i - v$ Characteristic of a Real Diode) *Given the following diode circuit where the real diode is modeled by D1N4002 in PSpice, use DC sweep from $-15V$ to $15V$ to generate the $v - i$ characteristic.*
Solution:

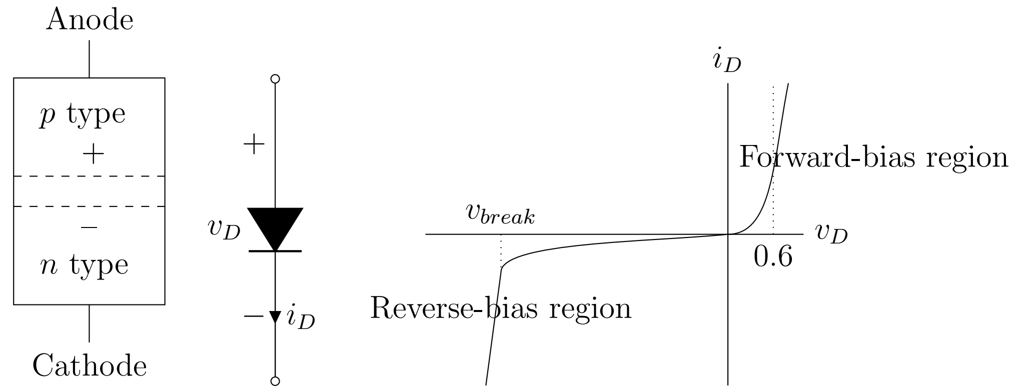
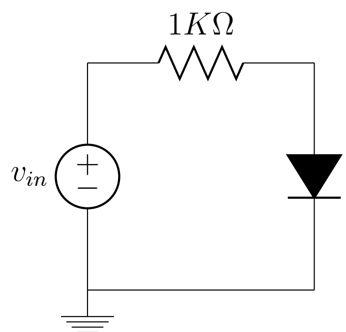


Figure 7.1: (a) A pn Junction, (b) Diode Symbol and (c) $i - v$ Characteristic



Objectives: (1) Verify the i/o characteristic of a diode. (2) Learn DC sweep technique. (3) Change axis variables.
PreLab: Understand a diode has two states – ON and OFF, which is controlled by the knee voltage.
Lab: The result confirms the analysis
PostLab: Can a mathematic model be devised to mimic the behavior of a diode?

□

Therefore to model a real diode, we often assume an offset/knee/threshold voltage value to be 0.6. This is the simplest gimmick, yet more to come.

7.2 Load-Line Analysis

Since a diode is a nonlinear circuit element, we don't know the value of v_D in a circuit. A graphic method provides a way to solve this problem. For example, consider a circuit in Figure 7.2. where v_s and R_s represent a Thevenin equivalent circuit and v_D is the diode voltage. To find the operating point (V_D, I_D), known as quiescent point, we write the KVL in a clockwise direction and yield

$$v_s = i_D R_s + v_D$$

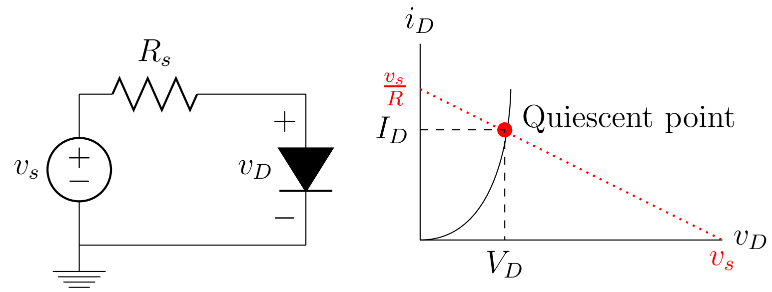


Figure 7.2: (a) Circuit (b) Load Line Analysis

This line can be found and drawn on the $i - v$ plot. To this end, find its interception points on x- and y-axis by setting $i_D = 0$ and $v_D = 0$. Then connecting these two lines to find the Q crossover point.

Example 7.1 (Real Diode) *Given a real diode circuit and its input waveform as shown below, find the output voltage waveform and the transfer function from v_{in} to v_{out}*

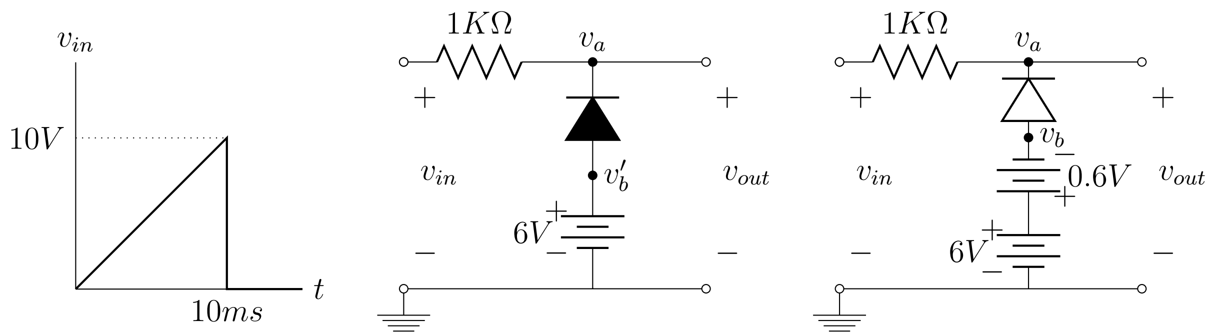


Figure 7.3:

Solution: *Obviously for the real diode to conduct, we must have $v_a \leq 5.4$ because $v_b = 5.4V$. Once it is conducting, the voltage v_a remains $5.4V$. For all voltage values between $10 \geq v_a > 5.4$, the real diode is an open circuit and thus, $v_{in} = v_{out}$. A diagram is depicted below.*

□

PSpiceLab 7.2 (Wave Shaping) *Redo Example 7.1 using PSpice.*
Solution:
Objectives: (1) Understand wave shaping capability of a diode. (2) Knee voltage can be designed by adding an external DC voltage.
PreLab: This diode circuit clips the low part ($V_{in} \leq 5.4V$) of the input signal.
Lab: The result confirms the analysis.
PostLab: Noticing that the line cutting the lower portion of the wave is NOT a line with zero slop (i.e, a horizontal line), but rather, it is a line with a slope of $1/r$.

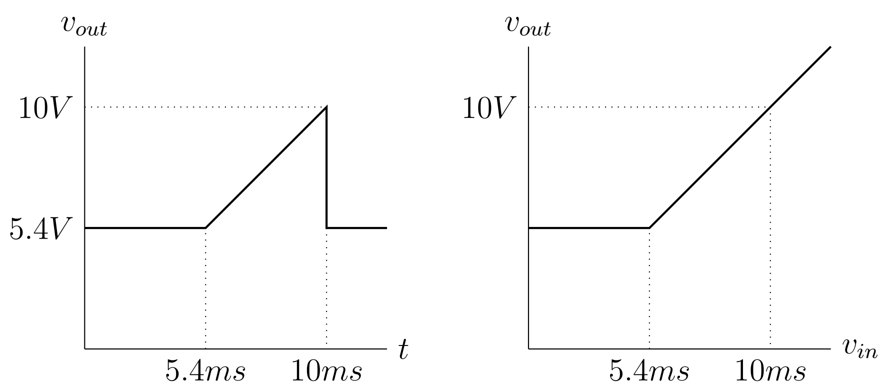


Figure 7.4: (a) Output Waveform and (b) Transfer Function

□

Example 7.2 (Zener Diode)

□

PSpiceLab 7.3 (Load Line Analysis) *Given the following Zener circuit where the Zener diode is modeled by D1N750 (whose break voltage is* $4.7V$*) in Pspice, use DC sweep from* $0V$ *to* $20V$ *to generate its* $i - v$ *characteristic. (b) Plot the load line.*

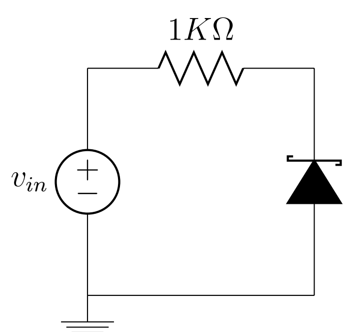


Figure 7.5: Load Line of a Zener Diode Circuit

Solution:
Objectives: (1) Understand reversed bias. (2) Lean DC sweep technique. (3) Draw a load line on PSpice probe window.
PreLab: To draw the load line, see Figure 7.2.
Lab: Follow the steps to find the result as theory has predicted.
PostLab: Why is that the direction of the Zener diode is reversed.[1]

□

[1] Ans: so that we don't need to reverse the polarity of source. Note that the plot is drawn on the first quadrant, not the third quadrant.

7.3 Ideal Diode Model

Ideal diode means the diode acts as a short circuit when the diode is forward-biased $v_D \geq 0$ and act as an open circuit when reverse-biased $v_D < 0$. Pictorially, we have the following figure to depict the idea. Moreover, another model, which is more accurate than the ideal one shown in red color, is to assume an offset value $0.6V$ directly as shown by the green color in the same figure.

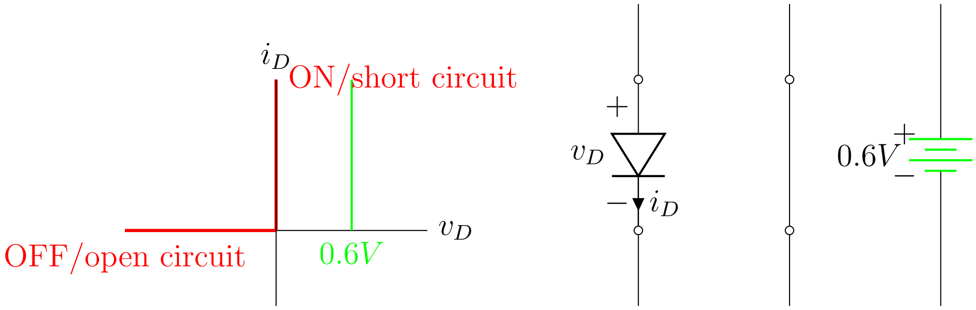


Figure 7.6: Ideal Diode Characteristic

7.3.1 Solving an ideal diode circuit

When solving a circuit containing ideal diodes, we don't know in advance which diodes are ON and which are OFF. A practical method to overcome this dilemma, solving a diode circuit, is to

- assume the state of diodes first,
- solve the assumed state condition to find a solution,
- check the consistency of the solution with the assumed states,
- If the result is consistent with the assumed states, the analysis is completed.
- Otherwise, restart from step 1.

Here is an example.

Example 7.3 (Analysis for Ideal Diodes) *Given a diode circuit, find the output voltage v_o for (1) $v_1 = v_2 = 5V$ (2) $v_1 = 5V, v_2 = 0V$, (3) $v_1 = v_2 = 0V$. Assume the diodes are ideal.*

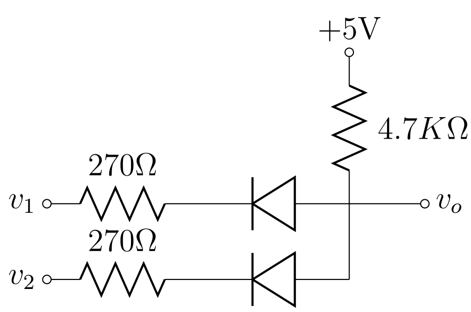


Figure 7.7: Circuit Diagram for Example 7.3

D_1	D_2
ON	ON
ON	OFF
OFF	ON
OFF	OFF

Solution: *There are $2^2 = 4$ possible scenarios for these two diodes to consider and they are*
(1) Assume D_1 is OFF and D_2 is OFF, meaning both diodes are open circuits and thus no current flowing through 4.7Ω resistor. So $v_o = 5$ confirms that both diodes must be OFF since v_0 is not larger than 5V.
(2) Assume D_1 is ON and D_2 is OFF, meaning D_1 is short circuit while D_2 remains open. Under this assumption, we should have current passing through D_1, but it is zero for $i_1 = \frac{5-5}{4970} = 0$. This is the contradiction we seek – NO GO.
Further D_1 is OFF and D_2 is ON, meaning D_2 is short circuit while D_1 remains open. Under this assumption, we should have current passing through D_2 and it is $i_1 = \frac{5-0}{4970} = 1mA$, which confirms the second trial assumption is correct. Thus, $v_0 = 5 - 4.72 = 0.27V$ Notice that if the second trial were in correct then we would have to go for a third trial and a forth trial.
(3) Assume D_1 is ON and so is D_2, meaning both are conducting currents. $i_1 = i_2 \frac{5}{4970} = 1mA$ and $v_0 = 0.27V$.
Actually, this is an AND gate in the view of digital logic.

• If a knee voltage, say $0.6V$ is assumed for a diode, then we need to take the given knee voltage into consideration. This is the topic of next section.

□

7.4 Piecewise-Linear Diode Model

If we need a more accurate diode model than the ideal model, a linear model, inspired by Figure 7.1 and introduced here, is usually considered. To derive, we write the linear model satisfying KVL as

$$v = iR_D + V_D \tag{7.2}$$

where R_D denotes the diode resistance and V_D denotes the knee voltage of the diode. It is verifiable that equation (7.2) is the line in Figure 7.8, R_D is the inverse of the slope and V_D is an intersection point of equation (7.2) with x-axis. By varying the slope, we can have equation (7.2) approximates the curve in Figure 7.1(c), representing the forward bias curve.

Example 7.4 *Given the following piecewise linear model, Figure 7.9, find the corresponding circuit model.*
Solution: *First, find the resistor for segments $0a$ and ab by inverting the corresponding slope of segments. Second, find the intersection of each segment at x-axis, which is zero and -2, respectively.*

□

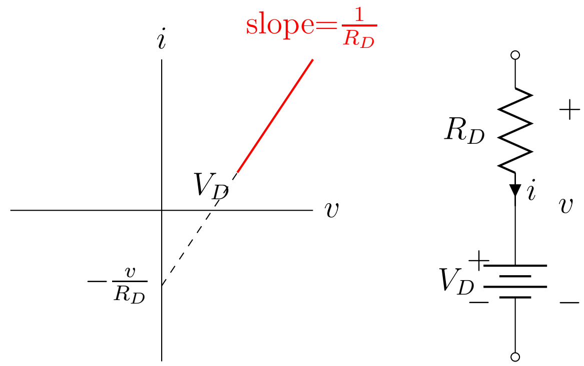


Figure 7.8: A Linear Function and Corresponding Circuit Model

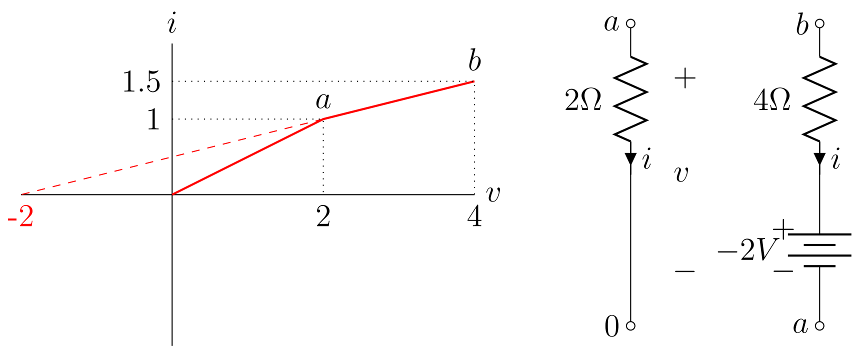


Figure 7.9: A Linear Function and Corresponding Circuit Model

In sum, we can use a piecewise-linear model to approximate the real model in Figure 7.1. However, another much simple linear model (vertical line) is often seen in application too. We that

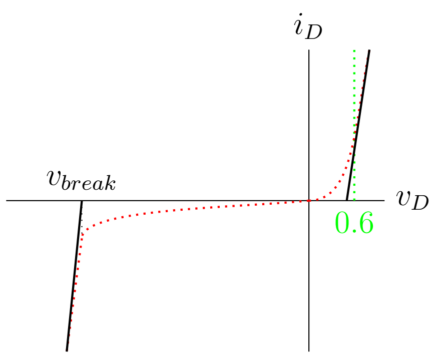


Figure 7.10: Graphic Model to Approximate a Real Diode Characteristic

information, we have established a piecewise-linear model model for the real diode.

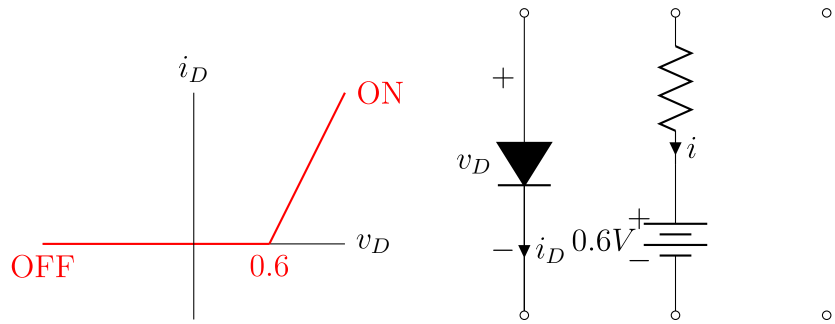


Figure 7.11: Piecewise-Linear Diode Characteristic

7.5 Small Signal AC Circuit Analysis

Since a real diode has a nonlinear v_D-i_D characteristic, the piecewise linear model provides an excellent technique to utilize a diode element in a circuit. We use a DC voltage to bias a nonlinear device at an operating point (as seen in the load line analysis) and then linearize the nonlinear device at the operating point. In a diode model, a dynamic resistor is therefore found. To see this, we recall the Shockley equation

$$i_D = I_s(exp(\frac{v_D}{nV_T}) - 1) \approx I_s exp(\frac{v_D}{nV_T}) = I_{DQ} + i_d \tag{7.3}$$

Linearizing, we have

$$\frac{di_D}{dv_D}|_{V_{DQ}} = \underbrace{I_s(exp(\frac{v_{DQ}}{nV_T})}_{I_{DQ}} \frac{1}{nV_T} = \frac{I_{DQ}}{nV_T} = \frac{1}{r_D}$$

Taking reciprocal of the above equation yields

$$r_D = \frac{nV_T}{I_{DQ}} \tag{7.4}$$

The linearization technique, Q-point determination and AC excitation are illustrated in the following diagram.

To implement the idea, we have the following circuit displayed in Figure 7.13 where C_1 is called bypassing capacitor whose capacitance is so large that it serves as a short circuit to the AC signal while functioning as an open circuit for DC signal. The quiescent operating point (Q point) is unaffected by AC source or the load. Therefore, conceptually, we have the following two circuits. The significance of this demonstration is that a nonlinear diode circuit is transformed into a linear circuit and the circuit theory from Chapters 1 $\sim$ 6 can be readily applied. To continue, the voltage gain is easily obtained as

$$A_v = \frac{v_{out}}{v_{in}} = \frac{R_p}{R + R_p} < 1$$

where $\frac{1}{R_p} = \frac{1}{R_C} + \frac{1}{r_d} + \frac{1}{R_L}$. Since the gain is less than unity, it is called a voltage attenuator.

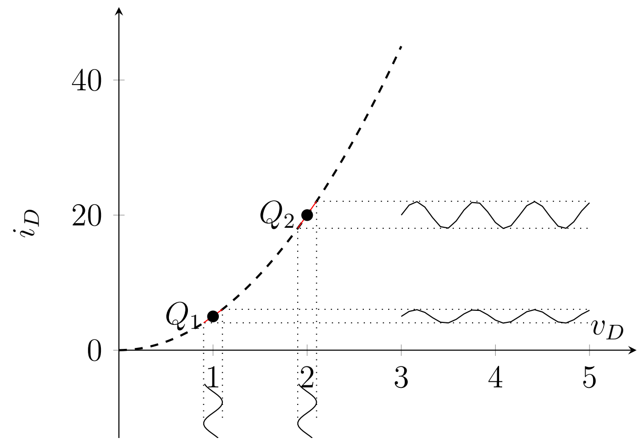


Figure 7.12: Linearization, Q Points and Magnification

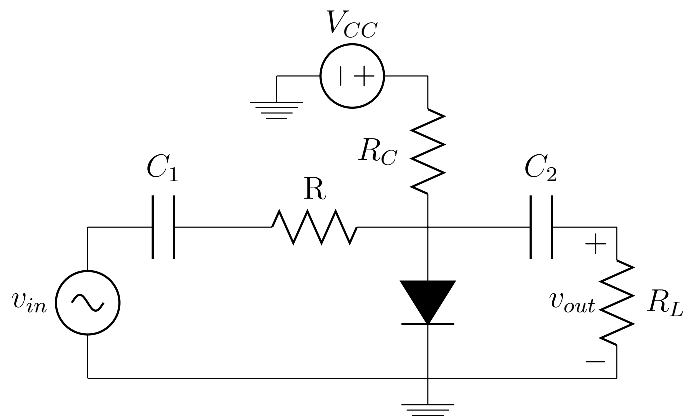


Figure 7.13: Nonlinear Diode Circuit

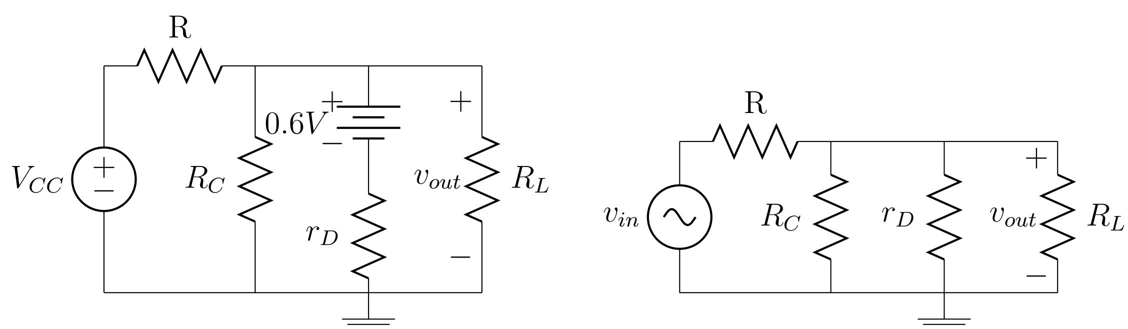


Figure 7.14: (a) DC Bias Circuit and (b) AC Excitation Circuit

Figure 7.14(a) is known as large-signal analysis and Figure 7.14(b) is known as small-signal analysis whose signal magnitude is always smaller than knee voltage $0.6V$ and thus named.

Example 7.5 (Bypassing Capacitor) *Given Figure shown below, find the voltage across* 2Ω.

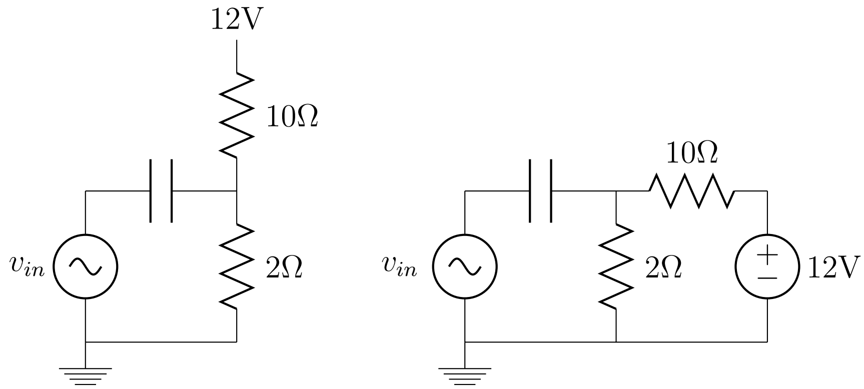


Figure 7.15: Circuit Diagram for Example 7.5

Solution: *Since an equivalent circuit is shown, we can applied superposition technique to solve it. For AC analysis, we have $v_1 = v_1'$. For the DC analysis, the capacitor becomes an open circuit and the voltage across 2Ω is $v_1'' = 2V$. The total voltage across 2Ω is than $v_1 = v_1' + 2V$. The example*

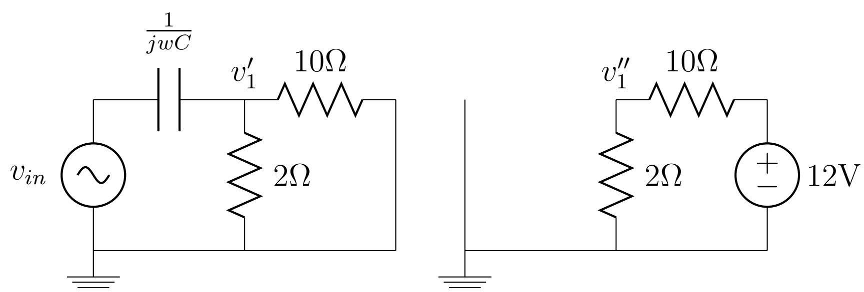


Figure 7.16: Small Signal Circuit and Bias Circuit

shows that bias DC source and small signal AC source using bypassing capacitor enable the circuit to be treated independently as two sources in a linear system that superposition is applied. This means the DC source is used to find Q point and AC source is used to find magnification.

□

Example 7.6 *Given the following diode circuit, find (a) voltage of R_L due to bias circuit and the voltage due to small signal. Assume $V_T = 25$, $n = 2$ for silicon and a real diode model is given by knee voltage $V = 0.6$ and $R = 10\Omega$.*
Solution: *For the DC bias analysis to find Q point, we have*

$$i_D = \frac{9 - 0.6}{10 + 2000} = 4.18mA$$

resulting in $V_{R_L} = 8.358V$. Also by equation (7.4), we obtain

$$r_D = \frac{2 \times 25}{4.18} = 12\Omega$$

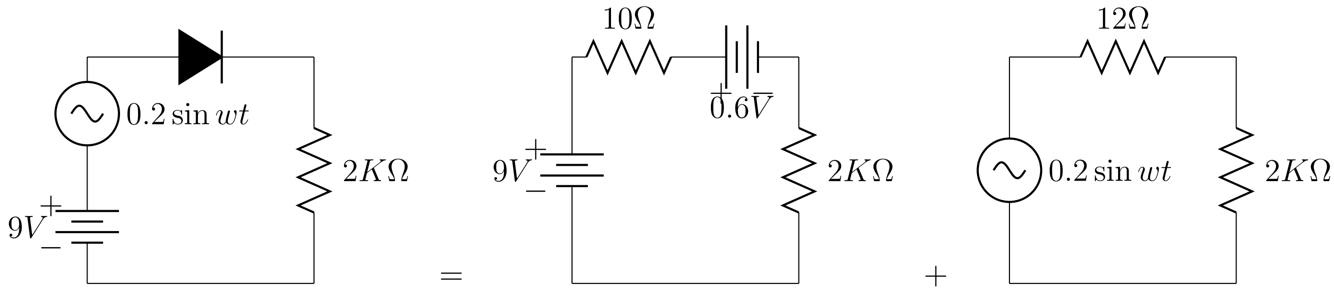


Figure 7.17: (a) DC Bias Circuit and (b) AC Excitation Circuit

For AC analysis, we have

$$v_{R_L} = \frac{0.2 \sin wt \times 2000}{2012} = 0.199 \sin wt$$

Thus, $v_{R_L} = 8.358 + 0.199 \sin wt$.

□

7.6 Nonlinear Circuit Applications

Diodes can have many applications that are often seen in applications. The basic idea behind all these is based on the binary state of diodes – ON and OFF states.

7.6.1 Rectifier circuits

Consider a rectifier circuit with a capacitor in parallel with an output load. First, we will consider

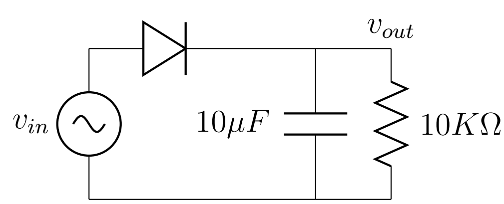


Figure 7.18: Half-Wave Rectifier with Smoothing Capacitor

the circuit without the capacitor. The diode will conduct every half cycle, resulting in a half-wave rectification as shown in Figure 7.19. Now adding capacitor, then during the OFF state, the *RC* circuit to the right of diode is discharging and thus the output voltage drops slowly until the diode is ON again. So this is the ideal how an AC voltage is converted into a DC voltage that supplies direct current to home appliances that requires DC such as personal computers.

PSpiceLab 7.4 (Full-Wave Rectifier) *Based on Figure 7.18, reverse the input AC source and plot the output voltage to see if any difference is observed when compared with Figure 7.19. Now*

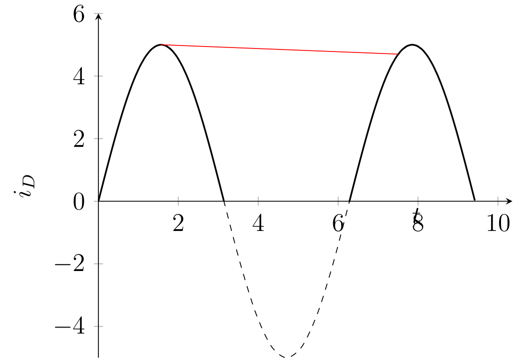


Figure 7.19: Half-Wave Rectifier Waveform

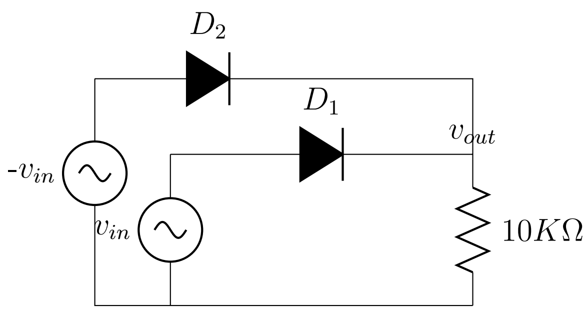


Figure 7.20: Full-Wave Rectifier

design a full-wave rectifier.

Solution

Objectives: From half-wave to full wave rectifiers.

PreLab: Study the idea half-wave rectifier and notice that knee voltage is assumed zero.

Lab: Follow the steps to gather ideas. It is noted that the peak value is less than an idea diode case. Why?[2]

PostLab: What will result if a smoothing capacitor is placed at the output terminal?[3]

□

7.6.2 Limiting circuits (diode clippers)

A clipper circuit clips off the some part of the input signals. In this section, we assume the diodes have $0.7V$ threshold voltage.

Based on the diode assumption, as long as v_a is less than $0.7V$, the diode is open (because it take more than 0.7 to make the diode admit conducting), meaning no voltage drop on the R resistor, therefore, $v_{in} = v_{out}$. When $v_a \geq 0.7V$ then the output will remain at $0.7V$ drop of the assumed

[2] Ans: This is because a real diode have offset value about $0.6V$.

[3] Ans: Then a similar result as shown in Figure 7.19 will smooth the curve.

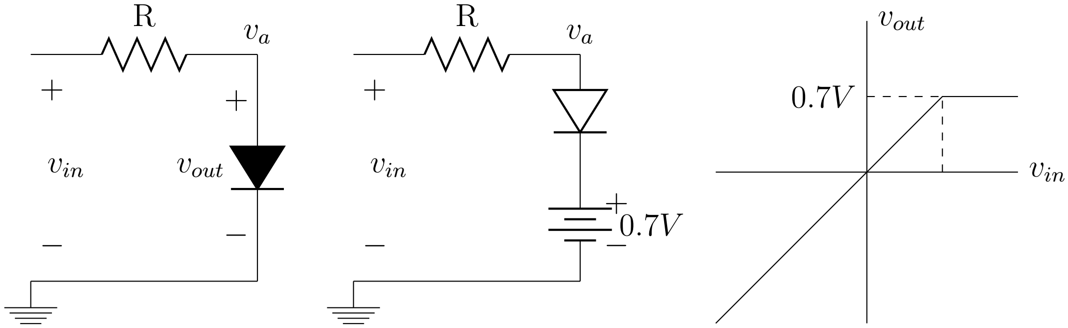


Figure 7.21: Clipper Circuit 1

voltage.

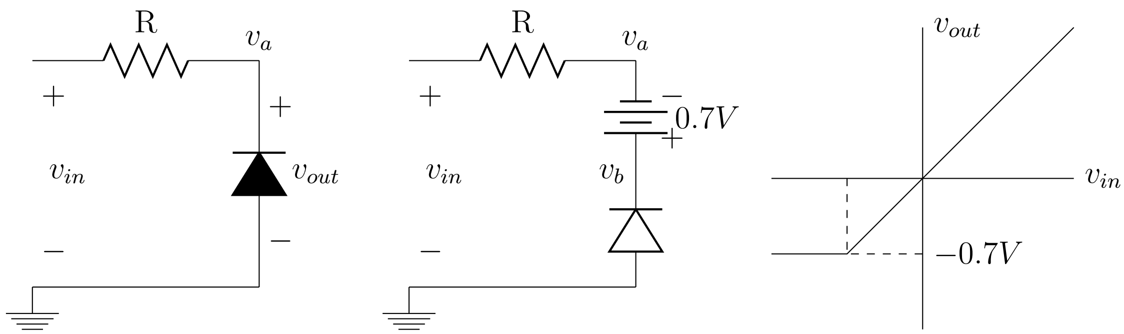


Figure 7.22: Clipper Circuit 2

Now for Figure 7.22, the direction of the diode is reversed. Whenever v_a is higher than $-0.7V$, the ideal diode remains open (because $0 - v_b < 0$) and no current flows through the branch, resulting $v_{in} = v_{out}$. When $v_a < -0.7$, the diode conducts and the drop of $-0.7V$ appears.

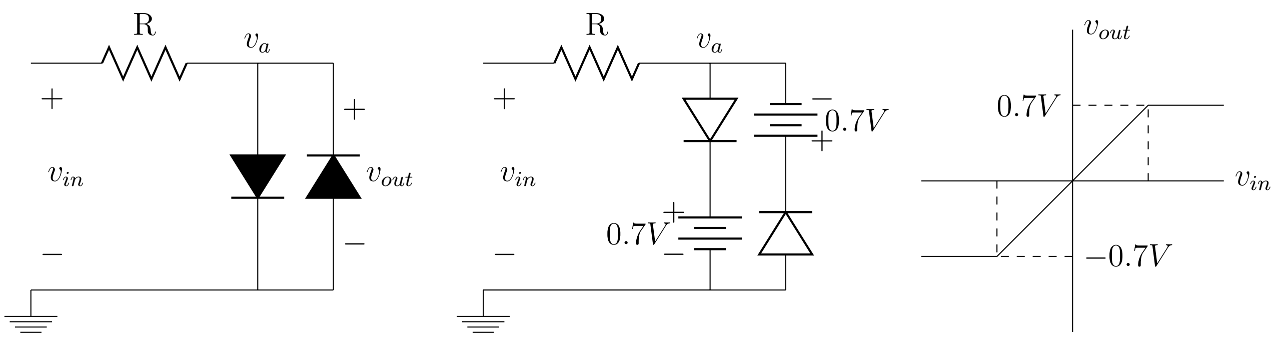


Figure 7.23: Clipper Circuit 3

For Figure 7.23, the reasoning for this clipper circuit is the combined notions of those of previous examples.

PSpiceLab 7.5 (Clipper Circuit) *Given the following clipper circuit where the real diode is modeled by D1N4002 in PSpice, (a) find the clipped waveform v_{out}, given the AC voltage. (b) Plot the transfer function $\frac{v_{out}}{v_{in}}$.*

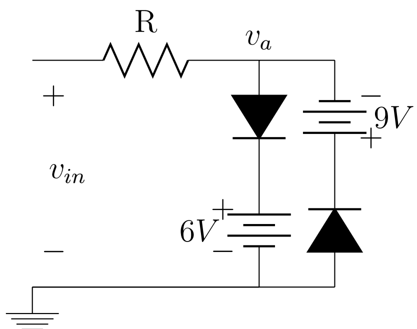


Figure 7.24: Circuit Diagram for PSpiceLab 7.5

Solution:
Objectives: (1) Understand how a clipper circuit works. (2) Understand polarity of knee voltage of real diode can make a difference.
PreLab: Review the analytical skills for clipper circuits.
Lab: Follow the steps to see the result.
PostLab: What happens if the direction of diodes or the direction of DC battery is reversed?[4]

□

7.6.3 Clamp circuits

For the circuit below, it moves up or down the input AC signal by adding a DC signal to the input and clamps it at the new position so that the peak of the AC signal takes a specified value. In this example, the output voltage is given by $v_{out} = v_{in} + 6V$. In other words, the output is clipped to $10V$. To lower the peak, just reverse the C polarity. Notice that the capacitance of the capacitor is so large that its impedance $\frac{1}{jwC}$ is small for the AC signal.

PSpiceLab 7.6 (Clamp Circuit) *Given the following clamp circuit where the real diode is modeled by part D1N4002 in PSpice library, plot the clamped waveform v_{out}, given the AC voltage.*
Solution:
Objectives: (1) Understand how a clamp circuit works. (2) Understand the difference between Clipper and clamp.
PreLab: Review the analytical skill involved in clamp circuit.
Lab: Follow the steps to find results as expected.
PostLab: What happens if the direction of diodes or the direction of DC battery is reversed?[5]

[4]It will the negative peak.
[5]It will clamp the negative peak.

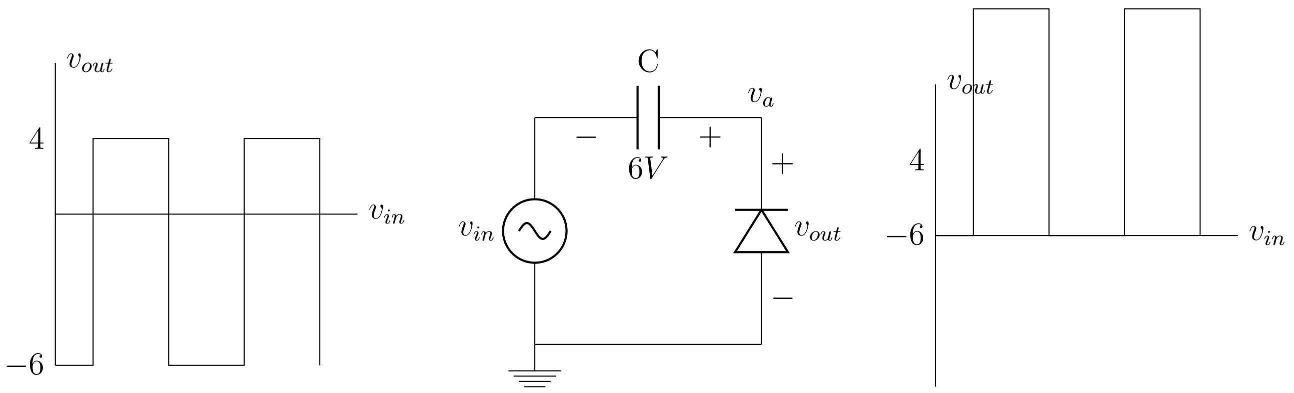


Figure 7.25: Clamp Circuit

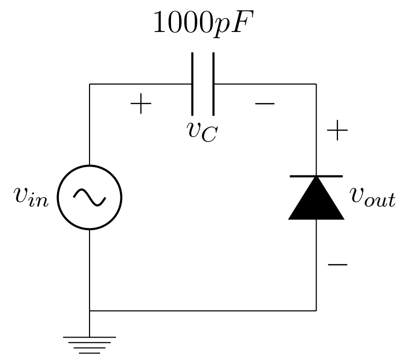


Figure 7.26: Circuit Diagram for PSpiceLab 7.6

□

7.7 Saturation and Clipping

When studying a nonlinear device, we normally want to operate the device at linear regions where linearization is applicable and nonlinear circuits becomes linear circuits and, therefore, circuit theory can be applied. However, we also need to understand some phenomena when the device is operated at extremes. This is better understood by plotting those phenomena. One is saturation associated to the property of the device itself and the other is associated to the output signals.

Here we assume a Q-point is established and it is located at the origin in Figure 7.27. We also assume that the device saturates when $v_{in} > 3$.

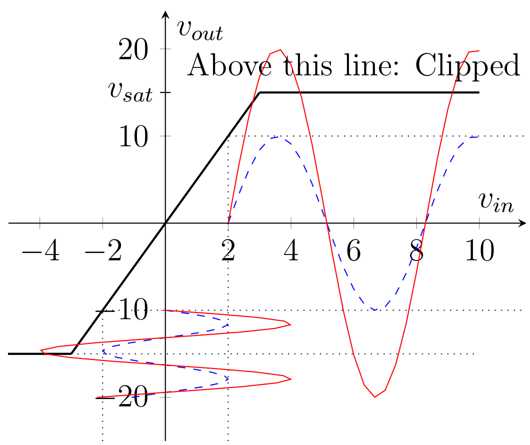


Figure 7.27: Saturation and Clipping

7.8 Recap

In this chapter, we have explored

- Nonlinear property of diodes.
- Different model to mimic the behavior of a diode.
- DC bias circuit to establish Q point.
- Linearization of an exponential function is used to find the small-signal circuit.
- Small-signal AC excitation circuit for amplification, but $A < 1$.
- Transformation from a diode circuit to the corresponding linear resistor circuit and vice versa.
- Usage of bypassing capacitors.
- The meaning of saturation and clipping.

7.9 Problems

Problem 7.1 *Find the values of I and V for the circuit of Figure 7.28 assuming that the diodes are ideal.*

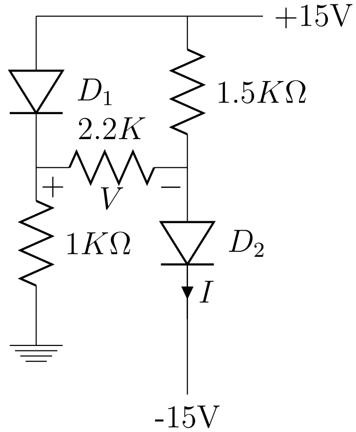


Figure 7.28: Circuit Diagram for Problem 7.1

Answer: $I = 5mA, V = 5V$.

Problem 7.2 *For the circuit of Figure 7.29, assume that D_1 and D_2 are ideal diodes. (a) For what range of values of V_1 is diode D_1 forward-biased? (b) For what range of values of V_1 is diode D_2 forward-biased?*

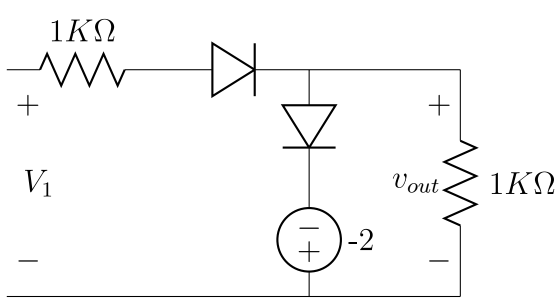


Figure 7.29: Circuit Diagram for Problem 7.2

Answer: *(a)* $V_1 \geq 0$, *(b)* $V_1 \geq 4$.

Problem 7.3 *Two identical silicon diodes, are connected as indicated in Figure 7.3. Assume the diodes have a threshold voltage of 0.5 V. (a) Find and plot the output voltage V_o versus V_{in} for $-6V \leq V_{in} \leq 6V$. (b) What is the max. current flowing in Figure 7.3. (c) If the 5 Ω resistor is rated at 1 W, what will happen if case (b) occurs.*
Answer:*(a) (b)* $I_{max} = 0.5A$. *(c) Burned out.*

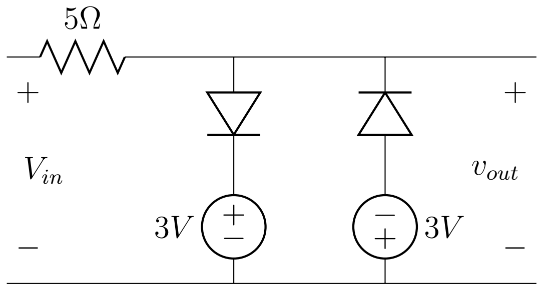


Figure 7.30: Problem 7.3

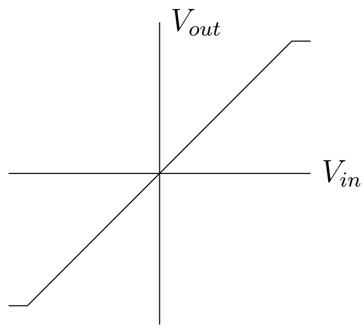


Figure 7.31: Solution for Problem 7.3

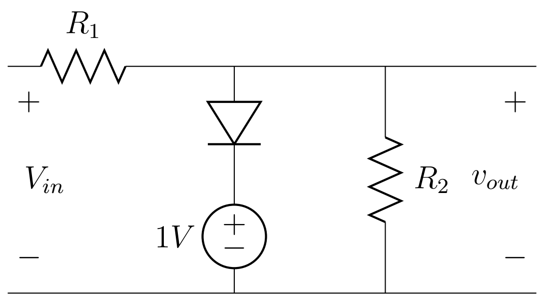


Figure 7.32: Circuit Diagram for Problem 7.4

Problem 7.4 *For a diode circuit as shown in Figure 7.32 with $v_{in} = 6\cos wt$, (a) find and plot the v_{out}. (b) Find and plot the v_{out} when R_2 is removed.*
Answer:

Problem 7.5 *The circuit below, Figure 7.33 contains two real silicon diodes. (assume $V_T = 0.7$ V.) (a) For switch S closed, estimate I_A and I_B for $V_A = -2, -1, 0, 1,$ and 2 V. (b) For switch S open, estimate I_A and I_B for $V_A = 1V$.*

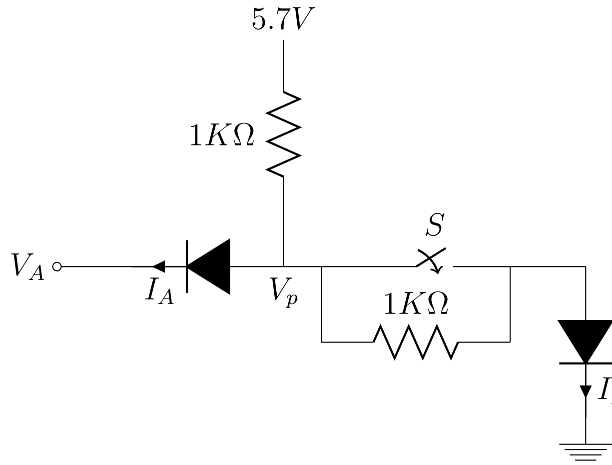


Figure 7.33: Circuit Diagram for Problem 7.5

Answer: *For S closed,*

V_A	I_A	I_B
-2	7mA	0A
-1	6mA	0A
0	2.5mA	2.5mA
1	0 mA	5mA
2	0 mA	5mA

For S open, $V_P = 1.7$, $I_p = 4mA$, $I_B = 1mA$, $I_A = 3mA$.

Problem 7.6 *For the circuit in Figure 7.34, sketch* i_D *for the following conditions: (a) Use the ideal diode model. (b) Use the ideal model with offset* $V_D = 0.6$. *(c) Use the piecewise linear approximation with* $r_D = 1K\Omega$, $V_D = 0.6V$.

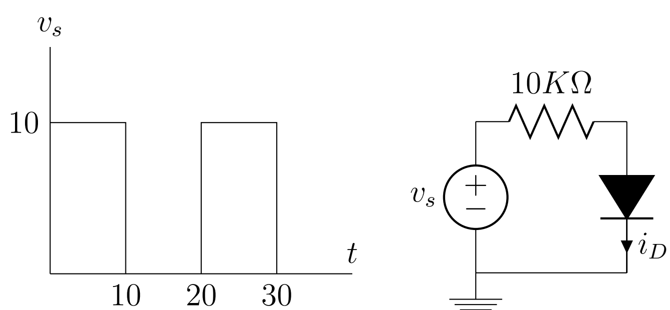


Figure 7.34: Circuit Diagram for Problem 7.6

Answer:*(a)* $i_D = 10/10K = 1mA$. *(b)* $i_D = 10 - 0.6/10K = 0.94mA$. *(c)* $i_D = 10 - 0.6/11K = 1mA$.

Problem 7.7 *Assuming the diodes in the circuit of Figure 7.36 are ideal, answer the following questions: (a) The two cases where both diodes are on and off are impossible, why? (b) Find the*

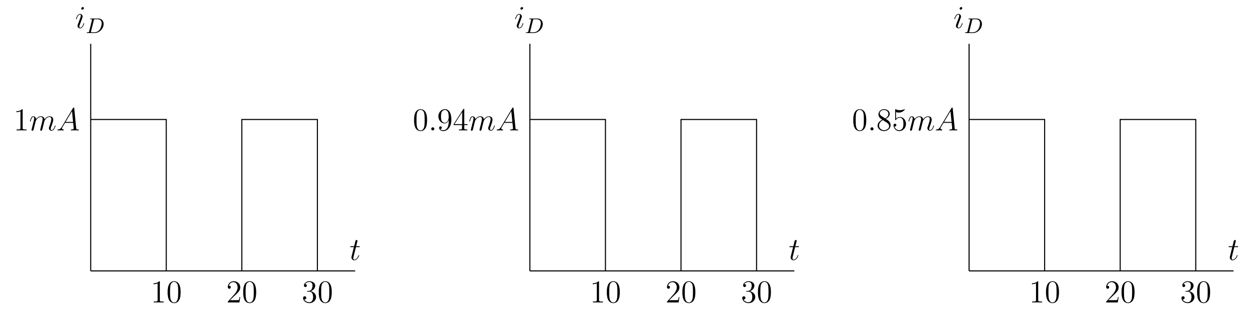


Figure 7.35: Solution for Problem 7.6

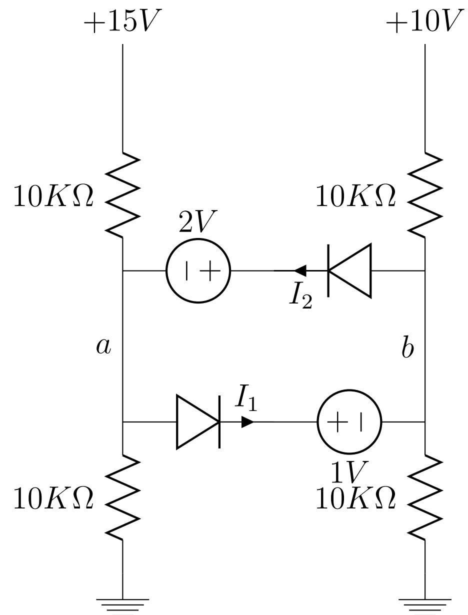


Figure 7.36: Circuit Diagram for Problem 7.8

label voltages,V_{ab}. (c) Find the currents, I_1, I_2. (Hint: Voltage at point a and point b)
Answer: *(a) that both diodes are ON leads to $2 \neq -1$ and that both diodes are OFF leads to $V_a = 7.5 > V_b = 5V$. Thus D_1 must be ON and D_2 must be OFF. (b)$V_{ab} = 1V$. (C) $I_1 = 0.15mA$.*

Problem 7.8 *Assume that the practical diode in Figure 7.37 has the characteristic of* $R_d = 3.66\Omega$, *and* $V_d = 0.8V$, *where* $C = \infty$. *Please find (a) the circuit for dc bias analysis. (b) The the circuit for AC analysis. (c) The voltage drop of 90*Ω *due to DC voltage. (d) The voltage drop of 90*Ω *due to AC voltage.*

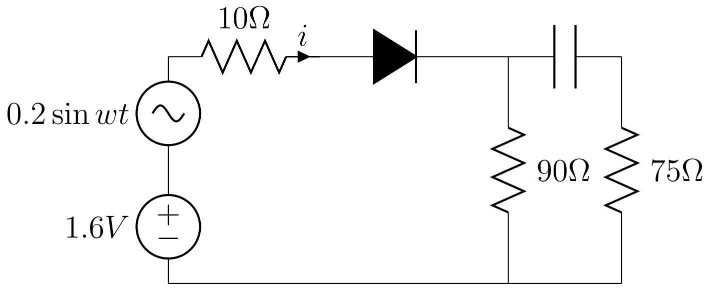


Figure 7.37: Circuit Diagram for Problem 7.7

Answer:

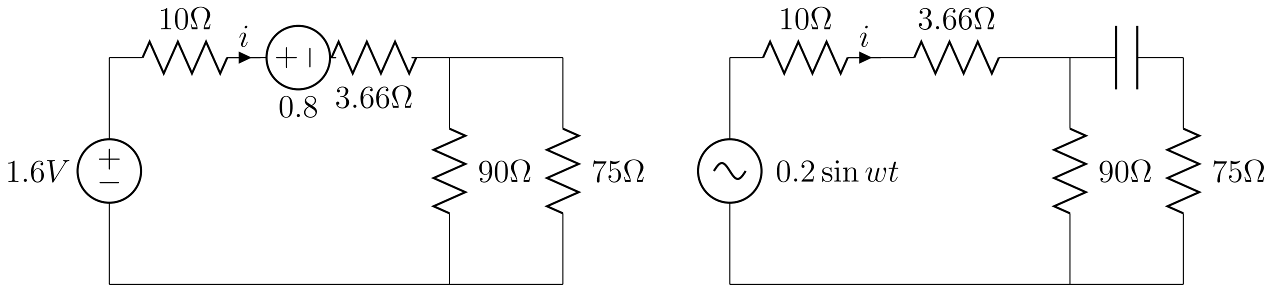


Figure 7.38: Solution for Problem 7.7

(c) $V_{90\Omega} = 0.6946V$. *(d)* $V_{90\Omega} = 149mV$.

Problem 7.9 *For the circuit in Figure 7.39, find the output voltage V_{out} if the input voltage V_1 and V_2 are as follows. Assume ideal diodes. (a) $V_1 = 5V, V_2 = 5V$. (b) $V_1 = 5V, V_2 = 0V$*

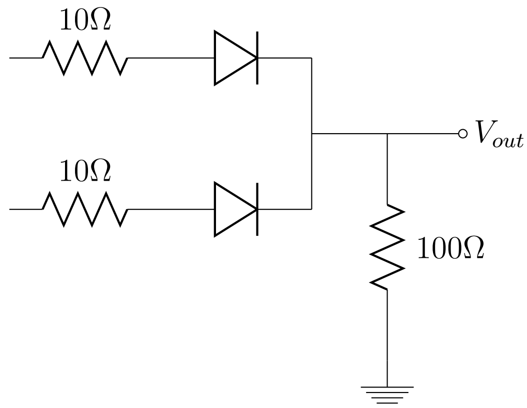


Figure 7.39: Circuit Diagram for Problem 7.9

***Answer**: (a) $V_{out} = 4.76V$. (b) $V_{out} = 4.545V$.*

Problem 7.10 *Determine whether the ideal diode in Figure 7.40 assuming that the diodes are ideal.*

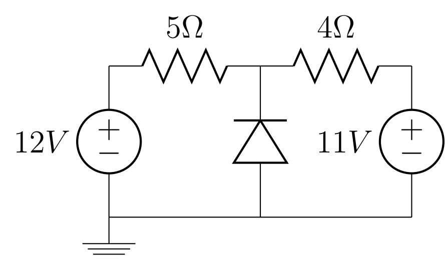


Figure 7.40: Circuit Diagram for Problem 7.10

***Answer:** Yes, it is ON.*

Problem 7.11 *Assuming the diode in the circuit of Figure 7.11 is ideal, plot the v_{R_2} voltages for the following cases. (a) $R_1 = R_2$. (b) $R_1 = R_2/2$. (c) $R_1/2 = R_2$. (d) R_2 is removed. (e) What is the ratio of R_1/R_2 so that the diode will critically conduct.*

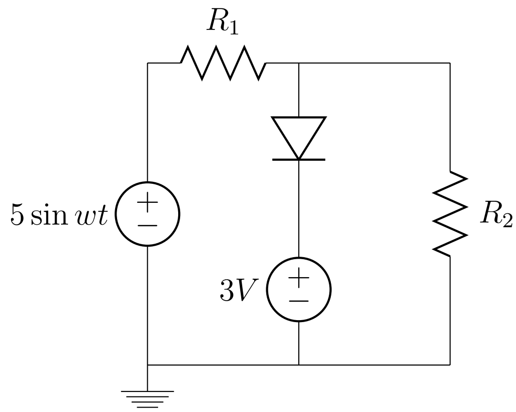


Figure 7.41: Circuit Diagram for Problem 7.11

Answer: *(a) and (c) are conducting but with* 2.5 *and* 1.67 *magnitudes. (b) and (d) are clipped at +3V. (e)* $R_1/R_2 = 2/3$.

Problem 7.12 *Assuming the diode in the circuit of Figure 7.12 is ideal, find the range for v_1 such that (a) diode D_1 is forward-biased. (b) Find the range for v_1 such that diode D_2 is forward-biased.*

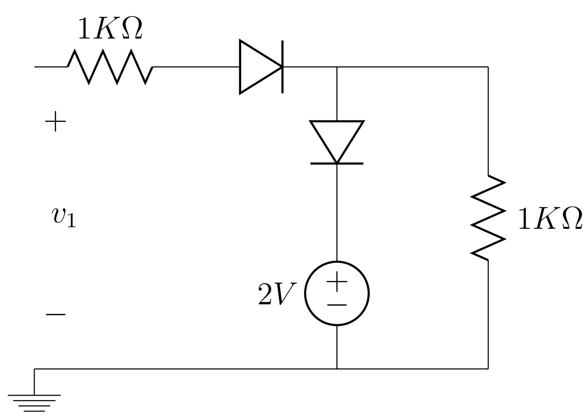


Figure 7.42: Circuit Diagram for Problem 7.12

Answer: *(a)* $V_1 \geq 0V$. *(v)* $v_1 \geq 4V$.

Chapter 8

Operational Amplifiers

An operational amplifier (op-amp) is a DC-coupled, high-gain electronic voltage amplifier with a differential input and a single-ended output. An op-amp produces an output voltage that is, at least, 10^6 times larger than the voltage difference between its input terminals. The gain of amplification is largely determined by the external components, not by variations in the op-amp itself and hence gaining its popularity. Operational amplifiers are important building block in an electronic device.

8.1 Fundamentals

Let's consider the following circuit that involves a voltage-controlled voltage source (part E in PSpice).

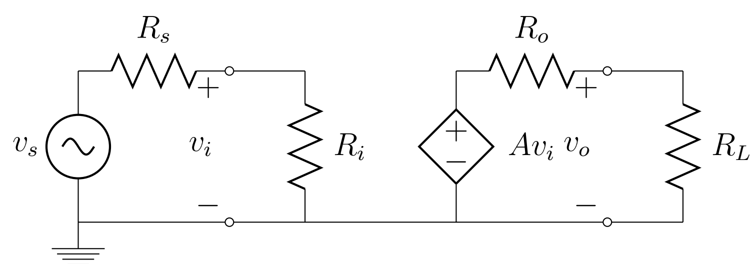


Figure 8.1: A Real Amplifier

where v_s and R_s represent a Thevenin equivalent circuit, R_i is input resistance, R_o is output resistance of the amplifier and R_L is the load resistance. A is called the gain of the amplifier. To continue, we define the voltage amplified to be

$$\begin{aligned} A_{real} &= \frac{v_o}{v_i} \\ &= \frac{A\frac{v_s R_i}{R_s+R_i}\frac{R_L}{R_o+R_L}}{v_s} \\ &= A\frac{R_i}{R_s+R_i}\frac{R_L}{R_o+R_L} \end{aligned} \tag{8.1}$$

Observing (8.1), it is readily seen that $A_{real} < A$ because the resistance ratio is less than one. However, An ideal op-amp has very high input impedance (for derivational purpose, it is often assumed to be infinite) and low output impedance (which is assumed to be zero). To see this, if we assume $R_i = \infty$ and $R_o = 0$ then $A_{real} = A$. With that in mind, we formally state that for an ideal amplifier we assume

- A negative feedback is used. (An op-amp almost always uses this structure.)
- $R_i = \infty$ ie., open
- $R_o = 0$ ie., shorted

It is readily seen that under the assumption on input and output resistances, we, from the gain equation (8.1), have $A_{real} = A$. Furthermore, these two assumptions lead to the differential input current is zero and the input voltage is zero too, which is called the summing-point constraint, also known as virtual short circuit or equally known as virtual open circuit. Thus, we have the following ideal amplifier model

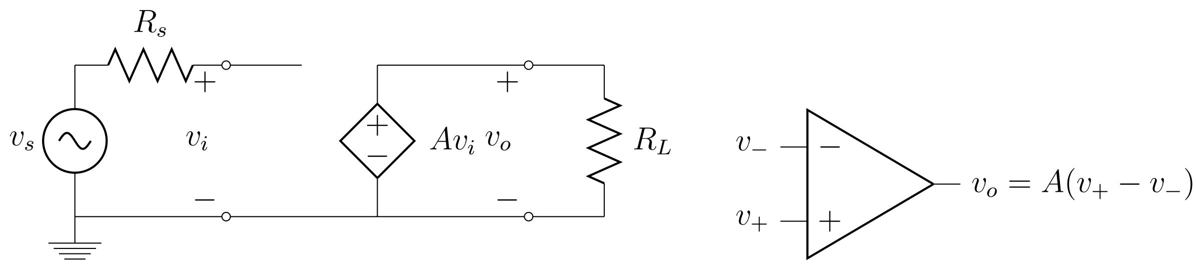


Figure 8.2: An Ideal Amplifier

Since the student version of PSpice has limitations (2) on number of op-amps being used in the free version, we may, instead, use the voltage-controlled voltage source (i.e., part E in PSpice) to overcome the limitations. In such case, we set the gain of part E to $1E10$, when using voltage-controlled voltage source to substitute the op-amps. Note that in PSpice student version only UA741 is available.

8.2 Amplifier Circuits

An interesting property of the ideal amplifier above is that the output voltage is only a function of the **difference** of the two input terminals. As such, There are some useful amplifier circuits, known as operational amplifier (op-amp), based on the ideal amplifier model.

8.2.1 Inverting amplifier

As shown in Figure 8.3

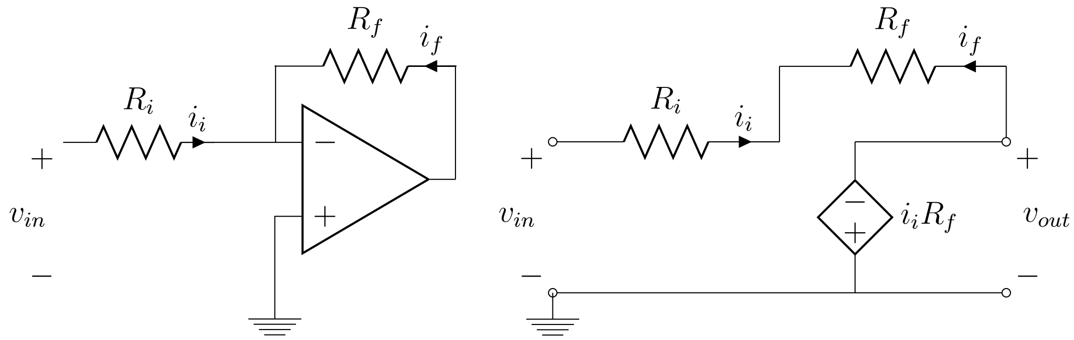


Figure 8.3: Inverting amplifier

Since $v_o = A(v_+ - v_-) = -Av_-$ and A is a high amplifier gain, we have $v_- = \frac{v_{out}}{A} \approx 0$. Furthermore, due to high input impedance R_i, the current flowing into the amplifier is zero. Applying KCL at node v_- yields

$$0 = i_1 + i_f = \frac{v_{in}}{R_1} + \frac{v_{out}}{R_f}$$

Thus the amplifier gain for this inverting amplifier is

$$v_{out} = -\frac{R_f}{R_1} v_i = -A_f v_{in}$$

The negative sign in the expression simply says that the output voltage is 180° out of phase with the input voltage. Also, based on the sign convention, there is a minus sign in from of ohm's law. Note that the gain A_f is independent of A and that the output voltage is independent of the load R_L.[1] This means that the Thevenin resistance seen by R_L is zero. Hence, we have an ideal voltage source at the output terminals. This also renders itself an equivalent current-controlled voltage source.

Example 8.1 *[2, Page 197] For the circuit Figure 8.4, find the maximum output voltage and maximum output current coming out from the op-amp.*
Solution: *It is readily obtained*

$$\frac{0.5 - v_-}{2K} = \frac{v_{out}}{50K}, \quad v_{out} = -\frac{50K}{2K} v_{in} = 12.5 \sin wtV$$

To find output current

$$i_{out} = i_f + i_L = 0.25mA + \frac{12.5}{10K} = 1.5mA.$$

Note that we must insure that this i_{out} does not exceed the saturation current of the op-amp. Otherwise, the output voltage is clipped.

□

[1] Prove this point by inserting different R_L and calculate its v_o, please.

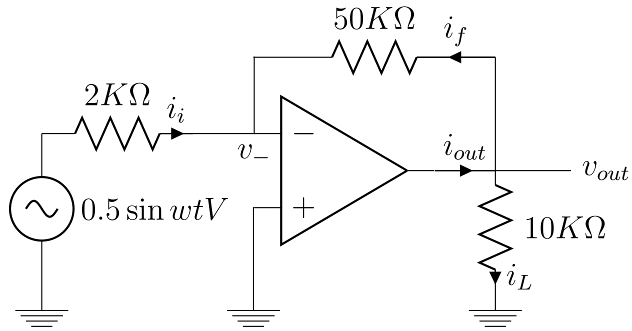


Figure 8.4: Circuit Diagram for Example 8.1

PSpiceLab 8.1 *Re-do Example 8.1 using circuit structures in Figure 8.3 (i.e, ideal op-amp and Voltage-Controlled Voltage Source, respectively) to understand the equivalence relationship.*
Solution: *As shown in the PSpice simulations, the results are consistence with hand computation shown in Example 8.1. This means that it is fair to use VCVS to break the limitations on op-amp usage imposed by the student version.*

□

8.2.2 Summing amplifier

As shown in Figure 8.5 It is readily seen that

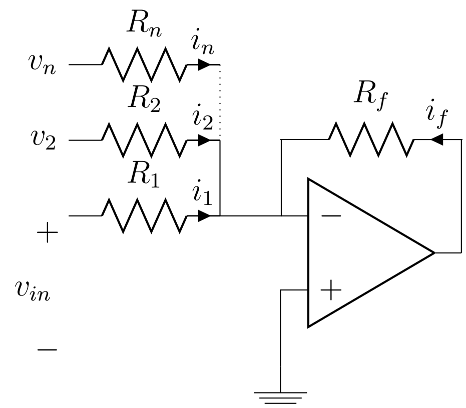


Figure 8.5: A Summing Amplifier

$$v_{out} = -(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n)$$

subsectionNon-inverting amplifier As shown in Figure 8.6

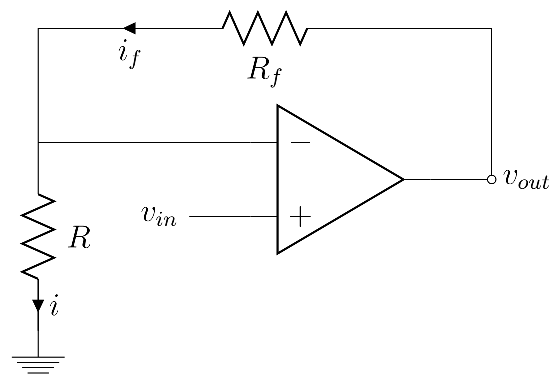


Figure 8.6: A Non-Inverting Amplifier

Applying summing point constraint, we have

$$\frac{v_{out} - v_{in}}{R_f} = \frac{v_{in} - 0}{R}$$

yielding

$$v_{out} = \frac{R + R_f}{R} v_{in}$$

Again, the output voltage is independent of the load resistance, hence an ideal voltage source.

Example 8.2 *Analyze the ideal op-amp circuit shown in Figure 8.7 to find an expression for v_o in terms of v_A and v_B.*

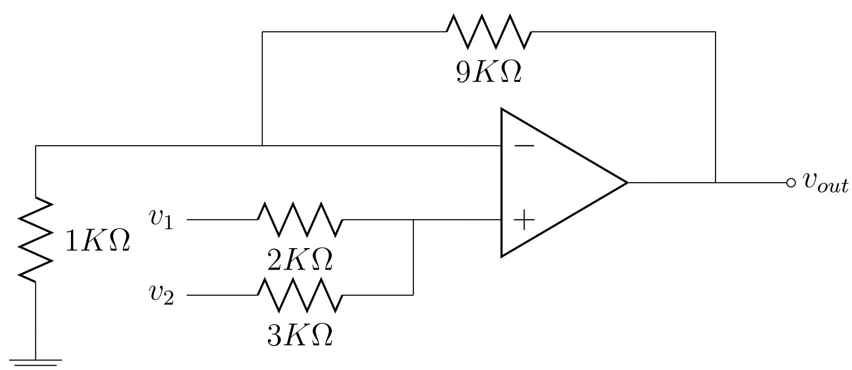


Figure 8.7: Circuit Diagram for Example 8.2

Solution: *Apply superposition for multi-input case. Grounding v_1 to find*

$$v'_+ = \frac{2}{5} v'_2 \textit{ and } \frac{v'_o - v'_+}{9} = \frac{v'_+ - 0}{1}$$

which yields

$$v'_o = 4v_2$$

Likewise, grounding v_2 *to find*

$$v''_+ = \frac{3}{5}v'_2 \ \textit{and}\ \frac{v''_o - v''_+}{9} = \frac{v''_+ - 0}{1}$$

which yields

$$v''_o = 6v_1$$

Thus, $v_{out} = 6v_1 + 4v_2$*. The trick in this example is to use superposition technique for multi-inputs.*

□

8.2.3 Difference amplifier

As shown in Figure 8.8

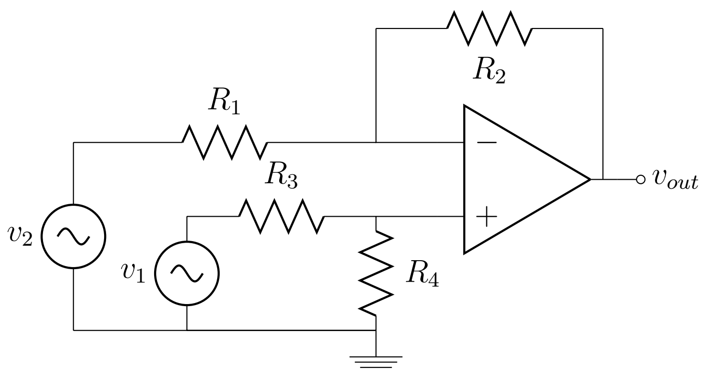


Figure 8.8: A Difference Amplifier

The analysis for difference amplifier is pretty straightforward by observing the fact that this is sum of inverting and non-inverting amplifier. To show this, we have

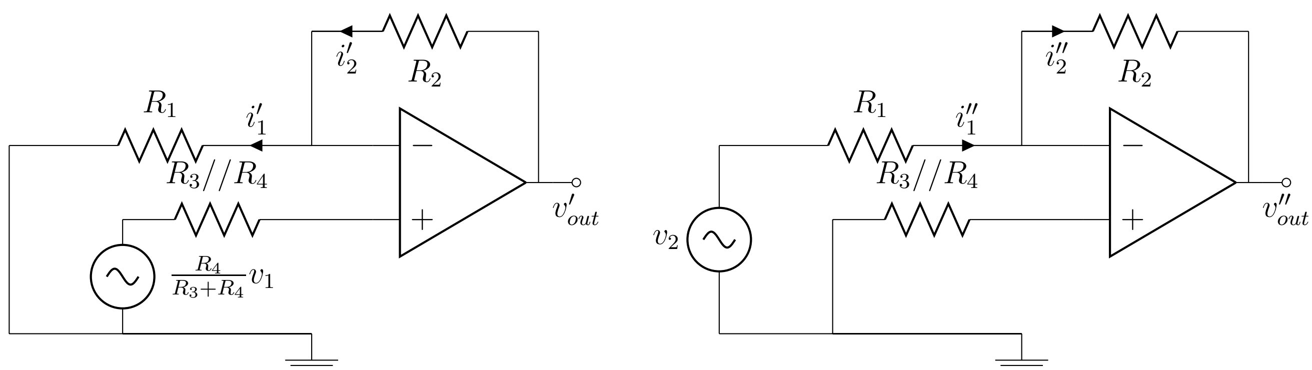


Figure 8.9: (a) Non-inverting and (b) Inverting Amplifier

For the non-inverting amplifier, we have

$$\frac{v'_{out} - \frac{R_4}{R_3+R_4}v_1}{R_2} = \frac{\frac{R_2 R_3}{R_3+R_4}v_1}{R_1}$$

yielding

$$v'_{out} = \frac{R_4}{R_3+R_4}\frac{R_1+R_2}{R_1}v_1$$

For the inverting amplifier, we have

$$\frac{v_2 - 0}{R_1} = \frac{0 - v''_{out}}{R_2}$$

yielding

$$v''_{out} = -\frac{R_2}{R_1}v_2$$

Thus the total output is

$$v_{out} = v'_{out} + v''_{out} = \frac{R_4}{R_3+R_4}\frac{R_1+R_2}{R_1}v_1 - \frac{R_2}{R_1}v_2$$

Example 8.3 (Strain Gauge Circuit) *[2] A strain gauge is a variable resistor that measures the strain (elongation) of a structure when subject to an applied force. To see the reason behind a strain gauge, we have 4 resistors connected to a Wheatstone bridge as shown below. Recall Example 3.26 on page 60 and understand that for the balance condition $v_a = v_b$. If two strain gauges $R + \Delta R$ are placed on the top of a beam and the remaining two strain gauges $R - \Delta R$ are placed on the bottom. If no force is exerted on the beam, the balance condition is reached.*

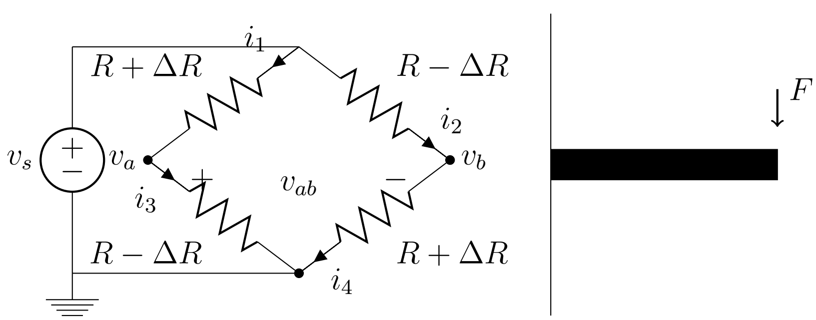


Figure 8.10: (a) Wheatstone Bridge and (b) a Beam

However, if a force is applied to the beam from top, causing deflection, the two $R + \Delta R$ on the top increase their resistance while $R - \Delta R$ decrease resistance.

$$v_a = \frac{R+\Delta R}{2R}, \quad v_b = \frac{R-\Delta R}{2R}$$

The difference voltage is

$$v_a - v_b = \frac{\Delta R}{R} v_s$$

A difference amplifier can be used to amplify the difference signal.

□

8.2.4 Voltage follower amplifier

As explained in Figure 1 on page 12, when a load is attached to a voltage source, the voltage across the load decreases due to internal resistance of the source, known as loading effect. To remove such loading effect, a voltage follower amplifier is inserted as shown in Figure 8.11. The analysis is

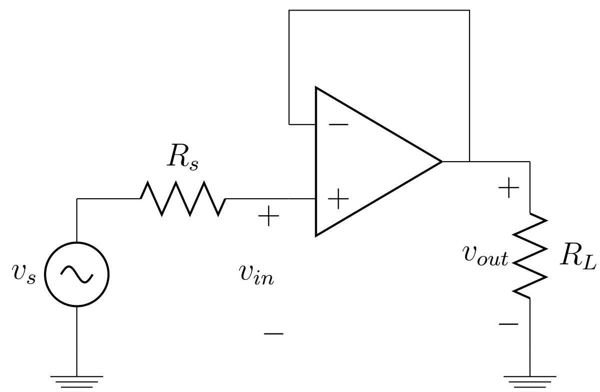


Figure 8.11: Voltage Follower Amplifier

again straightforward. By virtual short circuit constraint, we have $v_+ = v_- = v_{in}$ and the direction feedback connection says that $v_{out} = v_{in}$.

8.2.5 Comparator amplifier

All previously amplifier circuits are assumed to be operated in the linear region. That is, the saturation region is avoided. But for the comparator shown in Figure 8.12a, it is operated in the saturation region, resulting in a positive feedback structure, driving the device to saturation. This is an ideal amplifier without any feedback connection, whose output function is

$$v_{out} = A(v_+ - v_-) = A(v_{in} - V_{ref})$$

If $v_{in} > V_{ref}$, $v_{out} = V_{sat}$; $v_{out} = -V_{sat}$, otherwise. The property is also shown in Figure 8.12b.

8.2.6 Active lowpass Butterworth filter

Given the following Butterworth filter using Sallen-Key topology, we derive the transfer function

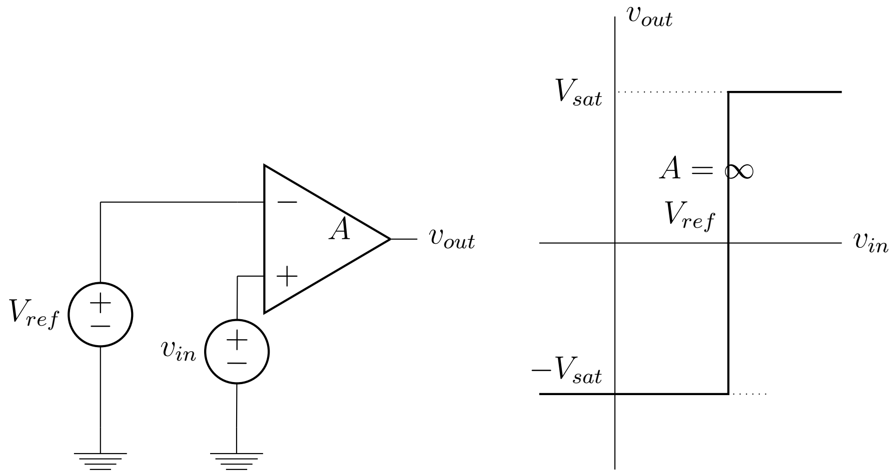


Figure 8.12: (a) Comparator Amplifier and (b) Its Characteristic

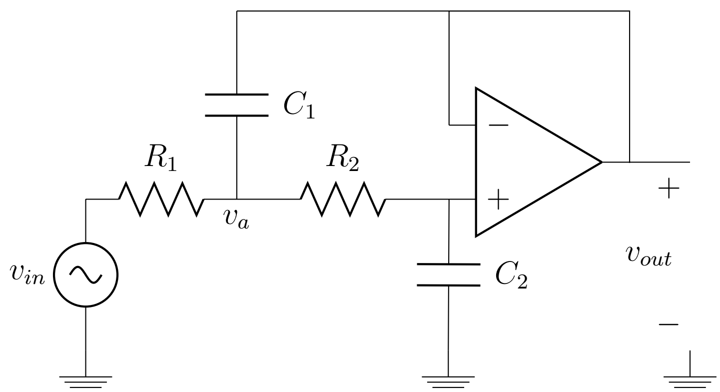


Figure 8.13: Butterworth Amplifier

of the Butterworth filter. Applying summing-point constraint yields

$$C_1 \frac{d(v_{out} - v_a)}{dt} + \frac{v_{in} - v_a}{R_1} = \frac{v_a - v_{out}}{R_2}$$

and

$$\frac{v_a - v_{out}}{R_2} = C_2 \frac{dv_{out}}{dt}$$

To ease the derivation, we take the Laplace transform of the aforementioned two equations and a straightforward substitution generates

$$\begin{aligned} H(s) &= \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_1 R_2 C_1 C_2 s^2 + (R_1 + R_2) C_2 s + 1} \\ &= \frac{w_n^2}{s^2 + 2\xi w_n s + w_n^2} \end{aligned}$$

where $w_n = \frac{1}{R_1 R_2 C_1 C_2}$ and $\xi = \frac{(R_1+R_2)C_2}{2(R_1 R_2 C_1 C_2)}$, which is a second-order low-pass filter. Notice that if cascading two second-order low-pass filer together, we have a fourth-order Butterworth low-pass filter, so on and so forth. To find the frequency response, we obtain (assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$)

$$|H(jw)|_{db} = 20 \log |\frac{1}{(1 - \frac{w^2}{w_{co}^2})^2 + (\frac{2w}{w_{co}})^2}|$$

where $w_{co} = \frac{1}{RC}$.

PSpiceLab 8.2 (Butterworth Low-Pass Filter) *Construct a fourth-order Butterworth filter with $R_1 = R_2 = 15.8K$ and $C_1 = C_2 = 0.1\mu F$ (so that the $f_{co} = 100KHz$) and (1) plot the frequency response for the second-order and fourth-order Butterworth active filter via PSpice UA471.(2) Plot the transient responses using VPULSE with period= 0.1.*

Solution:

PreLab: Review the analytical skill in this subsection.
Lab: Follow the step to see the results.
PostLab: How to construct an n^{th}-order Butterworth filter.[2]

[2]Ans: Cascade $n/2$ circuits together to obtain an n^{th}-order Butterworth filter.

8.3 Recap

In this chapter, we have learned
• For an ideal op-amp, summing-point constraint is instrumental in solving the ideal op-amp problem.
• An Ideal op-amp can be replaced by a voltage-control voltage source. • Although input currents of an ideal op-amp are assumed zero, the output current does exist.
• Be aware that the op-amp output current should be less than the saturation output current.
• Understand the analytical techniques for typical amplifiers.
• Know the differences between positive feedback and negative feedback.

8.4 Problems

Problem 8.1 *Analyze the ideal op-amp circuit shown in Figure 8.14 to find an expression for v_o in terms of v_A and v_B.*

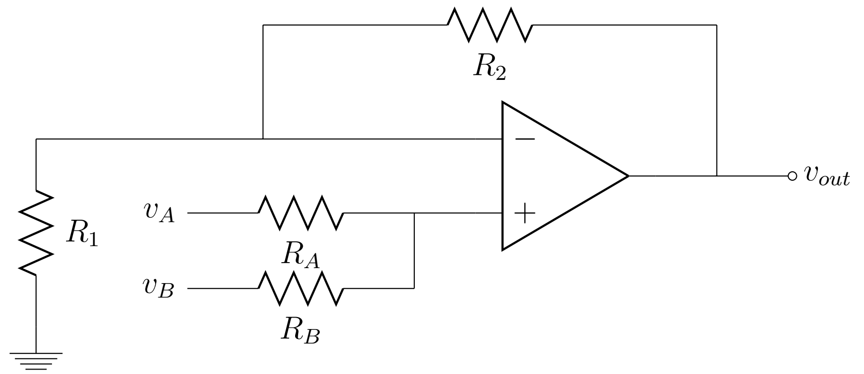


Figure 8.14: Circuit Diagram for Problem 8.1

Answer: $v_{out} = (\frac{R_1+R_2}{R_1})(\frac{v_A R_B + v_B R_A}{R_A+R_B})$.

Problem 8.2 *The circuit shown in Figure 8.15 employs a negative feedback. Derive expression for the voltage gain $A_1 = v_{o1}/v_i$ and $A_2 = v_{o2}/v_i$*

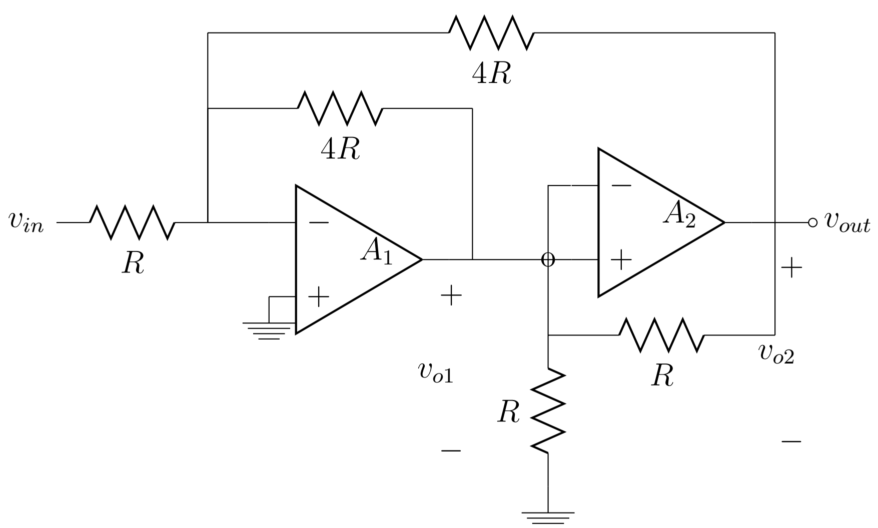


Figure 8.15: Circuit Diagram for Problem 8.2

Answer

Problem 8.3 *For Figure 8.16, derive v_{out} in terms of v_s, R_F and C_s.*

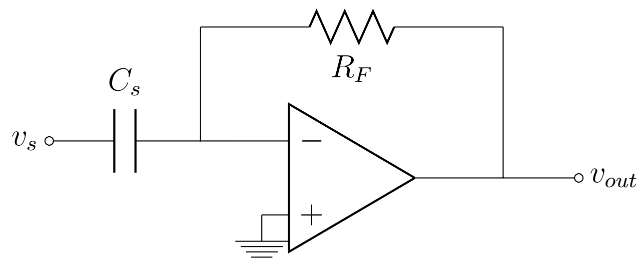


Figure 8.16: Circuit Diagram for Problem 8.3

Answer: $v_{out} = -C_s R_F \frac{dv_s}{dt}$.

Problem 8.4 *For Figure 8.17, derive v_{out} in terms of v_s, R_F and C_s.*

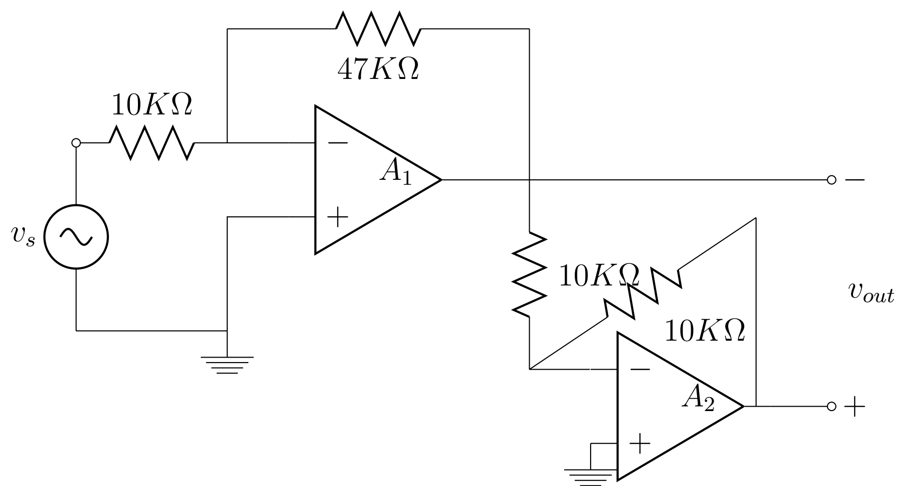


Figure 8.17: Circuit Diagram for Problem 8.4

Answer: $v_2 = 4.7V$ *and* $v_1 = -4.7V$ $v_{out} = v_2 - v_1 = 9.4$.

Problem 8.5 *The operational amplifier in the following circuit, Figure 8.18, is ideal. (b) Calculate* v_{out} *if* $v_a = 1V$ *and* $v_b = 2V$*. (a) Calculate* v_{out} *if* $v_a = 4V$ *and* $v_b = 0V$*. (c) If* $v_b = 1.6V$ *specify the range of* v_a *such that* $-15 < v_{out} < 15$*.*

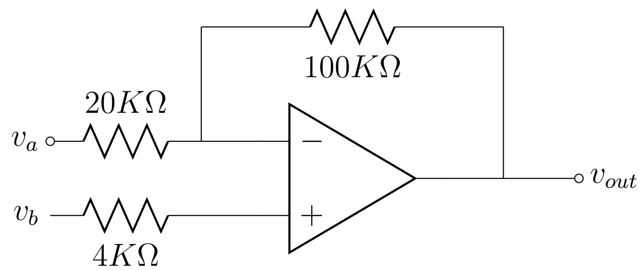


Figure 8.18: Circuit Diagram for Problem 8.5

Answer: *(a)* $v_{out} = -20$*. (b)* $v_{out} = 7$*. (c)* $-1.08 < v_{out} < 4.92$*.*

Problem 8.6 *Determine the output of the differential amplifier shown in 8.19*

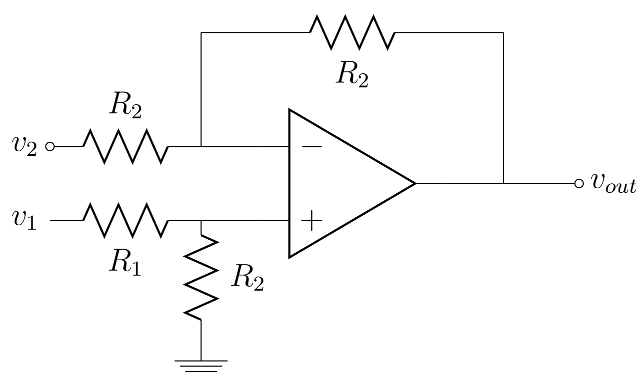


Figure 8.19: Circuit Diagram for Problem 8.6

Answer: $v_{out} = \frac{R_2}{R_1}(v_1 - v_2)$.

Problem 8.7 *The operational amplifier in the following circuit, Figure 8.20, is ideal. (a) Determine v_{out} in terms of V_1. (b) What kind of Op amp it is?*

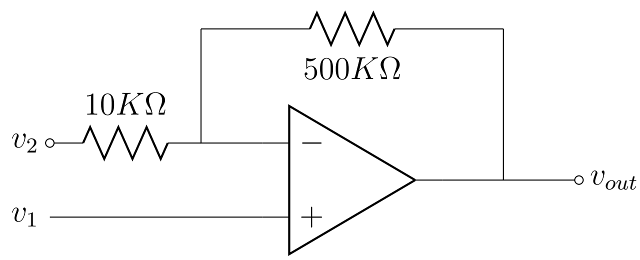


Figure 8.20: Circuit Diagram for Problem 8.7

Answer: *(a)* $v_{out} = 51v_1$. *(b) non-inverting.*

Problem 8.8 *The operational amplifier in the following circuit, Figure 8.21, is ideal. Determine v_{out} in terms of v_1 and v_2.*

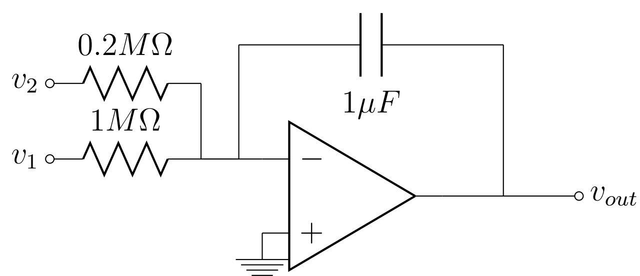


Figure 8.21: Circuit Diagram for Problem 8.8

Answer: *(a)* $v_{out} = -\int(v_1 + 5v_2)dt$.

Problem 8.9 *The operational amplifier in the following circuit, Figure 8.22, is ideal. Determine* v_{out}.

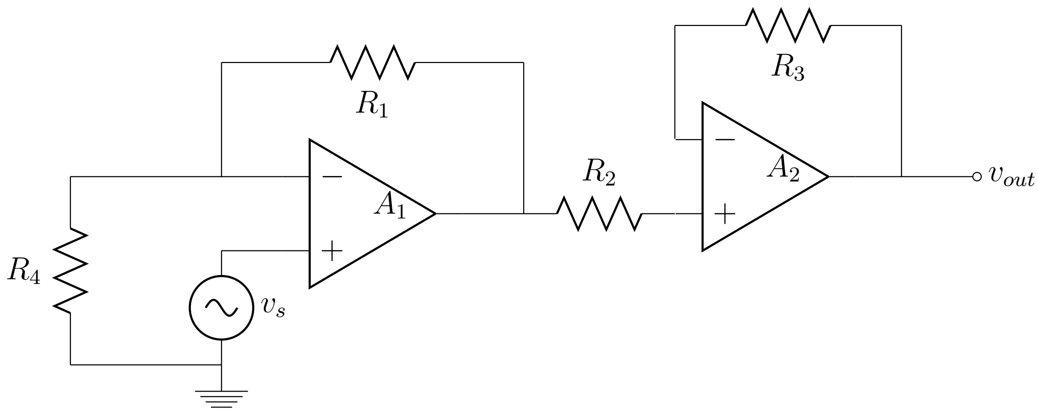


Figure 8.22: Circuit Diagram for Problem 8.9

Answer: $v_{out} = -\frac{R_1R_3+R_3R_4}{R_2R_4}v_s$.

Problem 8.10 *For Figure 8.23 where* $v_1 = 5 + 10^{-3}\sin wt$, *use the principle of superposition to find the ratio of* R_s/R_f *such that no DC voltage appears at the output* v_{out}.

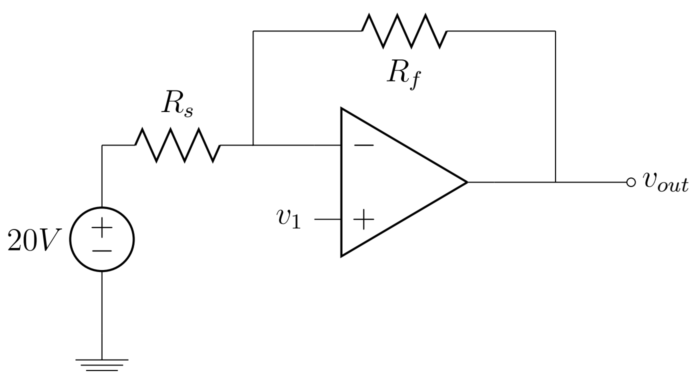


Figure 8.23: Circuit Diagram for Problem 8.10

Answer: $\frac{20-5}{R_s} = \frac{5-0}{R_f}$, *so* $R_s/R_f = 3$.

Problem 8.11 *For Figure 8.24, (a) if $v_1 - v_2 = \cos 1000tV$, find v_{out} at the output, (b) and the phase shift of v_{out}*

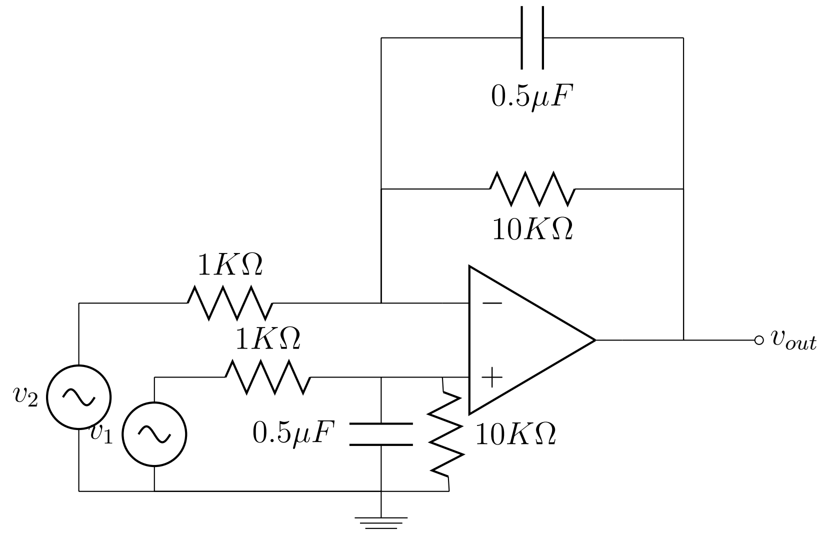


Figure 8.24: Circuit Diagram for Problem 8.11

Answer: *(a) $\bar{V}_{out} = \frac{\bar{Z}}{10^3}(\bar{V}_1 - \bar{V}_2)$, where $\bar{Z} = 10^4/1 + j5$. (b) $-78.7°$.*

Problem 8.12 *For Figure 8.25, (a) find v_{out} at the output, (b) and the current i*

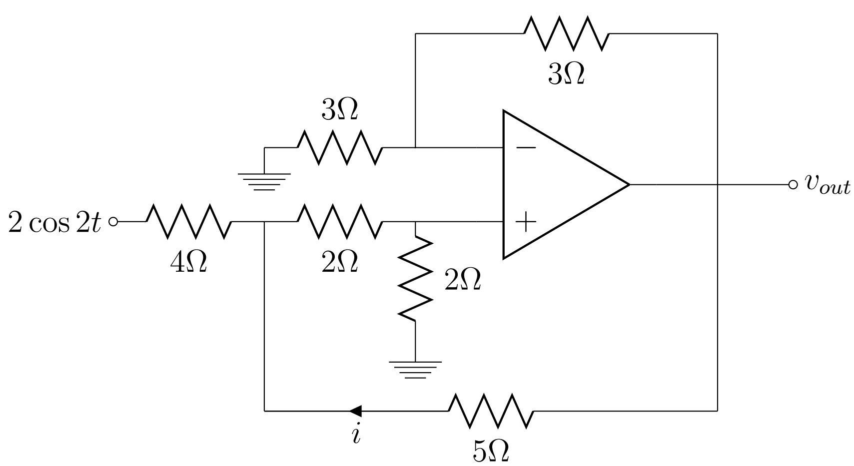


Figure 8.25: Circuit Diagram for Problem 8.12

Answer: *(a) $v = \cos 2tV$, (b) $i = 0$.*

Chapter 9

Bipolar Junction Transistors

The name transistor comes from the phrase "TRANsferring an electrical signal across a reSISTER." The Bipolar Junction Transistor (BJT) is an active device. In simple terms, it is a current controlled valve. The base current (i_B) controls the collector current (i_C). There are two BJTs – *npn* BJT and *pnp* BJT.

9.1 Relationships between Current and Voltage

This is a nonlinear circuit element, we need to understand the $v - i$ characteristic property and linearize it if necessary in order to apply linear circuit theory. We will assume that the collector-base junction is reverse biased ($v_{BC} < 0$) while the base-emitter junction is forward biased ($v_{BE} > 0$).

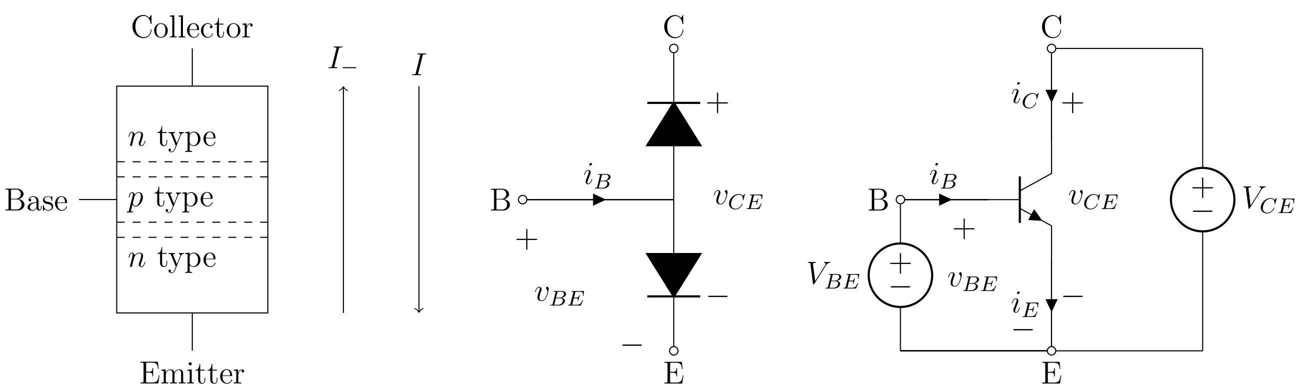


Figure 9.1: (a) An *npn* BJT Transistor (b) Symbol

Since the base-emitter terminal is a *pn* junction, the Schockley equation yields the emitter current i_E in terms of the v_{BE}

$$i_E = I_s(e^{V_{BE}/V_T} - 1) \tag{9.1}$$

where I_s is the saturation current ranging from 10^{-12} to 0^{-16}A, V_T is the thermal voltage about

$0.026mV$ at temperature $300K$. Based on the BJT circuit, we know

$$i_E = i_C + i_B$$

To derive a formula, we define the ratio of collector current to emitter current and to base current, respectively, as

$$\alpha = \frac{i_C}{i_E} < 1, \quad \beta = \frac{i_C}{i_B}$$

where $0.96 < \alpha < 0.997$. Therefore

$$i_E = \alpha i_E + i_B$$

leads to

$$i_B = (1-\alpha)i_E$$

and

$$\frac{i_C}{i_B} = \beta = \frac{\alpha}{1-\alpha} >> 1$$

where $24 < \beta < 330$. A common value is $\beta = 100$. This means collector current is magnified by β when a small i_B current is flowing into base terminal and this i_C constitutes the major current flowing out emitter terminal.

Example 9.1 *A transistor has $\beta = 50$, $I_s = 10^{-14}A$, $v_{CE} = 5V$, and $i_E = 10mA$. Assume $V_T = 0.026V$. Find v_{BE}, v_{BC}, i_B, i_C, and α.*

9.2 Common-Emitter Configuration (CE)

The structure shows a common-emitter circuit where the source between base and emitter supplies a positive voltage v_{BE} over the base-emitter junction, resulting in a forward bias. The voltage across the base and collector junction is determined by

$$v_{BC} = v_B - v_C = v_{BE} - v_{CE}$$

if $v_{CE} > v_{BE}$ then the base-collector is reverse biased. $v_{BC} < 0$.

The output characteristic curve in Figure 9.3 (b) shows that i_C depends on i_B. i.e. For each value of i_B, there exist a corresponding $i_C - v_{CE}$ curve.

PSpiceLab 9.1 (Input and Output Characteristics) *Given Figure 9.4, use the primary and secondary DC dual sweep to verify the input and output characteristics of BJT Q2N3904.*
Solution: *By dual sweep, we mean primary and secondary sweep on I_B and V_{CE} respectively and thus obtain the I/O characteristics.*

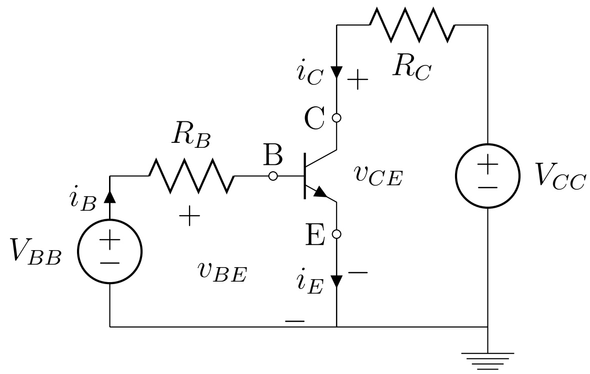


Figure 9.2: A Fixed Base Bias Circuit

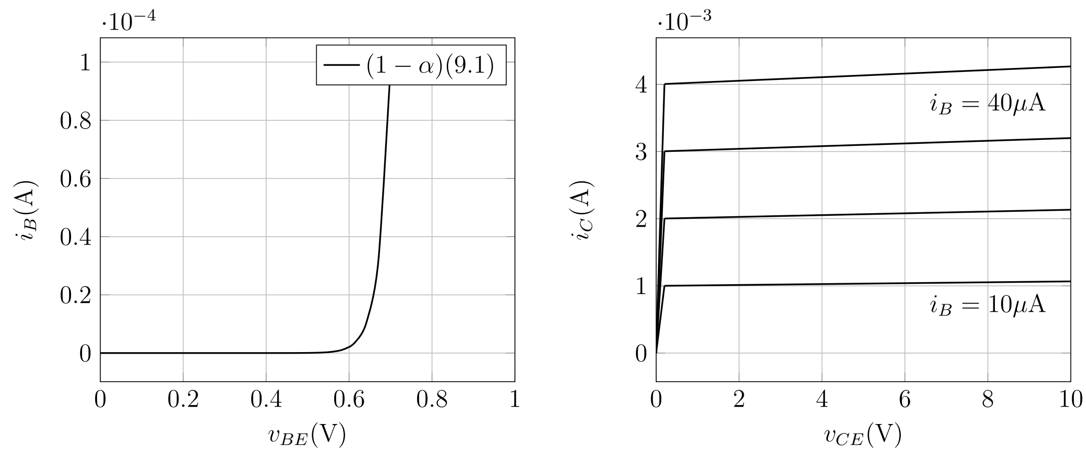


Figure 9.3: CE Characteristics (a) Input $v - i$ Curve (b) Output $v - i$ Curve, $\beta = 100$

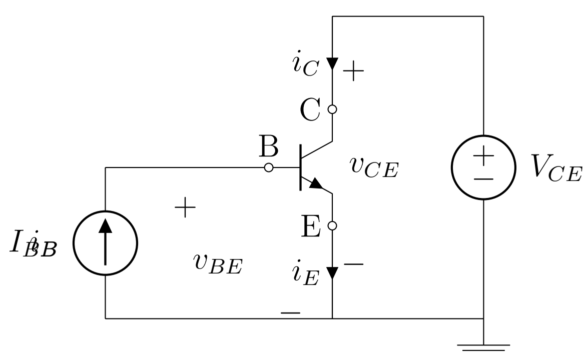


Figure 9.4: A Fixed Base Bias Circuit

9.2.1 Load-Line Analysis

To find an operating point in active region, we need to analyze the input circuit and output circuit respectively and this can be done using Kirchhoff's circuit laws.

$$V_{BB} = I_B R_B + v_{BE}$$

which will intersect the x- and y-axis of the input characteristic curve at

$$x = v_{BE} = V_{BB}, y = i_B = \frac{V_{BB}}{R_B}$$

Similarly, for the output circuit, we have

$$V_{CE} = V_{CC} - I_C R_C$$

$$x = v_{CE} = V_{CC}, y = i_C = \frac{V_{CC}}{R_C}$$

With this information, we have Figure 9.5 shown below.

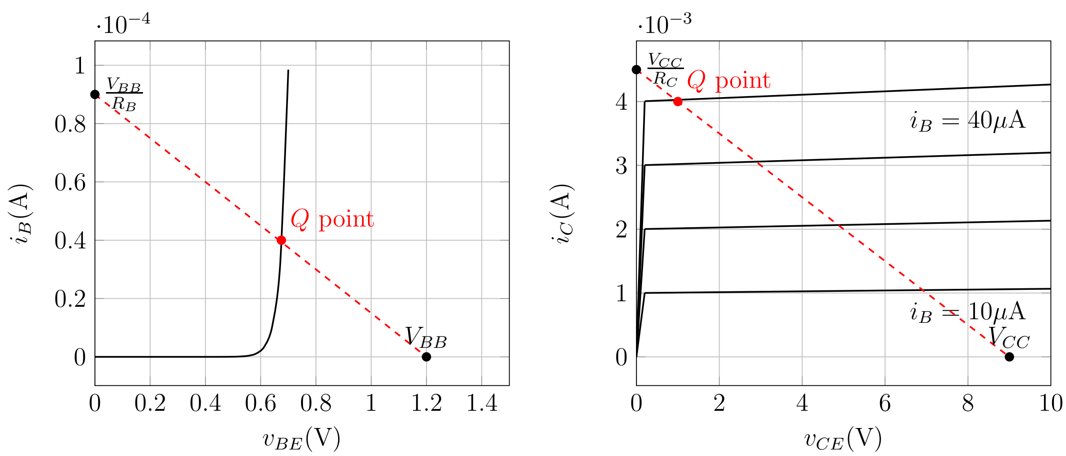


Figure 9.5: CE Load Line (a) Input $v - i$ Curve (b) Output $v - i$ Curve, $\beta = 100$

where the Q point is known as DC operating point. It is emphasized that with different V_{BB} or V_{CC} the load line can vary up and down. By the same token, different R_B or R_C cause the slope of the load line vary too. In sum, the dc power-supply voltages V_{BB} and V_{CC} **bias** the BJT at an operating point for a fixed R_B and R_C.

By appropriate choice of V_B, R_B, R_C, V_{CC}, the desired Q-point may be selected. Once the operating point is established, the BJT can serve as a linear amplifier. To see this, we substitute the dc source V_{BB} in the common emitter circuit of Figure 9.2 with $V_{BB} + v_{in}$. As shown in Figure 9.6, a small variation (say, a tiny triangular signal) at base terminal due to v_{in} will introduce a magnified effect because $i_C = \beta i_B$. This also paves the way that a linearized model at Q-point can be used for a nonlinear BJT element. However, it should be noted that a linearized model is valid in the neighborhood of 40μA. As seen from Figure 9.6, the BJT is driven to saturation region for $i_B = 50\mu$A and 60μA, since the Q-point is below the knee of the output characteristic curve. This observation verifies that for amplification, the Q-point must be in the active region, otherwise, as well as being amplified and inverted,[1] the output waveform is clipped.

In general, we want to establish a Q point near the middle of the load line so the output signal can vary in both directions without clipping.

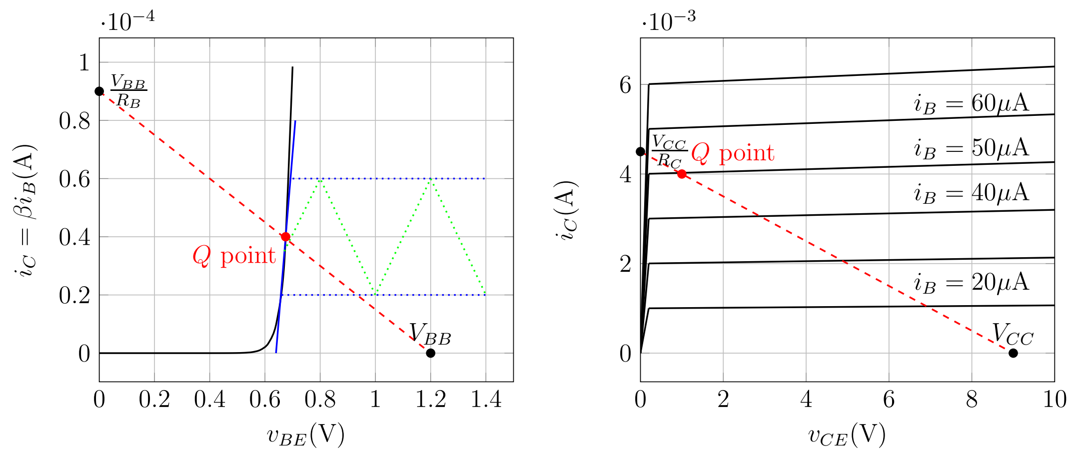


Figure 9.6: Common Emitter BJT as an Amplifier

Example 9.2 *The simplest biasing circuit is base-biased shown in Figure 9.7, (a) determine the Q point by hand and find i_C, V_{CE}, and V_{CB}. Assume $\beta = 165$, and $V_{BE} = 0.72$. (b) Use DC bias point analysis to find Q point and V_{CB}.*

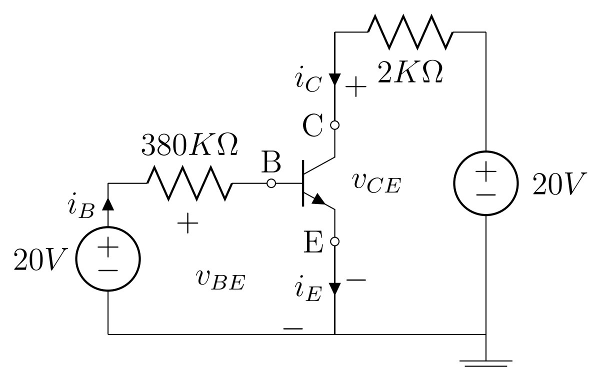


Figure 9.7: A Simple Base-Biased Circuit

Solution: *To find the Q point, we have the following analysis*

$$20 = 380KI_B + v_{BE} = 380KI_B + 0.72$$

[1]Why the signal is inverted? Hint: Q-point is equivalent to $v_{in} = 0$.

which yields $I_B = 50.7\mu A$*, thus* $I_C = 165 I_B = 8.37mA$*. Also*

$$V_{CE} = 20 - I_C 2K = 20 - 8.37m \times 2K = 3.26V$$

and

$$V_{BC} = V_{BE} - V_{CE} = 0.72 - 3.26 = -2.54V$$

The operation is in the active region.

□

9.2.2 Determination of operating regions

As we have seen that a BJT can operate in the active region, in saturation region, or in cutoff region. These circuits are known as BJT bias circuits or DC analysis circuits.

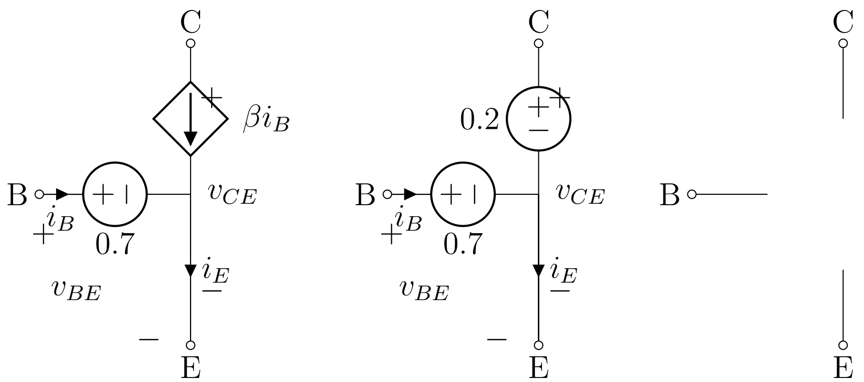


Figure 9.8: Circuit Models for Active, Saturation and Cutoff Regions

• In the active region, the BE junction is forward biased and the BC junction is reversed biased. The transistor is on. The collector current is proportional to and controlled by the base current ($i_C = \beta i_B$) and **relatively insensitive** to v_{CE}. In this region the transistor can be an amplifier.

• In the saturation region, both junctions are forward biased: $i_B >> 0$, $I_C < \beta i_B$.
The transistor is on. The collector current varies very little with a change in the base current in the saturation region. The v_{CE} is small, a few tenths of volt. The collector current is **strongly dependent** on v_{CE} unlike in the active region. It is desirable to operate transistor switches in or near the saturation region when in their on state.

• In the cutoff region, both junctions are reversed biased: $i_C = 0$.
The transistor is off. There is no conduction between the collector and the emitter. ($i_B = 0$ therefore $I_C = 0$)

The analysis above is known as large-signal model analysis (Switch)

• Cutoff region; BE terminal is reversed-biased, $I_B = 0, I_C = 0$
• Active region; BE terminal is forward-biased, $I_B > 0, I_C = \beta I_B$
• Saturation region; BE terminal is forward-biased, $I_B >> 0, I_C < \beta I_B$

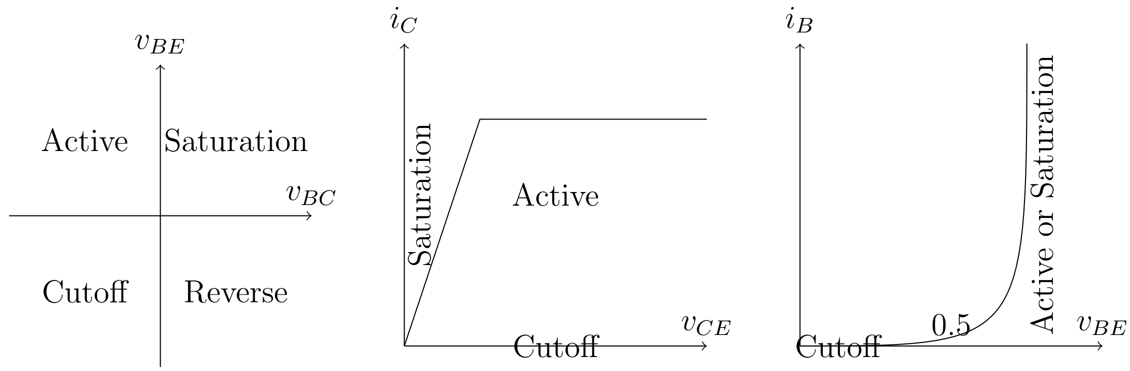


Figure 9.9: Operating Regions Based on Input/Output Characteristic

Practical BJT self-bias circuit

For a fixed base bias circuit (see Figure 9.2) the base current I_B is fixed to $\frac{V_{CC}}{R_B}$ and does not change for different values of β. The load line analysis shows that for different Q point (meaning different β values), the I_B must change. To design a circuit that is independent of β. Thus, we have the

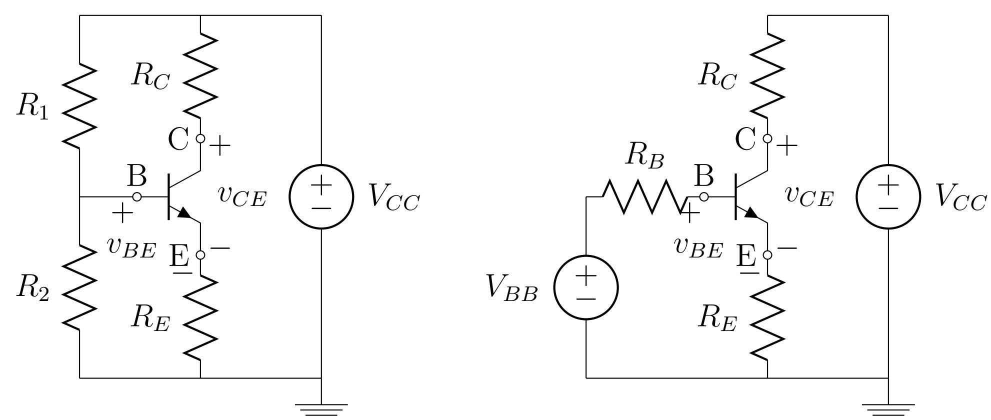


Figure 9.10: 4 Resistors BJT Bias Circuit

following equivalent circuit for DC analysis to determine Q point and relevant electrical quantities.
To analyze the four-resistor bias circuit, we use Thevenin theorem to find the equivalent voltage seen from the BE terminals

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and the equivalent resistance is

$$R_B = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Around the base-emitter circuit, BE loop

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

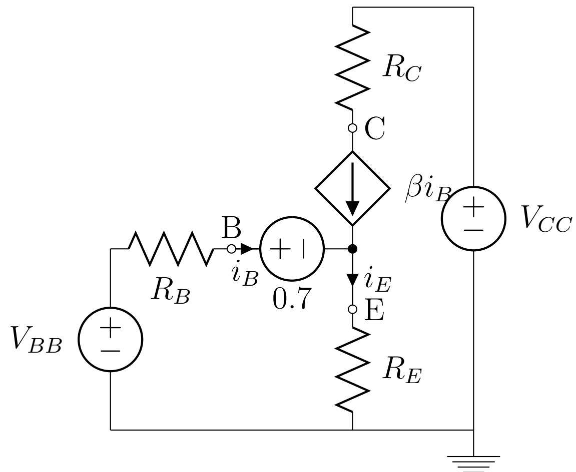


Figure 9.11: Equivalent DC circuit

$$\begin{aligned} &= [R_B + (\beta+1)R_E]I_B + V_{BE} \\ I_E &= I_C + I_B = \beta I_B + I_B \end{aligned}$$

Around the collector-emitter circuit, CE loop

$$\begin{aligned} V_{CC} &= I_C R_C + V_{CE} + I_E R_E \\ &= I_C[R_C + \frac{\beta+1}{\beta}R_E] + V_{CE} \\ I_E &= I_C + I_B = I_C + \frac{1}{\beta}I_C \end{aligned}$$

Solving, these two equations yield

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta+1)R_E}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C(R_C + \frac{\beta+1}{\beta}R_E) \\ &= V_{CC} - I_C(R_C + \frac{\beta+1}{\beta}R_E) \\ &\approx V_{CC} - I_C R_C - I_E R_E \end{aligned}$$

Example 9.3 *The most popular biasing is the voltage-divider biasing shown in Figure 9.10, (a) determine the Q point by hand and find* I_C, V_{CE} *and* V_{CB}. *Assume* $\beta = 165$, *and* $V_{BE} = 0.68$. *(b) Use DC bias point analysis to find Q point and* V_{CB}.

Solution: *First, the Thevenin equivalent seen from the* v_{BE} *terminals is* $V_{oc} = 4V$ *and* $R_t = 40K$. *To find the Q point, we have the following analysis*

$$4 = 40KI_B + v_{BE} + I_E R_E = (40K + 166 \times 1.5K)I_B + 0.68$$

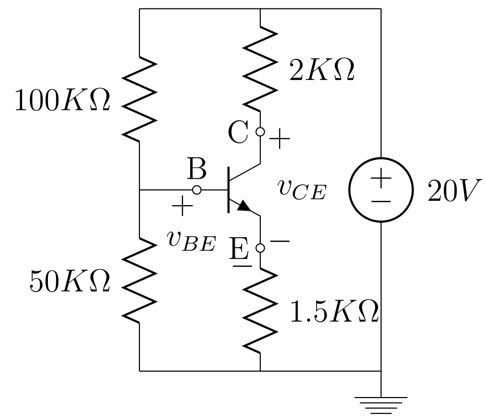


Figure 9.12: A Self-bias Circuit

which yields $I_B = 11.48\mu A$, *thus* $I_C = 165 I_B = 1.89mA$. *Also*

$$V_{CE} = 20 - I_C(2K + \frac{166}{165}1.5K) = 20 - 6.63 = 13.37V$$

and

$$V_{BC} = V_{BE} - V_{CE} = 0.68 - 13.37 = -12.69V$$

□

Example 9.4 (Independent of β) *Given the four resistors circuit, Figure 9.10, where* $R_1 = 10k\Omega$, $R_2 = 5K\Omega$, $R_C = 1K\Omega$, $R_E = 5K\Omega$, *and* $V_{CC} = 15V$, *find the values of* I_C *and* I_{CE} *for* $\beta = 100$ *and* $\beta = 300$.

Solution: *The Thevenin equivalent seen from terminal BE is determined to be* $V_{BB} = 5V$ *and* $R_B = 3.33K\Omega$. *Once this is found, the remaining relevant quantities are determined based on the formulae derived and they are listed in the Table below:*

β	I_B	I_C	I_E	V_{CE}
100	41.2μ A	4.12mA	4.16mA	6.72V
300	14.1μ A	4.24mA	4.25mA	6.51V

Table 9.1: Comparison Study for Different β

The example shows the advantage of a self-bias BJT circuit which can have a Q point that is almost independent of β.

□

Once the bias DC analysis technique is mastered, we can choose one of the BJT operating region and use the circuit model introduced in Figure 9.9 to analyze the circuit and determine I_C, I_B, V_{BE} and V_{CE}. Lastly, check whether the obtained electrical quantities comply with the region chosen. If yes, the analysis is completed. If not, redo the procedure.

9.3 Small-Signal Circuit Models

Note that the small-signal model assumes that the Q point (DC-bias point) of the transistor has been established and a linearized model due to biasing is found. To embark an analysis leading to a small-signal model, we use notation below, assuming a signal can be represented as a small AC excitation superimposed on the dc quantities

$$\begin{aligned}
v_{BE} &= V_{BEQ} + v_{be} \\
v_{CE} &= V_{CEQ} + v_{ce} \\
i_C &= I_{CQ} + i_c = I_{CQ} + g_m v_{be} \\
i_B &= I_{BQ} + i_b = I_{BQ} + \frac{v_{be}}{r_\pi} \\
i_E &= I_{EQ} + i_e = I_{EQ} + \frac{v_{be}}{r_e} \\
v_C &= V_{CQ} + v_c
\end{aligned}$$

where at a Q point the following identities hold

$$\begin{aligned}
V_{CQ} &= V_{CEQ} = V_{CC} - I_{CQ} R_C \\
I_{CQ} &= I_S e^{\frac{V_{BEQ}}{V_T}} \\
I_{EQ} &= \frac{i_{CQ}}{\alpha} = \frac{I_S}{\alpha} e^{\frac{V_{BEQ}}{V_T}} \\
I_{BQ} &= \frac{i_{CQ}}{\beta} = \frac{I_S}{\beta} e^{\frac{V_{BEQ}}{V_T}}
\end{aligned}$$

To operate as an amplifier, a transistor must be biased in the active region to establish a constant dc current in the emitter (or collector) and therefore, a linearized model due to biasing can be found.

• The transconductance

$$g_m = \frac{\partial i_C}{\partial v_{BE}}|_{v_{BE}=V_{BEQ}} = \frac{1}{V_T}(I_S e^{\frac{v_{BE}}{V_T}})|_{v_{BE}=V_{BEQ}} = \frac{I_{CQ}}{V_T}$$

• The base resistance

$$\frac{1}{r_\pi} = \frac{\partial i_B}{\partial v_{BE}}|_{v_{BE}=V_{BEQ}} = \frac{1}{\beta V_T}(I_S e^{\frac{v_{BE}}{V_T}})|_{v_{BE}=V_{BEQ}} = \frac{g_m}{\beta} = \frac{I_{CQ}}{\beta V_T} = \frac{I_{BQ}}{V_T}$$

• The emitter resistance

$$\frac{1}{r_e} = \frac{\partial i_E}{\partial v_{BE}}|_{v_{BE}=V_{BEQ}} = \frac{1}{\alpha V_T}(I_S e^{\frac{v_{BE}}{V_T}})|_{v_{BE}=V_{BEQ}} = \frac{g_m}{\alpha} = \frac{I_{EQ}}{V_T} \approx \frac{I_{CQ}}{V_T} = g_m$$

The linearization analysis shows that both DC and AC components exist, establishing the small-signal model after a DC bias circuit analysis is done. With that, we have

$$v_{be} = r_\pi i_b = r_e i_e, \quad r_\pi = (\frac{i_e}{i_b}) r_e = (\beta + 1) r_e$$

and

$$i_e = i_b + i_c = \underbrace{\frac{v_{be}}{r_\pi} + g_m v_{be}}_{VCCS} = \underbrace{\frac{v_{be}}{r_\pi}(1+\beta)}_{CCCS} = \frac{v_{be}}{\frac{r_\pi}{1+\beta}} = \frac{v_{be}}{r_e} \tag{9.2}$$

The equation (9.2) suggests two most widely used model for the BJT (small-signal circuit model) which are shown in Figure 9.3. Furthermore, to account for the early effect, the dependence of i_c on v_{CE}, a finite output resistance $r_o = \frac{V_A}{I_C}$ can be assigned in parallel to the controlled-current source.

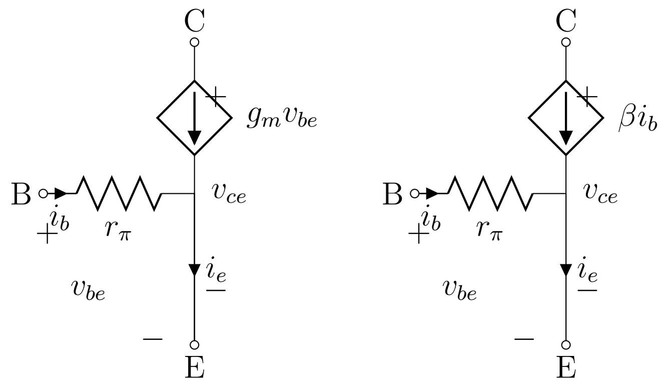


Figure 9.13: Voltage-Controlled and Current-Controlled Current Source

Once the small-signal models, Figure 9.3, are established, we, in what follows, will investigate the small-signal circuit for the most commonly seen amplifiers based on BJT.

9.3.1 Basic BJT Amplifier Configuration (CE, CB, CC)

All three configurations will be desired from a universal amplifier configuration in which capacitors C_1, C_2 and C_3 are assumed very large (ideally ∞), that is, acting as a perfect short circuit ($Z = 1/jwC = 0$) at signal frequency, but capacitors block dc ($Z = 1/j0C = \infty$), providing separate paths for DC and AC current. Such connections do not affect biasing of BJT. In particular, the capacitor C_2 is also known as a bypass capacitor since it provides a short-circuit path for i_E to ground.

For an AC analysis, in order to let the capacitor become short circuit, we need to choose

$$|\frac{1}{jwC_2}| << R_E$$

leading to

$$\frac{1}{wC_2} << R_E$$

The following example demonstrates the fact that when a coupling/bypassing capacitor is incorporated into a circuit with AC and DC sources, an independent effect (no mutual interaction) is introduced into the circuit analysis.

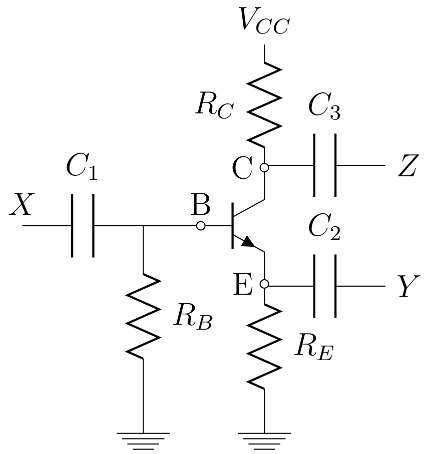


Figure 9.14: Universal Amplifier Configuration

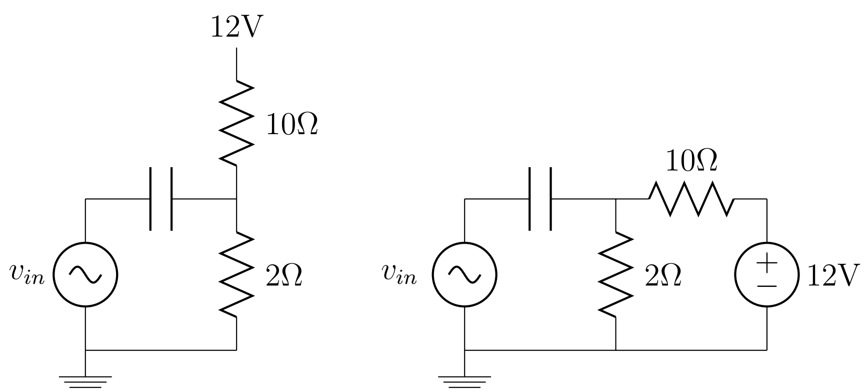


Figure 9.15: Problem 9.5

Example 9.5 (Bypassing Capacitor) *Given Figure shown below, find the voltage across* 2Ω*.*
Solution: *Since an equivalent circuit is shown, we can applied superposition technique to solve it. For AC analysis, we have* $v_1 = v_1'$*. For the DC analysis, the capacitor becomes an open circuit and the voltage across* 2Ω *is* $v_1'' = 2V$*. The total voltage across* 2Ω *is than* $v_1 = v_1' + 2V$*. The example*

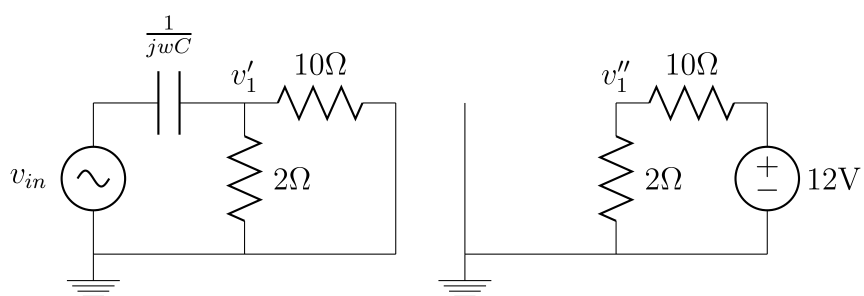


Figure 9.16: Small Signal Circuit and Bias Circuit

shows that bias DC source and small signal AC source using bypassing capacitor enable the circuit to be treated independently as two sources in a linear system that superposition is applied. This means the DC source is used to find Q point and AC source is used to find small signal magnification.

□

Common-Emitter Amplifier (CE)

Consider the following actual circuit for a common-emitter amplifier. Based on the small-signal just

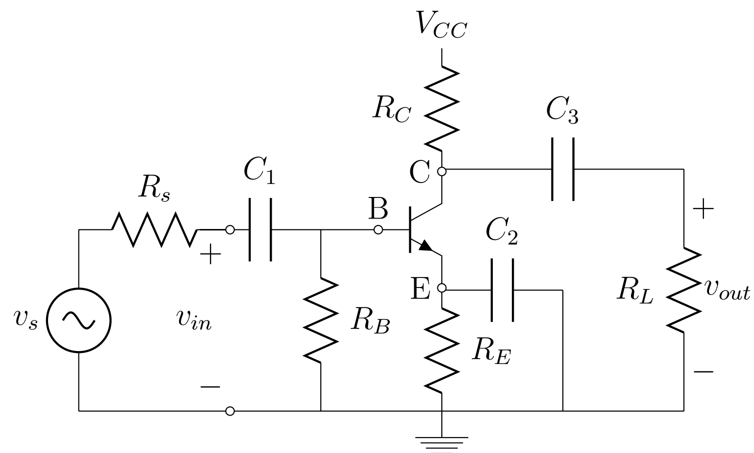


Figure 9.17: Common Emitter Configuration

obtained, Figure 9.17 is equivalent to the following small-signal AC circuit and the circuit analysis techniques can be applied.

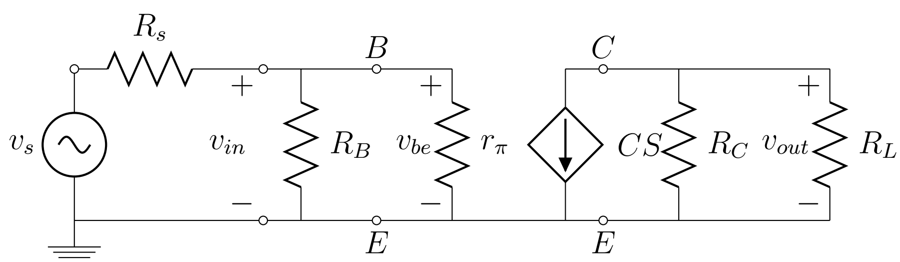


Figure 9.18: Equivalent Small Signal AC Circuit

where the controlled current $CS = g_m v_{be}$ or βi_b.

• Voltage gain

$$A_v = \frac{v_{out}}{v_{in}} = \frac{0 - g_m v_{be} R_L'}{v_{be}} = -g_m R_L' = -\frac{\beta}{r_\pi} R_L' \tag{9.3}$$

where $R_L' = R_L // R_C$ and the minus sign means a phase reversed. Had the circuit contained ideal dc current source, these would have been replaced by a short circuit.

- Open-circuit voltage gain

$$A_{vo} = \frac{v_{out}}{v_{in}}|_{R_L=\infty} = \frac{-g_m v_{be} R_C}{v_{be}} = -g_m R_C = -\frac{\beta}{r_\pi} R_C \tag{9.4}$$

- Input impedance seen looking into the input terminals

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{be}}{i_{in}} = R_B // r_\pi = \frac{1}{1/R_B + 1/r_\pi} \tag{9.5}$$

- Current Gain

$$A_i = \frac{i_{out}}{i_{in}} = \frac{\frac{v_{out}}{R_L}}{\frac{v_{in}}{Z_{in}}} = A_v \frac{Z_{in}}{R_L} \tag{9.6}$$

- Output impedance seen looking back from the output terminals with source zeroed

$$Z_{out} = R_C \tag{9.7}$$

This is because $i_b = 0$ and $v_{be} = 0$ due to source is shorted. Therefore, the voltage-controlled current source is open.

- Power gain

$$A_p = A_v A_i$$

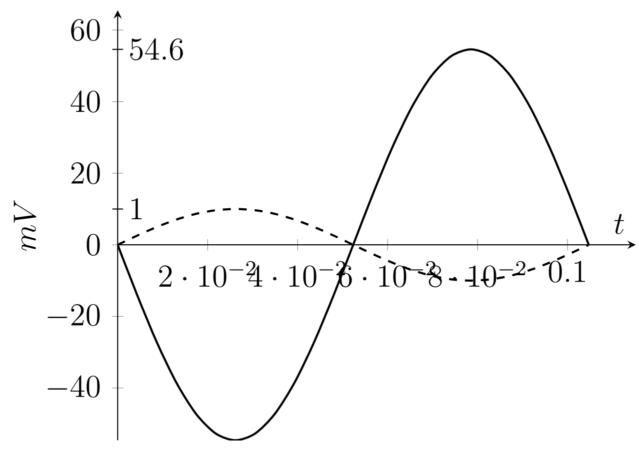


Figure 9.19: Inverted and Magnified AC Signal

Example 9.6

□

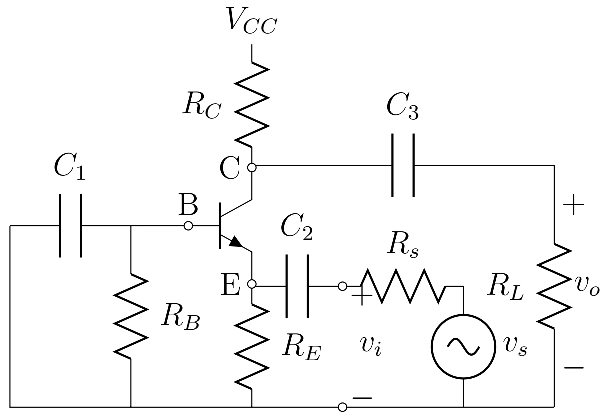


Figure 9.20: Common Base Configuration

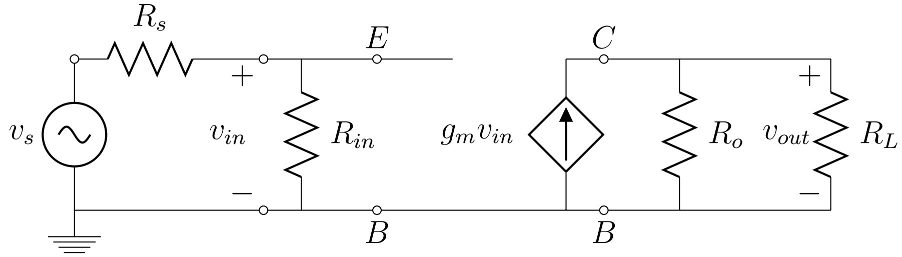


Figure 9.21: Equivalent Small Signal AC Circuit for CB Configuration

Common-Base Amplifier(CB)

where $R_{in} = R_E//r_e$ and $R_o = R_C//R_L$. Thus, the open-circuit voltage gain

$$A_{vo} = \frac{v_o}{v_i}|_{R_L=\infty} = \frac{g_m v_i R_o}{v_i} = g_m(R_C//r_o)$$

the short-circuit current gain

$$A_{is} = \frac{i_o}{i_i}|_{R_L=0} = \frac{g_m v_i}{\frac{v_i}{R_i}} = g_m R_i = g_m(R_E//r_e) = g_m r_e = \alpha < 1$$

the overall voltage gain

$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = [g_m(R_o//R_L)]\frac{R_i}{R_i + R_S} = (\frac{r_e}{r_e + R_S})g_m(R_C//r_o//R_L)$$

Common-Collector Amplifier(CC)

DC Analysis to determine Q point, AC analysis to compute amplification
(Capacitors become open) (Capacitors become shorted)

$$R_B = R_1//R_2$$

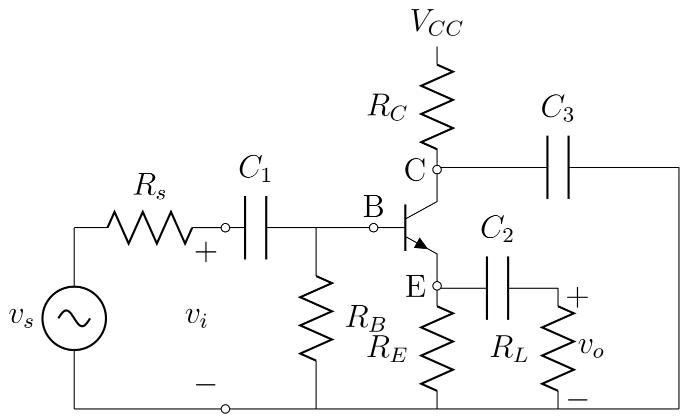


Figure 9.22: Common Collector Configuration

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC}$$

Around BE loop

$$V_{BB} = I_B R_B + V_{BE} + I_C R_E$$

Around CE loop

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

in these equations

$$I_E = I_B + I_C = (\beta + 1) I_B = (\frac{\beta + 1}{\beta}) I_C$$

$$\begin{aligned} i_{in} &= \frac{v_{in}}{R_B // h_{ie}} = \frac{v_s}{R_S + (R_1 // R_2 // h_{ie})} \\ \Delta &= \frac{v_{in}}{h_{ie}} \end{aligned}$$

$$r_i = R_1 // R_2 // h_{ie}$$

v_{oc} at the output terminal is

$$v_{oc} = -h_{fe} \Delta I_B R_C = -h_{fe} \frac{v_{in}}{h_{ie}} R_C$$

i_{sc} at the output terminal is

$$\begin{aligned} i_{sc} &= -h_{fe} \Delta I_B = -h_{fe} \frac{v_{in}}{h_{ie}} \\ r_o &= \frac{v_{oc}}{i_{sc}} = R_C \\ \mu &= \frac{v_{oc}}{v_{in}} = -\frac{h_{fe}}{h_{ie}} R_C \end{aligned}$$

9.4 *pnp* Bipolar Junction Transistors

Having investigated *npn* BJT, we turn our attention to *pnp* BJT where the base is constructed with n-type material that is situated between p-type material.

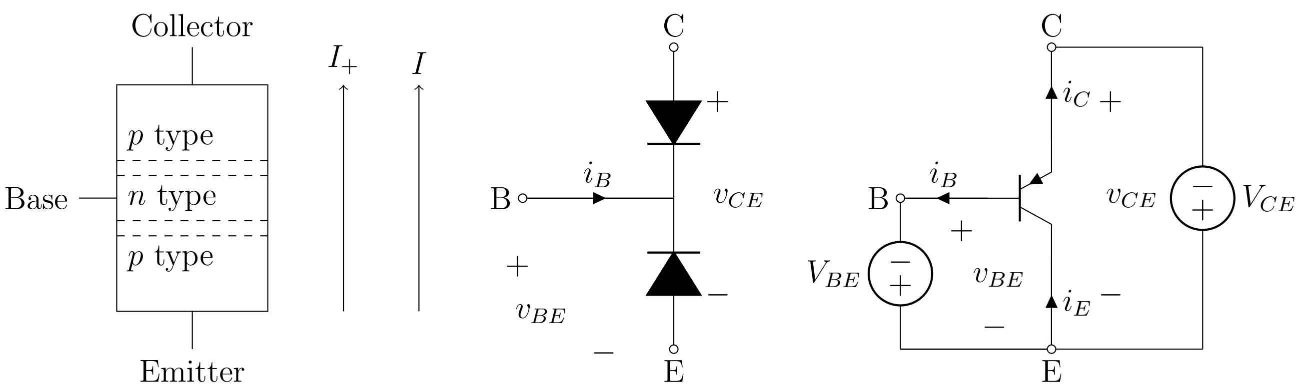


Figure 9.23: (a) A *pnp* BJT Transistor (b) Symbol

Compare Figure 9.23(b) with Figure 9.1(b), it is readily seen that except for the voltage polarity and current direction being reversed, the *pnp* BJT is almost identical to the *npn* BJT.

9.5 Recap

After this chapter, the following knowledge is gained

- BJT is a nonlinear circuit element, requiring input and output characteristic curves.
- Load line analysis is crucial for a DC operating point.
- If there is a R_E in the emitter branch, the computation is more involved.
- Must be aware what operating region the element is in and the corresponding circuit models.
- BJT is a current-controlled current source.

9.6 Problems

Problem 9.1 *For the elementary amplifier circuit in Figure 9.24, the collector-battery voltage* $V_{CC} = 10V$. *The quiescent point Q is at* $i_B = I_B = 0.1mA$ *and* $v_{CE} = V_{CE} = 5V$. $\beta = 40$. *(a) Find the collect current* I_C. *(b) Specify* R_L. *(c) Predict the current gain* A_i. *(d) The output voltage* v_{R_L} *for an input current* $i_B = 0.05 \sin t mA$.

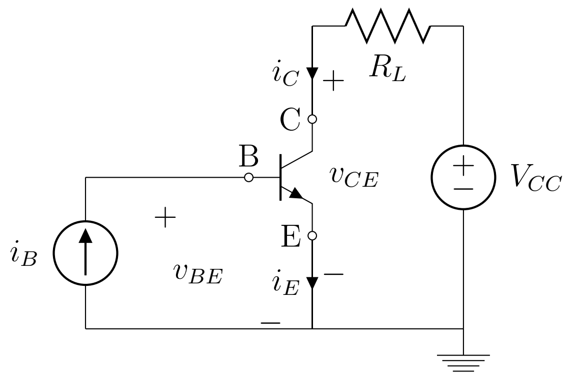


Figure 9.24: Circuit Diagram for Problem 9.1

Answer: *(a)* $I_C = \beta I_B = 0.004A$. *(b)* $R_L = 1250\Omega$. *(c)* $A_i = \beta = 40$. *(d)* $v_L = i_C R_L = \beta i_B R_L = 2.5 \sin wt$.

Problem 9.2 *For the circuit shown in Figure 9.25, determine the base voltage* V_{BB} *required to saturate the transistor. Assume* $V_{CEsat} = 0.1V$, $V_{BEsat} = 0.6V$ *and* $\beta = 50$

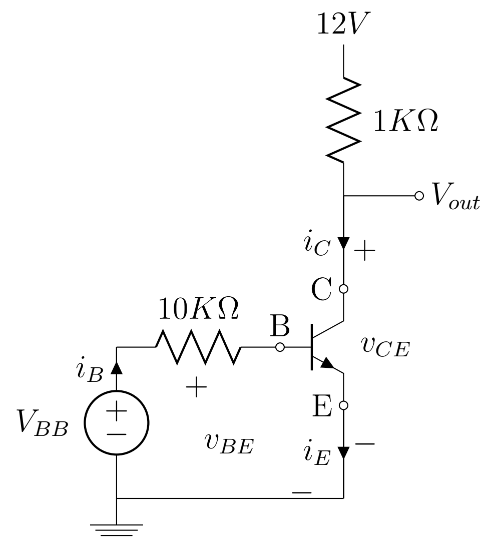


Figure 9.25: Circuit Diagram for Problem 9.2

Answer: $V_{BB} = 2.98V$.

Problem 9.3 *For the circuits of Fig. 3, $b = 85$, $R_C = 2K$, answer the following question: (a) when $R_B = 200K\Omega$ and $R_E = 0$, what mode is the BJT in? (b) when $R_B = 0$ and $R_E = 2K\Omega$, what mode is the BJT in? (c) when $R_B = 200K\Omega$ and $R_E = 2K\Omega$, find V_B, V_C, what mode is the BJT in?*

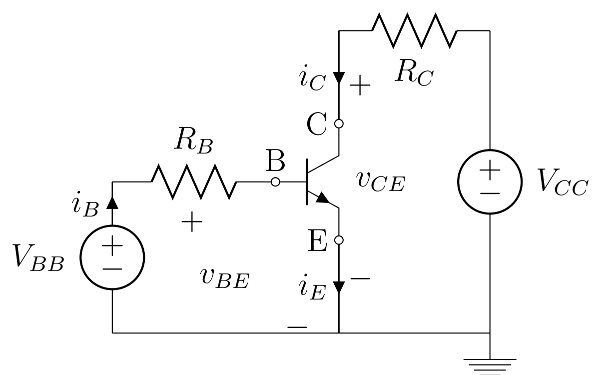


Figure 9.26: Circuit Diagram for Problem 9.3

Problem 9.4 *For the circuit in Figure 9.27 where $V_{CC} = 20V$, $R_C = 5K\Omega$, and $R_E = 1K\Omega$, determine the region of operation of the transistor if (a) $I_C = 1mA$, $I_B = 20\mu A$, $V_{BE} = 0.7V$. (b) $I_C = 3mA$, $I_B = 1.5\mu A$, $V_{BE} = 0.85V$.*

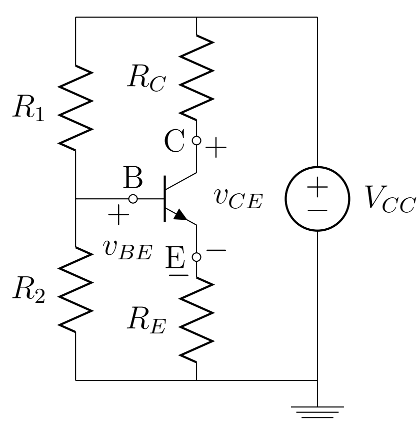


Figure 9.27: Circuit Diagram for Problem 9.4

Answer: *(a) $V_{CE} = 13.98V$. $V_{CB} = 13.28V$ Active region for CB junction is reverse-biased. (b) $V_C = 5V$, $V_{CE} = 0.5V$ and $V_{CB} = -0.35V$. Saturation region for CB junction is forward-biasd.*

Problem 9.5 *For the circuits shown in Figure 9.28 where $\beta = 100$ and $V_{BE} = 0.6V$, find (a) the Q point. (b) The maximum voltage gain.*
Answer: $I_B = 0.0218mA$. $I_C = 2.18mA$. $V_{CE} = 5.24V$. $A_v = -30/11$.

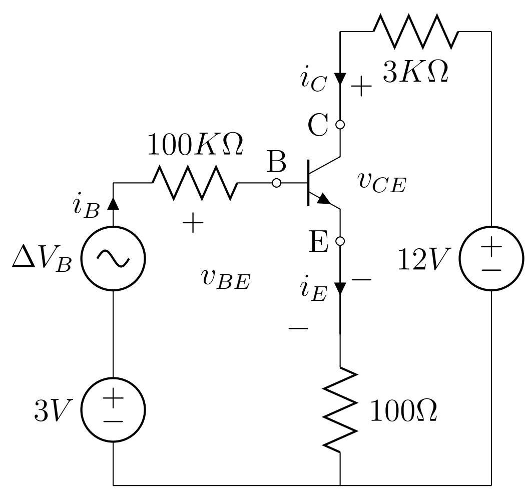


Figure 9.28: Circuit Diagram for Problem 9.5

Chapter 10

Unipolar Transistors

Unipolar means only a single type of charge carrier is necessary for device operation. Unipolar transistors are also known as Field-Effect Transistors (FETs). They are two types of FETs: Junction Field-Effect Transistor (JFET) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). Since only one type of charge carrier is needed for the device to work, all types of FETs are sub-categoried as

- n-type JFET and p-type JFET
- n-enhanced MOSFET and p-enhanced MOSFET.

10.1 Junction Field-Effect Transistor

A n-channel JFET is shown in Figure 10.1.

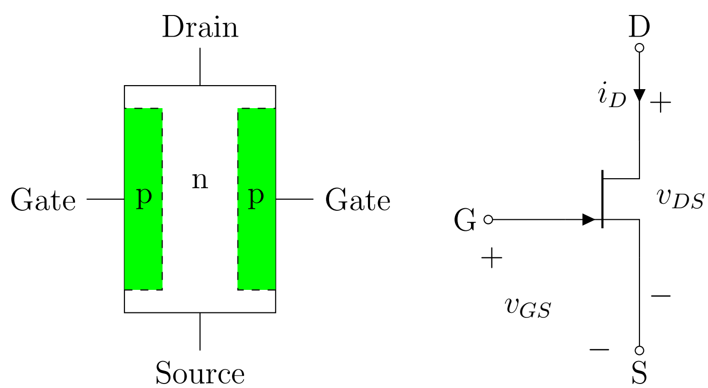


Figure 10.1: (a) A n-Channel JFET Transistor (b) Symbol

In almost all applications, the pn junction is always reverse biased, meaning the potential voltage at gate terminal is more negative than the source terminal (i.e., $v_{GS} < 0$) and resulting in the current flowing into the gate is zero ($i_G = 0$).

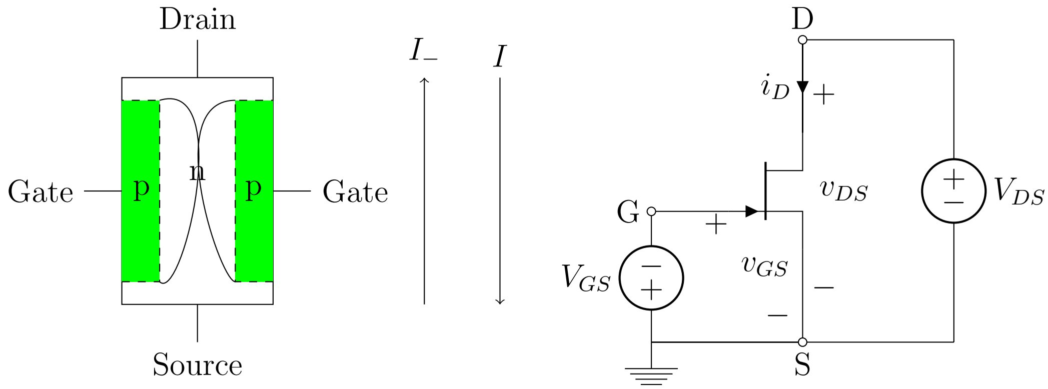


Figure 10.2: (a) Depletion Area for n-Channel (b) Reverse Biased at Gate-Source, $v_{GS} < 0$, $V_p < 0$

To begin, we define a depletion region is a region contains no mobile carriers and does not mean mobile carriers can not pass this region. A depletion region reduces the width of the conducting n channel when a reverse bias v_{GS} is applied to gate-source terminal. The depletion region increases (and hence resistance increases too) as the gate is more negative than the source. However, when the negative voltage reaches a critical negative value $V_p < 0$, the n channel is pinched off. Therefore, we define the pinch-off voltage (V_p) as the voltage of $v_{GS} < 0$ that will make the conducting channel almost disappears (because resistance becomes infinity) while the v_{DS} is held fixed.

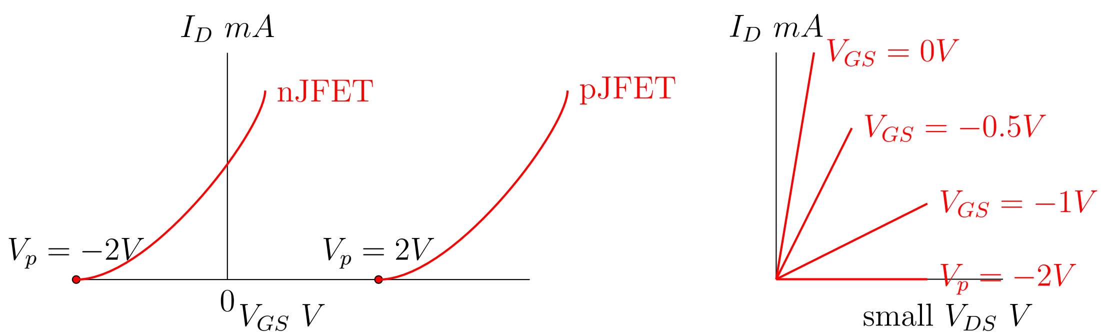


Figure 10.3: i_D vs. v_{GS}

Notice that for JFETs operations, $v_{GS} < 0$ must hold for all time because the pn junction will be forward biased when $v_{GS} > 0$ and the drain-source current will become uncontrollable.

As shown in Figure 10.2, under normal condition current will flow from drain to source if there is a voltage difference $v_{DS} > 0$ between them. (Notice that both pn junctions are reverse biased at all time while operating.)

1. When $0 < v_{DS} < 0.5$ is small, we have $v_{GD} = v_{GS} - v_{DS} < 0$ (still reverse biased on drain side pn junctions). The width of n-channel remains constant/uniform, like a resistor, and a linear relationship holds $i_D = \frac{v_{DS}}{r_{DS}}$, known as linear region (Figure 10.4)

2. When $0.5 < v_{DS}$ becomes larger, the reverse bias at the drain side $v_{GD} = v_{GS} - v_{DS} \leq V_p$ makes the n channel thinner and thinner, reaching pinch-off when $v_{GD} = v_{GS} - v_{DS} = V_p < 0$ or equivalently, $v_{DS} = v_{GS} - V_p > 0$.

3. When $v_{DS} \geq v_{GS} - V_p > 0 (= V_{DSS})$. The n channel becomes independent of further increases of v_{DS} because pinch-off is reached and no further depletion occurs. So the I_D current remains constant and it is called saturation region.

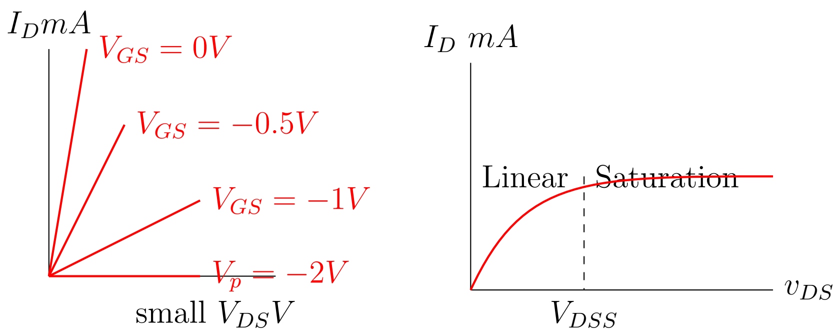


Figure 10.4: (a) Linear Region, $0 > V_{GS} > V_p$ (b) Linear and Saturation Region

Also notice that the negative electron flow goes from source to drain and the current is defined as flow of positive charges, we, therefore, have current flowing from drain to source for the n-channel JFETs, resulting in potential voltage at drain is higher than the potential voltage at source ($v_{DS} = v_D - v_S > 0$).

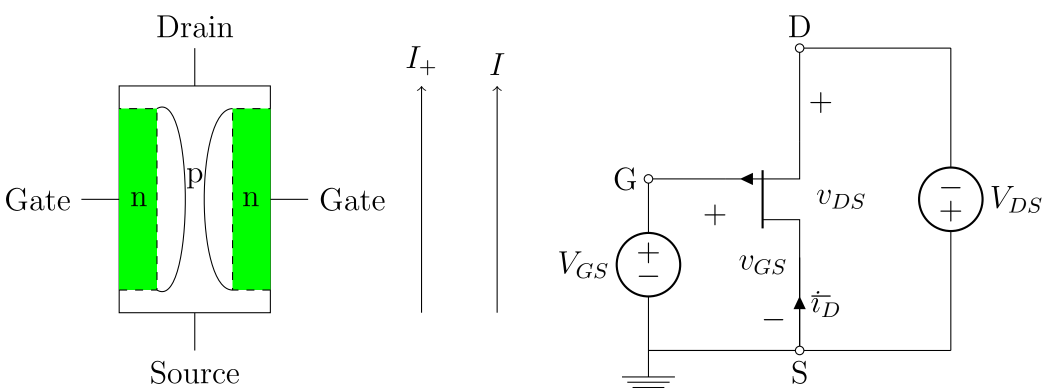


Figure 10.5: (a) Depletion Area for p-Channel (b) Reverse Biased at Gate-Source, $v_{GS} > 0$, $V_p > 0$.

We have explained the internal behaviors, resulting in are three operating regions:

- Cutoff Region: For $v_{GS} < V_p$, the pn junction between GS is reversed biased and $i_G = 0$.
- Triode Region (linear region): $v_{GD} \leq v_{GS} - V_p$ and $v_{GS} \geq V_p$. The drain current is given by

$$i_D = K[2(v_{GS} - V_p)v_{DS} - v_{DS}^2]$$

where V_p is the threshold voltage for JFET, device constant

$$K = \frac{W}{L}\frac{KP}{2}$$

and W and L is the width and length of the NMOS channel while $KP = 50\mu A$. It is noted that equation (10.1) is a function of v_{GS} and v_{DS} As readily seen in Figure 10.7, in the triode region the NMOS behaves as a voltage-controlled resistor whose i_D current is controlled by v_{DS}, but the resistor decreases as v_{GS} increases.

• Saturation Region: $v_{GD} > v_{GS} - V_p$ and $v_{GS} \geq V_p$ where i_D becomes constant in the sense that it is a function of v_{DS}, unknown but fixed at Q point.

$$i_D = K(v_{GS} - V_p)^2$$

It will become clear that these equations aforementioned are identical to MOSFETs. In summary, we have the following observations:

1. For n-type FETs, the charge carrier is free electrons and $V_p < 0$, while the charge carrier is holes for p-type FETs and $V_p > 0$.

2. Compared with Figures 10.2(b) and 10.5(b), the working principles are the same except the direction of drain current and polarity of bias voltage are reversed.

3. The Field Effect Transistor (FET) is an active device. In simple terms, it is a voltage controlled valve. The gate-source voltage (V_{GS}) controls the drain current (i_D).

4. A device which is normally-on at $v_{GS} = 0$ is termed a depletion-mode device.

5. We have explained the internal behaviors of JFETs from the physics properties of pn junctions. Another important unipolar devices to learn, known as MOSFETs, share the same internal behaviors and, fortunately, JFETs also share the same external behaviors with MOSFETs. Thus, in what follows, we will focus on study of the external electrical behavior of MOSFET when bias voltage is applied. In other words, we will skip the circuit analysis for JFETs because they are identical.

10.2 Metal-Oxide-Semiconductor Field-Effect Transistor

Abbreviated as MOSFET and shown in Figure 10.6, when a positive voltage is applied to the gate relative to the source, negative electrons are induced under the gate area because the oxide serve as a capacitor and in the beginning these electrons neutralize with p-type holes (resulting in depletion first), but as a threshold voltage is reached, the depletion area becomes an n-enhanced channel MOSFET (NMOS) and becomes conducting.

In a similar manner, PMOS is constructed by exchanging p and n material and a negative voltage is applied to the gate relative to the source, resulting in a p-enhanced channel under the gate area. Drain current is controlled by the voltage to the gate. The characteristics of an NMOS transistor

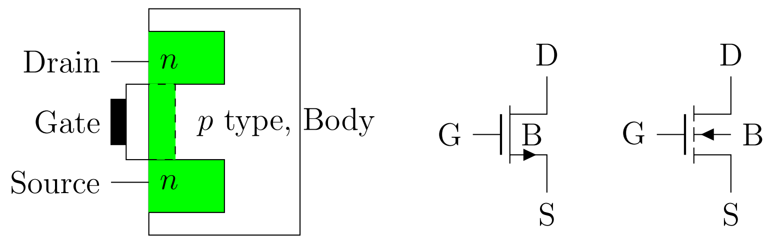


Figure 10.6: (a) NMOS/n Enhanced MOSFET Transistor, (b) Symbols

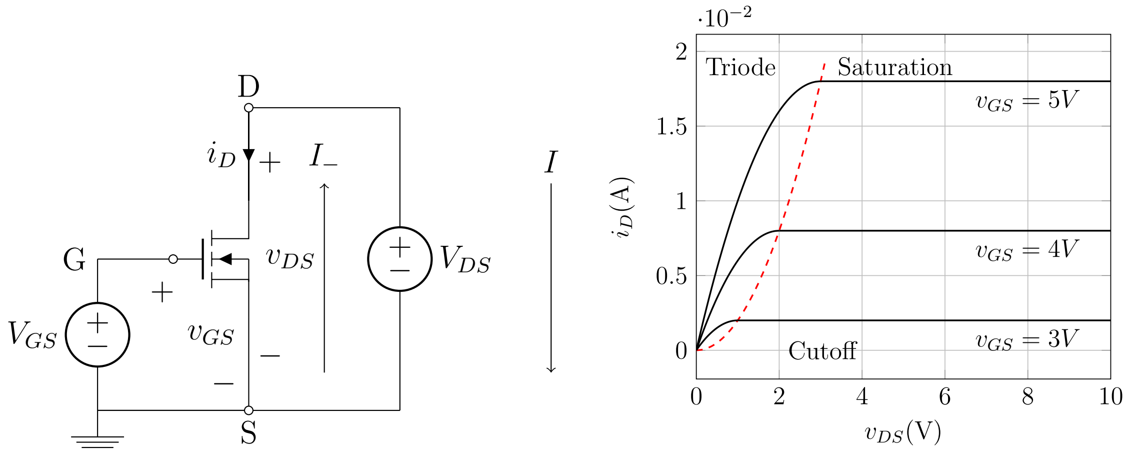


Figure 10.7: (a) Bias Circuit (b) Drain Characteristic Curves for an NMOS Transistor

is plotted below.
Since the internal behaviors are same as JFETs and were discussed previously, we will simply lay out three operating regions:

- Cutoff Region: For $v_{GS} < V_{to}$, the pn junction between DS is reversed biased and $i_D = 0$.
- Triode Region (linear region): $v_{DS} \leq v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$. The drain current is given by

$$i_D = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] \tag{10.1}$$

where V_{to} is the threshold voltage, device constant

$$K = \frac{W}{L}\frac{KP}{2}$$

and W and L is the width and length of the NMOS channel while $KP = 50\mu A$. It is noted that equation (10.1) is a function of v_{GS} and v_{DS} As readily seen in Figure 10.7, in the triode region the NMOS behaves as a voltage-controlled resistor whose i_D current is controlled by v_{DS}, but the resistor decreases as v_{GS} increases.

- Saturation Region: $v_{DS} > v_{GS} - V_{to}$ and $v_{GS} \geq V_{to}$ where i_D becomes constant in the sense that it is a function of v_{GS}, unknown but fixed at Q point.

$$i_D = K(v_{GS} - V_{to})^2 \tag{10.2}$$

• The boundary region occurs at $v_{DS} = v_{GS} - V_{to}$. Substituting $V_{to} = v_{GS} - v_{DS}$ into equation (10.1) yields

$$i_D = K v_{DS}^2 \tag{10.3}$$

characterizing the boundary in the $i_D - v_{DS}$ characteristic curve for NMOS transistors. Note that the curve is derived under the assumption of $v_{GS} \geq V_{to}$ and thus does not extend to $0 < v_{GS} < V_{to}$, because a forward bias on the junction would cause current to flow in the gate. Therefore $i_G = 0$ is a good approximation.

A device which is normally-off at zero gate-source voltage ($v_{GS} = 0$) is called a enhancement-made device.

10.3 Load-Line Analysis

Consider the following circuit, Figure 10.8, that could have been reduced from a self-biased four resistor structure. (See Figure 9.10 on 261 for inspiration.) To find an operating point in saturation

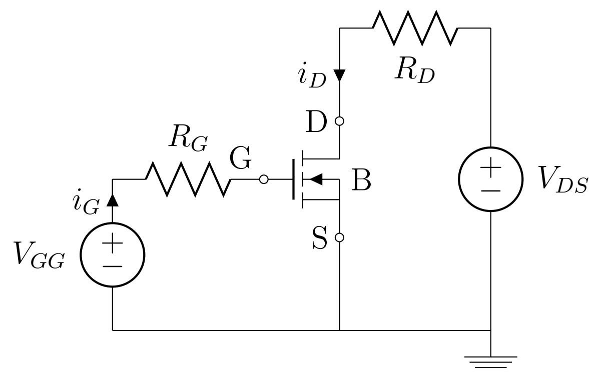


Figure 10.8: A Fixed Base Bias Circuit

region ($v_{DS} > v_{GS} - V_{to}$), we need to analyze the input circuit and output circuit respectively and this can be done using Kirchhoff's circuit laws.

$$V_{GG} = i_G R_G + v_{GS} + i_D R_D$$

which will intersect the x- and y-axis of the input characteristic curve at

$$x = v_{GS} = V_{GG}, \quad y = i_D = \frac{V_{BB}}{R_B}$$

and

$$i_D = K(v_{GS} - v_{to})^2$$

Similarly, for the output circuit, we have

$$V_{DD} = v_{DS} + i_D R_D$$

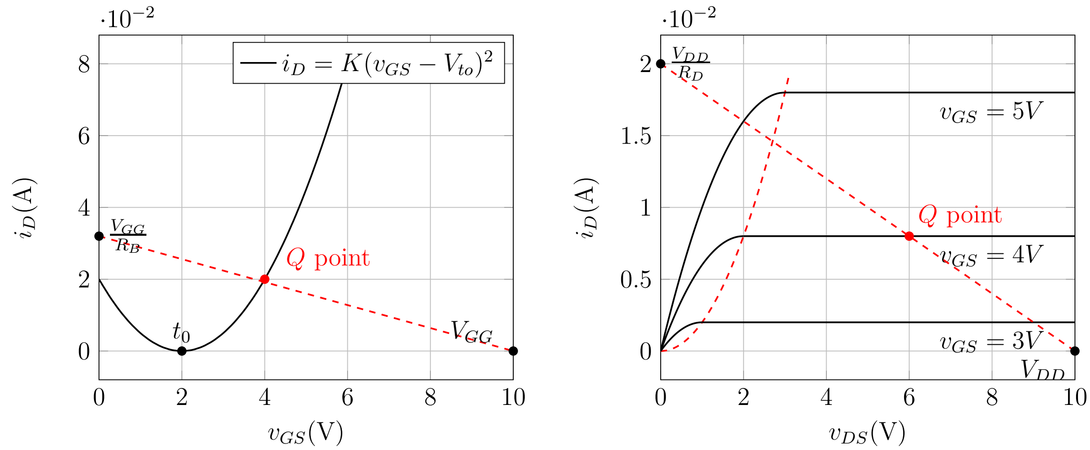


Figure 10.9: NMOS Load Line (a) Input $i - v$ Curve (b) Output $i - v$ Curve

$$x = v_{DS} = V_{DD}, \quad y = i_D = \frac{V_{DD}}{R_D}$$

Example 10.1 *Given the circuit shown in 10.10, find the Q point and v_{out}. The transistor has $KP = 50\mu A/V^2$, $V_{to} = 2V$, $L = 10\mu m$ and $W = 400\mu m$.*

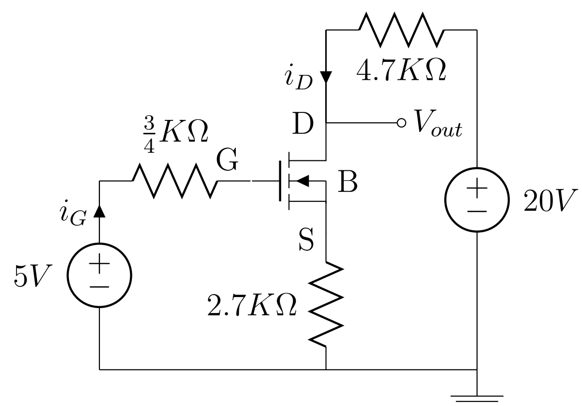


Figure 10.10: Example 10.1

Solution:

For input circuit and the analysis learned, to find Q point, we should solve the following simultaneous equations first

$$5 = v_{GSQ} + i_{DQ}2.7K \quad I_{DQ} = K(V_{GSQ} - 2)^2$$

where $K = \frac{W}{L}\frac{KP}{2} = 1mA/V^2$. After solving a quadratic equation, we find $V_{GSQ} = 2.87V$ and 0.74 (infeasible) and $I_{DQ} = 0.78mA$. And from the output circuit, we obtain

$$V_{out} = 20 - 0.78m \times 4.7K = 16.33V.$$

□

PSpiceLab 10.1 (Determination of Q Point) *Verify the circuits in Figure 10.10 and draw the load line via PSpice.*
Solution: *Objectives: (1) Understand the $i - v$ characteristics of input and output behaviors of NMOS. (2) Learn dual DC sweep techniques.*
PreLab: Study the analytical aspects detailed in 10.3.
Lab: Follow the steps to find the result as expected.
PostLab: Why is that R_G is missing?[1]

□

10.4 Small-Signal Circuit Models

The load line analysis is pretty straightforward and is known as the large-signal analysis because the bias DC values are much larger than AC excitations. Usually, for amplification, we need to apply circuit analysis instead of graphical analysis. To this end, we need an equivalent small-signal circuit in order that circuit theorem can be used. We have mentioned that for NMOS the drain current is a function of v_{DS} and v_{GS}, which is repeated here for convenience.

$$\begin{aligned} i_D &= K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2] \quad \text{for linear region} \\ i_D &= K(v_{GS} - V_{to})^2 \quad \text{for saturation region} \end{aligned}$$

We use notation below, assuming a Q point is established and a signal can be represented as a small AC excitation superimposed on the dc quantities

$$\begin{aligned} v_{GS} &= V_{GSQ} + v_{gs} \\ v_{DS} &= V_{DSQ} + v_{ds} \\ i_D &= I_{DQ} + i_d = I_{DQ} + \frac{v_{ds}}{r_d} \\ i_D &= I_{GQ} + i_d = I_{GQ} + g_m v_{gs} \end{aligned}$$

It is readily seen that transconductance between i_d and v_{gs} and drain resistance r_d

$$\frac{1}{r_d} = \frac{i_d}{v_{ds}} = \frac{\partial i_D}{\partial v_{DS}}|_{V_{DSQ}} = 2K[(V_{GSQ} - V_{to}) - V_{DSQ}] > 0 \text{ for linear region} \tag{10.4}$$

$$g_m = \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}|_{V_{GSQ}} = 2K(V_{GSQ} - V_{to}) \text{ for saturation region} \tag{10.5}$$

$$= 2\sqrt{KI_{DQ}} = \sqrt{2KP}\sqrt{W/L}\sqrt{I_{DQ}} \tag{10.6}$$

In particular, equation (10.6) says the values of g_m depend on Q point and device parameters. Thus increasing ratio of W/L or I_{DQ} obtains a higher value of g_m.

[1]Ans: $I_G = 0$ for reverse bias sake and the voltage drop on R_G would be zero.

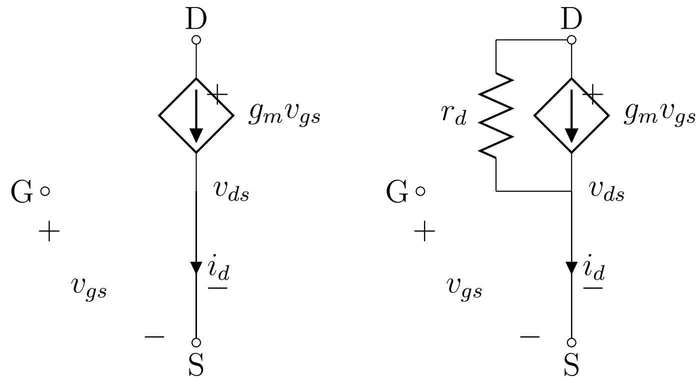


Figure 10.11: Voltage-Controlled Current Source

10.4.1 Basic NMOS Amplifier Configurations

Once the small-signal models, Figure 10.4, are established, we, in what follows, will investigate the small-signal circuit for the most commonly seen amplifiers based on NMOS.

Common-Source Amplifier (CS)

Consider the following actual circuit for a common-source amplifier. Based on the small-signal just

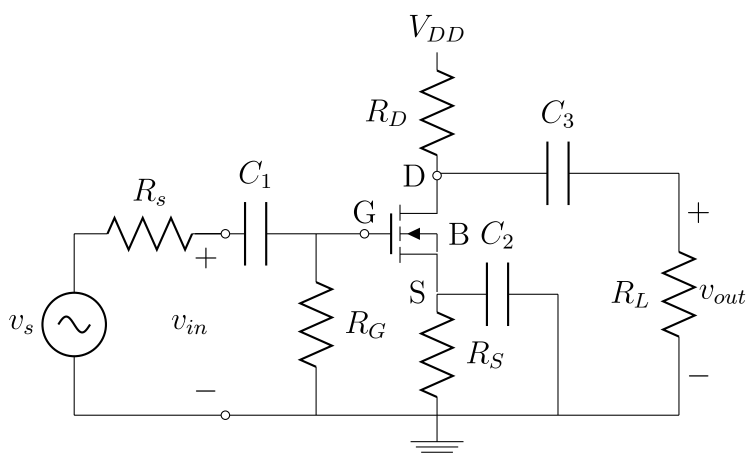


Figure 10.12: Common Source Configuration

obtained, Figure 10.12 is equivalent to the following small-signal AC circuit and the circuit analysis techniques can be applied.

- Voltage gain

$$A_v = \frac{v_{out}}{v_{in}} = \frac{0 - g_m v_{gs} R'_L}{v_{gs}} = -g_m R'_L \tag{10.7}$$

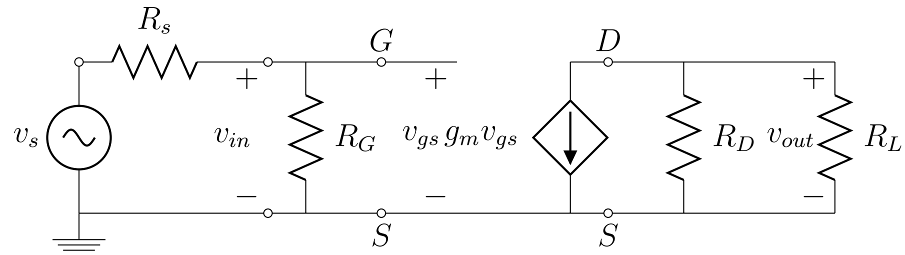


Figure 10.13: Small Signal AC Circuit for Common-Source Configuration

where $R_L' = R_L//R_D$ and the minus sign means a phase reversed.

- Open-circuit voltage gain

$$A_{vo} = \frac{v_{out}}{v_{in}}|_{R_L=\infty} = \frac{-g_m v_{be} R_C}{v_{be}} = -g_m R_C = -\frac{\beta}{r_\pi} R_C \tag{10.8}$$

- Input impedance seen looking into the input terminals

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{be}}{i_{in}} = R_G \tag{10.9}$$

- Current Gain

$$A_i = \frac{i_{out}}{i_{in}} = \frac{\frac{v_{out}}{R_L}}{\frac{v_{in}}{Z_{in}}} = A_v \frac{Z_{in}}{R_L} \tag{10.10}$$

- Output impedance seen looking back from the output terminals with source zeroed

$$Z_{out} = R_D \tag{10.11}$$

This is because $v_{gs} = 0$ due to source is shorted. Therefore, the voltage-controlled current source is open.

- Power gain

$$A_p = A_v A_i$$

Source follower

whose equivalent small-signal circuit is

- Voltage gain

Obviously, the output voltage is given below

$$v_{out} = g_m v_{gs} R_L'$$

and the input voltage is

$$v_{in} = v_{gs} + v_{out} = v_{gs}(1 + g_m R_L')$$

These two equations yield

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m R_L'}{1 + g_m R_L'} \tag{10.12}$$

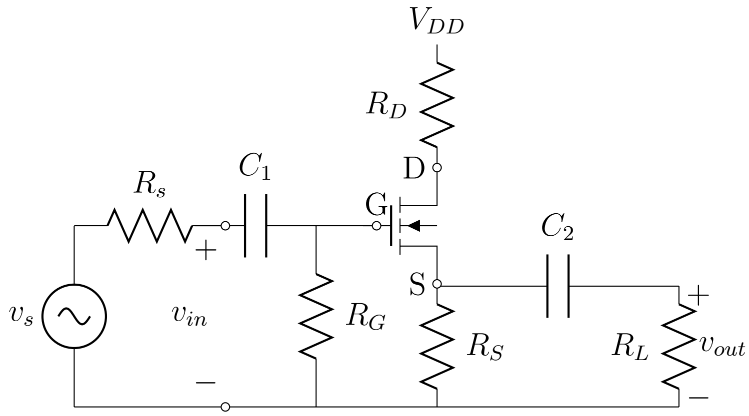


Figure 10.14: Source Follower Configuration

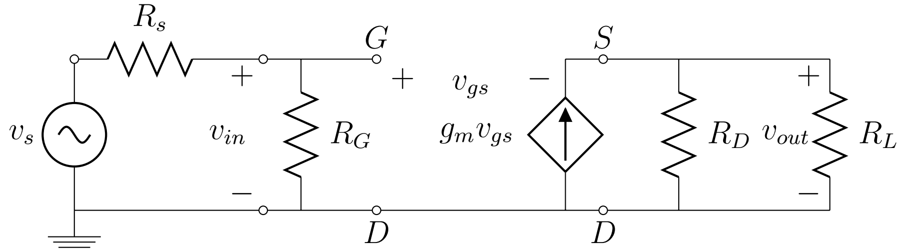


Figure 10.15: Small Signal AC Circuit for Source Follower Configuration

where $R'_L = R_L // R_D$ and the minus sign means a phase reversed.

- Open-circuit voltage gain

$$A_{vo} = \frac{v_{out}}{v_{in}}|_{R_L=\infty} = \frac{-g_m v_{be} R_C}{v_{be}} = -g_m R_C = -\frac{\beta}{r_\pi} R_C < 1 \tag{10.13}$$

- Input impedance seen looking into the input terminals

$$Z_{in} = \frac{v_{in}}{i_{in}} = R_G \tag{10.14}$$

- Current Gain

$$A_i = \frac{i_{out}}{i_{in}} = \frac{\frac{v_{out}}{R_L}}{\frac{v_{in}}{Z_{in}}} = A_v \frac{Z_{in}}{R_L} \tag{10.15}$$

- Output impedance seen looking back from the output terminals with source zeroed

$$Z_{out} = R_D \tag{10.16}$$

- Power gain

$$A_p = A_v A_i$$

Common-Gate Amplifier (CG)

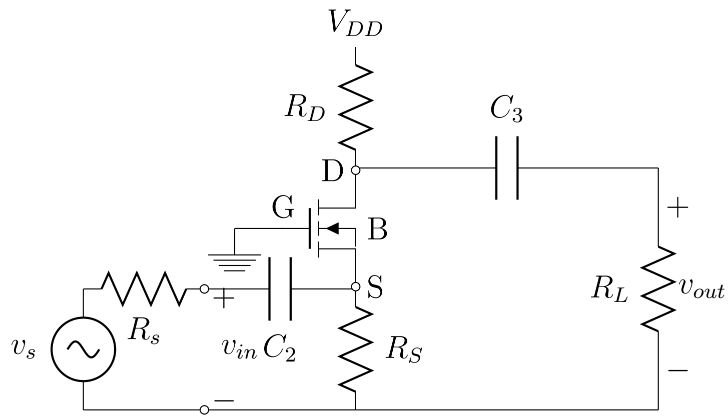


Figure 10.16: Common-Gate Configuration

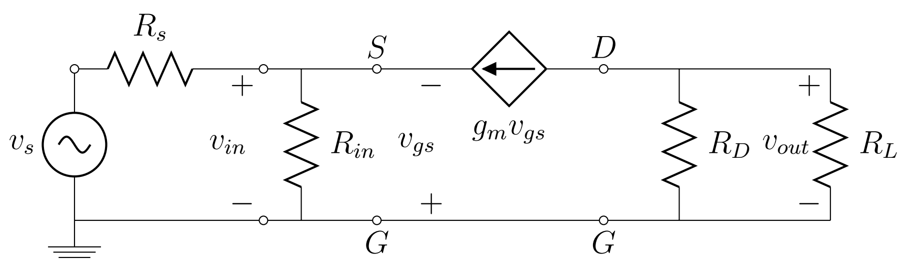


Figure 10.17: Small Signal AC Circuit for CG Configuration

where $R'_L = R_D//R_L$.

- Voltage gain

$$A_{vo} = \frac{v_{out}}{v_{in}}|_{R_L=\infty} = \frac{g_m v_i R_o}{v_i} = g_m(R_C//r_o)$$

the short-circuit current gain

$$A_{is} = \frac{i_o}{i_i}|_{R_L=0} = \frac{g_m v_i}{\frac{v_i}{R_i}} = g_m R_i = g_m(R_E//r_e) = g_m r_e = \alpha < 1$$

the overall voltage gain

$$A_v = \frac{v_o}{v_s} = \frac{v_o}{v_i}\frac{v_i}{v_s} = [g_m(R_o//R_L)]\frac{R_i}{R_i + R_S} = (\frac{r_e}{r_e + R_S})g_m(R_C//r_o//R_L)$$

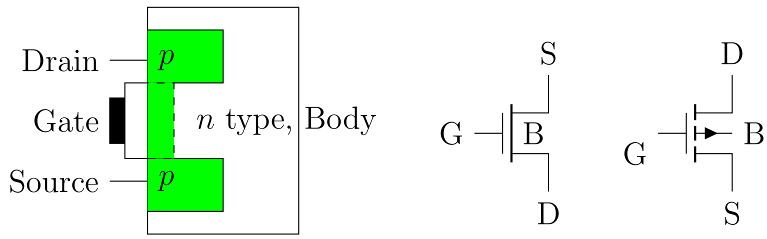


Figure 10.18: (a) PMOS/p Enhanced MOSFET Transistor (b) Symbols

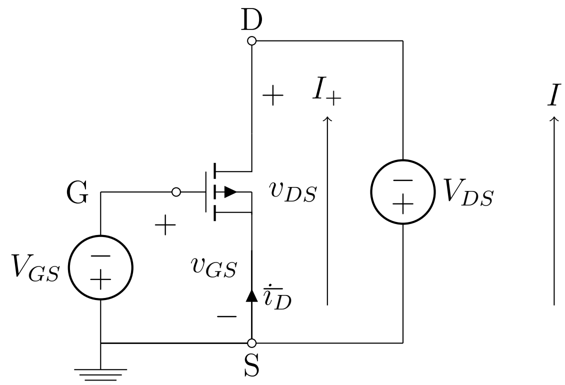


Figure 10.19: Bias Circuit for PMOS

10.5 PMOS Transistors

Interchanging the n and p region of n-enhanced NMOS devices establishes p-enhanced PMOS devices. The characteristics of PMOS is similar to those of NMOS and we will stop short on discussing their external properties further. However, the bias circuit merits an investigation.

Compare Figure 10.19 with Figure 10.7(a), we readily see that the voltage polarities and current direction are inverted. Notice that for PMOS, all v_{DS} and v_{GS} assume negative values and $V_{to} < 0$ while for NMOS, both assume positive values and $V_{to} > 0$.

When NMOS and PMOS are constructed on the same wafer, it is known as CMOS (complementary MOS)

PSpiceLab 10.2 (CMOS NOT Gate) *Verify the CMOS circuit via PSpice where a CMOS inverter is constructed with two MOS transistors. One is PMOS at the top and NMOS is at the bottom.*
Solution:
Objectives: NOT gate is the key to modern computer.
PreLab: NMOS at the top requires a positive voltage with respect to its source (which is connected to a +V_{CC}) to conduct while PMOS requires a negative voltage with respect to its source. Therefore.
V_{in}=high¿V_{to}, NMOS is shorted and PMOS is open. ⇒ V_{out}=low.
V_{in}=low¡V_{to}, NMOS is open and PMOS is shorted. ⇒ V_{out}=high.
Lab: Follow the steps to see confirmation.

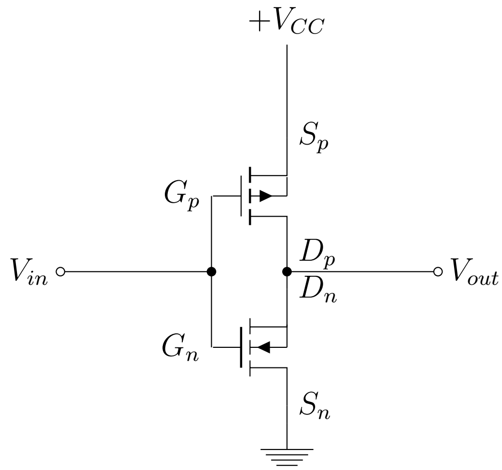


Figure 10.20: NOT GATE

PostLab: (1) CMOS NOT gate is known as logic gate since CMOS NAND gate and CMOS NOR gate can be constructed in a similar fashion. They are the backbone of VLSI (Very Large Scale Integration) circuits .

□

10.6 Recap

In this chapter, we learned

- Diode physics for *pn* junctions are crucial to understand the working principles of all bipolar devices.
- All sources are the providers of mobile carriers. *n*-type provides free electrons while *p*-time provides holes.
- NMOS can have 3 operating regions – triode, saturation and cutoff. It is a voltage-controlled current source.
- $i_G = 0$ is a unique feature in unipolar analysis.
- In triode region, it is linear region and serves as a resistor.
- Be aware of differences in the bias circuits for bipolar devices

10.7 Problems

Problem 10.1 *For the n-channel enhancement-only ideal MOSFET in Figure 10.21, the manufacturer specifies* $V_T = 4V$ *and* $I_{DS} = 7.2mA$ *at* $V_{GS} = 10V$. *For* $V_{DD} = 20V$ *and* $R_G = 100M\Omega$, *(a) find the constant* K. *(b) specify* R_D *for operation at* V_{DS} = *5 V.*

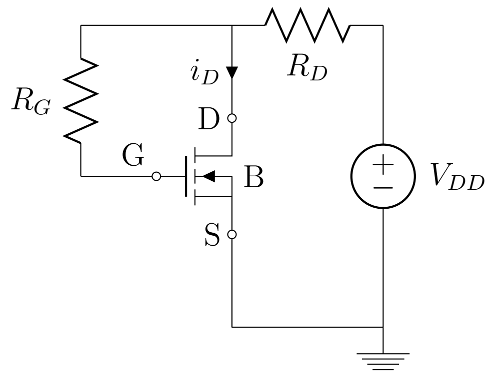


Figure 10.21: Circuit Diagram for Problem 10.1

Answer: *(a)* $I_{DS} = K(V_{GS} - V_T)^2$ *leads to* $K = 2 \times 10^{-4} A/V$. *(b) Since* $I_{DS} = 0.2mA$. $R_D = 75K\Omega$.

Chapter 11

PSpice Simulation Results

PSpice is a PC version of SPICE (which is currently available from OrCAD Corp. of Cadence Design Systems, Inc.). A student version (with limited capabilities) comes with various textbooks. The OrCAD student edition is called PSpice AD Lite. The PSpice Light version has the following limitations: circuits have a maximum of 64 nodes, 10 transistors and 2 operational amplifiers[5]-[10].

In this final chapter, we will pile up all the simulation results in each Chapter, obtained by using PSpice 9.1/9.2 simulation program. It is assumed that the readers have a PSpice program installed and have learned some basic knowledge such as

- Create a new Analog, mixed AD project.
- Place circuit parts.
- Connect the parts.
- Specify values and names.

If not, there are many wonderful web sites [5]-[10] providing such information and readers are encouraged to search and browse suitable web sites for a quick start.

11.1 Chapter 1

There are three PSpice lab experiments in this chapter. Aimed at introducing type of simulation analysis (Bias, DC sweep, AC sweep, and Time transient), this chapter brings **DC sweep** and **Time transient** analysis into attentions. All simulation procedures are listed, side by side, with PSpice circuits. It is imperative that first-time readers follow the step by step instructions to gain experiences and then modify them later.

11.2 Chapter 2

To verify KCL and KVL, PSpice is used to verify voltage divider and current divider.

11.3 Chapter 3

Circuit theorems are the focus of this chapter where equivalent circuits are sought. Among them, Thevenin and Norton equivalents are important. By attaching a mega resistance to terminals of concern and by closing the terminals of concern, Pspice can be used to find the V_{oc} and I_{sc}, respectively, resulting in Thevenin and Norton equivalent circuits. Another approach is to connect a switch that closes after a few seconds at the terminals of concern, we are able to find V_{oc} and I_{sc}, respectively, in setup.

For Chapter 1 to Chapter 3, DC bias point analysis is the main simulation tool in PSpice for DC circuit analysis.

11.4 Chapter 4

Turning to a new chapter, sinusoidal signal representing Alternating Current is introduced. Other than magnitude values, angle information is involved in dealing AC circuit, resulting in phasor representation of AC signals. Therefore, the complex computation is more involved than real number computations. Bias point analysis fails to provide a correct answer. Instead, sinusoidal steady-state solution requires **Frequency Sweep** for a single frequency and markers to show magnitudes and phases are often seen. Auxiliary commands/parts IPRINT and VPRINT2 are used to save the complex results into output files.

11.5 Chapter 5

In this chapter, we introduce switching circuits where ISIN, VSIN are the main current and voltage sources because this is a time solution which requires a fixed frequency in Hz be given. **Time Domain Transient** is the key analytical tool.

11.6 Chapter 6

This chapter focuses on frequency responses where VAC and IAC are selected for such purpose. **AC Sweep** is used to generate frequency responses. DB command and log scale are often seen in plotting a frequency response.

11.7 Chapter 7

For diodes circuits, we use PSpice to investigate $i - v$ characteristics of two important diodes, real diodes and Zener diodes and some examples on clipper circuits. DC sweep and Time transient are repeated here. Yet more plotting techniques are introduced. For example, (1) change the variables of x-axis, whose default variable is Time. (b) How to add text, line, find extremes, and/or insert its datum to an existing plot for better presentation of output.

11.8 Chapter 8

Since only two op-amps are allowed to use, we demonstrate via PSpice that an ideal amplifier is equivalent to a voltage-controlled voltage source from an input-output perspective. So VCVS can be a substitute for op-amps if more than two op-amps are needed.

11.9 Chapter 9

For BJT circuits, we introduce dual **DC Sweep** to generate output characteristic of a common-emitter BJT amplifier. With the load line technique taught in Chapter 7. Reader are able to find Q-point for small-signal analysis. Furthermore, such Q-point cab be found directly by DC bias point analysis,without using load line, .

11.10 Chapter 10

Again the dual **DC Sweep** learned from Chapter 9 works well for MOSFETs when $i-v$ characteristic curve are desired to plot. Load line analysis is repeated in this chapter for n enhanced MOSFETs where Q point analysis is obtained by load line as well as DC bias point. To appreciate the huge applications of MOSFETs in modern PC and communications, a CMOS inverter gate is demonstrated as a logic gate in this chapter.

Note: All circuits for **PSpiceLab** are drawn and tested when preparing PSpice simulations. The step by step procedure for conducting a PSpice simulation is written along with the corresponding circuits. Since these files are not compatible with the typesetting software LaTeX2e, the circuits diagram and simulation outputs are saved and stored in the accompanied CD rom.

Index

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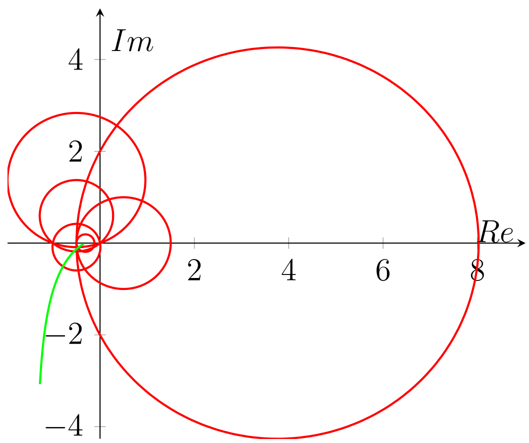
$$G(s) = \frac{50}{s(s+3)(s+6)}$$



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J.C. LO is a Professor of Mechanical Engineering at National Central University, Taiwan, receiving his Ph.D. degree in Electrical Engineering from Michigan State University, East Lansing, Michigan, in 1990. Since graduation, he jointed the Mechanical Engineering, actively teaching in circuits, microprocessor, and automatic control and deeply indulging in the area of fuzzy, robust, linear and nonlinear control.

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