A diagram of a machine

AI-generated content may be incorrect.

**Figure 1. Datapath of 5-Stage RV32I Pipelined Processor with Full Hazard Detection, Forwarding, and Control Logic**

A diagram of a computer hardware

AI-generated content may be incorrect.

**Figure 2. 5-Stage RV32I Pipelined Processor with External Instruction and Data Memory Interfaces**

**Table 1. Categorized Signal and Bus Lines in a 5-Stage RV32I Pipelined Processor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal Name** | **Bit Width** | **Source** | **Destination** | **Description** |
| CLK | 1 | Global | All synchronous logic | Clock signal |
| PCF | 32 | PC Register | Instruction Memory | Program Counter (current) |
| PCF' | 32 | PC Update Logic | PC Register | Next PC (from mux) |
| InstrF | 32 | Instruction Memory | IF/ID Register | Fetched instruction |
| PCPlus4F | 32 | Adder | IF/ID Register | PC + 4 for normal flow |
| StallF | 1 | Hazard Unit | PC Register | Stall PC update |
| InstrD | 32 | IF/ID Register | Control Unit | Instruction for decoding |
| PCD | 32 | IF/ID Register | Decode Stage | PC passed to Decode |
| Rs1D, Rs2D | 5 | InstrD | Register File / Hazard Unit | Source register IDs |
| RD1, RD2 | 32 | Register File | Decode Stage | Read data from registers |
| ImmExtD | 32 | Immediate Generator | ID/EX Register | Extended immediate value |
| PCPlus4D | 32 | IF/ID Register | ID/EX Register | PC+4 forwarded |
| PCE | 32 | ID/EX Register | Execute Stage | PC forwarded to execute stage (for jal/jalr) |
| RdD | 5 | InstrD | ID/EX Register | Destination register ID |
| RegWriteD | 1 | Control Unit | ID/EX Register | Write register enable |
| MemWriteD | 1 | Control Unit | ID/EX Register | Memory write enable |
| ALUSrcD | 1 | Control Unit | ID/EX Register | Select ALU source B |
| ResultSrcD | 2 | Control Unit | ID/EX Register | Select result (ALU, mem, PC+4) |
| BranchD | 1 | Control Unit | Hazard/Branch Logic | Branch instruction |
| JumpD | 1 | Control Unit | Hazard/Branch Logic | Jump instruction |
| ALUControlD | 3 | Control Unit | ID/EX Register | ALU control (pre-decoded) passed to execute stage |
| ImmSrcD | 2 | Control Unit | Imm. Gen | Immediate extension type |
| FlushD | 1 | Hazard Unit | IF/ID Register | Flush decode stage |
| StallD | 1 | Hazard Unit | IF/ID Register | Stall decode stage |
| RD1E, RD2E | 32 | ID/EX Register | Forwarding Muxes | Register data |
| Rs1E, Rs2E | 5 | ID/EX Register | Hazard Unit | Source register IDs |
| ImmExtE | 32 | ID/EX Register | ALU SrcB Mux | Extended immediate |
| SrcAE, SrcBE | 32 | Muxes | ALU | Operands to ALU |
| ALUResultE | 32 | ALU | EX/MEM Register | ALU computation result |
| ZeroE | 1 | ALU | Branch Control Logic | Zero flag from ALU result |
| WriteDataE | 32 | ID/EX Register | EX/MEM Register | Data to write to memory |
| PCTargetE | 32 | ALU/Branch Logic | PC Mux | Branch target |
| PCPlus4E | 32 | ID/EX Register | EX/MEM Register | PC+4 forwarded |
| RdE | 5 | ID/EX Register | EX/MEM Register | Destination register ID |
| RegWriteE | 1 | ID/EX Register | EX/MEM Register | Write register enable |
| MemWriteE | 1 | ID/EX Register | EX/MEM Register | Memory write enable |
| ALUSrcE | 1 | ID/EX Register | ALU SrcB Mux | Select ALU source B |
| ALUControlE | 3 | ALU Decoder | ALU | ALU operation select |
| ResultSrcE | 2 | ID/EX Register | EX/MEM Register | Select result |
| BranchE | 1 | ID/EX Register | Branch Logic | Branch indicator |
| JumpE | 1 | ID/EX Register | Branch Logic | Jump indicator |
| PCSrcE | 1 | Branch Control Logic | PC Mux / PC Register | Select next PC (branch taken) |
| FlushE | 1 | Hazard Unit | ID/EX Register | Flush execute stage |
| ForwardAE, ForwardBE | 2 | Hazard Unit | Muxes | Forwarding control |
| ALUResultM | 32 | EX/MEM Register | Data Memory | Memory address |
| WriteDataM | 32 | EX/MEM Register | Data Memory | Data to store |
| ReadDataM | 32 | Data Memory | MEM/WB Register | Data from memory |
| PCPlus4M | 32 | EX/MEM Register | MEM/WB Register | PC+4 forwarded |
| RdM | 5 | EX/MEM Register | MEM/WB Register | Destination register ID |
| MemWriteM | 1 | EX/MEM Register | Data Memory | Write enable |
| RegWriteM | 1 | EX/MEM Register | MEM/WB Register | Write register enable |
| ResultSrcM | 2 | EX/MEM Register | MEM/WB Register | Select result source |
| ReadDataW | 32 | MEM/WB Register | Writeback Mux | Memory read data |
| ALUResultW | 32 | MEM/WB Register | Writeback Mux | ALU result |
| PCPlus4W | 32 | MEM/WB Register | Writeback Mux | PC+4 (e.g., for jal) |
| ResultW | 32 | Writeback Mux | Register File | Final result to write |
| RdW | 5 | MEM/WB Register | Register File | Destination register ID |
| RegWriteW | 1 | MEM/WB Register | Register File | Register write enable |
| ResultSrcW | 2 | MEM/WB Register | Writeback Mux | Select result source |