A diagram of a machine

AI-generated content may be incorrect.

**Figure 1. Datapath of 5-Stage RV32I Pipelined Processor with Full Hazard Detection, Forwarding, and Control Logic**

A diagram of a computer hardware

AI-generated content may be incorrect.

**Figure 2. 5-Stage RV32I Pipelined Processor with External Instruction and Data Memory Interfaces**

**A diagram of a green square

AI-generated content may be incorrect.**

**Figure 3. Netlist View of 5-Stage RV32I Pipelined Processor with External Instruction and Data Memory Interfaces**

**A diagram of a computer

AI-generated content may be incorrect.**

**Figure 4. Netlist View of 5-Stage RV32I Pipelined Processor**

**A diagram of a computer

AI-generated content may be incorrect.**

**Figure 7. Netlist View of Controller of 5-Stage RV32I Pipelined Processor**

**A computer screen shot of a diagram

AI-generated content may be incorrect.**

**Figure 8. Netlist View of Hazard Unit of 5-Stage RV32I Pipelined Processor**

**A computer screen shot of a computer

AI-generated content may be incorrect.**

**Figure 8. Overall Netlist View of Data Path of 5-Stage RV32I Pipelined Processor**

**A computer screen shot of a computer

AI-generated content may be incorrect.**

**Figure 5. Netlist View of Data Memory**

**A computer program with text

AI-generated content may be incorrect.**

**Figure 6. Netlist View of Instruction Memory**

**Table 1. Categorized Signal and Bus Lines in a 5-Stage RV32I Pipelined Processor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal Name** | **Bit Width** | **Source** | **Destination** | **Description** |
| **Global Signals** | | | | |
| clk | 1 | Global | All synchronous logic | Clock signal |
| rst | 1 | Global | All reset logic | Asynchronous reset |
| **Fetch Stage (F)** | | | | |
| pcF | 32 | Freg | Instruction Memory | Program Counter (current) |
| pcF0 | 32 | PCmux | Freg | Next PC value |
| InstrF | 32 | Instruction Memory | Dreg | Fetched instruction |
| PCPlus4F | 32 | PCplus4 adder | Dreg | PC + 4 for sequential flow |
| StallF | 1 | Hazard Unit | Freg | Stall PC update |
| **Decode Stage (D)** | | | | |
| InstrD | 32 | Dreg | Controller | Decoded instruction |
| pcD | 32 | Dreg | Ereg | PC value in decode |
| Rs1D, Rs2D | 5 | InstrD | Hazard Unit | Source register IDs |
| Read1D, Read2D | 32 | reg\_file | Ereg | Register read data |
| ImmExtD | 32 | extender | Ereg | Extended immediate |
| PCPlus4D | 32 | Dreg | Ereg | PC+4 forwarded |
| RdD | 5 | InstrD | Ereg | Destination register |
| RegWriteD | 1 | Controller | Ereg | Register write enable |
| MemWriteD | 1 | Controller | Ereg | Memory write enable |
| JumpD, BranchD | 1 | Controller | Ereg | Jump/Branch control |
| ALUSrcD | 1 | Controller | Ereg | ALU source select |
| ALUControlD | 3 | Controller | Ereg | ALU operation control |
| ResultSrcD | 2 | Controller | Ereg | Result source select |
| ImmSrcD | 2 | Controller | extender | Immediate format select |
| **Execute Stage (E)** | | | | |
| Read1E, Read2E | 32 | Ereg | Forwarding muxes | Register data |
| pcE | 32 | Ereg | PCplusbranch | PC in execute |
| ImmExtE | 32 | Ereg | srcBmux2 | Extended immediate |
| PCPlus4E | 32 | Ereg | Mreg | PC+4 forwarded |
| PCTargetE | 32 | PCplusbranch | PCmux | Branch/Jump target |
| SrcAE, SrcBE | 32 | Muxes | ALU | ALU operands |
| ALUResultE | 32 | ALU | Mreg | ALU result |
| WriteDataE | 32 | srcBmux1 | Mreg | Store data |
| RegWriteE | 1 | Ereg | Mreg | Register write enable |
| MemWriteE | 1 | Ereg | Mreg | Memory write enable |
| ALUSrcE | 1 | Ereg | srcBmux2 | ALU source B select |
| ResultSrcE | 2 | Ereg | Mreg | Result select |
| ZeroE | 1 | ALU | Branch logic | Zero flag |
| OverflowE | 1 | ALU | - | Overflow flag |
| **Memory Stage (M)** | | | | |
| ALUResultM | 32 | Mreg | Data Memory/Wreg | Memory address/ALU result |
| WriteDataM | 32 | Mreg | Data Memory | Store data |
| PCPlus4M | 32 | Mreg | Wreg | PC+4 forwarded |
| RegWriteM | 1 | Mreg | Wreg | Register write enable |
| MemWriteM | 1 | Mreg | Data Memory | Memory write enable |
| ResultSrcM | 2 | Mreg | Wreg | Result select |
| RdM | 5 | Mreg | Wreg | Destination register |
| **Writeback Stage (W)** | | | | |
| ALUResultW | 32 | Wreg | rsltmux | ALU result |
| ReadDataW | 32 | Wreg | rsltmux | Memory read data |
| PCPlus4W | 32 | Wreg | rsltmux | PC+4 value |
| ResultW | 32 | rsltmux | reg\_file | Write data |
| RegWriteW | 1 | Wreg | reg\_file | Register write enable |
| ResultSrcW | 2 | Wreg | rsltmux | Result select |
| RdW | 5 | Wreg | reg\_file | Destination register |

**Table 2. ImmSrc Encoding**

|  |  |  |  |
| --- | --- | --- | --- |
| **ImmSrc** | **ImmExt** | **Type** | **Description** |
| **000** | {{20{Instr[31]}}, Instr[31:20]} | **I** | 12-bit signed immediate |
| **001** | {{20{Instr[31]}}, Instr[31:25], Instr[11:7]} | **S** | 12-bit signed immediate |
| **010** | {{20{Instr[31]}}, Instr[7], Instr[30:25], Instr[11:8], 1’b0} | **B** | 13-bit signed immediate |
| **011** | {{12{Instr[31]}}, Instr[19:12], Instr[20], Instr[30:21], 1’b0} | **J** | 21-bit signed immediate |
| **100** | {Instr[31:12], 12’b0} | **U** | 12-bit signed immediate |

**Table 3. Main Decoder Truth Table**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **op** | **Reg-Write** | **Imm-Src** | **ALU-Src** | **Mem-Write** | **Result-Src** | **Branch** | **ALU-Op** | **Jump** | **Instruction** |
| 0110011 | 1 | xxx | 00 | 0 | 00 | 0 | 10 | 0 | R-type |
| 0010011 | 1 | 000 | 01 | 0 | 00 | 0 | 10 | 0 | I-type ALU |
| 0000011 | 1 | 000 | 01 | 0 | 01 | 0 | 00 | 0 | I-type Load |
| 0100011 | 0 | 001 | 01 | 1 | 00 | 0 | 00 | 0 | S-type |
| 1100011 | 0 | 010 | 00 | 0 | 00 | 1 | 01 | 0 | B-type |
| 1101111 | 1 | 011 | 00 | 0 | 10 | 0 | 00 | 1 | jal |
| 1100111 | 1 | 000 | 01 | 0 | 10 | 0 | 00 | 1 | jalr |
| 0110111 | 1 | 100 | 01 | 0 | 00 | 0 | 11 | 0 | lui |
| 0010111 | 1 | 100 | 11 | 0 | 00 | 0 | 11 | 0 | auipc |
| 1110011 | 0 | xxx | 00 | 0 | 00 | 0 | 00 | 0 | ecall, ebreak |

**Table 4. ALU Decoder Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **ALUOp** | **funct3** | **{op5, funct75}** | **ALUSrc1** | **ALUControl** | **Instruction** |
| 00 | x | x | x | 0000 | I-type Load, S-type, jal, jalr, ecall, ebreak |
| 01 | x | x | x | 0001 | B-type |
| 10 | 000 | 00, 01, 10 | x | 0000 | add, addi |
| 000 | 11 | x | 0001 | beq, bne |
| 001 | x | x | 0110 | sll, slli |
| 010 | x | x | 0101 | slt, slti, blt, bge |
| 011 | x | x | 1001 | sltu, sltui, bltu, bgeu |
| 100 | x | x | 0100 | xor, xori |
| 101 | x0 | x | 0111 | srl, srli |
| x1 | x | 1000 | sra, srai |
| 110 | x | x | 0011 | or, ori |
| 111 | x | x | 0010 | and, andi |
| 11 | x | x | 0 | 1011 | lui |
| x | x | 1 | 1100 | auipc |

**Table 5. BRU Truth Table**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Branch** | **Jump** | **funct3** | **Zero** | **ALUResult0** | **PCSrc** | **Instruction** |
| 1 | 0 | 000 | x | x | Zero | beq |
| 001 | x | x | ~Zero | bne |
| 100 | x | x | ALUResult0 | blt |
| 101 | x | x | ~ALUResult0 | bge |
| 110 | x | x | ALUResult0 | bltu |
| 111 | x | x | ~ALUResult0 | bgeu |
| 0 | 1 | xxx | x | x | 1 | jal, jalr |

**Table 6. EU Truth Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **op** | **funct12** | **Ecall** | **Ebreak** | **Instruction** |
| 1110011 | 000000000000 | 1 | x | ecall |
| 1110011 | 000000000001 | x | 1 | ebreak |