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**Figure 1. Datapath of 5-Stage RV32I Pipelined Processor with Full Hazard Detection, Forwarding, and Control Logic**

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**Figure 2. 5-Stage RV32I Pipelined Processor with External Instruction and Data Memory Interfaces**

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**Figure 3. Netlist View of 5-Stage RV32I Pipelined Processor with External Instruction and Data Memory Interfaces**

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**Figure 4. Netlist View of 5-Stage RV32I Pipelined Processor**

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**Figure 7. Netlist View of Controller of 5-Stage RV32I Pipelined Processor**

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**Figure 8. Netlist View of Hazard Unit of 5-Stage RV32I Pipelined Processor**

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**Figure 8. Overall Netlist View of Data Path of 5-Stage RV32I Pipelined Processor**

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**Figure 5. Netlist View of Data Memory**

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**Figure 6. Netlist View of Instruction Memory**

**Table 1. Categorized Signal and Bus Lines in a 5-Stage RV32I Pipelined Processor**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal Name** | **Bit Width** | **Source** | **Destination** | **Description** |
| **Global Signals** | | | | |
| clk | 1 | Global | All synchronous logic | Clock signal |
| rst | 1 | Global | All reset logic | Asynchronous reset |
| **Fetch Stage (F)** | | | | |
| pcF | 32 | Freg | Instruction Memory | Program Counter (current) |
| pcF0 | 32 | PCmux | Freg | Next PC value |
| InstrF | 32 | Instruction Memory | Dreg | Fetched instruction |
| PCPlus4F | 32 | PCplus4 adder | Dreg | PC + 4 for sequential flow |
| StallF | 1 | Hazard Unit | Freg | Stall PC update |
| **Decode Stage (D)** | | | | |
| InstrD | 32 | Dreg | Controller | Decoded instruction |
| pcD | 32 | Dreg | Ereg | PC value in decode |
| Rs1D, Rs2D | 5 | InstrD | Hazard Unit | Source register IDs |
| Read1D, Read2D | 32 | reg\_file | Ereg | Register read data |
| ImmExtD | 32 | extender | Ereg | Extended immediate |
| PCPlus4D | 32 | Dreg | Ereg | PC+4 forwarded |
| RdD | 5 | InstrD | Ereg | Destination register |
| RegWriteD | 1 | Controller | Ereg | Register write enable |
| MemWriteD | 1 | Controller | Ereg | Memory write enable |
| JumpD, BranchD | 1 | Controller | Ereg | Jump/Branch control |
| ALUSrcD | 1 | Controller | Ereg | ALU source select |
| ALUControlD | 3 | Controller | Ereg | ALU operation control |
| ResultSrcD | 2 | Controller | Ereg | Result source select |
| ImmSrcD | 2 | Controller | extender | Immediate format select |
| **Execute Stage (E)** | | | | |
| Read1E, Read2E | 32 | Ereg | Forwarding muxes | Register data |
| pcE | 32 | Ereg | PCplusbranch | PC in execute |
| ImmExtE | 32 | Ereg | srcBmux2 | Extended immediate |
| PCPlus4E | 32 | Ereg | Mreg | PC+4 forwarded |
| PCTargetE | 32 | PCplusbranch | PCmux | Branch/Jump target |
| SrcAE, SrcBE | 32 | Muxes | ALU | ALU operands |
| ALUResultE | 32 | ALU | Mreg | ALU result |
| WriteDataE | 32 | srcBmux1 | Mreg | Store data |
| RegWriteE | 1 | Ereg | Mreg | Register write enable |
| MemWriteE | 1 | Ereg | Mreg | Memory write enable |
| ALUSrcE | 1 | Ereg | srcBmux2 | ALU source B select |
| ResultSrcE | 2 | Ereg | Mreg | Result select |
| ZeroE | 1 | ALU | Branch logic | Zero flag |
| OverflowE | 1 | ALU | - | Overflow flag |
| **Memory Stage (M)** | | | | |
| ALUResultM | 32 | Mreg | Data Memory/Wreg | Memory address/ALU result |
| WriteDataM | 32 | Mreg | Data Memory | Store data |
| PCPlus4M | 32 | Mreg | Wreg | PC+4 forwarded |
| RegWriteM | 1 | Mreg | Wreg | Register write enable |
| MemWriteM | 1 | Mreg | Data Memory | Memory write enable |
| ResultSrcM | 2 | Mreg | Wreg | Result select |
| RdM | 5 | Mreg | Wreg | Destination register |
| **Writeback Stage (W)** | | | | |
| ALUResultW | 32 | Wreg | rsltmux | ALU result |
| ReadDataW | 32 | Wreg | rsltmux | Memory read data |
| PCPlus4W | 32 | Wreg | rsltmux | PC+4 value |
| ResultW | 32 | rsltmux | reg\_file | Write data |
| RegWriteW | 1 | Wreg | reg\_file | Register write enable |
| ResultSrcW | 2 | Wreg | rsltmux | Result select |
| RdW | 5 | Wreg | reg\_file | Destination register |

**Table 2. ImmSrc Encoding** A screenshot of a computer

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**Table 3. Main Decoder (Controller) Truth Table**

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A table with numbers and letters

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**A table with numbers and letters

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**Table 3. ALU Decoder (Controller) Truth Table**

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