POSSESSION OF MOBILES IN EXAM IS UFM PRACTICE

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Jaypee Institute of Information Technology, Noida
Test-2 Examination, ODD Semester 2024
B.Tech., V Semester

Course Title: Computer Organization and Architecture **Max Time: 1 Hr**
Course Code: 15B11CI313 **Max Marks: 20**

Course Outcomes: At the end of the course, students will be able to:

CO1	Summarize and Classify the different computer systems based on RISC and CISC Architecture.
CO2	Apply the knowledge of performance metrics to find the performance of systems.
CO3	Examines various types of computers based on Instruction Set Architectures.
CO4	Analyze RISC and CISC based system designs for Hardwired and Micorprogrammed Controller.
CO5	Apply the knowledge of pipeline, IO and cache to understand these systems. Further, analyze the performance of such systems.
CO6	Create and analyze an assembly language program of RISC and CISC-based systems

Note: Attempt all the questions.

Q1. Write the program code for the following expression with three address and zero address instructions

X=A-B+C*(D*E-F)/G

(a) Using a general register computer with three address instructions.

(b) Using a stack organized computer with zero address operation instructions.

In the problem, assume that values of A, B, C, D, E, F, G reside in memory. Also assume that opcodes are 8 bits, memory addresses are 64 bits, and register addresses are 8 bits. Find the total size of code in bytes in each case . **[CO3 (Applying), 3 Marks]**

Q2. Assume an instruction set that uses a fixed 16 bit instruction length. Each operand specifiers requires 6 bits in length. So two operand will require 12 bits and one operand 6 bits and so on. There are K two - operand instructions and L zero-operand instructions. What is the maximum number of one operand instructions that can be supported? Suppose K is 15 and L is 1024. Give possible opcode range of two-operand , one-operand and zero-operand instructions in binary. **[CO3 (Applying), 3 Marks]**

Q3. The instruction **LHLD 3148H** is stored at memory location **2500H** in an 8085 microprocessor. This instruction is used to load the content of two consecutive memory locations into the **H** and **L** registers. Assume that the memory locations **3148H** and **3149H** hold the values **34H** and **12H** respectively. The machine code for **LHLD** is **2AH**.

a) Find the number of machine cycle and T states required for the execution of this instruction.

b) After the execution of the **LHLD** instruction, what will be the values of the **L** and **H** registers?.

c) Draw the timing diagram for the execution of the **LHLD 3148H** instruction, including all necessary address, data, ALE, IO/M, S0, S1, RD, WR for opcode fetch. **[CO4 (Analyzing), 4 Marks]**

Q4. Suppose 8085 microprocessor uses RAM chips of 1024*4 bit capacity. How many chips will be required to obtain a memory of capacity of 64 K bytes? Also explain how the chips are to be connected to address bus. Draw diagram for selection/decoder logic and give address range for each byte read.

[CO5 (Analyzing), 4 Marks]

Q5. Calculate the time delay for this program. Assume the clock frequency of the system is 5 MHz. Calculate the total time delay for this program. What will be the final value in the accumulator after the execution of the loop?

```
        MVI A ,25H      7T
        MVI B ,02H      7T
        MVI C,07H       7T
LOOP:   ADD B           4T
        DCR C           4T
        JNZ LOOP        10/7T
```

[CO6 (Evaluating), 3 Marks]

Q6. Given MIPS assembly code:

```
lw $t1, 8($t2)      # Line 1
beq $t0, $t1, 8     # Line 2
```

Initial conditions:

- Instruction memory starts at address 0*2000
- $t2 = 0*1000
- Memory [0*1008] = 5
- $t0 = 5

What instruction format and addressing mode is used for the lw and beq instruction in line 1 and 2, and what is the effective/target address for the memory access?. **[CO6 (Evaluating), 3 Marks]**

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