CS 250 Spring 2017 Homework 03
Due 11:58pm Wednesday, February 01, 2017
Submit your typewritten file in PDF format to Blackboard.

1. If propagation delay in a combinatorial circuit is measured in gate delays, how long before all outputs are valid for a 16-bit ripple carry adder circuit?

   1-bit ripple carry adder has 1 full adder, therefore a 16-bit ripple carry adder circuit has 16. The propagation delay is therefore 3 + 15 * 2 = 33 gate delays. (3 in the beginning and 2 for every thereafter)

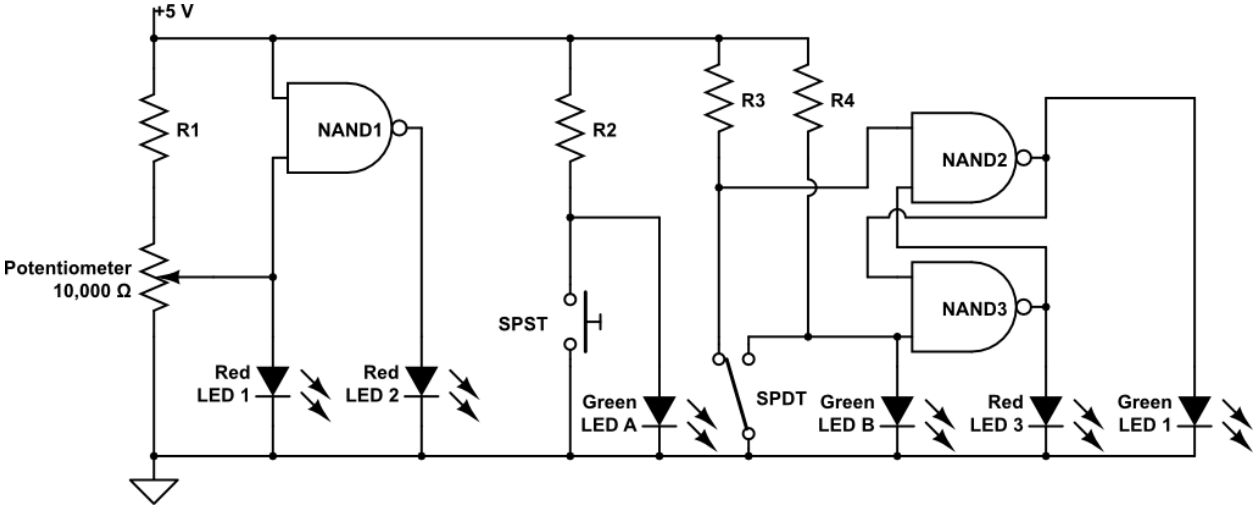
2. The rising-edge-triggered 74163 counter chip is being clocked with an SR latch, the same as in Lab 02.
   a. What is the shortest sequence of Set and Reset operations that will advance the count from 14 to 3? Use S to mean set and R to mean reset and write your answer in the form of an ASCII character string.

      SRSRSRSRS

   b. Extra thought: Using a regular expression, describe all sequences of Set and Reset that will drive the count from 14 to 3.

      (R-S){9}

3. Consider the schematic below for the following questions. The difference between this circuit and the circuit of Lab 02 is that the 74163 counter has been removed.



   a. Which LED shows that it is possible to operate LEDs at half brightness rather than just fully off or fully on. Be sure to use the exact name shown in the schematic so that there is no ambiguity in your answer.

Red LED1 shows this when turning the potentiometer as it shows it can operate at a variety of brightness's. Also, Green LED A and Green LED B are consistently dimly lit, also showing that it is possible to operate LEDs at half brightness however this could be due to lack of resistance and not part of the experiment. The main demonstration of dimly lit LEDs was the Red LED1.

b. Name all LEDs in the schematic above that are connected to debounced clock signals. If no such LED exists, write "None." Be sure to use the exact name shown in the schematic so that there is no ambiguity in your answer.

Red LED 2 and Red LED 3

c. Let Red LED3 be the Q' output of the S'R' latch formed by NAND2 and NAND3. The moving pole of the SPDT switch has three positions: connected to R3 (R3, for a short name), in between the R3 and R4 contacts (B, for a short name) where the pole is connected to nothing, and connected to R4 (just called R4). Fill in the five missing entries in the following table for each time step from 0 to 5.

Time	SPDT position	Red LED 3 state
0	R3	OFF
1	R3	**OFF**
2	B	**OFF**
3	R4	**ON**
4	B	**ON**
5	**R3**	OFF

4. Complete the table to show how the given binary strings are writing in each representational form. If a binary string is not valid for a given representation, write "error" in the table.

Given binary string	**Written as octal**	**Written as hexadecimal (0x)**
110011011111	6337	CDF
010111110001	2761	5F1

5. Complete the table to show how the given binary strings are interpreted in each data representation. For numerical representations write your answer in the form of a decimal number. Use care when writing a decimal number equivalent to show a sign when there is ambiguity if a sign is not shown. The table headings "1's" and "2's" are short for one's complement and two's complement, respectively. If a binary string is not valid for a given representation, write "error" in the table.

Given binary string	Unsigned integer	Sign magnitude	1's	2's	ASCII character
10110100	180	-52	01001011	01001100	error
00000101	5	5	11111010	11111011	ENQ
00000000	0	0	11111111	100000000 (assuming >8 bits allowed, 'error' if not allowed)	NUL
11111111	255	-127	00000000	00000001	error

6. What is the 16-bit representation of the 2's complement number 11101010?

Following the rule of sign extension for 2's complement….

Final Answer: 1111111111101010