CS 250 Spring 2017 Homework 02
Due 11:58pm Wednesday, January 25, 2017
Submit your typewritten file in PDF format to Blackboard.


1. Write out the POS expression for 2-intput XNOR.

   Product of Sums: $F = (A + B')(A' + B)$

2. The normally-open (NO) SPST push button switch (same type as in the lab kit) transitions from high resistance to low resistance when pushed. The normally-closed (NC) SPST push button switch reverses this behavior. The schematic symbols for these two switches are shown here.
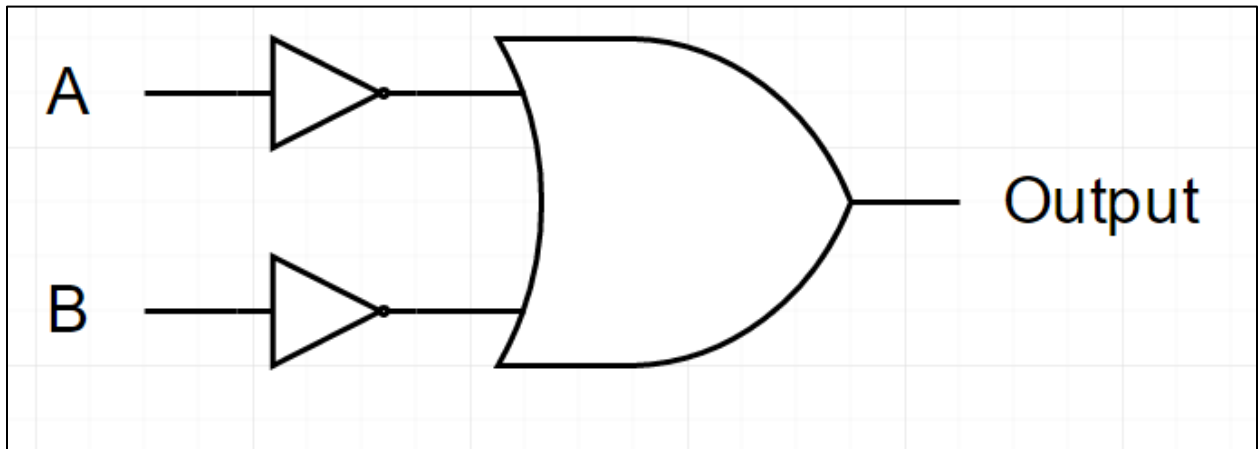
   NO SPST   **NC SPST**
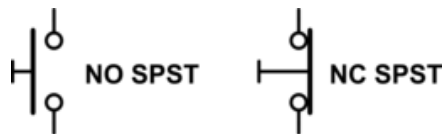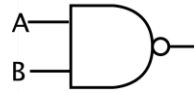
   Using these two switch types, wire, and connections to +5 V and ground, draw a schematic to implement (AB)' and clearly label your inputs and output.

   NAND a.k.a. (AB)'

   +5v

   A   B

   Output

   A

   B
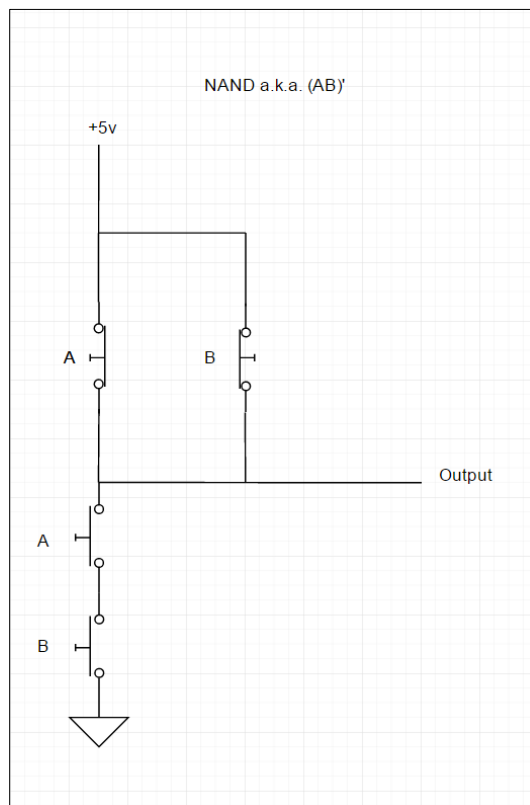
   Made with draw.io

3. Examine the gate shown below, then draw an equivalent single gate that does not contain a NAND gate nor an AND gate.

We can achieve a similar output to the NAND gate shown by negating the inputs of an OR, as seen above.

Above image made with draw.io

4. The most important logic gate parameter for the prevention of error is the
   a. width of the voltage band representing logic 1
   b. width of the voltage band representing logic 0
   c. power supply voltage
   d. gap between the highest logic 1 voltage and the lowest logic 0 voltage
   e. gap between the lowest logic 1 voltage and the highest logic 0 voltage

   The correct answer above is **E**.

5. A revised version of the Lab01 take home problem has been assigned. You are to rebuild the
    XNOR gate using only 2-input NAND gates, with one difference. Because you are
    practicing to qualify to compete in the Olympic Games, you must operate the circuit using
    the tip of an epée while in a fencing pose as shown at the web link and standing far enough
    away from your breadboard that by stretching you can only just reach the circuit with the tip
    of the epée.
    See https://en.wikipedia.org/wiki/Épée - /media/File:Fencing_epee_valid_surfaces.svg to
    become familiar with an epée.
    Can you re-build the XNOR circuit using fewer than 5 two-input NAND gates as was done
    originally in lab? If yes, describe why and how.

    Yes, it is possible with only **four** NAND gates! This is because of the situation the user is in
    (training for an Epee Olympic Tournament and only using the single point of the blade),
    disallowing him to push more than own button down at once. Due to this, he will never be
    able to replicate an output where both A and B (switches A and B) are pressed down
    simultaneously. Instead, the Epee champion must choose to press none or only one of the two
    at any given time. Taking this into consideration we can modify the circuit to only replicate
    this output, ignoring output where A=1 and B = 1. The circuit is drawn below (using
    draw.io).