Project

CMPEN 331 – Computer Organization and Design

Due Thursday December 7, 2017 at 11:59 pm (Drop box on Canvas)

Late submission is not accepted and will result in not getting any credits for the project

In this project, the students will implement a pipeline CPU using the Xilinx design package for FPGAs. You can use any information available in previous labs if needed.

1. **Pipelining**

   As described in lab 4

2. **Circuits of the Instruction Fetch Stage**

   As described in lab 4

3. **Circuits of the Instruction Decode Stage**

   As described in lab 4

4. **Circuits of the Execution Stage**

   As described in lab 5

5. **Circuits of the Memory Access Stage**

   As described in lab 5

6. **Circuits of the Write Back Stage**

   As described in lab 6

   In order to focus our attention on the WB stage easily, the baseline CPU shown in Figure 1 is redrawn by putting the register file on the WB stage where the execution result of an instruction is written as shown in Figure 2. The state of the art content can be read correctly in the ID stage after it is written at the end of its WB stage. Data hazards occur in the code example shown in Figure 3. **One solution that you need to do is to force these instructions to wait until the register $3 is updated by the first instruction. This waiting is called a pipeline stall**

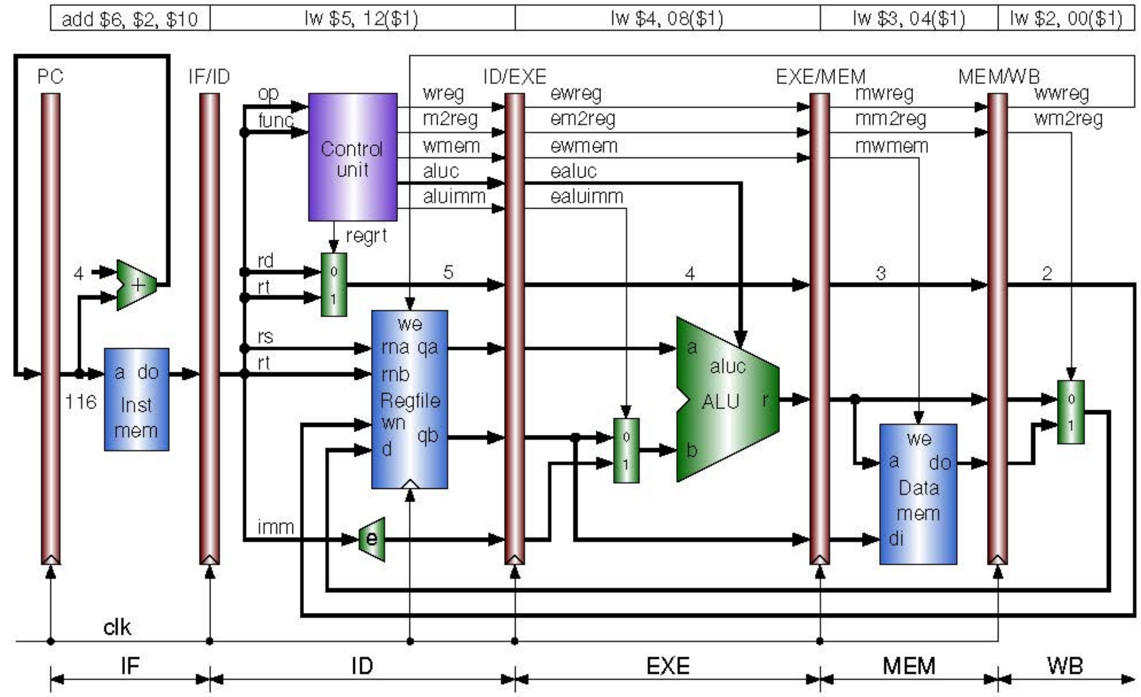


Figure 1 Pipeline write back (WB) stage

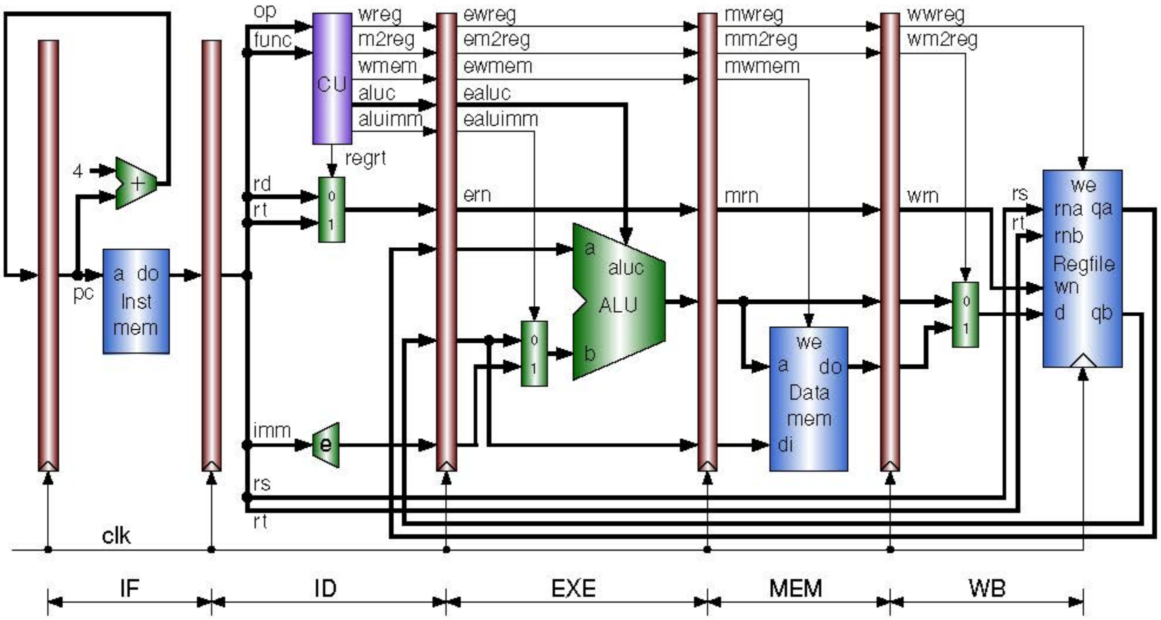


Figure 2 Writing result to the register file in the write back stage

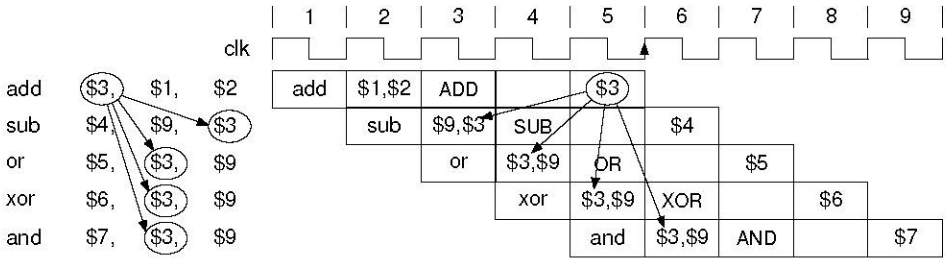


Figure 3 Data hazard examples

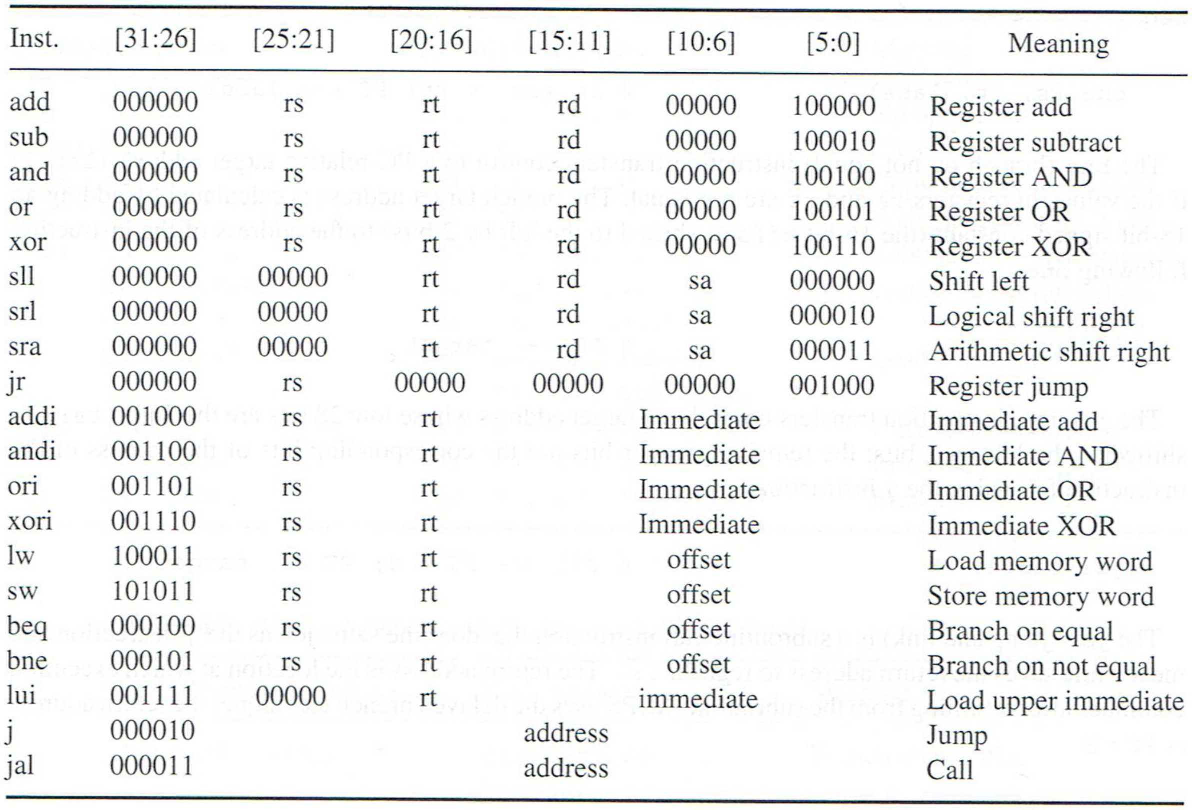
7. Table 1 lists the names and usages of the 32 registers in the register file.

Table 1 MIPS general purpose register

Register Name	Register Number	Usage
$zero	0	Constant 0
$at	1	Reserved for assembler
$v0, $v1	2, 3	Function return values
$a0 - $a3	4 – 7	Function argument values
$t0 - $t7	8 – 15	Temporary (caller saved)
$s0 - $s7	16 – 23	Temporary (callee saved)
$t8, $t9	24, 25	Temporary (caller saved)
$k0, $k1	26, 27	Reserved for OS Kernel
$gp	28	Pointer to Global Area
$sp	29	Stack Pointer
$fp	30	Frame Pointer
$ra	31	Return Address

8. Table 2 lists some MIPS instructions that will be implemented in our CPU

Table 2 MIPS integration instruction



Inst.	[31:26]	[25:21]	[20:16]	[15:11]	[10:6]	[5:0]	Meaning
add	000000	rs	rt	rd	00000	100000	Register add
sub	000000	rs	rt	rd	00000	100010	Register subtract
and	000000	rs	rt	rd	00000	100100	Register AND
or	000000	rs	rt	rd	00000	100101	Register OR
xor	000000	rs	rt	rd	00000	100110	Register XOR
sll	000000	00000	rt	rd	sa	000000	Shift left
srl	000000	00000	rt	rd	sa	000010	Logical shift right
sra	000000	00000	rt	rd	sa	000011	Arithmetic shift right
jr	000000	rs	00000	00000	00000	001000	Register jump
addi	001000	rs	rt		Immediate		Immediate add
andi	001100	rs	rt		Immediate		Immediate AND
ori	001101	rs	rt		Immediate		Immediate OR
xori	001110	rs	rt		Immediate		Immediate XOR
lw	100011	rs	rt		offset		Load memory word
sw	101011	rs	rt		offset		Store memory word
beq	000100	rs	rt		offset		Branch on equal
bne	000101	rs	rt		offset		Branch on not equal
lui	001111	00000	rt		immediate		Load upper immediate
j	000010			address			Jump
jal	000011			address			Call

9. Initialize the first 10 words of the register (Regfile block) with the following HEX values:

00000000
A00000AA
10000011
20000022
30000033
40000044
50000055
60000066
70000077
80000088
90000099

10. Write a Verilog code that implement the following instructions using the design shown in **Figure 3**. Write a Verilog test bench to verify your code: (You have to show qa and qb signals that output from the Regfile block in your simulation outputs)

11. Write a report that contains the following:
    a. Your Verilog design code. Use:
        i. Device: Zyboboard (XC7Z010- -1CLG400C)
    b. Your Verilog® Test Bench design code. Add "`timescale 1ns/1ps" as the first line of your test bench file.
    c. The waveforms resulting from the verification of your design with ModelSim showing all the signals written in and out from the MEM/WB register and the inputs to the Regfile block.
    d. The design schematics from the Xilinx synthesis of your design. Do not use any area constraints.
    e. Snapshot of the I/O Planning and
    f. Snapshot of the floor planning

g. Generate the bitstream.
h. The design should be free from errors when synthesized, implemented and generated of bit stream.
i. Connect the board and power it ON. Open a hardware session, and program the FPGA. Make sure that the micro-USB cable is connected to the JTAG PROG connector (next to the power supply connector). Make sure that the jumper on the board is set to select USB power.
j. Select the Open Hardware Manager option and click OK.
k. Click on the Open target link, then Auto Connect from the dropdown menu.
l. The Hardware Session status changes from Unconnected to the server name and the device is highlighted. Also notice that the Status indicates that it is not programmed.
m. Select the device in the Hardware Device Properties, and verify that the (.bit) file is selected as the programming file in the General tab.
n. Choose sw0 of the logic slide switches (item number 9, page 38and 39, Week 8) as an input to control the beginning of fetching of the instructions.
o. After finishing the last instruction, choose LED 0 of the logic LEDs (item number 8, page 38and 39, Week 8) to light on. You need to choose a signal as indicator that you finish your code.
p. You need to take pictures of the ZyboBoard to show that the download is done without problems and to show the configurations described in items n and o. Failed to do that will result in 15 points deduction of your project grade.

12. REPORT FORMAT: Free form, but it must be:
    a. One report per group.
    b. Have a cover sheet with identification: Title, Class, Your Names, etc.
    c. You have to write an abstract at the beginning of the project report to describe what you are doing in the project.
    d. You should include an introduction for the project explaining with diagrams the connection between all the stages and what would be the benefit of using that architecture in the computer organization field.
    e. Use Microsoft word and your report should be uploaded in word format not PDF. If you know LaTex, you should upload the Tex file in addition to the PDF file.
    f. Single spaced

13. You have to upload the whole project design file zipped with the word file.