YASHAS ND

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EXPERIENCE

Centre for Cloud Computing and Big Data, PES University August 2020 – Present
Junior Research Fellow *Bengaluru, India*

- Designing hardware accelerators on FPGAs.

CYRAN AI Solutions - Indian Institute of Technology, Delhi January 2020 – June 2020
Intern *Delhi, India*

- Worked on various applications powered by various ML architectures such as GANs, CNNs.
- Worked on software development for BUDDHI Kit, India's first AI DIY Kit.

PES University August 2019 – December 2019
Teaching Assistant *Bengaluru, India*

- Worked as a TA for the course "Digital Design and Computer Organization".
- Assistance during the lab sessions.

NVM Research Lab - Indian Institute of Technology, Delhi May 2019 – July 2019
Summer Intern *Delhi, India*

- Investigated image related, and audio-related ML techniques using GANs, CNNs, and RNNs.
- Gained in-depth experience in ML frameworks such as TensorFlow and PyTorch.

Centre for Cloud computing and Big Data February 2018 – December 2019
Research Intern *Bengaluru, India*

- Hardware design for accelerated matrix multiplication on FPGAs.
- Utilization of elastic circuits techniques for handling critical path delays.
- Full flow from High-level logic description till final FPGA configuration and testing.

NextGen Earth Labs (NGEL) December 2018 – May 2019
Project Intern *Bengaluru, India*

- Developed cloud-based back-end to manage data logging and broadcasting control messages to nodes.
- Developed front end to visualize air quality data in different areas.

PACE PES August 2017 - August 2018
Software development Intern *Bengaluru, India*

- Developed back-end for analyzing data procured from the electric vehicle.
- Development of software for vehicle control through multiple interfaces.

EDUCATION

University of Southern California August 2021 - Present
Graduate *LA, CA, USA*

Majors in Computer Engineering. GPA : **4.0** / **4.0**
- EE 457 Computer Systems Organization - Prof. Gandhi Puvvada
- EE 477 MOS VLSI

PES University August 2016 - November 2020
Undergraduate *Bengaluru, India*

Specialization in *Systems and Core Computing*.
Majors in Computer Science and Engineering. CGPA : **9.44** / **10**
Minors in Electronics and Communication Engineering.

Manasarovar Pushkarini Vidyashram Pre-University College August 2014 - May 2016
Pre-University study (12th grade) *Mysuru, India*

Focus on Computer Science, Physics, Chemistry, and Mathematics. Score: 97%.

Mahajana Public School (Under CBSE of India) August 2010 - May 2014
10th-grade *Mysuru, India*

Score: **10/10 CGPA**

PATENTS

- "*Elastic Pipelines for Data Processing. Application number 201941028170*" filed at the Indian patent office.
  Inventors: Reetinder Sidhu, Vaibhav BV, **Yashas Nagavane Dattatreya**, Rachana Aithal KR.
- "*A system and method for real-time correction of collision-free flight paths of flying objects. Application number 201941047692*" filed at the Indian patent office.
  Inventors: Antony Louis Piriyakumar Douglas, **Yashas Nagavane Dattatreya**, Vivek Partal, Devashish Satyanarayan Vaishnav.

PAPERS AND PRESENTATIONS

- "*Hardware Accelerated Matrix Multiplication using a 400 MHz Systolic Array on a CPU+FPGA Platform.*" by Reetinder Sidhu, **Yashas ND**, Vishal Rao, Rachana Aithal, Vennela Katasani, Sneha Rao GR, and Vishal S. Poster presentation at 33rd VLSI Design Conference 2020. Awarded the **best poster paper award in the user design track category**.

PROJECTS

- **Dhwani** An *English* to *Indic* language phonetic conversion engine.
- **Digital Design for Regular expression matching on FPGAs and implementation on PYNQ ZYNQ board:** Designed circuit in Xilinx Vivado and tested using IPython framework on JupyterNotebook.
- **Third-I-v2.0:** Implemented a user-space file system on Linux using FUSE. Further, implemented extended functionalities such as soft-links and hard-links in operations.
- **Compiler for generating object code from parsing JavaScript code:** Built using "lex" and "yacc" tools, implemented iterative backend optimizer for object code optimization.
- **Demonstrative CPU design:** Designed various parts such as ALU, Register File, Program Counter, and Control Unit. Integrated all of these and tested for functional correctness of the design.

ACHIEVEMENTS

- Recipient of *Prof. CNR Rao Merit Scholarship* from PES University from the past three years.
- Recipient of "Distinction award" for securing First class with Distinction in multiple semesters from PES University.
- **Ranked 290 out of 170,000** candidates in State level Engineering competitive Exam (KCET 2016).
- Completed PACE Project of *Personal Urban Mobility Access*, organized by General Motors, PACE Global Annual Forum, Warren, Michigan; July 2018.