YASHAS NAGAVANE DATTATREYA

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EXPERIENCE

Centre for Cloud Computing and Big Data, PES University August 2020 – June 2021
RTL Design Engineer (Junior Research Fellow) *Bengaluru, India*

Project 1: Hardware accelerated matrix multiplier

- Wrote RTL for a 64 × 64 cached matrix-multiplication accelerator on Intel Stratix 10 FPGA.
- Designed recursive high-speed full-cycle LFSRs for use in caching FIFOs.
- Interfaced multiplier AFU with Intel CCI-P (Core Cache Interface). This achieves state-of-the-art throughput of 2.5 TFLOPS at 309MHz.

Project 2: Cluster monitoring and controlling tool supporting

- Unified graphical view of cluster machines, User login activities, Remote reboot/shutdown support, RAM and CPU usage monitoring.

Centre for Cloud Computing and Big Data, PES University February 2018 – August 2020
Digital Logic Design Intern *Bengaluru, India*

- Wrote RTL for a 16 × 16 matrix-multiplication accelerator on Intel Arria 10, CPU+FPGA platform.
- Improved FMAX by 60% from 250MHz to 400MHz over initial implementation Resulting in a peak of 204.8 GFLOPS.

This was awarded the "Best Poster Presentation" award at the 2020 VLSID conference.

CYRAN AI Solutions - Indian Institute of Technology, Delhi January 2020 – June 2020
Intern *Delhi, India*

- Worked on various applications powered by various ML architectures such as GANs, CNNs.
- Worked on software development for BUDDHI Kit, India's first AI DIY Kit.

PES University August 2019 – December 2019
Teaching Assistant *Bengaluru, India*

- Worked as a TA for the course "Digital Design and Computer Organization".
- Assistance during the lab sessions.

NVM Research Lab - Indian Institute of Technology, Delhi May 2019 – July 2019
Summer Intern *Delhi, India*

- Investigated image related, and audio-related ML techniques using GANs, CNNs, and RNNs.
- Gained in-depth experience in ML frameworks such as TensorFlow and PyTorch.

PACE PES August 2017 - August 2018
Software development Intern *Bengaluru, India*

- Developed back-end for analyzing data procured from the electric vehicle.
- Development of software for vehicle control through multiple interfaces.

EDUCATION

University of Southern California August 2021 - Present
Graduate *LA, CA, USA*

Majors in Computer Engineering. GPA : **4.0** / **4.0**

- EE 557 Computer Systems Architecture
- EE 577a VLSI System Design - 1
- EE 457 Computer Systems Organization - Prof. Gandhi Puvvada
- EE 477 MOS VLSI

PES University August 2016 - November 2020
Undergraduate *Bengaluru, India*

Specialization in *Systems and Core Computing*.
Majors in Computer Science and Engineering. CGPA : **9.44 / 10**
Minors in Electronics and Communication Engineering.

Manasarovar Pushkarini Vidyashram Pre-University College August 2014 - May 2016
Pre-University study (12th grade) *Mysuru, India*

Focus on Computer Science, Physics, Chemistry, and Mathematics. Score: 97%.

Mahajana Public School (Under CBSE of India) August 2010 - May 2014
10th-grade *Mysuru, India*

Score: **10/10 CGPA**

PATENTS

- "*Elastic Pipelines for Data Processing. Application number 201941028170*" filed at the Indian patent office.
  Inventors: Reetinder Sidhu, Vaibhav BV, **Yashas Nagavane Dattatreya**, Rachana Aithal KR.
- "*A system and method for real-time correction of collision-free flight paths of flying objects. Application number 201941047692*" filed at the Indian patent office.
  Inventors: Antony Louis Piriyakumar Douglas, **Yashas Nagavane Dattatreya**, Vivek Partal, Devashish Satyanarayan Vaishnav.

PAPERS AND PRESENTATIONS

- "*Hardware Accelerated Matrix Multiplication using a 400 MHz Systolic Array on a CPU+FPGA Platform.*" by Reetinder Sidhu, **Yashas ND**, Vishal Rao, Rachana Aithal, Vennela Katasani, Sneha Rao GR, and Vishal S. Poster presentation at 33rd VLSI Design Conference 2020. Awarded the **best poster paper award in the user design track category**.

PROJECTS

RISC-V cores supporting rv32i instruction set
System Verilog | C++ | Verilator | GTKWave

Designing RISC-V cores supporting the rv32i instruction set.

Simulation of supporting modules such as L1 Instruction and data cache, and stalls.

Supporting modules written in C++ and simulated using Verilator, and debugged using GTKWave.

5-stage pipelined MIPS Processor Design
Verilog | ModelSim

Designed a pipelined 5-stage CPU with an internally forwarding register file to execute MIPS R-type, Branch, and mem instructions using RTL (Register Transfer Level) coding in Verilog and simulating on ModelSim.

Design included forwarding and hazard detection unit to prevent the Read-After-Write data dependencies by stalling for the early and late branch designs.

Digital Spiking Neuron Design
Cadence Virtuoso

Designed and implemented schematic and layout of a digital circuit that mimics a spiking neuron in with Cadence Virtuoso.

Simulated the digital spiking neuron on SPECTRE and performed the timing analysis of the signals. Validated the physical design with DRC and LVS and optimized it to have a minimum area-delay product.

R-LMON Systems Monitoring Tool for cluster systems
Bash | Python | JavaScript

Cluster monitoring and controlling tool. Used at Center for Cloud Computing and Big Data, PES University, and now at AMD Bangalore.

Unified graphical view of cluster machines, User login activities, Remote reboot/shutdown support, RAM and CPU usage monitoring.

High-speed full-cycle recursive Linear-Feedback-Shift-Registers
iverilog | GTKWave

Wrote recursive HLS design for a full-cycle / arbitrary-cycle Linear Feedback Shift Register.

Test scripts in Python for functional verification.

Written in Flo-Hask HLS framework in Haskell, developed by Dr. Reetinder Sidhu.

Simulation and waveform viewing done was done using iverilog, and GTKWave.

Regular expression matching on FPGA
Vivado | Verilog | iverilog | GTKWave

Non-deterministic Finite Automata-based regular expression matching.

Tested on PYNQ ZYNQ FPGA board.

Written in Flo-Hask HLS framework in Haskell, developed by Dr. Reetinder Sidhu.

Third-I-v2.0:
C | FUSE

Implemented a user-space file system on Linux using FUSE.

Implemented extended functionalities such as soft-links and hard-links in operations.

Dhwani
Python

An *English* to *Indic* language phonetic conversion tool.

ACHIEVEMENTS

- **MS Honors Program** admitted to the MS Honors program at USC where $< 5\%$ of students are admitted for maintaining a 4.0 GPA.
- Recipient of *Prof. CNR Rao Merit Scholarship* from PES University from the past three years.
- Recipient of "Distinction award" for securing First class with Distinction in multiple semesters from PES University.
- **Ranked 290 out of 170,000** candidates in State level Engineering competitive Exam (KCET 2016).
- Completed PACE Project of *Personal Urban Mobility Access*, organized by General Motors, PACE Global Annual Forum, Warren, Michigan; July 2018.