Planning Document

Hamming Error Correction Module

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Assignee map:
A: Aditya
B: Omkar

Color codes:
Green: Completed.
Light red: Slipped, but plan to catch up exists.
Red: Slipped, no further information.
Yellow: Requires Vijay uncle's time. Is always paired with a date **and** time to meet.

1 Specification

1.1 Theory

Prerequisites: Basic linear algebra, group theory.
Assignee: A.
Process: Study theory from Error Control Coding (Lin), use relevant parts on linear and Hamming codes to write theory section.
Finish condition: Section written and review passed.
Deadline: <2022-06-11 Sat>
Completed: <2022-06-11 Sat>

1.2 Interface

Prerequisites: Understanding of I/O interface of Hamming module.
Assignee: B.
Process: Figure out how to "read" data stream to encode; latency and clock frequency required.
Finish condition: Section written and review passed.
Deadline: <2022-06-12 Sun>
Completed: <2022-06-16 Thu>

1.2.1 Timing Diagrams

Prerequisites: Understanding expected behavior of Hamming module.
Assignee: ?
Process: Making timing diagrams for expected inputs to Hamming module.
Finish condition: Section written and review passed.
Deadline: <2022-06-12 Sun>

1.3 Review

Prerequisites: Specification is in a complete state.
Assignee: With Vijay uncle.
Process: Review spec, correct errors.
Finish condition: Spec passes all reviews.
Deadline: <2022-06-12 Sun>
Completed: <2022-06-17 Fri>

2 Paper Design

2.1 Encoder

Prerequisite: Specification complete.
Assignee: A
Process: Make paper design of functions and FSMs used to implement parameterized Hamming encoder.
Finish condition: Ready to write RTL, encoder matches specification.
Deadline: <2022-06-13 Mon>
Completed: <2022-06-13 Mon>

2.2 Decoder

Prerequisite: Specification complete.
Assignee: B
Process: Make paper design of functions and FSMs used to implement parameterized Hamming decoder.
Finish condition: Ready to write RTL, decoder matches specification.
Deadline: <2022-06-19 Sun>

3 RTL

3.1 Encoder

Prerequisite: Paper design of encoder complete.
Assignee: A
Process: Write Verilog for the paper design, make sure specification is matched.
Finish condition: RTL passes basic "manual" testing.
Deadline: <2022-06-14 Tue>
Completed: <2022-06-15 Wed>

3.2 Decoder

Prerequisite: Paper design of decoder complete.
Assignee: B
Process: Write Verilog for the paper design, make sure specification is matched.
Finish condition: RTL passes basic "manual" testing.

Deadline: <2022-06-19 Sun>

3.3 Code Review for RTL

Prerequisite: RTL complete.
Assignee: With Vijay uncle
Process: Make sure Verilog is correct, synthesizable, and follows coding guidelines.
Finish condition: Passes review.
Deadline: <2022-06-20 Mon 19:00>

4 Testing

4.1 Testing Theory

Prerequisite: None.
Assignee: With Vijay uncle
Process: Learn verification environments, test plans, tests, verification reviews.
Deadline: <2022-06-19 Sun 14:00>

4.2 Testing Plan

Prerequisite: Learn how to write tests.
Assignee: ?
Process: Create testing plan for RTL.
Finish condition: Tests ready to write.
Deadline: <2022-06-15 Wed>

4.3 Encoder

Prerequisite: Encoder RTL complete.
Assignee: A
Process: Write a testbench for Hamming encoder, make sure written module passes all tests (directed and randomized).
Finish condition: Passes all tests.
Deadline: <2022-06-18 Sat>

4.4 Decoder

Prerequisite: Decoder RTL complete.
Assignee: B
Process: Write a testbench for Hamming decoder, make sure written module passes all tests (directed and randomized).
Finish condition: Passes all tests.
Deadline: <2022-06-18 Sat>

5 Review

Prerequisites: Module built, passing all tests.
Assignee: With Vijay uncle.
Process: Review all work, make changes as required.
Finish condition: Passes review.
Deadline: <2022-06-20 Mon 19:00>