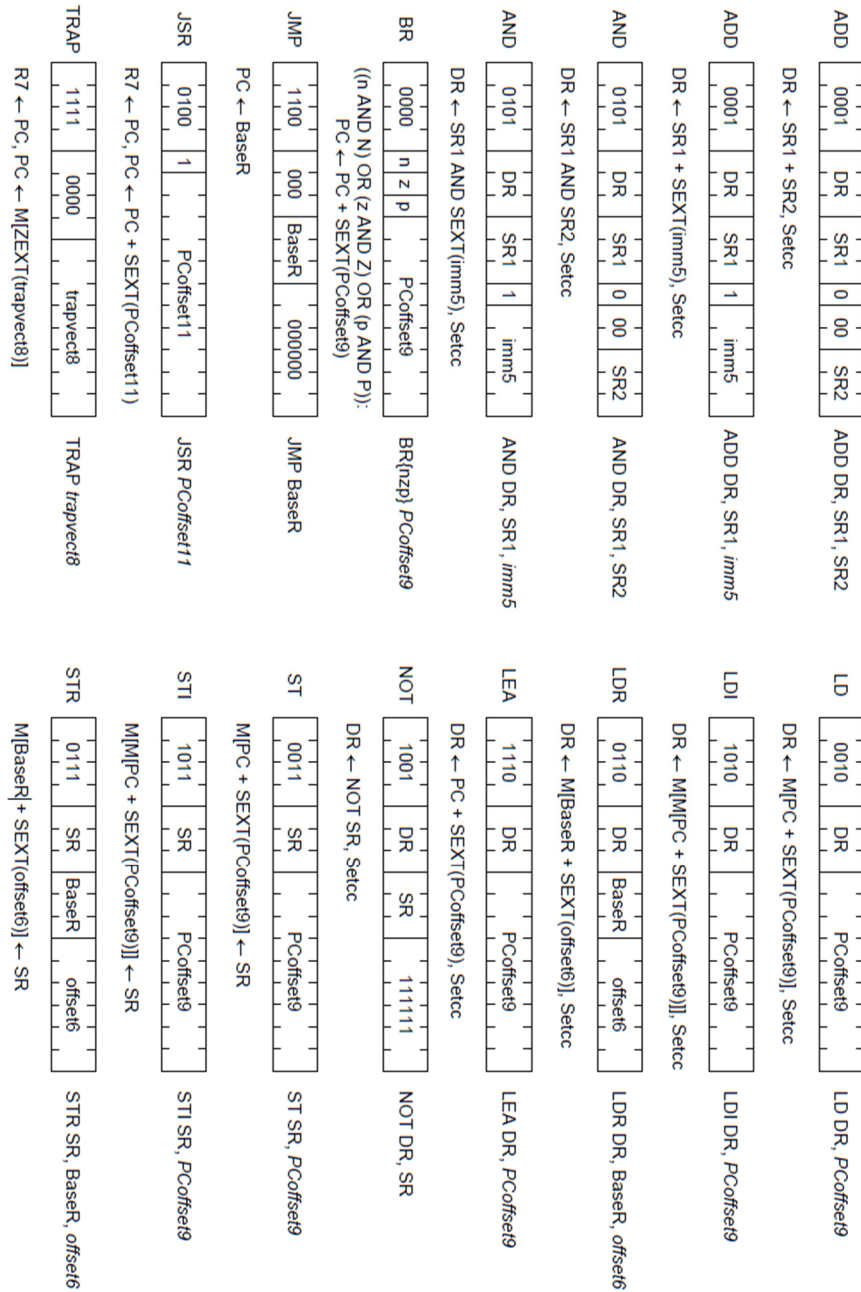
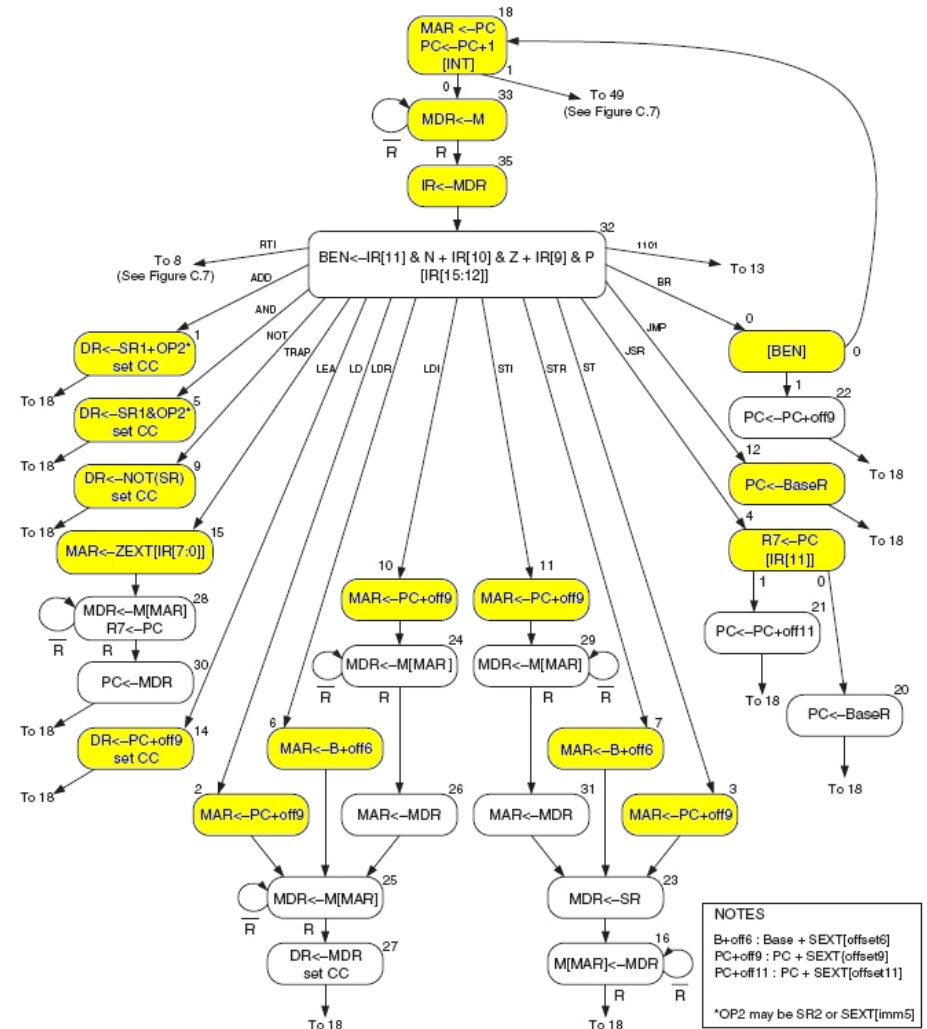


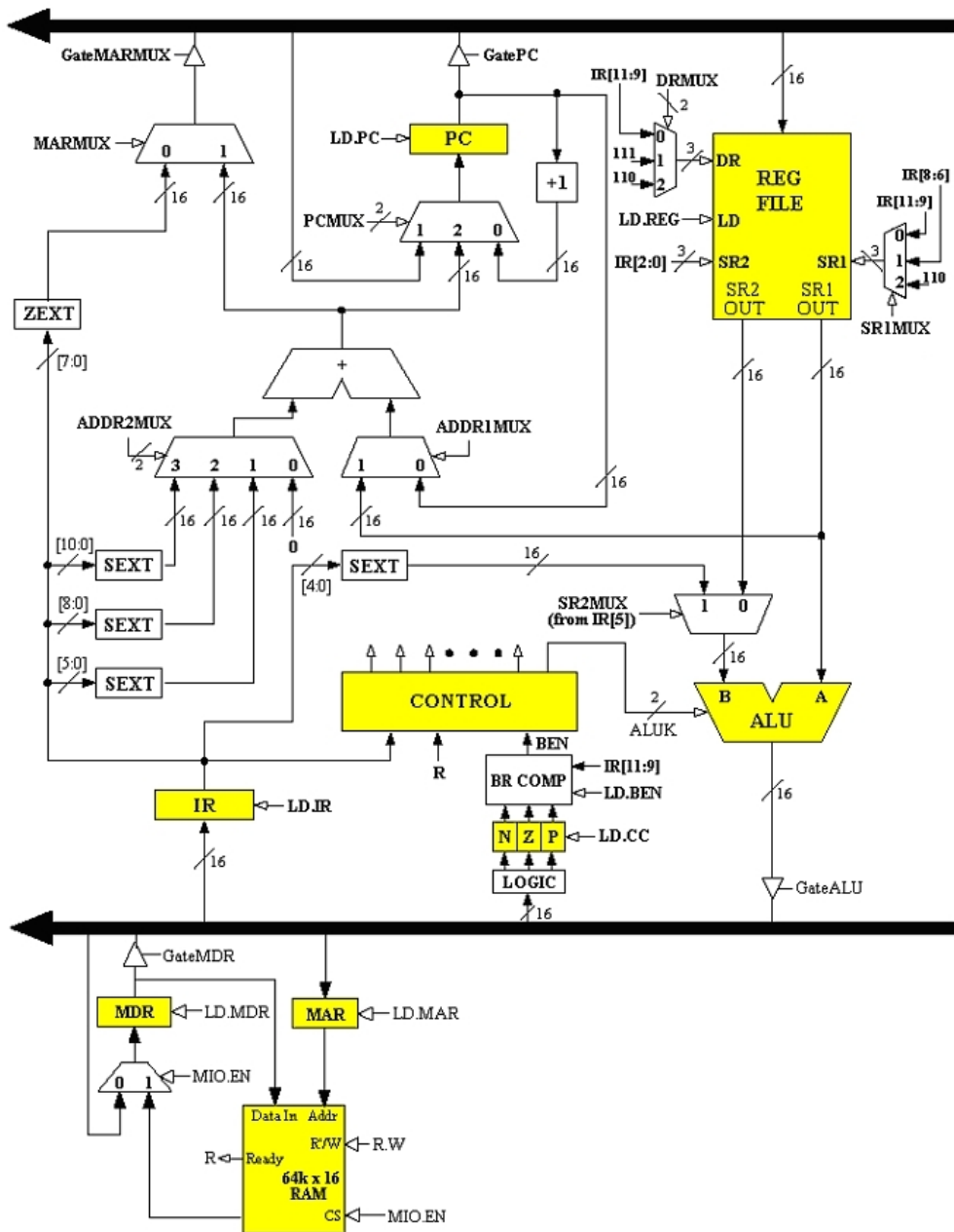
LC-3 Instructions



NOTES: RTL corresponds to execution (after fetch!); JSRR not shown

LC-3 FSM





Signal	Description	Signal	Description
LD.MAR	= 1, MAR is loaded	LD.CC	= 1, updates status bits from system bus
LD.MDR	= 1, MDR is loaded	GateMARMUX	= 1, MARMUX output is put onto system bus
LD.IR	= 1, IR is loaded	GateMDR	= 1, MDR contents are put onto system bus
LD.PC	= 1, PC is loaded	GateALU	= 1, ALU output is put onto system bus
LD.REG	= 1, register file is loaded	GatePC	= 1, PC contents are put onto system bus
LD.BEN	= 1, updates Branch Enable (BEN) bit		
MARMUX	= 0, chooses ZEXT $IR[7:0]$ = 1, chooses address adder output	MIO.EN	= 1, Enables memory, chooses memory output for MDR input = 0, Disables memory, chooses system bus for MDR input
ADDR1MUX	= 0, chooses PC = 1, chooses reg file $SR1$ OUT	R.W	= 1, M[MAR] < MDR when MIO.EN = 1 = 0, MDR < M[MAR] when MIO.EN = 1
ADDR2MUX	= 00, chooses "0...00" = 01, chooses SEXT $IR[5:0]$ = 10, chooses SEXT $IR[8:0]$ = 11, chooses SEXT $IR[10:0]$	ALUK	= 00, ADD = 01, AND = 10, NOT A = 11, PASS A
PCMUX	= 00, chooses PC + 1 = 01, chooses system bus = 10, chooses address adder output	DRMUX	= 00, chooses $IR[11:9]$ = 01, chooses $IR[8:6]$ = 10, chooses "110"
SR1MUX	= 00, chooses $IR[11:9]$ = 01, chooses $IR[8:6]$ = 10, chooses "110"		